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VLSI Read-Out System for Knife-Edge Detectors

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VLSI READ-OUT SYSTEM

FOR

KNIFE-EDGE DETECTORS

See back page

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SSC Laboratory

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1. System configuration

The read-out system consists of 4 basic blocks shown in Figure 1. The first block is analog, and consists of a preamp-comparator combination. The preamp is designed to provide sufficient amplification for the incoming signals to trip the comparator. The nominal input signal is $2x10^5$ e^- on a 5 pF strip capacitance. The rise and fall time of the signal are 10 ns, its pulse width is 20 ns. This is equivalent to an input current of $3.2x10^{-14}$ C/30 ns ≈ 1.07 μA. The comparator is designed to be sensitive to signals that are twenty times smaller.

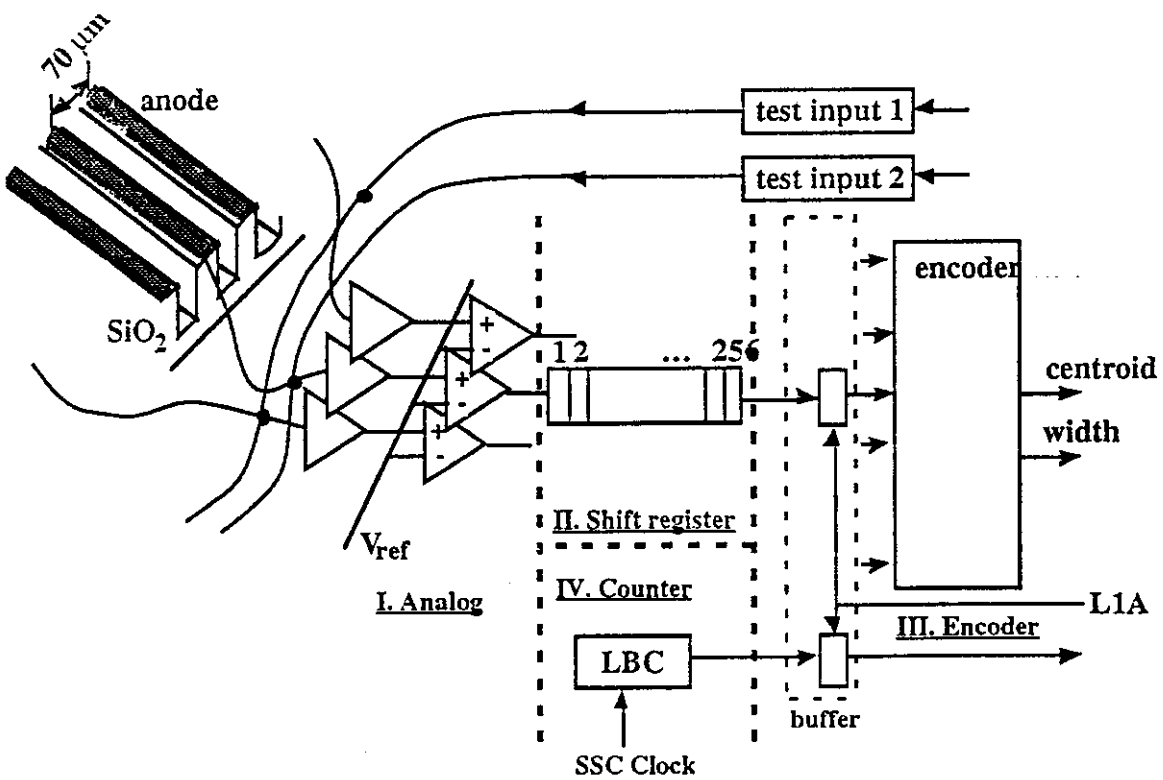


Fig. 1: Architecture of the read-out system.

Further requirements or desires are a low power dissipation, minimal slewing, minimum recovery time, and an input referred noise of less than 1000 e^-. The second

block consists of a series of latches organized as a shift register that samples the comparator and stores the result during the level 1 trigger decision time, which is currently estimated to be around 4 μs. The shifting is synchronous with the SSC clock, running at 62.5 MHz. Because the pulse width of the comparator is longer than one clock period, a '1'-suppression circuit is build into the shift register. This circuit will pass only the first '1' in a series. Upon arrival of a level 1 trigger signal, data from the shift register is made available to the third block, an encoder circuit, which encodes the input data of the parallel channels into a centroid and a width code. The encoder should be able to handle multiple hits, represented by more than one group of activated channels. The final block is an 8 bit digital counter, which performs the task of local bunch counter (LBC). Its count is latched into a buffer each time the encoder accepts new input, and is made available together with the encoded data. In this way, relative timing information is provided.

2. Preamp-comparator combination.

2a. Basics.

The large detector capacitance makes a preamp with low input impedance a necessity. This can be accomplished by using a diode connected MOSFET to receive the signal, or by using a current sensitive amplifier. Both methods are explained below. To obtain high speed and low power dissipation, a basic dilemma has to be solved. This can be illustrated for a generative voltage sensitive amplifier characterized by g_m, the transconductance of the input transistor, r_o, the output impedance and C_L, the load capacitance. The gain for this amplifier is $g_m r_o$, its bandwidth (BW) is given by $1/(r_o C_L)$. Achieving a BW of 10 MHz and a gain of 200 requires for C_L = 50 fF that $g_m > 625$ μS and that $r_o < 320$ kΩ. If the input transistor is biased in strong inversion, then $g_m = \sqrt{2\beta I_{ds}}$, with $\beta = \mu C_{ox}\frac{W}{L}$. In the latter formula, μ is the minority carrier surface mobility in $cm^2/(Vs)$, C_{ox} is the oxide capacitance in F/cm^2 and W/L is the width to length ratio of the MOS device. For a typical 1.2 μm CMOS process, $\beta \approx 47\frac{W}{L}$ μS, resulting in the requirement $I_{ds}\frac{W}{L} > 4.2$ mA. If for example W/L = 100, then $I_{ds} > 42$ μA, which contradicts with the restrictions on power dissipation.

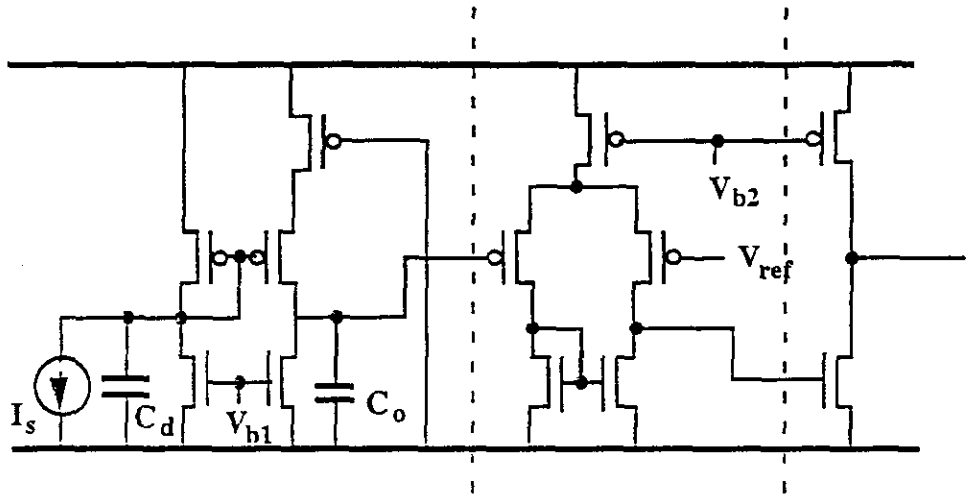


Fig. 2: preamp with diode connected input transistor.

The first method to achieve low imput impedance is illustrated in Figure 2. The diode connected MOSFET M1 takes care of resetting the strip capacitance, M2 is the input transistor for the preamp. The gain for this configuration is limited to approximately 40. A problem with the circuit is the recovery of dc node voltages after applying an input pulse. The recovery time can only be shortened by increasing the bias current. This however decreases the gain. In order to have an input range of 0.05 to 1 μA, the preamp has to be followed by an additional amplifier stage and a high gain comparator. A further disadvantage of the current-mirror input is an increase in input referred noise due to the use of a current mirror.

2b. *Folded cascode.*

The second solution is a current sensitive amplifier. Figure 3 depicts the design in the Westinghouse n-well process. A 'Half Folded Cascode' (HFC) configuration is used as preamp. Table 1 gives the transistor dimensions corresponding to Figure 3. The preamp-comparator combination uses ± 1.5 V as supply voltage. Only one additional bias voltage (V_b = 0.5 V) is needed.

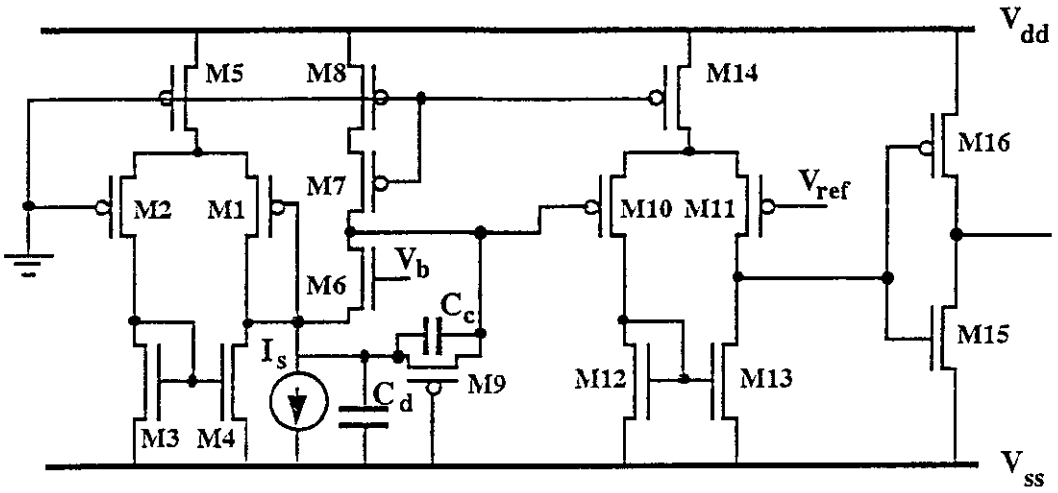


Fig. 3: Current sensitive amplifier combined with comparator and output buffer, and to be implemented in the 1.2 μm n-well Westinghouse process.

Table 1: Transistor sizes and dc parameters for the HFC-comparator circuit

Transistor	W/L	I_{ds} [μA]	g_m [μS]	g_{ds} [μS]
M1 = M2	500/2	10.7	338.0	19.5
M3	20/1.2	10.7	133.6	0.1
M4	40/1.2	20.6	266.4	0.2
M5	10/2	21.4	59.0	4.2
M6	4/1.2	9.9	55.9	0.2
M7	4/1.2	9.9	36.2	1.1
M8	10/2	9.9	16.8	48.9
M9	3/40	0.0	0.0	0.93
M10 = M11	40/1.2	8.75	11.3	3.4
M12 = M13	5/1.2	8.75	59.1	0.15
M14	6/1.5	17.5	44.6	8.4
M15	4/1.2	11.9	9.5	71.3
M16	8/1.2	11.9	90.3	0.19

For stability reasons a small compensation capacitor C_c of 50 fF is needed in parallel with the feedback resistor. If this capacitor is eliminated, the ac response shows peaking around 10 MHz. The frequency response of the preamp, V_{out}/I_{in} and the phase shift, with and without C_c are shown in Figure 4. The total power dissipation for the circuit is 181 µW. Figure 5 illustrates the magnitude of the signals for a 0.05 µA input signal. Figure 6 shows the slewing, recovery time, double pulse resolution and width of the output pulse for the circuit. The double pulse resolution (DPR) is defined as the distance of two input pulses that appear as two separate pulses at the output. By increasing the size of M13 (increasing current) the slewing for small input signals can be improved. However, this would be at the cost of DPR. The recovery time and slewing can be changed by adapting the switching threshold voltage of the output inverter. By lowering the threshold voltage the slewing is decreased and the recovery time is increased.

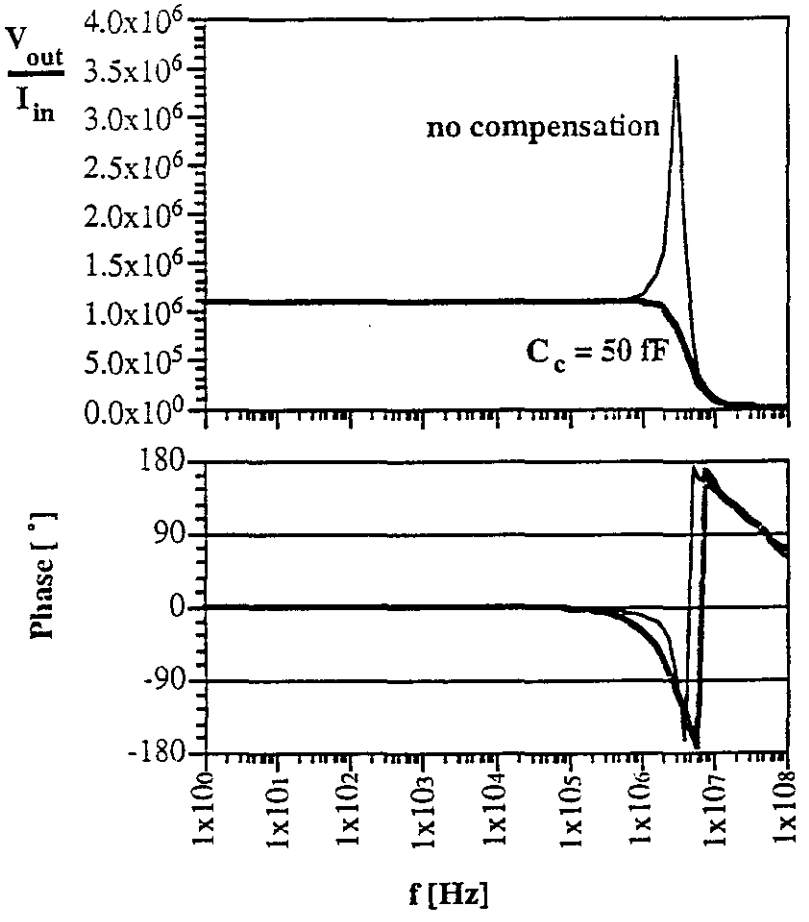


Fig. 4: Transresistance and phase of the preamp with and without compensation.

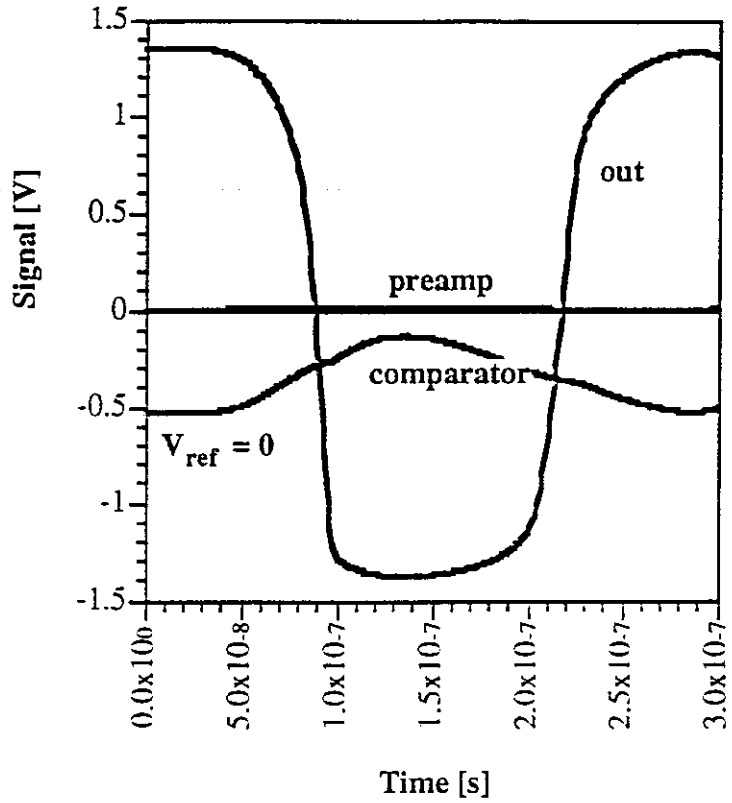


Fig. 5: Output signal of the preamp, comparator and buffer in response to a 0.05 μA input signal. The plot indicates how tiny the actual input signal is.

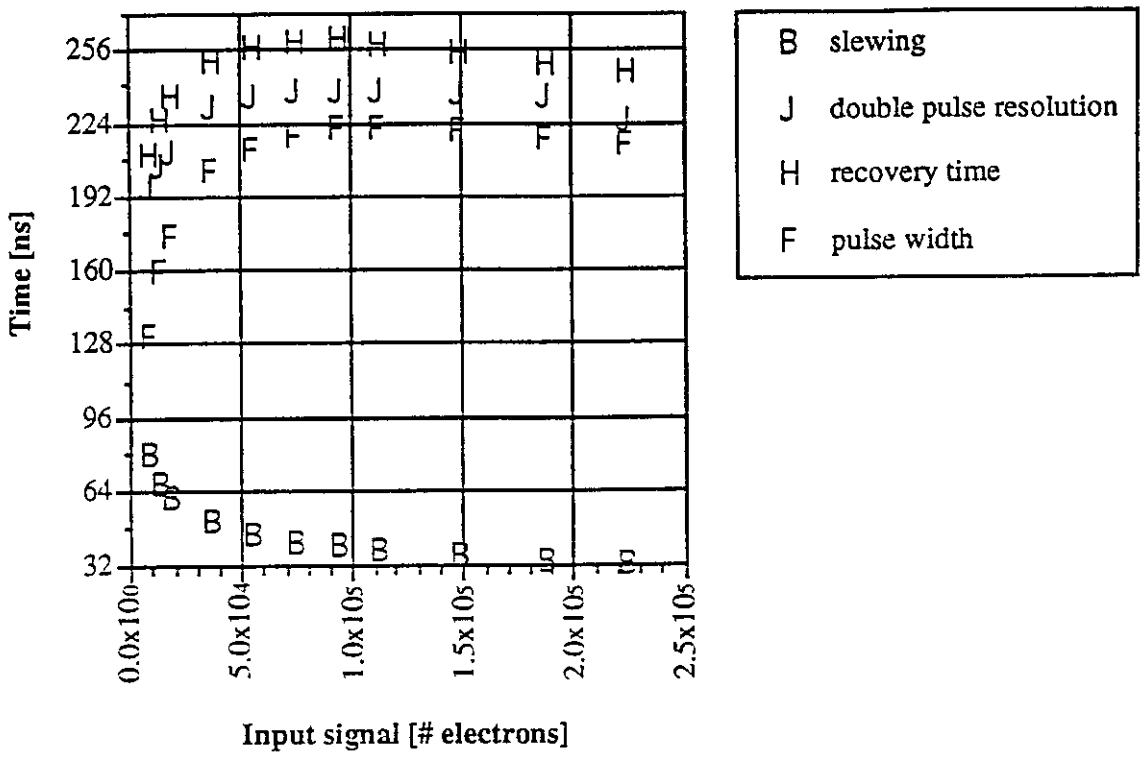


Fig. 6: Slewing, double pulse resolution, recovery time and output pulse width as a function of the input signal.

A version of the analog circuit suitable for fabrication in the UTMC p-well process is shown in Figure 7. The circuit dissipates 100 μW. Its speed is reflected by Figure 8. The transistor parameters are given in Table 2. Notwithstanding the body effect for the input devices, the same comparator is used as for the Westinghouse n-well process. The reason being the fact that this type provides a convenient dc output voltage, putting the output inverter in a region of almost zero stand-by power. A p-channel device was chosen over an n-channel device to implement the feedback resistor because of its higher resistance. C_c had to be increased to 150 fF in this circuit.

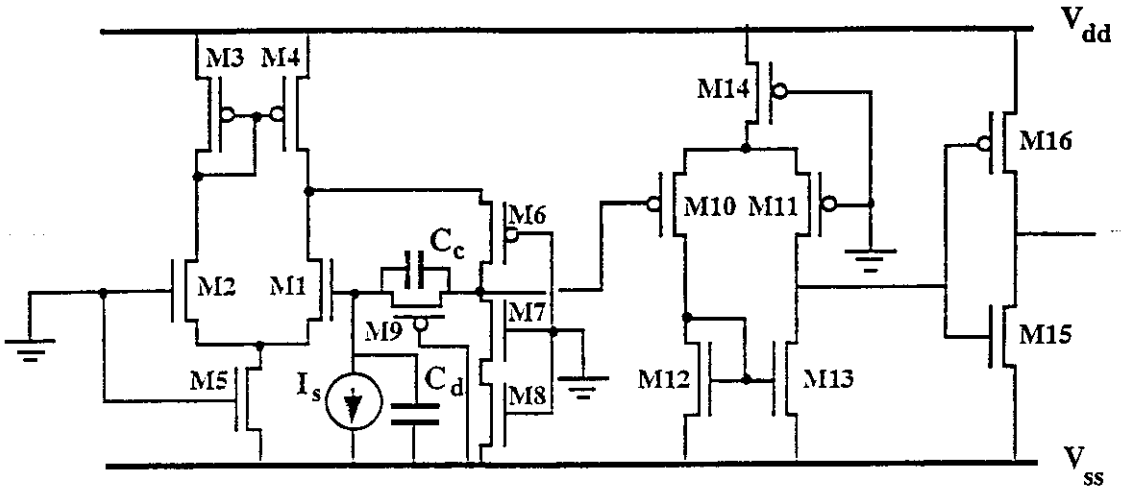


Figure 7: Analog circuitry for the 1.2 μm p-well UTMC process.

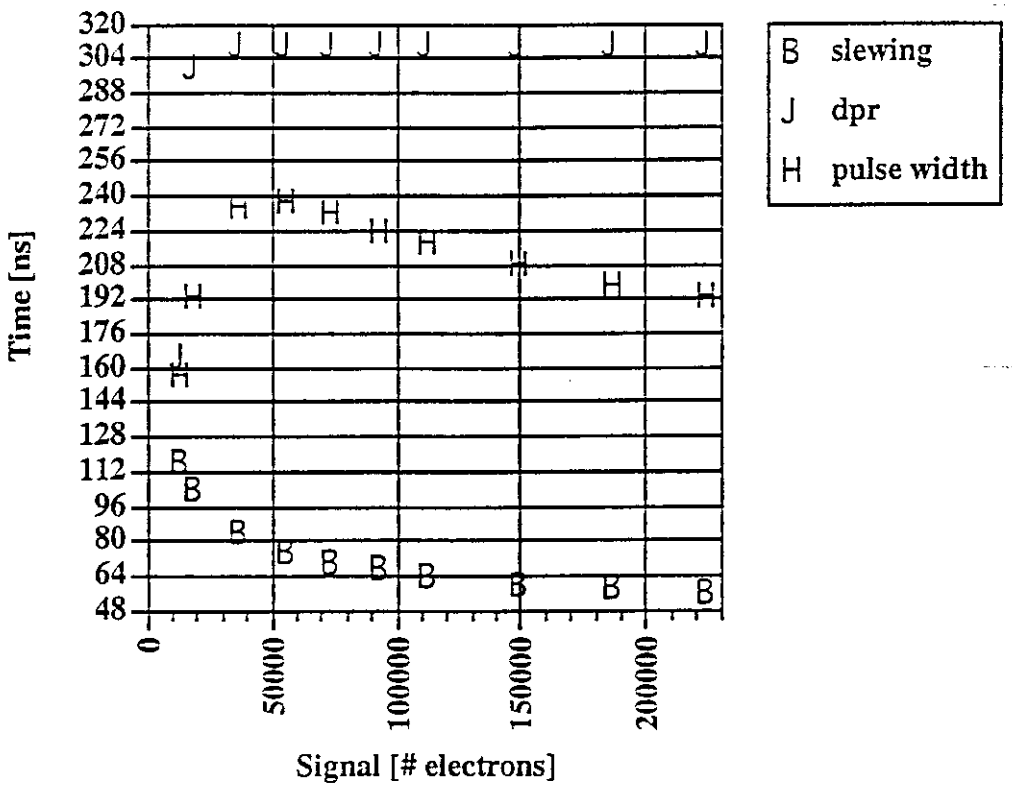


Fig. 8: Slewing, double pulse resolution, recovery time and output pulse width for the circuit of Figure 7.

Table 2: Transistor sizes and dc parameters for the UTMC HFC-comparator circuit

Transistor	W/L	I_{ds} [μA]	g_m [μS]	g_{ds} [μS]
M1 = M2	250/2	3.6	235.0	0.17
M3	4/2	3.6	18.4	0.03
M4	11.2/2	10.8	53.7	0.09
M5	4/8	7.2	18.8	136 pS
M6	15/1.2	7.2	77.3	1.15
M7	15/1.2	7.2	109.4	0.59
M8	4/8	7.2	18.8	136 pS
M9	4/25	0.0	0.0	1.29
M10 = M11	40/1.5	9.1	119.5	0.59
M12 = M13	10/1.2	9.1	98.9	0.54
M14	6/2	18.2	38.0	15.7
M15	4/1.2	2.0	29.8	0.16
M16	4/1.2	2.0	1.35	170.9

2c. Noise performance.

The noise voltage due to the amplifier only and measured at the output, v_N^2, is given by:

$$v_N^2 \approx BW \left[2\, v_1^2 + 2 \left(\frac{g_{m3}}{g_{m1}}\right)^2 + \left(\frac{g_{m8}}{g_{m1}}\right)^2 v_8^2 + v_9^2 \right] \qquad (1)$$

where v_i^2 is the equivalent input noise voltage of transistor M_i

$$v_i^2 = \frac{8}{3}\frac{kT}{g_{mi}} \, [V^2/Hz] \qquad i \neq 9$$

$$v_i^2 = 4\,\frac{kT}{g_{dsi}} \, [V^2/Hz] \qquad i = 9$$

In equation (1) the noise due to the feedback resistor, v_9^2, is dominant. For the preamp the transimpedance is determined by the feedback resistor:

$$\frac{V_{out}}{I_{in}} = \frac{1}{g_{ds9}} \qquad (2)$$

As a result the input referred noise current is given by:

$$i_N^2 = v_N^2 g_{gs9}^2 \tag{3}$$

This current is equivalent to an input noise charge with shape described in the introduction of this report. The magnitude of the noise is:

$$ENC = \frac{i_N \times 30\ ns}{1.6\times10^{-19}\ C} \approx 56\ e^- \text{ rms for the Westinghouse design} \tag{4}$$

$$\approx 24\ e^- \text{ rms for the UTMC design}$$

An HSPICE simulation indicates a somewhat lower number.
The main contribution to the total noise is the kTC noise of the input capacitance. The kTC input noise voltage is:

$$v_C = \sqrt{\frac{kT}{C_d}} \tag{5}$$

which for $C_d = 5$ pF is equivalent to:

$$ENC_C = \frac{v_C\ C_d}{1.6\times10^{-19}\ C} \approx 899\ e^-\ \text{rms} \tag{6}$$

A comparison between (4) and (6) shows that the amplifier noise is negligible.

2d. Speed improvements.

i) Recovery feedback.

Simulations show that the OTA type comparator reacts rapidly to an input signal, but requires a long recovery time, during which its output is high. The recovery time can be improved by increasing the current that discharges the output node as long as this one is high. A way to do this is shown in figure 9. This design is called 'Comparator with Recovery Feedback' (CRF). The resulting speed improvement can be seen from figures 10a and b.

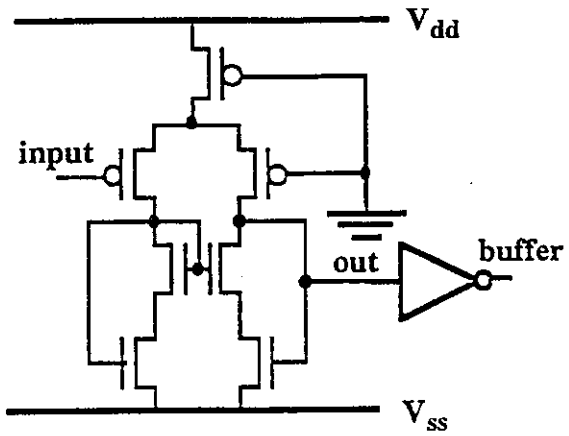


Fig. 9: OTA type comparator with recovery feedback.

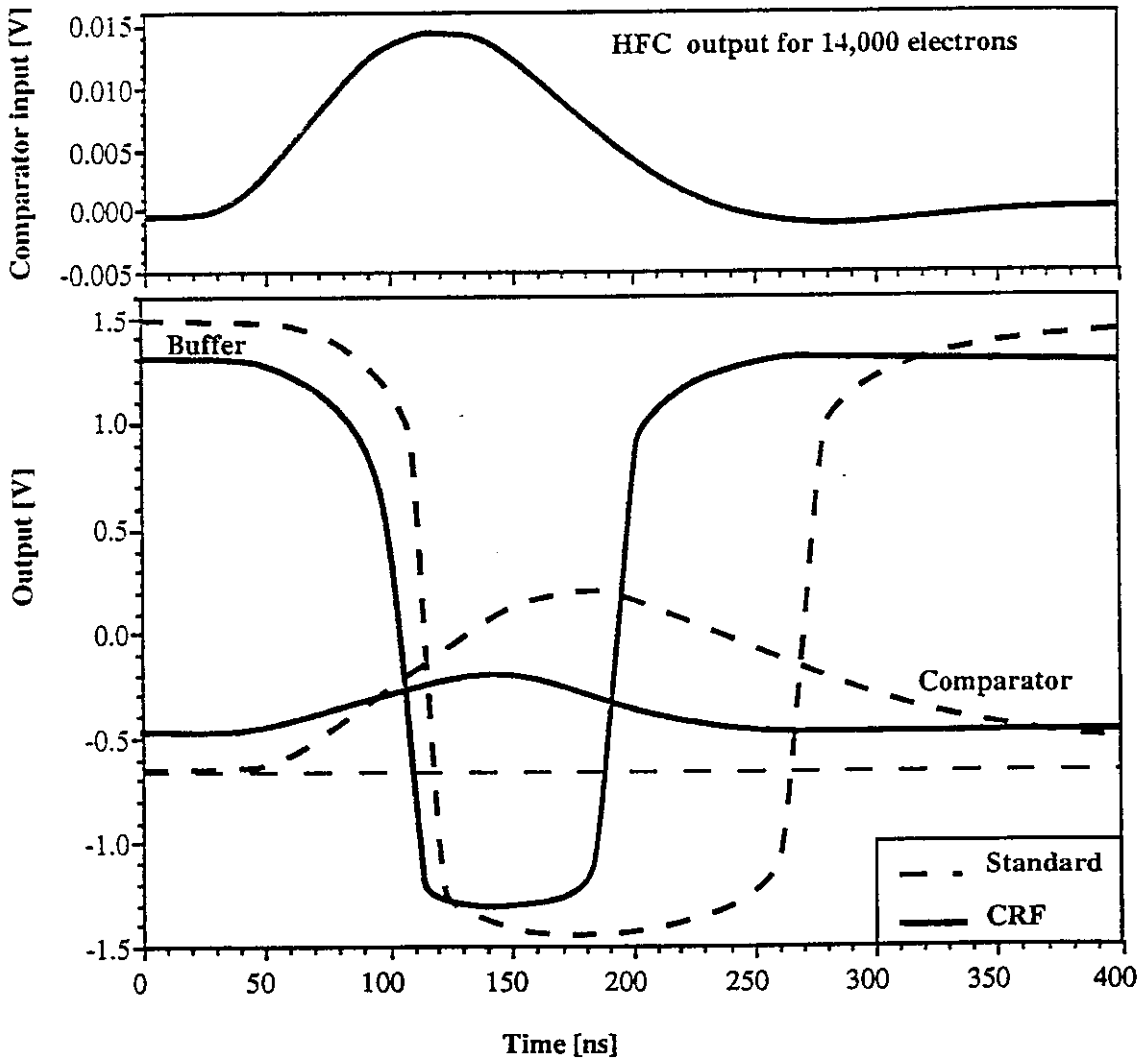


Fig. 10a: Signal shape of the original and improved design.

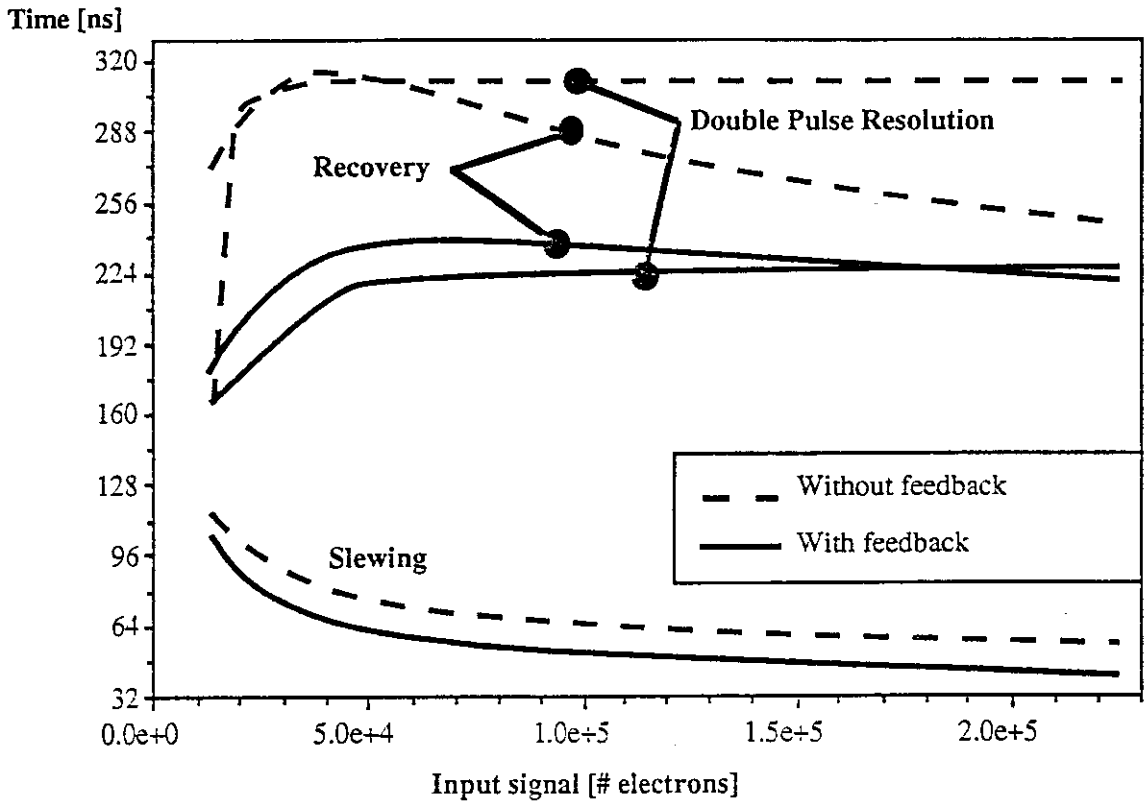


Fig. 10b: Comparison of slewing, recovery time and double pulse resolution of the improved HFC-CRF combination and the original design.

ii) Latched comparator

An alternative is the use of a faster type of comparator, namely a latched comparator, which is basically an OTA, extended with a latch function. The OTA itself, without the latch (Figure 11) is not very fast. For this circuit, the relation between input voltage and output voltage as a function of time can be described as [1]:

$$V_{out}(\Delta t) \approx V_{in} \cdot \frac{g_m}{C_L} \cdot \Delta t \qquad (7)$$

In this formula, g_m is the transconductance of the input transistor and C_L is the load capacitance. A tail current I_b of 10 μA and a gate-to-source voltage minus threshold voltage, $V_{gs} - V_T$, of 0.2 V, result in $g_m = I_b/(V_{gs} - V_T) = 50$ μS. Taking a realistic $C_L \approx 20$ fF results for a 10 mV differential input signal in $V_{out} = 3$ V after a $\Delta t \approx 120$ ns. This is however an optimistic value. As a result of the higher order poles and a clipping effect of the output voltage against the power supply lines, the response time

increases further. So, it can be concluded that a simple OTA is only suitable for use at low frequencies.

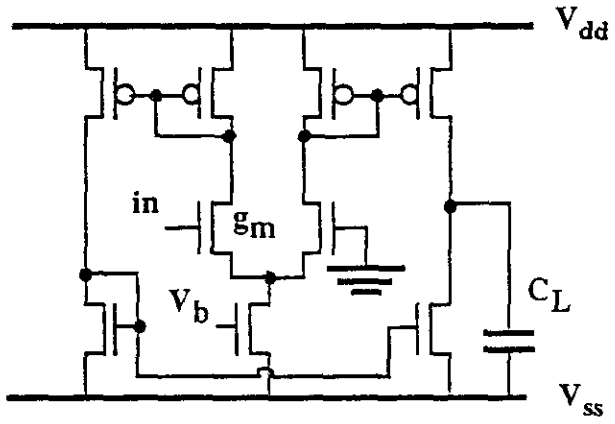


Fig. 11: OTA type comparator.

To overcome the limited response time, latched comparators are often used. They get their name from the latch that is incorporated in the structure. Latched comparators have two phases, the reset mode and the compare mode. In the reset mode the nodes of the latch are shortened to set it to an unstable high gain mode. In the compare mode these nodes are released. Depending on the input voltage the latch will switch very fast to the high or low state due to the positive feedback in the latch. A version that is often used in high speed flash A/D converters and high accuracy oversampling A/D converters is shown in Figure 12. It consists of two inverters (M8, M9 and M12, M13), assembled as a latch, in combination with an OTA. By closing the switch (M14), the latch is set in its unstable state. An important advantage of this structure over other latched comparators is the fact that the input stage does not contain any switches,. This avoids problems with clock feedthrough injected to the input nodes. Problems with clock feedthrough are further minimized because a complete symmetrical structure is used. It is also important that a two inverter latch structure is used. The connected circuit usually is an inverter to buffer the output signal further. As a result, if identical inverters are used, the output voltage in reset mode is the threshold voltage of the connected inverter. This results in almost equal response times for the high and low transitions. A disadvantage is the fact that the reset mode corresponds to the biasing condition where the inverter current is maximum. This has its consequences for the power dissipation. The only way to limit the standby current is to give the inverters a small W/L ratio. For the technology being used, 4 μm is the minimum width. In order to limit the current to around 10 μA, a length of at least 10 μm

for the n-channel devices is needed. The capacitance corresponding to these dimensions is limiting the speed to reset frequencies less than 40 MHz. For this reason a reset clock running at half the SSC frequency (period of 32 ns) is chosen. This means that the time resolution is limited to 32 ns. To obtain a 16 ns resolution, two readout channels can be used, offset by half a clock period.

The comparator speed can be approximated by:

$$t = \frac{C_p}{g_m} \ln\left(\frac{2\, V_{out}\, g_m}{V_{in}\, G_m}\right)$$

where g_m is the transconductance of the inverters (assumed identical p-channel and n-channel), G_m is the transconductance of the amplifier and C_p is the load capacitance of the amplifier.

Using $g_m \approx 30\ \mu S$, $G_m \approx 50\ \mu S$ and $C_p \approx 20$ fF results in a response time of 2.6 ns, which is considerably smaller than that for the OTA comparator. The speed is mainly determined by g_m/C_p, which is the speed of a loaded inverter. The accuracy of the comparator can be increased by increasing the size of the latch transistors. This will however increase C_p and as a result will degrade the speed.

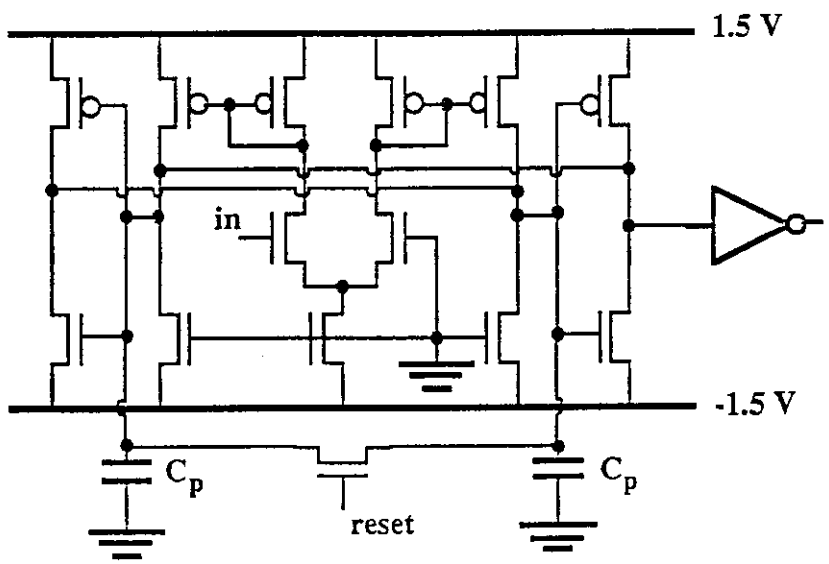


Fig. 12: Fast latched comparator.

2d. Combination with a fast preamp

The fast comparator discussed in the previous section should be combined with a fast preamp. Chosen was "ICON" [2], a current mode preamp, design and tested in CERN for use in high-rate hadron colliders. Its schematic is shown in Figure 13. The most important characteristics of this design fabricated in the 1.5 μm MIETEC process are shown in Table 3. Features that were to be changed for the knife-edge detector read-out system include noise, power and gain. The final characteristics are shown in the second column of Table 3. A comparison with the HFC in section 2b shows a considerably higher input noise. The main contributors are the current mirrors in the input stage and the feedback resistor.

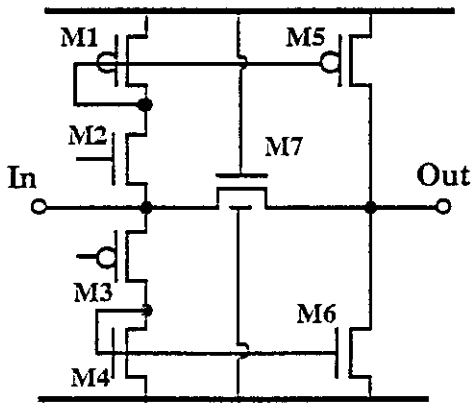


Fig. 13: ICON, a fast current mode preamp.

Table 3: Characteristics of ICON.

	CERN design	Altered design
Gain	14 mV/10^5 electrons	100 mV/10^5 electrons
Power dissipation	1 mW	85 μW
Noise	3000 e^- rms	1300 e^- rms
Peaking time	< 10 ns	65 ns

2e. Combination of ICON and a latched comparator.

Figure 14 shows the slewing, pulse width and double pulse resolution for the combination ICON-latched comparator. An important feature of the combination of a preamp with a latched comparator is the fact that the delay is not determined by the preamp, but it is set by the period of the reset clock. This is the reason why there is no slewing. If the period of the reset clock would be decreased to 16 ns, slewing would show up again.

So, the absence of slewing means that the change in delay over the range of input signals is less than the period of the reset clock.

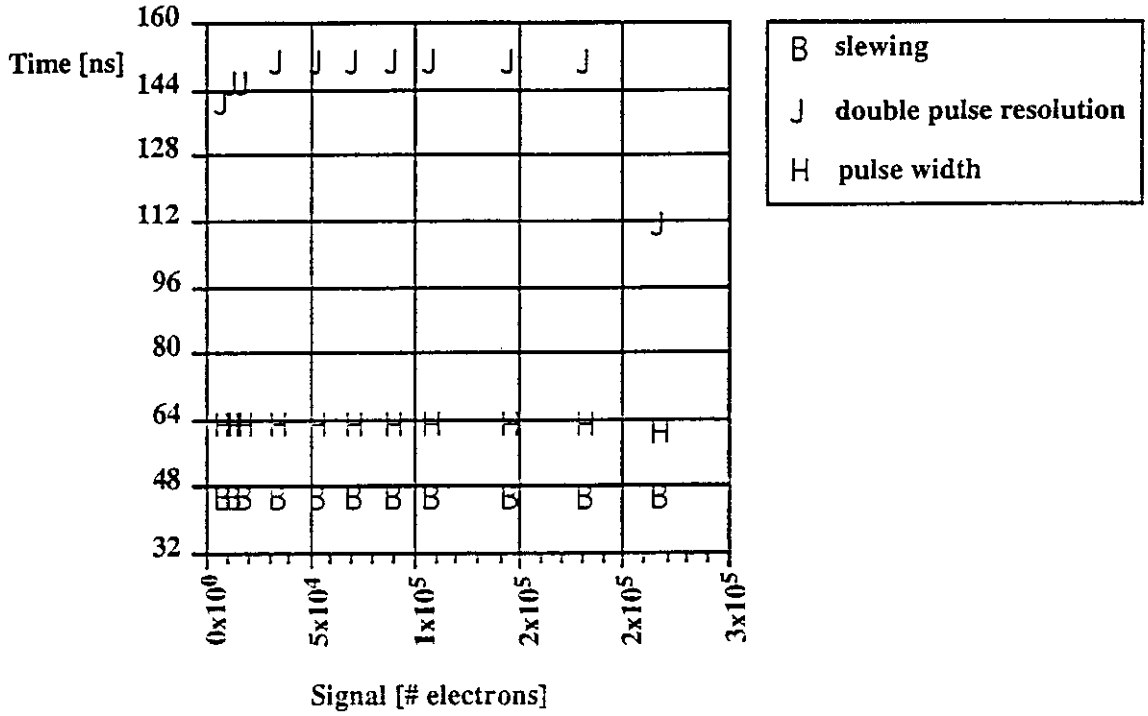


Fig. 14: Slewing, pulse width and double pulse resolution.

The output signals of the comparator are shown in Figure 15 for a 0.05 μA input current (≈ 10,000 electrons) and a 1.2 μA input current (≈ 200,000 electrons). The comparator is reset with a 31.25 MHz clock. Every 16 ns the output of the comparator is latched into the FIFO. This means that also the reset state will be latched if it is not filtered out. This will cause a problem with the 1-suppression which will consider every output pulse of the comparator as a new input signal, not as a continuation of the previous signal. To avoid this, the output signals of the comparator have to be merged before the 1-suppression is carried out. Merging can be accomplished with two D-flipflops (David and Goliath type, see buffer), driven by the reset clock. The first D-flipflop should read in data during the compare mode when the reset clock is low.

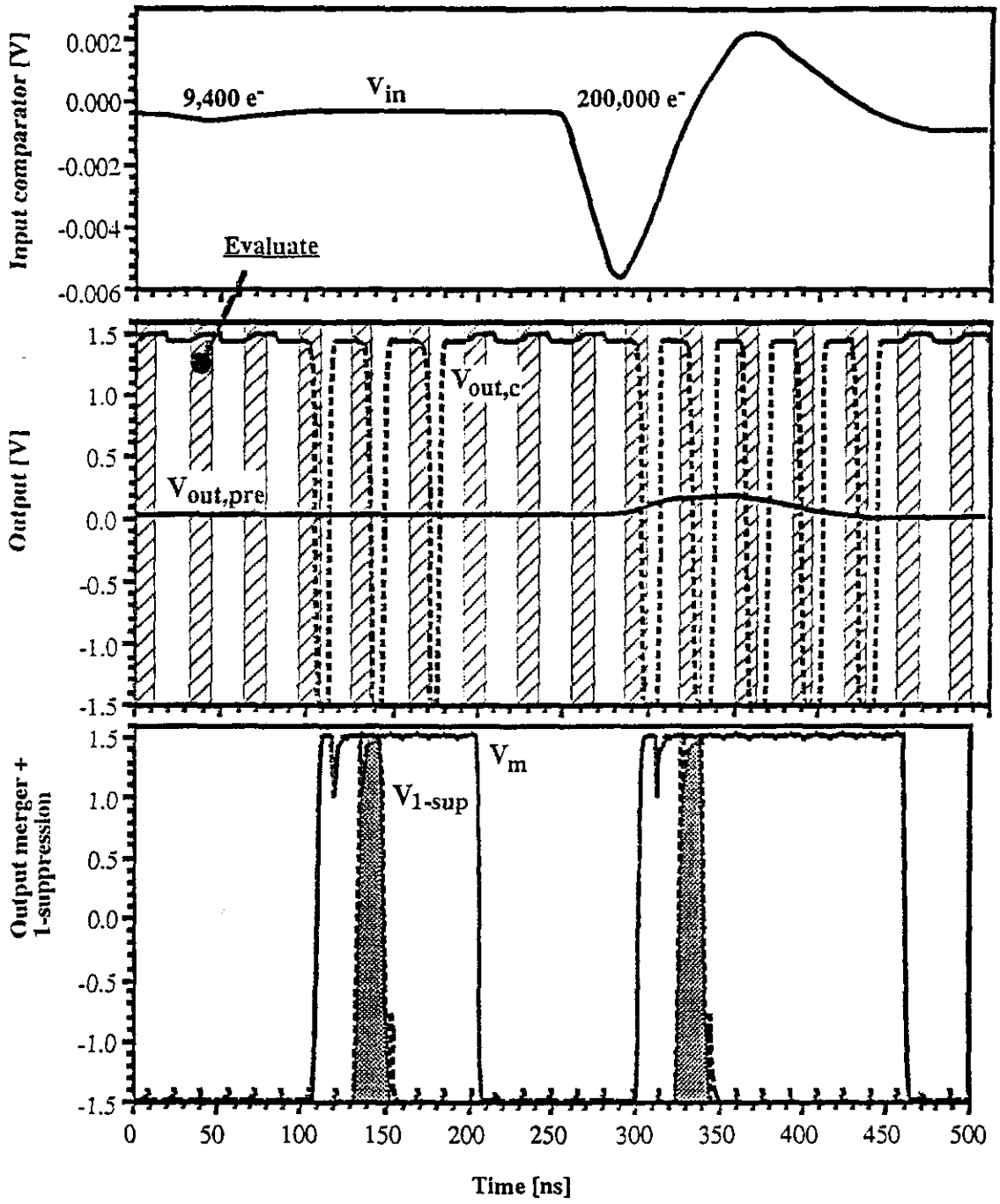


Fig. 15: Input and output signals of the comparator and merging circuit..

2f. Combination HFC and latched comparator.

The performance of the combination HFC and latched comparator is shown in Figure 16. The power consumption of this design is 200 μW.

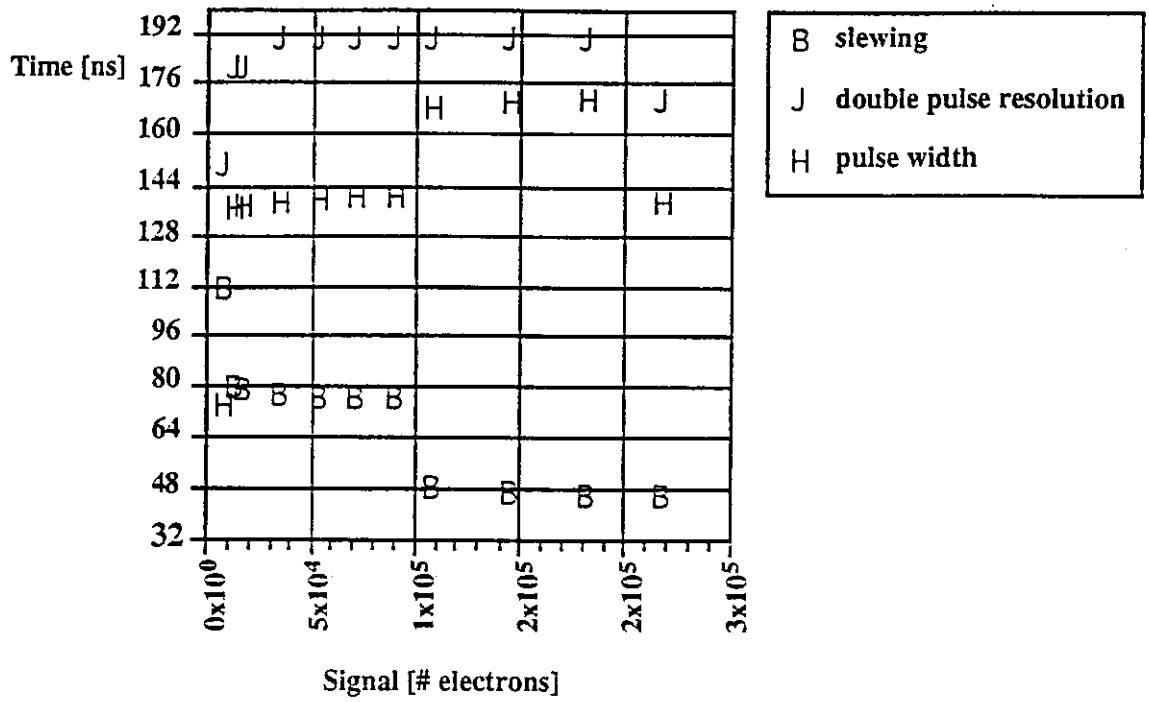


Fig. 16: Slewing, double pulse resolution and pulse width for the combination HFC-LC.

3. Buffer with '1'-suppression

3a. Buffer

The buffer is basically a simple shiftregister providing storage for the comparator output during the level 1 trigger decision time. This time is currently estimated to be 4 µs or 256 clock cycles, which is also the number of cells in the buffer. The buffer is built with 'David and Goliath' type latches (Figure 17a), where Goliath is the large inverter and David is the small feedback inverter. David restores the cell input, which is degraded by the use of a single pass transistor and refreshes it during the hold time. The single pass transistor configuration is chosen because it avoids the need for complementary pass transistors and two driving clocks. A drawback is the loss in speed. An n-channel transfer gate is known to be bad in passing a logic '1'. The speed of the nDG can be increased by giving G a low threshold such that it already switches after a slight increase of the G input. Speed can be further optimized by making D switch at a high input voltage. In the same way the pDG latch, which is affected by the bad characteristics of the p-channel device in passing a '0', is speeded up by giving G a high and D a low threshold voltage. The increased speed is illustrated in Figure 17b.

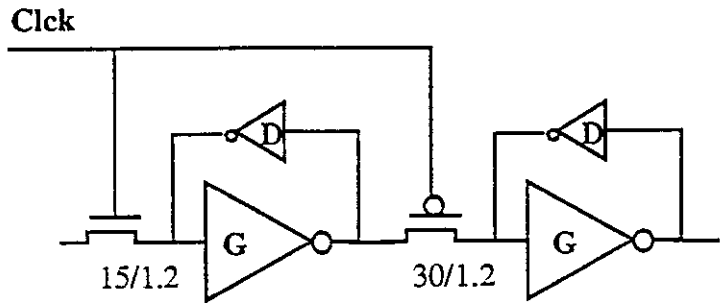


Fig. 17a: D-latch, consisting of 'David & Goliath' type latches. The divice sizes are given for the UTMC process.

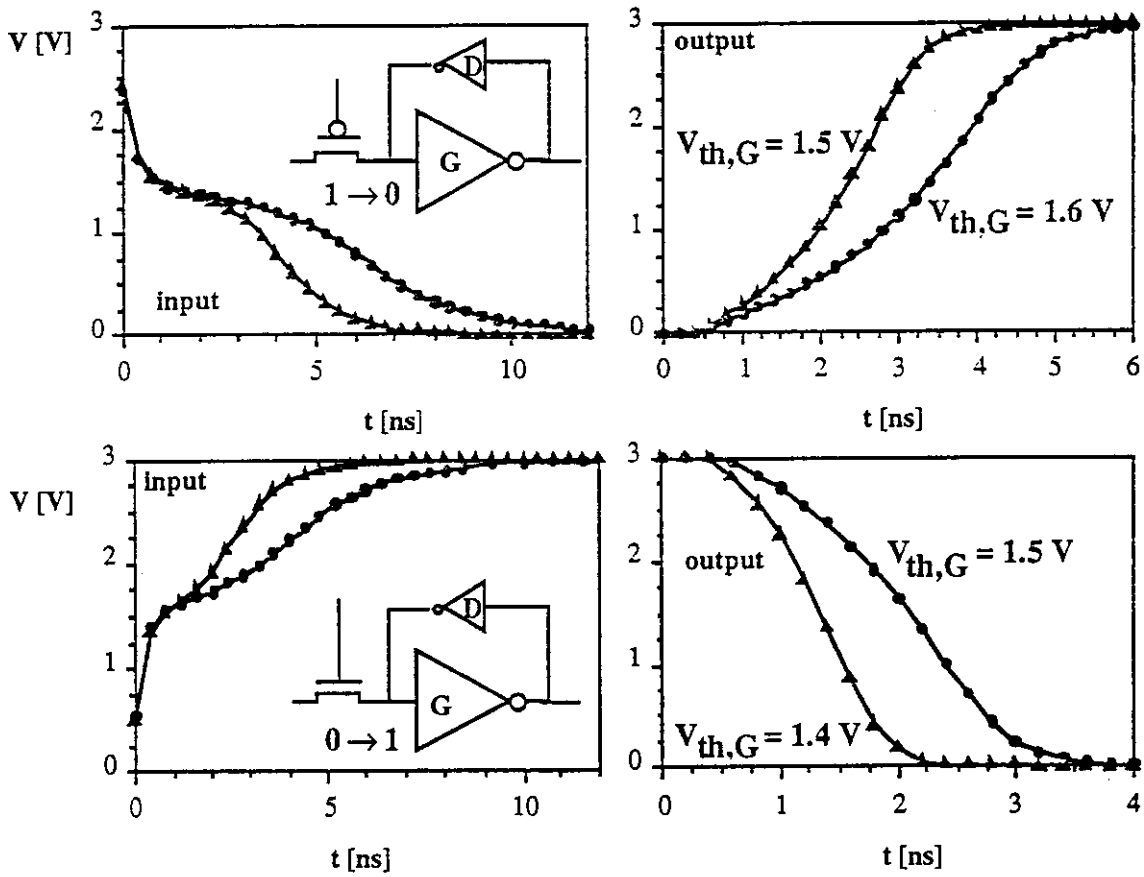


Fig. 17b: Effect optimized threshold voltages on the speed.

The D and G transistors have to be dimensioned such that the driving capability of G is enough to force a logic level to the input of G in the next cell. This has to be done against the action of D in that cell, which tries to maintain the old value. Table 4 gives the parameters for the latches to be implemented in the UTMC process. In this table, t_{dLH} and

t_{dHL} are the delay time for switching low to high, and high to low. The values are measured from the moment the switch is opened. The power consumed by the clocking of the shift register only is given by

$$P^{pF} = V\,f \approx 0.56\ \text{mW/pF} \quad \text{or} \quad 0.56\text{x}0.09\ \text{pF/cell} \approx 50\ \mu\text{W/cell}$$

For a complete channel with 256 cells, the total power dissipation becomes approximately 13 mW.

Table 4: Parameters for the D&G cells.

	nDG	pDG
nMOST-G	8/1.2	12/1.2
pMOST-G	15/1.2	4/1.2
nMOST-D	4/12	4/5
pMOST-D	4/4	4/5
t_{dLH} [ns]	3.25	3.25
t_{dHL} [ns]	1.25	1.0

b. '1'-suppression

The '1'-suppression circuit is designed to filter out successive '1' values in the buffer. Only a '1' following a '0' is passed. All succeeding '1' signals are replaced by a '0'. Figure 18 shows a circuit that realizes this function. Table 5 reflects its operation based on the values of present and previous input value to the circuit.

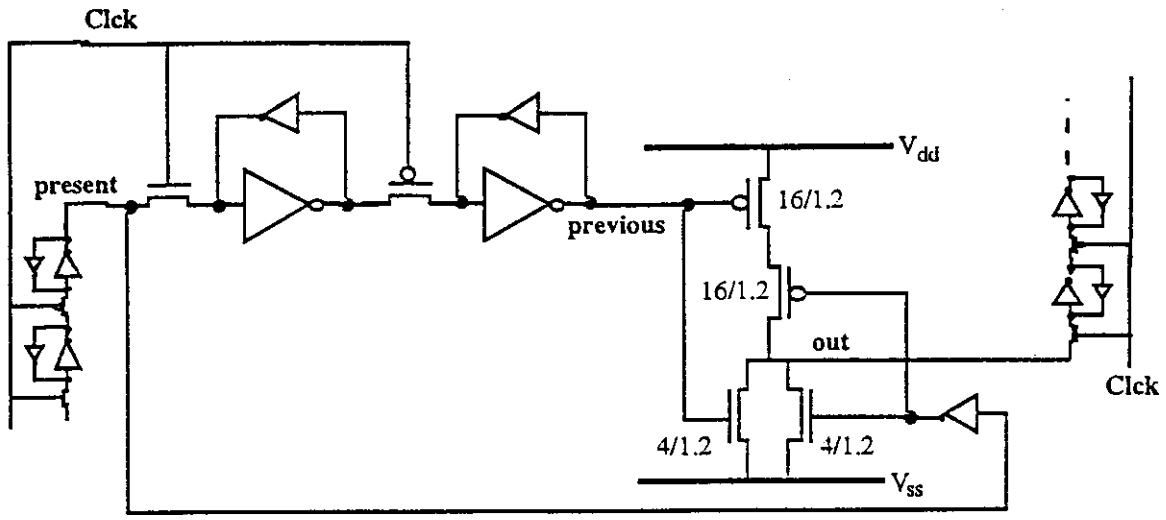


Fig. 18: '1'-suppression circuit.

Table 5: Operation of the '1'-suppression circuit.

previous	present	out
0	0	0
0	1	1
1	0	0
1	1	0

3c. Addressable FIFO.

For some applications it might be desirable to be able to peek any location of the FIFO before a level 1 for the corresponding data has been issued. In this case the FIFO should be build as indicated in Figure 19. For this case the address of the cell that is to be sampled is put into a 'Time_Out' register. A decoder decodes the 8 bit address into one of 256 output lines, which gates the contents of the corresponding FIFO cell into a readout register.

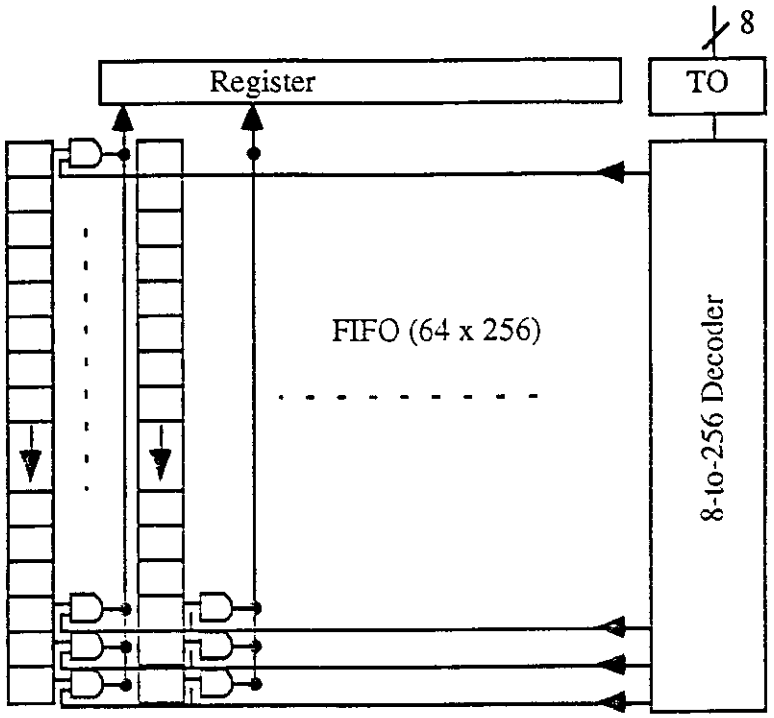
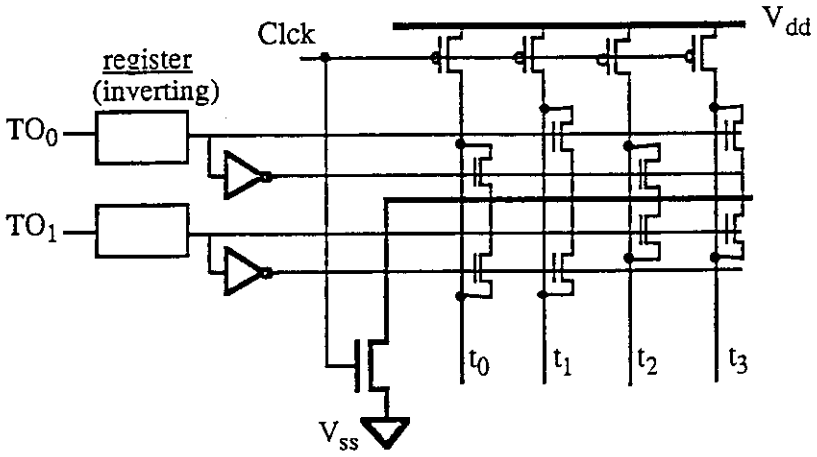


Fig. 19: Block diagram for an addressable FIFO.

A straightforward approach to implement a decoder, a so called tree-decoder, is shown in figure 20. During the negative Clck phase an addresss is read into a 'Time_Out' register TO. The contents of this register and its inverse are put onto the input lines of the decoder. At the same time the output lines of the decoder are precharged high. To avoid a discharging of the output lines by the input transistors, the latter are disconnected from V_{ss} by a switch also driven by Clck. When Clck goes high, the evaluation phase starts. All output lines are pulled low, except the active one.



TO_0	TO_1	t_0	t_1	t_2	t_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig. 20: Dynamic tree decoder.

A consequence of this approach is that all ouput lines except the one that is active, dissipate power. An estimate for the dynamic power dissipation of one ouput line at an operating frequency f is given by:

$$P = 1\ pF\ (V_{dd} - V_{ss})^2\ f \approx 0.56\ mW/pF$$

For an 8-bit decoder, the total power consumption approaches 143 mW/pF!!! This is untolerable. An alternative approach is the direct realization of all minterms. Doing this with a single gate would require an 8-input NAND gate, which is impossible with a 3 V supply voltage. The 8-input NAND can however be decomposed in multiple layers of 2-input NAND and NOR gates. For example, the minterm $TO_7TO_6TO_5TO_4TO_3TO_2TO_1TO_0$ can be written as $\overline{\overline{TO_7TO_6} + \overline{TO_5TO_4}}\ \overline{\overline{TO_3TO_2} + \overline{TO_1TO_0}}$. The hardware implementation requires two NANDs, a NOR and an inverter. The total delay of these gates is approximately 4 ns. Figure 21 shows the schematic for the realization of one of the 256 minterms. The total number of gates required for the 8-bit decoder is 256x8 = 2048. The total number of devices in this approach is given by 256x30 = 7680. Not included in these numbers are the gates required to accomplish the inverse bits $\overline{TO_i}$.

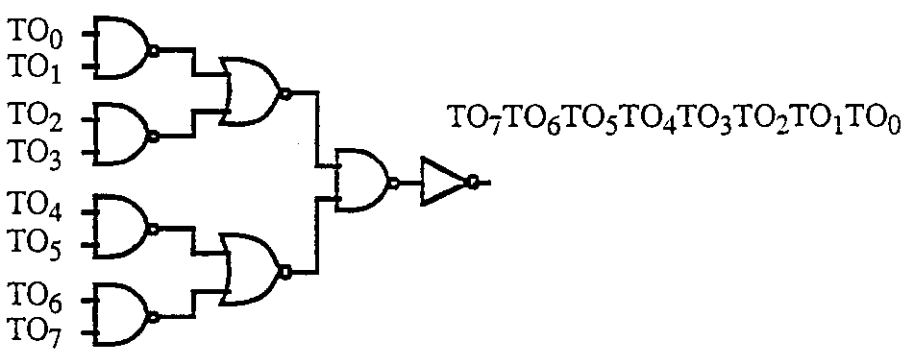


Fig. 21: 4 level realization of a minterm.

The power dissipation is in this case due to only two output lines (one deactivating and an other going active) and the charging of the gate input capacitances, which is 75 fF for a NOR or NAND. More specific, two TO_i values will change (each involving 256 inputs), giving rise to P_{in} = 20.8 mW, two output lines, P_{out} = 0.56 mW/pF, four internal

gates, P_{int} = 0.16 mW. The total power dissipation can be estimated to be 20.96 mW + 0.56 mW/pF, which is lower than in the previous case. A disadvantage is the larger input capacitance that has to be driven, namely approximately 128x75 fF = 9.6 pF!!!
A second problem is gating the contents of a FIFO cell onto an output bus. One solution is the use of a transmission gate to gate the contents of a latch onto a bus, from where it is latched in a register. An approach compatible with the tree-decoder is shown in Figure 22. The use of a single transmission gate will result in a voltage loss, and a weak signal on the large bus capacitance, which can very difficult be latched again by the type of register used in the FIFO. It has to be recovered first by a buffer, preferably one with a low threshold in the case of an n-channel as transmission gate and one with a high threshold if a p-channel device is used. The address is available during the positive half of the clock period. At this time the FIFO cell contents is put on the output bus, buffered and latched into a register. Because the bus will remember its value (high impedance node) an extra reset transistor is needed. The bus is reset during the negative half of the clock period. An alternative approach compatible with the static decoder is shown in figure 23. In this case the address will enable an inverter gating the contents of the FIFO cell onto a bus. There it can be latched again. If for the static decoder Time_Out is latched during the negative clock period, then the address will be become available during this time. If latching of Time_Out and the generation of an address leaves enough time to read the contents of the FIFO, all can be done during the same half of the clock period. The contents of the bus could be latched during the second half.

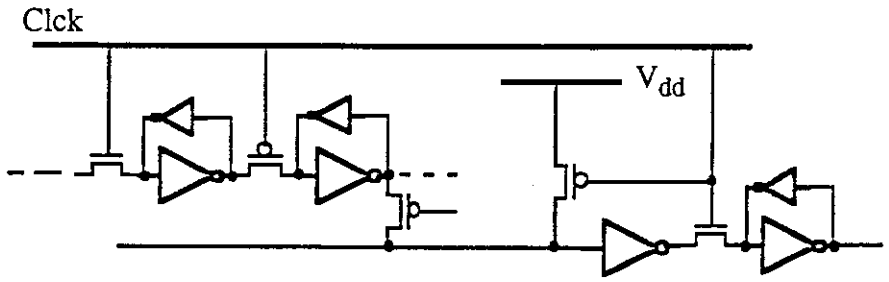


Fig. 22: FIFO readout compatible with the tree-decoder.

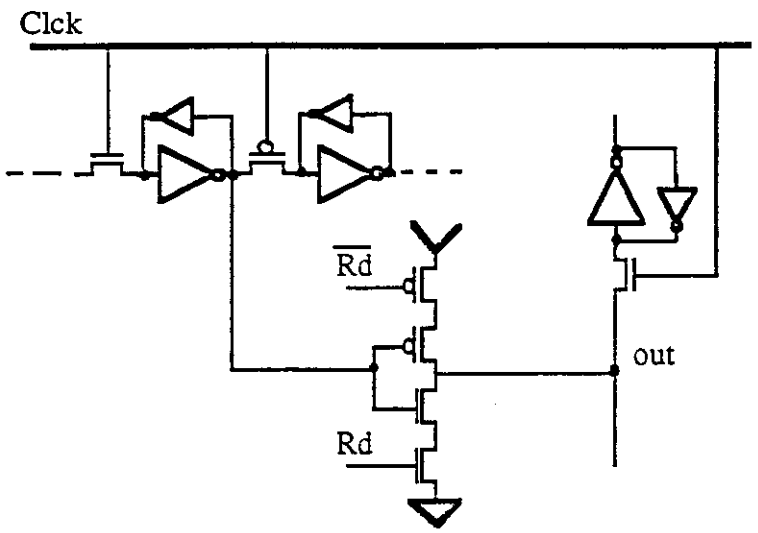


Fig. 23: Static FIFO readout.

4. Encoder

Each time a Level 1 trigger occurs the bit pattern at the end of the buffers should be given out in an encoded form. This is accomplished by the encoder, which puts out the width and the centroid of each group of consecutive activated channels ('1'-value). From two neighboring channels two signals are generated, a (01) signal indicating the leading edge of the group and a (10) signal indicating the trailing edge. Each channel has its address register. An address activated by a (01) signal is put on the 'leading address' bus. A (10) signal causes the address to be put on the 'trailing address' bus. The width of the group is obtained by subtracting the contents of both buses. Problems occur if more than one group is hit. This is solved by scanning successive channels until an active (01) and corresponding (10) signal is found. Each time the addresses are transferred and subtracted. This approach is shown in Figure 24a. Because of the exponential increase in gate number if carry look ahead is used for a fast subtraction. A pipelined approach is used instead. Using a counter to scan all channels would mean that a number of clock cycles equal to the channel number is needed for the scan. This does not take into account the time needed for address transfer and subtraction. As a result of that, an unacceptable dead time will result. A much faster approach is to ripple a signal through an inverter chain until it is stopped by a (01) or (10) signal. Hereafter the addresses are transferred and the scanning continues. This is shown in Figure 24b. The scanning is initiated by the clock going high. After the addresses are transferred, the corresponding latches are cleared and the scan signal will ripple through to the next (01) edge. The value of the last cell is used to initiate a reset of

the scan circuit and to store new data in the encoder input latch. Using this method an unlimited number of activated groups can be handled. The maximum number of groups is intentionally limited to four, using a group counter. The dead time to read one group is given by the ripple-through time added to the time for the address transfer. The latter is half a clock period.

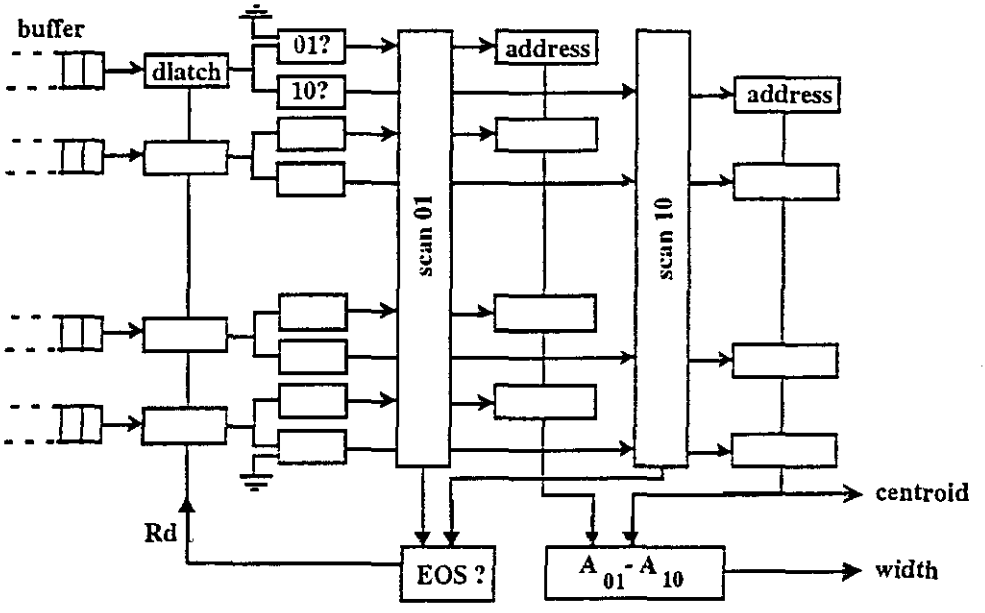


Fig. 24a: Approach used for the width encoding.

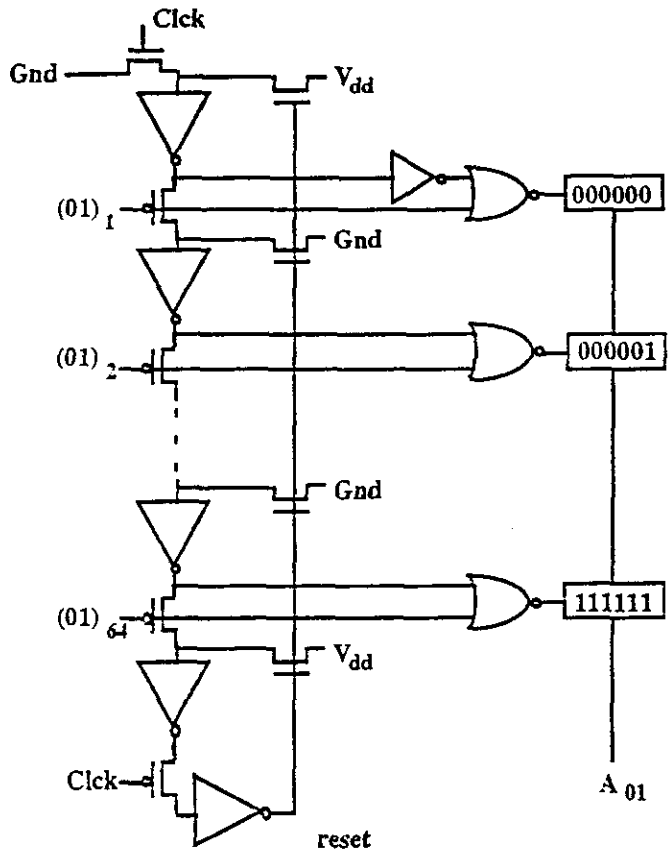


Fig. 24b: Inverter chain used for the scanning.

5. Local Bunch Counter

An 8 bit counter operating at the 62.5 MHz SSC frequency gives timing information for successive outputs of the encoder. To obtain high speed and avoid the rippling through of carry information, the counter can either make use of a carry look ahead scheme with an exponential increase in the gate count, or it can be realized as a pipeline. The main disadvantage of existing binary counters is the fact that they are not modular, or an n bit counter can not be extended to an m bit counter by just adding (m-n) identical library cells. Here, a complete modular counter was designed by using a new counting code, which is illustrated in Table 6. In this code all bit changes are defined or initiated by a low-to-high transition of the next lower order bit. This causes all carries to be known one clock period in advance of a bit change, hereby avoiding any carry delay. Because all bits are treated in the same way, their structure is identical and consequently extending a counter to any number of bits becomes straightforward.

Table 6: New counting code.

0	0	0
0	0	1
0	1	0
1	1	1
1	0	0
1	0	1
1	1	0
0	1	1
0	0	0

The hardware implementation of this counting scheme is easy. Only three functional blocks are needed: a latch to retain the previous bit value, a '0' to '1' detection block which output signal, $(01)_{out}$, to allow the next bit to change, and finally, a circuit that generates the next bit value based on a $(01)_{in}$ signal and the present bit value. Figure 25 shows a possible implementation[1]. The counter designed for a 1.2 μm CMOS process has a simulated speed of 300 MHz with a supply voltage of 3 V. By using CMOS transmission gates and dynamic logic the speed can easily be increased to 0.5 GHz.

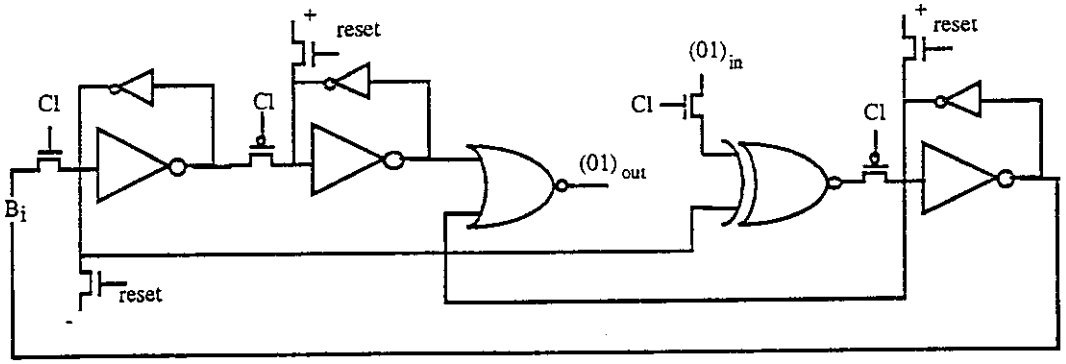


Fig. 25: Possible implementation of a counter cell.

6. Interfaces.

To assemble the individual blocks that were described in the previous sections into an integrated system, additional interface blocks are needed. These blocks are desribed next.

6a. OTA comparator-buffer.

---

[1] Patent pending.

In order to avoid clock feedthrough from the latch on the comparator, an extra buffer has to be used. The buffer at the same time provides the driving capability needed to drive the DG latch. A CMOS inverter is used as buffer a. Its dimensions are given in Table 7.

nMOST	6/1.2
pMOST	12/1.2
t_d [ns] with C_L = 50 fF	0.5

Table 7: Buffer.

6b. Buffer-Encoder

Each time a scan cycle has been completed, data from the buffer is latched into the encoder input latch. This latch is of the D&G type. This device keeps the data available during the full scan cycle. The (01) and (10) transition signals are derived from its outputs.

References

[1] R. S. Soin, F. Maloberti and J. Franca, "Analogue-Digital ASICs: circuit techniques, design tools and applications", IEEE Circuits and Systems series, 1991

[2] F. Anghinolfi, P. Aspell, M. Campbell. E. H. M. Heijne, P. Jarron, G. Meddeler, J. C. Santiard and S. Buytaert, "ICON, A Current Mode Preamplifier in CMOS Technology for Use With High-Rate Particle Detectors", Proc. IEEE Nucl. Science Symposium, November 1991

```
*******************************************
* HFC AS A PREAMP FOR KNIFE-EDGE DETECTOR *
*******************************************
* modeled for UTMC
VDD 1  0  1.5
VSS 10 0 -1.5
VB6 21 0 -0.0
VB7 7  0  0.0
VB9 9  0 -0.0
v2  22 0  0.0
II  4  0  PULSE(0 0.075u 10N 10N 10N 20N 2000N)
*iN 4  0  ac 1
CIN 4  0  5p
Cfb 6  4  150f
cut 6  0  50f
*
**************
*HFC CIRCUIT *
**************
*
M1 3 4 12 12  tn W=250U L=2U AD=900P  AS=900P  PD=507U  PS=507U
M2 5 0 12 12  tn W=250U L=2U AD=900P  AS=900P  PD=507U  PS=507U
M3 3 5 1 1    tp W=11.2U L=2U AD=39.6P AS=39.6P PD=29.2U PS=29.2U
M4 5 5 1 1    tp W=4U L=2U AD=14.4P AS=14.4P PD=15.2U PS=15.2U
M5 12 9 10 10 tn W=4U   L=8U AD=14.4P AS=14.4P PD=15.2U PS=15.2U
*
M6 6 21 3 1  tp W=15U L=1.2U AD=54P AS=54P  PD=37.2U PS=37.2U
M7 6 7 8 8   tn W=15U L=1.2U AD=54P AS=54P  PD=37.2U PS=37.2U
M8 8 9 10 10 tn W=4U L=8U   AD=14.4P AS=14.4P PD=15.2U PS=15.2U
*
************************
* FEEDBACK TRANSISTOR *
************************
*
M9 6 10 4 1  tp W=4U L=25U AD=15P AS=15P PD=15.5U PS=15.5U
*
**************
* Comparator *
**************
*
m10 11 22 1  1  tp w=6u   l=2u   ad=21.6p as=21.6p pd=19.2u ps=19.2u
m11 15 6  11 1  tp w=40u  l=1.5u ad=144p  as=144p  pd=87.2u ps=87.2u
m12 14 0  11 1  tp w=40u  l=1.5u ad=144p  as=144p  pd=87.2u ps=87.2u
m13 15 15 10 10 tn w=10u l=1.2u  AD=36P AS=36P PD=27.2U PS=27.2U
m14 14 15 10 10 tn w=10u l=1.2u   AD=36P AS=36P PD=27.2U PS=27.2U
*
*
**********************
* An Output Inverter *
**********************
*
m15 16 14 1  1  tp w=4u l=1.2u ad=15p as=15p pd=15.5u ps=15.5u
m16 16 14 10 10 tn w=4u l=1.2u ad=15p as=15p pd=15.5u ps=15.5u
*
*****************
* output buffer *
*****************
*x1 16 17 1 10 buf
*
* subcircuit
*
*.subckt buf 1 2 3 4
*m1  2 1 3 3 tp w=12u l=1.2u ad=25.8p as=25.8p pd=28.3u ps=28.3u
*m2  2 1 4 4 tn w=6u  l=1.2u ad=12.9p as=12.9p pd=16.3u ps=16.3u
```

```
*.ends
*
.include '/home/slug/vstrael/models/utmc.m'
.OPTION post nomod
.temp 27
.TRAN 1N 700N
.PRINT TRAN v(6) v(14) v(16)
.OP
*.AC DEC 10 1 100MEGHZ
.END
```

```
*****************************************
* HFC AS A PREAMP FOR KNIFE-EDGE DETECTOR *
* FAST COMPARATOR
*****************************************
* modeled for UTMC
VDD 1  0  1.5
VSS 10 0 -1.5
VB6 21 0 -0.0
VB7 7  0  0.0
VB9 9  0 -0.0
v2  22 0  0.0
II  4  444  PULSE(0 100u 10N 0N 0N 1N 500N)
Vmeas 444 0 dc 0
CIN 4  0  5p
Cfb 6  4  150f
Cout 17 0 1p
*
**************
*HFC CIRCUIT *
**************
*
m1 3  4 12 12  tn W=250U  L=2U AD=900P  AS=900P  PD=507U  PS=507U
m2 5  0 12 12  tn W=250U  L=2U AD=900P  AS=900P  PD=507U  PS=507U
m3 3  5 1  1   tp W=11.2U L=2U AD=39.6P AS=39.6P PD=29.2U PS=29.2U
m4 5  5 1  1   tp W=4U    L=2U AD=14.4P AS=14.4P PD=15.2U PS=15.2U
m5 12 9 10 10  tn W=4U    L=8U AD=14.4P AS=14.4P PD=15.2U PS=15.2U
*
m6 6 21 3 1  tp   W=15U   L=1.2U AD=54P AS=54P  PD=37.2U PS=37.2U
m7 6 7  8 8  tn   W=15U   L=1.2U AD=54P AS=54P  PD=37.2U PS=37.2U
m8 8 9 10 10 tn   W=4U    L=8U   AD=14P AS=14P  PD=15.2U PS=15.2U
*
************************
* FEEDBACK TRANSISTOR *
************************
*
m9 6 10 4 1  tp W=4U L=25U AD=15P AS=15P PD=15.5U PS=15.5U
*
**************
* FAST Comparator *
**************
*
m10  11 22 1  1   tp w=6u  l=2u   ad=57.6p as=57.6p pd=39.2u   ps=39.2u
m11  15 6  11 1   tp w=50u l=1.2u ad=252p  as=252p  pd=147.2u ps=147.2u
m12  14 0  11 1   tp w=50u l=1.2u ad=252p  as=252p  pd=147.2u  ps=147.2u
*
*m13  15 15 10 10 tn w=15u l=2u   AD=36P   AS=36P   PD=27.2U   PS=27.2U
*m14  14 15 10 10 tn w=15u l=2u   AD=36P   AS=36P   PD=27.2U   PS=27.2U
*
m13  15 15 99 99  tn w=10u l=2u   AD=36P   AS=36P   PD=27.2U   PS=27.2U
m13b 99 15 10 10  tn w=10u l=1.2u AD=36P   AS=36P   PD=27.2U   PS=27.2U
m14  14 15 98 98  tn w=10u l=2u   AD=36P   AS=36P   PD=27.2U   PS=27.2U
m14b 98 14 10 10  tn w=10u l=1.2u AD=36P   AS=36P   PD=27.2U   PS=27.2U
*
**********************
* An Output Inverter *
**********************
*
m15 16 14 1  1  tp w=4u l=1.2u ad=15p as=15p pd=15.5u ps=15.5u
m16 16 14 10 10 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.5u ps=23.5u
*
* second inverter
*
m17 66 16 1  1  tp w=16u l=1.2u ad=57.6p as=57.68p pd=39.2u ps=39.2u
m18 66 16 10 10 tn w=4u l=1.2u ad=14.4P AS=14.4P  PD=15.2U PS=15.2U
```

```
*
*****************
* output buffer *
*****************
*
x1 66 17 1 10 buf
*
* subcircuit
*
.subckt buf 1 2 3 4
m1  2 1 3 3 tp w=16u l=1.2u ad=57.6p as=57.68p pd=39.2u ps=39.2u
m2  2 1 4 4 tn w=32u  l=1.2u AD=115.2P AS=115.2P  PD=71.6U PS=71.6U
.ends
*
.include '/home/slug/vstrael/models/utmc.m'
.OPTION post nomod spice tnom=27
.temp 27
.tran 1n 300n
.print tran v(6) i(vmeas) v(17)
.op
.end
```

```
**********************************************
* LATCHED COMPARATOR FOR KNIFE-EDGE DETECTOR *
**********************************************
*
VDD 20 0  1.5
VSS 19 0 -1.5
VB  12 0  0.0
vd  a0 0  0.0
vt  18 0  pulse(1.5 -1.5 0n 1n 1n 15n 32n)
*vf  88 0 pulse(1.5 -1.5 11n 1n 1n 4n 32n)
*
vm a1  0  1.5
VS a10 0 -1.5
ibb b1 0  2ua
icc c1 0  6.8ua
iI  4  0  PULSE(0 0.075ua 20n 10n 10n 20n 140n)
cd  4  0  5p
cl  13 0  40ff
*
mr a7 a10 4 a1 tp w=4u l=18u  ad=14.4p as=14.4p pd=15.2u ps=15.2p
*
***************
*ICON CIRCUIT *
***************
*
Ma1 2  2  a1  a1  tp  w=5U   L=2U ad=18p  as=18p   pd=17.2u  ps=17.2u
Ma2 a7 2  a1  a1  tp  w=5U   L=2U ad=18p  as=18p   pd=17.2u  ps=17.2u
Ma3 2  b2 4   4   tn  w=47U  L=2U ad=169p as=169p  pd=101u   ps=101.2u
Ma4 6  c1 4   a1  tp  w=55U  L=2U ad=198p as=198p  pd=117u   ps=117u
Ma5 6  6  a10 a10 tn  w=5U   L=2U ad=18p  as=18p   pd=17.2u  ps=17.2u
Ma6 a7 6  a10 a10 tn  w=5U   L=2U ad=18p  as=18p   pd=17.2u  ps=17.2u
*
******************************
* LATCHED COMPARATOR CIRCUIT *
******************************
*
m1 8  a7 7  7  tn w=33u l=1.2u ad=144p   as=144p   pd=87.2u  ps=87.2u
m2 9  a0 7  7  tn w=33u l=1.2u ad=144p   as=144p   pd=87.2u  ps=87.2u
M3 8  8  20 20 tp w=4U  l=5U   AD=14.4P  AS=14.4P  PD=15.2U  PS=15.2U
M4 9  9  20 20 tp w=4U  l=5U   AD=14.4P  AS=14.4P  PD=15.2U  PS=15.2U
M5 7  12 19 19 tn w=4U  l=8U   AD=28.8P  AS=28.8P  PD=23.2U  PS=23.2U
*
M6 10 8  20 20 tp w=4U l=5U   AD=14.4P  AS=14.4P  PD=15.2U  PS=15.2U
M7 10 12 19 19 tn w=4U l=16U  AD=14.4P  AS=14.4P  PD=15.2U  PS=15.2U
M8 11 9  20 20 tp w=4U l=5U   AD=14.4P  AS=14.4P  PD=15.2U  PS=15.2U
M9 11 12 19 19 tn w=4U l=16U  AD=14.4P  AS=14.4P  PD=15.2U  PS=15.2U
*
********************
* Output Inverters *
********************
*
m10 11 10 20 20 tp w=6u l=5u   ad=21.6P  AS=21.6P  PD=19.2U  PS=19.2U
m11 11 10 19 19 tn w=6u l=1.2u AD=21.6P  AS=21.6P  PD=19.2U  PS=19.2U
m12 10 11 20 20 tp w=6u l=8.5u ad=21.6P  AS=21.6P  PD=19.2U  PS=19.2U
m13 10 11 19 19 tn w=6u l=2u   AD=21.6P  AS=21.6P  PD=19.2U  PS=19.2U
*
* Reset switch
*
m14 10 18 11 19 tn w=8u l=1.2u ad=28.8P  AS=28.8P  PD=23.2U  PS=23.2U
*
* Output buffer
*
m15 13 10 20 20  tp w=8u l=1.2u ad=28.8P  AS=28.8P  PD=23.2U  PS=23.2U
m16 13 10 19 19  tn w=4u l=1.2u ad=14.4P  AS=14.4P  PD=15.2U  PS=15.2U
```

```
*
* OUTPUT LATCH
*
*ml1 12 11 20 20 tp  w=12u l=1.2u ad=43.2p as=43.2p pd=31.2u ps=31.2u
*ml2 12 11 19 19 tn  w=4u  l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
*
*ml3 11 12 20 20 tp  w=4u  l=5u   ad=14.4p as=14.4p pd=15.2u ps=15.2u
*ml4 11 12 19 19 tn  w=4u  l=5u   ad=14.4p as=14.4p pd=15.2u ps=15.2u
*
*mls 13 88 11 20 tp  w=30u l=1.2u ad=108p as=108p pd=67.2u ps=67.2u
*
* BIASING CIRCUIT
*
*
mb1  b2 b1 a1  a1  tp  w=4u  l=20u
mb2  b1 b1 a1  a1  tp  w=4u  l=20u
mb3  b2 b2 b3  b3  tn  w=6u  l=43u
mb4  b3 b3 a10 a10 tn  w=7u  l=2u
*
mc1  c2 c1 a1  a1  tp  w=4u  l=20u
mc2  c1 c1 a1  a1  tp  w=4u  l=20u
mc3  c2 c2 c3  c3  tn  w=6u  l=43u
mc4  c3 c3 a10 a10 tn  w=7u  l=2u
*
*
*
.include '/home/slug/vstrael/models/utmc.m'
.option post nomod spice dcon=1
*.ic v(12)=1.5 v(11)=-1.5
.temp 27
.OP
.tran 1n 250n
.print tran v(13)
.end
```

```
Fast modular counter
.include  '/home/slug/vstrael/models/schot.m'
*
*
.subckt nand 1 2 3 4
*            in out vdd
m1  3 1 4 4 tp w=5u l=1.2u ad=8.6p as=8.6p pd=12.3u ps=12.3u
m2  3 2 4 4 tp w=5u l=1.2u ad=8.6p as=8.6p pd=12.3u ps=12.3u
m3  3 1 5 0 tn w=4u l=1.2u ad=6.45p as=6.45p pd=10.3u ps=10.3u
m4  5 2 0 0 tn w=4u l=1.2u ad=6.45p as=6.45p pd=10.3u ps=10.3u
.ends
.subckt nor 1 2 3 4
m1  5 2 4 4 tp w=12u l=1.2u ad=25.8p as=25.8p pd=28.3u ps=28.3u
m2  3 1 5 5 tp w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
m3  3 1 0 0 tn w=4u l=1.2u ad=8.6p as=8.6p pd=12.3u ps=12.3u
m4  3 2 0 0 tn w=4u l=1.2u ad=8.6p as=8.6p pd=12.3u ps=12.3u
.ends
.subckt inverter 1 2 3
m1  2 1 3 3 tp w=5u l=1.2u ad=10.75p as=10.75p pd=14.3u ps=14.3u
m2  2 1 0 0 tn w=2.5u l=1.2u ad=3.3p as=3.3p pd=9.3u ps=9.3u
.ends
.subckt big_inverter 1 2 3
m1  2 1 3 3 tp w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
m2  2 1 0 0 tn w=4u l=1.2u ad=8.6p as=8.6p pd=14.3u ps=14.3u
.ends
.subckt driver 1 2 3
m1  2 1 3 3 tp w=100u l=1.2u ad=215p as=215p pd=210u ps=210u
m2  2 1 0 0 tn w=50u l=1.2u ad=108p as=108p pd=106.3u ps=106.3u
.ends
.subckt driver2 1 2 3
m1  2 1 3 3 tp w=300u l=1.2u ad=645p as=645p pd=307u ps=307u
m2  2 1 0 0 tn w=150u l=1.2u ad=320p as=320p pd=156.3u ps=156.3u
.ends
.subckt exor 1 2 7 8
*           in1 in2 out vdd
x1 1 3 8 inverter
x2 2 4 8 inverter
x3 2 3 5 8 nand
x4 4 1 6 8 nand
x5 5 6 7 8 nand
.ends
*
.subckt nexor 1 2 6 11
x1 1 3 11 inverter
x2 2 4 11 inverter
x3 5 6 11 big_inverter
m1  7 2 11 11 tp w=16u l=1.2u ad=34.4p as=34.4p pd=36.3u ps=36.3u
m2  8 1 11 11 tp w=16u l=1.2u ad=34.4p as=34.4p pd=36.3u ps=36.3u
m3  5 3 7 7 tp w=16u l=1.2u ad=34.4p as=34.4p pd=36.3u ps=36.3u
m4  5 4 8 8 tp w=16u l=1.2u ad=34.4p as=34.4p pd=36.3u ps=36.3u
m5  5 4 9 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
m6  9 3 0 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
m7  5 2 10 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
m8  10 1 0 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
.ends
*
.subckt david 1 2 3
m1  2 1 3 3 tp w=5u l=5u ad=10.75p as=10.75p pd=14.3u ps=14.3u
m2  2 1 0 0 tn w=2.5u l=5u ad=5.4p as=5.4p pd=9.3u ps=9.3u
.ends
.subckt high_david 1 2 3
m1  2 1 3 3 tp w=2.5u l=1.2u ad=5.3p as=5.3p pd=11.3u ps=11.3u
m2  2 1 0 0 tn w=2.5u l=5u ad=5.3p as=5.3p pd=11.3u ps=11.3u
.ends
```

```
.subckt low_david 1 2 3
m1  2 1 3 3 tp w=2.5u l=2.5u ad=5.3p as=5.3p pd=11.3u ps=11.3u
m2  2 1 0 0 tn w=2.5u l=2.5u ad=5.3p as=5.3p pd=11.3u ps=11.3u
.ends
.subckt buf 1 2 3
m1  2 1 3 3 tp w=15u l=1.2u ad=30.8p as=30.8p pd=34.3u ps=34.3u
m2  2 1 0 0 tn w=6u l=1.2u ad=12.9p as=12.9p pd=16.3u ps=16.3u
.ends
.subckt low_buf 1 2 3
m1  2 1 3 3 tp w=12u l=1.2u ad=25.8p as=25.8p pd=28.3u ps=28.3u
m2  2 1 0 0 tn w=12u l=1.2u ad=25.8p as=25.8p pd=28.3u ps=28.3u
.ends
.subckt high_buf 1 2 3
m1  2 1 3 3 tp w=18u l=1.2u ad=37p as=37p pd=40.3u ps=40.3u
m2  2 1 0 0 tn w=6u l=1.2u ad=12.9p as=12.9p pd=16.3u ps=16.3u
.ends
.subckt reset 1 4 2 3
*            in reset out vdd
m1  6 1 3 3 tp w=10u l=1.2u ad=21.5p as=21.5p pd=24.3u ps=24.3u
m2  6 4 5 0 tn w=5u l=1.2u ad=10.75p as=10.75p pd=12.3u ps=12.3u
m3  5 1 0 0 tn w=5u l=1.2u ad=10.75p as=10.75p pd=12.3u ps=12.3u
m4  2 6 3 3 tp w=30u l=1.2u ad=60.8p as=60.8p pd=64.3u ps=64.3u
m5  2 6 0 0 tn w=15u l=1.2u ad=30.8p as=30.8p pd=34.3u ps=34.3u
.ends
.subckt dlatch_p 1 2 3 4 5
*               in out in_cl cl vdd
x1 3 2 5 high_buf
x2 2 3 5 low_david
msp 1 4 3 5 tp w=30u l=1.2u ad=64p as=64p pd=64.3u ps=64.3u
.ends
.subckt dlatch_n 1 2 3 4 5
*               in out in_cl cl vdd
x1 3 2 5 low_buf
x2 2 3 5 high_david
msn  1 4 3 0 tn w=15u l=1.2u ad=32p as=32p pd=34.3u ps=34.3u
.ends
.subckt dlatch 1 2 8 6 3 4 5
*            in out in_cl in_cl_bar reset clock vdd
x1 1 6 8 4 5 dlatch_n
x2 6 2 7 4 5 dlatch_p
mreset1  8  3 0 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
mreset2  5  3 7 0 tn w=15u l=1.2u ad=32p as=32p pd=34.3u ps=34.3u
.ends
.subckt dlatch1 1 2 8 6 3 4 5
*            in out in_cl in_cl_bar reset clock vdd
x1 1 6 8 4 5 dlatch_n
x2 6 2 7 4 5 dlatch_p
mreset1  8  3 5 0 tn w=15u l=1.2u ad=32p as=32p pd=34.3u ps=34.3u
mreset2  7  3 0 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
.ends
*
.subckt count1 1 3 6 7 5
*             out 01out reset clock vdd
x1 1 2 12 13 6 7 5 dlatch1
x2 2 4 3 5 nor
x3 13 10 5 buf
x4 10 1 4 7 5 dlatch_p
mreset 4 6 0 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
.ends
.subckt count 1 9 3 6 7 5
*            out 01in 01out reset clock vdd
x1 1 2 12 13 6 7 5 dlatch
x2 2 4 3 5 nor
x3 8 12 10 5 nexor
```

```
x4 10 1 4 7 5 dlatch_p
mreset1 5 6 4 0 tn w=15u l=1.2u ad=32p as=32p pd=34.3u ps=34.3u
mreset2 8 6 0 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
ms 9 7 8 0 tn w=8u l=1.2u ad=17.2p as=17.2p pd=20.3u ps=20.3u
.ends
*
* circuit description
*
x1 1 5 8 9 10 count1
x2 2 5 6 8 9 10 count
x3 3 6 7 8 9 10 count
x4 4 7 15 8 9 10 count
x5 16 15 17 8 9 10 count
x6 19 17 18 8 9 10 count
x8 20 18 22 8 9 10 count
x9 21 22 23 8 9 10 count
x10 x16 23 x17 8 9 10 count
x11 x19 x17 x18 8 9 10 count
x12 x20 x18 x22 8 9 10 count
x13 x21 x22 x23 8 9 10 count
x14 y16 x23 y17 8 9 10 count
x15 y19 y17 y18 8 9 10 count
x16 y20 y18 y22 8 9 10 count
x17 y21 y22 y23 8 9 10 count
*
vdd   10   0   dc  3
vcl 998 0 pulse(0 3 4n 1n 1n 63n 128n)
x99 998 9 10 driver2
vreset 11 0 pulse(0 3 0n 1n 1n 4n 10m)
x7 11 9 8 10 reset
*
*
.tran 1n 8388.612u
.option tnom=27 limpts=50000 itl5=100000
.temp 27
*.print tran power
.meas tran avgval avg power from=4n to=8388.612u
.meas tran rmsval rms power from=4n to=8388.612u
.meas tran maxval max power from=4n to=8388.612u
.end
```

```
counter
.include  '/home/slug/vstrael/models/utmc.m'
* optimized size for latches
*
*
.subckt nand 1 2 3 4
*            in out vdd
m1  3 1 4 4 tp w=5u l=1.2u ad=18p as=18p pd=17.2u ps=17.2u
m2  3 2 4 4 tp w=5u l=1.2u ad=18p as=18p pd=17.2u ps=17.2u
m3  3 1 5 5 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m4  5 2 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt nor 1 2 3 4
m1  5 2 4 4 tp w=12u l=1.2u ad=43.2p as=43.2p pd=31.2u ps=31.2u
m2  3 1 5 5 tp w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m3  3 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m4  3 2 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt inverter 1 2 3
m1  2 1 3 3 tp w=4u l=2.4u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m2  2 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt big_inverter 1 2 3
m1  2 1 3 3 tp w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m2  2 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt driver2 1 2 3
m1  2 1 3 3 tp w=300u l=1.2u ad=1080p as=1080p pd=607.2u ps=607.2u
m2  2 1 0 0 tn w=150u l=1.2u ad=540p as=540p pd=307.2u ps=307.2u
.ends
.subckt exor 1 2 7 8
*           in1 in2 out vdd
x1 1 3 8 inverter
x2 2 4 8 inverter
x3 2 3 5 8 nand
x4 4 1 6 8 nand
x5 5 6 7 8 nand
.ends
*
.subckt nexor 1 2 6 11
x1 1 3 11 inverter
x2 2 4 11 inverter
x3 5 6 11 big_inverter
m1  7 2 11 11 tp w=16u l=1.2u ad=57.6p as=57.6p pd=39.2u ps=39.2u
m2  8 1 11 11 tp w=16u l=1.2u ad=57.6p as=57.6p pd=39.2u ps=39.2u
m3  5 3 7 11 tp w=16u l=1.2u ad=57.6p as=57.6p pd=39.2u ps=39.2u
m4  5 4 8 11 tp w=16u l=1.2u ad=57.6p as=57.6p pd=39.2u ps=39.2u
m5  5 4 9 9 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m6  9 3 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m7  5 2 10 10 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m8  10 1 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
.ends
*
.subckt david 1 2 3
m1  2 1 3 3 tp w=4u l=5u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m2  2 1 0 0 tn w=4u l=10u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt low_david 1 2 3
m1  2 1 3 3 tp w=4u l=5u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m2  2 1 0 0 tn w=4u l=5u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt buf 1 2 3
m1  2 1 3 3 tp w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m2  2 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
```

```
.ends
.subckt high_buf 1 2 3
m1  2 1 3 3 tp w=25u l=1.2u ad=90p as=90p pd=57.2u ps=57.2u
m2  2 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt high_david 1 2 3
m1  2 1 3 3 tp w=4u l=4u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m2  2 1 0 0 tn w=4u l=12u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt low_buf 1 2 3
m1  2 1 3 3 tp w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m2  2 1 0 0 tn w=25u l=1.2u ad=90p as=90p pd=57.2u ps=57.2u
.ends
.subckt reset 1 4 2 3
*            in reset out vdd
m1  6 1 3 3 tp w=10u l=1.2u ad=36p as=36p pd=27.2u ps=27.2u
m2  6 4 5 5 tn w=5u l=1.2u ad=18p as=18p pd=17.2u ps=17.2u
m3  5 1 0 0 tn w=5u l=1.2u ad=18p as=18p pd=17.2u ps=17.2u
m4  2 6 3 3 tp w=30u l=1.2u ad=108p as=108p pd=67.2u ps=67.2u
m5  2 6 0 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
.ends
.subckt dlatch_p 1 2 3 4 5
*               in out in_cl cl vdd
x1 3 2 5 high_buf
x2 2 3 5 low_david
msp 1 4 3 5 tp w=30u l=1.2u ad=108p as=108p pd=67.2u ps=67.2u
.ends
.subckt dlatch_n 1 2 3 4 5
*               in out in_cl cl vdd
x1 3 2 5 low_buf
x2 2 3 5 high_david
msn  1 4 3 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
.ends
.subckt dlatch 1 2 8 6 3 4 5
*            in out in_cl in_cl_bar reset clock vdd
x1 1 6 8 4 5 dlatch_n
x2 6 2 7 4 5 dlatch_p
mreset1  8  3 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
mreset2  5  3 7 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
.ends
.subckt dlatch1 1 2 8 6 3 4 5
*            in out in_cl in_cl_bar reset clock vdd
x1 1 6 8 4 5 dlatch_n
x2 6 2 7 4 5 dlatch_p
mreset1  8  3 5 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
mreset2  7  3 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
.ends
*
.subckt count1 1 3 6 7 5
*             out 01out reset clock vdd
x1 1 2 12 13 6 7 5 dlatch1
x2 2 4 3 5 nor
x3 13 10 5 buf
x4 10 1 4 7 5 dlatch_p
mreset 4 6 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
.ends
.subckt count 1 9 3 6 7 5
*            out 01in 01out reset clock vdd
x1 1 2 12 13 6 7 5 dlatch
x2 2 4 3 5 nor
x3 8 12 10 5 nexor
x4 10 1 4 7 5 dlatch_p
mreset1 5 6 4 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
mreset2 8 6 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
```

```
ms 9 7 8 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
.ends
*
* circuit description
*
x1 1 5 8 9 10 count1
x2 2 5 6 8 9 10 count
x3 3 6 7 8 9 10 count
x4 4 7 15 8 9 10 count
x5 16 15 17 8 9 10 count
x6 19 17 18 8 9 10 count
x8 20 18 22 8 9 10 count
x9 21 22 23 8 9 10 count
*
vdd   10   0   dc  3v
vcl 999 0 pulse(0 3 4n 1n 1n 4n 10n)
xcl 999 9 10 driver2
vreset 11 0 pulse(0 3 0n 1n 1n 3n 50000n)
x7 11 9 8 10 reset
*
*
.tran 1n 2564n
.option post tnom=27 limpts=50000 itl5=100000
.temp 27
.print tran power
.meas tran avgval avg power from=4n to=2564n
.meas tran rmsval rms power from=4n to=2564n
.meas tran maxval max power from=4n to=2564n
.end
```

```
Fast modular counter
.include  '/home/slug/vstrael/models/utmc.m'
* optimized size for latches
*
*
.subckt nand 1 2 3 4
*            in out vdd
m1  3 1 4 4 tp w=5u l=1.2u ad=18p as=18p pd=17.2u ps=17.2u
m2  3 2 4 4 tp w=5u l=1.2u ad=18p as=18p pd=17.2u ps=17.2u
m3  3 1 5 5 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m4  5 2 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt nor 1 2 3 4
m1  5 2 4 4 tp w=12u l=1.2u ad=43.2p as=43.2p pd=31.2u ps=31.2u
m2  3 1 5 5 tp w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m3  3 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m4  3 2 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt inverter 1 2 3
m1  2 1 3 3 tp w=4u l=2.4u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m2  2 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt big_inverter 1 2 3
m1  2 1 3 3 tp w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m2  2 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt driver2 1 2 3
m1  2 1 3 3 tp w=300u l=1.2u ad=1080p as=1080p pd=607.2u ps=607.2u
m2  2 1 0 0 tn w=150u l=1.2u ad=540p as=540p pd=307.2u ps=307.2u
.ends
.subckt exor 1 2 7 8
*           in1 in2 out vdd
x1 1 3 8 inverter
x2 2 4 8 inverter
x3 2 3 5 8 nand
x4 4 1 6 8 nand
x5 5 6 7 8 nand
.ends
*
.subckt nexor 1 2 6 11
x1 1 3 11 inverter
x2 2 4 11 inverter
x3 5 6 11 big_inverter
m1  7 2 11 11 tp w=16u l=1.2u ad=57.6p as=57.6p pd=39.2u ps=39.2u
m2  8 1 11 11 tp w=16u l=1.2u ad=57.6p as=57.6p pd=39.2u ps=39.2u
m3  5 3 7 11 tp w=16u l=1.2u ad=57.6p as=57.6p pd=39.2u ps=39.2u
m4  5 4 8 11 tp w=16u l=1.2u ad=57.6p as=57.6p pd=39.2u ps=39.2u
m5  5 4 9 9 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m6  9 3 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m7  5 2 10 10 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m8  10 1 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
.ends
*
.subckt david 1 2 3
m1  2 1 3 3 tp w=4u l=5u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m2  2 1 0 0 tn w=4u l=10u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt low_david 1 2 3
m1  2 1 3 3 tp w=4u l=5u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m2  2 1 0 0 tn w=4u l=5u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt buf 1 2 3
m1  2 1 3 3 tp w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m2  2 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
```

```
.ends
.subckt high_buf 1 2 3
m1  2 1 3 3 tp w=25u l=1.2u ad=90p as=90p pd=57.2u ps=57.2u
m2  2 1 0 0 tn w=4u l=1.2u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt high_david 1 2 3
m1  2 1 3 3 tp w=4u l=4u ad=14.4p as=14.4p pd=15.2u ps=15.2u
m2  2 1 0 0 tn w=4u l=12u ad=14.4p as=14.4p pd=15.2u ps=15.2u
.ends
.subckt low_buf 1 2 3
m1  2 1 3 3 tp w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
m2  2 1 0 0 tn w=25u l=1.2u ad=90p as=90p pd=57.2u ps=57.2u
.ends
.subckt reset 1 4 2 3
*            in reset out vdd
m1  6 1 3 3 tp w=10u l=1.2u ad=36p as=36p pd=27.2u ps=27.2u
m2  6 4 5 5 tn w=5u l=1.2u ad=18p as=18p pd=17.2u ps=17.2u
m3  5 1 0 0 tn w=5u l=1.2u ad=18p as=18p pd=17.2u ps=17.2u
m4  2 6 3 3 tp w=30u l=1.2u ad=108p as=108p pd=67.2u ps=67.2u
m5  2 6 0 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
.ends
.subckt dlatch_p 1 2 3 4 5
*               in out in_cl cl vdd
x1 3 2 5 high_buf
x2 2 3 5 low_david
msp 1 4 3 5 tp w=30u l=1.2u ad=108p as=108p pd=67.2u ps=67.2u
.ends
.subckt dlatch_n 1 2 3 4 5
*               in out in_cl cl vdd
x1 3 2 5 low_buf
x2 2 3 5 high_david
msn  1 4 3 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
.ends
.subckt dlatch 1 2 8 6 3 4 5
*            in out in_cl in_cl_bar reset clock vdd
x1 1 6 8 4 5 dlatch_n
x2 6 2 7 4 5 dlatch_p
mreset1  8  3 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
mreset2  5  3 7 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
.ends
.subckt dlatch1 1 2 8 6 3 4 5
*            in out in_cl in_cl_bar reset clock vdd
x1 1 6 8 4 5 dlatch_n
x2 6 2 7 4 5 dlatch_p
mreset1  8  3 5 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
mreset2  7  3 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
.ends
*
.subckt count1 1 3 6 7 5
*             out 01out reset clock vdd
x1 1 2 12 13 6 7 5 dlatch1
x2 2 4 3 5 nor
x3 13 10 5 buf
x4 10 1 4 7 5 dlatch_p
mreset 4 6 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
.ends
.subckt count 1 9 3 6 7 5
*            out 01in 01out reset clock vdd
x1 1 2 12 13 6 7 5 dlatch
x2 2 4 3 5 nor
x3 8 12 10 5 nexor
x4 10 1 4 7 5 dlatch_p
mreset1 5 6 4 0 tn w=15u l=1.2u ad=54p as=54p pd=37.2u ps=37.2u
mreset2 8 6 0 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
```

```
ms 9 7 8 0 tn w=8u l=1.2u ad=28.8p as=28.8p pd=23.2u ps=23.2u
.ends
*
* circuit description
*
x1 1 5 8 9 10 count1
x2 2 5 6 8 9 10 count
x3 3 6 7 8 9 10 count
x4 4 7 15 8 9 10 count
x5 16 15 17 8 9 10 count
x6 19 17 18 8 9 10 count
x8 20 18 22 8 9 10 count
x9 21 22 23 8 9 10 count
*
vdd   10   0   dc  3v
vcl 999 0 pulse(0 3 4n 1n 1n 4n 10n)
xcl 999 9 10 driver2
vreset 11 0 pulse(0 3 0n 1n 1n 3n 50000n)
x7 11 9 8 10 reset
*
*
.tran 1n 2564n
.option post tnom=27 limpts=50000 itl5=100000
.temp 27
.print tran power
.meas tran avgval avg power from=4n to=2564n
.meas tran rmsval rms power from=4n to=2564n
.meas tran maxval max power from=4n to=2564n
.end
```

APPENDIX A

Preliminary Gas Microstrip Detector Readout Characteristics

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0. Introduction

In order to avoid stability problems due to temperature variations, a new circuit with local feedback was designed. The readout circuit consists of five amplifier stages, followed by a comparator. In a first stage, the input current is transformed into a voltage by means of a resistive feedback. In the second stage, the voltage is again transformed into a current. This process is again repeated in the third and fourth stage. In the fifth stage the final output voltage is created by the transformation I-to-V. An advantage of using five stages is that the whole chain can be considered as a pipeline. While a first signal is still propagating, a second input signal can be applied to the recovered input stage.

1. Dynamic Range (Fig. 1a, b)

All simulations were done with a δ-pulse current signal with zero rise and fall time and a pulse width of 1 ns. A δ-pulse of 1 μA corresponds to the deposition of 1 fC of charge on the input capacitor of 5 pF.

In order to be sensitive to small signals, the gain has to be large enough. However, since the output voltage swing is limited by the supply voltage to roughly 3 V, care has to be taken that the preamp output stage does not saturate. The dynamic range over which the amplifier behaves normal is [Q_{min}, Q_{min} + 3 V/(gain [V/fC])], where Q_{min} is the minimum input signal to which the preamp (more particular the comparator) is sensitive, which is for this first design. ≈ 0.7 fC. The worst case dynamic range, corresponding to the maximum gain of 450 mV/fC, becomes **[0.7 fC, 7.4 fC]**. From the simulation results it can be seen that the amplifier saturates for input signals in excess of 7.4 fC. The dynamic range can only be improved by using a larger supply voltage. This will however increase the power dissipation. For further optimization the most important range of input signals has to be known.

2. Bandwidth (Fig. 2, 3a, 3b)

The complete transimpedance amplifier has a bandwidth around **20 MHz** (Fig. 2), with a DC transresistance V_{out}/I_{in} ≈ **3 MΩ**. The transfer characteristics of the individual

stages (Fig. 3a, b), this is V/I for the fist, third and fifth stage and I/V for the second and fourth stage are given in Table 1.

Table 1: Characteristics of the 5 amplifier stages.

First stage	V/I ≈ 65 kΩ
Second stage	I/V ≈ 144 μS
Third stage	V/I ≈ 62 kΩ
Fourth stage	I/V ≈ 10 μS
Fifth stage	V/I ≈ 30 kΩ

3. Power dissipation

The circuit works on a ± 2.5 V power supply. The total power dissipation is **6.4 mW** and consists of 4.85 mW for the five gain stages and 2.65 mW for the comparator.

4. Slewing (Fig. 4)

The maximum slewing is **16 ns**, measured at the zero crossing of the comparator output. This value can however be optimized by shifting the threshold of the comparator. From the simulation results it can be seen that the comparator is the main cause of the slewing. For small input signals, the force pulling this circuit out of its equilibrium is very small.

5. Noise

The following is part of the HSPICE output file:

frequency = 100 Mhz

**** total output noise voltage = 307.0957f sq V/Hz
= 554.1622 nV/rt Hz

transfer function value:
v(17)/in = 684.3476 kΩ
equivalent input noise at Iin = 809.7671 fA/rt Hz

**** total output noise voltage = 13.3485 mV volts
**** total equivalent input noise = 4.9135 nA

This is the total noise integrated over the frequency range [1 Hz, 100 MHz]. It corresponds to an ENC ≈ 31 e^- rms /ns integration time. The noise threshold of 1000 e^- rms is reached after ≈ 33 ns integration.

6.Stability with temperature

The DC output voltage changes by ≈ 29 mV/°C. The circuit is still working correctly at 0 and 100 °C.

APPENDIX B

Improved Gas Microstrip Detector Readout v2.0

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A VLSI readout system was designed for GMDs [0]. A drawback of this design was the high power dissipation and slewing. In this optimized design, it was tried to bring the power dissipation down to 1 mW, while at the same time reducing the slewing to a value less than 8 ns. Since the electron drift time varies from 0 to 7 ns [1], the slewing must be less than 9 ns in order to have a total time uncertainty less than the bunch crossing time. Furthermore, the circuit was optimized for an input dynamic range 4 - 40 fC. In the readout circuit the number of stages was reduced to 3, being an I-to-V, a V-to-I and again an I-to-V stage. The amplifier stages are followed by a comparator with recovery feedback [2]. This readout system is shown in Figure 1.

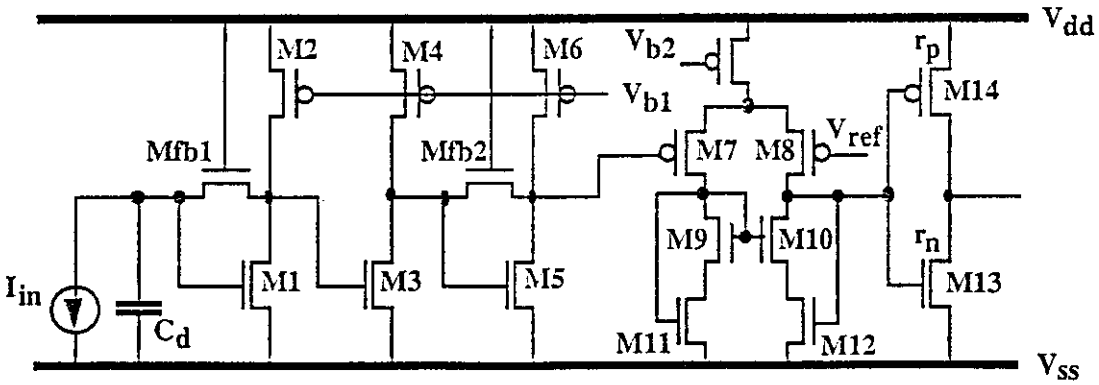

Fig. 1: I-to-V, V-to-I and I-to-V stage, followed by a comparator.

1. Dynamic Range

As before, all simulations were done with a δ-pulse current signal with zero rise and fall time and a pulse width of 1 ns. A δ-pulse of 1 μA corresponds to the deposition of 1 fC of charge on the detector capacitor C_d of 5 pF. Figure 2 gives the total gain as a function of the input signal. It can be seen that the circuit behaves linearly for input signals smaller than 10 fC. For larger signals the gain decreases. This is however not caused by 'saturation' in the meaning of a clipping of the internal signal against the power rails, but by the load of the third stage being driven into the linear region of operation.

Since this effect does not deteriorate the recovery time, 40 fC is a valid input signal and the dynamic range can be defined as [0.2 fC, 40 fC].

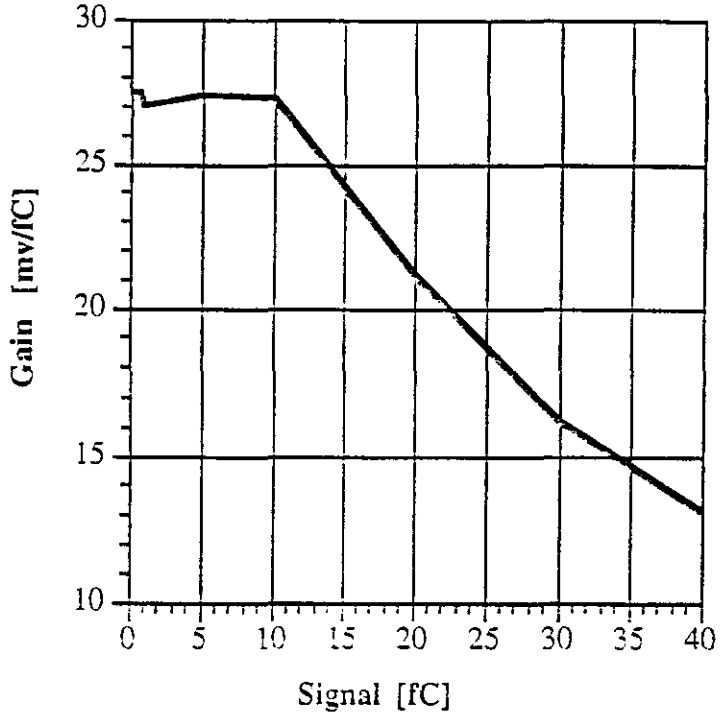

Figure 2: Total gain as a function of the input signal

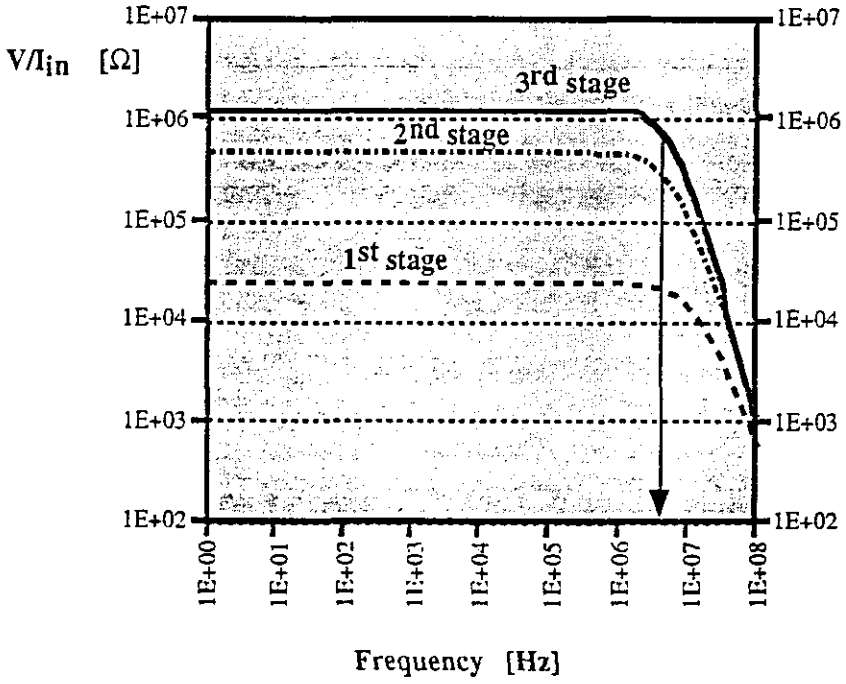

Fig. 3: Bandwidth and gain of the 3 stages.

2. Bandwidth

The complete transimpedance amplifier has a bandwidth around **70 MHz** (Fig. 3), with a DC transresistance $V_{out}/I_{in} \approx 1$ MΩ. The compensation capacitors, which were required in the 5-stage design, could be eliminated here because of the decreased gain.

3. Power dissipation

The circuit works on a ± 2.5 V power supply. The total power dissipation is **1.6 mW** and consists of 0.7 mW for the three gain stages and 0.9 mW for the comparator, the largest part of which is taken by the output inverter. The reason for this high value is explained more in detail in the next section.

4. Slewing

The maximum slewing is 8 ns, measured at the zero crossing of the comparator output. This value depends for a given reference voltage V_{ref} strongly on the threshold voltage of the output inverter of the comparator. Figure 4a shows the maximum slewing (occurring for small input signals) as a function of $r_p/r_n = (W_p/L_p)/(W_n/L_n)$. When the width of the p-channel device is increased, the inverter threshold is shifted upwards. This is seen in Figure 4b, giving the inverter threshold voltage as a function of r_p/r_n. The threshold voltage is very sensitive to the exact device sizes around $V_{th} \approx 0$. In this region the optimization for minimum slewing is difficult. For this reason, V_{ref} is set such that the DC output voltage of the comparator is located in the less critical area above 0.2 V (V_{ref} = -0.2 V, V_{DC} = 0.277 V). In practice V_{ref} will have to be changed until a minimum value for the slewing is obtained. It can be seen that the best result is obtained for the maximum inverter threshold that is still below the DC output voltage of the comparator, or in other words, such that the DC output voltage of the comparator is considered as a 'high' signal. When a signal is applied, the comparator output voltage goes down and crosses the inverter threshold voltage, causing the latter to trip. The explanation for this behavior is that in this case the DC output voltage of the comparator is in the steep high gain (and high current) region of the DC transfer characteristic of the inverter. A small change in input voltage will move the output voltage of the inverter to one of the supply voltages. From Figure 4b, it can be noticed that the price to be paid for a small value of the slewing is power. The values given depend however strongly on the load of output inverter. In the simulations, the load capacitance was taken to be 200 fF, and for this case

a device length of 2 μm was necessary for both the n-channel and p-channel device. If the load capacitance allows the device length to be increased, then a considerable reduction in power dissipation is possible. A length of 4 μm already reduces the dissipation to 0.6 mW. There is no way to avoid this effect.

Finally, Figure 5 gives the delay for the optimum case as a function of the input signal.

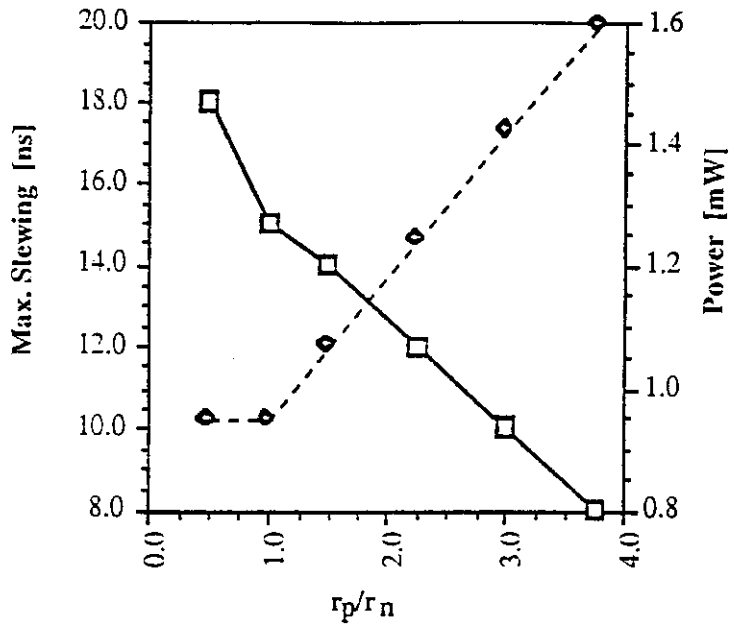

Figure 4a: Slewing as a function of $r_p/r_n = (W_p/L_p)/(W_n/L_n)$.

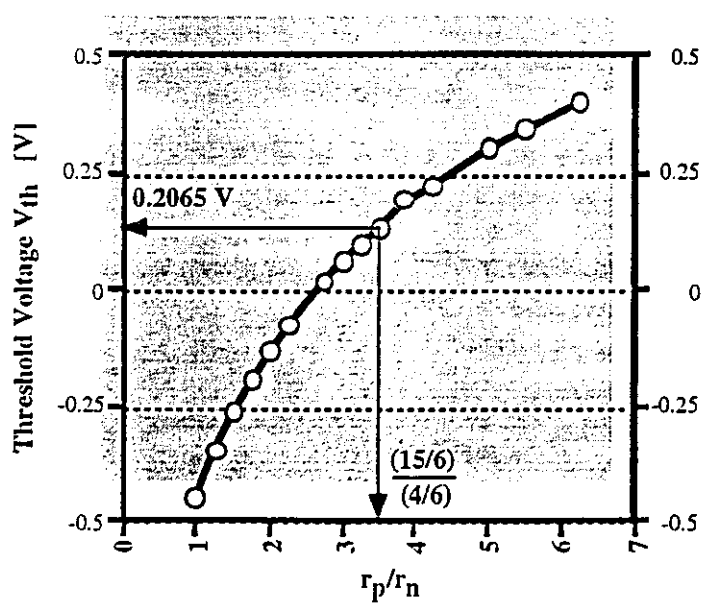

Fig. 4b: Inverter threshold voltage as a function of r_p/r_n.

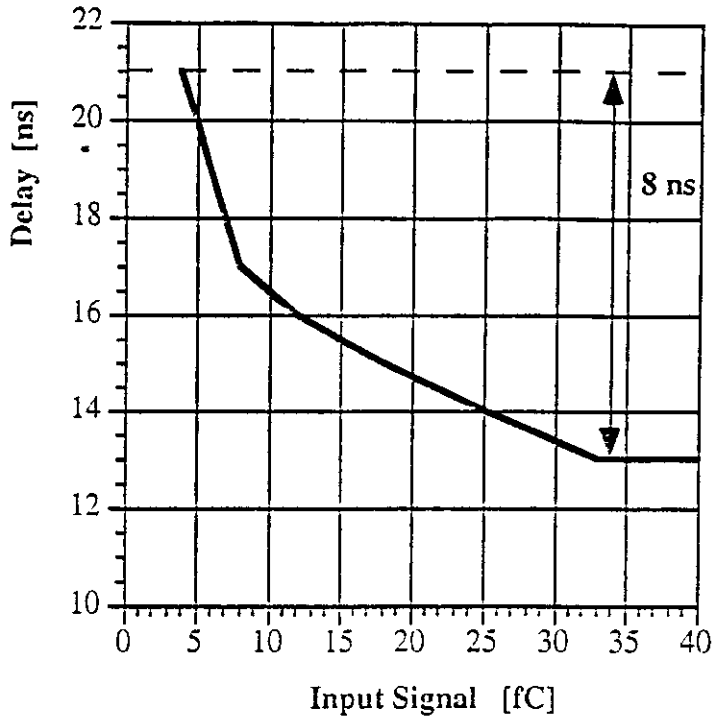

Figure 5: Delay for the optimum case as a function of the input signal.

5. Noise

The following is part of the HSPICE output file:

f = 100 MHz

```
**** total output noise voltage      =  1.9055 f sq v/hz
                                     = 43.6524 nV/rt hz
   transfer function value:
    v(7)/in                          = 878.2854
   equivalent input noise at in      =  49.7019 pA/rt hz

**** total output noise voltage  =   4.6904 mV
**** total equivalent input noise =  269.8150 nA
```

This is the total noise integrated over the frequency range [1 Hz, 100 MHz]. It corresponds to an ENC ≈ 1700 e^- rms /ns integration time. The reason for the increased input referred noise compared with the first design, is the lower gain (27.5 mV/fC instead of 650 mV/fC). An apparent question is: "Why not increasing the gain by a factor of two,

such that the input referred is reduced by the same factor?". This is very easy in words, but in practice reducing the gain means changing device sizes by fractions of a micron. This is something to be avoided in an only 1.2 μm CMOS process. Even with the high noise of 1700 e^-, the Signal to Noise ratio S/R is still ≈ 15 for the minimum input signal of 4 fC.

6. Stability with temperature

The DC output voltage of the preamps changes at a rate < 11 mV/°C. To keep the circuit working correctly at different temperatures, the comparator reference voltage, V_{ref}, has to be changed. This can be seen from Table 1.

Table 1: DC output voltage at the preamp output and V_{ref} to be used.

	0 °C	27 °C	50 °C
DC voltage @ output preamp	-347.7 mV	-142.0 mV	213.8 mV
V_{ref} to be used	-400 mV	-200 mV	150 mV

7. Conclusion

The circuit that was demonstrated fulfills all requirements except power dissipation. It is possible to reduce the power dissipation further by increasing the bias voltage V_{b1} (Fig. 1). However, because the threshold voltage, V_T, of the p-channel devices will increase after radiation, it is better to keep small safety margin $V_{dd} - V_{b1} - V_T$. The largest part of the power dissipation is taken by the output inverter of the comparator. In order to have a fast response, which depends little on the amplitude of an incomming signal, the inverter has to be biased in its high gain and also high current mode. The maximum current that is needed to obtain a certain speed depends on the load capacitance. In order to be able to make a more accurate estimate of the dissipation, it is important to know what follows the comparator. In the best case it is an output buffer (Cin < 30 fF), which would allow to bring the dissipation within the specification of 1 mW.

Because the requirements for this circuit really stretch the limits of what is possible in terms of slewing and power dissipation, the characteristics of prototypes will probably be

very sensitive to process variation, but this is something that can not be taken in consideration before prototypes have been made and have been tested.

References

[0] "Preliminary Gas Microstrip Detector Readout Characteristics", G. Vanstraelen.

[1] "Conceptual Design Intermediate Angle Track Detector", SDC-92-171, January 20, 1992.

[2] "Low-Voltage-Swing CMOS Transceivers", G. Vanstraelen and J. Dorenbosch, SSCL-608, December 1992.