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Integrated APD Quenching Circuit

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1. Introduction

Avalanche Photo Diodes (APD's) are silicium diodes that are used with a reverse bias in excess of the breakdown voltage. Charge generated in the depletion layer (e.g. by photons) is accelerated towards the electrodes by the high electric field. During their movement, the carriers collide with the silicium lattice and generate additional charge, which in turn goes through the same process of acceleration and collision. The net effect is an avalanche. A recovery from avalanche is only possible if the voltage across the diode is lowered to a value below the breakdown voltage, and this is where the quenching circuit comes in. Figure 1 shows a block diagram of the quenching circuit that was built using discrete components* . The circuit consists of a tristate buffer, a comparator (preferably with hysteresis) and a delay circuit. The operation is as is described next. In avalanche the voltage across the APD increases by 30 mV/ns. When the voltage applied to the comparator input exceeds the reference voltage applied to the comparator, the latter will trip, bringing the output from a low to a high state. The 'high' signal enables the tristate driver, taken to be inverting in this example, which output is connected to the diode.

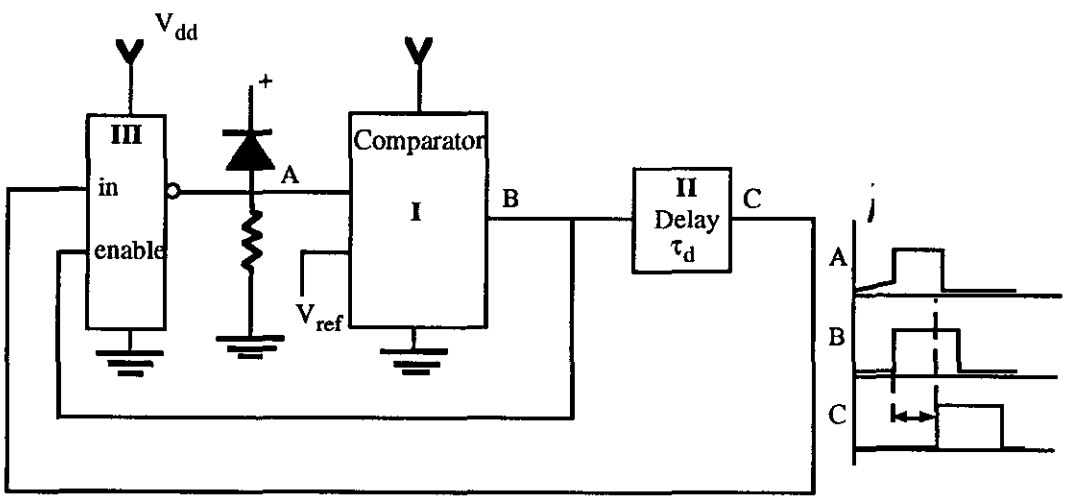

Fig. 1: Block-diagram for the quenching circuit and timing diagram.

* T. Regan et al (1991)

At this time, the input to the tristate is still low because of the delay introduced by the delay circuit, which means that the tristate output will go high, hereby quenching the APD. When the 'high' output of the comparator has rippled through the delay circuit, the output of the tristate goes low and this resets the diode to its original voltage. As soon as the diode voltage is low again, the comparator will recover and disable the tristate. In order to provide some noise immunity the comparator must have hysteresis. The pulse width of the quenching signal should be variable in the range between 20 and 50 ns. A further requirement is TTL compatibility of the output signals of the circuit.

2. Integrated version

Figure 2 displays the schematic for the ASIC version of the quenching circuit. The comparator is a very basic two stage comparator with hysteresis. Because the reference voltage V_{ref} is near to zero, the supply voltage for the comparator was chosen to be ±5 V.

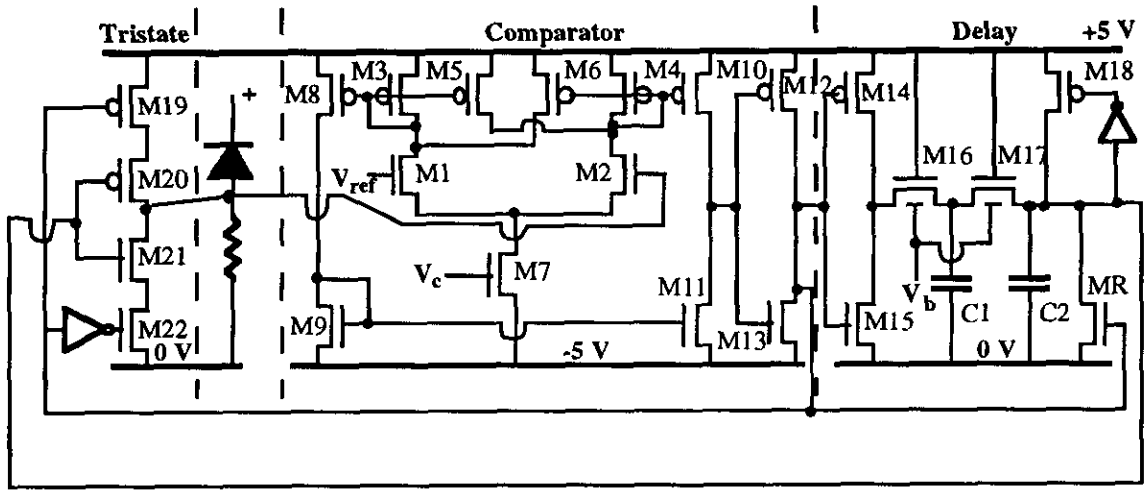

Fig. 2: ASIC version of the quenching circuit.

V_{ref} is applied to the inverting input, the diode is connected to the non-inverting input terminal. The hysteresis is obtained as a difference in positive (M5, M6) and negative (M3, M4) feedback gain. Small hysteresis values are obtained by making (M3, M5) and (M4, M6) almost equal in size. However, the exact hysteresis value then becomes very sensitive to process variation. In this design, a hysteresis value of approximately 30 mV was chosen. This is shown in figure 3, giving the DC transfer characteristic for the comparator. To provide a full output voltage swing, the comparator is followed by an inverter with

threshold voltage around 0.6 V. This threshold value allows a large spread in DC output voltage for the comparator (-5 V to 0.6 V) without affecting the correct operation . The output of this inverter will go low in the case of a positive input signal. The delay introduced by the comparator is in between 17 ns and 20 ns. No significant slewing was found in the SPICE simulations. The comparator keeps working correctly for V_c values larger than -2.3 V.

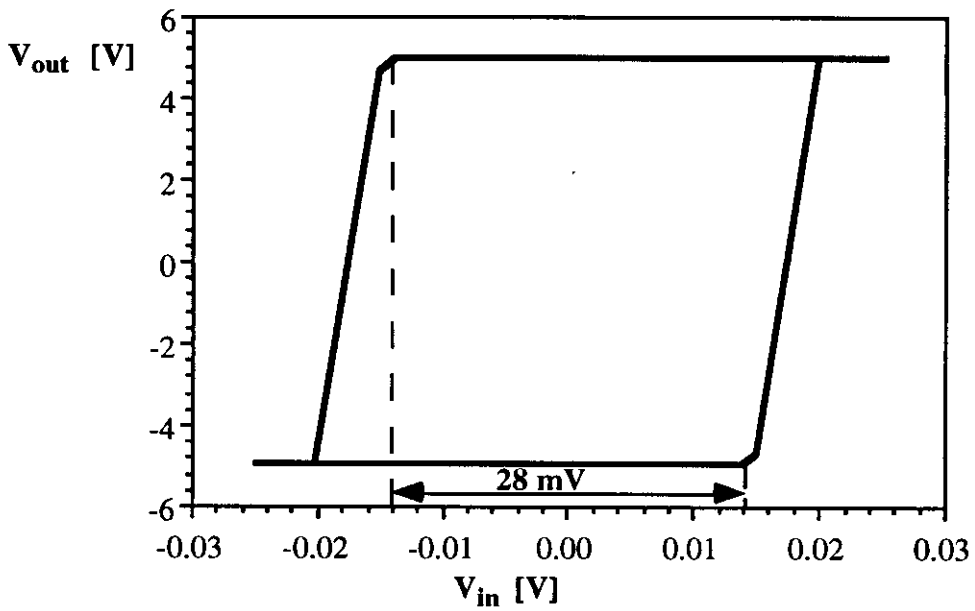

Fig. 3: DC transfer characteristic for the comparator showing an hysteresis of 28 mV.

The delay circuit consists of an inverter, two RC elements in series and a signal recovery circuit. The resistors are formed by nMOS transistors with the gate connected to the positive power supply. The back-gate can be used to modify the resistance. The capacitors C1 and C2 are both 0.68 pF. In the single poly layer process that is used, they are both formed by an n-channel device of 20x20 μm^2 with the gate being one terminal, and source, drain and p-well, all connected to Gnd (0 V), being the second terminal. In passing a high voltage through a n-channel device, a signal loss equal to the threshold voltage of the device occurs. As a result, if, by the application of a non-zero bulk-to-source voltage, V_{bs}, to increase the delay, the threshold voltage becomes larger than the switching threshold of the tristate ($\approx$ 2.4 V), the quenching will never halt. For this reason, a signal recovery circuit is provided. When the output voltage of the delay circuit supersedes the threshold voltage of the inverter driving M17, the latter is switched on and recovers the signal. The threshold for this inverter is put at 2.3 V, as such allowing for a maximum

signal loss of 2.7 V. Figure 4 gives the pulse width of the tristate output signal as a function of the substrate bias for the pass transistors.

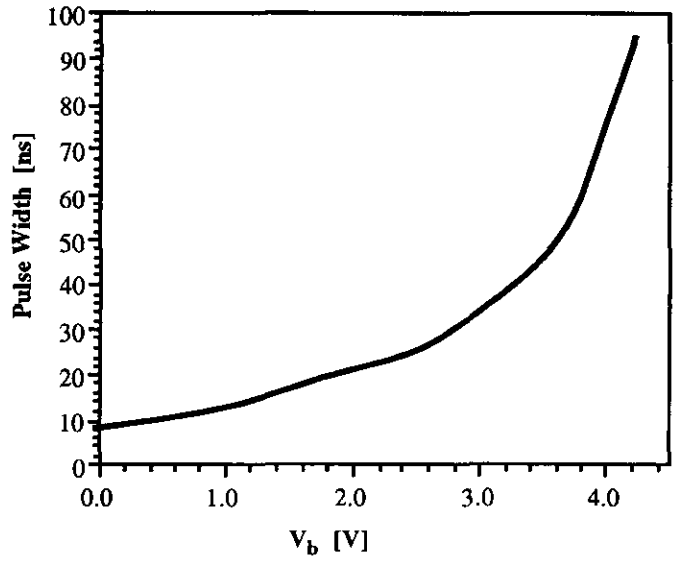

Fig. 4: Width of the output signal of the tristate as a function of the substrate bias for the pass transistors.

An extra reset transistor driven by the comparator output is used to avoid an unnecessary delay of the return signal of the comparator, which would put a lower limit on the minimum time that has to elapse before the comparator can react to a new signal. The shape of the output signal of the three parts of the circuit is seen in Figure 5.

3. Transistor parameters

Table 1 summarizes for $V_{ref} = 0.1$ V the size, gate-to-source voltage V_{gs}, drain-to-source-voltage V_{ds}, current I_{ds}, transconductance g_m and output impedance g_{ds} of the various transistors used in the design. The total static power dissipation of the circuit is 12.2 mW for $V_c = -2.3$ V.

4. The chip

The chip that was layed out (Fig. 6) has 8 channels on a pitch of 90 μm. The chip size is 1.3 x 1.7 mm^2. The comparator output signal is buffered to TTL level and is made available off chip. The buffering is done using a cascade of four CMOS inverters (Fig. 7).

The width of the n-channel devices in these inverters is respectively 5 μm, 15 μm, 45 μm and 150 μm. Their length is 1.2 μm. The p-channel devices are twice as wide. The buffer should be able to drive a 10 pF load capacitor at 50 MHz. Figure 7 shows the layout for the quenching circuit.

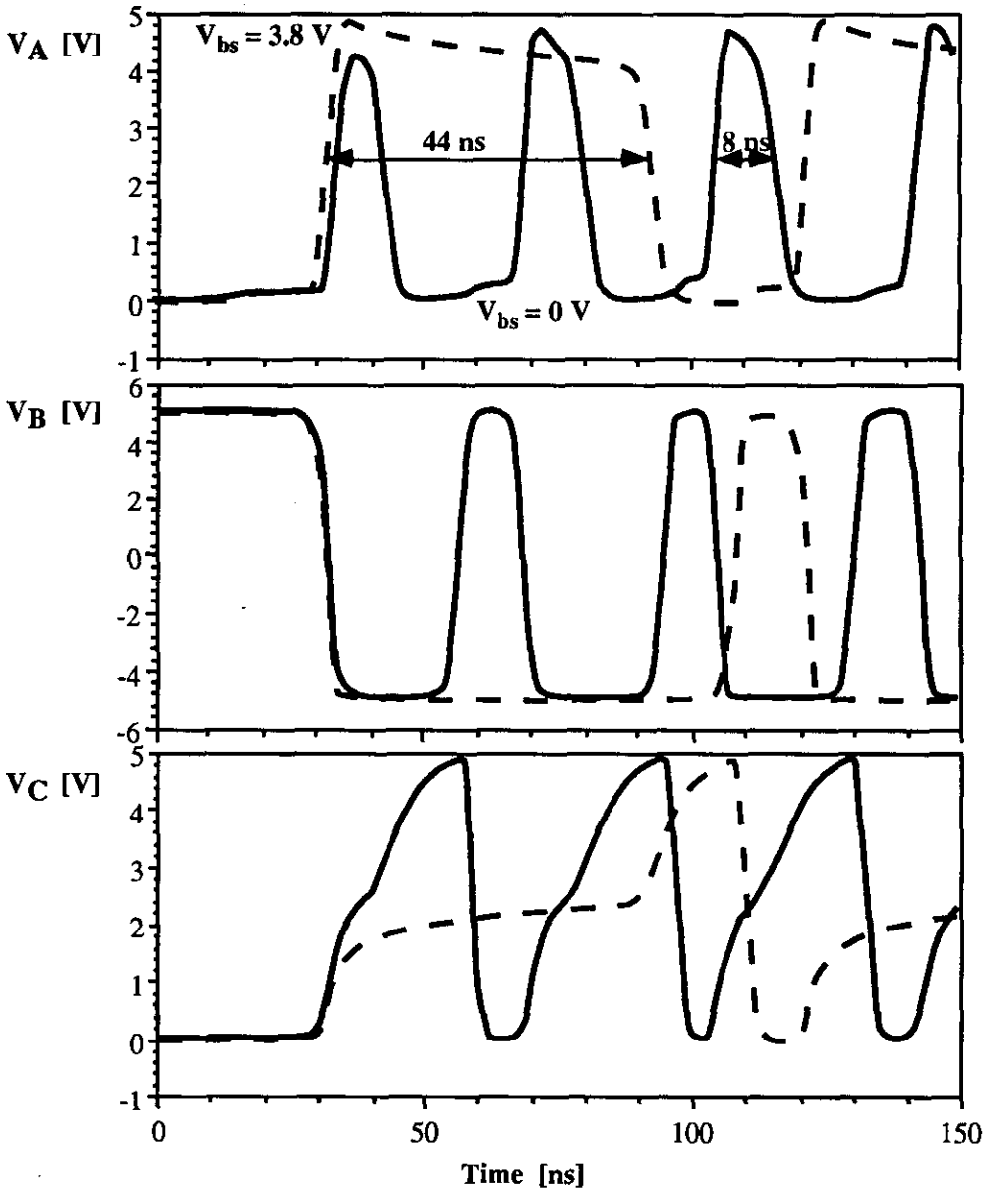

Fig. 5: Output signals from the tristate, comparator and delay circuit.

Table 1: DC-parameters for the transistors used in the design, V_{ref} = 0.1 V.

Device	W/L	I_{ds} [mA]	V_{gs} [V]	V_{ds} [V]	g_m [mS]	g_{ds} [μS]
M1	40/1.5	0.63	1.65	4.71	1.28	2.78
M2	40/1.5	0.52	1.55	6.0	1.18	2.55
M3	46/1.2	0.63	-1.85	-1.85	1.12	26.39
M4	46/1.2	0.0	-0.53	-0.53	0.0	0.0
M5	50/1.2	0.52	-1.85	-0.53	0.63	0.77
M6	50/1.2	0.0	-0.53	-1.85	0.0	0.0
M7	20/1.5	1.15	2.70	3.45	1.08	2.34
M8	4/1.2	0.067	-1.85	-8.42	0.12	2.92
M9	4/1.2	0.067	1.58	1.58	0.15	0.80
M10	4/1.2	0.0	-0.53	-1.0	0.0	0.0
M11	4/1.2	0.0	1.58	0.0	0.0	266.0
M12	8/1.2	0.0	-10.0	0.0	0.0	1,694.0
M13	4/2	0.0	0.0	10.0	0	0
M14	8/1.2	0.0	0.0	-5.0	0.0	0.0
M15	4/1.2	0.0	5.0	0.0	0.0	1,332.0
M16	8/1.2	0.0	5.0	0.0	0.0	1,819.0
M17	8/1.2	0.0	5.0	0.0	0.0	1,819.0
M18	4/1.2	0.0	0.0	-5.0	0.0	0.0
MR	10/1.2	0.0	5.0	0.0	0.0	3,338.0
M19	100/1.2	0.0	0.0	-3.63	0.0	0.0
M20	100/1.2	0.0	-1.37	-1.37	3.5 μS	0.0
M21	50/1.2	0.0	0.70	0.70	2.1 μS	0.0
M22	50/1.2	0.0	0.0	-0.70	0.0	0.0

5. Potential problems

A potential problem for the correct operation of the circuit could be the crosstalk from the tristate enable to the comparator input. HSPICE simulations show that when the tristate is disabled, charge is injected onto its output capacitor, hereby raising it above the comparator trip voltage. This causes the circuit to oscillate at a frequency determined by the setting of the delay circuit. For the minimum delay, the oscillation frequency is around 25 MHz. Because it is a well known fact that SPICE exaggerates the effects of crosstalk, no

special measures were taken to cancel it out. Prototypes will be measured to study this effect.

6. Conclusions

An 8 channel APD quenching circuit was designed. The circuit consists of a comparator with hysteresis (30 mV), a delay circuit to tune the width of the quenching pulse and a tristate buffer, which performs the actual quenching. The width of the quenching pulse can be changed upwards from 8 ns. The standby power dissipation of the circuit is 12.2 mW. The chip will be fabricated in the 1.2 μm, radhard p-well CMOS process of UTMC.

```
*****************************************************
* APD quenching circuit - comparator with hysteresis *
*****************************************************
*
vb 333 0 dc -5
* substrate bias for pass gate
vb2 334 0 dc -3.8
* substrate bias for recovery inverter
vb3 335 0 dc 0
* power supply
VDD 20 0  5
VSS 19 0 -5
* Bias for ampli tail current source
v0 21 0 dc 0
vc 22222 0 dc -2.3
*
Vin0 1 0 .1
*
*
* Comparator
*
.subckt cwh 5 6 17 19 20 21
*         in1 in2 out vss vdd vs
* 5 is negative input
m10 14 21 19  19  tn w=20u   l=1.5u   ad=36p as=36p pd=27.2u ps=27.2u
m11 12 5  14 14  tn w=40u  l=1.5u ad=144p  as=144p  pd=87.2u ps=87.2u
m12 13 6  14 14  tn w=40u  l=1.5u ad=144p  as=144p  pd=87.2u ps=87.2u
m13 12 12 20 20 tp w=45.9u l=1.2u  AD=180P AS=180P PD=107.2U PS=107.2U
m14 13 13 20 20 tp w=45.9u l=1.2u   AD=180P AS=180P PD=107.2U PS=107.2U
m13b 13 12 20 20 tp w=50u l=1.2u  AD=180P AS=180P PD=107.2U PS=107.2U
m14b 12 13 20 20 tp w=50u l=1.2u   AD=180P AS=180P PD=107.2U PS=107.2U
m15 22 12 20 20 tp w=4u l=1.2u   AD=14.4P AS=14.4P PD=15.2U PS=15.2U
m16 23 13 20 20 tp w=4u l=1.2u   AD=14.4P AS=14.4P PD=15.2U PS=15.2U
m17 22 22  19 19  tn w=4u  l=1.2u ad=14.4p  as=14.4p  pd=15.2u ps=15.2u
m18 23 22  19 19  tn w=4u  l=1.2u ad=14.4p  as=14.4p  pd=15.2u ps=15.2u
x1 23 17 19 20 high_inverter
*x2 17 18 19 20 inverter
.ends
*
* Delay circuits
*
.subckt delay 1 2 3 4 5
*            in out vss vdd vb
x1 1 6 3 4 inverter
*m1 6 3  2  4  tp  w=4U  L=1.2U ad=57.6p as=57.6p  pd=39.2u   ps=39.2u
m2 6 4  2  5  tn  w=8U  L=1.2U ad=57.6p as=57.6p  pd=39.2u   ps=39.2u
.ends
.subckt delay2 1 2 3 4 5 9
*            in out vss vdd vb vbi
x1 1 6 3 4 inverter
m2 6 4  8  5  tn  w=8U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
cd1 8 0 0.6p
m3 8 4  2  5  tn  w=8U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
cd2 2 0 0.6p
m1 2 7  4  4  tp  w=4U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
x2 2 7 3 4 9 binv
.ends
.subckt delay3 1 2 3 4 5 9
*            in out vss vdd vb vbi
x1 1 6 3 4 inverter
m2 6 4  8  5  tn  w=8U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
xcd1 8 3 cap
m3 8 4  2  5  tn  w=8U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
xcd2 2 3 cap
```

```
m1 2 7  4  4  tp  w=4U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
x2 2 7 3 4 9 binv
.ends
*
* Tristate buffers
*
.subckt tri 1 2 3 4 5
*          in out c vss vdd
x1 3 8 4 5 small_inverter
m1 6 3  5  5  tp  w=32U   L=1.2U ad=115.2p as=115.2p  pd=71.2u   ps=71.2u
m2 2 1  6  5  tp  w=32U   L=1.2U ad=115.2p as=115.2p  pd=71.2u   ps=71.2u
m3 2 1  7  7  tn  w=16U  L=1.2U ad=57.6p as=57.6p  pd=39.2u   ps=39.2u
m4 7 8  4  4  tn  w=16U  L=1.2U ad=57.6p as=57.6p  pd=39.2u   ps=39.2u
.ends
.subckt trib 1 2 3 4 5 10
*          in out c vss vdd vb
x1 3 8 4 5 small_inverter
m1 6 3  5  5  tp  w=100U   L=1.2U ad=360p as=360p  pd=207.2u   ps=207.2u
m2 2 1  6  5  tp  w=100U   L=1.2U ad=360p as=360p  pd=207.2u   ps=207.2u
m3 2 1  7  7  tn  w=50U  L=1.2U ad=180p as=180p  pd=107.2u   ps=107.2u
m4 7 8  4  10  tn  w=50U  L=1.2U ad=180p as=180p  pd=107.2u   ps=107.2u
.ends
.subckt tric 1 2 3 4 5 10
*          in out c vss vdd vb
x1 3 8 4 5 inverter
m1 6 8  5  10  tn  w=16U   L=1.2U ad=57.6p as=57.6p  pd=39.2u   ps=39.2u
m2 2 1  6  5  tp  w=32U   L=1.2U ad=115.2p as=115.2p  pd=71.2u   ps=71.2u
m3 2 1  7  7  tn  w=16U  L=1.2U ad=57.6p as=57.6p  pd=39.2u   ps=39.2u
m4 7 8  4  10  tn  w=16U  L=1.2U ad=57.6p as=57.6p  pd=39.2u   ps=39.2u
.ends
.subckt binv 1 2 3 4 5
*           in out vss vdd vb
m1 2 1  4  4  tp  w=4U   L=2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
m3 2 1  3  5  tn  w=4U  L=3.5U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
.ends
.subckt high_inverter 1 2 3 4
*              in out vss vdd
m1 2 1  4  4  tp  w=8U   L=1.2U ad=28.8p as=28.8p  pd=23.2u   ps=23.2u
m2 2 1  3  3  tn  w=4U  L=2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
.ends
.subckt small_inverter 1 2 3 4
*              in out vss vdd
m1 2 1  4  4  tp  w=4U   L=2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
m2 2 1  3  3  tn  w=4U  L=4U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
.ends
.subckt big_inverter 1 2 3 4
*              in out vss vdd
m1 2 1  4  4  tp  w=12U   L=1.2U ad=32.4p  as=32.4p   pd=33.2u  ps=33.2u
m2 2 1  3  3  tn  w=6U  L=1.2U ad=16.2p as=16.2p  pd=21.2u   ps=21.2u
.ends
.subckt inverter 1 2 3 4
*              in out vss vdd
m1 2 1  4  4  tp  w=8U   L=1.2U ad=28.8p  as=28.8p   pd=23.2u  ps=23.2u
m2 2 1  3  3  tn  w=4U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
.ends
.subckt low_inv 1 2 3 4
*              in out vss vdd
m1 2 1  4  4  tp  w=4U   L=2.3U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
m2 2 1  3  3  tn  w=4U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
.ends
.subckt cap 1 2
mc 2 1  2  2  tn  w=20U  L=20U ad=72p as=72p  pd=47.2u   ps=47.2u
.ends
*
```

cwh6

```
* Circuit
*
d1  2 3333  diode
r1  2 0  100k
vd 4444 0  199.5
via 3333 4444  pulse(0 0.6 1ns 17ns 1ns 0ns 40ns)
x1 1 2 3 19 20 22222 cwh
x2 5 2 3 21 20 333 trib
x3 3 5 21 20 334 335 delay3
mr 5 3  21  21  tn  w=10U  L=1.2U ad=14.4p as=14.4p  pd=15.2u   ps=15.2u
*Cd 5 0 0.3p
cout 2 0 2p
*
.model diode d vj=1v vb=200v
*
.include '/home/slug/vstrael/models/utmc.m'
.option post nomod spice tnom=27
.temp 27
.OP
.tran 1n 150n
.print tran v(2) v(3) v(5)
*.dc vin 0.05 -0.05 0.005
*.print dc v(3)
*.dc vin -0.05 0.05 0.005
*.print dc v(3)
.end
```