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Cathode Strip Readout for the GEM Muon Detector

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1 Overview

The GEM muon detector[1] consists of an arrangement of segmented-cathode multi-wire proportional chambers called "Cathode Strip Chambers" (CSC's), surrounding the inner tracker and calorimeter portions of the detector. A typical CSC module comprises six detection layers as shown schematically in Figure 1. Each layer consists of a plane of anode wires and two cathode planes. A pattern of narrow strips running perpendicular to the wires is etched onto one of the cathode planes.

Typical individual cathode strips are 300 cm long and 5 mm wide. The cathode strip signals are short current pulses induced by the passage of a muon. The signals from each strip are amplified, integrated, and digitized by detector-mounted electronics. An offline determination of the center-of-gravity of the image charge induced on the cathode is used to provide a position resolution of about 1% of the strip pitch, or 50 μm.

A functional block diagram of a 96-channel front-end printed circuit board (FEPCB) is shown in Figure 2. For reasons explained below, each FEPCB is designed to accept inputs from 16 strips from each of the 6 layers that comprise a detector module. The signals from each strip are amplified using a MOS-based charge-sensitive preamplifier, which drives slow

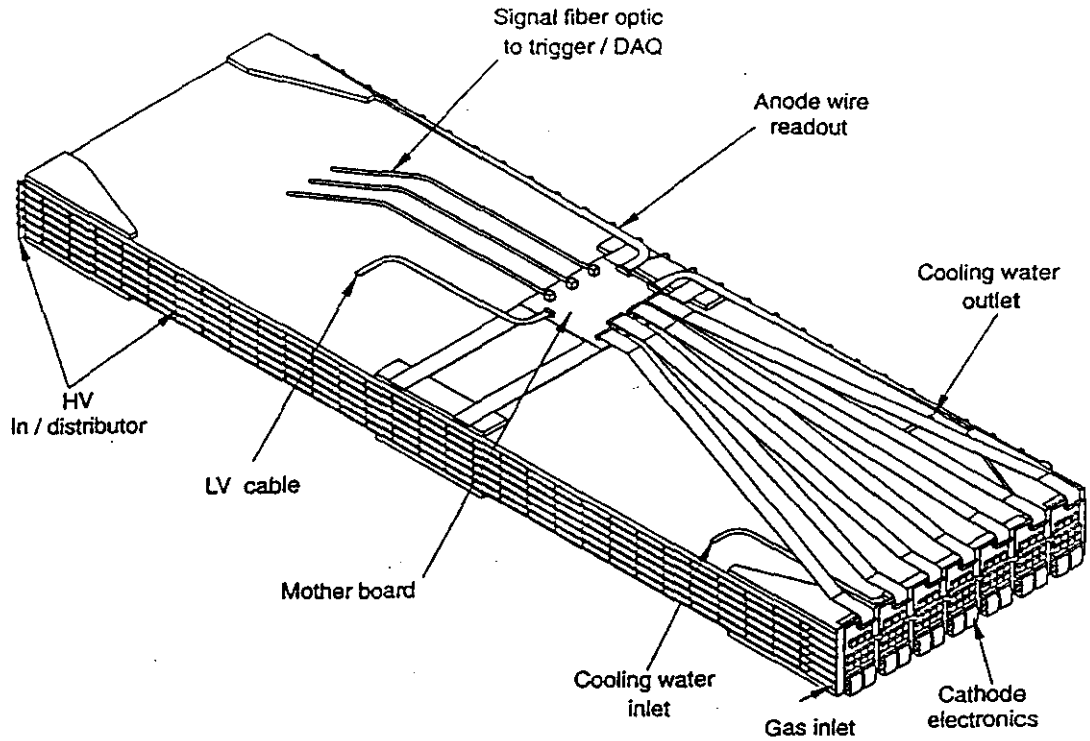

Figure 1: GEM muon detector supermodule.

and fast shaper circuits. The output of the slow shaper ($t_p \simeq 300$ ns) is used for offline pulse-height and timing measurements, whereas the output of a fast shaper ($t_p \simeq 30$ ns) drives a timing discriminator that provides input to the Level 1 trigger as well as information to steer the readout.

In this paper, we describe a design based on switched-capacitor analog storage of the preamplifier/shaper outputs from individual cathode strips. The design incorporates local logic to identify charged tracks traversing the chamber. Switched-capacitor sampling allows one to extract both pulse-height and timing information from a single data stream and provides a natural way to implement the required Level 1 trigger delay without compromising pulse-pair resolution. The GEM collaboration is also considering another scheme based on a single track and hold, which is described elsewhere[1, 2]. The charge-sensitive preamplifier and shaper circuits, which are common to both schemes, are under development at Brookhaven National Laboratory[2, 3]. The general framework of the GEM data acquisition system is described in the GEM Technical Design Report[1].

The storage locations in the switched capacitor array (SCA) are allocated in a fashion closely analogous to that described in reference [4]. The SCA must be large enough to store all samples of the shaper output pending Level 1 accept as well as those samples that have been accepted by Level 1 but have not been read out to the A/D converter. At the specified rate of 10 megasamples per second (MSPS), twenty samples are sufficient to store data for the 2 μs Level 1 latency interval. Upon receipt of a Level 1 accept, the addresses of the five samples adjacent in time to the event are stored in a buffer pending A/D conversion.

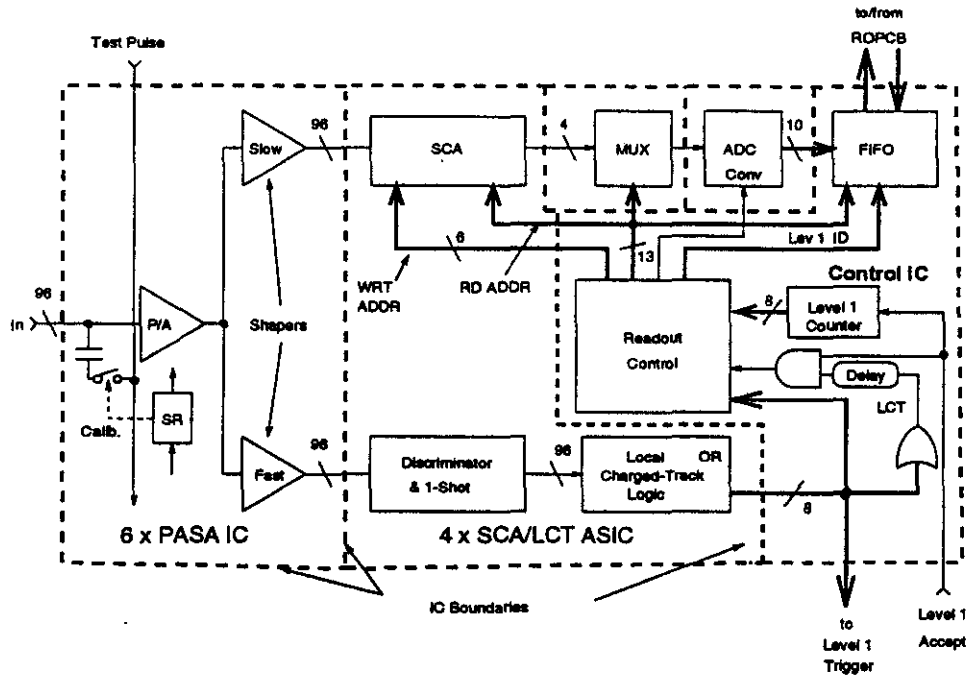

Figure 2: Block diagram of the 96-channel cathode front end printed circuit board (FEPCB).

Assuming a random (Poisson) time distribution for the Level 1 accept signals and a A/D converter throughput that is matched on average to the input rate, a 25-cell buffer—*i.e.*, five Level 1 accepts—is sufficient to retain at least 99.95% of the pending A/D conversion data.

Each 96-channel FEPCB incorporates an address list processor (Control IC) that allocates storage cell addresses, controls the sequence of A/D conversions, and reports overflow conditions when the SCA's are full. The shifting of addresses internal to the list processor allows data to be kept in the same storage cell as long as it remains in the SCA.

The SCA storage cells must provide adequate signal-to-noise ratio to permit interpolation of the track position to 1% of the strip spacing, and enough dynamic range to accommodate chamber gain variations and Landau fluctuations in the amount of ionization from charged tracks. At least ten, and preferably eleven, bits of dynamic range are needed to meet these requirements.

The SCA readout rate would normally be designed to keep up with the average Level 1 accept rate of 100 kHz and five samples per Level 1 accept. However, the corresponding average readout rate of 500 kHz would place excessive strain on the readout system, and, considering the low occupancy for individual strips, would be significantly higher than actually necessary. The system has therefore been designed such that only strips in the vicinity of charged tracks are read out. A key ingredient in this approach is the formation of a local charged track (LCT) signal that is asserted whenever a charged particle traverses the region of the chamber instrumented by the FEPCB in question. By arranging the physical system layout such that each FEPCB receives input from all six layers, one ensures that the basic information required to identify local charged tracks is present. This approach has the added cost-reduction benefit of decreasing the effective readout pitch from 5 mm to 5/6 mm,

which takes better advantage of the packaging density of the custom IC technologies under consideration.

In the GEM muon system operating at the highest luminosities, the average charged particle rate over the $\sim 8 \times 300$ cm^2 swath covered by an FEPCB is expected to be 30 kHz or less. Assuming a 30 ns resolving time, the coincidence rate C between the LCT signal and the worst-case Level 1 accept signal is given by

$$C = R_{\mathrm{L1}} R_{\mathrm{LCT}} \Delta t = 10^5 \ \times \ (3 \times 10^4) \ \times \ (3 \times 10^{-8}) \simeq 100 \text{ Hz} \tag{1}$$

One thus expects an average readout rate of 100 events (or 500 samples) per second per strip. The neutron background rate is expected to be a few ($\sim$ 2–5) times greater than the rate from charged particles. As discussed below, however, the LCT logic is largely insensitive to neutrons, rendering their contribution to the readout rate almost negligible.

From the preceding, it is clear that the readout throughput requirements can be dramatically reduced by employing a data-driven approach. In fact, with such an approach the throughput requirements are no longer determined by the Level 1 trigger rate, but rather are set by the desire to keep the readout latency to less than 100 μs. Thus if one is to digitize five samples for each of the 96 channels on a FEPCB, the average digitization rate must be 5 MSPS. This is well within reach of low-cost commercial 10- or 12-bit ADC's.

Details of the SCA and LCT logic circuitry are presented in the following paragraphs along with preliminary performance data from SCA test chips designed to verify the overall readout architecture.

2 Design Details & Circuit Test Results

2.1 Switched Capacitor Array (SCA)

A functional block diagram of the switched capacitor array is shown in Figure 3. CMOS switches are used to control the writing of input data into the storage capacitors and subsequent readout in a conventional "voltage write, voltage read" operating mode. This mode requires access to both plates of the storage capacitor and exhibits a small gain loss because of charge sharing in the read bus structure. However, the "double-pole" switching of the

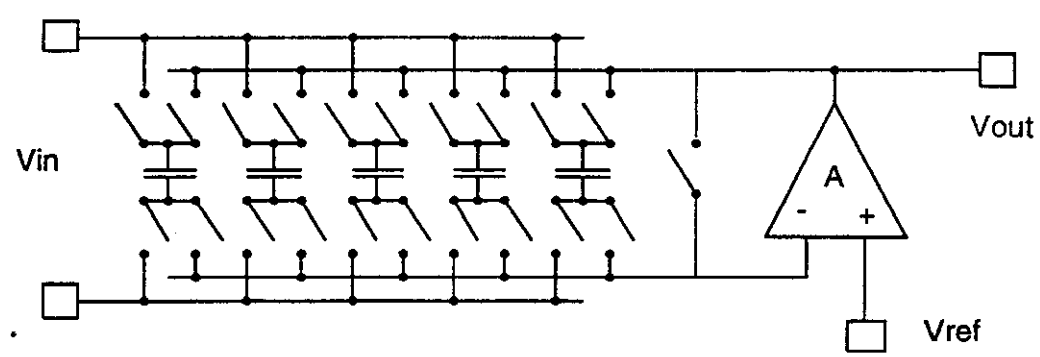

Figure 3: SCA block diagram.

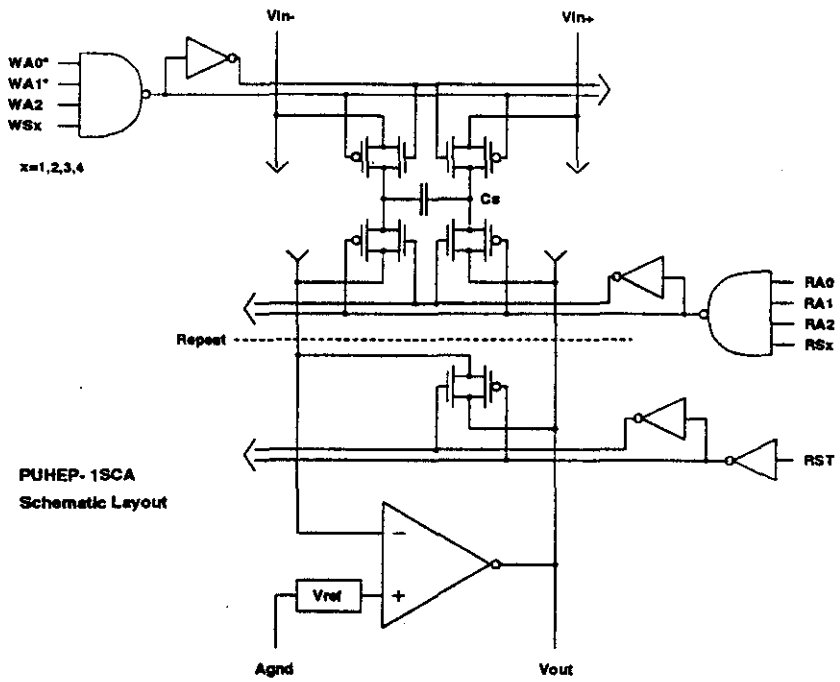

Figure 4: SCA memory cell schematic.

storage capacitors between the input and output circuits provides a significant degree of isolation between the cathode chamber and the readout electronics. A detailed schematic circuit of a typical storage cell and associated readout amplifier are shown in Figure 4.

Static clocking of shielded differential read/write lines and extensive use of guard rings were incorporated to minimize clock feedthrough. The output amplifier is a differential operational transimpedance type with cascode followers and nominal open-loop gain of 10^4. Compensation is provided by capacitive loading of the output. The circuit diagram of the amplifier is shown in Figure 5.

A test circuit consisting of three channels of 28 storage cells each has been fabricated using the Orbit Semiconductor 1.2 μm n-well CMOS process. Linearity measurements were made by applying a signal from a 12-bit DAC to the cells in the array during a 10 MSPS write cycle and reading the array back out at a reduced speed using a 12-bit ADC. A straight-line fit applied to the data from a single cell and the corresponding residuals are shown in Figure 6. The slight bowing is common to all cells and can be corrected through the addition of a second-order term to the fit.

A dynamic range of $\sim$ 11 bits is observed using a single set of three parameters (an offset, a slope, and a correction for the nonlinearity) for all 28 cells in the array, provided that the end cell is removed from the sample. That cell, which has a pedestal value that differs by approximately 8 ADC counts from the others, would normally be used as a dummy guard cell in a full-scale layout. Electrical noise fluctuations are near the measurement limits of the 12-bit hardware used for the tests.

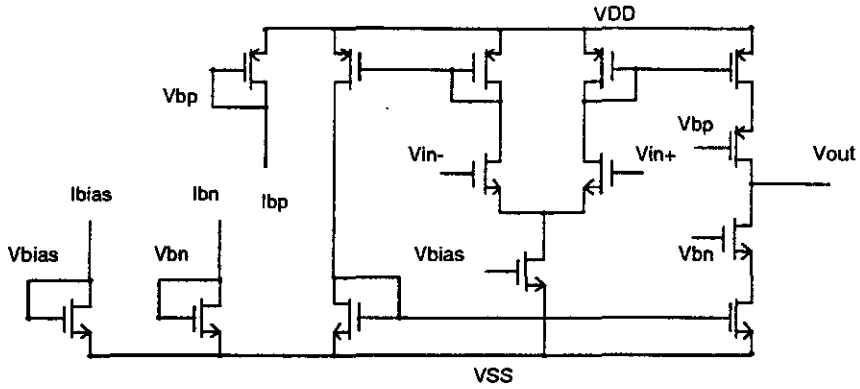

Figure 5: SCA readout amplifier schematic.

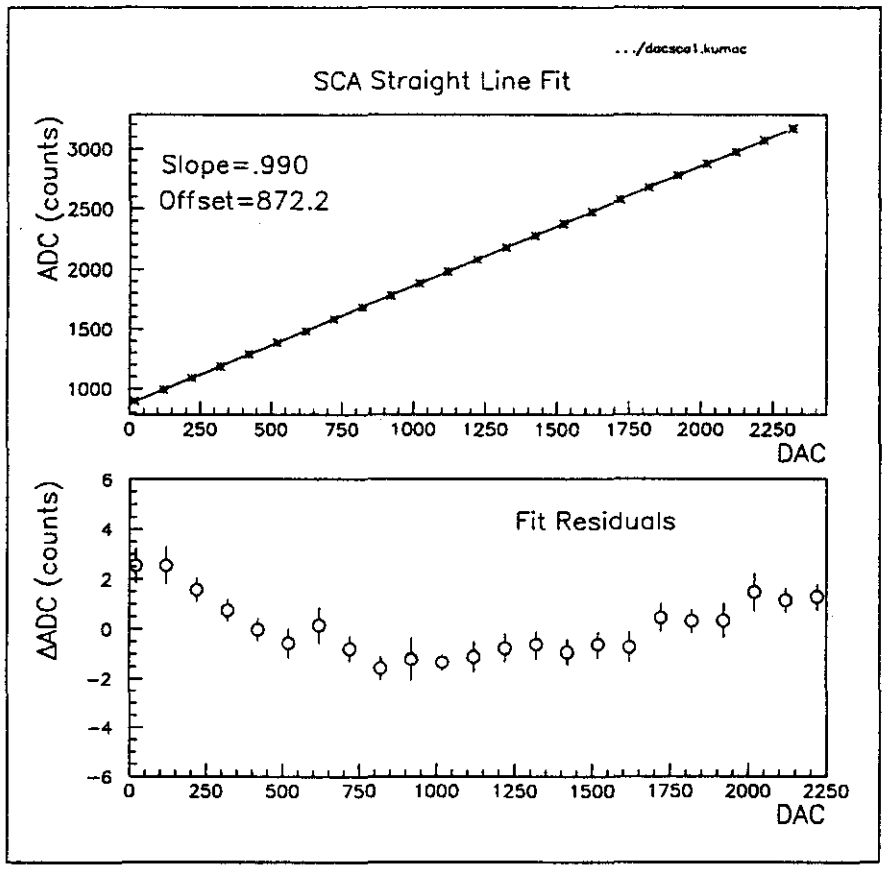

Figure 6: Upper: Straight-line fit for data from an SCA sampling at 10 MSPS. Lower: Fit residuals for the above. The error bars indicate the RMS values for random (event-to-event) fluctuations.

2.2 Local Charge Track (LCT) Logic Electronics

An efficient method for identifying charged particle tracks can be developed by noting that a stiff muon track will deposit a detectable charge on at least four of the six layers of a module. A neutron hit, on the other hand, will typically deposit a larger detectable charge, but usually only on one or two layers of the module. All of the data required to implement such an algorithm is locally available, suggesting that the required logic circuitry be located on the cathode FEPCB's. The added "cost" associated with formation of the LCT signals is in fact quite small since these signals, or their functional equivalent, are already required as input to the Level 1 trigger logic.

The LCT logic can be developed by enumerating the possible combinations of cathode strips that can produce credible tracks with sufficient stiffness. Figure 7 illustrates a possible set of 13 different track combinations. Each track combination consists of a logic element

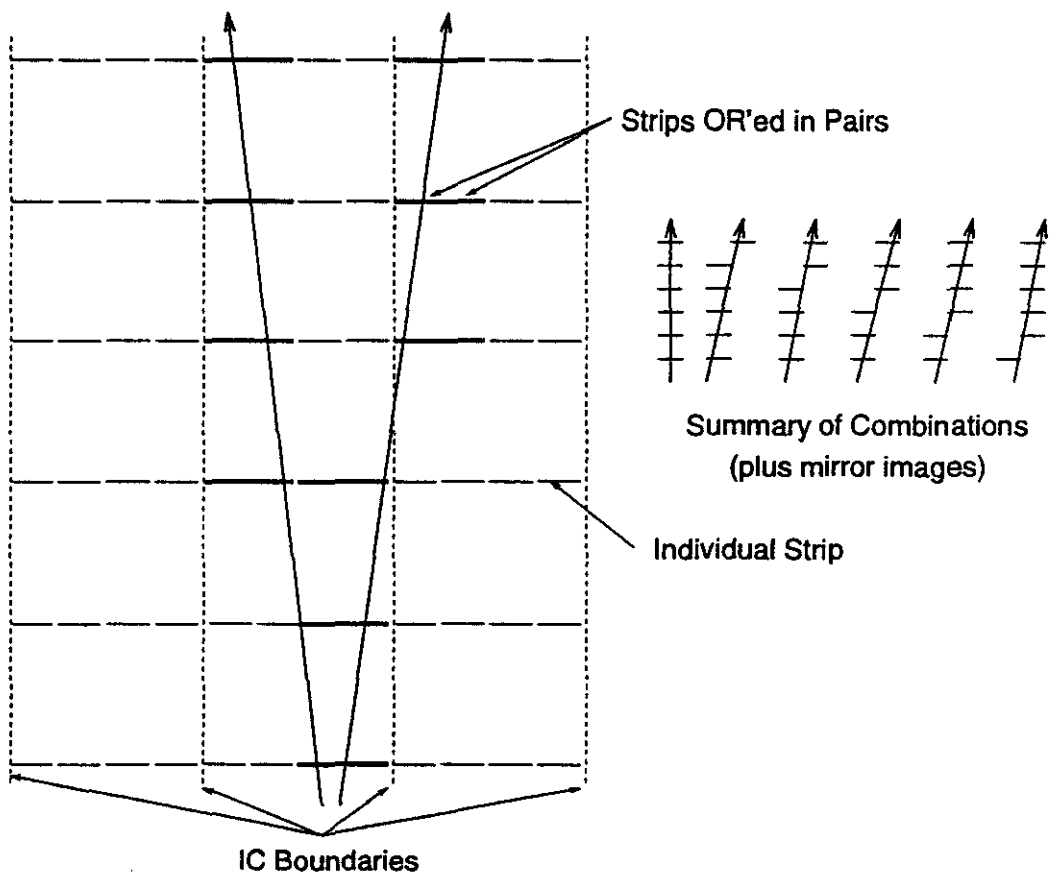

Figure 7: LCT track logic.

that asserts an output if at least four of the six of its inputs are asserted. Implementation of this LCT logic structure involves the formation of 13 individual four-out-of-six terms followed by a logical OR of the 13 results.

An alternate approach[7], which is "non-directional," and therefore more susceptible to false coincidences, but simpler to implement, is also under study.

A key element in the implementation of the LCT circuitry is a fully integrated CMOS timing discriminator to convert the fast shaper outputs to digital logic pulses. The schematic block diagram of the discriminator subcircuit is shown in Figure 8. The circuit provides an output logic pulse with timing that is independent of the input pulse amplitude. The circuit meets this requirement by comparing the fast shaper input signal with its integral, derived using a series *RC* combination. The basic circuit was originally developed in discrete form by Turko and Smith[5]. An important advantage of their approach is that it does not require a delayed version of the signal as is needed by the conventional constant fraction discriminator[6]. This feature is essential and allows us to develop a compact multi-channel integrated version of the circuit.

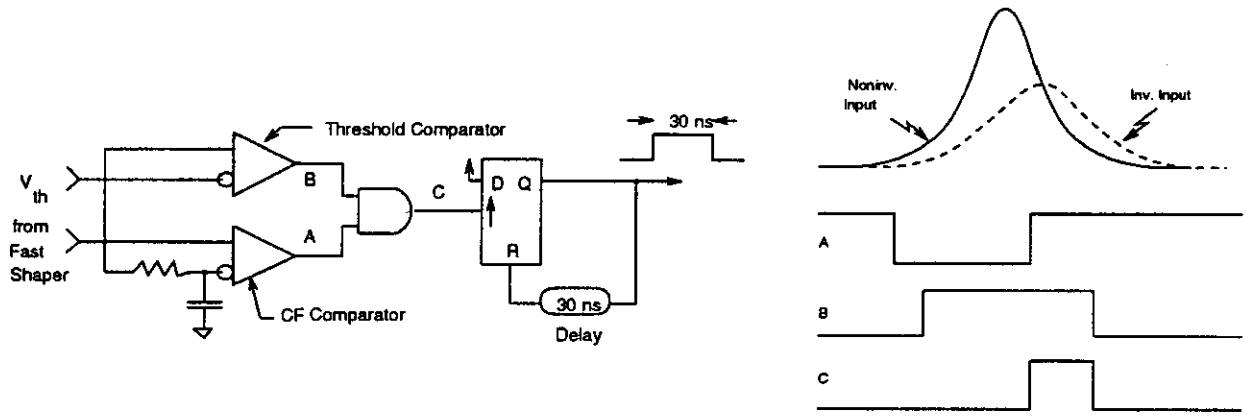

Figure 8: Timing discriminator block diagram.

A conventional comparator circuit, also applied to the fast-shaper output waveform, is used to provide an adjustable threshold function. The output of the timing discriminator is gated by this signal.

The performance of the discriminator is determined by that of the comparator, which is shown in schematic form in Figure 9. Experimental measurements using a prototype comparator test circuit fabricated on the same die as the SCA have verified the expected performance. For pulses between 2 times and 20 threshold, the timing of the output pulse varies by less than ± 1 ns, as shown in Figure 10. In practice, larger timing errors will occur as a result of noise and avalanche-dependent variations in pulse shape.

3 Summary

Data obtained from test subcircuits indicate that practical cathode strip readout circuits can be designed and fabricated in a conventional CMOS process. Adequate dynamic range, input sample rate, and output readout rate can be achieved. Further development of a larger SCA array with a full complement of 48 storage cells per channel is underway. An integrated-circuit timing discriminator has been built and tested. An optimized design of a set of IC's for a complete readout chain is in progress.

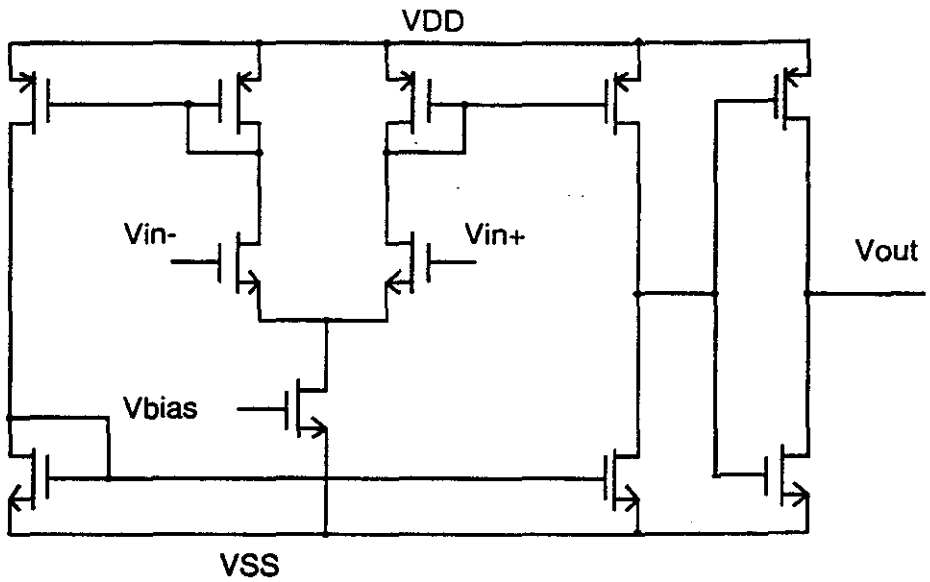

Figure 9: Comparator schematic.

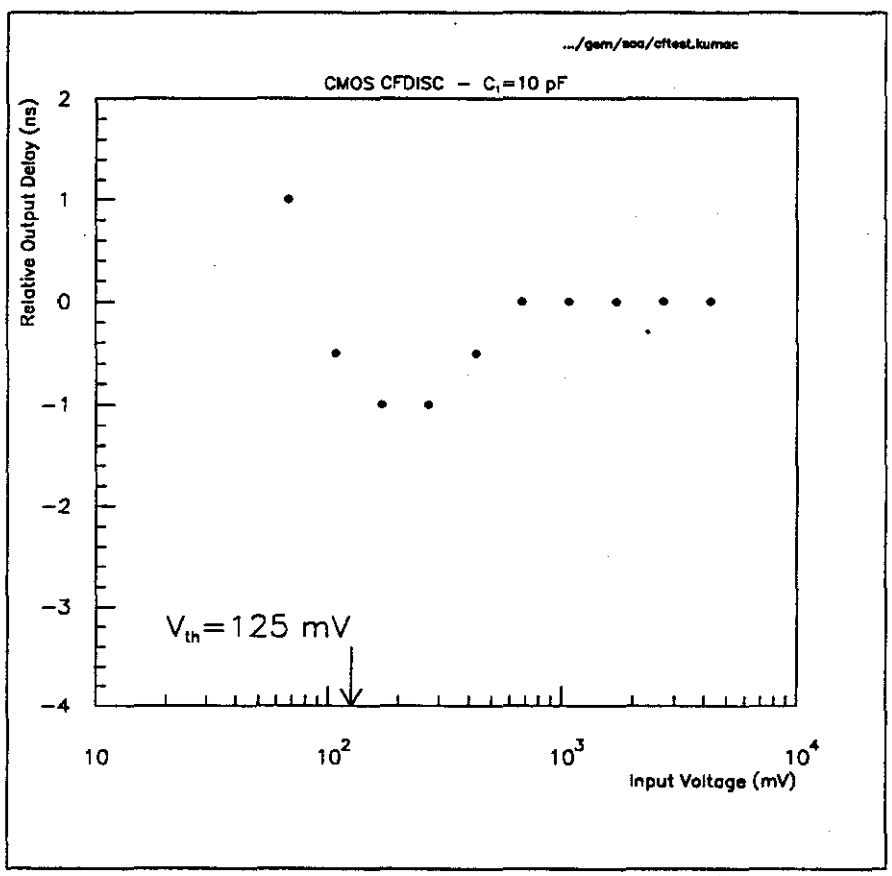

Figure 10: Measured time-walk for integrated timing discriminator.

4 Acknowledgements

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