GEM TN-93-436

10 Bit CAMAC A.D.C. for GEM CSC Readout

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Brookhaven National Laboratory

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Experimental and theoretical studies have been made of the performance of a CAMAC based A.D.C. readout system for the GEM CSC electronics. It employs a 60Mhz 10 bit flash analog to digital converter made by Analog Devices. The electronic test results that follow show the A.D.C. module to have low noise and good differential and integral non linearity characteristics.

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1. INTRODUCTION

Studies of the GEM CSC prototype detector in the Texas Test Rig at SSCL revealed the need for more accurate digitization electronics. The current readout used a CERN developed 8 bit system called DRAMS (Dynamic Readout for Analog Multiplexed Signals). These electronics are CAMAC based, and consists of one control module and one or more A.D.C. modules. The new 10 Bit A.D.C. was designed to replace the existing 8 bit DRAMS A.D.C. and work in conjunction with the existing control module.

2. FUNCTIONAL DESCRIPTION

A functional description of the 10 bit A.D.C. shows the module to contain a fast conversion flash A.D.C. (AD9020kz - 60Mhz) and a bank of 4096, 11 bit memory locations. Analog data is digitized and stored in the onboard memory with the use of an address register and a channel count register. The address register indexes memory for both newly digitized data and for data transfer during readout via CAMAC. Each time the module receives a legal gate input the value at the analog input is digitized and stored in the memory location pointed to by the address register. The address register is automatically incremented whenever digitization takes place, or when an event is read out by the CAMAC bus. The channel count register allows the user to define the number of channels to be digitized. It signals when all channels are finished digitizing via a LAM (look at me), and it signals with a Q=0 response when all of the data has been read out over the CAMAC bus. The channel counter will also cause the module to ignore superfluous gate inputs.

The data read from the module is in the form of 10 bits of digitized information and an 11th bit for overflow flagging. The module is read out by setting the address register to index the onboard memory to the first byte of desired data. A CAMAC read is then executed for each successive byte of data read out. The address register is automatically incremented, and a Q=0 response is generated at A.R. = C.C. so fast DMA and block transfers are also possible.

A.D.C. Input Range	**0, ~+/-.5V**
Pedestal	**~28 counts**
A.D.C. @ Full Scale	**1023 counts**

For 1 A.D.C. channel

$$V = V_{MAX}/Chan_{Total\#}=(.5V)/(1023-28) = .0005V/\ A.D.C.\ Chan.$$

3. COMMAND LIST

The module responds to the following CAMAC function calls.

F(16)A(0)	- Write value to the 12 bit Address Register (A.R.)
F(16)A(1)	- Write value to the 12 bit Channel Counter (C.C.)
F(8)	- Test LAM. Q=1 when LAM=1
F(0)	- Read next value from memory (11Bits), A.R.=A.R.+1, Q=0 when A.R. = C.C.

4. FRONT PANEL AND FEATURES

Figure 1. shows a drawing of the module's front panel. It contains two K-LOC type connectors for gate and analog input as well as some LED's which indicate module activity. The gate input to the module is a positive going TTL edge. This input is terminated with a 50 Ohm resistor, and the gate input must reach at least +1.7V. The analog input is preset to have a dynamic range at the input of 0V to -.5V full scale. Input polarity and gain can be easily changed with internal jumpers, and by switching some resistor values at the input stage.

The module is currently set to receive gate inputs at rates up to 1 Mhz. Higher rates (up to the 60Mhz nyquist frequency) may be achieved by changing the time constants of the monostables at the gate input. The AD9020KZ gate requires a duty cycle of 50%.

The front panel LED's give an indication of the activity in the module. The X led indicates a CAMAC X response to any valid command. The GATE led flashes when a gate is received, and the LAM led illuminates whenever the module is producing a LAM. The X and GATE leds flash for a very short period of time and they may not be seen with the eye unless the gates or valid X responses are produced in a rapid bursts. These bursts are the common mode of reading out multiplexed data.

5. PERFORMANCE EVALUATION

The A.D.C. module was subjected to several in depth tests in order to evaluate it's performance. Some of the measured specifications were differential non linearity, integral non linearity, gate to digitization delay, signal to noise ratio, and long term stability.

Differential non linearity was measured by accumulating a large amount of data over the entire range of the A.D.C. using the finest granularity available from the 16 bit DAC. The A.D.C. module was read 275 times at 36,500 different DAC settings which corresponded to the A.D.C.'s full range input of 0,-.5V. This converts to an average channel receiving about 10,000 hits. Statistically the number of hits that any channel received is propotional to the width of that channel with respect to the other channels in the A.D.C. Figure 2 shows a plot of relative channel width in accumulated hits.

From Figure 2:
Sigma bin width = 1740 Hits = 17.4%

A plot showing the distribution of channel widths is shown for the data presented in figure 2.(Figure 3) Data was histogrammed in bins 100 counts wide. The standard deviation of the differential non linearity of 17% is not uncommon for flash A.D.C.'s due to comparator mismatch within the device.

The integral non linearity was measured with the help of a LeCroy 1976 A.D.C./T.D.C. tester module. It is a CAMAC module which contains a precision 16 bit DAC and a gate generator. The test for integral non linearity was achieved by accumulating data at several points throughout the dynamic range of the device. A straight line was then fit to the data points, and error was measured in residuals (see Figure 4.).

So for n points:

$$y = mx + b$$

Where:

$$m = \frac{\sum xy - \frac{\sum x \sum y}{n}}{\sum x^2 - \frac{(\sum x)^2}{n}} \quad , \qquad B = \frac{\sum y}{n} - m\frac{\sum x}{n}$$

The straight line was fit to all 72 points of data. Error is shown in A.D.C. counts which are each .1% of full scale, or ~.5mV for the input range of 0,.5V. A .05% error is inherent to the line fit due to a high signal to noise ratio at the input and the .1% resolution of 10 bits. Integral non linearity was found to create a residual line fit error of less than .1% of full scale. A distribution of the residuals to a fit with a large number of data points is also presented.(See figure 5.)

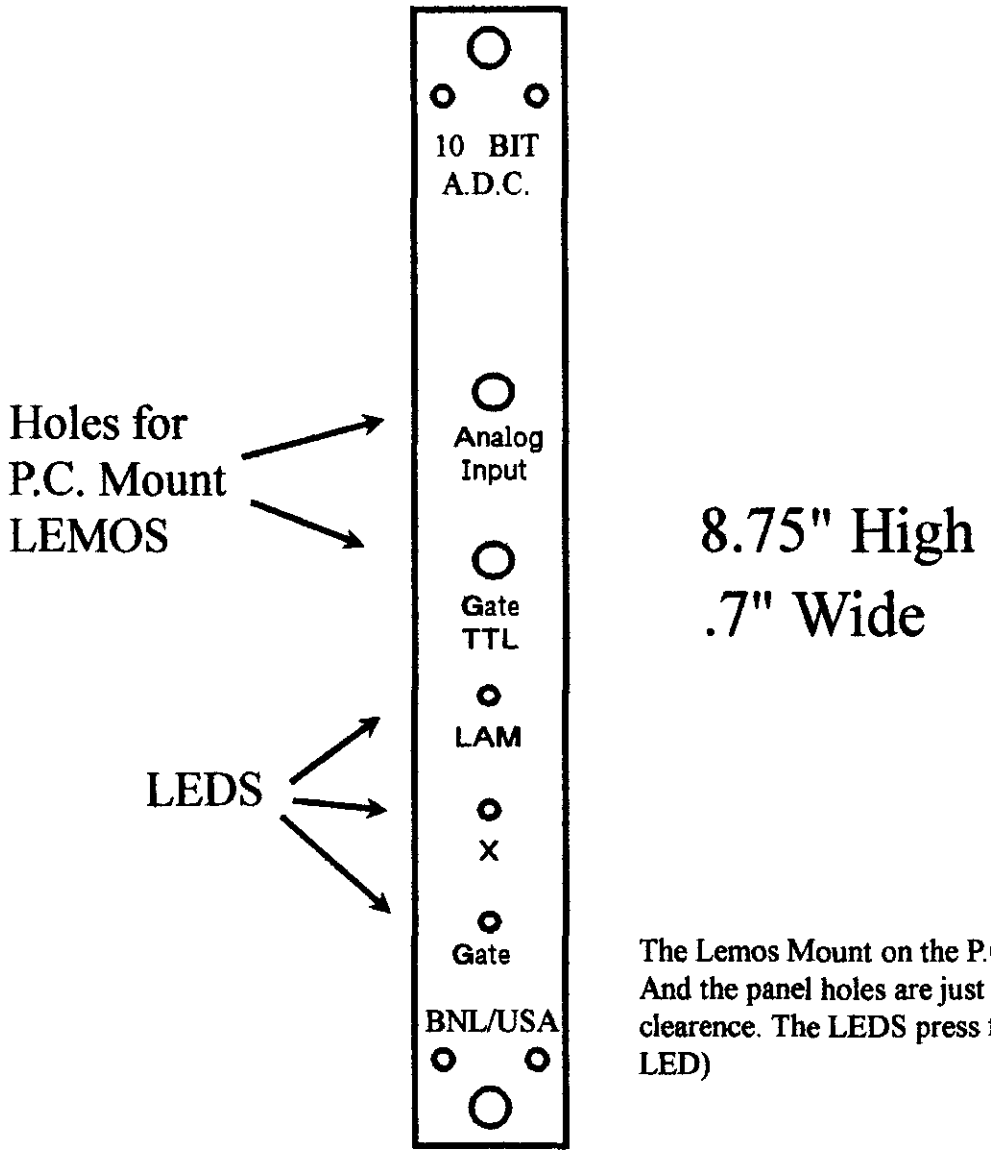
Gate digitization delay was examined with the test setup shown in figure 6. A precision pulser was used to fire a discriminator and two outputs were used to drive gate generators. The NIM (0,-.8V @2nS) output of one gate generator was used as an analog input to the A.D.C. module. The output from the second gate generator was used to drive a NIM - TTL level shifter. This signal was then used for the A.D.C. gate. The timing of the gate generators were adjusted such that the A.D.C. module digitized at -.4V the mid point of the analog inputs slew. Both the gate and analog inputs were then examined on a newly calibrated Tektronics model 485 oscilloscope. Digitization was observed to occur 42nS after the arrival of the gate.

The next characteristic of the A.D.C. module to be examined was the signal to noise ratio on the analog input. This was measured by accumulating a large amount of data for a single DAC setting. Several points throughout the dynamic range of the device were tested. The test result showed a full width at 1/2 maximum to be 1 bin for the entire dynamic range of the device. Figure 7 shows 100,000 events accumulated for a single DAC settings.

Finally, long term stability was examined. This was done by periodically repeating the measurements used to measure the integral non linearity. By examining the plot of residuals to the original straight line fit, any variations in gain, pedestal or integral non linearity became visible. It is important to again point out the .05% or 1/2 l.s.b. error in the straight line fit. A worst case drift of about 4 channels was observed after two days of checking. The mean drift for all A.D.C. channels was measured at .386% or 3.86 A.D.C. channels. Sigma of the residuals changed slightly, going from 0.383 A.D.C. counts to 0.4395 A.D.C. counts. (See Figure 4)

Figure 1.

10 Bit CAMAC A.D.C Front Panel



The Lemos Mount on the P.C. Board
And the panel holes are just connector
clearence. The LEDS press fit into the front panel. (see sample
LED)

Figure 2.

Differential Non Linearity

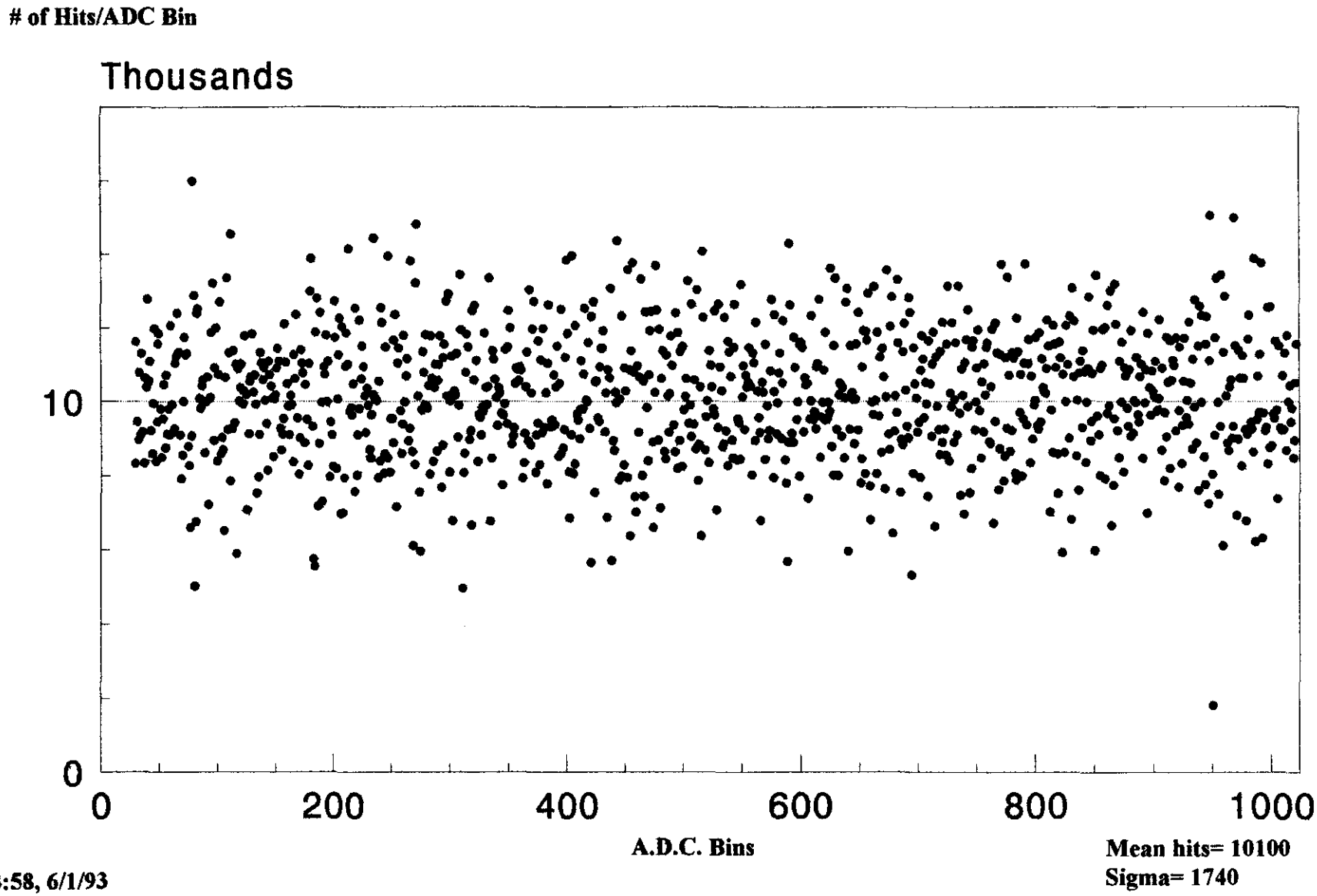
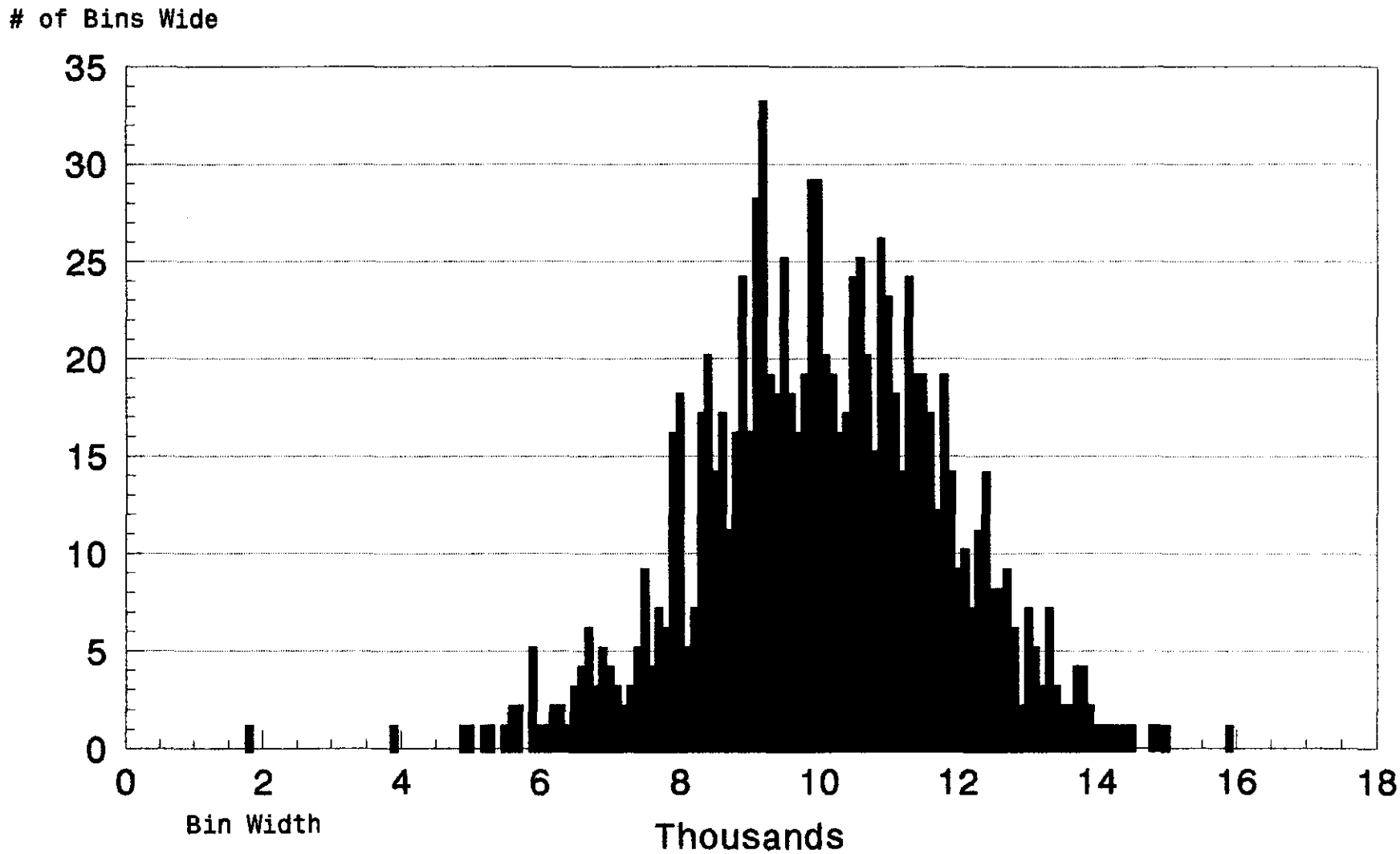


Figure 3.

Distribution Of Bin Widths

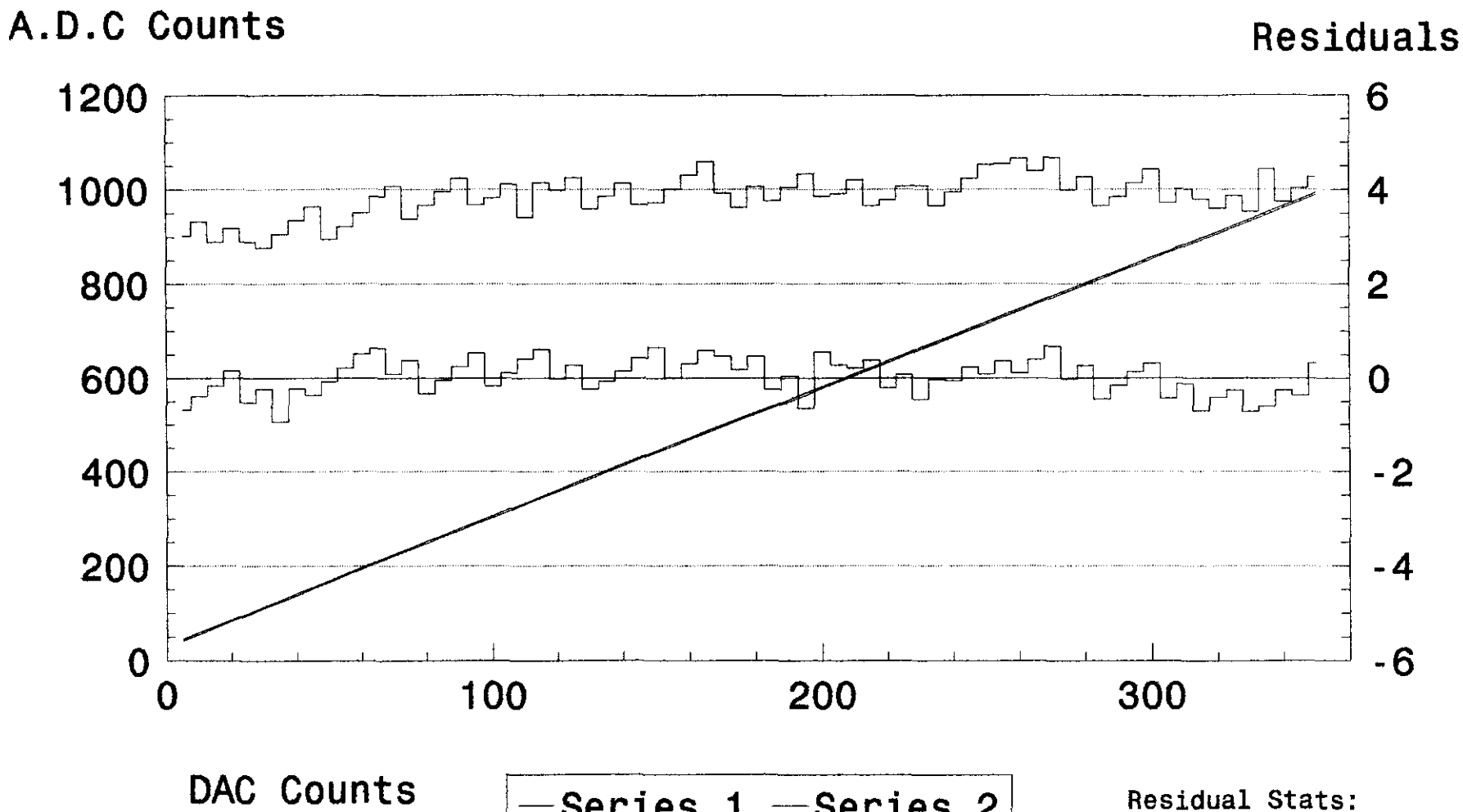


14:58, 6/1/93

Mean bin width:10100
Sigma = 1740

Figure 4.

Integral Non Linearity



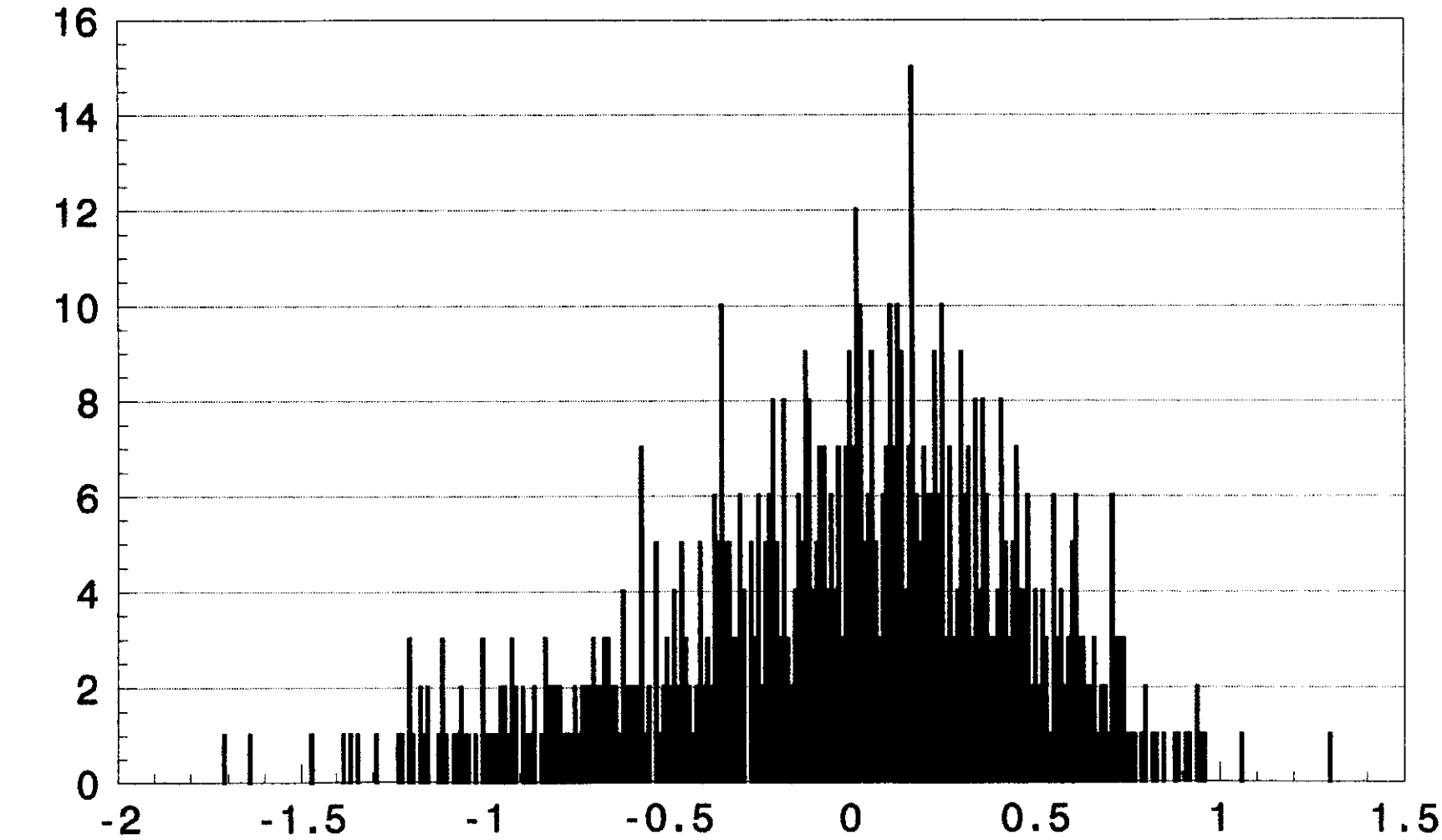
—Series 1 —Series 2
—Series 3 —Series 4

09:42, 6/1/93
Residual fit updated

Residual Stats:
Min: -.978
MAX: 0.678
Mean: 0.00011
Sigma:0.3979
Units in ADC Counts

Figure 5.

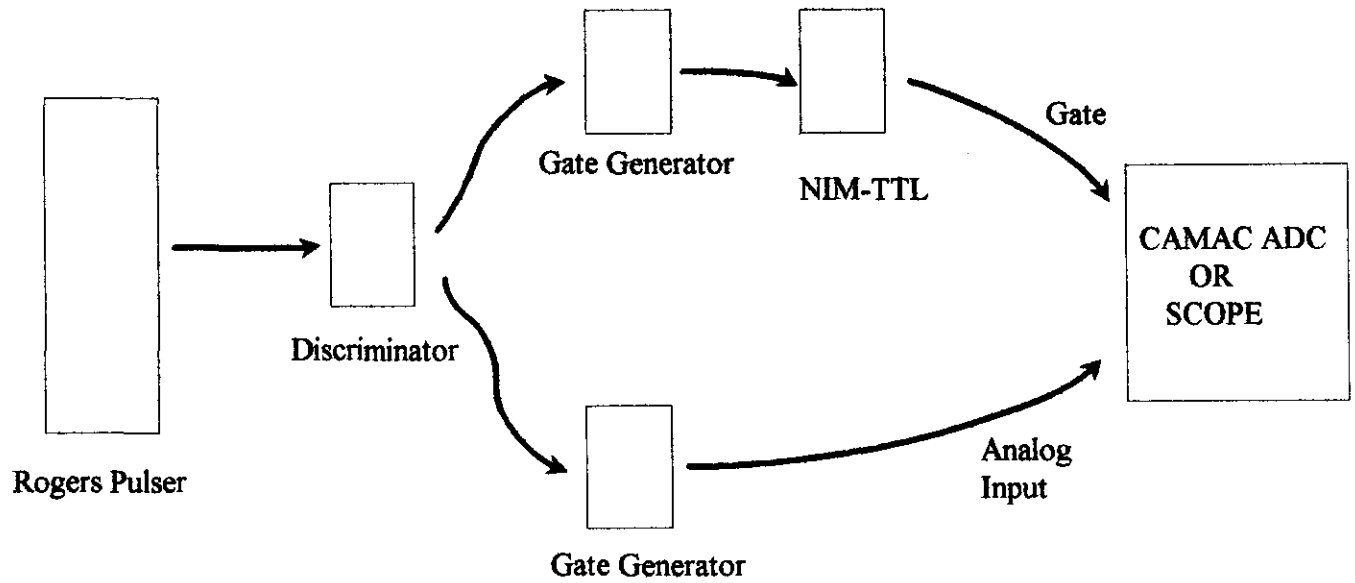
Integral Nonlinearity Residual Distribution



10:06, 6/1/93

Figure 6.

Gate Digitization Delay Measurement



The Rogers pulser generated a fast pulse which triggered a discriminator. Two separate outputs from the discriminator each drove gate generators. Both gate generators were set to 1us gate widths. The output of one was run into a NIM-TTL converter and used as a gate (Rising edge TTL ,5nS). the second (NIM -.8V-0, 2nS) was used as an analog input. The timing of the two gates was then adjusted such that the value read by the ADC corresponded to 1/2 the analog inputs slew, about -.4V. The gate and analog inpus were then removed from the ADC module and placed into two separate scope inputs. The digitization delay was measured as ~42nS.

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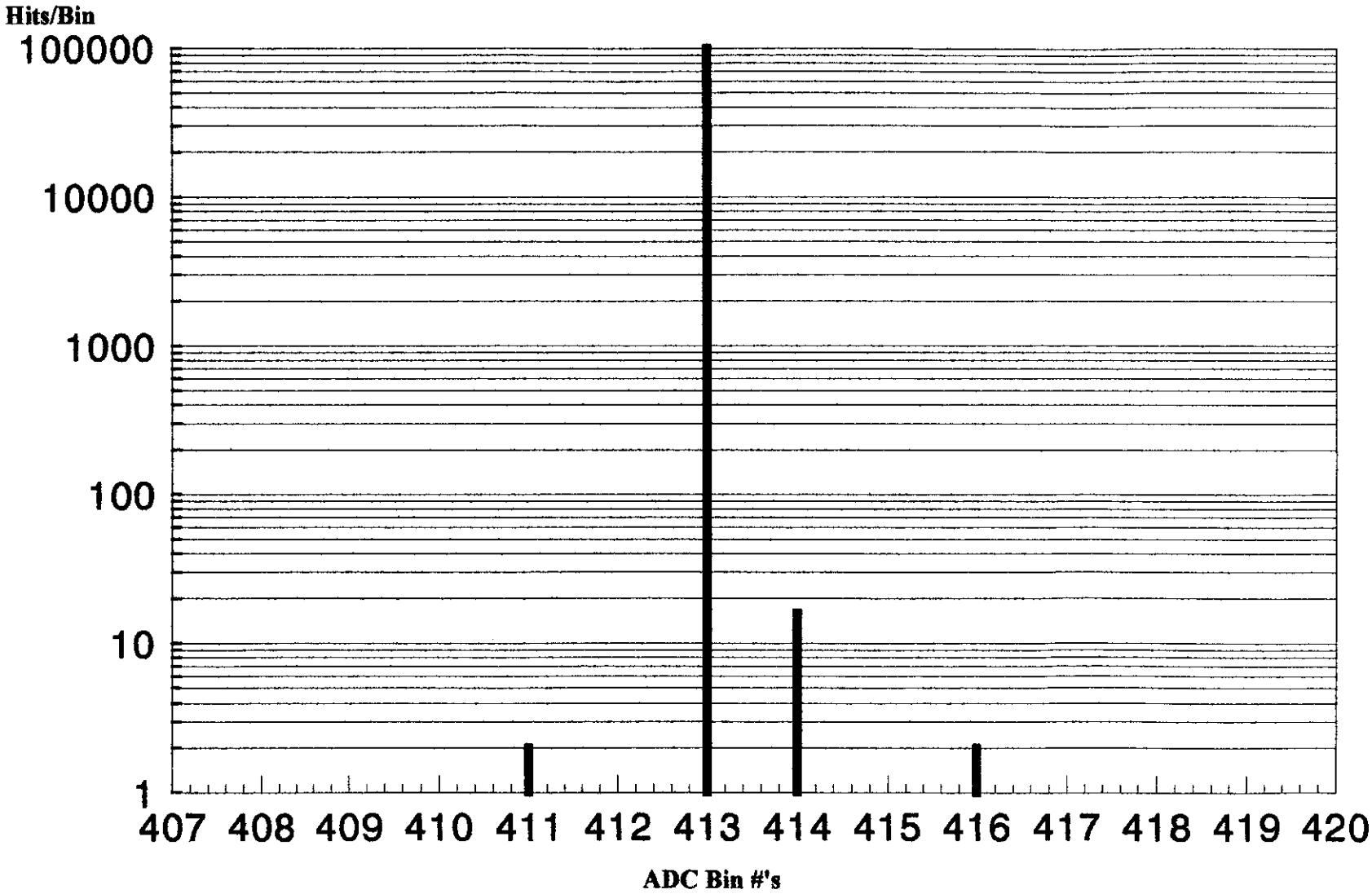
Figure 7

Noise Data