

GEM CSC Front-End IC Design

M. A. Baturitsky, V. A. Chekhovsky, O. V. Dvorknikov, I. A. Golutvin,
I. F. Emel'ianchik, A. V. Litomin, V. A. Mikhajlov, V. V. Shuliak,
N. M. Shumeiko, A. V. Solin, V. A. Yatskevich
Education Ministry of Republic of Belarus'
National Scientific and Education
Center of Particle and High Energy Physics

July 2, 1993

Abstract;

The first iteration stage of custom monolithic front-end electronics for cathode strip chambers supposed to be used in muon detectors of GEM experiment is reported. Two versions of IC were made. The first one uses a low noise microwave bipolar n-p-n transistor at input, the second one uses p-type JFET. Each IC version contains two channels consisted of a charge-sensitive preamplifier followed by a low shaper in signal path and a fast shaper in a trigger path. A noise performance of BJT version $ENC = 1980e + 7e/pF$ has been achieved at peaking time 300 nsec and power dissipation 67 mW per channel. The JFET version has $ENC = 3300e + 20e/pF$ at peaking time 300 nsec and power dissipation 150 mW. To achieve better ENC the JFET version should be modified by increasing gain and improving capacitance matching.

EDUCATION MINISTRY OF REPUBLIC OF BELARUS'
NATIONAL SCIENTIFIC AND EDUCATIONAL
CENTER OF PARTICLE AND HIGH ENERGY PHYSICS
ATTACHED TO BYELORUSSIAN STATE UNIVERSITY

GEM CSC FRONT-END IC DESIGN

Technical Report

REPUBLIC OF BELARUS'

Minsk-1993

LIST OF AUTHORS

1. Baturitsky M.A.
2. Chekhovsky V.A.
3. Dvornikov O.V.
4. Golutvin I. A.
5. Emel'ianchik I.F.
6. Litomin A.V.
7. Mikhajlov V.A.
8. Shuliak V.V.
9. Shumeiko N.M.
10. Solin A.V.
11. Yatskevich V.A.

ABSTRACT

The first iteration stage of custom monolithic front-end electronics for cathode strip chambers supposed to be used in muon detectors of GEM experiment is reported. Two version of IC were made. The first one uses a low noise microwave bipolar n-p-n transistor at input, the second one uses p-type JFET. Each IC version contains two channels consisted of a charge-sensitive preamplifier followed by a low shaper in signal path and a fast shaper in a trigger path. A noise performance of BJT version $ENC = 1980e + 7e/pF$ has been achieved at peaking time 300 nsec and power dissipation 67 mW per channel. The JFET version has $ENC = 3300e + 20e/pF$ at peaking time 300 nsec and power dissipation 150 mW. To achieve better ENC the JFET version should be modified by increasing gain and improving capacitance matching.

LIST OF DESIGNATIONS

BJT	- bipolar (junction) transistor
CSC	- cathode strip chamber
CSP	- charge-sensitive preamplifier
FS	- fast shaper
SS	- slow shaper
ENC1	- series r. m. s. equivalent noise charge component to be dependent on BJT transconductance
ENC2	- series r. m. s. equivalent noise charge component to be dependent on BJT base spread resistance
ENC3	- parallel r. m. s. equivalent noise charge component to be dependent on input current
ENC4	- series r. m. s. equivalent noise charge component to be dependent on JFET transconductance
ENC5	- parallel r. m. s. equivalent noise charge component to be dependent on detector leakage current
ENC6	- MOSFET flicker noise component
ENC7	- MOSFET bulk-resistance and component
ENC8	- MOSFET channel noise component
q	- electron's charge
Cd	- detector's capacitance
Cf	- feedback capacitance
Ci	- input capacitance of the head transistor
k	- Boltzmann's constant
T	- temperature
Rbb'	- base spread resistance of BJT transistor
Gm	- transconductance
K	- charge-to-voltage transform efficiency
Ku	- open loop voltage gain
Tp	- peaking time
Vcb	- breakdown voltage of a collector-base junction of BJT
Vbe	- breakdown voltage of BJT base-emitter junction
Vce	- breakdown collector-emitter voltage
Ua	- Early's voltage
Uth	- threshold voltage of JFETs and MOSFETs
Uds	- drain-source voltage
Ugs	- gate-source voltage
Udng	- down gate voltage
Udngs	- down gate-source voltage
Id	- drain current

CONTENT

INTRODUCTION.....7

1. GEM CSC FRONT-END IC DESIGN BASIS.....8

- 1.1. The preamplifier/shaper IC specification8
- 1.2. Comparison of available semiconductor technologies.....9
- 1.3. Main formulae for noise estimations9
- 1.4. The head transistor parameters optimization.....10
 - 1.4.1. JFET optimization.....10
 - 1.4.2. Bipolar transistor optimization.....11
- 1.5. CSP head element choice.....12
 - 1.5.1. The structure and characteristics of JFET.....12
 - 1.5.2. The structure and characteristics of bipolar transistor.....13
 - 1.5.3. Main conclusions about the head element choice.....14
- 1.6. Choice and calculation of readout path (CSP + slow shaper)..15
 - 1.6.1. Preliminary notes.....15
 - 1.6.2. Calculation of CSP and slow shaper.....15
 - 1.6.3. The timing channel calculation.....16
- 1.7. The CSP head-element estimation for the peaking time 1.0 and 0.3 usec and noise levels 3000 and 1000 r.m.s. e-.....19
- 1.8. THE CSP CMOS IC production possibility estimation for the case ENC=1000 r.m.s. e- and Tp=300 nsec.....21
 - 1.8.1. General notes.....21
 - 1.8.2. The comparison of existant CMOS CSPs.....21
 - 1.8.3. The CSP parameters to be achieved with CMOS technology available in Minsk.....23
 - 1.8.4. Short conclusions.....23
- 1.9. Description of the IC design.....24
 - 1.9.1. BJT/JFET IC channel 1/2 parameters.....24
 - 1.9.2. Head stage technology features.....24
 - 1.9.3. IC layouts.....24
 - 1.9.4. Electric circuits of BJT version.....25
 - 1.9.5. Electric circuits of JFET version.....29
 - 1.9.6. Pspise BJT version simulations.....29
 - 1.9.7. Discrete elements BJT version breadboard modelling....35
 - 1.9.8. Pspise JFET version simulations.....35
 - 1.9.9. Discrete elements JFET version breadboard modelling....36

2. PREAMPLIFIER/SHAPERS IC ELECTRONIC COMPONENT MEASUREMENTS.....50

- 2.1. Purposes and content of the investigation.....50
- 2.2. On-wafer measurements.....50
 - 2.2.1. Wafers with TA1 structures.....50
 - 2.2.2. TA2 wafer measurements.....51
- 2.3. Packaged test structures.....51
 - 2.3.1. TA1 structures.....51
 - 2.3.2. TA2 structures.....53
 - 2.3.3. Test capacitance measurements (TA1 structures).....53

2.4. n-p-n transistor measurements.....	53
2.4.1. Static parameters of TA1 n-p-n test structures.....	53
2.4.2. Static parameters of TA2 test n-p-n transistors.....	55
2.4.3. Ft measurements of TA1 structures.....	56
2.4.4. Ft measurements of TA2 n-p-n transistors.....	57
2.4.5. n-p-n transistors noise measurements.....	57
2.5. JFET tests.....	59
2.5.1. TA1 JFETs.....	59
2.5.2. TA2 test JFET static characteristics measurements.....	60
2.5.3. TA2 test JFET noise measurements.....	62
2.5.4. TA1/TA2 pJFET constructions comparison.....	64
2.6. Discussion of the TA1/TA2 measurements results.....	64
2.7. About an opportunity of using of CMOS technology, available in Minsk, for CSP/shaper tasks	65
2.7.1. Test MOSFET structures.....	65
2.7.2. MOSFET static parameter measurements.....	66
2.7.3. MOSFET noise measurements.....	70
2.7.4. Conclusions.....	72
3.0. IC PARAMETERS MEASUREMENTS RESULTS.....	74
3.1. The measurements methodic.....	74
3.2. The BJT version IC measurements results.....	77
3.3. The JFET version IC measurements results.....	79
3.4. The measurement results discussion.....	89
CONCLUSION.....	91
REFERENCIES.....	92
A1. APPENDIX. Pspise simulation protocol.....	93

INTRODUCTION

This report presents first iteration results of GEM Muon Detector Cathode Strip Chamber Front-End Custom IC design being made in Minsk, Republic of Belarus'. The Part 1. of this report is devoted to ground of the choose of electric circuits and semiconductor technology of the ICs. Noise levels, speeds and power consumptions were analysed in dependence on the circuit and technology parameters.

Two versions are chosen: the first one with an bipolar junction transistor (BJT) used as a head element of a charge-sensitive preamplifier (CSP) and the second version with JFET at this place. The amplifier structure circuitry is chosen to be an folded cascode, the semiconductor technology to implement the IC is selected to be combined BJT-JFET. The results of Pspice simulations and breadboard modelling are presented at the end of the part.

The second part presents the electronic component measurements results for designed IC to characterize the potential abilities of the electronic circuits and technology used. The monolithic capacitors, resistors, microwave n-p-n BJTs, p-type JFET characteristics were tested, both static and dynamic. To investigate the possibilities of CMOS technology available in Minsk the test CMOS MOSFET structures were produced. Their test results are presented here too.

The designed IC characteristics of the two versions (BJT and JFET CSP head transistor version) were investigated. The dependencies of ENC versus the head transistor structure, current, peaking time T_p and detector capacitance C_d were measured. The block-circuit of a test bench to measure the IC noise characteristics both the measurements results are presented here.

In the CONCLUSION part the inferences on the circuit structures and characteristics are formulated.

Appendices contain the Pspice simulation protocol.

1. GEM CSC FRONT-END IC DESIGN BASIS

1.1. The preamplifier/shaper IC specification

A structure and specification for CSC front-end preamplifier/shaper IC to be designed in Minsk were accepted after discussion on two meetings in Dubna-Minsk, April 27 - 30, 1992 and in Dubna, June 16 - 17, 1992.

One channel of IC was supposed to consist of a charge-sensitive preamplifier (CSP) followed by two shapers: slow one (SS) for signal path and fast (FS) one for trigger path. The circuit is shown on Fig.1.0, and its parameters are listed in Table 1.1.

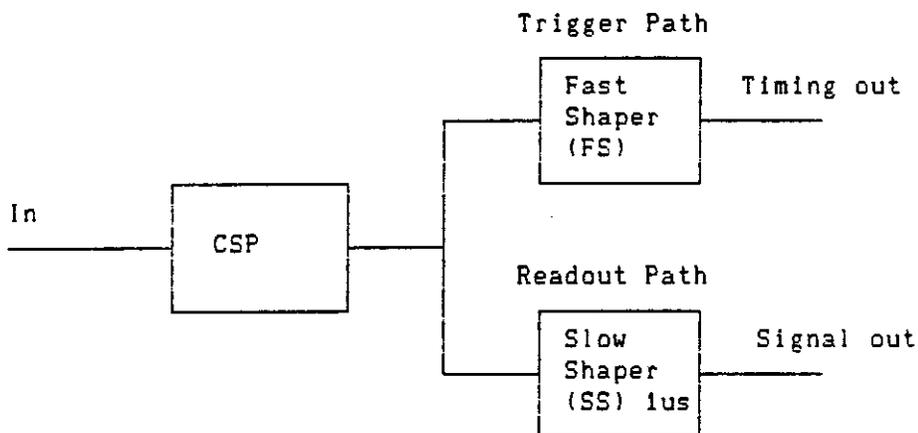


Fig.1.1. A Block-Circuit of Front-End IC Channel

Table 1.1
Electrical specifications for GEM CSC Front-End Custom IC

Parameter	Required	Desirable	Comments
Readout Path:			
Input Noise, r.m.s. e-	3000	1500	Cd=100pF, Tp=1.0us
Shaping time Tp, us	1.0+/-0.2	1.0+/-0.2	
Crosstalk, dB	<-50	<-60	
Conversion Gain, mV/fC	5.0	10.0	
Integral nonlinearity, %	<0.5	<0.5	after correction
Maximum input charge, fC	200	400	
Timing channel:			
Input threshold, fC	16	8	must drive MVL407
Time jitter, r.m.s ns	<4	<2	for Qin=40fC
Time walk, ns	<4	<2	2X - 10X threshold
Common			
Power Dissipation, mW	<100	20	
Package	SO 8ch/pkg		
Input protection	yes		against large positive inputs

1.2. Comparison of available semiconductor technologies

The possibility of the IC implementation in different semiconductor technology to be in our disposal (microwave bipolar junction transistors (BJT), CMOS and combined microwave BJT-JFET). Different charge-sensitive amplifier basic circuit structures were analysed to be used for cathode strip chamber muon detectors: voltage amplifiers /1/, current amplifiers /2/, amplifiers based on difference stage /3, 4/ and folded-cascode structures /5 - 13/. To choose the type of IC production technology the noise, speed and power characteristics were theoretically analysed above all.

The opinion most wide spread in low noise IC literature is that in accordance with signal source characteristics such as internal resistance, capacitance and signal length JFET's and bipolar transistors with optimized collector current are to be used preferably as an input device.

MOSFET's are traditionally considered:

- to use special build-in static-electricity protection devices which increase input currents (and naturally noises caused by them) from level of $10E-15$ A to $10E-12$ A, which is comparable with JFET gate leakage current;

- to possess extremely large flicker-noise about 50 - 200 $nV/Hz^{1/2}$ for 10 Hz (for comparison JFET has 5 - 20 $nV/Hz^{1/2}$);

- to have practically unremovable drawback - time drift of threshold current during electric load work at high temperature - which is explained by charge migration in gate oxide, changing MOSFET and overall circuit regime.

However, low-noise low-power dissipation CMOS IC were reported recently /10, 13, 14/. Their satisfactory noise characteristics are believed to be explained by very good agreement with specific conditions of their environment. Such IC's have the set of advantages:

- low power dissipation;

- possibility of high resistivity resistors production (1 M Ω - 1 G Ω) by using common gate MOSFET's which allows all the optimal filter elements to be formed inside the chip without external discrete hang-up elements.

Nevertheless, the most high speed shapers with peaking time about 5 - 50 nsec can be realised only in bipolar /15, 21/ or bipolar-JFET (Bi-JFET) /6/ technology using bipolar microwave transistor as a head element. The last seems to be more preferable because proposed GEM muon detector front-end electronics architecture includes fast shapers. The fast shaper's specified parameters are estimated (see undermentioned calculations) to be achieved only for the RC-CR shaper with peaking time less than 10 nsec, but this is impossible when using known CMOS technologies of IC production /10, 13/.

1.3. Main formulae for noise estimations

The next formulae were used for calculations of charge-sensitive preamplifier noise levels in the case of detectors with large output capacitance:

$$ENC1 = (e/2q)(Cd + Cf + Ci)(kT/TpGm)^{1/2} \quad (1.1)$$

$$ENC2 = (e/2q)(Cd + Cf)(2kT*Rbb'/Tp)^{1/2} \quad (1.2)$$

$$ENC3 = (e/2q)(Tp*ql)^{1/2} \quad (1.3)$$

$$ENC4 = (e/q)(Cd + Cf + Ci)(kT/3Tp*Gm)^{1/2} \quad (1.4)$$

$$ENC5 = (e/q)(kT*Tp/2Rp) \quad (1.5)$$

where

ENC1,2,3,4,5 - mean squared equivalent noise charge

q - electron's charge

Cd - detector's capacitance

Cf - feedback capacitance

Ci - input capacitance of the head transistor

k - Boltzmann's constant

T - temperature

I - detector leakage or CSP input current

Rbb' - base spread resistance of Bi transistor

Rp - resistance of parallel connection of feedback resistor Rf and detector bias resistor Rb

Gm - transconductance

ENC1,4,2,3,5 depend on the transconductance of BJT and JFET transistors, Rbb', input current of amplifier and leakage current of the detector and parallel resistance accordingly.

The summary noise of CSP using JFET as a head element is described by the next equation:

$$ENCj = (ENC4^2 + ENC3,1^2 + ENC3,2^2 + ENC5^2)^{1/2} \quad (1.6)$$

Note that ENC3,1 are calculated for input current of CSP, and ENC3,2 for detector leakage current.

The summary noise of CSP with BJT transistor head element is

$$ENCbi = (ENC1^2 + ENC2^2 + ENC3,1^2 + ENC3,2^2 + ENC5^2)^{1/2} \quad (1.7)$$

ENC3,1 is the same as in (6).

1.4. The head transistor parameters optimization

1.4.1. JFET optimization

The dimension of JFET, i.e. the ratio of the channel width Z to its length L, determines the maximal values of its transconductance Gmax and capacitances of source-gate Cgs and drain-gate Cgd. Increasing Z/L leads to increasing Gmax, Cgs and Cgd, therefore ENC4 must have minimum.

Taking into account the next relations:

$$Gmax = A1(Z/L), \quad (1.8)$$

$$Cgd = A2*Z*L, \quad (1.9)$$

where A1, A2 - constants,

and keeping in mind that in specific technological process the channel length L tends to be maintained minimal and practically only the channel width Z can be altered, it is possible to show that

$$G_{\text{max}} = A_3 * C_{\text{gd}}, \quad (1.10)$$

and function $ENC_4(C_{\text{gd}})$ reaches its minimum at

$$C_{\text{gd}} = C_{\text{d}} + C_{\text{f}}. \quad (1.11)$$

Miller's effect is often stated in literature to be taken into account in the optimization process. In this case the optimization condition for JFET dimensions will be

$$C_{\text{d}}(1 + K_{\text{u}}) = C_{\text{d}} + C_{\text{f}} \quad (1.12)$$

For the most frequently used type of the first stage - cascode JFET-BJT we have

$$K_{\text{u}} = (G_{\text{max}} * \phi_{\text{t}} / I_{\text{d}}) \{1 - [1 - (I_{\text{d}} / I_{\text{dmax}})^{1/2}]^{1/2}\}, \quad (1.13)$$

where $\phi_{\text{t}} = kT/q$ is the temperature potential.

For chosen JFET (see lower, variant 1) $G_{\text{max}} = 8.6 \text{ mA/V}$, $I_{\text{d}} = 7.33 \text{ mA}$, $I_{\text{dmax}} = 14.4 \text{ mA}$ we have $K_{\text{u}} = 0.014$.

For variant 3 $G_{\text{max}} = 39.2 \text{ mA/V}$, $I_{\text{d}} = 2.94 \text{ mA}$, $I_{\text{dmax}} = 78.3 \text{ mA}$ we attain $K_{\text{u}} = 0.035$.

1.4.2. Bipolar transistor optimization

Optimization of BJT is more difficult, because in this case it is possible to optimize both the geometrical size and the collector current, taking into consideration the influence of contradictory factors, namely:

- minimization of ENC_2 due to minimization of $R_{\text{bb}'}$ results in increasing of transistor dimensions and collector-base capacitance C_{bc} , but this leads to increasing of ENC_1 , being particularly large in the case of strong Miller's effect (large gain of first stage);

- dependence of bipolar transistor input capacitance C_{i} on emitter current

$$C_{\text{i}} = C_{\text{bc}}(1 + K_{\text{u}}) + I_{\text{e}} / (\omega_{\text{t}} * \omega_{\text{t}}), \quad (1.14)$$

where K_{u} is gain of the first stage,

$\omega_{\text{t}} = 2 f_{\text{t}}$ - transition frequency,

leads to existence of minimum value of series noise ENC_1 in dependence of the collector current;

- increasing of collector current made in the process of optimization of series current causes the increasing of the parallel noise ENC_3 .

Minimum ENC is estimated in our analysis to achieve at emitter current equal to

$$I_{\text{opt1}} = \phi_{\text{t}} * 2 \pi f_{\text{t}} [C_{\text{d}} + C_{\text{f}} + C_{\text{bc}}(1 + K_{\text{u}})] \quad (1.15)$$

At the same time minimum of the sum $ENC_1^2 + ENC_3^2$ occurs at

$$I_{opt2} = (C_T / T_p) (\alpha B^{-1/2}), \quad (1.16)$$

where C_T - the total capacity
 B - the current gain of the head bipolar transistor.

$$C_T = C_d + C_f + C_{bc}(1 + K_u) + I_e / (\alpha \omega_T) \quad (1.17)$$

Substitution eq. (17) to eq. (16) gives

$$I_{opt2} = [I_e / (T_p \omega_T^{1/2} (1 - 1/\omega_T))] [C_d + C_f + C_{bc}(1 + K_u)]. \quad (1.18)$$

It should be noted that equation (1.13) is valid for usual cascode rather than folded one. Usual cascode made with Bi transistors has unit gain (at the point of input transistor collector). Folded cascode has larger gain and hence it reveals stronger Miller's effect.

Folded cascode gain K_u should be estimated separately for every specific circuitry taking into account the type of active devices being used as well as desirable combination of speed and power consumption.

1.5. CSP head element choice

1.5.1. The structure and characteristics of JFET

Standard low noise p-type JFET of basic technology has the next characteristics:

- maximum transconductance G_{max} 180 $\mu A/V$
- maximum saturation drain current I_{dmax} 300 μA
- threshold voltage U_p 2.0 - 3.0 V
- dimensions ratio Z/L 60 $\mu m / 2.42 \mu m$
- capacitance to substrate C_{sub} 2 pF
- capacitance gate-drain C_{gd} 2.1 pF

Furthermore now we are finishing design of modified JFET with improved ratio G_{max}/C_{sum} . The modification is going in two directions:

- separation of top and bottom gates and execution of JFET control only with top gate as in /16/;
- development of advanced technological process to increase the transconductance without increasing of transistors' size /17/.

Unfortunately, this modification is accomplishing with low-power JFETs. The ratio Z/L being increased, only G_{max} , I_{dmax} and capacity of top gate, which equals $0.2C_{gd}$, would change in linear proportion. The dependences of C_{sub} and $0.8C_{gd}$ (the capacitance of the bottom gate) on Z/L may have been estimated only experimentally, and we have received this dependencies at the measurements of test transistor structures, described in Part 2. Therefore the proportional growth of known characteristics of JFET with increasing of Z/L is stated to be incorrect for the case of C_{sub} and C_{gd} .

For the worst case of scaling JFET, matched with the detector capacitance, would have the next characteristics:

Characteristics	Variant 1	Variant 2	Variant 3
Capacitance C_{gd} , pF	100	100	100
Dimension ratio Z/L	2680/2.42=1185	11470/2.42=4700	2900/2.42=1198
Threshold voltage, V	2.0 - 3.0	2.0 - 3.0	2.0 - 3.0
Max. drain current I_{dmax}	14.4 mA	57.6 mA	78.3 mA
Max. transconductance G_{max}	8.604 mA/V	19.27 mA/V	39.2 mA/V

Table 1.2 summarizes JFET white noise calculation results (flicker noise is not taken into account) and minimum power dissipated only by the head JFET:

$$P_{min} = I_d \times V_p (I_d / I_{dmax})^{1/2} \quad (1.19)$$

Estimates to be shown are made for operational current I_d which is equal that of ref. /10/, i.e. $I_d = 200 \mu A$, and provides the desired level of noise.

Table 1.2

Characteristics	Variant 1		Variant 2		Variant 3	
I_{dmax} , mA	14.4		57.6		78.3	
G_{mmax} , mA/V	8.604		19.27		39.2	
$C_T = C_d + C_f + C_{in}$, pF	200,5		200,5		200,5	
I_d (operational value), mA	0.2	7.33	0.2	7.07	0.2	2.94
G_m (operational value), mA/V	0.523	4.0	0.576	4.0	1.003	4.0
ENC4, r.m.s. e- (*)	5500	2000	5300	2000	4000	2000
P_{min} , mW	0.071	15.7	0.035	7.43	0.0303	1.71

* Rounded to hundreds of electrons.

1.5.2. The structure and characteristics of bipolar transistor

Combined BJT-JFET technology provides the next low-power n-p-n transistor parameters:

$B = 70$, $I_e = 3.0 \text{ mA}$, $f_T \geq 2.5 \text{ GHz}$, breakdown collector-emitter voltage $U_{ce} > 8.5 \text{ V}$ ($I_b = 0$), $C_{cb} < 1.2 \text{ pF}$ ($U_{cb} = 0V$).

If Bi transistor were used in CSP input stage connected to detector with internal capacitance $C_d = 100 \text{ pF}$, the dimension optimization would be reduced to $R_{bb'}$ minimization only, and capacitance matching would be made by collector current changing. These estimates have been made for three variants of the head Bi transistor.

Characteristics	Variant 1	Variant 2	Variant 3
Overall emitter zone area, μm	300 x 2.5	150 x 2.5	90 x 2.5
Spread base resistivity $R_{bb'}$, Ohm	6	12	20
Collector-base capacitance C_{cb} , pF	2.4	1.9	1.7
Transition frequency f_T , GHz	2.5	2.5	2.5
Current gain B	70	70	70

Minimum possible power dissipated by the head transistor has been estimated too:

$$P_{min} \geq 0.8B \cdot I_e \quad (1.20)$$

The results are summarized in Table 1.3.

Table 1.3

Characteristics	Variant 1			Variant 2	Variant 3
lopt1 (capacit. matching), mA	42.98			42.58	42.41
lopt2 (min. ENC1 ² +ENC3 ²), uA	27.3 (B=100)				
B = 70	22.9			22.7	22.6
B = 50	19.4				
Rbb', Ohm	6			12	20
Ie (operational value), uA	200	20	2.0	200	200
Gm (operational value), mA/V	7.69	0.769	0.0769	7.69	7.69
Ci=2Cbc+Ie/(ot* Γ);Ku=1, pF	5.29	4.85	4.805	4.29	3.89
Cf=Cd+Cf+Ci, pF	105.8	105.35	105.305	104.6	104.4
Pmin, uW	160	16	1.6	160	160
ENC1, r.m.s. e- (*)	660	2080	6560	650	650
ENC2, r.m.s. e- (*)	190	190	190	270	350
ENC3, r.m.s. e- (*), B=100	4810	1520	480	4810	4810
B=70		1820			
B=50		2150			
ENCsum, r.m.s. e-(*), B=100		2580			
B=70		2770			
B=50		3000			
Ccb, pF		2.4		1.9	1.7

(*) Rounded to tens of electrons.

1.5.3. Main conclusions about the head element choice

Analysis of data shown in Table 2, 3 permits to make the next conclusions:

1.5.3.1. About usage of bipolar transistors for the case of Cd = 100 pF and Tp = 1 us:

- the series noise minimization achieved by optimization of the head transistor emitter current lopt1 leads to unacceptable increasing of the parallel noise ENC3;

- the emitter current optimization should be made by minimization of ENC1² + ENC3². In this case we get lopt2 = 15 - 30 uA for different head transistor structures and B's;

- distinctions of the BI transistor structures don't affect noticeably on the total noise level because contributions of ENC2 and ENC1 versus Cbc are very small in comparison with those of ENC3 and ENC1 determined by the input current and transconductance;

- to achieve more realistic estimates of ENC one should use more precision values of Ku and the experimentally measured dependence ENC1 on $\omega t = \omega t(I_e)$ and lopt2 in the region of microcurrents (Ie = 1...100 uA);

- use of the bipolar transistor in the input stage of CSP is not the best decision in the sense of noise because in the case of Cd = 100 pF, Tp = 1 usec, B = 50...100 and optimal emitter current about 20 uA resulted noise is equal 2500 - 3000 electrons without taking into consideration noises of detector leakage current and CSP feedback resistor;

- the main advantages of BJT transistor in the mentioned case are very small occupied area in comparison with JFET, rather small dissipated power and higher speed.

1.5.3.2. About use of JFET in the case of Cd = 100 pF and the peaking time Tp = 1 usec it should be noted the next:

- all JFET variants provide the required noise level $ENC = 2000$ e- taking into account the noise produced gate leakage current about 10^{-9} A and different minimum values of the head element dissipated power 15.7 mW, 7.43 mW and 1.71 mW;

- variants 1 and 2 of JFET structures provide the same noise levels but JFET of variant 2 being of the same design rule occupies 4 times greater area and dissipates two times less power;

- The most suitable for use as the head element is JFET of variant 3;

- electrical circuitry of CSP should give a possibility to vary the head transistor drain current because this permits to provide the best combination of noise (regulated by G_m) and power dissipation (regulated by I_d).

1.5.3.3. These calculations have estimation nature. After taking into account characteristics of the new designed p-JFET's now we hope to attain more precise estimates in future.

1.6. Choice and calculation of readout path (CSP + slow shaper)

1.6.1. Preliminary notes

Let us estimate the noise contribution of factors being unknown at the beginning of this design, namely: the detector leakage current I_l and parallel resistance R_p (parallel connection of CSP feedback resistor R_f and detector bias resistor R_b). If R_b is absent, i.e. $R_b = \infty$, $R_p = R_f$, and we have

R_p	1 MΩ	10 MΩ	50 MΩ	100 MΩ
ENC_5	770 e-	240 e-	110 e-	80 e-

I_l	10^{-11} A	10^{-10} A	10^{-9} A	10^{-7} A	10^{-6} A
ENC_3	10 e-	30 e-	110 e-	1080 e-	3420 e-

Eq. (6) includes components, being dependent on T_p , both increasing and decreasing, so it possible to find the optimal peaking time

$$T_p \text{ opt} = 2C_f \left[\frac{\phi t * R_p}{3G_m(2\phi t + R_p(I_l + I_{in}))} \right]^{1/2} \quad (1.21)$$

1.6.2. Calculation of CSP and slow shaper

Readout path configuration is shown in fig. 1.1. Let us choose basic p-JFET with $2/L = 60/2.42$ as the head element of the slow shaper and JFET of variant 1 for CSP. Then we obtain the next characteristics:

Slow shaper:

Feedback capacitance C_f	0.5 pF
Coupling capacitance C_c	4.0 pF
JFET dimensions	60 μm/2.42 μm

JFET transconductance: maximum G_{mmax}	180 $\mu A/V$
operational G_m	15.58 $\mu A/V$
Peaking time T_p	1.003 μsec
Operational drain current I_d	8.2 μA
Feedback resistor R_{fc}	3.9 $M\Omega$
Total shaper capacitance $C_{ts} = C_c + C_{is} + C_{fs}$	6.6 pF
Input shaper capacitance C_{is} (Miller's effect is neglected, i.e. $K_u = 0$)	2.1 pF
Output shaper capacitance $C_{os} = C_{fs} +$ parasitic capacitance 0.1 pF	0.6 pF
Load capacitance (neglected)	0 pF
Shaper's gain A_{vs}	15.55

CSP:

Feedback capacitance C_f	0.5 pF
Feedback resistor R_f	>50 $M\Omega$
p-JFET dimensions	2868/2.42 μm
Transconductance: maximum G_{mmax}	8.6 mA/V
operational	4.0 mA/V
Operational drain current I_d	7.33 mA
Total gain (CSP + slow shaper)	11.44 mV/fC
Total noise (CSP + slow shaper):	
head JFET	2000 e-
feedback resistor R_f	110 e-
total	2010 e-
Drain current I_d provided ENC = 3000 e- ($G_m = 1.781$ mA/V)	1.98 mA
Minimum power dissipated by the head JFET when ENC = 3000 e-	2.2 mW

1.6.3. The timing channel calculation

The main timing channel characteristics are the time jitter T_j and the time walk T_w :

$$T_w = T_{w1} + T_{w2} \quad (1.22)$$

where T_{w1} - the component stipulated by the shaper pulse rise time (wavefront steepness) dependence on a value of output voltage;
 T_{w2} - the component conditioned by comparator time delay due to input signal value.

$$T_{w1} = (T_{ps2} * U_t / A_{vf} * A_{vs2}) (1/Q_{in1} + 1/Q_{in2}) \quad (1.23)$$

where T_{ps2} - fast shaper peaking time
 U_t - comparator threshold
 $A_{vf} * A_{vs2}$ - overall trigger path gain (CSP + fast shaper).
 On another hand the circuit parameters are chosen to satisfy the next inequality:

$$A_{vf} * A_{vs2} * Q_{int} \geq U_t \quad (1.24)$$

where Q_{int} - input current causing the comparator switch on.

Taking into account eq. (1.21), we have

$$T_{w1} \leq T_{ps2}(Q_{int}/Q_{in1} - Q_{int}/Q_{in2}) \quad (1.25)$$

For threshold value given in specification /9/ $Q_{int}/Q_{in1} = 0.5$, $Q_{int}/Q_{in2} = 1$ we have $T_{w1} \leq 0.4 T_{ps2}$, and since $T_w < 4$ ns the next equation is valid

$$T_{ps2} < 10 \text{ nsec.}$$

From eq. (1.24) for known $Q_{int} = 16 \text{ fC}$, $U_t = 5 \text{ uV}$ and $A_{vf} = 0.735$ we get

$$A_{vs2} > 0.431.$$

The time scattering dispersion is known to satisfy the equation

$$\sigma_t^2 = u^2 / [du(t)/dt]^2 \quad (1.26)$$

In our case this equation transforms to

$$\sigma_t = T_{ps2}/40 \text{ fC} \cdot ENC = 10 \text{ nsec} \cdot 0.48 \text{ fC}/40 \text{ fC} = 0.12 \text{ nsec.} \quad (1.27)$$

The jitter is supposed to be measured with the input charge 40 fC provided that signal amplitude dispersion is considered to be caused only by the input noise transferred through the whole system CSP + fast chapter. Summarizing this discussion we have to state the next requirements to the fast shapers:

Parameter	Required	Desired
T_{ps2}	<10 nsec	<10 nsec
A_{vs2}	>0.431	>0.86

1.6.3.1. The fast shaper head element choice

The fast shaper head element type choice was based on the peaking time calculation method of ref. /10/. It should be noted that this method is fully correct for OTA with voltage controlled head element (MOSFET or JFET) only. For Bi transistors its results may be considered to be rather qualitative than quantitative.

According ref. /10/ the peaking time is estimated to be equal

$$T_{ps2} = 2C_{ts2} / (G_{ms2} \cdot C_{fs2} / \cos^2 + 1/R_{fs2}) \quad (1.28)$$

The next types of electronic devices were considered for use as the head element of the fast shaper: low-power p-JFET, low-power JFET's of variants 1,2 and 3, Bi transistor and MOSFET with characteristics recovered from ref. /10, 13/, namely for low-power MOSFET:

$Z/L = 390/0.8$, $G_m = 220 \text{ uA/V}$ provided that $I_d = 10 \text{ uA}$, $C_i = 0.5 - 0.7 \text{ pF}$ (Miller's effect has been taken into account),

and for high-power MOSFET:

$$2/L = 4000/0.8, G_m = 3 \text{ mA/V} \text{ provided that } I_d = 200 \text{ uA,} \\ C_i = 6.9 - 7.1 \text{ pF.}$$

High-power JFETs of variants 1, 2 and 3 used in calculations had the characteristics shown in Table 1.1, but in addition we have made an attempt to get a real scaling of capacitance C_{gd} taking into consideration 20% contribution of the top gate made in the total capacitance value.

JFET's variant	G_{mmax} , mA/V	C_{gd} , pF, the worst case	C_{gd} , pF, the real case
1	8.604	100	24.7
2	19.27	100	84.7
3	31.6	100	24.7

The calculation results obtained for $C_{fs2} = 10 \text{ pF}$, $C_{c2} = 0.5 \text{ pF}$ are shown in table 1.4.

Table 1.4

Active device used		Input capacitance, pF	Transconductance, mA/V	
			maximum	for $T_p = 10.0 \text{ nsec}$
MOSFET	Low-power	0.6	0.22 for $I_d = 10 \text{ uA}$	2.73 mA/V
	High-power	7.0	3.0 for $I_d = 200 \text{ uA}$	4.35 mA/V
JFET	The worst case, $I_d = 75.3 \text{ mA}$	var.1	100	8.64
		var.2	100	19.27
		var.3	100	31.6
	More realistic scaling, $I_d = 17.5 \text{ mA}$	var.1	24.7	8.604
		var.2	84.7	19.27
		var.3	24.7	31.6
JFET, low-power		2.1	0.18	
Bipolar transistor		1.2		2.88 for $I_d = 74.9 \text{ uA}$

$$C_{fs2} = 10 \text{ pF}, C_{c2} = 0.5 \text{ pF}$$

Data of Table 1.4 permits to state that the fast shaper with the peaking time of about 10 nsec can't be realised using the CMOS technology with parameters, specified in ref. /10, 13/, because the transconductance for this purposes should to be 1.45 times greater.

Among the proposed JFETs only var.3 permits to make 10 nsec shaper, but it demands $I_d = 75.3$ mA in the worst case. Both this value and the more realistic $I_d = 17.5$ mA are unacceptable due to the high power dissipation.

Such a shaper seems to be realised only with low-power Bi transistor at relatively low operational current 75 uA, but it should be noticed once again that the calculation method being applied to Bi transistors gives large errors in the case of their operation with emitter currents greater than 0.5 uA, so these results appear to be rather qualitative in nature.

To the fire end let us provide the parameters calculated for the fast shaper used Bi transistor as the head element. Since the fast shaper introduces additional noise, the parameters has calculated for two cases: for optimum emitter current I_{opt} and the least noise (without taking into account the feedback resistor noise) and for the similar case but with enlarged R_{fs2} .

Table 1.5

The fast shaper specification

(Cfs2 = 0.5 pF, Cc2 = 0.5 pF, Cos = 3.0 pF, Cts = 2.1 pF)

I_{opt2}	: 88 uA	:	
I_e operational	: 90 uA	:	56.2 uA
Gms2	: 3.46 mA/V	:	2.16 mA/V
Tps2	: 7.15 nsec	:	10.9 nsec
Rfs2	: 100 kOhm	:	40.9 kOhm
Avs2	: 6.99	:	1.876
Avf*Avs2	: 5.146 mV/fC	:	1.38 mV/fC
ENC5, r.m.s. e- (*)	: 250	:	390
ENC3, r.m.s. e- (*)	: 450	:	360
ENC1, r.m.s. e- (*)	: 110	:	140
ENC2, r.m.s. e- (*)	: 70	:	70
ENCsum, r.m.s. e- (*)	: 530	:	550
du/dt	: 28.79 nV/nsec	:	5.52 mV/nsec
Jitter due to the shaper noise	: 0.006 nsec	:	0.032 nsec
Total jitter	: 0.120 nsec	:	0.124

In the final variant the fast shaper parameters should be recalculated taking into consideration the real values of K_u and components' parameters.

1.7. The CSP head-element estimation for the peaking time 1.0 and 0.3 usec and noise levels 3000 and 1000 r.m.s. e-

During accomplishing of this analysis we received a suggestion to investigate the possibility to achieve noise levels 3000 and 1000 r.m.s. e- at peaking times 1.0 and 0.3 us.

The head element estimation was made by the same method used for the calculations of JFET structures of the variants 1, 2, 3 and the bipolar transistor structures of the variants 1, 3 (see parts 1.4., 1.5.). The calculation results are summarized in Table 1.6.

JFET	Variant 1		Variant 2		Variant 3	
Id max, mA	14.4		57.6		78.3	
Gm max, mA/V	8.604		19.27		39.2	
Cr, pF	200.5		200.5		200.5	
Tp, usec	1.0	0.3	1.0	0.3	1.0	0.3
(ENC3 ² +ENC5 ²) ^{1/2} , r.m.s.e-	153.7	84.2	153.7	84.2	153.7	84.2
ENCsum:ENC4, r.m.s.e-	2996	2999	2996	2999	2996	2999
3000e- Gm, mA/V	1.784	5.935	1.784	5.935	1.784	5.935
r.m.s. Id operat, mA	1.989	11.76	1.796	15.64	0.620	6.134
Pmin, mW	1.848	26.57	0.793	20.37	0.138	4.292
ENCsum:ENC4, r.m.s.e-	988	996	988	996	988	996
1000e- Gm, mA/V	16.4	53.21	16.4	53.21	16.4	53.21
r.m.s. Id operat, mA	NO	NO	55.07	NO	34.28	NO
Pmin, mW	NO	NO	134.68	NO	56.07	NO
=====						
n-p-n	Variant 1		Variant 3		Comments	
Rbb', Ohm	6		20			
Tp, usec	1.0	0.3	1.0	0.3		
Iopt2, B=70, uA	22.9	76.3	22.7	75.7		
ENC2, r.m.s. e-	190	347	348	634		
ENC3, r.m.s. e-	1943	1952	1934	1936	B=70, Ie=Iopt2	
Gm, mA/V	0.881	2.93	0.873	2.91	Ie=Iopt2	
ENC1, r.m.s. e-	1940	1942	1948	1948		
ENCsum, r.m.s. e-	2746	2769	2767	2818		
Pmin, uW	18.32	61.04	18.16	60.56		

Ig = 10⁻⁹ A, Rf = 50 kOhm
 NO - the implementation is impossible.

Being analyzed they permit us to make the next conclusions:
 - BJT of all the constructions considered don't allow to attain a noise level lower than 2700 e-;

- decreasing of the peaking time to 0.3 usec leads to 3.3 times increasing of the power dissipated by the head transistor with the same noise level supported;

- all the considered constructions of JFETs don't allow to provide ENC = 1000 e- at Tp = 0.3 usec;

- it were possible to attain ENC = 1000 at Tp = 1.0 usec with JFETs if the power dissipated by the head transistor would increase to 135 mW and 56 mW for JFETs of variants 2 and 3 respectively.

In addition it should be noted that detector leakage currents were not taken into account in this estimation, and the active elements were considered to work in the theoretical limiting case of the saturation region boundary where the dissipated power is minimum. In the real circuits the transistors will be far of the saturation due to impossibility to stand the operational regime precisely, so the real head-element power dissipation will be greater than the theoretical one. Moreover, some additional power will be dissipated by another elements of the circuit especially by the fast shaper with the peaking time RC-CR of 10 nsec.

1.8. The CSP CMOS IC production possibility estimation for the case ENC=1000 r.m.s. e- and Tp=300 nsec

1.8.1. General notes

The estimation was made for a CMOS charge-sensitive preamplifier (CSP) with a RC-CR shaper according to the methodics used above for BJTs and MOSFETs with addition of the eq. (1.29 -1.31) taken from ref.[10]. A MOSFET flicker noise component is supposed to be equal

$$ENC6 = (Ct * e / q) * [Fk / (2W * Leff)]^{1/2} \tag{1.29}$$

A bulk-resistance and a channel noise components are equal

$$ENC7 = (Ct * e / q) * [Rb * S1^2 * kT / (2Tp)]^{1/2} \tag{1.30}$$

and

$$ENCB = (Ct * e / q) * [\lambda (S1 + 1) kT / (3Gm * Tp)], \tag{1.31}$$

respectively,

where:

- λ - the excess noise factor,
 - $S1 = Cdep / Cox$ - the slope factor,
 - Rb - the bulk resistance,
- the rest of terms are the same as in part 1.3. above.

1.8.2. The comparison of existant CMOS CSPs

Different implementations of CMOS CSPs known from literature [8, 10, 13, 20] were analysed with reference to GEM muon detector application. This work happened to be rather difficult due to absence of the exhaustive information needed for the noise level recalculation for the detector capacitance Cd=100 pF and the peaking time 300 nsec.

Furthermore, there are different approaches to noise estimation and results presentation accepted in the publications, namely:

- the different substrate influence description:
 $n = (1 + C_{dep}/C_{ox})$ in [13] and $S_1 = C_{dep}/C_{ox}$ in [10];
 - the different flicker noise description: one provided with A_f of $[V^2 \cdot m^2]$ dimension in ref. [10] and H_f of $[J]$ dimension in ref. [8, 20];
 - different types of shapers being used: RC-CR in ref. [8, 10, 13] and symmetric squared form in ref. [13, 20];
 - noise data is represented graphically in ref. [8, 20] and in a form of analytical equation in ref. [10, 13]. (Using of the graphic representation is very awkward because we have large errors during the ENC recalculation for our Cd, Tp.).
- The peculiarities being mentioned above lead to the next:
- the parameters signed with (*) were recalculated;
 - the parameters signed with (**) were given as standard ones.

Summarized noises of the known CSPs are given in Table 1.7.

Table 1.7

Noise possibility interpolation to JEM application
for CSPs made with different CMOS technologies

Reference	[13]	[10]	[8]	[8]	[20]	[20]	Minsk
			Fig.8	Fig.3	Fig.4a	Fig.5a	
Parameter \							
Head element	PMOS	PMOS	NMOSFET enhance- ment	PMOSFET	Monoli- PMOS	Monoli- NMOS	PMOS var.1/ /var.2
Transconduc- tance, mA/V	1.4 $I_d=50\mu A$	3.0 $I_d=200\mu A$			1.2 $I_d=100\mu A$	1.5 $I_d=100\mu A$	15.48/ /4.89* $I_d=200\mu A$
Excess noise factor \hat{s}	1.4	2.0					2.0 **
Flicker noise	$A_f=3x$ $x10^{-14}$ V^2 $S=25300$ μm^2	$A_f=2.2x$ $x10^{-13}$ $V^2 *$ $S=3440$ μm^2			$H_f=A_f x C_i =$ $5.5x10^{-24}$ $J, C_i=3$ pF $S=2800$ μm^2	$H_f=1.5x$ 10^{-23} J $C_i=3$ pF $s=2800$ μm^2	
Factor $F_k,$ $V^2 \times m^2$	$7.59x$ $x10^{-22}$	$7.6x10^{-22}$			$5.13x$ $x10^{-21}*$	$14x$ $10^{-21}*$	$9.0x**$ $x10^{-22}$
Bulk resis- tance $R_b, k\Omega m$	1.2 *	2.0					2.0 **
Slope factor $S_1=C_{dep}/C_{ox}$	0.3 ** $U_{gs}=0$ V	0.296 * $U_{gs}=0$ V					0.374 $U_{gs}=0V/$ /0.176 $U_{gs}=2.0V$
ENC6 (flicker noise), r.m.s. e-, Cd=100 pF		590					283/694

1	2	3	4	5	6	7	8
ENC7 (bulk resistance noise), r.m.s. e-, Cd=100 pF, Tp=300 nsec		989 Ugs=2.0V					1488/ /1153
Reported noise level, r.m.s.e-	400+33Ci Tp=350ns	160+12Ci Tp=1.5us	5067 Cd=100pF Tp=500ns	1500 Cd=100pF Tp=1.0us	2500 Cd=30pF Tp=100ns	2290 Cd=30pF Tp=100ns	
Interpolated noise ENCsum for Cd=100pF, Tp=0.3 ns, r.m.s.e-	3930*	2752*	6542*	2739*	4811*	4407*	2435/ 2951

* The interpolated value
** The standard value

1.8.3. The CSP parameters to be achieved with CMOS technology available in Minsk

CMOS technology used in Minsk is intended for production of digital and simple analog-digital LSI/VLSI, so the noise parameters of MOSFETs were not investigated. To estimate ENC of CSP the standard values of λ , F_k and R_b have been chosen (see Table 1.7). Two constructions of a head p-MOS transistor were estimated: with capacitance matching and without it.

	Variant 1	Variant 2
The input capacitance matching with a detector $C_i=(C_d+C_f)/3$	yes, $C_i=33.5$ pF	no, $C_i=3.35$ pF
The dimension ratio W/L	32300um/0.9um	3230um/0.9um
The transconductance G_m at $I_d=0.2$ mA	15.48 mA/V	4.89 mA/V
The noise levels, r.m.s. e-:		
ENC6	283	694
ENC7	1488	1153
ENC8	1903	2624
ENC5	109.3	109.3
ENCsum	2435	2951

1.8.4. Short conclusions

The results of the investigations given in Table 1.7 allow us to make the next conclusions:

- no one of CSP reported in literature can provide the noise less than 2700 e- with Cd=100 pF and Tp=300 nsec;
- the least achievable noise about 2400 e- could be expected with MOS transistor of variant 1 which can be made with CMOS technology available in Minsk too;
- the gigantic size of such a transistor (32.3 mm) is supposed to lead to a low yield and, consequently, to high price of ICs.

1.9. Description of the IC design

1.9.1. BJT/JFET IC construction

We have chosen two versions of IC for realisation based on analyses reported above. The first one has a bipolar n-p-n microwave transistor used as a head element of amplifier circuit, the second one uses for such a purpose p-type JFET. The BJT version seems to be more preferable to achieve necessary time jitter and time walk, but it seems to possess no reserves in decreasing of ENC at peaking times about 1 us. Our calculations show the possibility to achieve ENC about 2500 - 3000 r.m.s.e- at peaking time 1.0 us, and this results are in a good agree with 2800 e- from literature [8, 20]. Nevertheless, this drawback seems to be less obvious with the peaking time decreasing to 0.3 us.

The second version has JFET as a head amplifier active element. It assumed to be more promising for achieving low ENC (we estimated 2000 r.m.s. e- for 1.0 us, but there we may have met some problems with speed of the fast shaper and power consumption in the head CSP transistor).

For the purpose of more precise estimation of a CSP head transistor parameters to be realised in the next production iteration we have made the two channels of one IC with different input transistor parameters both for BJT and JFET versions. Both the BJT and JFET versions are made in the same chips with overall number of channels being equal 4, and one or other IC version (two channels) is wired to pins accordingly the user demand.

IC is placed in 48 pin planar four-side package. Each channel has separate voltage supply inputs. In addition a substrate output has no galvanic contact with the most negative potential bus. This construction peculiarities appear to decrease crosstalks between the channels as much as possible. To decrease ICs' price they were packaged into the cheapest packages made from oxidized aluminium.

1.9.2. Head stage technology features

CSC CSP/shapers ICs are made in high radio frequency combined bipolar-field (BJT-JFET) technology. Element base construction peculiarities consist of the next items:

- only n-p-n BJTs and pJFETs are used as active devices;
- presence of two buried layers n+ and p+ in n-type epitaxial structures;
- combined interelement insulation;
- selfalignment of n+ gate and n+ emitter areas.

The technology to be used has the next features:

- using of only ion doping;
- Boron doping through a preliminary grown thermal oxide;
- simultaneous formation of different conductivity type regions;
- two-level metallization.

The technological process includes 14 photolithography operations, 8 ion doping operations and has a block structure.

1.9.3. IC layouts

To speed up the optimization of IC design IC was made from separate cheme-topological parts which being internally interconnected and accomplished with discrete elements gave possibility to implement

the desired functions. This parts were different both in chematics and in head transistor construction. The BJT version contains:

- similar in the two channels slow (signal) and fast (trigger) shapers having a head n-p-n made with a design rule $h = 1.5 \text{ } \mu\text{m}$, a number of emitter strips $n = 3$ and $R_{bb}' = 93 \text{ Ohm}$, $\text{AREA} = 0.3$;

- different in the two channels CSP head transistors:
channel 1 (input pin 45) - $h = 1.5 \text{ } \mu\text{m}$, $n = 3$, $R_{bb}' = 93 \text{ Ohm}$, $\text{AREA} = 0.3$;
channel 2 (input pin 05) - $h = 1.5 \text{ } \mu\text{m}$, $n = 10$, $R_{bb}' = 15 \text{ Ohm}$, $\text{AREA} = 1.0$; this transistor was supposed to be basic one for model constructions and measurements;

- a scaling factor for minimum size n-p-n $\text{AREA} = 0.012$;
- all the JFETs are the same and have $U_{th} = 2.6 \text{ V}$; VT4, VT5, VT7, VT13, T16 have $\text{AREA} = 0.117$, VT10, VT11 have $\text{AREA} = 0.091$. The TA2 connected-gates JFETS measurements results listed in part 2.6 correspond to $\text{AREA} = 1.5$;

- a protective diod chain is placed only in channel 1 and operates with a biased substrate and zero potential on the channel 1 ground pin (0 V at pin 47 and -Ecc at pin 24).

The JFET version contains:

- similar in the two channels slow and fast shapers having head pJFETs with $\text{AREA} = 0.235$;

- output pJFETs with $\text{AREA} = 0.235$;

- channel 1 and 2 differ by the head element:

channel 1 (input pin 2) has pJFET with $\text{AREA} = 1.5$;

channel 2 (input pin 5) has pJFET with $\text{AREA} = 1.0$;

- all the n-p-n transistors have the same scaling factor $\text{AREA} = 0.012$;

- all the resistors of all the channels have 60% overstated values in reality compared with nominals to be supposed.

The large number of the interconnections lead to a large number of contact pads whose size and pitch determine the die size. The contact pads are placed on two rings (44 pads for BJT version 1 and 34 pads for JFET version 2). Inside area of the internal contact pad ring is occupied by two JFET version channels and two BJT version channels together with test array TA2 dedicated to optimize the technological process and constructions of the head transistors.

The overall single channel size without contact pads and RC-CR elements equals:

- $1300 \times 300 \text{ } \mu\text{m}$ for version 1 (BJT)

- $1100 \times 400 \text{ } \mu\text{m}$ for version 2 (JFET).

1.9.4. Electric circuits of BJT version

As it was mentioned above one readout BJT-version channel contains CSP, fast shaper, slow shaper supplied by two separate equal biasing networks. The BJT version channel 1 electric circuit is shown in Fig. 1.2, the channel 2 circuit, being identical except of pin designation, is shown in Fig.1.3. CSP consists of transistors VT2, VT5, VT6, VT10, VT11 and VTc2. VT2 is the low noise input (head) transistor (different in channels 1 and 2) having rather large size to minimize thermal series noise. VT5 is a p-channel JFET. VT5 cascodes the VT2 and is loaded with current generator VT6. Application of the active load (current generator VT6) allows to increase the gain and gives the possibility of adjusting of the standing current. VT10, VT11 form an output buffer, where the capacitance feedback is closed. It is implemented with JFETs rather than with BJTs because such a configuration is more suitable when the output signal is negative.

Channel 1

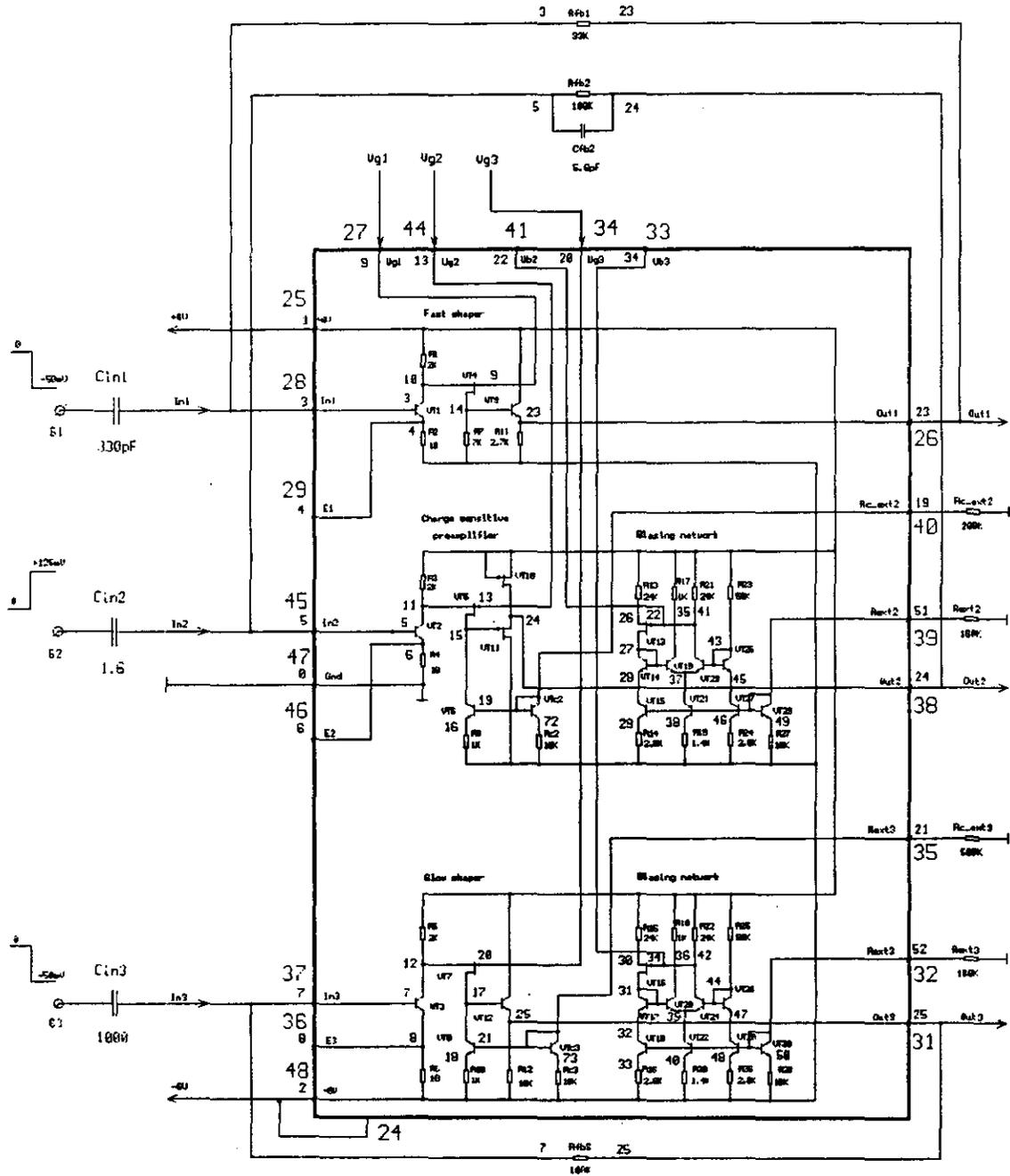


Fig.1.2. The bipolar version of IC

Channel 2

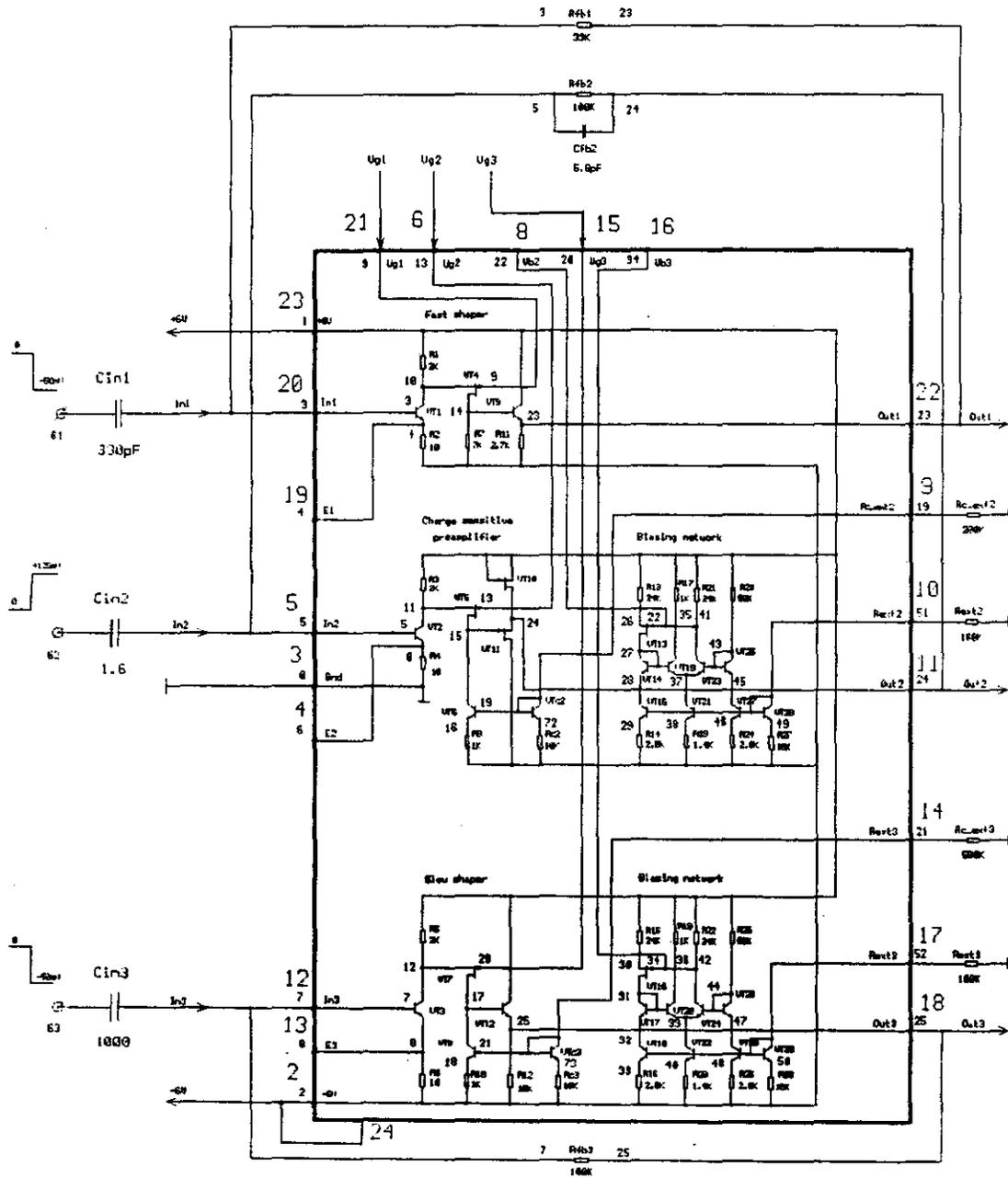


Fig.1.3. The bipolar version of IC

The high speed in this amplifier is obtained, since VT1 has very high transition frequency at low standing current and VT2 has very small dimensions with, consequently, a negligible output parasitic capacitance.

The biasing networks are separate and identical for the CSP and for the slow shaper.

The standing currents of transistors VT2 and VT5 are setted through the current mirror VT6-VTc2 by the resistor Rc_ext2, external to the chip.

The CSP biasing network (VT13 - VT15, VT19, VT21, VT23, VT25, VT27, VT29) also provides insensitivity of CSP to changes of a threshold voltage of JFET VT5. No matter, what concrete value of the threshold voltage VT5 has (in reasonable limits, of course), the biasing network will set such potential on the gate of VT2, that it will be in the nominal current mode. It consists of a multistage current mirror VT16, VT21, VT27 and VT29 with external setting of working currents with the external resistor Rext2. The difference stage VT19-VT21 compares voltage dictated by the drain current of the reference JFET VT13 being identical to the cascode JFET VT5 of CSP, with the reference voltage made by the stable current of VT27. As VT5 and VT13 have similar size and construction they have similar both threshold voltages and their drifts, which are compensated by the biasing circuit.

In order to get the best compromise between speed, noise and power dissipation the biasing of the preamplifier can be modified by means of external resistors. It should be pointed the need of separate sets made with Rext2 for the gate voltage of the cascode VT5 and for its drain current made with Rc_ext2.

The circuit of the slow shaper (VT3, VT7, VT8, VT12 and VTc3) is somewhat alike that of CSP. The difference in the output buffer (the BJT rather than JFET) is caused by different polarity of the output signal. The standing currents of the slow shaper transistors are less than those in the preamplifier because there is no necessity of very fast operation here. This allows to diminish the total power consumption. Biasing of the slow shaper is identical to that for CSP and is made with external resistors Rc_ext3 and Rext3 through the separate biasing circuit (VT16 - VT18, VT20, VT22, VT24, VT26, VT28 and VT30) being identical to the CSP biasing circuit and through the same current mirror VT8-VTc3. It should be noted that in the next production iteration this external resistors Rc_ext3 and Rext3 should be placed into the chip.

The fast shaper is somewhat simplified version of the same folded cascode circuit. The dimensions of the input transistor VT1 here are much less than that of the preamplifier, because the noises considerations here are of no interest. So this transistor operates faster. The absence of the current generator in the drain circuit of the JFET VT4 also makes the circuit faster. This absence also decrease the gain, but it is of no importance here. The shaping time of the fast shaper, calculated with the emulating program SPICE, is about 25 nsec. The total power consumption in the nominal mode (Rext=100k) is estimated to be equal 60 mW (it is the calculated value).

All the inputs and outputs of the six BJT amplifying structures of the (CSP + slow shaper + fast shaper)x2 are separated and led to chip pins as far as inputs and outputs of the two biasing circuits and the dynamic load transistors current setting inputs of CSPs and slow shapers. Such an organization permits us to optimize the head transistor currents in all amplifying structures of the chip for minimizing noise levels and dissipated power, to connect feedback capacitors and resistors of different values to set different peaking time, to inves-

tigate the dependence of crosstalks on biasing circuit shared between the amplifier structures of a single channel and between the two channel of a single chip.

In addition all the head transistor emitters points are led to output pins to permit measurements of the head transistors currents and to investigate experimentally the possibilities of the electrical circuits structures optimization.

In the next design iteration we suppose to hide all the auxiliary inputs and outputs inside the chip, providing more large number of channels per package.

1.9.5. Electric circuits of JFET version

The second version with a head JFET seems to be more promising for achieving low ENC (we estimated 2000 r.m.s. e⁻ for 1 usec), but there are some problems with the speed of the fast shaper and power consumption of the head CSP JFET.

The JFET version IC is shown in Fig. 1.4 (channel 1) and in Fig.1.5 (channel 2). Their electric circuits are similar except of the size of the head CSP JFETs being mentioned above. The first CSP stage is a folded cascode, but the head transistor in contradistinction to the BJT version is p-type JFET, the cascode transistor is n-p-n. There is a JFET source follower at the output of CSP to make negative pulse front more fast. The fast and slow shapers have n-p-n BJT emitter followers at their outputs being adopted for such a purpose with positive pulses. The bias of the cascode n-p-n is made with a resistor divider and a filtering capacitor, but in the second design iteration pull-down resistors are supposed to be replaced by diode chains. The CSP input is protected against large positive pulse voltages with a diode chain being connected or disconnected by wiring. The input-output ideology is the same as in the former case.

1.9.6. Pspise BJT version simulations

The proposed electric circuit of readout channel for the cathode strip chamber was simulated with Spice. The main goal of simulation was to get convinced in the operatability of the basic design concepts and to set more presiously the nominal values of passive elements and operating modes of transistors. Spice models of JFET and bipolar transistor were composed from measurement results of test specimens, which were produced earlier by the same technology. Full Spice model of the circuit and the simulation results including circuit response on the maximum input charge (200fC) are presented in fig. 1.6 - 1.8, and the Spice description of the circuit is presented in Appendix 1.

The simulation performed allows to predict some main parameters of designed integrated circuit. Voltage gain of charge sensitive preamplifier and slow shaper will be about 400, and voltage gain of fast shaper will be almost ten times less then that value. It is caused by the absence of active load in the fast shaper's cascode. Having less gain, fast shaper has much faster response. In the case of delta-pulse stimulation the risetime of output signals will be:

- for the fast shaper - about 40ns;
- for the slow shaper - about 300ns;
- for the charge sensitive preamplifier - about 40ns.

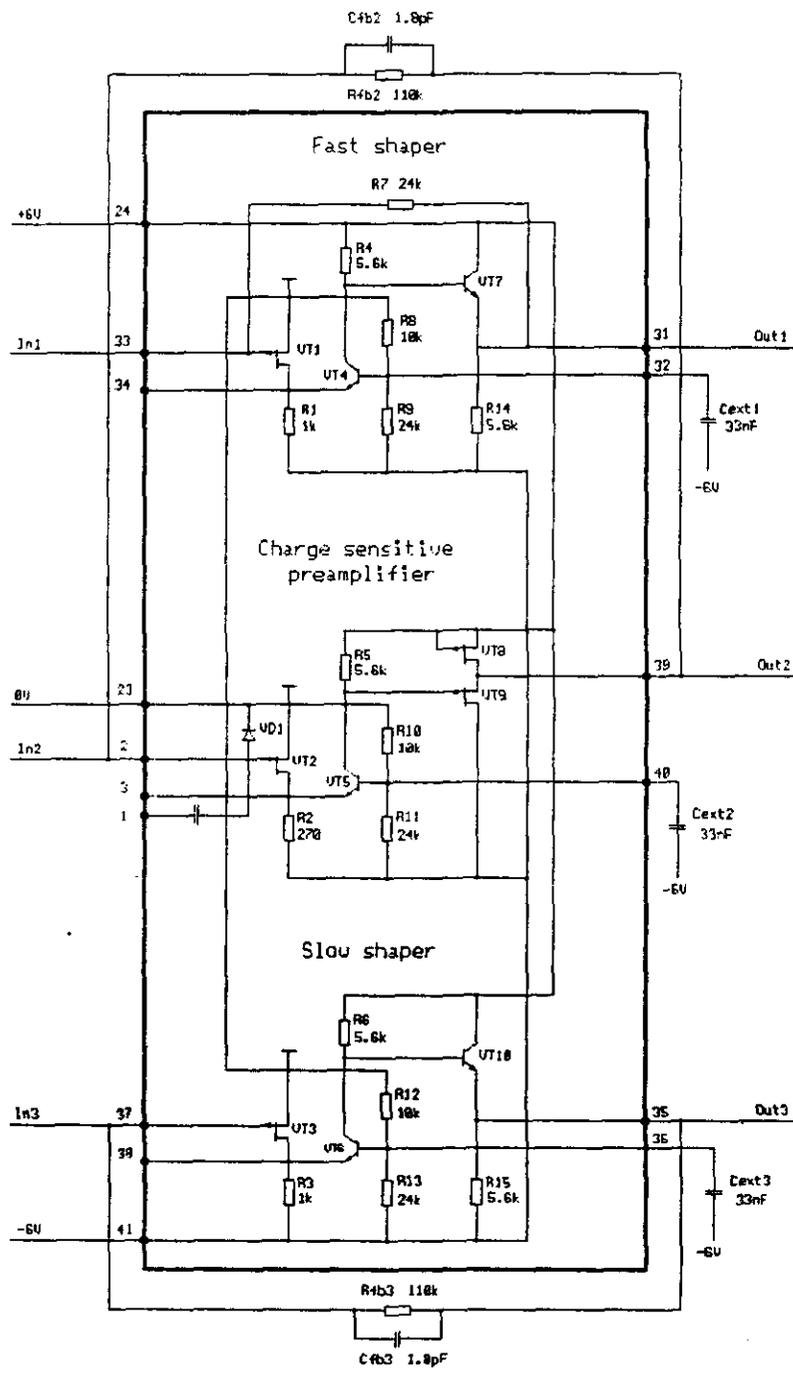


Fig 1.4. The JFET version of IC (channel 1)

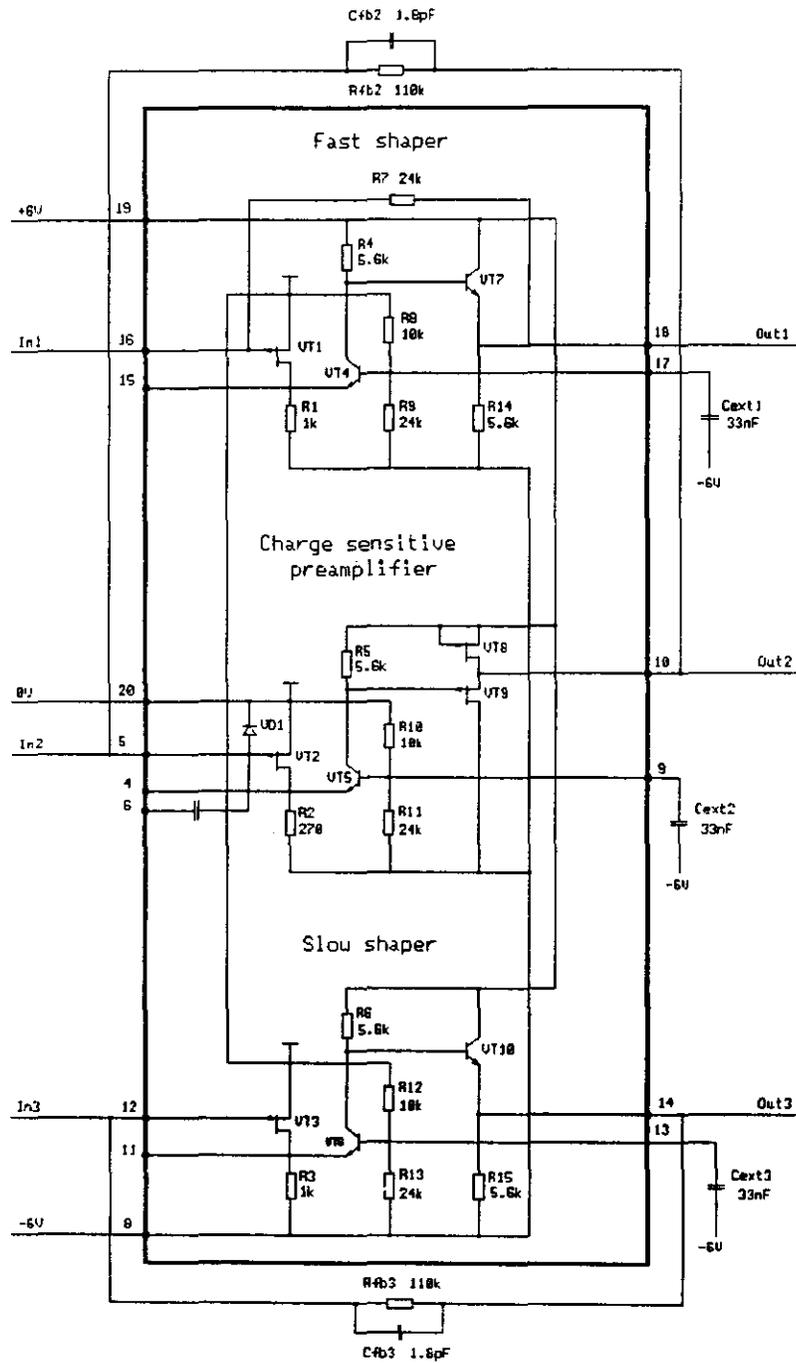


Fig 1.5. The JFET version of IC (channel 2)

Fig.1.6 CSA response (simulation)

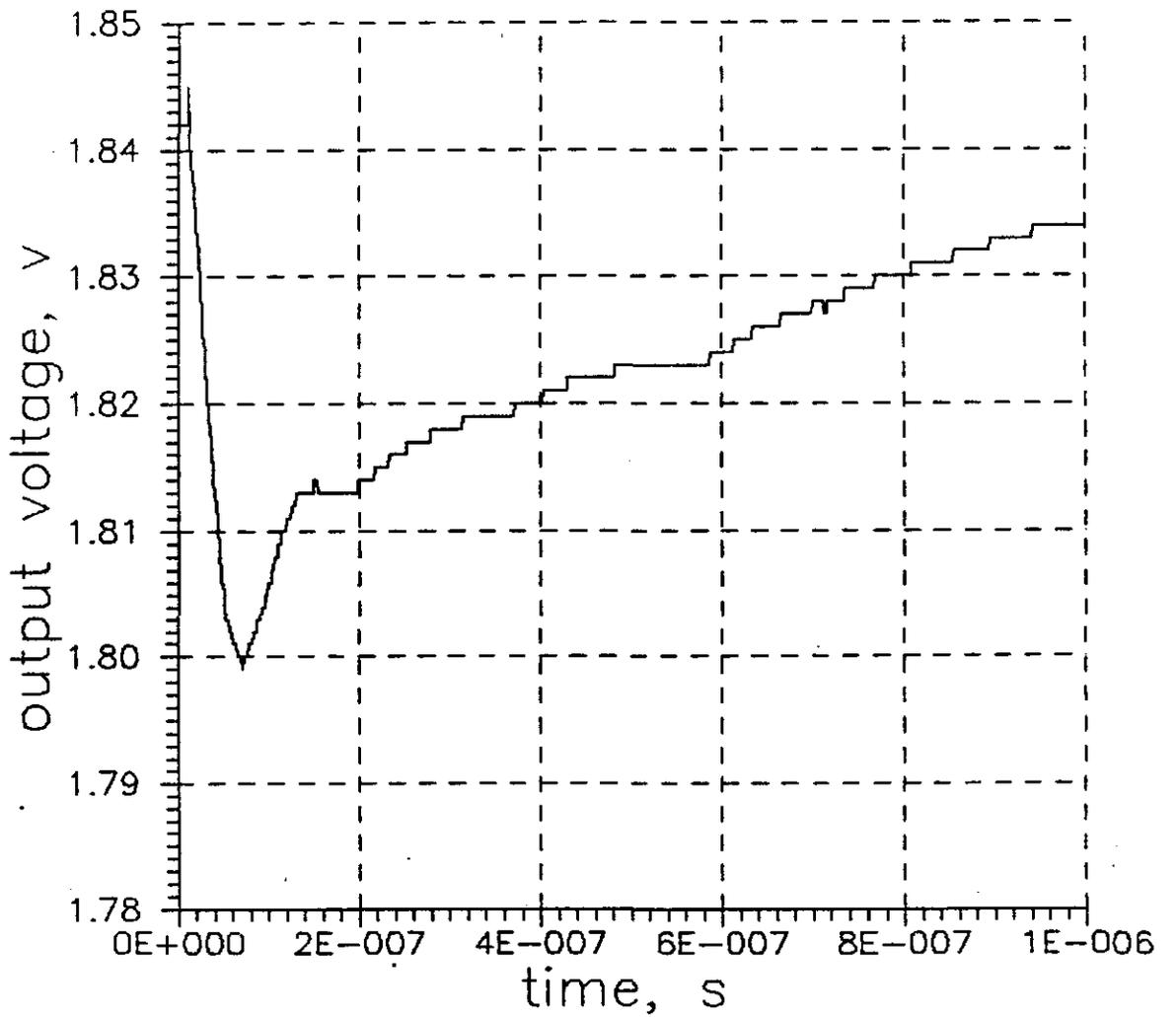


Fig. 1.7. Slow shaper response (simulation)

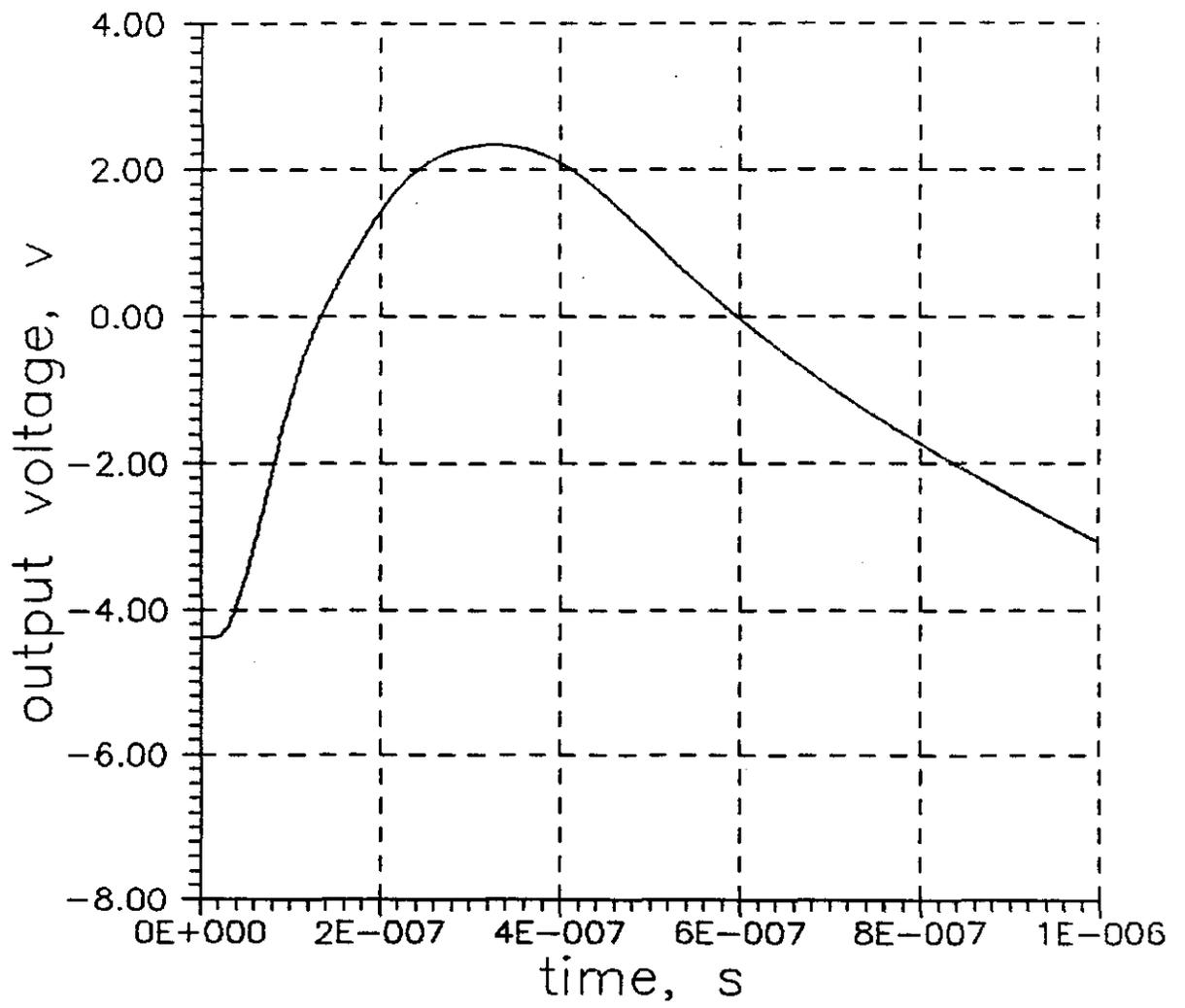
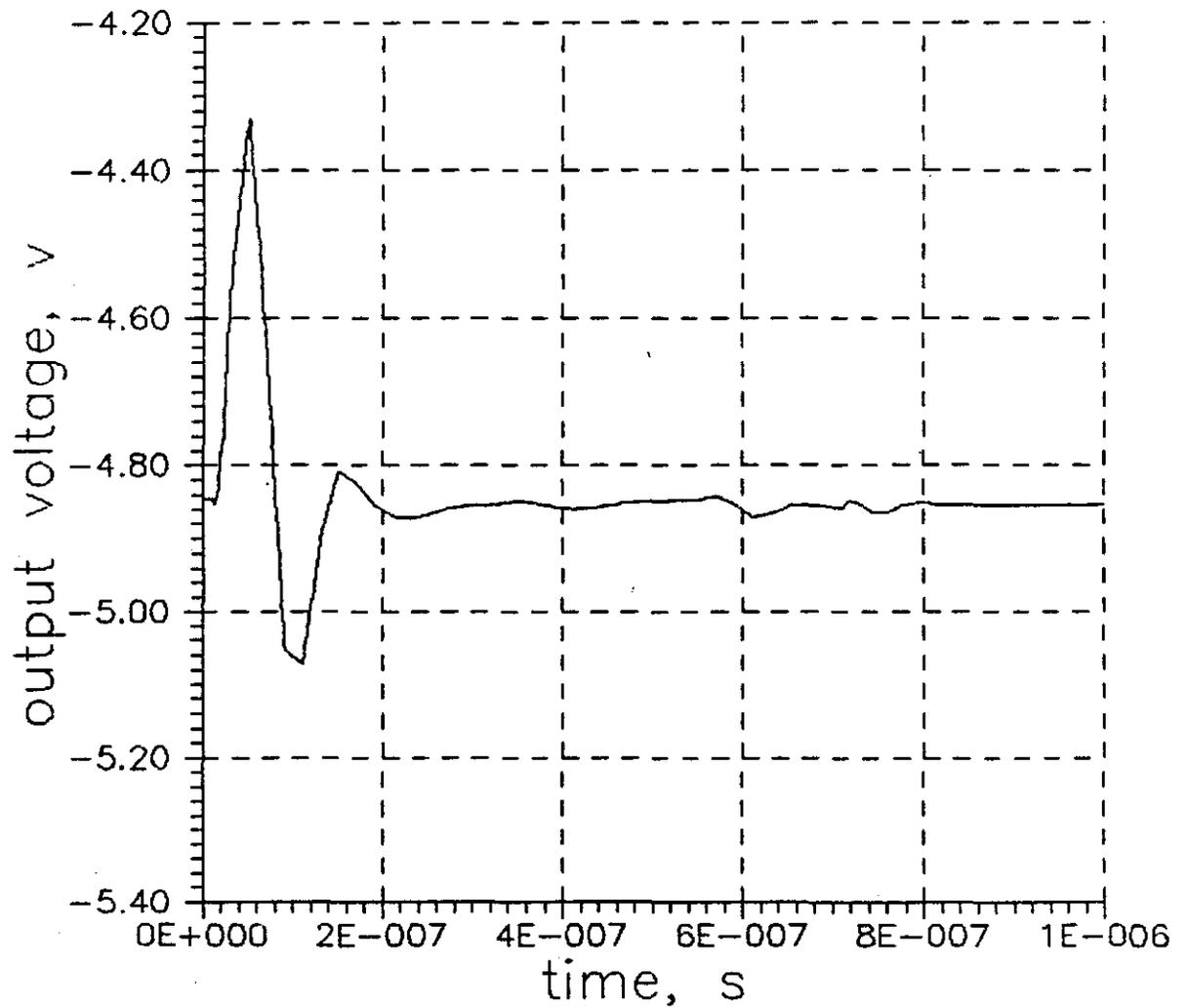


Fig.1.8. Fast shaper response (simulation)



The standing current of charge sensitive preamplifier input device can be adjusted in the range 0.5mA...2.0mA by means of external current setting circuits.

The large number of external current setting circuits in the scheme of first iteration provides an ability to set circuit in the optimal operating mode even if real parameters of integrated elements would differ (in reasonable range) from ones used in Spice simulation.

The test electronic device measurements reported in the next Part 2. of this report were used to modify BJT and JFET Pspice models and face values of resistors. Figs.1.9 - 1.11 show the results of the refined Pspice stimulation, the Pspice circuit description is presented in Appendix 1 too.

1.9.7. Discrete elements BJT version breadboard modelling

The bipolar version of CSP made with discrete components on a breadboard was tested. The electric circuit to be modelled is shown in Fig.1.12. The channel consists of CSP, SS and FS and has a common biasing circuit to compensate cascode JFET threshold voltage shift and to set collector current of the head CSP transistor. The head CSP element VT1 was made of four parallel connected low noise microwave transistors KT640A, the head transistors of SS and FS VT7 and VT11 as far as the CSP cascode load VT3 and the FS/SS output emitter followers VT13 and VT10 are KT399A, field-effect transistors are the JFET double-transistor groups K504HT1A. All the resistors forming the biasing circuit are five-transistor groups K198HT1A. The model tests has shown the operability of all the parts of the circuit. The front edge was found to be equal 40 nsec for the CSP and 20 nsec for the fast shaper.

1.9.8. Pspice JFET version simulations

The electric circuit of the two channels of the JFET version IC is shown in Fig. 1.4, 1.5 and is described in part 1.9.5.

The JFET version CSP noise characteristic is determined in the first order by head JFET VT2 transconductance G and gate capacitance C_g . At the first step of JFET version Pspice simulations G and C_d were supposed to be equal 10 m/V and 5 pF respectively. Such a value of the transconductance gives a value $R_s = 67 \text{ Ohm}$ for series noise resistance of the JFET channel. The second simulation step was made after the mentioned above Pspice parameter modification. The head JFET of the channel 2 is considered to have $G_{\max} = 15 - 19 \text{ mA}$, $U_{th} = -2.5 \text{ V}$, $AREA = 1.0$. The head JFET of the first channel has the area coefficient $AREA = 1.5$. JFETS of the SS/FS input stages and at the CSP output have $AREA = 0.235$. For BJTs an area coefficient was determined respectively the BJT version channel 2 head n-p-n transistor and was equal $AREA = 0.012$.

The CSP JFET electric circuit used in the refined Pspice simulation is shown in Fig.1.13. Pspice description of the circuit is the next.

*T-2, JFET, AREA=1, Cd=100p, Cin=1p, Cfb=3.3p

```

j1 2 1 0 kpf2
r1 2 200 150
r2 100 3 8.2k
q2 3 4 2 200 mod2 0.06
r3 0 4 10k
r4 4 200 24k
Cext 4 200 0.033u
j3 5 100 100 kpf2 0.235
j4 200 3 5 kpf2 0.235

```

```

Rfb 1 5 100k
Cfb 1 5 3.3p

```

```

Rin 50 0 50
Cin 50 1 1p

```

Cd 1 0 100p

```

Vp 100 0 DC 6
Vn 200 0 DC -6

```

Vin 50 0 pulse(0 -10000mv 10ns 1ns 1ns 2000ns 10000ns)

```

.MODEL mod2 npn IS=95e-18 BF=90 VAF=20 IKF=10m ISE=95e-18 xtb=1.5
+ NE=1.2 BR=0.7 VAR=20 IKR=1m ISC=2.39E-13 NC=2 RB=15 IRB=10m
+ RBM=10 RE=5 RC=15.0 CJE=1.45p MJE=88m VJE=0.75 CJC=1.93p MJC=88m
+ VJC=0.82 XCJC=0.2 CJS=2.2p MJS=0.5 VJS=0.75 tr=10n tf=20p itf=10m
+ vtf=20 xtf=2

```

```

.MODEL kpf2 pjf VTO=-2.5 BETA=2.5m LAMBDA=43.3m RS=15 RD=15
+ CGS=9.27p CGD=9.2p FC=0.5 PB=1 IS=10f

```

```

.TRAN/OP 1nS 500nS
.PROBE
.END

```

The simulation results are presented in Figs.1.14 - 1.21. From Figs.1.14, 1.15, 1.18 and 1.19 it is seen that CSP has large speed, the pulse front edge lasts less than 10 nsec. Waveforms shown in Figs.1.16, 1.17, 1.20 and 1.21 show the gain is too low to use such a circuit for CSC muon detector application: the channel 1 has $K_u = 42$ and the channel 2 has $K_u = 28$.

1.9.9. Discrete element JFET version breadboard modelling

The charge sensitive preamplifier was modelled with discrete components on a breadboard. The electric circuit of the model is presented in Fig. 1.22. The head VT1 is low noise high transconductance n-type JFET KA903A with $G = 50 \text{ mA/V}$, VT2 and VT3 are KT363ü. The model has demonstrated the operability of the circuit. The front edge of the output pulse was equal 25 nsec at $C_d = 220 \text{ pF}$, $R_f = 100 \text{ k}\Omega$, $C_f = 10 \text{ pF}$ and 100 nsec at $R_f = 10 \text{ M}\Omega$ and $C_f = 2.2 \text{ pF}$. The noise measurements gave $ENC = 900 \text{ e}^-$ at $C_d = 0$.

Fig.1.10 Response of the circuit, presented on the Fig.2.3, simulated with more precise transistor's models.

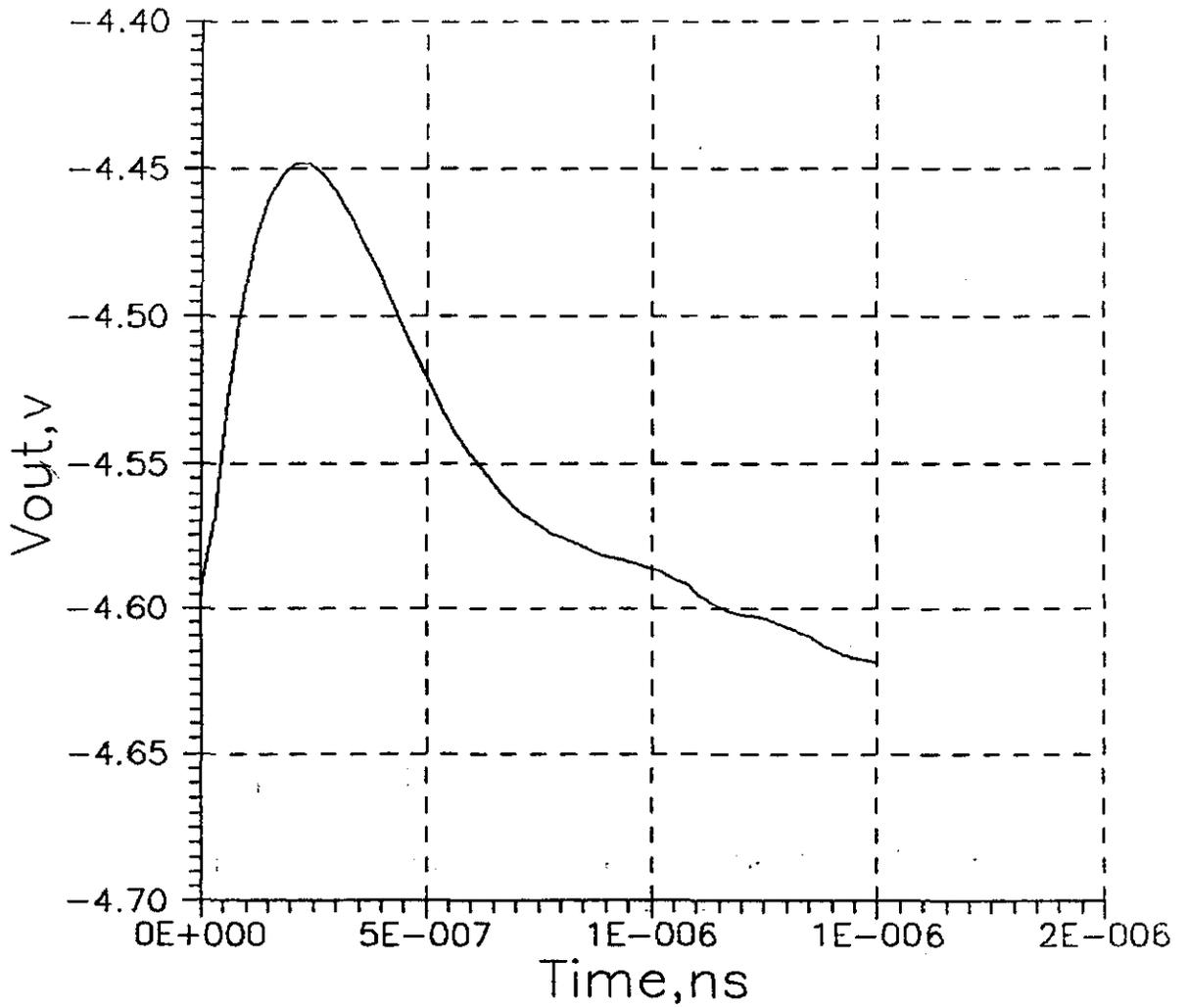


Fig.1.11. Fast shaper response (simulation).

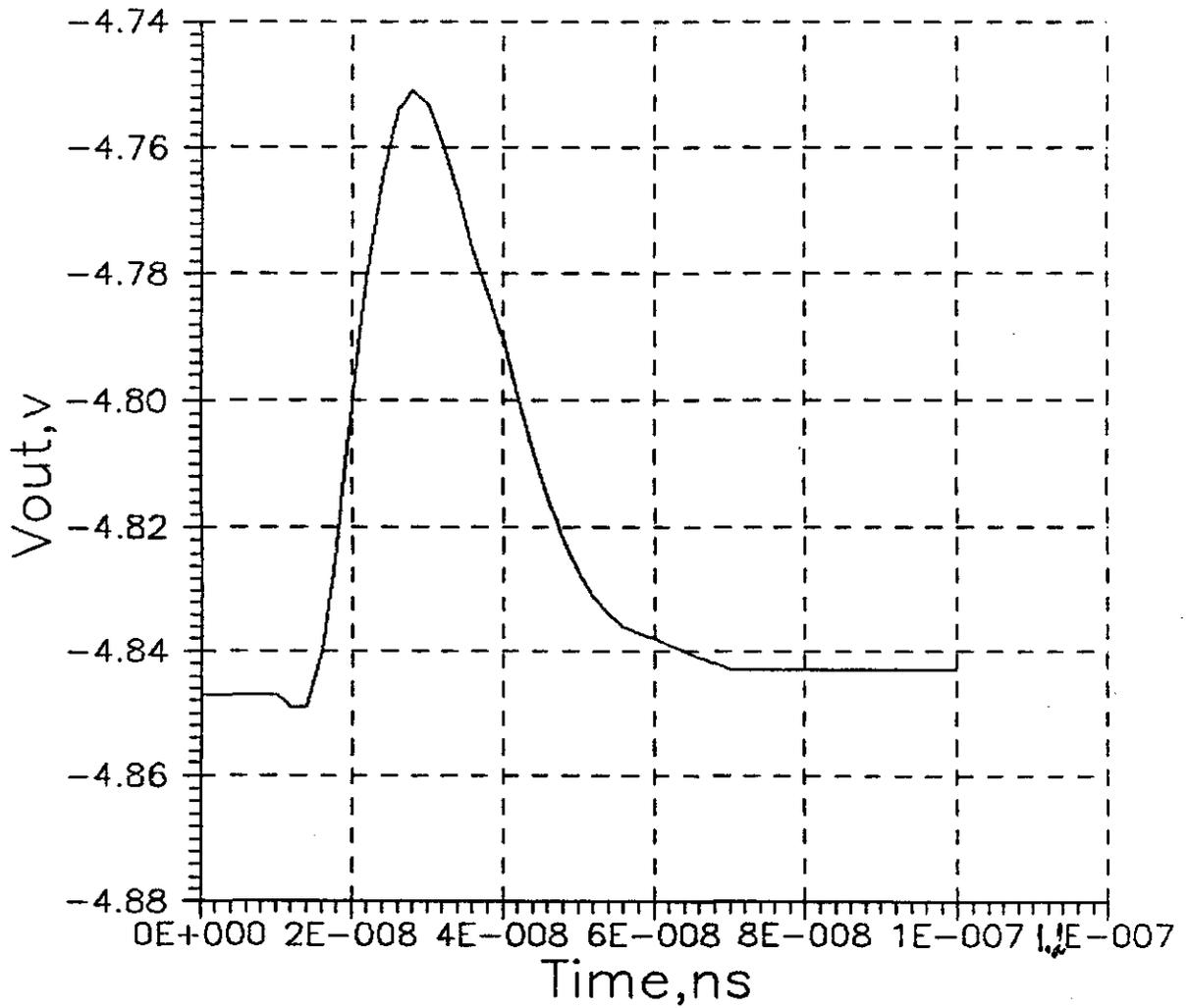
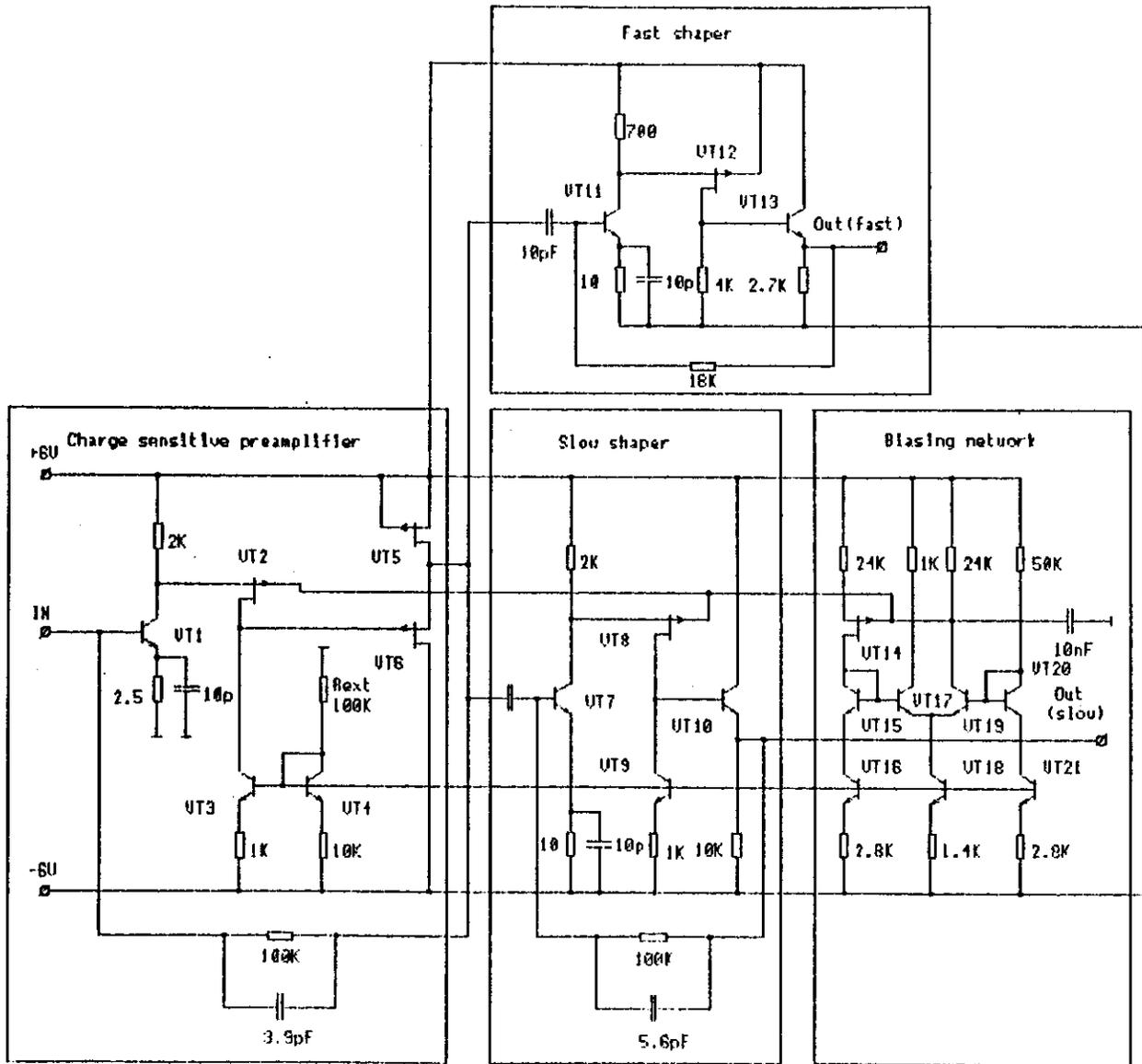


Fig. 4.12. An Electric Circuit modelled with discrete elements
 Clements



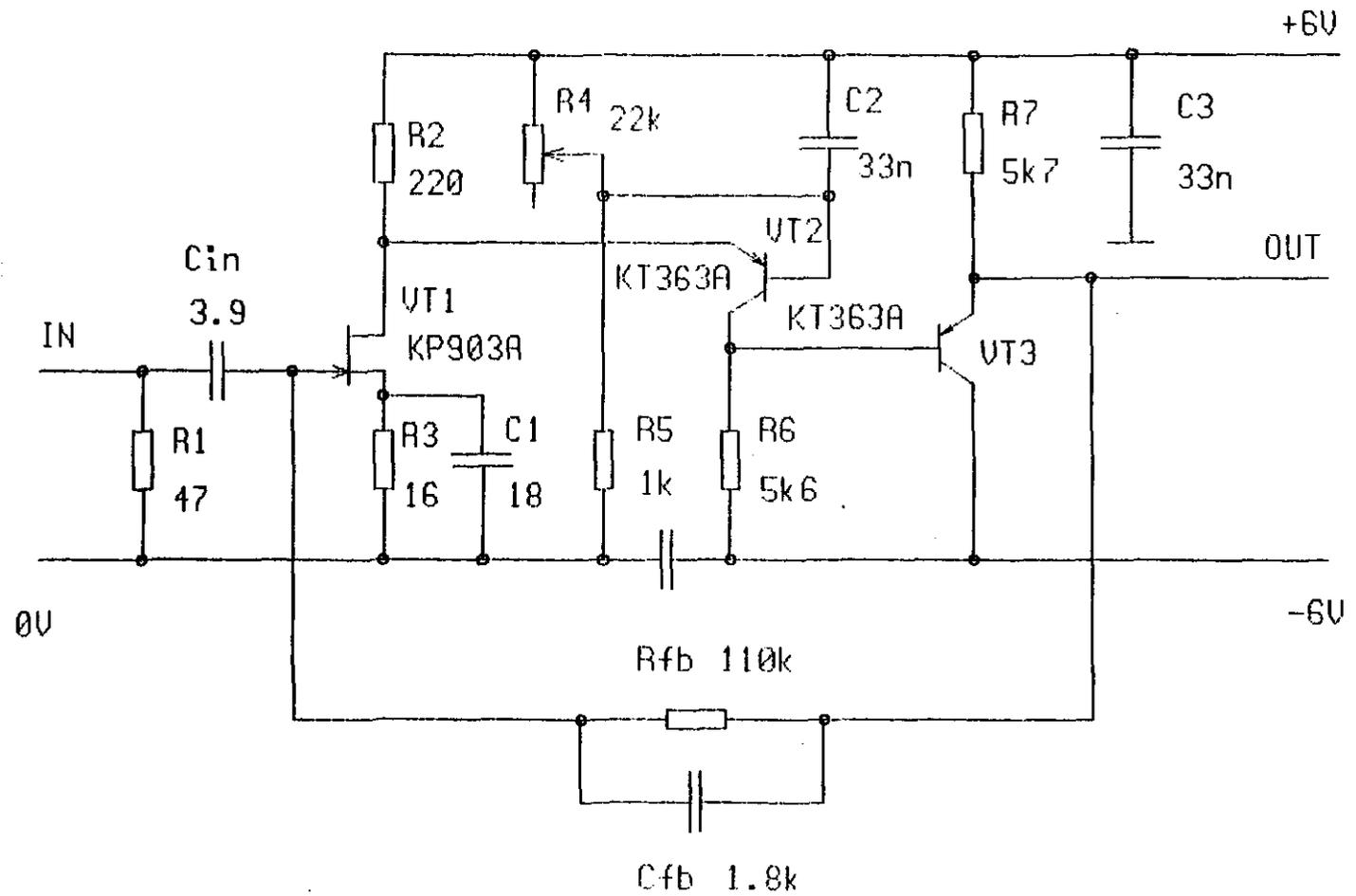


Fig. 1.13. The breadboard model of the charge sensitive preamplifier.

Fig.1.14. Channel 1. Preamplifier, response with $C_d=0$, Risetime=5ns.

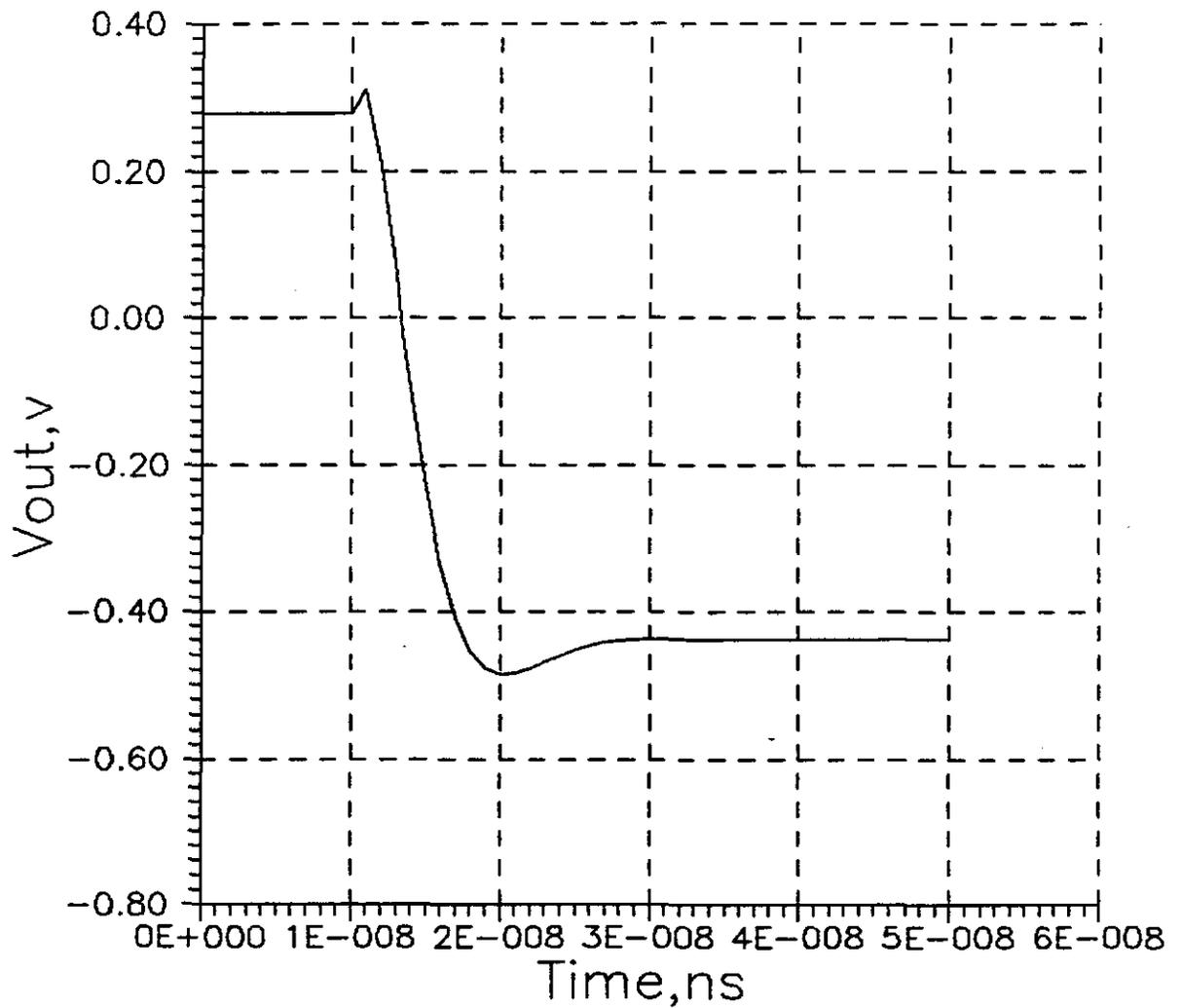


Fig.1.15. Channel 1. Preamplifier, response with $C_d=100p$, Risetime=14ns.

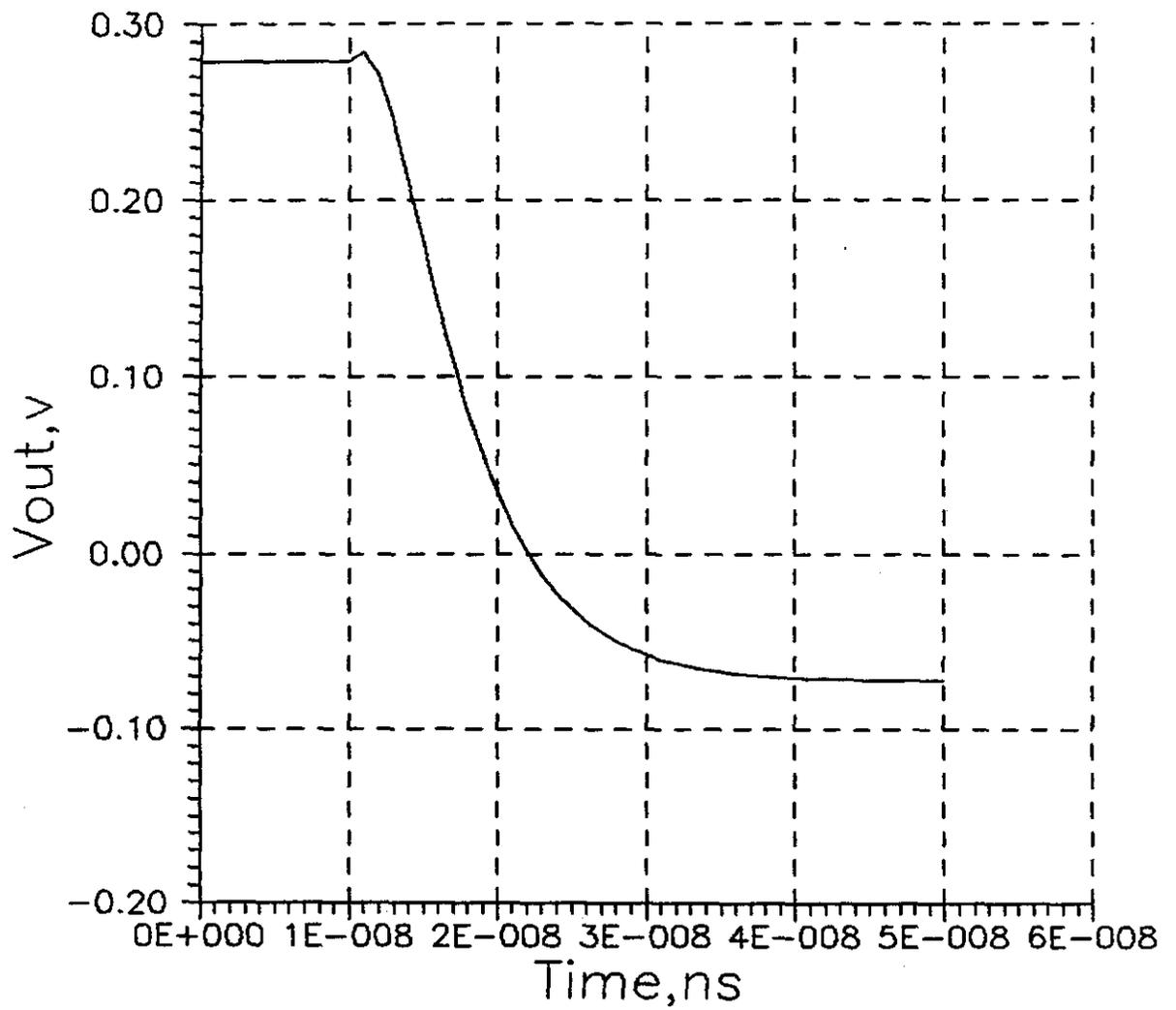


Fig.1.16. Channel 1. Response of the preamplifier, which is set in the voltage gain mode, $V_{in}=-100\text{mV}$, $C_{fb}=0$, $C_{in}=0.068$, $\text{Gain}=42$, $\text{Risetime}=20\text{ns}$.

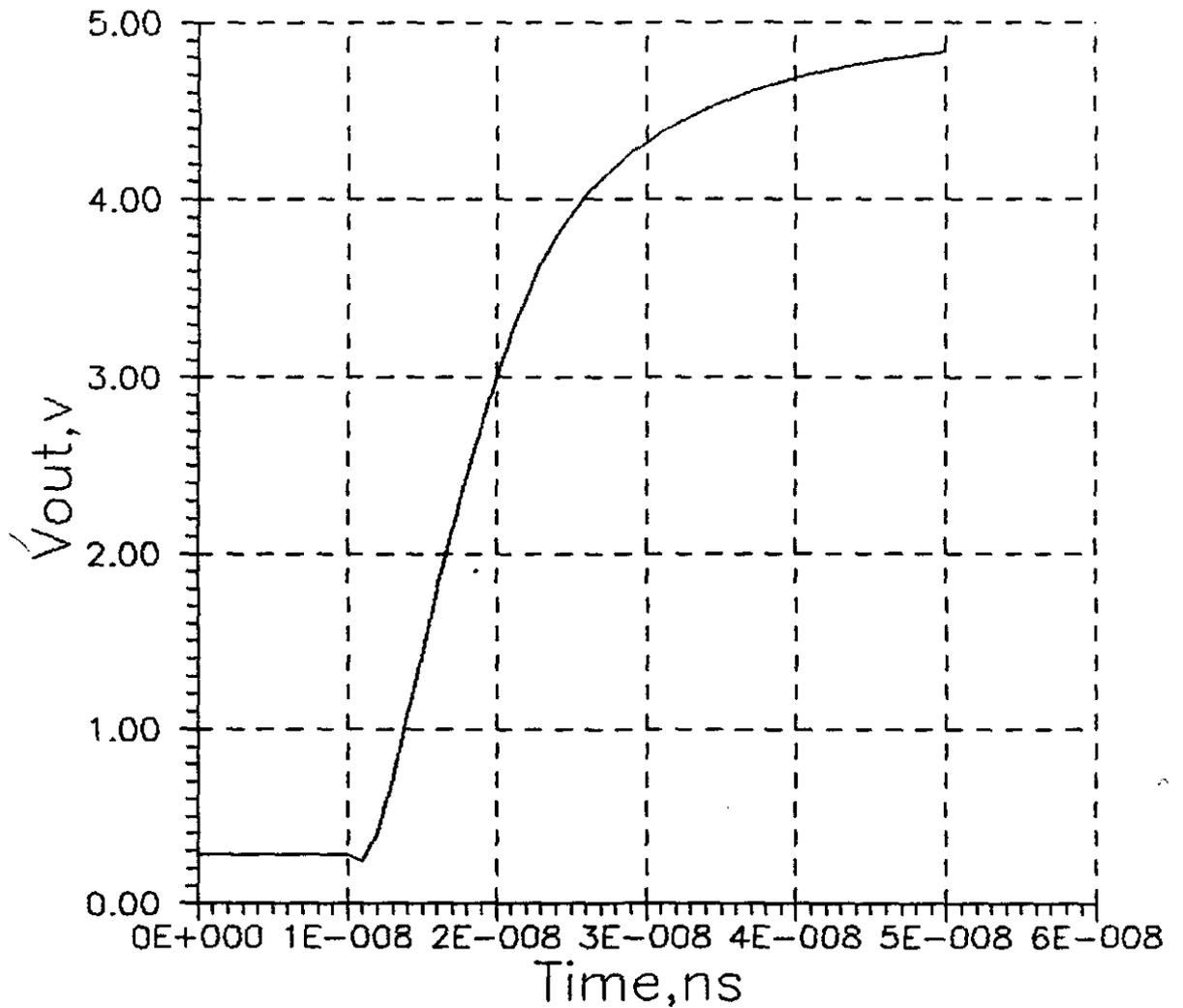


Fig.1.17. Channel 1. Response of the preamplifier, which is set the voltage gain mode, $V_{in}=40\text{mV}$, $C_{fb}=0$, $C_{in}=0.068$, $\text{Gain}=42$, $\text{Risetime}=20\text{ns}$.

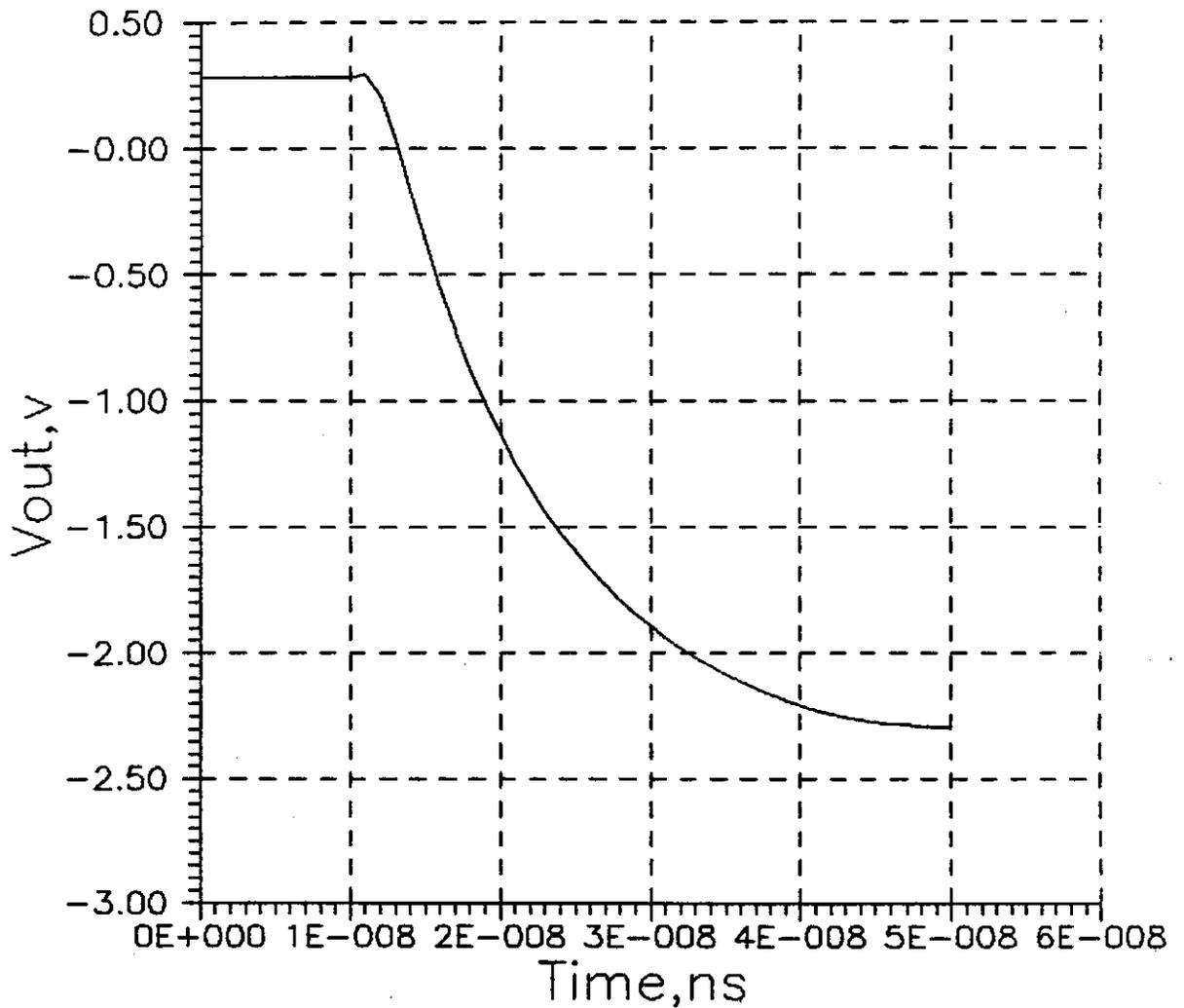


Fig.1.18. Channel 2. Preamplifier, response with $C_d=0$, Risetime=5ns.

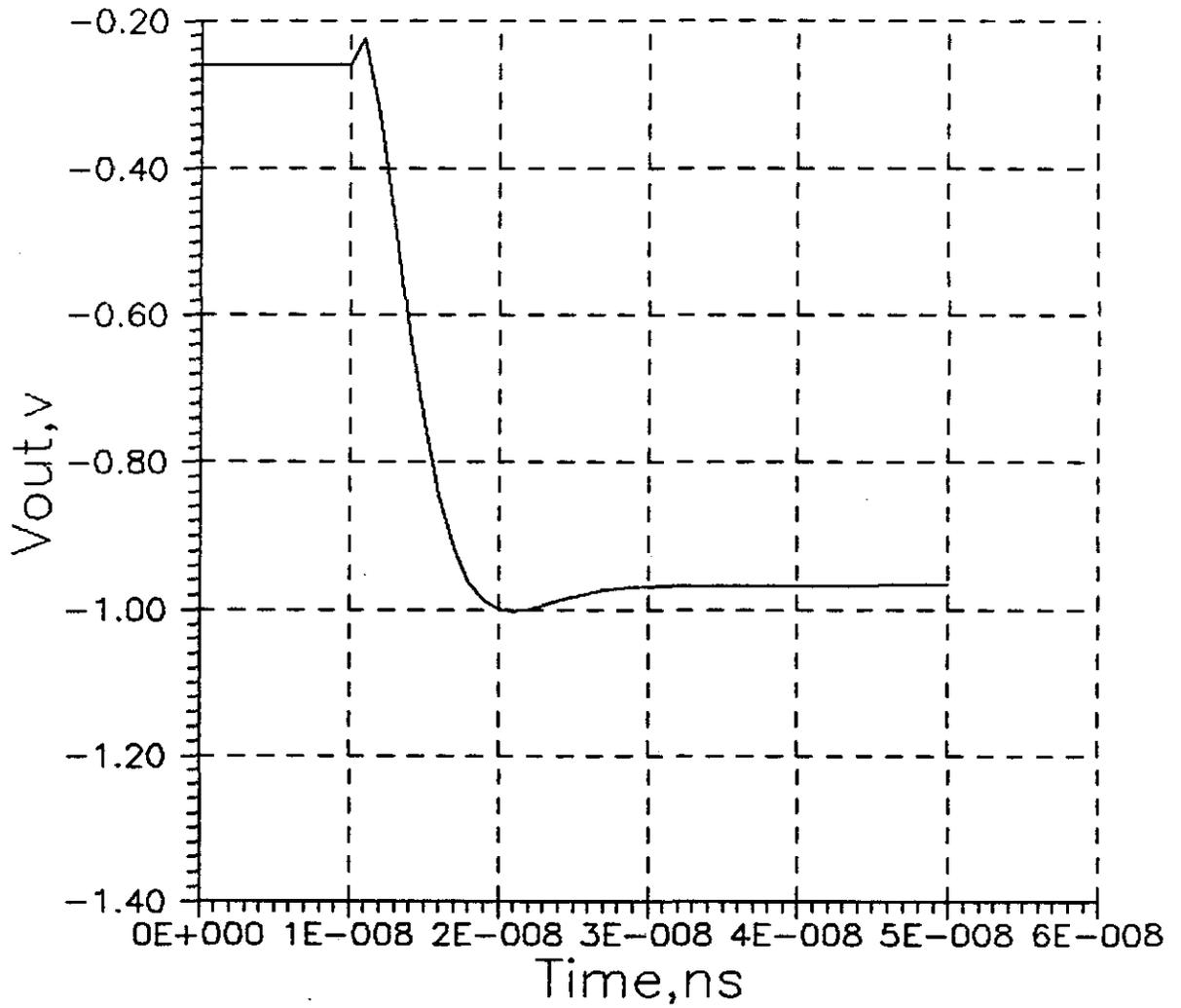


Fig.1.19. Channel 2. Preamplifier, response with $C_d=100\text{p}$, Risetime=16ns.

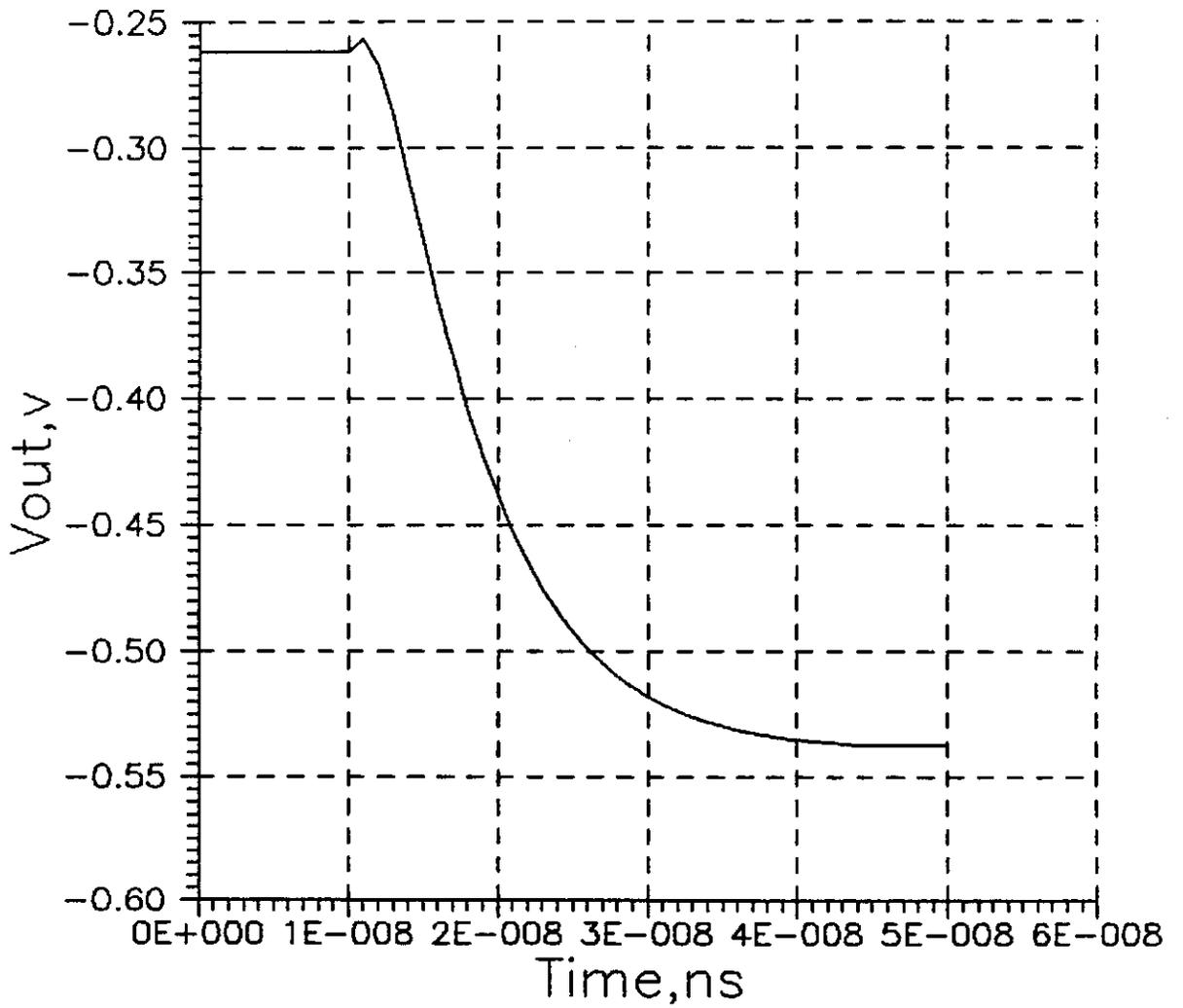


Fig.1.20. Channel 2. Response of the preamplifier, which is set the voltage gain mode, $V_{in}=-100\text{mV}$, $C_{fb}=0$, $C_{in}=0.068$, $\text{Gain}=28$, $\text{Risetime}=20\text{ns}$.

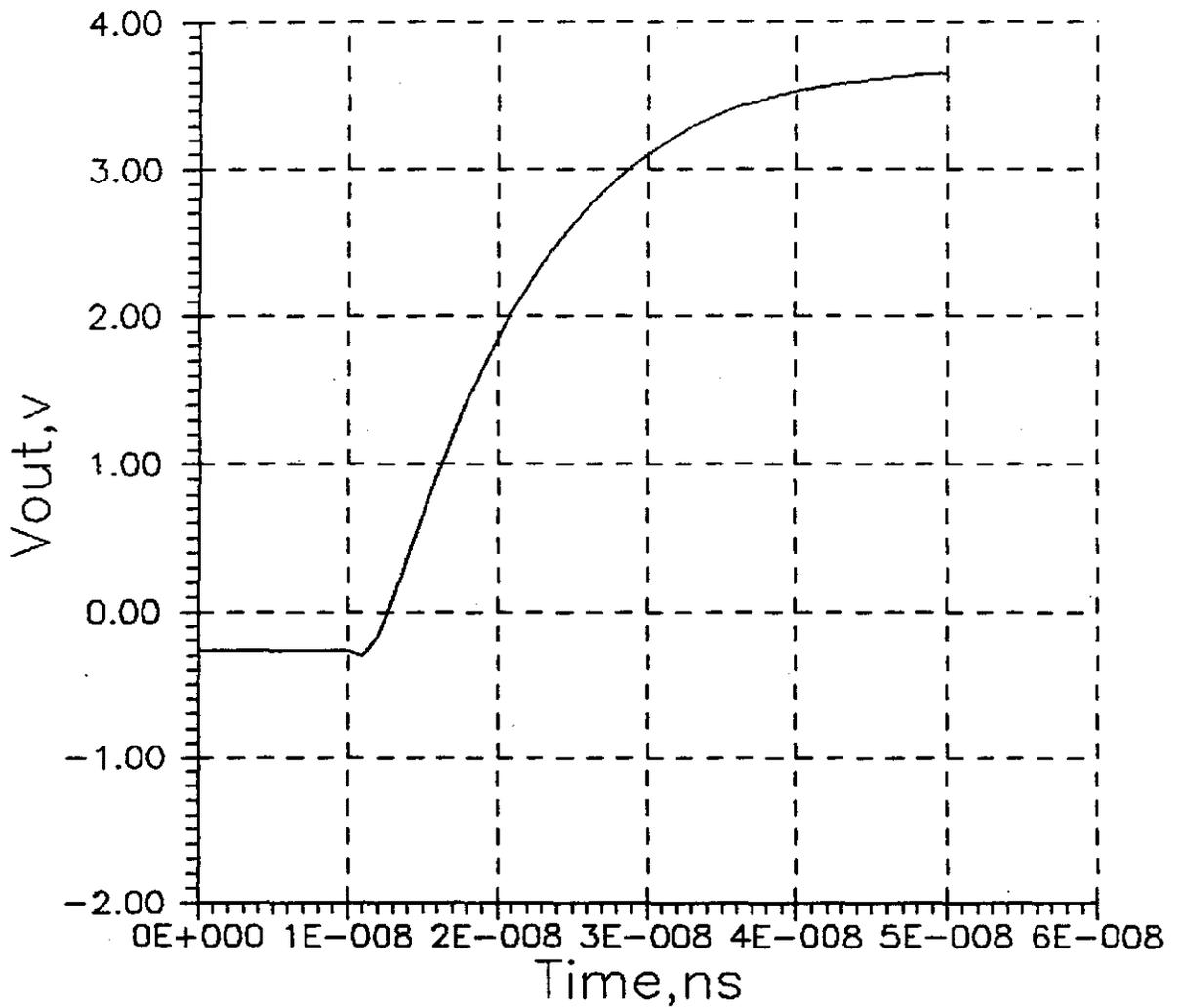
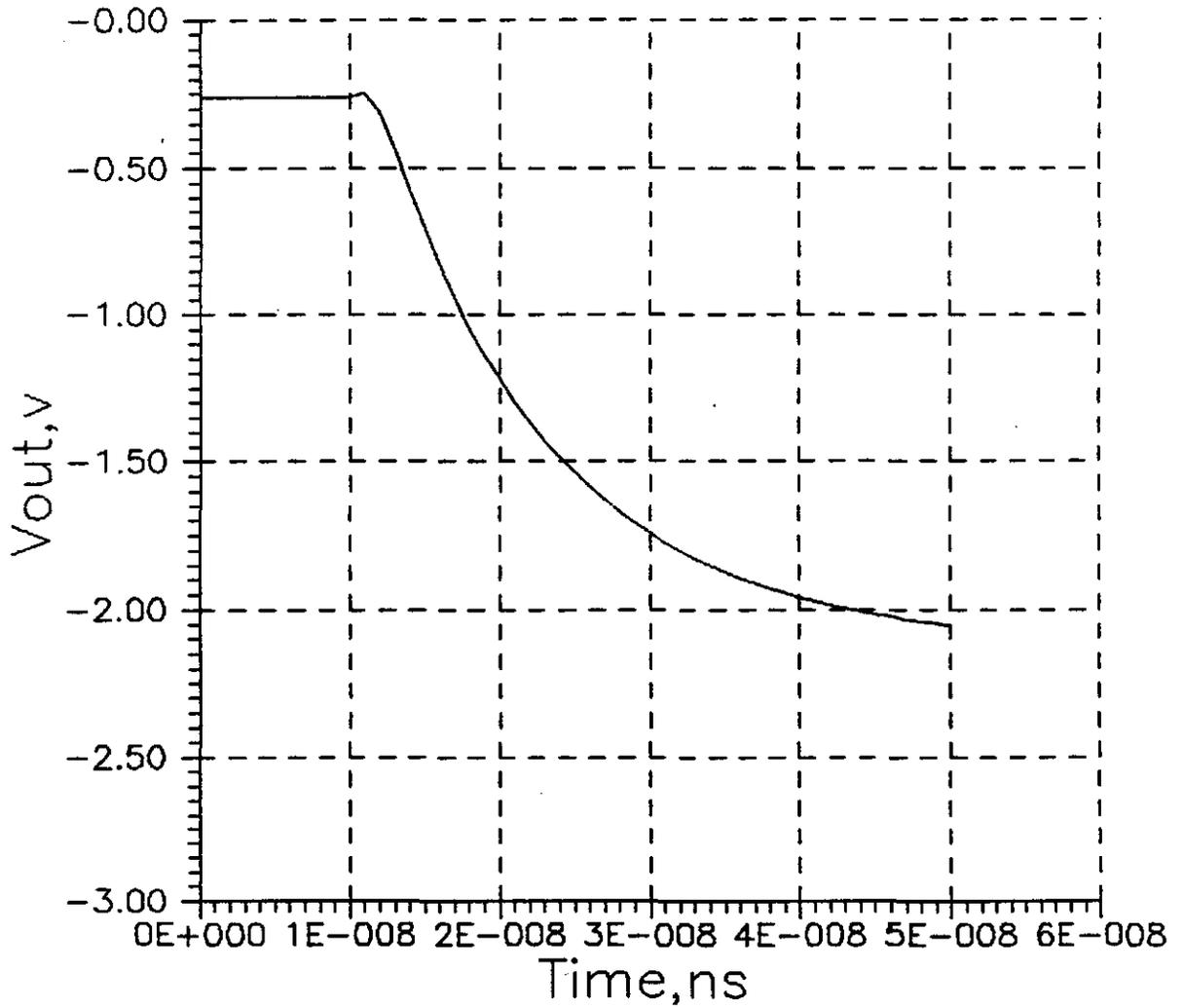


Fig.1.21. Channel 2. Response of the preamplifier, which is set the voltage gain mode, $V_{in}=40\text{mV}$, $C_{fb}=0$, $C_{in}=0.068$, $\text{Gain}=28$, $\text{Risetime}=20\text{ns}$.



2. PREAMPLIFIER/SHAPERS IC ELECTRONIC COMPONENT MEASUREMENTS

2.1. Purposes and content of the investigation

Two series of electronic component parameter measurements have been made to get their dependencies on BJT-JFET process parameters in operational current/voltage region, to be able to predict potential characteristics of CSP/shapers built with the technology and to modify the electronic component SPICE parameters used in the circuit computer modelling.

The first set of the component parameter measurements had been made preparatory to the first IC production iteration. For such a purpose a set of test structures (different types of a head bipolar transistor, minimal size BJT-transistors, JFETs and capacitances) has been made in a test array designed for another goals (hereinafter referred to as "the test array 1" (TA1)).

The second set of the measurements has been made for the test structures grown together with CSP/shapers circuits on the same die, subsequently referred to as "the test array 2" (TA2).

To investigate the noise parameters of CMOS digital technology available at "INTEGRAL" to estimate the possibility of its application to low noise amplifying devices production a set of MOSFETs has been made, their measurement results are reported there too.

2.2. On-wafer measurements

2.2.1. Wafers with TA1 structures

Two TA1 wafers labelled 1-6 and 1-7 have been subjected to investigation. The resistivities (a surface Rs) of the next layers have been measured:

- * TIP - surface resistivity of p- base
- * TIPK - resistivity of JFET's p channel
- * TIG - resistivity of a deep n+ collector
- * TIPSS - for p+ burried layer
- * TIHSS - for n+ burried layer
- * TIEP - for epi layer
- * TIE - for n+ emitter
- * TI2 - for pJFET's n- gate
- * TIPP - for p+ base.

In addition values of 40 Ohm, 1 k, 10k, 50k resistors were measured.

The die yield of TA1 is shown in Table 2.1.

Table 2.1

The die yield of the TA1 of investigated wafers

```

=====
Wafer : Packaged dies : Fuctionally operable dies
-----
1-6      40              5
1-7      50              28
=====

```

The main types of defects are the next:

a) for the wafer 1-6:

- * short-circuit between emitter and collector of head transistors;
- * no connection between Si and metal1 or between metal1 and metal2;

b) for the wafer 1-7:

- * the minimal size n-p-n emitter-base short-circuits;
- * very fast emitter/base junction degradation after reverse biasing.

Metal problems are explained mostly by temporary unsatisfactory work of the metallisation division.

2.2.2. TA2 wafer measurements

The number of TA2 wafers to be measured equals four: 1450-02, 1450-05, 1450-06 and 1450-09. Here we present results of measurements only for one wafer which has the largest breakdown voltages between all the TA1/TA2 wafers as the most interesting from the technology and circuitry point of view. Surface resistivities R_s of the process test structures, breakdown voltages of BJT junctions/JFET channels and values of all the operational resistors 10 Ohm, 0.6 k and so on to be used in circuits have been measured.

We would point out at the large departure of the base resistivity $R_s=812$ Ohm/sq. from the required value 550 Ohm/sq. This circumstance is supposed to magnify considerably the values of operational resistors at 45 - 70% and probably to increase a head n-p-n noise level. The relative operational resistors values disagreement appears to be explained by averaging of the resistor values being made during the measurements.

The TA2 wafer 1450-09 die yield equals 96%. There were 48 functionally operable dies among 50 packaged.

2.3. Packaged test structures

2.3.1. TA1 structures

As the two wafers have very similar R_s in all the formed layers, we have decided to wire devices from both wafers, moreover the wafer 1-6 have provided mainly JFETs. The packaged devices are listed in Table 2.2.

Table 2.2

TA1 packaged devices							
Pa- cka- ge	Pin numbers	Desig- nation	Design rule	Device description Emitter/gate strip number	Design h,um	Emitter/gate strip number	Comments
1	2	3	4	5	6	7	8
Wafer 1-7							
1	7	5	6	Q1	1.5	10	The head n-p-n transistors:
1	12	11	10	Q2	2.5	10	
1	14	15	13	Q3	1.5	3	
2	7	5	6	Q4	1.5	10	
2	12	11	10	Q5	2.5	10	

1	2	3	4	5	6	7	8
2	14	15	1	Q6	1.5	3	
3	7	5	6	Q7	1.5	10	
3	12	11	10	Q8	2.5	10	
3	14	15	13	Q9	1.5	3	
4	7	5	6	Q11	1.5	10	
4	12	11	10	Q12	2.5	10	
4	14	15	13	Q13	1.5	3	
5	12	11	10	Q14	1.5	10	Deep ring collector for collector resistance Rc lowering
5	16+	1-		C1	p-n junction capacitor Cp-n, S=120x120 sq.um		
5	9	8		C2	Metal-deep collector capacitor Cmos, supposed area S=350*400 um		
6	12	11	10	Q5	1.5	10	Head deep collector transistor
6	16	1		C3	Cp-n, area 120*120 sq.um		
6	9	8		C4	MOS capacitor(Cmos), 350*400 sq.um		
7	12	11	10	Q16	1.5	10	Head deep collector transistor
7	16	1		C5	Cp-n, S = 120*120 sq.um		
7	9	8		C6	Cmos, S = 350*400 sq.um		
11	7	5	6	Q20	1.5	1	Minimum size n-p-n, emitter 1.5*4.0 um
12	7	5	6	Q21	1.5	1	Minimum size n-p-n
13	7	5	6	Q22	1.5	1	Minimum size n-p-n
14	7	5	6	Q23	1.5	1	Minimum size n-p-n
1	2	3	4	5	6	7	8

Wafer 1-6

8	7	5	6	Q17	1.5	15	Head n-p-n transistor
8	1	2	8	J1	1.5	1	pJFET, width 20 um
8	15	16	9	J2	1.5	2	pJFET, width 30 um
8	14	13	12	J3	1.5		Two-gate pJFET, pin 14-upper gate, 12-down gate, 13-source
9	7	5	6	Q18	1.5	15	Head n-p-n transistor
9	1	2	8	J4	1.5	1	pJFET, width 20 um
9	15	16	9	J5	1.5	2	pJFET, width 30 um
9	14	13	12	J6	1.5		Two-gate pJFET
10	7	5	6	Q19	1.5	15	Head n-p-n transistor
10	1	2	8	J7	1.5	1	pJFET, width 20 um
10	15	16	9	J8	1.5	2	pJFET, width 30 um
10	14	13	12	J9	1.5		Two-gate pJFET

2.3.2. TA2 structures

The next TA2 electronic devices types were packaged:

- * a head n-p-n transistor having a design rule $h=1.5 \mu m$, a number of emitter strips $n=10$ and a structure with a deep ring collector (collector - pin 10, base - 11, emitter - 12)
- * pJFET with the two gates being connected (Version 1, source - 15, drain - 13, gate - 14)
- * pJFET with the two separate gates, an upper gate has a strip form like the Tektronix type JFET (Version 2, d-7, s-5, down gate - 8, upper gate - 6)
- * pJFET with the two separate gates, an upper gate has a ring form like the Analog Devices type JFET (Version 3, s-4, d-2, ug-3, dg-16).

The ring gate pJFET is supposed to possess the least possible flicker noise value, but it has very low yield now which is supposed to be explained by difficulties in making $1.5 \mu m$ gap in the tilted parts of the layout.

2.3.3. Test capacitance measurements (TA1 structures)

All the test capacitances C1 - C6 have been measured by impedance meter E7-12. Summary stray capacitance of a test socket and package was subtracted from the measured values. Contact pad stray capacitances were neglected since contact pad metal is deposited on a thick oxide insulating layer about $1.5 \mu m$. The dependence of the mean capacitance values on reverse bias voltage V_{rev} are shown in Table 2.3.

Table 2.3

Mean test capacitor values versus reverse bias voltage							
V rev, V:	0	1.0	2.0	3.0	4.0	5.0	10.0
Cp-n, pF:	3.78	2.76	2.36	2.12	1.96	1.83	0.71
Cmos, pF:	20.09	-	-	-	-	-	19.95

2.4. n-p-n transistor measurements

2.4.1. Static parameters of TA1 n-p-n test structures

To measure test n-p-n transistor static characteristic the transistors with breakdown voltage $V_{ce} > 8.0 V$ at $I_b = 0$ and leakage current $10 \mu A$ were selected. The measurements were made with transistor-and-diode tester I2-70. There are averaged junctions breakdown voltages shown in Table 2.4, where

V_{ce} - collector-emitter breakdown voltage with base being unconnected, $I_b = 0$;

V_{eb} - emitter-base breakdown voltage;

V_{bc} - collector-base breakdown voltage.

All the breakdown voltages were measured with a transistor-and-diode tester i2-56 at leakage current 10 uA. Averaged dependencies of static common-emitter current gain on $\langle h_{21E} \rangle$, typical individual h_{21E} and difference gain h_{21e} for the tested transistors are shown too, where

$$h_{21E} = \frac{I_c}{I_b} \Big|_{U_{ce}=\text{Const}}, \quad h_{21e} = \frac{dI_c}{dI_b} \Big|_{U_{ce}=\text{Const}}$$

Table 2.4

Static TA1 n-p-n characteristics

Sample	I_e , mA ---->															
	Operation		Breakdown		0.1	0.3	0.5	1.0	2.0	5.0	10	30	50			
	volt. /	h ₂₁	V _{eb}	V _{cb}												
	U _{cb} , V/	h ₂₁	V _{eb}	V _{cb}	V _{ce}											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		
Wafer 1-7																
Q6	3.0	$\langle h_{21E} \rangle$	5.8	20.0	11.5	258	255	247	238	221	171	132	69	51		
h=1.5um	1.0	h _{21E}				199	193	188	182	179	149	128	66	34		
	1.0	h _{21e}				185	184	178	168	153	124	98	29	15		
n=3	3.0	h _{21E}				219	215	207	194	177	140	109	48	20		
U _a =13.1V	3.0	h _{21e}				238	230	221	212	198	171	144	86	48		
Q4	3.0	$\langle h_{21E} \rangle$	5.8	19.0	11.7	215	228	228	229	224	201	167	107	84		
h=1.5um	1.0	h _{21E}				150	160	162	163	161	155	146	119	100		
n=10	1.0	h _{21e}				154	166	164	162	158	144	130	93	66		
U _a =14.5V	3.0	h _{21E}				169	184	185	187	187	177	167	136	116		
	3.0	h _{21e}				176	189	188	186	180	163	147	106	83		
Q14, n=10	3.0	$\langle h_{21E} \rangle$	5.8	19.5	11.5	265	261	255	239	221	180	146	102	81		
h=1.5um	1.0	h _{21E}				224	222	217	210	200	151	110	65	-		
U _a =9.9V*	1.0	h _{21e}				210	211	208	200	158	106	67	40	-		
Deep ring collector	3.0	h _{21E}				283	275	267	257	238	167	121	78	54		
	3.0	h _{21e}				262	260	255	241	178	158	114	48	30		
Q5	3.0	$\langle h_{21E} \rangle$	5.8	19.0	11.9	363	326	307	306	280	272	251	181	-		
h=2.5um	1.0	h _{21E}				244	227	220	213	203	190	151	137	120		
n=10	1.0	h _{21e}				209	212	208	202	196	175	146	109	95		
U _a =11.1V	3.0	h _{21E}				347	285	271	258	243	228	211	170	-		
	3.0	h _{21e}				257	256	248	240	224	205	183	133	111		
Wafer 1-6																
Q18	3.0	$\langle h_{21E} \rangle$	5.8	22.0	12.8	205	211	210	209	205	202	178	184	150		
h=1.5um	1.0	h _{21E}				183	186	185	183	181	171	164	135	116		
n=15	1.0	h _{21e}				180	186	184	181	177	161	150	109	80		
U _a =18.2V	3.0	h _{21E}				211	214	211	209	202	197	160	134	134		
	3.0	h _{21e}				206	212	211	205	198	190	128	126	100		

* U_a - Early's voltage
 $\langle h_{21E} \rangle$ - averaged value

2.4.2. Static parameters of TA2 test n-p-n transistors

The test n-p-n transistors were measured with the next testers:

- * TR-4805 (breakdown voltages V_{eb} , V_{cb} and V_{ce})
- * i2-70 (h_{21E} , h_{21e} , U_a)
- * i2-68 (F_t)
- * E7-12 (C_{cb} , C_{be} , C_{cs}).

The measurement results are shown in Tables 2.5 and 2.6.

Table 2.5.

Static TA2 test n-p-n characteristics ($h=1.5 \mu m$, $n=10$, ring deep collector)

Sample	I_e , mA --->					0.1	0.3	0.5	1.0	3.0	5.0	10	50
	Operation	Straw	capa-										
	volt. /--	citances,	pF										
	$U_{cb}, V/h_{21}/$	C_{cs}	C_{cb}	C_{be}									
1	2	3	4	5	6	7	8	9	10	11	12	13	15
N10	1.0	h_{21E}	2.37	2.04	1.45	102	104	103	102	88	78	53	24
$U_a = 16.63V$	3.0	h_{21E}				118	119	118	113	97	86	60	34
$V_{cb} = 24.0 V$	1.0	h_{21e}				100	103	102	92	74	54	33	15
$V_{be} = 5.9 V$	3.0	h_{21e}				115	118	117	102	80	64	36	20
$V_{ce} = 11.4 V$													
N16	1.0	h_{21E}	2.26	1.94	1.43	82	85	86	85	70	56	41	20
$V_{cb} = 24.5 V$	3.0	h_{21E}				86	92	92	91	74	60	49	24
$V_{be} = 6.0 V$	1.0	h_{21e}				87	89	86	80	56	36	21	11
$V_{ce} = 12.4 V$	3.0	h_{21e}				94	96	94	83	63	37	28	22
$U_a = 16.8 V$													
N14	1.0	h_{21E}	2.22	1.93	1.45	71	74	75	70	69	60	50	26
$U_a = 16.2 V$	3.0	h_{21E}				76	78	84	80	74	68	53	36
$V_{cb} = 19.0 V$	1.0	h_{21e}				74	76	83	80	57	43	32	16
$V_{be} = 6.0 V$	3.0	h_{21e}				78	82	86	91	70	45	36	24
$V_{ce} = 12.2 V$													
N20	1.0	h_{21E}	2.23	1.89	1.47	93	96	97	97	95	75	52	25
$U_a = 17.2 V$	3.0	h_{21E}				107	110	110	108	94	83	60	33
$V_{cb} = 21.0 V$	1.0	h_{21e}				98	98	97	90	72	52	36	14
$V_{be} = 6.0 V$	3.0	h_{21e}				106	110	111	100	78	64	38	32
$V_{ce} = 11.8 V$													

Table 2.6

TA2 test n-p-n transistor stray capacitances dependence on a reverse bias voltage

U_{rev}, V	0	1.0	3.0	5.0
C_{cb}, pF	1.93	1.53	1.24	1.13
C_{be}, pF	1.45	1.17	0.87	0.79
C_{cs}, pF	2.22	1.79	1.51	1.40

2.4.3. Ft measurements of TA1 structures

Unit gain frequency Ft was determined by measurements of /h21e/ at high frequencies Fm:

$$F_T = /h_{21e}/ * F_m$$

A transistor-and-diode tester I2-68 to be used for the measurements can measure /h21e/ <=32 at Fm = 100 kHz, i.e. we were able to measure Ft up to 3.2 GHz. Transistors with larger Ft up to 9.0 GHz should be packaged to four pin "helicopter-type" package. To test a large number of transistors with Ft < 3.2 GHz during this test we were forced to set our test devices to 16 pin micropackage HO1.16-1b. Contact adapter test sockets of used tester can measure the package of this type at frequency not more than 100 MHz.

The measurement results are shown in Table 2.7. It is seen that some n-p-n samples demonstrate Ft > 3.2 GHz, so at the next stages the Ft measurements are supposed to be made with adequate packaged devices.

It should be noted that the results have shown good repetitivity for the same device type from package to package. Ft dispersion appears to be less than 2%, which is no more than the measurement channel error of the testor itself.

Table 2.7

TA1 test n-p-n Ft estimates versus emitter current

Sample	Ie, mA	Ft, MHz									
		0.1	0.3	0.5	1	3	5	10	30	50	
Q6, h=1.5um, n=3	1.0	119	324	530	936	2430	>3200	>3200	1290	681	
	3.0	120	327	532	943	2490	>3200	>3200	2530	983	
Q4, h=1.5um, n=10	1.0	92	248	396	681	1600	2210	2290	>3200	3010	
	3.0	94	254	406	704	1690	2360	>3200	>3200	>3200	
Q5, h=2.5, n=10	1.0	89	249	404	698	1650	2260	3120	>3200	>3200	
	3.0	87	244	405	712	1740	2430	3180	>3200	>3200	
Q18, h=1.5, n=15	1.0	82	214	338	613	1280	1720	2280	2660	2210	
	3.0	83	222	352	603	1380	1890	2570	3170	3100	
Q14, ring deep c. h=1.5, n=10	1.0	97	264	429	748	1810	2510	>3200	3190	>3200	
	3.0	98	269	437	771	1910	2660	>3200	3190	>3200	

2.4.4. Ft measurements of TA2 n-p-n transistors
est n-p-n transistors noise measurements

TA2 test n-p-n transistors frequency measurements results are shown in Table 2.8.

Table 2.8

TA2 test n-p-n transistor Ft measurements results

Sample	Ic, mA	Ft, MHz							
		0.1	0.3	0.5	1	3	5	10	50
N10	3.0	265	423	724	1660	2240	2940	3000	
N16	3.0	266	427	733	1700	2320	3110	3200	
N14	3.0	262	422	721	1650	2250	2960	3130	
N20	3.0	265	425	728	1680	2270	3010	3080	

2.4.5. n-p-n transistors noise measurements

TA1/TA2 n-p-n transistors noise measurements results have been made in two steps. For the first of all the TA1 n-p-n transistors made with design rule $h = 1.5 \mu m$ and placed in packages N 16, 17, 18 (deep ring collector head transistor type with the number of emitter strips $n = 10$), 19 (pins 7-5-6), 20 (7-5-6), 21 (7-5-6), 22 (7.5.6), 27 (7-5-6) (head transistors with $n = 10$ but of usual construction) head transistors numbers 20, 22, 27 (14-15-13) and head transistors with $n = 3$. Samples N 19, 20, 21, 27 (all of them have pins 21-11-10) are build in 2.5 design rule. These results are shown in Table 2.9. The measurements were spent in the next conditions: $I_c = 0.01 \text{ mA}$, 0.1 mA , 1.0 mA , $U_{ce} = 3.0 \text{ V}$.

The second stage measurements were conducted with TA2 samples N 3 - 7, 13, 15, 18, 20. The measurement conditions are the next: $I_c = 3.0 \text{ mA}$, $U_{ce} = 3.0 \text{ V}$. An equivalent base circuitry resistance in a base region $R_{eq} = 52.5 \text{ Ohm}$. The results of these measurements are shown in Table 2.10.

Table 2.9

TA1 test n-p-n transistors noise measurements results

Sample	Ic, mA	En, nV/Hz ^{1/2}			Rbb', Ohm	
		10 Hz	25kHz	<h21e>		
1	2	3	4	5	6	7
N27, n=3, h=1.5 um, pins 14-15-13	1.00 0.10 0.01	14.34 31.66 27.70	0.60 1.83 4.82	210 230 210	<8.66	
N27, n=10, h=1.5 um, 7-5-6	1.00 0.10 0.01	17.77 17.35 31.50	0.53 1.59 2.18	190 170 150	<3.90	

1	2	3	4	5	6	7
N=22, n=3, h=1.5 um, 14-15-13	1.00 0.10 0.01	28.82 31.24 39.81	1.9 2.24 2.18	210 230 210	192.0	
N=22, n=10, h=1.5 7-5-6	1.00 0.10 0.01	<11.66 11.35 44.66	1.00 1.50 3.39	190 170 150	35.3	
N21, n=10, h=1.5 um, 7-5-6	1.00 0.10 0.01	11.0 18.83 22.38	0.71 1.59 4.82	190 170 150	5.4	
N20, n=3, h=1.5 um, 14-15-13	1.00 0.10 0.01	39.88 19.3 25.7	2.15 1.59 4.71	190 170 150	78.3	
N20, n=10, h=1.5 um, 7-5-6	1.00 0.10 0.01	39.88 19.30 25.70	2.15 1.59 4.71	190 170 150		
N19, n=10, h=1.5 um, 7-5-6	1.00 0.10 0.01	41.40 39.85	2.44 11.17	190 170		
N=27, n=10, h=2.5 um, 12-11-10	1.00 0.10 0.01	16.40 29.15 31.62	0.82 0.86 5.30	240 320 300	16.1	
N=21, n=10, h=2.5 12-11-10	1.00 0.10 0.01	44.13 19.93 39.80	0.67 1.50 3.59	240 320 300	2.1	
N20, n=10, h=2.5 um, 12-11-10	1.00 0.10 0.01	13.31 63.07 56.21	0.89 1.64 3.98	240 320 300	22.8	
N19, n=10, h=2.5 um, 12-11-10	1.00 0.10 0.01	29.16 38.90 31.60	1.02 1.45 -	240 320 300	37.8	
N=16, n=10, h=1.5 um, 12-11-10	1.00 0.10 0.01	125.89 63.09 100.00	1.08 2.39 8.55	250 270 240		Ring deep collector
N=17, n=10, h=1.5 12-11-10	1.00 0.10	25.11 28.16	1.42 3.91	250 270		Ring deep collector
N18, n=10, h=1.5 um, 12-11-10	1.00 0.10 0.01	19.95 34.48	1.10 4.69	250 270		Ring deep collector

Table 2.10

The second stage TA2 n-p-n noise measurements

Sample	f, kHz	En, nV/Hz ^{1/2}				
		0.01	0.1	1.0	10.0	25.0
3		31.57	2.04	1.46	0.65	0.74
4		56.23	2.32	1.50	0.89	0.74
5		48.96	4.41	1.40	1.11	0.74
6		40.73	1.96	1.31	0.74	0.58
7		48.41	4.54	2.40	1.03	0.74
13		28.18	1.72	1.59	0.91	0.67
15		66.06	2.73	1.06	0.83	0.62
18		63.10	2.26	1.29	0.92	0.90
20		50.11	2.46	1.52	0.65	0.65

2.5. JFET tests

2.5.1. TA1 JFETs

TA1 includes JFETs designed for cascode stages of the charge-sensitive preamps and the shapers with a bipolar head transistors. They possess too small capacitance values to make precise measurements with equipment to be available now (testers 12-56 and 12-46), so at the first stage we were forced to restrict our works by express analysis only. The results are presented in Tables 2.11 and 2.12.

Table 2.11

Mean value pJFET characteristics, measured with 12-56

Sample	* I _{init} , mA	U _{th} , V	S(U _g =0, dU=0.1V), mA/V	Breakdown voltage, V	V _{ds}	V _{gd}	V _{gs}
pJFET, l=20um, h=1.5, n=1	0.469	2.5V	0.262	31.7	32.0	33.0	
pJFET, l=30um, h=1.5, n=2	1.390	2.7	0.767	31.8	30.9	31.0	

* I_{init} = I_d
:U_{gs}=0, U_{ds}=U_{th}

Table 2.12

Mean value pJFET characteristics, measured with 12-56, E7-12

Sample, pJFET, h=1.5 um	U _{th} , V	I _{init} , mA	U _g =0 V	S, mA/V				C _{gs} , pF	C _{gsub} , pF
				0.5	1.0	1.5	2.0		
l=20um, n=1	2.65	0.44	0.17	0.15	0.12	0.095	0.06	1.2	1.52
l=30um, n=2	2.60	1.23	0.60	0.65	0.47	0.38	0.27	1.0	1.18

2.5.2. TA2 test JFET static characteristics measurements

pJFET static characteristics, namely the dependences of a drain current I_d on a gate-source voltage U_{gs} at a fixed drain-source voltage $U_{ds} = 3$ V, were determined by a tester TR-4805, and in the process a down gate of Versin 2/3 pJFET was biased by a constant reversed voltage $U_{bg} = 0, 1.0, 2.0, 3.0$ V, taken from an external voltage supply. An output difference resistance and parameter L^{-1} ($1/\lambda$) were determined by TR-4805 too. Junction capacitances were measured by E7-12.

Current-voltage characteristics are assumed to satisfy the next equation:

$$I_c = B(1 + LU_{ds})(U_{th} - U_{gs})^2 \quad (2.1)$$

$$\text{at } U_{ds} > U_{th} - U_{gs} \quad (2.2)$$

To get the model parameter B from eq. (2.1) we should neglect L and fix $U_{gs} = 0$. Then we have

$$B1 = \frac{I_d}{U_{th}^2}; U_{gs}=0 \quad (2.3)$$

B1 estimate precision is seen from (2.3) to be determined by I_d and U_{th} measurement accuracy with the latter having the greatest error being measured any one of testers i2-56, Aëö&-1 or TR-4805. So B may be calculated from the next equation:

$$B2 = \left[\frac{(I_d2)^{1/2} - (I_d1)^{1/2}}{U_{gs2} - U_{gs1}} \right]^{1/2} \quad (2.4)$$

at $U_{ds} = \text{Const} = 3.0$ V,

where I_{d2}, I_{d1} - drain currents at voltages U_{gs1} and U_{gs2} respectively and at fixed U_{ds} .

With known B2 we can calculate U_{th}

$$U_{th} = U_{gs1} + (I_{d1}/B2)^{1/2}, \quad (2.5)$$

where I_{d1} - drain current at U_{gs1} and fixed $U_{ds} = \text{Const} = 3.0$ V, and pJFET transconductance in its dependence on the drain current

$$S = \frac{dI_d}{dU_{gs}} = 2(B2 \cdot I_d)^{1/2} \quad (2.6)$$

The pJFET unit gain frequency is determined to be

$$F_t = S/2\pi C_{sum}, \quad (2.7)$$

where C_{sum} - the total capacitance connected to the gate,
 $\pi = 3.14$.

For version 1 pJFET we have

$$F_t = S/2\pi(C_{gsb} + C_{gs}). \quad (2.8)$$

The versions 2, 3 unit gain frequency equals

$$F_t = S/2\pi C_{gs} \quad (2.9)$$

Measured and calculated according eq. 2.3 - 2.9 parameters are shown in Tables 2.13, 2.14.

Table 2.13
TA2 test pJFET static characteristics measurement results

Sample: N, pins	Udngs: V	Id(Uds=3.0), mA			Uth: V	L^-1: V	B1, /V^2	B2, /V^2	S(Uds=3.0V) mA/V			
		Ugs=0 V	Ugs=0.5V	Ugs=1.0V					0.2 mA	1.0 mA	max.	
	1	2	3	4	5	6	7	8	9	10	11	12
Version 1 pJFETs												
N17, 15-14-13		15.0	10.1	5.8	2.5	24.3	2.400	2.14	1.31	2.93	11.33	
N6, 15-14-13		15.0	10.1	6.0	2.5	23.3	2.400	2.14	1.31	2.93	11.33	
N10, 15-14-13		16.9	11.2	6.7	2.5	22.9	2.704	2.28	1.35	3.01	14.40	
N4, 15-14-13		17.1	11.8	7.1	2.5	23.1	2.736	2.09	1.29	2.89	11.96	
N3, 15-14-13		19.3	13.5	8.4	2.6	19.1	2.855	2.24	1.34	2.99	13.15	
N19, 15-14-13		18.9	13.3	8.3	2.6	20.5	2.800	2.15	1.31	2.91	11.32	
Version 2 pJFETs												
N19, 5-6-7	0.0	9.0	7.5	6.2	5.5	30.0	0.297	0.26	0.45	1.02	3.06	
	1.0	7.2	5.8	4.3	4.1			0.37	0.54	1.22	3.29	
	2.0	5.4	4.0	2.7	3.3			0.46	0.60	1.36	3.16	
	3.0	3.8	2.5	1.4	2.3			0.59	0.68	1.53	3.00	
N1, 5-6-7-8	0.0	7.5	6.1	4.9	5.0	30.0	0.300	0.27	0.47	1.05	2.89	
	1.0	5.7	4.4	3.2	3.3			0.35	0.53	1.20	2.85	
	2.0	4.2	2.9	1.8	2.6			0.50	0.63	1.41	2.89	
	3.0	2.8	1.7	0.7	2.0			0.70	0.75	1.67	2.80	
N2, 5-6-7-8	0.0	7.4	6.2	5.0	4.8	29.6	0.328	0.23	0.43	0.96	2.62	
	1.0	5.8	4.4	3.2	3.3			0.35	0.53	1.18	2.83	
	2.0	4.3	3.0	1.9	2.5			0.48	0.62	1.39	2.88	
	3.0	3.0	1.7	0.8	2.0			0.70	0.74	1.68	2.90	
N8, 5-6-7-8	0.0	8.0	6.7	5.4	5.0	26.7	0.320	0.27	0.47	1.05	2.89	
	1.0	6.4	5.0	3.7	3.8			0.37	0.55	1.22	3.09	
	2.0	4.7	3.4	2.2	2.8			0.47	0.62	1.38	2.98	
	3.0	3.4	2.0	1.1	2.2			0.63	0.71	1.59	2.93	
Version 3 pJFET												
N3, 2-3-4-16	0.0	9.0	7.6	6.3	5.5	25.7	0.298	0.24	0.44	0.98	2.93	
	1.0	7.4	5.7	4.4	4.1			0.39	0.56	1.24	3.38	
	2.0	5.5	4.1	2.8	3.3			0.46	0.60	1.35	3.16	
	3.0	4.0	2.6	1.4	2.5			0.57	0.73	1.64	3.27	
N18, 2-3-4-16	0.0	7.4	6.1	4.9	5.0	29.6	0.296	0.26	0.46	1.02	2.77	
	1.0	5.8	4.4	3.2	3.8			0.38	0.55	1.24	2.98	
	2.0	4.2	2.9	1.8	2.6			0.50	0.63	1.42	2.91	
	3.0	2.8	1.6	0.7								
N4, 2-3-4-16	0.0	8.0	6.6	5.3	5.0	29.1	0.320	0.28	0.47	1.06	2.99	
	1.0	6.3	5.0	3.7	3.8			0.35	0.53	1.18	2.96	
	2.0	4.8	3.3	2.1	2.8			0.55	0.66	1.48	3.24	
	3.0	3.3	2.0	1.0	2.0			0.67	0.73	1.63	2.97	

Table 2.14

TA2 test pJFET unit gain frequency measurement results

Sample	Udgs V	<Cgs> pF	<Cgd> pF	<Cgsb> pF	Uth V	Uth,V ?	Ft calculated MHz
1	2	3	4	5	6	7	8
Version 1 pJFETs							
17, 15-14-13		9.27	9.20	5.78	2.5	2.65	120
6, 15-14-13					2.5	2.65	120
10, 15-14-13					2.5	2.72	152
4, 15-14-13					2.5	2.86	127
3, 15-14-13					2.6	2.93	139
14, 15-14-13					2.6	2.96	120
Version 2 pJFETs							
19, 5-6-7-8	0.0	3.12	3.10		5.5	5.88	157
8	1.0				4.1	4.38	
	2.0				3.3	3.41	
	3.0				2.3	2.53	
N1, 5-6-7-8	0.0				5.0	2.58	147
	1.0				3.3	3.99	
	2.0				2.6	2.90	
	3.0				2.0	2.00	
N2, 5-6-7-8	0.0	3.12	3.10		4.8	5.66	133
	1.0				3.3	4.09	
	2.0				2.5	2.99	
	3.0				2.0	2.07	
N8, 5-6-7-8	0.0				5.0	5.57	146
	1.0				3.8	4.15	
	2.0				2.8	3.15	
	3.0				2.2	2.32	
Version 3 pJFET							
N3, 2-3-4-16	0.0	3.49	3.55		5.5	6.12	137
	1.0				4.1	4.38	
	2.0				3.3	3.47	
	3.0				2.5	2.44	
N18, 2-3-4-16	0.0				5.0	5.33	126
	1.0				3.8	3.89	
	2.0				2.6	2.89	
	3.0						
N4, 2-3-4-16	0.0				5.0	5.33	136
	1.0				3.8	4.25	
	2.0				2.8	2.95	
	3.0				2.0	2.22	

2.5.3. TA2 test JFET noise measurements

Noise levels were measured for all the three versions of the TA2 test JFETs. The results are shown in tables 2.15 - 2.17.

Table 2.15.
Connected gate (Version 1) pJFET noise ($U_{ds} = 3.0$ V)

Version 1 samples	f, kHz	En, nV/Hz ^{1/2}				
		0.01	0.1	1.0	10.0	25.0
	Id, mA					
3	19.3	31.15	15.84	4.46	1.99	1.99
4	17.1	29.17	8.51	2.31	1.75	1.60
5	17.4	46.77	16.40	3.75	1.77	1.75
6	15.0	35.48	15.84	7.07	3.16	3.16
7	17.3	32.73	7.41	3.31	1.99	1.99
10	16.9	46.77	10.47	3.93	1.84	1.84
13	16.2	30.01	16.78	5.75	3.31	2.69
15	17.9	27.22	7.94	3.63	2.37	1.99
16	18.0	46.77	10.23	2.29	2.11	1.54
Gate biasing circuit spectral density (calculated), nV/Hz ^{1/2}						1.33

Table 2.16.
Double-gate (Version 2) pJFET noise ($U_{ds} = 3.0$ V)

Version 1 samples	Down gate v, U _{dgs} , V	f, kHz	En, nV/Hz ^{1/2}				
			0.01	0.1	1.0	10.0	25.0
		Id, mA					
4	0.0	7.6	72.28	20.18	6.91	4.16	3.31
	2.0	4.4	56.23	15.48	5.82	2.63	2.63
5	0.0	8.5	89.12	27.86	8.70	4.37	4.07
	2.0	5.0	75.85	14.79	6.09	3.98	2.16
10	0.0	7.8	47.31	29.17	8.22	3.71	3.63
	2.0	4.6	56.67	28.91	9.66	5.24	5.62
16	0.0	7.6	79.43	24.26	10.11	6.53	4.62
	2.0	4.4	65.00	20.65	10.00	4.73	4.46
Gate biasing circuit spectral density (calculated), nV/Hz ^{1/2}						1.91	
it spectral density (calculated), nV/Hz ^{1/2}						1.57	

Table 2.17.

Double-gate (Version 3) pJFET noise (U _{ds} = 3.0 V)								
Version 1 samples	Down gate v, U _{dgs} , V	I _d , mA	E _n , nV/Hz ^{1/2}					
			f, kHz	0.01	0.1	1.0	10.0	25.0
4	0.0	8.0	88.10	19.72	6.76	3.98	3.50	
	2.0	4.7	31.26	11.61	3.07	3.08	3.12	
5	0.0	8.5	86.09	23.17	9.88	3.31	3.05	
	2.0	5.0	26.91	11.22	3.54	2.63	2.37	
10	0.0	8.0	74.13	19.95	5.12	3.75	3.23	
	2.0	4.7	23.44	13.33	2.88	2.48	2.48	
16	0.0	8.2	69.18	19.05	8.51	3.71	3.30	
	2.0	4.7	34.27	14.45	5.43	4.07	2.78	
Gate biasing circuit spectral density (calculated), nV/Hz ^{1/2}		0.0						2.44
		2.0						1.57

2.5.4. TA1/TA2 pJFET constructions comparison

To compare the different type pJFETs to have been made on TA1 and TA2 the corresponding measurements results are given in Table 2.18 together with the supposed values.

Table 2.18

TA1/TA2 pJFET constructions comparison						
	Low power pJFET			Powerful pJFETs		
	I _{ds} , mA	S, mA/V	U _{th} , V	I _{ds} , mA	S, mA/V	U _{th} , V
Desired	1.4	0.95-1.2	2-3	14	9.0-10.0	2-3
TA1	1.39	0.767	2.7	-	-	-
TA2	2.4	1.4	2.5	15-19	11-13	2.5-2.6

2.6. Discussion of results

2.6.1. Both n-p-n and pJFET head element transistor constructions to be designed with the combined BJT-JFET technology meet the design requirements but without the necessary technology reserves (10 - 15)%.

2.6.2. The TA2 head BJT has the same frequency characteristics as the TA1 one has also the technological process to be used for TA2 production should provide F_t by 16% less.

2.6.3. The powerful pJFETs appear to permit to measure Ft more precisely. The connected-gates construction possess Ft = 120 - 150 MHz compared to 35 MHz for the low power TA1 pJFETs.

2.6.4. All the TA2 resistors have too large values on the average about 60% above the desired values.

2.6.5. The ring gate pJFET construction is found to have low yield.

2.6.6. The most promising results happen to belong to the double-gate pJFETs being controlled by the upper gate and with the drain current set by the down gate. In this case it is possible to keep the maximum trans-conductance and hence Ft practically constant whereas the drain current decrease can be rather significant. For example, look at the next table.

Table 2.19

The double-gate pJFETs parameters at different Id

	Version 1	Version 1	Version 2	Version 3
<Id>, mA	3.0	4.0	3.25	4.37
<Smax>, mA/V	5.90	5.90	2.91	3.14
<Ft>, MHz	62	62	149	143

2.7. About an opportunity of using of CMOS technology, available in Minsk, for CSP/shaper tasks

2.7.1. Test MOSFET structures

We have made an attempt to answer the question, did the digital CMOS technology, available in Minsk, provide the noise requirements to be need for CSC preamplifier. For such a purpose a set of test MOSFETs have been produced. There are n- and p-type transistors of different channel length L (design rule) and width W. The maximum test MOSFET channel width equals 2240 um with L = 1.8 um to be comparable with those of AMPLEX CSP (W/L = 3000/3 for the CSP POTA and 2000/3 for shaper NOTA). The test MOSFET structures are shown in Table 2.20.

Table 2.20

Test MOSFET structures

Type of MOSFET	n	p	n	p	n	p	n	p
Channel length L, um	1.4	1.8	1.4	1.8	5.0	5.0	50	50
Channel width W, um	1120	2240	80	160	80	160	80	60

Test MOSFET structure wafer consisted of 16 die modules to be placed and labelled in accordance with Table 2.21.

Dies' placing and marking in the test wafer module

AC 157	AC 158	G 157	AC 158
AC 04	14	AC 34	8
AC 257	AC 258	AC 257	TM
AC 86	12	AC 86	10

Modules 14, 8 and TM were packaged and wired like shown in Table 2.22.

Table 2.22

Test MOSFET structure wiring and marking

Package number	Pin No d	g	s	sb	Wafer number	Module number	Cond. type	W/L
1-10	2	5	7		09	8	p	60/50
11-20	2	5	7		09	8	p	160/1.8
11-20	10	13	15		09	8	p	160/5.0
31-40	2	5	7	8	09	14	n	80/50
41-50	2	5	7	8	09	14	n	80/1.4
51-60	2	5	7		09	TM	p	2240/1.8
51-60	10	13	15		09	TM	n	1120/1.4
71-80	2	5	7	8	20-08	14	n	80/1.4
81-90	2	5	7		20-08	8	p	60/50
91-100	2	5	7		20-08	8	p	160/1.8
101-110	2	5	7		20-08	TM	p	2240/1.8
61-70	2	5	7	8	20-08	14	n	80/50
71-80	10	13	15	8	20-08	14	n	80/5.0
91-100	10	13	15		20-08	8	p	160/5.0
101-110	10	13	15		20-08	TM	n	1120/1.4

2.7.2. MOSFET static parameter measurements

Static MOSFET parameters measurements were performed with use of a tester I2-56 at bias/supply voltages shown in Fig.2.1.

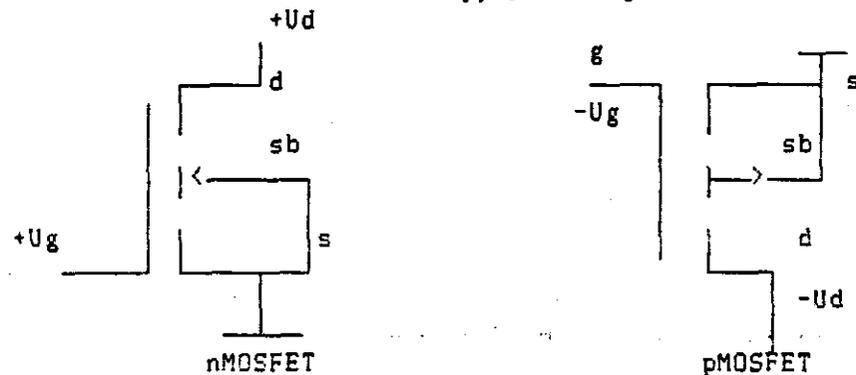


Fig.2.1. MOSFET bias/supply voltages used during the test

The next characteristics were measured:
a common-source drain MOSFET characteristic (Fig. 2.2a.)

$$I_d = f(U_{ds}) \quad (2.10)$$

$$U_{gs} = 2.0, 2.5, 3.0 \text{ V}$$

and a transfer MOSFET characteristic (Fig. 2.2b)

$$I_d = f(U_{sd}) \quad (2.11)$$

$$U_{dg} = 0$$

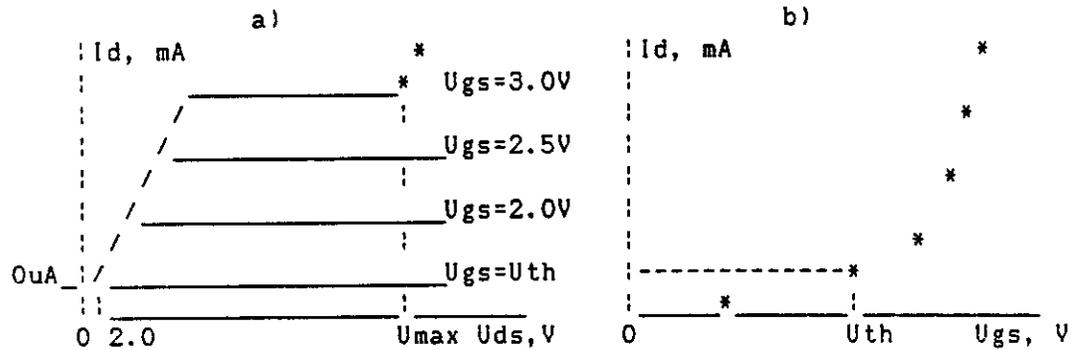


Fig.2.2. Drain (a) and transfer (b) MOSFET characteristics, measured during the test

The characteristics were used to determine the next MOSFET parameters:

- a threshold voltage U_{th} from Fig.2.2b as

$$U_{th} = U_{gs} \quad ; I_d = 10 \mu\text{A}, U_{dg} = 0 \text{ V}$$

or from Fig.2.2a as

$$U_{th} = U_{gs} \quad ; I_d = 10 \mu\text{A}, U_{ds} = 2.0 \text{ V}$$

- maximum drain-source voltage at which the drain current begin to rise sharply along the curve of $U_{gs} = 3.0 \text{ V}$ (see Fig.2.2a). The results of the measurements are listed in Table 2.23.

Table 2.23

MOSFET static characteristic measurements results

Sample, pins, type, size	$I_d(U_{ds}=2.0\text{V}), \text{ mA}$			L^{-1} V	$I_d(U_{gd}=0.0\text{V}), \text{ mA}$			$U_{th}, \text{ V}$	U_{ds} at $I_d = 10 \mu\text{A}$	U_{ds} max,
	$U_{gs} = 2.0\text{V}$	$U_{gs} = 2.5\text{V}$	$U_{gs} = 3.0\text{V}$		$U_{gs} = 2.0\text{V}$	$U_{gs} = 2.5\text{V}$	$U_{gs} = 3.0\text{V}$			
	2	3	4	5	6	7	8	9	10	
N2, p, 2-5-7, 60/50	0.017	0.042	0.075		0.030	0.07	0.12	1.70	10	
N3, p, 2-5-7, 60/50	0.034	0.064	0.112		0.054	0.10	0.16	1.30	10	
N81, p, 2-5-7, 60/50	0.017	0.041	0.074		0.034	0.07	0.12	1.70	10	

	1	2	3	4	5	6	7	8	9	10
N82, 2-5-7, p, 60/50		0.034	0.066	0.112		0.058	0.10	0.16	1.25	10
N15, 2-5-7, p, 160/1.8		0.90	1.9	3.0	9.0	1.8	3.5	5.7	1.05	10
N16, 2-5-7, p, 160/1.8		0.90	1.8	3.0	9.0	1.8	3.5	5.7	1.10	10
N97, 2-5-7, p, 160/1.8		2.2	3.5	4.9	8.6	3.8	6.7	9.5	0.75	9
N95, 2-5-7, p, 160/1.8		1.8	3.2	4.5	7.5	3.2	5.8	8.8	0.8	9
N95, 10-13-15, p, 160/5.0		0.42	0.84	1.34	44.7	0.65	1.35	2.0	0.9	9
N97, 10-13-15, p, 160/5.0		0.40	0.78	1.18	39.3	0.7	1.25	2.0	0.9	9
N74, 10-13-15, n, 80/5.0		0.95	2.05	3.50	21.0	1.5	3.0	5.0	1.0	6
N73, 10-13-15, n, 80/5.0		0.90	2.00	3.90	39.0	1.5	3.1	5.2	1.1	6
N45, 10-13-15, n, 80/5.0		0.80	1.75	3.50	46.7	1.2	2.6	4.5	1.1	6
N43, 10-13-15, n, 80/5.0		0.75	1.60	2.70	40.5	1.2	2.5	4.3	1.05	6
N103, 10-13-15, n, 1120/1.4	24	48	76	19.0	40	50	110	0.8	5	
N107, 10-13-15, n, 1120/1.4	22	46	73	24.3	32	64	100	0.8	5	
N51, 10-13-15, n, 1120/1.4	20	42	67	22.3	30	58	90	0.8	5	
N55, 10-13-15, n, 1120/1.4	18.5	40	65	32.5	30	58	90	0.8	5	
N15, 10-13-15, p, 160/5.0	0.22	0.52	0.92	46.0	0.4	0.9	1.4	1.2	9	
N11, 10-13-15, p, 160/5.0	0.20	0.50	0.90	45.0	0.4	0.8	1.4	1.2	9	
N51, 2-5-7, p, 2240/1.8	34	58	84	12.6	54	86	124	0.7	8	
N55, 2-5-7, p, 2240/1.8	21	42	67	13.4	50	83	120	0.8	8	
N102, 2-5-7, p, 2240/1.8	21	47	87	10.9	50	88	130	0.8	8	
N103, 2-5-7, p, 2240/1.8	44	72	104	9.4	80	100	130	0.6	8	
N107, 2-5-7, p, 2240/1.8	34	63	94	10.1	68	104	144	0.75	8	
N63, 2-5-7, n, 80/50	0.026	0.068	0.128	192	0.050	0.12	0.220	1.4	6	
N64, 2-5-7, n, 80/50	0.028	0.072	0.134	167.5	0.050	0.125	0.225	1.4	6	
N65, 2-5-7, n, 80/50	0.029	0.070	0.127		0.050	0.120	0.330	1.5	5	
N34, 2-5-7, n, 80/50	0.024	0.052	0.077		0.100	0.190	0.325	1.2	6.5	

	1	2	3	4	5	6	7	8	9	10
N36,	2-5-7,									
n,	80/50	0.024	0.056	0.085		0.100	0.200	0.325	1.4	6.5
N43,	2-5-7,									
n,	80/1.4	1.2	2.5	4.15	27.0	1.8	3.7	6.2	1.0	6
N45,	2-5-7,									
n,	80/1.4	1.2	2.6	4.35	26.1	2.0	4.0	6.5	1.1	6
N73,	2-5-7,									
n,	80/1.4	1.2	2.25	3.35	27.9	2.4	4.6	7.3	1.0	6
N74,	2-5-7,									
n,	80/1.4	1.5	3.15	5.0	25.0	2.3	4.6	7.3	1.0	6

It is known that the MOSFET Volt-Ampere characteristic in a large output difference-resistance region is described by the next equation:

$$I_d = B(1 + LU_{ds})(U_{gs} - U_{th*})^2, \quad (2.12)$$

at

$$U_{ds} > U_{gs} - U_{th*} \quad (2.13)$$

Eq. (2.12) is used to simulate MOSFET with PSpice. By assuming that $U_{ds} = \text{Const}$ one obtains PSpice model parameters

$$B = \left[\frac{(I_{d2})^{1/2} - (I_{d1})^{1/2}}{U_{gs2} - U_{gs1}} \right]^2 \quad (2.14)$$

$$U_{th*} = U_{gs} - (I_{d1}/B)^{1/2} \quad (2.15)$$

$$S = 2(BI_d)^{1/2}, \quad (2.16)$$

where I_{d1} , I_{d2} - the MOSFET drain currents at U_{gs1} , $U_{gs2} > U_{th*}$ and $U_{ds} = \text{Const} > U_{gs} - U_{th*}$ (for example, at $U_{ds} = 2.0$ V) respectively,

$$S = \frac{dI_d}{dU_{gs}|_{U_{ds}=\text{Const}}} \quad - \text{MOSFET transconductance, which depends on the drain current.}$$

on the drain current.

The parameter L can be calculated from eq. 2.12 taking into account the condition $U_{gs} = \text{Const}$:

$$L = \frac{I_{d2} - I_{d1}}{(U_{ds2} - U_{ds1})I_{d1}}, \quad (2.17)$$

where I_{d2} , I_{d1} - MOSFET drain currents at $U_{gs} > U_{th*}$, $U_{gs} = \text{Const}$ and U_{ds1} , $U_{ds2} > U_{gs} - U_{th}$.

The values of B , U_{th*} , S and L^{-1} calculated from the measurement data, are listed in Table 2.23 too.

2.7.3. MOSFET noise measurements

MOSFET noise spectral density E_n was measured in frequency points $f = 10\text{Hz}, 100\text{ Hz}, 1\text{ kHz}, 10\text{ kHz}$ and 25 kHz . It is believed to be the most informative noise characteristic because its using gives the possibility to calculate r.m.s. noise voltage U_n in a frequency band $f_1 - f_2$

$$U_n = \left[\int_{f_1}^{f_2} (E_n)^2 df \right]^{1/2} \quad (2.18)$$

The dimension of E_n is $V/\text{Hz}^{1/2}$.

The noise spectral density measurements were performed according the block-circuit shown in Fig.2.2.

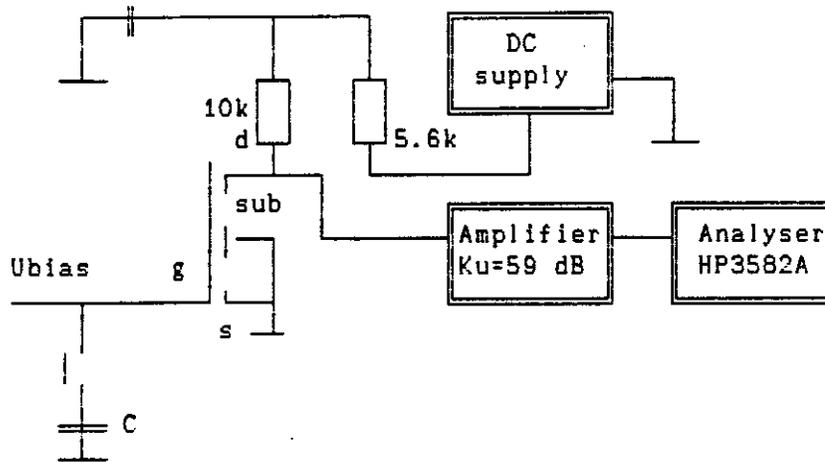


Fig. 2.2. Block-circuit of the noise measurement bench

To measure noise the next experimental procedures were used:
 2.7.3.1. The MOSFET voltage gain K_u is determined for given frequency region $f_2 - f_1$.

2.7.3.2. An output noise voltage U_{nos} at frequency f is measured provided that the MOSFET input is shorted out. Then

$$E_n = \frac{U_{nos}}{K_u(f_2 - f_1)^{1/2}}, \quad (2.19)$$

where $f_2 - f_1$ is a spectral analyser bandwidth for Hewlett-Packard device HP3582A at the measurement frequency.

To provide the AC short-circuit regime at the input the impedance of the input capacitor should be extremely low, i.e. the value of its capacitance should be very large.

The noise spectral density results estimated with eq. (2.15) are listed in Table 2.24.

Table 2.24

The MOSFET test structures noise measurements results

Sample, pins		B, mA/V ²	U _{th} * eq.	S, mA/V	E _n , nV/Hz ^{1/2} at I _d = 0.2 mA				
type, size			(2.15) I _d = 0.2 mA	I _d = 1 mA	0.01 kHz	0.1 kHz	1.0 kHz	10.0 kHz	25.0 kHz
1	2	3	4	5	6	7	8	9	10
N2, 2-5-7									
p, 60/50	0.0206	1.09	0.128	-					
N3, 2-5-7									
p, 60/50	0.0226	0.77	0.135	-					
N81, 2-5-7									
p, 60/50	0.0201	1.08	0.127	-					
N82, 2-5-7									
p, 60/50	0.0226	1.08	0.134	-					
N15, 2-5-7									
p, 160/1.8	0.613	0.79	0.700	1.57	1259	354	100	25.1	15.9
N16, 2-5-7									
p, 160/1.8	0.613	0.79	0.700	1.57	794	224	100	22.4	17.8
N97, 2-5-7									
p, 160/1.8	0.560	0.02*	0.657	1.45	1122	398	100	31.6	22.1
N95, 2-5-7									
p, 160/1.8	0.606	0.28*	0.698	1.56	1000	447	112	37.6	22.4
N95, 10-13-15									
p, 160/5.0	0.260	0.73	0.458	1.02	501	200	71	22.4	14.1
N97, 10-13-15									
p, 160/5.0	0.208	0.56	0.408	0.89	562	158	100	15.8	11.2
N74, 10-13-15									
n, 80/5.0	0.964	1.09	0.878	1.96	31623	1995	1178	446.7	281.9
N73, 10-13-15									
n, 80/5.0	1.010	1.03	0.890	2.01	31623	1000	1178	446.7	177.8
N45, 10-13-15									
n, 80/5.0	0.954	1.08	0.874	1.95	1412	447	141	56.2	31.6
N43, 10-13-15									
n, 80/5.0	0.620	0.91	0.704	1.58	2818	1000	398	112.2	63.1
103, 10-13-15									
n, 1120/1.4	14.58	0.72	3.420	7.64	512	316	71	20.0	14.1
107, 10-13-15									
n, 1120/1.4	14.85	0.78	3.450	7.71	631	178	71	22.4	12.6
N51, 10-13-15									
n, 1120/1.4	13.80	0.80	3.320	7.43	414	212	40	15.6	10.2
N55, 10-13-15									
n, 1120/1.4	14.20	0.86	3.370	7.54	506	246	58	18.3	14.1
N15, 10-13-15									
p, 160/5.0	0.240	1.04	0.438	0.98	501	200	50	22.4	20.0
N11, 10-13-15									
p, 160/5.0	0.252	1.11	0.448	1.00	502	100	32	17.7	11.2
N51, 2-5-7									
p, 2240/1.8	11.12	0.37*	2.980	6.67	1585	447	28	17.8	27.8
N55, 2-5-7									
p, 2240/1.8	13.00	0.73	3.220	7.21	224	100	25	10.0	7.9
N103, 2-5-7									
p, 2240/1.8	0.039	1.18	0.176	-					

	1	2	3	4	5	6	7	8	9	10
N64, 2-5-7										
n, 80/50	0.040	1.16	0.178	-						
N65, 2-5-7										
n, 80/50	0.035	1.08	0.166	-						
N34, 2-5-7										
n, 80/50	0.015	0.73	0.110	-						
N36, 2-5-7										
n, 80/50	0.019	0.87	0.122	-						
N43, 2-5-7										
n, 80/50	0.888	0.84	0.844	1.89	3162	1122	355	125.9	79.4	
N45, 2-5-7										
n, 80/1.4	0.940	0.85	0.867	1.94	1995	891	251	79.4	44.7	
N73, 2-5-7										
n, 80/1.4	0.541	0.51	0.658	1.47	3981	1585	562	354.8	158.5	
N74, 2-5-7										
n, 80/1.4	1.030	0.80	0.908	2.03	15848	5623	1778	316.2	177.8	
N102, 2-5-7										
p, 2240/1.8	22.50	1.03	4.240	9.49	3981	1995	759	354.8	199.5	
N103, 2-5-7										
p, 2240/1.8	12.73	0.14*	3.190	7.14	17782	7080	4466	707.0	560.0	
N107, 2-5-7										
p, 2240/1.8	14.94	0.49*	3.416	7.73	200	89	20	11.9	11.2	
===== ===== ===== ===== ===== ===== ===== ===== ===== ===== =====										

2.7.4. Conclusions

Analysis of MOSFET test structure measurement data given in Tables 2.23 and 2.24, as applied to using investigated digital CMOS technology available in Minsk, allows one to draw the next conclusions:

2.7.4.1. n-type MOSFETs have low allowable source-drain voltage about 5 - 6 V which restricts IC supply voltage by approximately +/- 5 V boundaries. To increase the supply voltage one may use some traditional measures such as cascode MPOSFET connections, internal biasing circuits, but all of them don't permit to increase the allowable input/output in-phase signal region for analog IC.

2.7.4.2. Short-channel pMOSFETs have low difference resistivity (full parameter L^-1) which restricts usual amplifier circuits gain.

$$Ku' = S_{pmos} * (R_{outpmos} \parallel R_{outnmos}) = S_{pmos} \left(\frac{1}{L_{pmosld}} \parallel \frac{1}{L_{nmosld}} \right)$$

(See Fig.2.3a.)

$$Ku'' = S_{pmos} * (R_{outpmos} \parallel 5 k) = S_{pmos} \left(\frac{1}{L_{pmosld}} \parallel 5 k \right)$$

(See Fig. 2.3b.)

NOTE. The small values Uth*, marked with asterix "*" in Table 2.24, illustrate large errors of the transistor threshold value determination.

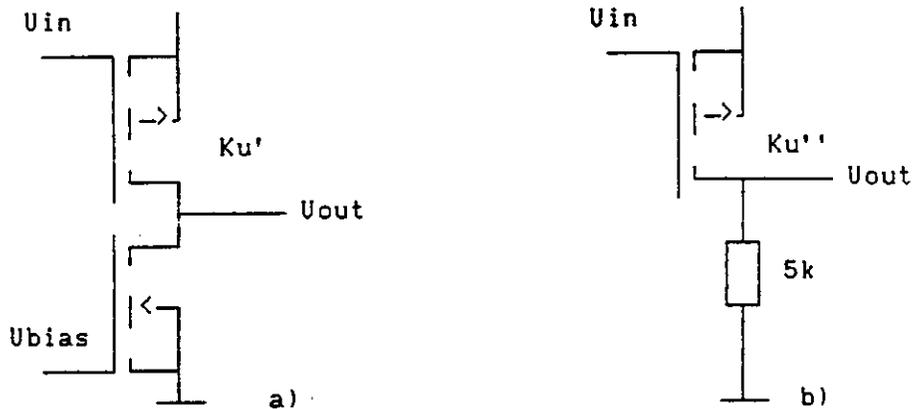


Fig.2.3. Test MOSFET connection: a) complementary circuit, b) resistor load

Short-channel pMOSFETs and nMOSFETs have at $I_d = 1 \text{ mA}$ $L_{p\text{mos}}^{-1} = 9 \text{ V}$ and $L_{n\text{mos}}^{-1} = 25 \text{ v}$, $S_{\text{pmos}} = 1.5 \text{ mA/V}$. Then

$$K_u' = 1.5 \text{ mA/V}[(9 \text{ V}/1 \text{ mA}) \parallel (25 \text{ V}/1\text{mA})] = 10.0$$

$$K_u'' = 1.5 \text{ mA/V}[(9 \text{ V}/1 \text{ mA}) \parallel 5\text{k}] = 4.84$$

For long-channel pMOSFETs and NMOSFETs with $l = 5.0 \text{ um}$ at $I_d = 1 \text{ mA}$ we have $L_{p\text{mos}}^{-1} = 40 \text{ V}$, $L_{n\text{mos}}^{-1} = 40 \text{ V}$, $S_{\text{pmos}} = 1.0\text{mA/V}$ and

$$K_u' = 1.0 \text{ mA/V}(40\text{k} \parallel 40\text{k}) = 20.0$$

$$K_u'' = 1.0 \text{ mA/V}(40\text{k} \parallel 5\text{k}) = 4.44$$

2.7.4.3. Shot-channel MOSFETs ($l = 1.8 \text{ um}$) in the average have 2.5 - 3.0 times larger flicker noise than long-channel ($l = 5.0 \text{ um}$) ones while their channel white noises are approximately the same at the 25 kHz.

2.7.4.4. Among the equal channel-length p- and nMOSFETs pMOSFETs have noise levels approximately 3 - 4 times less at 100 Hz.

2.7.4.5. Short-channel MOSFETs of the best construction ($S = 6-8 \text{ mA/V}$ at $I_d = 1 \text{ mA}$) have rather large channel noise $E_n = 10-15 \text{ nV/Hz}^{1/2}$. For comparison pJFET of the same transconductance has $E_n = 2-4 \text{ nV/Hz}^{1/2}$, and $E_n = 7-8 \text{ nV/Hz}^{1/2}$ for $S = 0.5 \text{ mA/V}$.

2.7.4.6. Similar foreign AMPLEX MOSFET structures [1] have significantly better noise parameters:

- flicker noise at 100 Hz - $17.3 \text{ nV/Hz}^{1/2}$
- thermal noise at 100 kHz - $4.8 \text{ nV/Hz}^{1/2}$.

Nevertheless taking into account 3.7 times larger AMPLEX head pMOSFET size $5000 \times 3 = 15000 \text{ sq.um}$ as compared with $2240 \times 1.8 = 4032 \text{ sq.um}$ for our largest test MOSFET structures, one may suppose flicker noise levels about $24.0 - 27.0 \text{ V/Hz}^{1/2}$ to be for the best samples if they would have the same square as in AMPLEX. The flicker noise is assumed to be reduced by further modernisation of the existing MOSFET technology.

3. IC PARAMETERS MEASUREMENTS RESULTS

3.1. The measurement methodic

The main parameter of the preamplifier, crucial for the detector resolution, is the equivalent noise charge (ENC). The experimental noise measuring bench was created for the ENC measurement. Its block-diagram is presented on the Fig.3.1. The noise measurements were made according the peak detector methodic with a sample oscilloscope used as the peak detector. A measurement bench is based on ABM PC AT-286 and CAMAC. The measurement bench is operating in a following way. The measurement cycle is initiated by computer. The computer commands the output register, installed in the CAMAC crate, to generate the start pulse for the generator 61-15. The generator gives out the voltage pulse with front edge 250 psec, which goes through the attenuator TT4132/C to the calibrated capacitor, connected in series with the preamplifier input (the electric circuit of the readout channel prototype, used in ENC measurement, is presented in the Fig.3.2). The capacitor acquires the electric charge

$$Q = C \frac{U}{10^{(K/20)}} \quad (3.1)$$

where C is the calibrated capacity, F;
 U is the pulse amplitude, V;
 K is the attenuation factor, dB.

The signal from the preamplifier, shaped by the shaping amplifier (see Fig. 3.2) comes to the input of sampling oscilloscope. The sample and hold device (SHD) of the sampling oscilloscope CK7-18 gets the amplitude of received signal and holds it for some time. From the SHD the signal is put to the 12-bit ADC 08-71, installed in the CAMAC crate. The digitized signal then is being read by computer.

The measurement cycle described above is being repeated over and over again. The result is the amplitude spectrum. When there are no parasite oscillations and other distorting factors the acquired spectrum has a gaussian shape. Two amplitude spectra, acquired with different values of attenuation factor, are necessary to get one value of ENC. The attenuation factor is set by means of programmable attenuator, controlled by the computer. The charge-to-voltage conversion coefficient K is calculated with the next formula:

$$K = \frac{U_1 - U_2}{Q_1 - Q_2} \quad (3.2)$$

where Q1 and Q2 are the input charges for two different attenuation factors, calculated with formula (3.1), whereas U1 and U2 are mean amplitudes of the system response. U1 and U2 are calculated by fitting the acquired amplitude spectra with gaussian by maximum likelihood method. The second parameter of the fitting procedure is the standard deviation sigma, which is used further for calculation of equivalent noise charge:

$$ENC_{r.m.s.} = \frac{\sigma}{K} \quad (3.3)$$

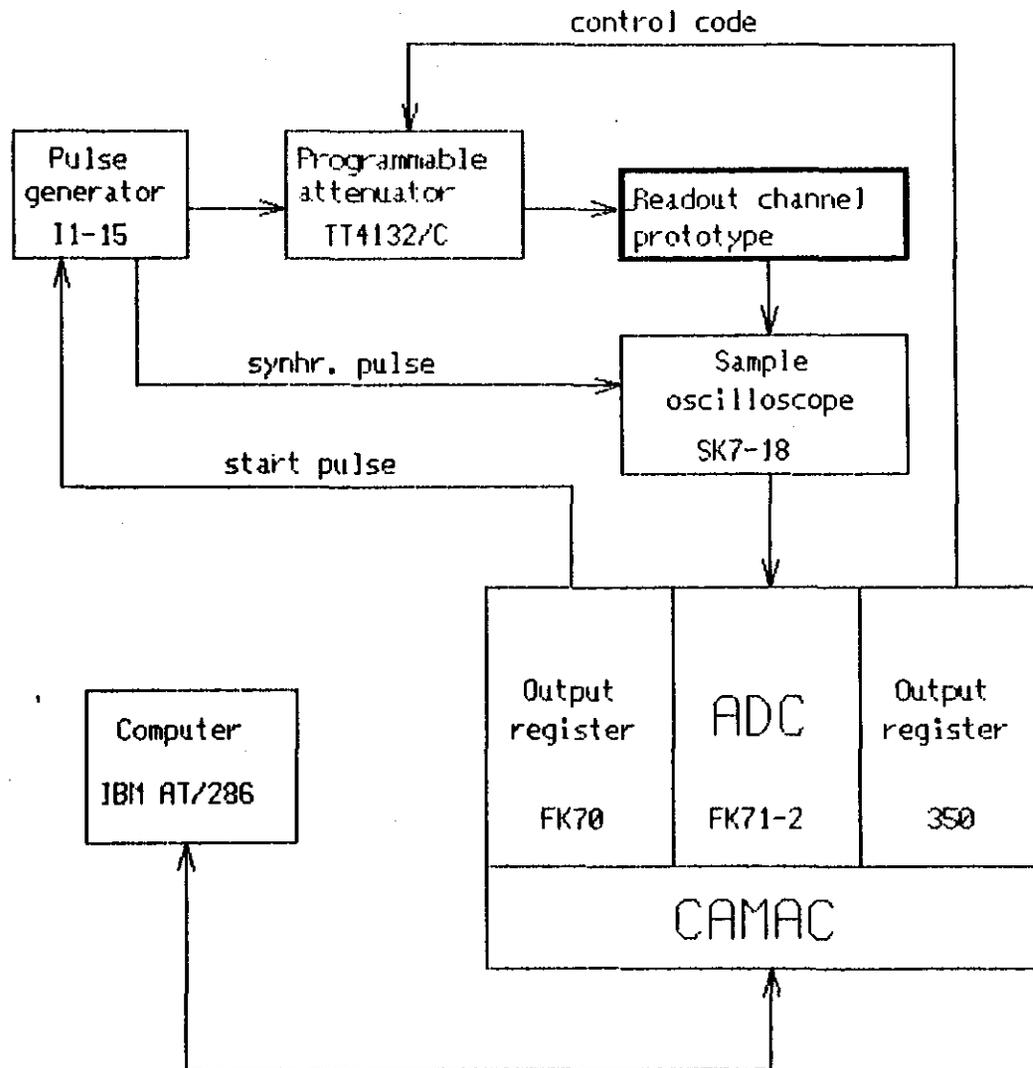


Fig.3.1. Experimental setup for ENC measurement

The value of ENC, calculated with formula (3.3), describes the full noise of the system. To get in consideration the noise of the measuring tract itself one have to perform the measurement of σ_{tract} with the preamplifier turned off. The σ_{tract} is being calculated with the same fitting procedure mentioned above.

Then the response amplitude standard deviation of the preamplifier itself is calculated:

$$\sigma_{preamp} = (\sigma_{full}^2 - \sigma_{tract}^2)^{1/2} \quad (3.4)$$

Putting the calculated value of σ_{preamp} into the formula (3.3) one obtains the ENC of the preamplifier itself.

The calculated value of the ENC together with some auxiliary information (the charge-to-voltage conversion coefficient, the detector capacity, the shaping time etc.) is being wrote to the computer hard disk, where the information about tested lot of IC's is being accumulated.

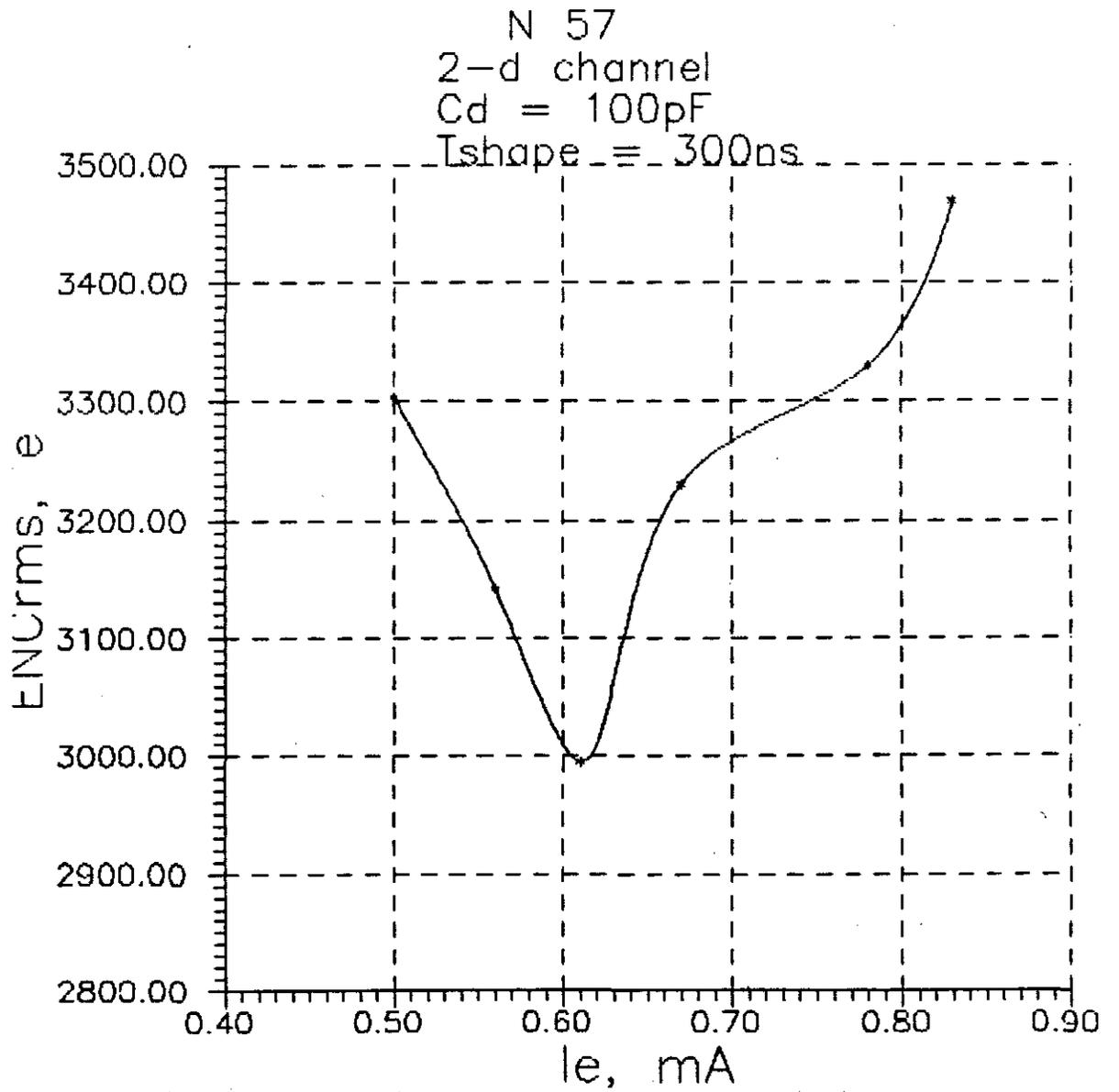
When all measurement are finished, the program of format transformation makes file in the GRAPHER format for the visual interpretation of the measurement results.

3.2. The BJT version IC measurements results

Electric connection circuit of the BJT version channel 1 of CSP/Shapers IC to measure ENC is drawn in Fig.3.2. An CSP input head transistor of the first channel is supposed theoretically to have $R_{bb}' = 93 \text{ Ohm}$. A CSP output signal comes to a SS input with time characteristics determined by capacitances C7, C8 and resistors R5, R6. The values to be used in the test circuit form $T_p = 300 \text{ nsec}$. The filtered signal trough the buffer amplifier (transistors VT1 and VT2) comes to the sample oscilloscope 50 Ohm input.

Three external elements are connected to CSP and SS. The capacitances C4 and C7 shunt high frequency oscillations which may have arisen at the cascode and reference JFETs' gates. Resistors R3 and R8 set drain currents of common gate stages. The drain currents may have values 100 - 200 μA . The cascode JFET drain current increasing causes the channel dissipated power to increase, and the current decreasing cause the JFET transconductance to decrease and consequently to decrease the circuit gain and speed. Resistors R4, R5 and R9 regulate the CSP/SS head transistor currents. The values of resistors shown in Fig.3.2. give the possibility to change this currents in interval 0.5 - 1.0 mA. The current lower boundary restriction is caused by the fact that the JFETs' gate voltage can't be more positive than +6 V. The upper boundary current restriction is due to transition of the cascode JFET to resistive operation region at larger values of the current. All the noise measurements have been made at the head transistor collector current equal 0.61 mA. This current value corresponds to minimum ENC for the most of CSP chips as exemplified by a drawing in Fig. 3.3.

Fig.3.3. ENC versus input device standing current



In Figs. 3.4 - 3.6 are shown the output signals of the CSP, SS and FS. The slow shaper peaking time $T_p = 300$ nsec. In such conditions the dependence $ENC = f(C_d)$ was measured for both channels of five chips. The curves are presented in Figs. 3.7, 3.8. It is seen that the channel 1 CSP with the head BJT $R_{bb'}$ supposed to be equal 93 Ohm has ENC about 200 - 300 e- more, than this for the channel 2, whose input transistor $R_{bb'}$ has supposed to be equal 15 Ohm. The slope of the curve $ENC = f(C_d)$ is approximately the same for all the chips and is equal to no more than 8 e-/pF for most of the chips (7e/pF for the best one, see fig.3.9).

The CSP and SS open loop voltage gain estimated in the test is equal $K_v = 800$.

The power dissipated in one channel (CSP+SS+FS) is measured to be equal $P_{sup} = 67$ mW. This value is one third less again the specified one due to the less head transistor collector current optimised for ENC.

In Figs.3.10, 3.11 are presented ENC histograms of 51 and 57 chips for the first and the second channels respectively at $C_d = 100$ pF to compare the noise characteristics of the two channels. The histogram area of the first channel input device is less than that of the second channel.

3.3. The JFET version IC measurements results

The electric circuit of the JFET version channel 1 connection for ENC measurements is presented in Fig. 3.12. In this circuit the slow shaper is connected as an integrator, the fast one - as a differentiator. This configuration is explained by the unsufficiently low gain of the JFET version CSP which forced us to achieve an additional gain in the shaper stages. The peaking time $T_p = 300$ nsec, shaper's gain is 10. The buffer amplifier made of transistors VT1 and VT2 transmits the signal to the 50 Ohm impedance sample oscilloscope.

In fig. 3.13 the first channel ENC dependence on a detector capacity is shown. The head JFET there has larger size and larger gate capacitance (about 10 pF) and hence better capacitance matching. ENC for this case is substantially larger than for the BJT version and can be represented as $ENC = 3300e + 20e/pF$ at the interval of $C_d = 0 - 220$ pF.

The second channel has the head CSP JFET of less size and gate capacitance (about 6 pF). Its noise is estimated to be equal $ENC = 4400e + 27e/pF$. The preamplifiers of all the two channels have open loop voltage gain not enough to be used as a charge-sensitive preamplifiers for CSC muon detectors: $K_u = 57$ for the first channel CSP and $K_u = 30$ for the second one.

The output signals of the preamplifier and the signal path shaper are shown in Fig. 3.14.

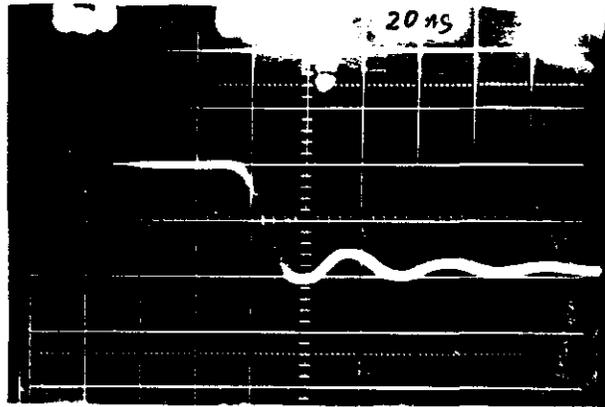


Fig.3.4. Preamplifier response, Channel 2,
 $V_{in}=100$ mV, $C_{in}=1$ pF, $C_d=100$ pF.

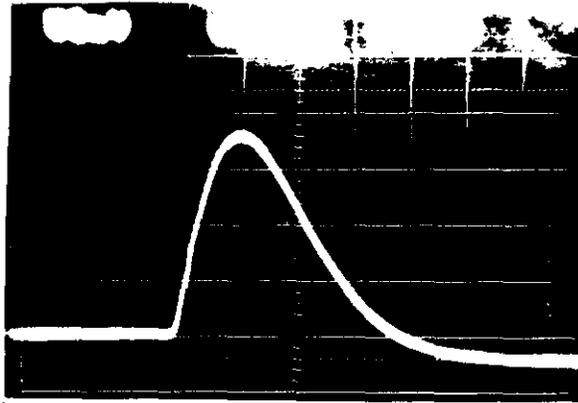


Fig. 3.5. Response of the circuit,
presented on the Fig 3.2, Channel 2,
 $V_i=100\text{mV}$, $C_{in}=1\text{pF}$, $C_d=100\text{pF}$.

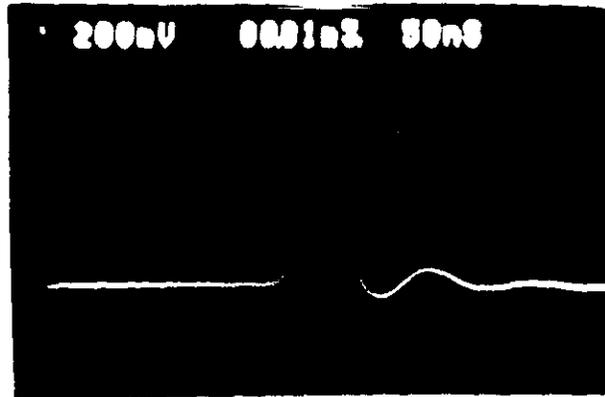


Fig.3.6. Fast shaper response.
Channel 2.
 $V_{in}=100mV$, $C_{in}=1pF$, $C_d=100pF$.

Fig.3.7. ENC versus detector capacity
(first channel)

NN 50,51,52,57,65
1 channel
 $I_e = 0.61\text{mA}$
 $T_{\text{shape}} = 300\text{ns}$

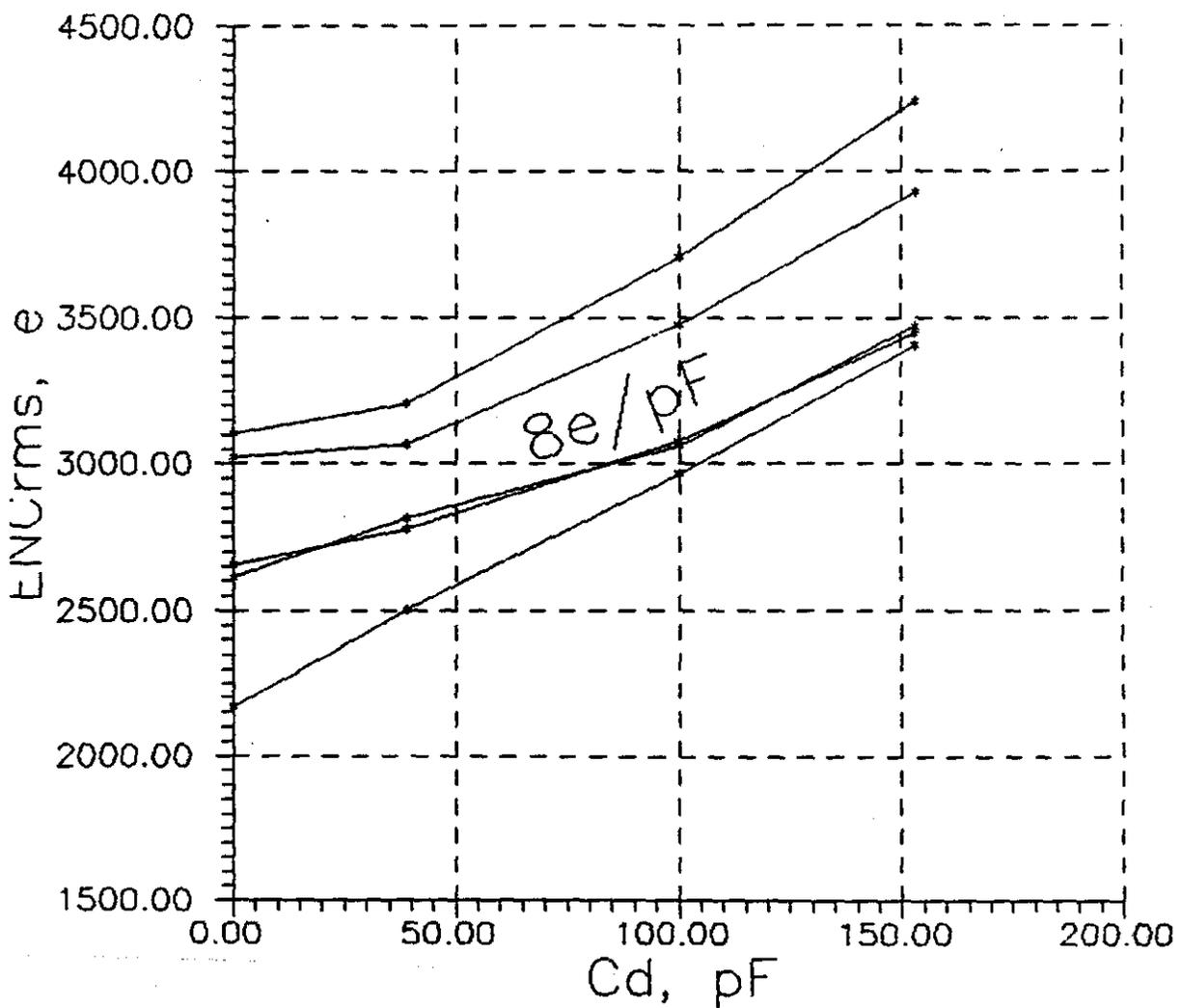


Fig.3.8. ENC versus detector capacity
(second channel)

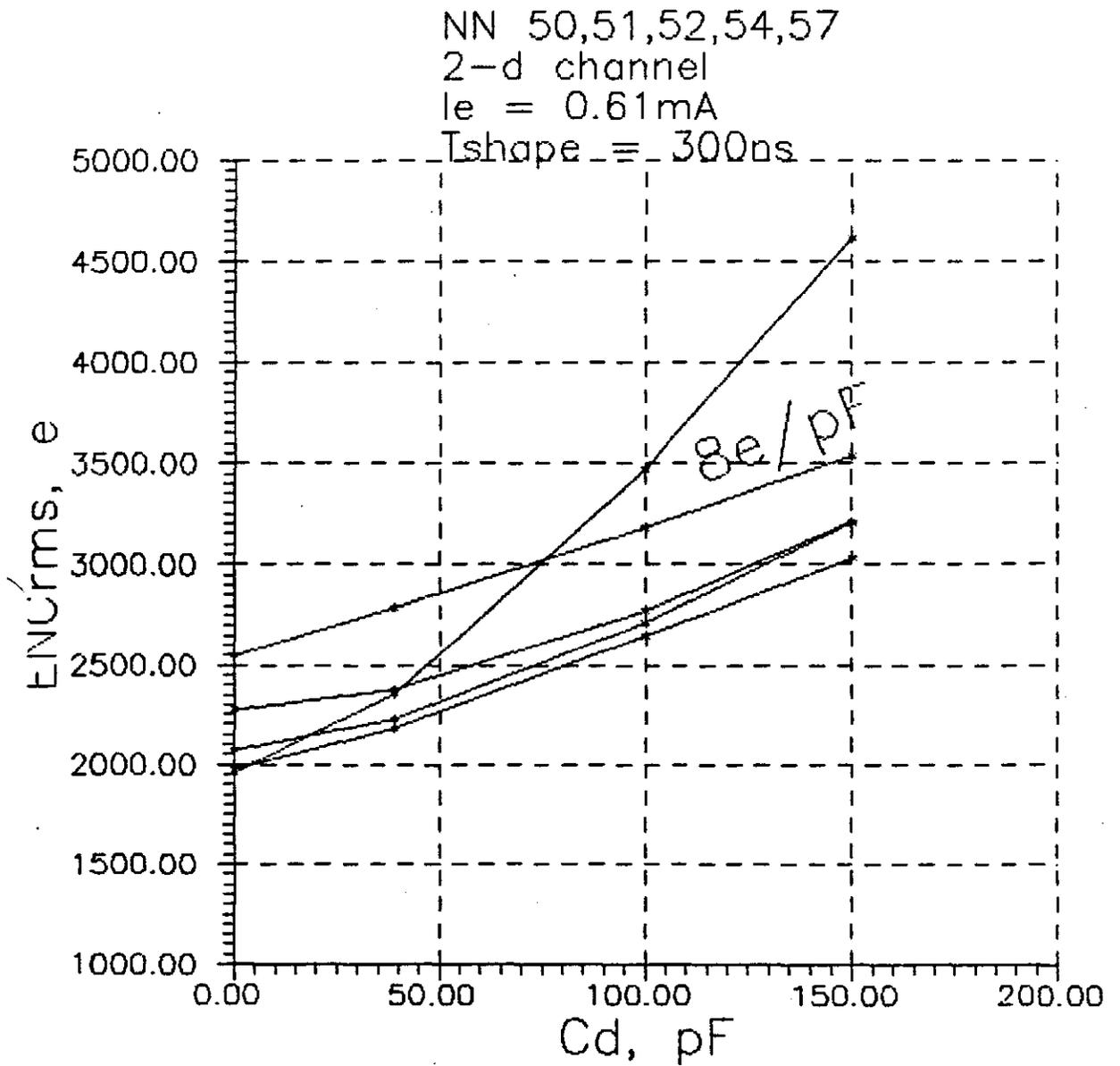


Fig.3.9

N 50
2-d channel
 $I_e = 0.61\text{mA}$
 $T_{\text{shape}} = 300\text{ns}$

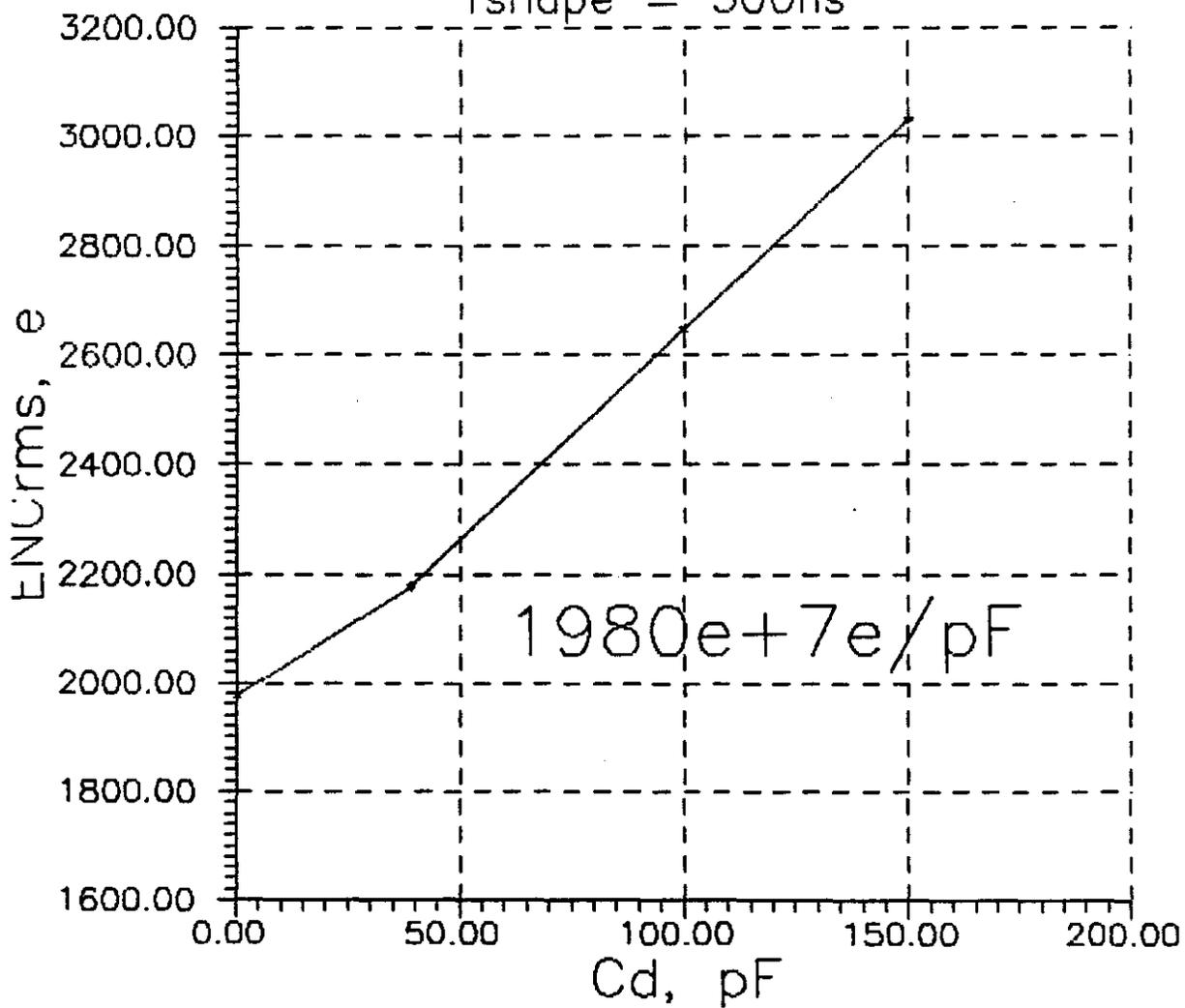


Fig.3.10
Channel 1 (51 IC)
Cd = 100pF
T_shape = 300ns

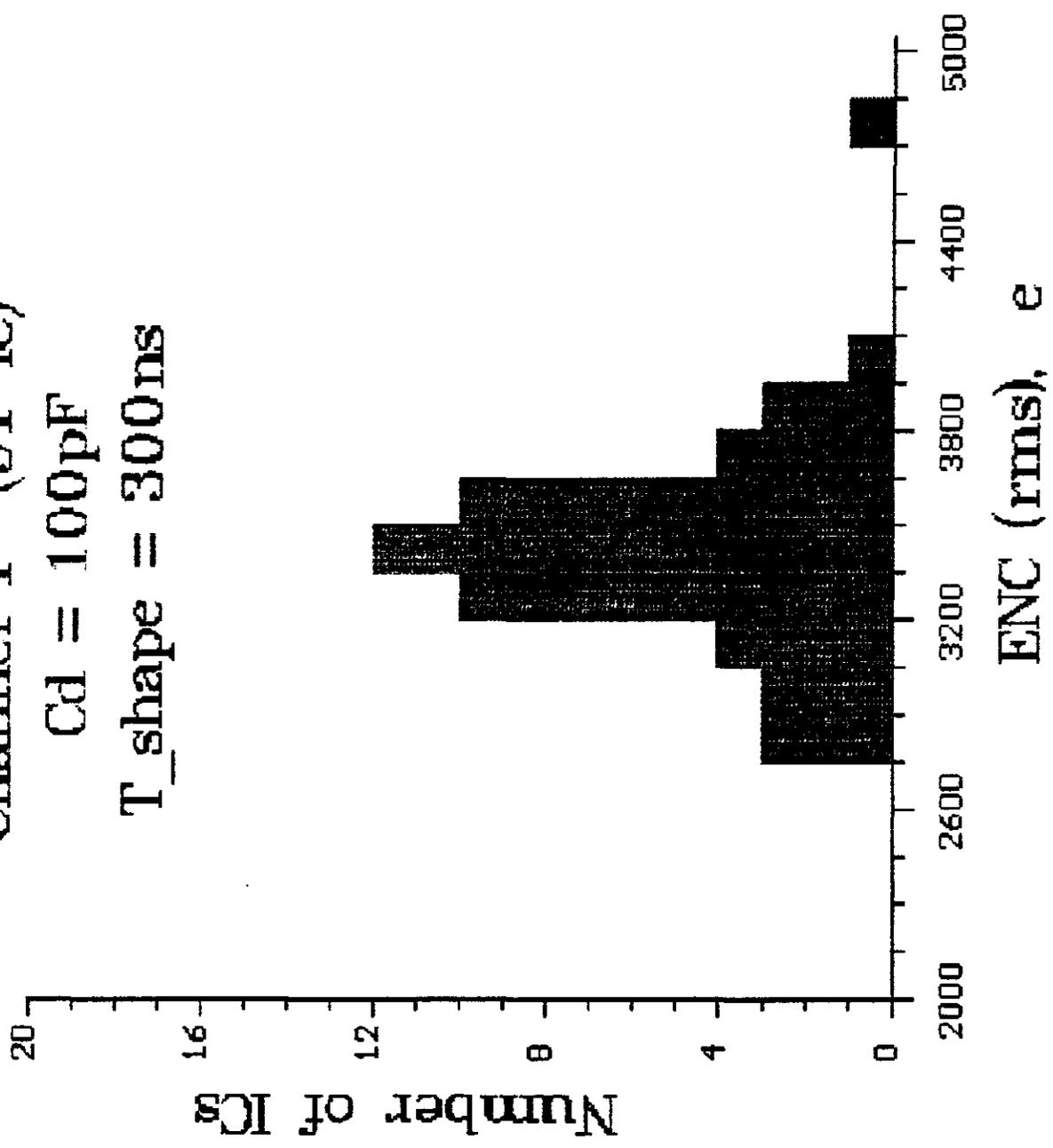


Fig.3.11

Channel 2 (57 IC)

$C_d = 100\text{pF}$

$T_{\text{shape}} = 300\text{ns}$

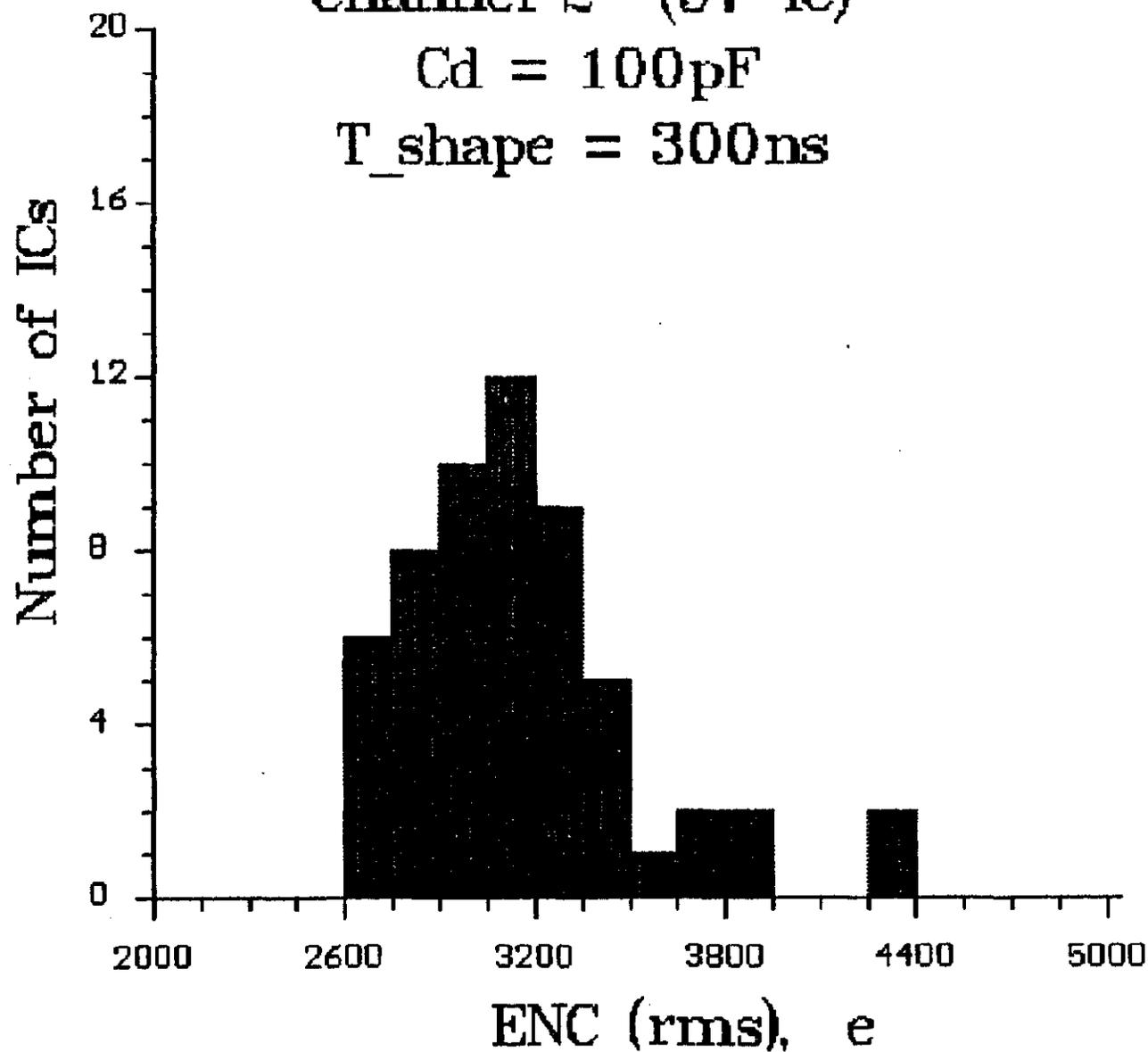
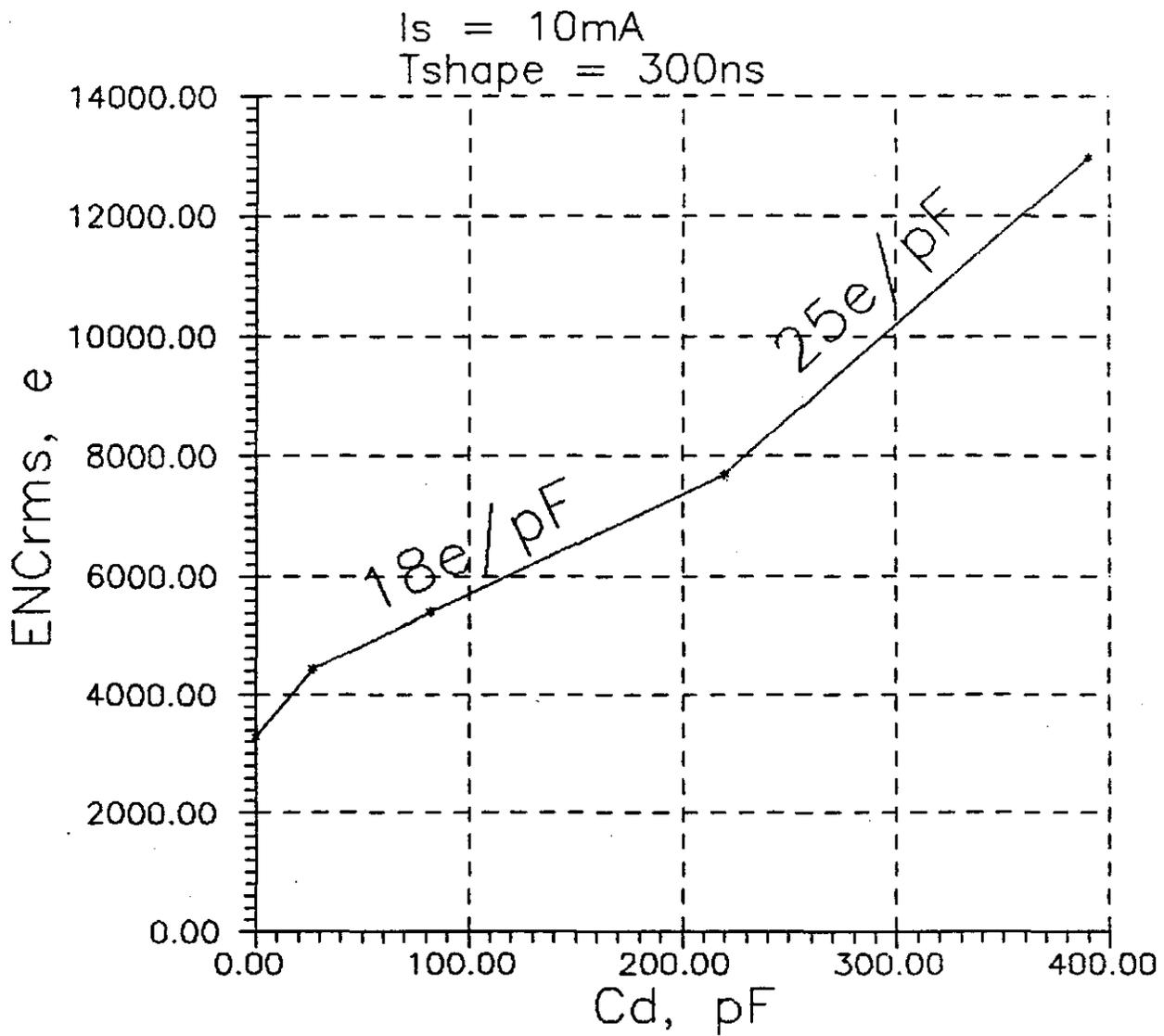


Fig.3.13. ENC versus detector capacity for the first channel of the JFET version of IC



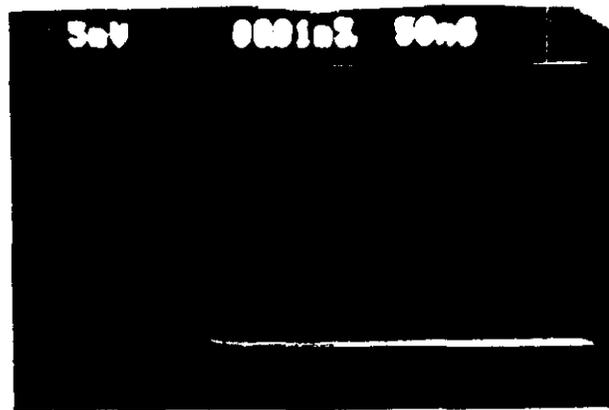


Fig. 3.14.a. Preamplifier response, JFET version Channel 1, $C_d=100\text{pF}$, $C_{fb}=C_{in}=1\text{pF}$, $V_{in}=10\text{mV}$.

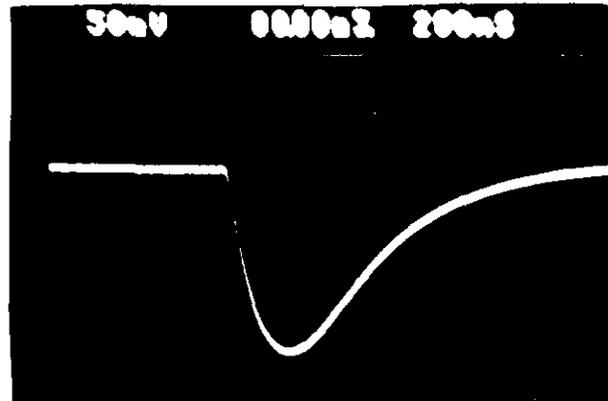


Fig. 3.14.b. Slow shaper response for $V_{in}=100\text{mV}$, $C_d=100\text{pF}$.

The Pspice simulation with the mentioned above refined element parameters gives gain value 42 as it is seen from Figs. 1.16, 1.17. The low open loop voltage gain causes the the strong conversion factor dependence on a detector capacitance C_d to be evident from Figs. 1.14 and 1.15. Connection a capacitor 100 pF to the input of the CSP leads to one third degradation of the CSP output signal. The open loop voltage gain for the circuit chown in Fig. 1.13 may be calculated with the formula $K_u = G_{max} * R_2$. The voltage gain is supposed to be increased by introducing of an active load to the cascode stage. It should be noted another drawback of this JFET version circuit. The circuit element parameter dispersion forced us to use an additional external resistor R (see Fig.3.11) to increse a drain current of VT1 and to set operational point of the circuit. To eliminate this drawback we must change the circurity of this JFET version.

3.4. The measurement results discussion

The next conclusions are supposed to be made based on the reported results of the first iteration CSC front-end IC measurements.

3.4.1. The first version of IC contained two channels, each being consisted of a charge-sensitive preamplifier with microwave bipolar transistor with R_{bb}' supposed to be equal 15 Ohms used as an input head transistor, followed by a slow shaper in signal path and a fast shaper in trigger path, have ENC less than 3000 r.m.s.e- at detector capacitance $C_d = 100$ pF and peaking time $T_p = 300$ nsec. The best samples have $ENC = 1980e + 7e/pF$, the typical value of the slope is $8e/pF$. The dissipated power is less than 70 mW per channel at the noise optimum value of the head transistor collector current being equal 0.61 mA.

3.4.2. The same channel but with the head transistor possessing $R_{bb}' = 93$ Ohm have about 200 - 300 r.m.s.e- more ENC than the mentioned above measured at the same conditions. It seems possible to achieve an additional diminishing of ENC through the further lowering of R_{bb}' , but it must have not be very large according our calculations reported in chapter 1 of this report and in literature [20 , 21].

3.4.3. The second IC version of the same configuration but with p-type JFET head transistor with gate capacitance $C_g = 10$ pF has $ENC = 3300e + 20e/pF$ at the same conditiones. The dissipated power is equal 150 mW per channel at the standard connecion, but it is possible to diminish this value to approximately 80 mW per channel by decreasing the negative suppling voltage. The CSP has open loop voltage gain $K_u = 57$. Tis value seems to be too small to use the circuit for CSC muon detector.

3.4.4. The channel with the head JFET of less size has noise $ENC = 4400e + 27e/pF$ (this value may have been refined in future in the direction of less noise values). The dissipated power is some less than in the former case. Voltage gain is too small again and is equal 30.

3.4.5. The BJT version IC is supposed to be refined in the next way:

3.4.5.1. The minimum size BJT with $AREA = 0.012$ used in the output CSP stage should be enlarged or replaced with a Darlington's emitter follower to increase the ouput power of the circuit and to improve its stability in respect to autoexcitation.

3.4.5.2. The resistor in the head transistor emitter circuit should be removed to enlarge the input stage transconductance and open loop voltage gain.

3.4.5.3. The slow/fast shaper circuit version is investigated which has JFET output stage.

3.4.6. The JFET head transistor version is considered to introduce the next improvements:

3.4.6.1. The head transistor transconductance should be enlarged to decrease the series input resistance to $R_s = 20 \text{ Ohm}$.

3.4.6.2. The active load should be introduced to the cascode stage to enlarge the open loop voltage gain and through this to diminish the dependence of charge-to-voltage transformance coefficient on the input capacitance.

3.4.6.2. The electric circuit should be modified to exclude possible latching due to monolithic circuit parameter scattering.

3.5.7. Pspice simulations results after the models refinements are in a good agreement with values measured on the real IC.

3.5.8. The measurement bench should be refined to give more versatility.

CONCLUSIONS

On the base of all the investigations reported above it is possible to make the next conclusions:

- the supposed combined BJT-JFET technology seems to be appreciable for GEM CSC front-end custom monolithic electronics;

- the refined electronic component models used in Pspice simulations proved to provide satisfactory coincidence of the parameters the simulated circuits and realized IC;

- the IC version with the head microwave BJT appears to be acceptable after future modernization for CSC muon detector; the first iteration product IC consisted of a charge-sensitive preamplifier followed by slow signal shaper and fast trigger one have demonstrated the noise performance $ENC = 1980 + 7e/pF$ at input capacity 100 pF, peaking time 300 nsec and dissipated power less than 70 mW per channel;

- the IC version with the head JFET needs in circuit modernization due to low open loop voltage gain; nevertheless, it seems to be promising too because good performance of JFET being used as a head element;

- the second design iteration should made further impact on problems of multiplication of channel-per-chip number, diminishing of the interconnection capacitors values and dissipated power, stability in respect to autoexcitation;

- the slow shaper should realize RC-CR⁴ filtering;

- the measurement bench should be modified for mor versatility.

We hope to take all this in account during the second design iteration.

REFERENCES

1. Kostromin P.P. et al. Fast operating Proportional Chamber Working with Freon-14 and Isobutane Mixture: IHEP preprint 87-59.-Serpukhov, 1987.-p8, figs. 4, refs.: 4
2. Kurchaninov L.L. et al. Fast-Cycling Minidrift Chamber with Freon-14 (80%) and Isobutan (20%) Mixture: IHEP Preprint 89-131.-Serpukhov, 1989.-p.6, figs. 4, refs.: 6
3. R.J. Yarema, T. Zimmerman. A High Speed, High Gain Preamplifier System for Silicon Strip Detectors: IEEE Trans. Nucl. Sci., Vol. 37, No. 2 April 1990
4. N.N. Fediakin et al. Cable connection between detector and preamplifier to avoid the radiatin damage: Nucl. Instr. and Meth., A317 (1992), 313-314
5. V. Radeka, IEEE Trans. Nucl. Sci. Ns-21, No. 1 (1974) p.51
6. A. Gola et al. Monolithic Readout electronics for the Silicon Calorimeters at SSC/LHC Colliders: Nucl. Phys. B (Proc. Suppl.) 23A (1991) 207-213
7. A. Gola et al. Monolithic matching of silicon detectors with high number of channels at very short shaping time: Nucl. Instr. and Meth. A320 (1992) 317-324
8. P. F. Manfredi, V. Sperziani. High Densiti Monolithic Front-End Systems for Detectors without Charge Multiplication: Nucl. Instr. and Meth. A279 (1989) 152-168
9. W. Butler et al. JFET-CMOS Microstrip Front-end. Nucl. Instr. and Meth. A279 (1989) 204-211
10. E. Nygard et al. CMOS Low Noise Amplifier for Microstrip Readout. Design and Results. Nucl. Instr. and Meth. A301 (1991) 506-516
11. W. Butler. Short Channel, CMOS-compatible JFET in Low Noise Applications, Nucl. Instr. and Meth. A326 (1993) 63-70
12. W. Butler et al. NJFET-PMOS preamplifier System: an upgraded version. Nucl. Instr. and Meth. A315 (1992) 420-424
13. Eric Beuville et al. Amplex, a Low-Noise, Low-Power Analog CMOS Signal Processor for Multi-Element Silicon Particle Detectors. Nucl. Instr. and Meth. A288 (1990) 157-167
14. Nucl. Instr. and Meth. A253 (1987) 439-443
15. Nucl. Instr. and Meth. A300 (1991) 335-342
16. IEEE Trans. on Electr. Devices. 1988. - V.35, N11, 1924-1934
17. Proc. IEEE Custom Integrated Circuits Conference. - 1987. pp.341-344.
18. Electrical specifications for the GEM CSC Readout. Version 1.0. Princeton-Brookhaven, May 25, 1992.
19. Summary of GEM CSC Discussion at Dubna, June 15-17, 1992
20. P.F.Manfredi et al. Low noise design of readout electronics for microstrip vertex detectors. Nucl. Instr. and Meth. A274 (1989) 477-484
21. Veljko Radeka. Low-noise techniques in detectors. Ann. Rev. Nucl. Part. Sci. 1988, 38, 217-277

A1. APPENDIX. PSPICE SIMULATION PROTOCOL

A1.1. BJT version

***** 05/12/93 ***** PSpice 4.03A - March, 1990 ***** 13:35:58 *****

dvorn

**** CIRCUIT DESCRIPTION

.opt nopage nomod

*Fast shaper

r1 1 10 2k
q1 10 3 4 mod5 0.5
r2 4 2 10
j4 14 9 10 kpf 2
r7 14 2 7k
q9 1 14 23 mod5 0.5
r11 23 2 2.7k
Rfb1 23 3 33k
*Rshort1 1 9 0.001
Vg1 9 0 4

Cin1 61 3 12pf

*Charge sensitive preamplifier

r3 1 11 2k
q2 11 5 6 mod5 5
r4 6 0 10
j5 15 13 11 kpf 2
q6 15 19 16 mod5 0.5
r9 16 2 1k
j10 24 1 1 kpf 2
j11 2 15 24 kpf 2
rfb2 24 5 100k
cfb2 24 5 3.9pf
*Rshort2 22 13 0.001
Vg2 13 0 5.3

qc2 19 19 72 mod5 0.5
Rc2 72 2 10k
Rc_ext2 0 19 200k

Cin2 62 5 1.6pf
vin2 62 0 pulse(0 0.125 10ns ins ins 2000ns 10000ns)

*Connecting conductors

Rshort2_1 24 61 0.001
Rshort2_3 24 63 0.001

*Biasing network (preamp)

r13 1 26 24k
j13 27 22 26 kpf 2
q14 27 27 28 mod5 0.5
q15 28 51 29 mod5 0.5
r14 29 2 2.8k
r17 1 35 1k
q19 35 27 37 mod5 0.5
q21 37 51 38 mod5 0.5
r19 38 2 1.4k
r21 1 22 24k
q23 22 43 37 mod5 0.5
r23 1 43 50k
q25 43 43 45 mod5 0.5
q27 45 51 46 mod5 0.5
r24 46 2 2.8k

q29 51 51 49 mod5 0.5
r27 49 2 10k
Rext2 51 0 160k

*Slow shaper

r5 1 12 2k
q3 12 7 8 mod5 0.5
r6 8 2 10
j7 17 20 12 kpf 2
q8 17 21 18 mod5 0.5
r10 18 2 1k
q12 1 17 25 mod5 0.5
r12 25 2 10k
rfb3 25 7 100k
*cfb3 25 7 5.6pf
*Rshort3 34 20 0.001
Vg3 20 0 5.3

qc3 21 21 82 mod5 0.5
Rc3 82 2 10k
Rc_ext3 0 21 500k

Cin3 63 7 1000pf

*Biasing network (slow form)

r15 1 30 24k
j16 31 34 30 kpf 2
q17 31 31 32 mod5 0.5
q18 32 52 33 mod5 0.5
r16 33 2 2.8k
r18 1 36 1k
q20 36 31 39 mod5 0.5
q22 39 52 40 mod5 0.5
r20 40 2 1.4k
r22 1 34 24k
q24 34 44 39 mod5 0.5
r25 1 44 50k
q26 44 44 47 mod5 0.5
q28 47 52 48 mod5 0.5
r26 48 2 2.8k

q30 52 52 50 mod5 0.5
r28 50 2 10k
Rext3 52 0 160k

v1 1 0 6
v2 2 0 -6

.MODEL MOD5 NPN IS=95e-18 BF=92 VAF=5.34 IKF=23M ISE=95e-18 xtb=1.5
+ NE=1.2 BR=0.7 VAR=5.34 IKR=1M ISC=2.39E-13 NC=2 RB=20.4 IRB=10M
+ RBM=13.5 RE=4.0 RC=25.0 CJE=0.84P MJE=88m VJE=0.75 CJC=1.19P MJC=88m
+ VJC=0.82 XCJC=0.2 CJS=2.8P MJS=0.5 VJS=0.75 tr=10n tf=11.8p itf=13.5m
+ vtf=10 xtf=2
.MODEL KPF PJP (VTO=-2.0 BETA=180U LAMBDA=50M RS=21 RD=21
+ CGS=2PF CGD=2PF FC=0.5 PB=1 IS=1.7F)
.TRAN/DP 1nS 1000nS
*.PRINT V(25)
.PROBE
.end

**** INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	6.0000	(2)	-6.0000	(3)	-5.1946	(4)	-5.9864
(5)	.7267	(6)	.0081	(7)	-5.2055	(8)	-5.9887
(9)	4.0000	(10)	2.7573	(11)	4.0113	(12)	3.6379
(13)	5.3000	(14)	-4.0962	(15)	1.9837	(16)	-5.7988
(17)	-3.6543	(18)	-5.9444	(19)	-5.0653	(20)	5.3000
(21)	-5.2294	(22)	5.2417	(23)	-4.8460	(24)	1.8416
(25)	-4.3779	(26)	3.7278	(27)	1.3667	(28)	.6303
(29)	-5.7367	(30)	3.7278	(31)	1.3667	(32)	.6303
(33)	-5.7367	(34)	5.2417	(35)	5.8596	(36)	5.8596
(37)	.6364	(38)	-5.7537	(39)	.6364	(40)	-5.7537
(43)	1.3286	(44)	1.3286	(45)	.5923	(46)	-5.7368
(47)	.5923	(48)	-5.7368	(49)	-5.7246	(50)	-5.7246
(51)	-5.0207	(52)	-5.0207	(61)	1.8416	(62)	0.0000
(63)	1.8416	(72)	-5.7650	(82)	-5.9053		

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
Vg1	-9.346E-12
Vg2	-4.612E-12
vin2	0.000E+00
Vg3	-1.062E-11
v1	-6.827E-03
v2	6.119E-03

TOTAL POWER DISSIPATION 7.77E-02 WATTS

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**** BIPOLAR JUNCTION TRANSISTORS

NAME	q1	q9	q2	q6	qc2
MODEL	mod5	mod5	mod5	mod5	mod5
IB	1.06E-05	3.05E-06	1.11E-05	1.83E-06	5.79E-07
IC	1.35E-03	4.35E-04	7.95E-04	1.99E-04	2.29E-05
VBE	7.92E-01	7.50E-01	7.19E-01	7.33E-01	7.00E-01
VBC	-7.95E+00	-1.01E+01	-3.28E+00	-7.05E+00	0.00E+00
VCE	8.74E+00	1.08E+01	4.00E+00	7.78E+00	7.00E-01
BETADC	1.27E+02	1.42E+02	7.13E+01	1.09E+02	3.96E+01
GM	4.95E-02	1.65E-02	3.04E-02	7.62E-03	8.74E-04
RPI	2.61E+03	9.12E+03	2.52E+03	1.53E+04	4.88E+04
RX	4.07E+01	4.08E+01	4.08E+00	4.08E+01	4.08E+01
RO	9.24E+03	3.37E+04	9.94E+03	5.84E+04	2.02E+05
CBE	1.09E-12	6.81E-13	5.18E-12	5.74E-13	4.91E-13
CBC	9.67E-14	9.48E-14	1.03E-12	9.75E-14	1.19E-13
CBX	3.87E-13	3.79E-13	4.13E-12	3.90E-13	4.76E-13
CJS	6.54E-13	4.67E-13	5.56E-12	7.35E-13	6.13E-12
BETAAC	1.29E+02	1.51E+02	7.66E+01	1.17E+02	4.26E+01
FT	5.01E+09	2.28E+09	4.67E+08	1.14E+09	1.28E+08

NAME	q14	q15	q19	q21	q23
MODEL	mod5	mod5	mod5	mod5	mod5
IB	2.09E-06	1.01E-06	1.66E-06	1.81E-06	4.43E-07
IC	9.09E-05	9.30E-05	1.40E-04	1.74E-04	3.16E-05
VBE	7.36E-01	7.16E-01	7.30E-01	7.33E-01	6.92E-01
VBC	0.00E+00	-5.65E+00	-4.49E+00	-5.66E+00	-3.91E+00
VCE	7.36E-01	6.37E+00	5.22E+00	6.39E+00	4.61E+00
BETADC	4.35E+01	9.19E+01	8.47E+01	9.61E+01	7.13E+01
GM	3.44E-03	3.56E-03	5.36E-03	6.64E-03	1.21E-03

RPI	1.34E+04	2.78E+04	1.69E+04	1.54E+04	6.39E+04
RX	4.08E+01	4.08E+01	4.08E+01	4.08E+01	4.08E+01
RO	5.06E+04	1.10E+05	6.48E+04	5.89E+04	2.71E+05
CBE	5.25E-13	5.24E-13	5.47E-13	5.62E-13	4.94E-13
CBC	1.19E-13	9.92E-14	1.01E-13	9.92E-14	1.02E-13
CBX	4.76E-13	3.97E-13	4.04E-13	3.97E-13	4.08E-13
CJS	8.34E-13	1.03E-12	4.72E-13	1.03E-12	4.95E-13
BETAAC	4.61E+01	9.90E+01	9.04E+01	1.03E+02	7.74E+01
FT	4.89E+08	5.56E+08	8.11E+08	9.99E+08	1.92E+08

NAME	q25	q27	q29	q3	q8
MODEL	mod5	mod5	mod5	mod5	mod5
IB	2.09E-06	1.01E-06	6.71E-07	8.28E-06	9.86E-07
IC	9.09E-05	9.30E-05	2.69E-05	1.13E-03	5.46E-05
VBE	7.36E-01	7.16E-01	7.04E-01	7.83E-01	7.15E-01
VBC	0.00E+00	-5.61E+00	0.00E+00	-8.84E+00	-1.58E+00
VCE	7.36E-01	6.33E+00	7.04E-01	9.63E+00	2.29E+00
BETADC	4.35E+01	9.16E+01	4.01E+01	1.36E+02	5.54E+01
GM	3.44E-03	3.56E-03	1.02E-03	4.18E-02	2.09E-03
RPI	1.34E+04	2.77E+04	4.21E+04	3.34E+03	2.85E+04
RX	4.08E+01	4.08E+01	4.08E+01	4.07E+01	4.08E+01
RO	5.06E+04	1.10E+05	1.73E+05	1.19E+04	1.14E+05
CBE	5.25E-13	5.24E-13	4.93E-13	9.89E-13	5.07E-13
CBC	1.19E-13	9.93E-14	1.19E-13	9.58E-14	1.08E-13
CBX	4.76E-13	3.97E-13	4.76E-13	3.83E-13	4.33E-13
CJS	8.42E-13	1.05E-12	6.09E-12	5.83E-13	4.81E-12
BETAAC	4.61E+01	9.86E+01	4.31E+01	1.39E+02	5.94E+01
FT	4.89E+08	5.55E+08	1.50E+08	4.53E+09	3.17E+08

NAME	q12	qc3	q17	q18	q20
MODEL	mod5	mod5	mod5	mod5	mod5
IB	1.30E-06	2.51E-07	2.09E-06	1.01E-06	1.66E-06
IC	1.69E-04	9.22E-06	9.09E-05	9.30E-05	1.40E-04
VBE	7.24E-01	6.76E-01	7.36E-01	7.16E-01	7.30E-01
VBC	-9.65E+00	0.00E+00	0.00E+00	-5.65E+00	-4.49E+00
VCE	1.04E+01	6.76E-01	7.36E-01	6.37E+00	5.22E+00
BETADC	1.30E+02	3.68E+01	4.35E+01	9.19E+01	8.47E+01
GM	6.48E-03	3.52E-04	3.44E-03	3.56E-03	5.36E-03
RPI	2.16E+04	1.13E+05	1.34E+04	2.78E+04	1.69E+04
RX	4.08E+01	4.08E+01	4.08E+01	4.08E+01	4.08E+01
RO	8.43E+04	5.06E+05	5.06E+04	1.10E+05	6.48E+04
CBE	5.59E-13	4.82E-13	5.25E-13	5.24E-13	5.47E-13
CBC	9.51E-14	1.19E-13	1.19E-13	9.92E-14	1.01E-13
CBX	3.80E-13	4.76E-13	4.76E-13	3.97E-13	4.04E-13
CJS	4.67E-13	6.28E-12	8.34E-13	1.03E-12	4.72E-13
BETAAC	1.40E+02	4.00E+01	4.61E+01	9.90E+01	9.04E+01
FT	9.97E+08	5.21E+07	4.89E+08	5.56E+08	8.11E+08

NAME	q22	q24	q26	q28	q30
MODEL	mod5	mod5	mod5	mod5	mod5
IB	1.81E-06	4.43E-07	2.09E-06	1.01E-06	6.71E-07
IC	1.74E-04	3.16E-05	9.09E-05	9.30E-05	2.69E-05
VBE	7.33E-01	6.92E-01	7.36E-01	7.16E-01	7.04E-01
VBC	-5.66E+00	-3.91E+00	0.00E+00	-5.61E+00	0.00E+00
VCE	6.39E+00	4.61E+00	7.36E-01	6.33E+00	7.04E-01
BETADC	9.61E+01	7.13E+01	4.35E+01	9.16E+01	4.01E+01
GM	6.64E-03	1.21E-03	3.44E-03	3.56E-03	1.02E-03
RPI	1.54E+04	6.39E+04	1.34E+04	2.77E+04	4.21E+04
RX	4.08E+01	4.08E+01	4.08E+01	4.08E+01	4.08E+01
RO	5.89E+04	2.71E+05	5.06E+04	1.10E+05	1.73E+05
CBE	5.62E-13	4.94E-13	5.25E-13	5.24E-13	4.93E-13
CBC	9.92E-14	1.02E-13	1.19E-13	9.93E-14	1.19E-13
CBX	3.97E-13	4.08E-13	4.76E-13	3.97E-13	4.76E-13
CJS	1.03E-12	4.95E-13	8.42E-13	1.05E-12	6.09E-12
BETAAC	1.03E+02	7.74E+01	4.61E+01	9.86E+01	4.31E+01
FT	9.99E+08	1.92E+08	4.89E+08	5.55E+08	1.50E+08

**** JFETS

NAME	j4	j5	j10	j11	j13
MODEL	kpf	kpf	kpf	kpf	kpf
ID	-2.75E-04	1.99E-04	1.71E-03	1.69E-03	9.47E-05
VGS	1.24E+00	1.29E+00	0.00E+00	1.42E-01	1.51E+00
VDS	-6.85E+00	-2.03E+00	-4.16E+00	-7.84E+00	-2.36E+00
GM	7.29E-04	5.62E-04	1.72E-03	1.84E-03	3.90E-04
GDS	1.02E-05	9.05E-06	7.07E-05	6.09E-05	4.23E-06
CGS	2.67E-12	2.64E-12	3.96E-12	3.71E-12	2.52E-12
CGD	1.33E-12	1.93E-12	1.76E-12	1.34E-12	1.81E-12

NAME	j7	j16
MODEL	kpf	kpf
ID	-5.59E-05	-9.47E-05
VGS	1.66E+00	1.51E+00
VDS	-7.29E+00	-2.36E+00
GM	3.31E-04	3.90E-04
GDS	2.05E-06	4.23E-06
CGS	2.45E-12	2.52E-12
CGD	1.27E-12	1.81E-12

JOB CONCLUDED

TOTAL JOB TIME 100.90

A1.2. JFET version.

***** 05/31/93 ***** PSpice 4.03A - March, 1990 ***** 07:21:57 **

*T-2, JFET, AREA=1, Cd=100p, Cin=1p, Cfb=3.3p

**** CIRCUIT DESCRIPTION

*****>

j1 2 1 0 kpf2
r1 2 200 150
r2 100 3 8.2k
q2 3 4 2 200 mod2 0.06

r3 0 4 10k
r4 4 200 24k
Cext 4 200 0.033u
j3 5 100 100 kpf2 0.235
j4 200 3 5 kpf2 0.235

Rfb 1 5 100k
Cfb 1 5 3.3p

Rin 50 0 50
Cin 50 1 1p

Cd 1 0 100p

Vp 100 0 DC 6
Vn 200 0 DC -6

Vin 50 0 pulse(0 -10000mv 10ns 1ns 1ns 2000ns 10000ns)

.MODEL mod2 npn IS=95e-18 BF=90 VAF=20 IKF=10m ISE=95e-18 xtb=1.5
+ NE=1.2 BR=0.7 VAR=20 IKR=1m ISC=2.39E-13 NC=2 RB=15 IRB=10m
+ RBM=10 RE=5 RC=15 CJE=1.45p MJE=88m VJE=0.75 CJC=1.93p MJC=88m
+ VJC=0.82 XCJC=0.2 CJS=2.2p MJS=0.5 VJS=0.75 tr=10n tf=15p itf=10m
+ vtf=20 xtf=2

.MODEL kpf2 pjf VTO=-2.5 BETA=2.5m LAMBDA=43.3m RS=15 RD=15
+ CGS=9.27p CGD=9.2p FC=0.5 FB=1 IS=10f

.TRAN/OP 1nS 500ns
.PROBE
.END

***** 05/31/93 ***** PSpice 4.03A - March, 1990 ***** 07:21:57 *****

*T-2, JFET, AREA=1, Cd=100p, Cin=1p, Cfb=3.3p

**** BJT MODEL PARAMETERS

```
mod2
NPN
IS 95.000000E-18
BF 90
NF 1
VAF 20
IKF .01
ISE 95.000000E-18
NE 1.2
BR .7
NR 1
VAR 20
IKR 1.000000E-03
ISC 239.000000E-15
RB 15
RBM 10
IRB .01
RE 5
RC 15
CJE 1.450000E-12
MJE .088
CJC 1.930000E-12
VJC .82
MJC .088
XCJC .2
CJS 2.200000E-12
MJS .5
TF 15.000000E-12
KTF 2
VTF 20
ITF .01
TR 10.000000E-09
XTB 1.5
```

***** 05/31/93 ***** PSpice 4.03A - March, 1990 ***** 07:21:57 *****

*T-2, JFET, AREA=1, Cd=100p, Cin=1p, Cfb=3.3p

**** Junction FET MODEL PARAMETERS

	kpf2
	PJF
VTO	-2.5
BETA	2.500000E-03
LAMBDA	.0433
RD	15
RS	15
CGD	9.200000E-12
CGS	9.270000E-12

***** 05/31/93 ***** PSpice 4.03A - March, 1990 ***** 07:21:57 *****

*T-2, JFET, AREA=1, Cd=100p, Cin=1p, Cfb=3.3p

**** INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
(1)	-.5193	(2)	-2.8957	(3)	-.5606	(4)	-1.9564
(5)	-.5193	(50)	0.0000	(100)	6.0000	(200)	-6.0000

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
Vp	-4.581E-03
Vn	2.464E-02
Vin	0.000E+00

TOTAL POWER DISSIPATION 1.75E-01 WATTS

***** 05/31/93 ***** PSpice 4.03A - March, 1990 ***** 07:21:57 *****

*T-2, JFET, AREA=1, Cd=100p, Cin=1p, Cfb=3.3p

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**** BIPOLAR JUNCTION TRANSISTORS

NAME	q2
MODEL	mod2
IB	2.72E-05
IC	8.00E-04
VBE	9.39E-01
VBC	-1.40E+00
VCE	2.34E+00
BETADC	2.95E+01
GM	1.97E-02
RPI	9.95E+02
RX	2.43E+02
RO	2.54E+04
CBE	9.69E-13
CBC	2.14E-14
CBX	8.56E-14
CJS	4.67E-14
BETAAC	1.96E+01
FT	2.91E+09

**** JFETS

NAME	j1	j3	j4
MODEL	kpf2	kpf2	kpf2
ID	-1.99E-02	-3.78E-03	-3.78E-03
VGS	-5.19E-01	0.00E+00	-4.14E-02
VDS	-2.90E+00	-6.52E+00	-5.48E+00
GM	1.26E-02	3.35E-03	3.29E-03
GDS	3.10E-03	1.30E-04	1.35E-04
CGS	1.05E-11	1.96E-12	1.99E-12
CGD	5.24E-12	8.01E-13	8.68E-13

JOB CONCLUDED

TOTAL JOB TIME 15.99