GEM TN-93-411

GEM IPC Preamp/Shaper

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Abstract:

A preamplifier/shaper ASIC has been designed for the GEM IPC Tracker. The ASIC has been implemented in the Harris 1.2 micron radiation-hard CMOS process. Design details, simulation results, and layout drawings are presented in this note.

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1.0 Overview

The preamplifier/shaper IC for the GEM Interpolating Pad Chamber (IPC) must amplify the charge signal from the pad cathodes into a voltage pulse which goes to the Analog Random Access Memory (ARAM) chip. The objectives of the preamp/shaper are:

1. Achieve a noise of less than 2000 r.m.s. electrons equivalent noise charge (ENC) [1000 desirable].
2. Voltage output: semiGaussian pulse with peaking time around 30 nsec.
3. Charge-to-voltage gain of about 10.
4. Linear response up to 150 fC input charge.
5. Survive 2 Mrad ionizing and $2 \cdot 10^{14}$ n/cm^2 radiation dose over several years of operation at the SSC.

During 1992 several prototype ICs were fabricated through MOSIS to address goals 1-4 above. We now seek to assess the feasibility of meeting objective (5) with the Harris AVLSI-RA process.

2.0 Preamplifier (Fig. 1)

The preamp was adapted from a design done in the MOSIS 2 μm nwell CMOS process. A large (10,000/2 μm) input n-MOSFET is used to achieve the noise specification. The circuit is a folded cascode integrating (charge-sensitive) configuration with 1 pF MIM feedback capacitor and 400/2 source follower M3 within the feedback loop.

A long channel MOSFET M8 biased in the triode region provides a discharge path for the integrated charge with a time constant that can be adjusted from around 10^{-7} - 10^{-5} sec.

The simulated behavior of the preamp is shown in the table below:

Input device M1	10000/2 μm NMOS
M1 bias current	4 mA
Feedback C	1 pF
Feedback "R"	3/160μm PMOS, R_{eq} ~ 2MΩ at VG=0V
Noise at Cin=35 pF	1480 r.m.s. e^- with ideal 25 nsec shaper
Risetime (10 - 90%)	32 nsec
Input impedance	230 Ω

3.0 Shaper

The shaper realizes the transfer function

$$H(s) = \frac{A_0 s\tau}{(1+s\tau)^{n+1}}$$

with n=4 and A_0 positive. This has a semiGaussian step response, a pulse like function with peaking time of $n\tau$.

The shaper is implemented as a passive differentiator followed by two second-order lowpass stages shown in Fig. 2. The lowpass stages use an OTA with an internal and external pole. The loop gain is adjusted so that the two closed-loop poles coincide on the real axis at $s = -1/\tau$[1]. The Q factor of the stage is set by component geometrical ratios, while the natural frequency depends on the ratio of g_m of M1 to total capacitance at its drain. The pole frequency (and hence peaking time) can be adjusted by changing the bias current of the input differential pair, without disrupting the semiGaussian pulse shape.

Second-stage noise must be considered when designing the shaper. The major contributors are R_{diff} and R1, M1, M2, M3, and M4 of the first lowpass section. Reducing the transistor noise is accomplished by increasing their W/L ratio and bias currents. Series resistor noise can be reduced by choosing lower values for R_{diff} and R1; however, this

1. Chang, Z. and Sansen, W., Low Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies, Kluwer, 1991 pp. 186-188

requires one to increase C_{diff} and to use larger, more power consuming transistors elsewhere to drive the lower on-chip impedances. The present design is thus a compromise between noise and power/area.

The dynamic range of this stage is limited by the need to keep the output transistors M6 and M8 saturated.

4.0 Other Circuit Components

4.1 Output Source Follower.

A 200/2 μm PMOS source follower reduces the output impedance to about 375Ω, which is adequate for driving small off-chip capacitive loads. (Fig. 3).

4.2 Calibration circuit

For calibration, it is desirable to inject a uniform, known quantity of charge into each channel. The circuit of Fig. 4 has an injection capacitor whose top plate is connected to the preamp input. The bottom plate is connected to an external pulse input, or to ground by the action of a pair of NMOS switches M5 and M6.

4.3 Bias circuits

Current mirrors control the bias currents of each subcircuit. Fig. 5 shows the mirrors which control the preamp input and cascode branch currents. In Fig. 6 the bias circuits for the shaper and follower are shown. Preamp and shaper bias currents are supplied through external pins, while the follower current is set by an on-chip resistor.

4.4 I/O Pads

Standard Harris bond pads were used. These incorporate grounded-gate FETs for ESD protection. No series resistors are used.

5.0 Simulation results

A full channel consisting of input pad, calibration cell, preamp, shaper, follower, and output bond pad was simulated. The Magic layout editor provided the layout parasitics. Transistor model parameters were supplied by Harris to represent typical, best, and worst case process runs before and after exposure to 1Mrad of ionizing radiation. The model parameters, in Cadence Spice Level 5 format, were converted to HSpice Level 3 format. For all simulations C_{in}=35pF, C_{load}=10pF, and the typical case, pre-radiation model was used except where noted.

5.1 Preamp transient response - Fig. 7

Fig. 7 shows the response of the preamp to charge impulses of 30 - 150 fC. The 35 nsec risetime, gain of 1mV/fC, and slow falltime controlled by feedback transistor M8 can be clearly seen.

5.2 Peaking time and gain variation - Fig. 8

Fig. 8 shows the response of the full channel to a charge impulse of 30 fC and illustrates how the peaking time can be controlled by changing the shaper bias current. A peaking time adjustment range of about 15 nsec is possible. Pulse shape is practically constant with a change of the time and amplitude scales. For nominal bias, the gain is 11.3 mV/fC.

5.3 Dynamic range and calibration switch - Fig. 9

In Fig. 9, a series of positive and negative charge impulses of increasing amplitude is injected through the calibration capacitor. Linear response from about -100 to +150 fC is observed. The figure also illustrates the action of the calibration cell switch, which changes from enabled to disabled at 2 μsec. Subsequent calibration pulses are not injected into this channel and no output is produced. The signal at 2.6 μsec is from a 30 fC charge injected at the cathode.

5.4 Effect of capacitive load - Fig. 10

Fig. 10 shows the channel responding to a 30 fC signal, for load capacitances from 0 to 50 pF. High capacitance decreases the gain (~ 1%/pF) and lengthens the peaking time (~ 0.8 ns/pF).

5.5 Noise performance - Fig. 11

Noise simulations were done for the full channel including bond pads and input protection devices (3.04 pF), calibration circuit (1 pF), and wiring parasitics (1.65 pF). The overall ENC can be fit to the expression

$$\mathrm{ENC} = 1208\ e^- + 23.1\ (e^-/\mathrm{pF}) \bullet C_{in}$$

Fig. 11 shows the output noise spectrum (dv_n^2/df). The noise is dominated (75%) by the input transistor. The other major contributors are the resistor of the high pass circuit, and the feedback resistors and input transistors of the first shaper stage.

5.6 Effect of process variations and radiation - Fig. 12

Fig. 12 shows the output of the preamp and shaper for the typical, best, and worst case pre-radiation process files, and for the typical post-radiation process file. The simulated noise behavior for each of these 4 cases is shown in the table below:

PROCESS FILE	ENC@Cin=35pF	GAIN (NORMALIZED)
TYP- PRE-RAD	1890	1
BEST - PRE-RAD	1892	1.39
WORST- PRE-RAD	2279	0.39
TYP- POST-RAD	1926	0.95

6.0 Chip layout

Nine channels of preamp/shaper are included in the chip. Channels 0-4 and 5-8 are separately biased to allow lower power during testing. Channel 0 has the connections between preamp, shaper, and follower stages brought out to external pads for separate testing. Channel 1-4 have only preamp and shaper. Four test transistors are also included on the die. Area of one full channel is 299 x 1276 μm. Chip size is pad-limited at 4.74 x 3.78 mm, and is designed to match the width dimension of the ARAM.

The layout of the preamp/shaper is shown in Fig. 13 with pin assignments.

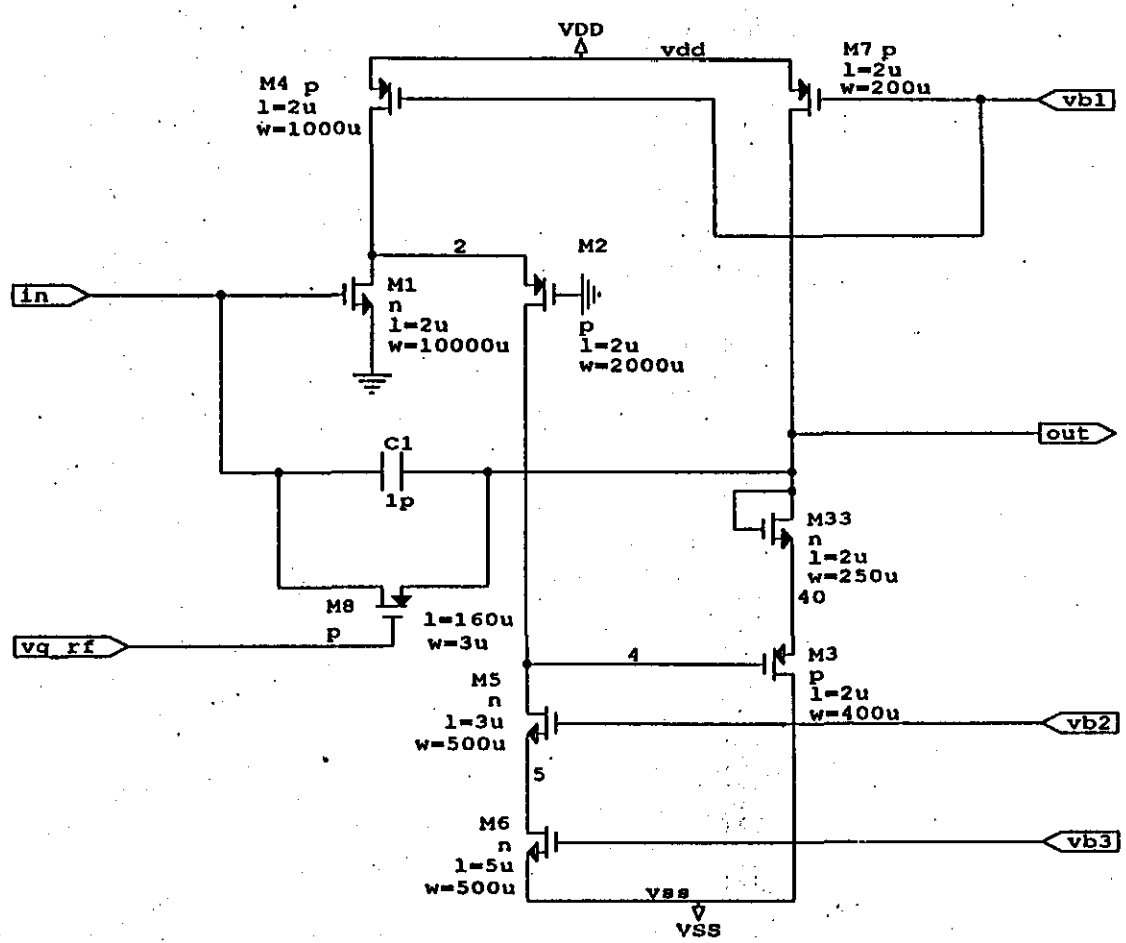

Fig. 1

Brookhaven National Laboratory Instrumentation Division		
Title IPC PREAMP FOR HARRIS AVLSI-RA		
Size A	Document Number IPC-HS-1-1	REV
Date: January 19, 1993	Sheet 1 of 1	

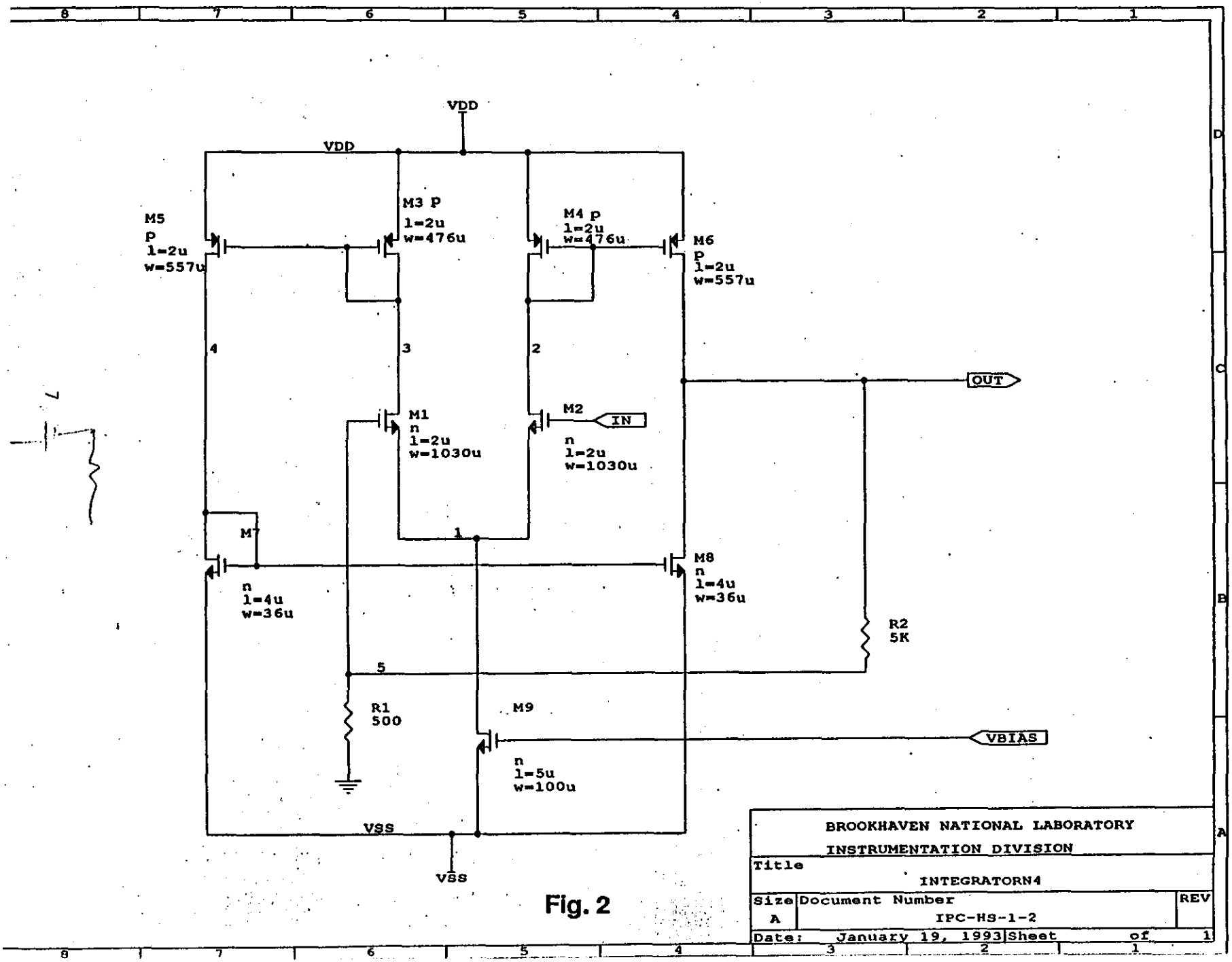
VDD
VDD
M5
p
l=2u
w=557u
M3 p
l=2u
w=476u
M4 p
l=2u
w=476u
M6
p
l=2u
w=557u
4
3
2
OUT
M1
n
l=2u
w=1030u
M2
IN
n
l=2u
w=1030u
M7
1
M8
n
l=4u
w=36u
n
l=4u
w=36u
R2
5K
5
R1
500
M9
VBIAS
n
l=5u
w=100u
VSS
VSS
BROOKHAVEN NATIONAL LABORATORY
INSTRUMENTATION DIVISION
Title
INTEGRATORN4
Size
A
Document Number
IPC-HS-1-2
REV
Date: January 19, 1993
Sheet of 1

Fig. 2

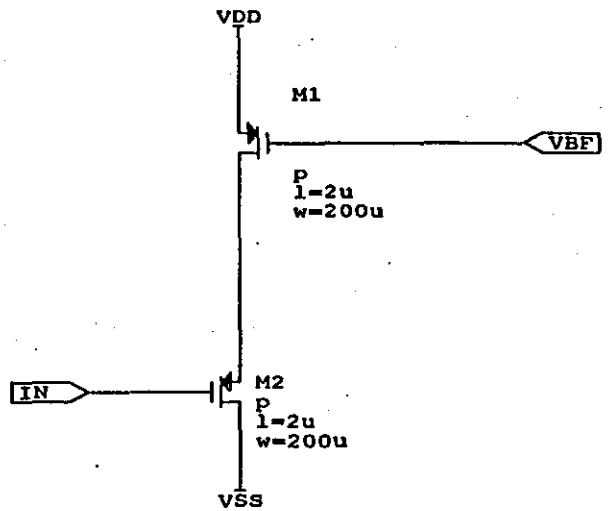

Fig. 3

BROOKHAVEN NATIONAL LABORATORY INSTRUMENTATION DIVISION		
Title FOLLOWER		
Size A	Document Number IPC-HS-1-4	REV
Date: January 19, 1993	Sheet 1 of 1	

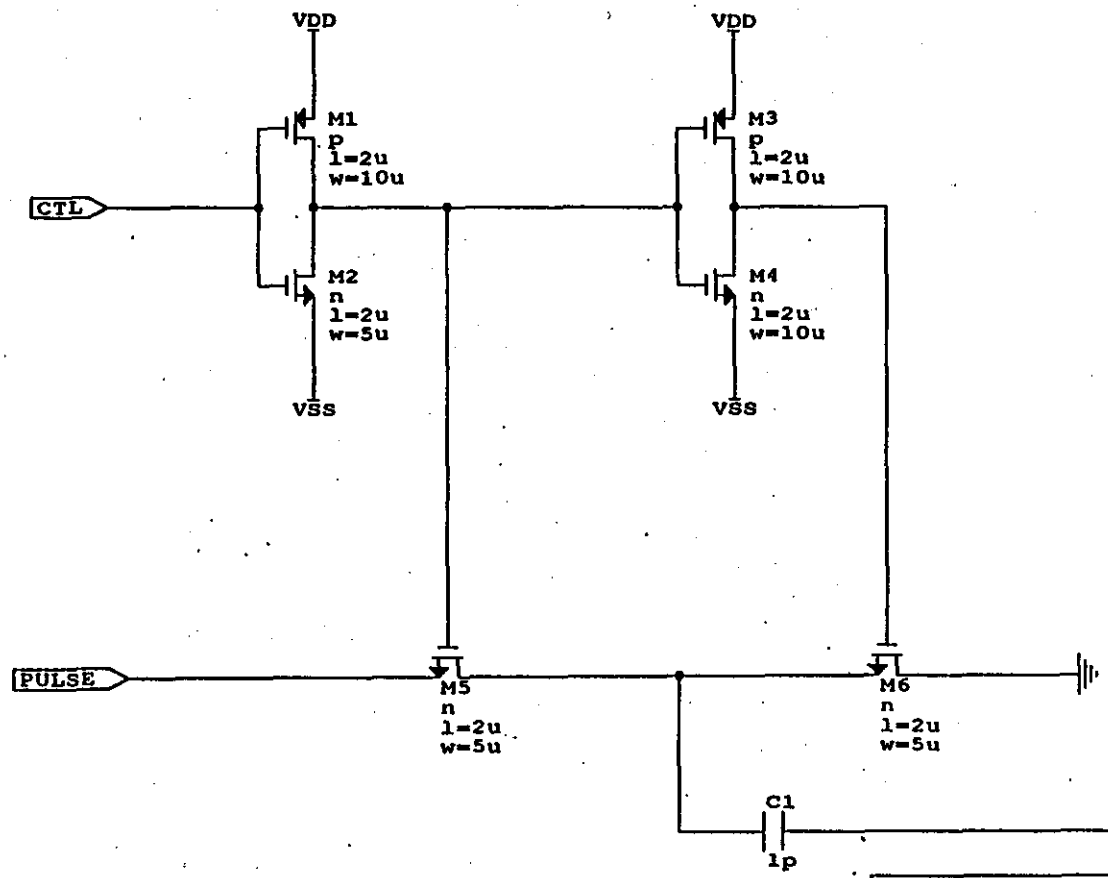

Fig. 4

BROOKHAVEN NATIONAL LABORATORY INSTRUMENTATION DIVISION		
Title CALCELL		
Size A	Document Number IPC-HS-1-5	REV
Date: January 19, 1993	Sheet 1 of 1	

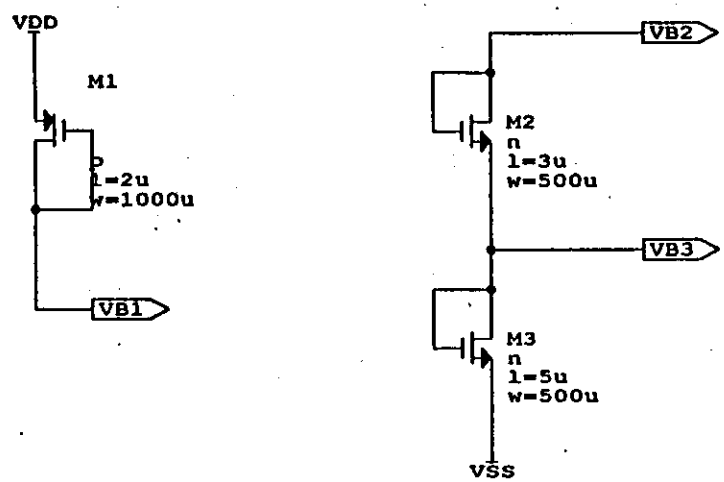

Fig. 5

BROOKHAVEN NATIONAL LABORATORY INSTRUMENTATION DIVISION		
Title VB123		
Size A	Document Number IPC-HS-1-6	REV
Date: January 19, 1993	Sheet of	

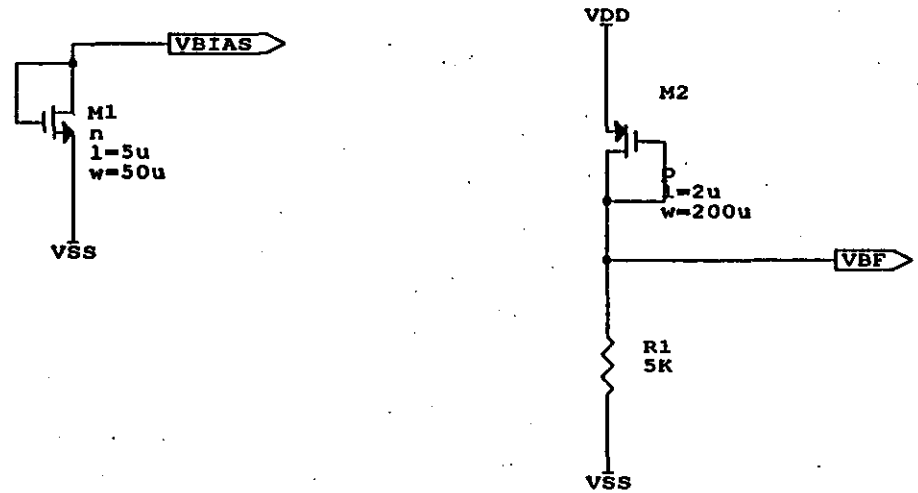

Fig. 6

BROOKHAVEN NATIONAL LABORATORY INSTRUMENTATION DIVISION		
Title VBIASF		
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Date: January 19, 1993	Sheet of	

$C_D = 35pF$

$C_{out} = 10pF$

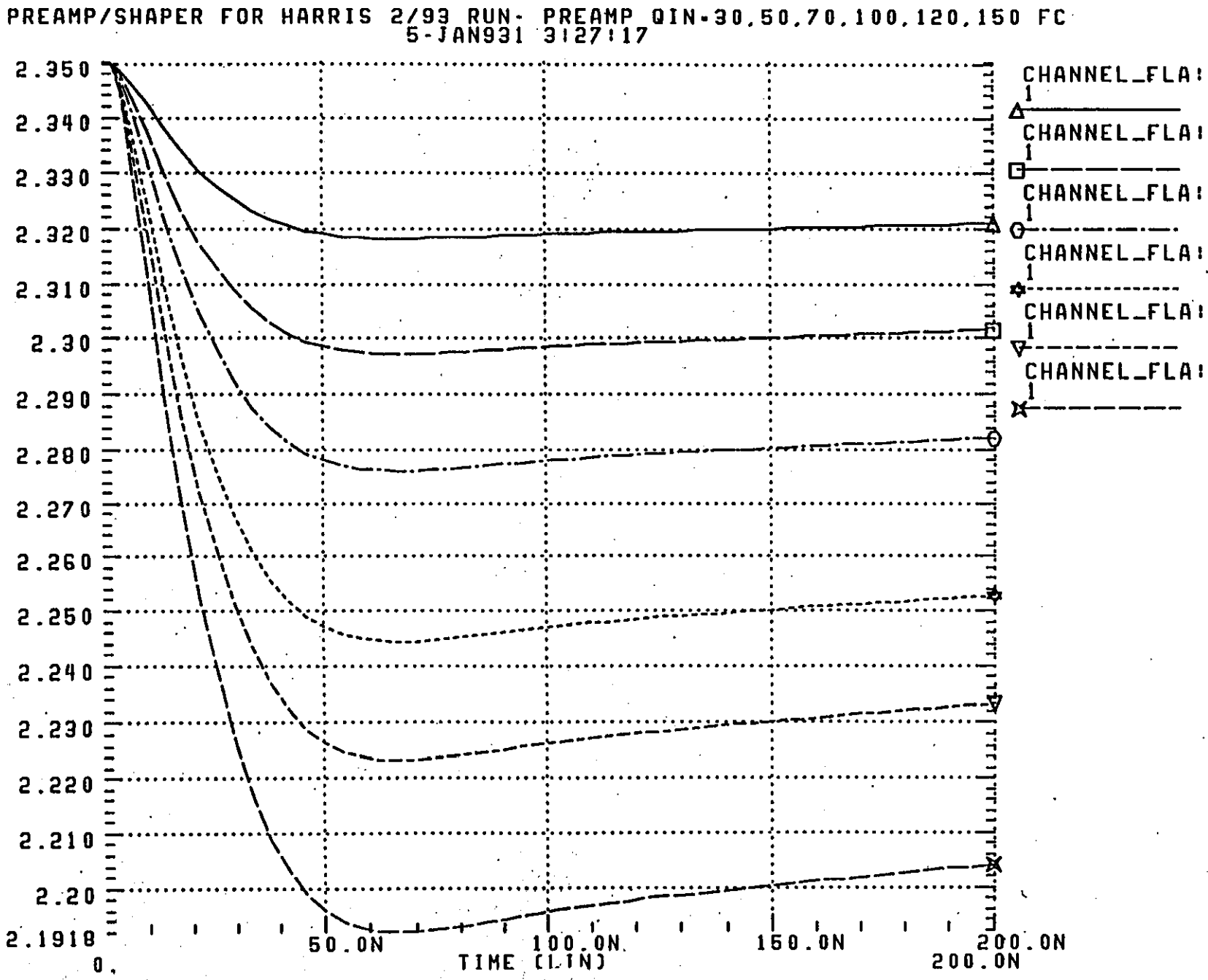

Fig. 7

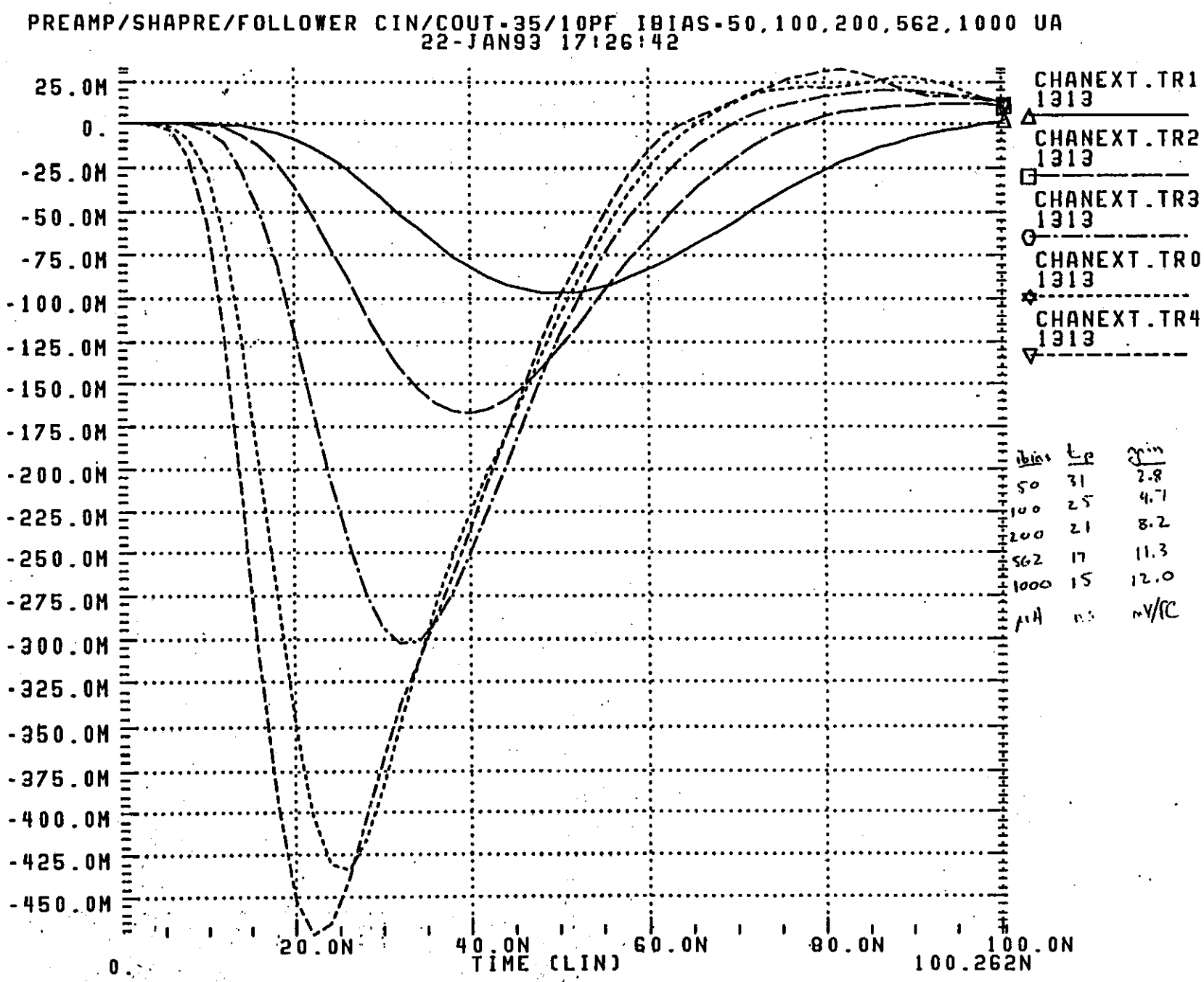
PREAMP/SHAPRE/FOLLOWER CIN/COUT=35/10PF IBIAS=50,100,200,562,1000 UA
22-JAN93 17:26:42
25.0M
0.
-25.0M
-50.0M
-75.0M
-100.0M
-125.0M
-150.0M
-175.0M
-200.0M
-225.0M
-250.0M
-275.0M
-300.0M
-325.0M
-350.0M
-375.0M
-400.0M
-425.0M
-450.0M
VOLT LIN
0.
20.0N
40.0N
60.0N
80.0N
100.0N
100.262N
TIME (LIN)
CHANEXT.TR1
1313
CHANEXT.TR2
1313
CHANEXT.TR3
1313
CHANEXT.TR0
1313
CHANEXT.TR4
1313
ibias tp gain
50 31 2.8
100 25 4.7
200 21 8.2
562 17 11.3
1000 15 12.0
μA ns mV/fC

Fig. 8

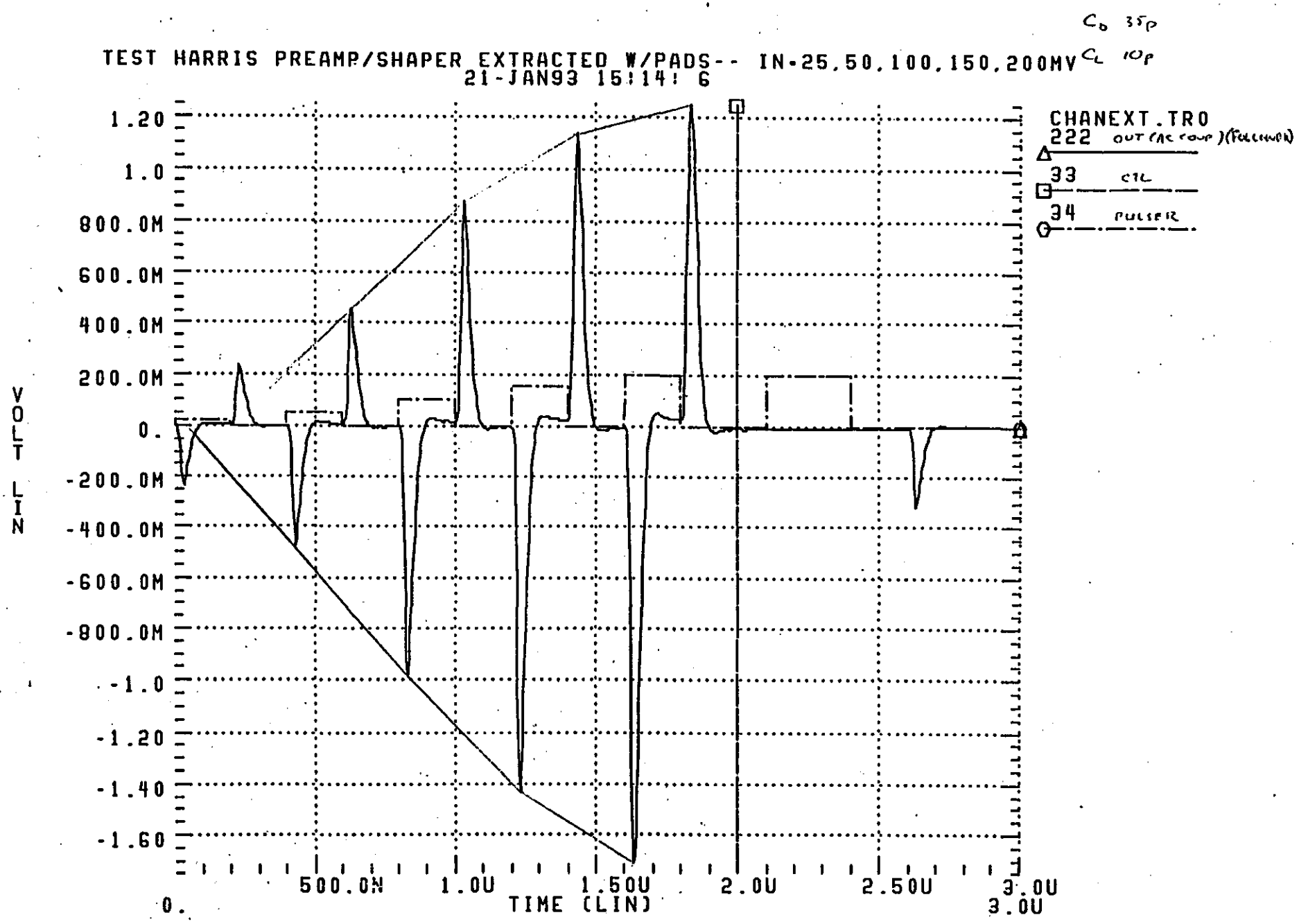
C_D 35p
C_L 10p
TEST HARRIS PREAMP/SHAPER EXTRACTED W/PADS-- IN-25,50,100,150,200MV
21-JAN93 15:14: 6
CHANEXT.TRO
222 OUT (AC COUP) (FOLLOWER)
33 CTL
34 PULSER
1.20
1.0
800.0M
600.0M
400.0M
200.0M
0.
-200.0M
-400.0M
-600.0M
-800.0M
-1.0
-1.20
-1.40
-1.60
VOLT LIN
0.
500.0N
1.0U
1.50U
2.0U
2.50U
3.0U
3.0U
TIME (LIN)

Fig. 9

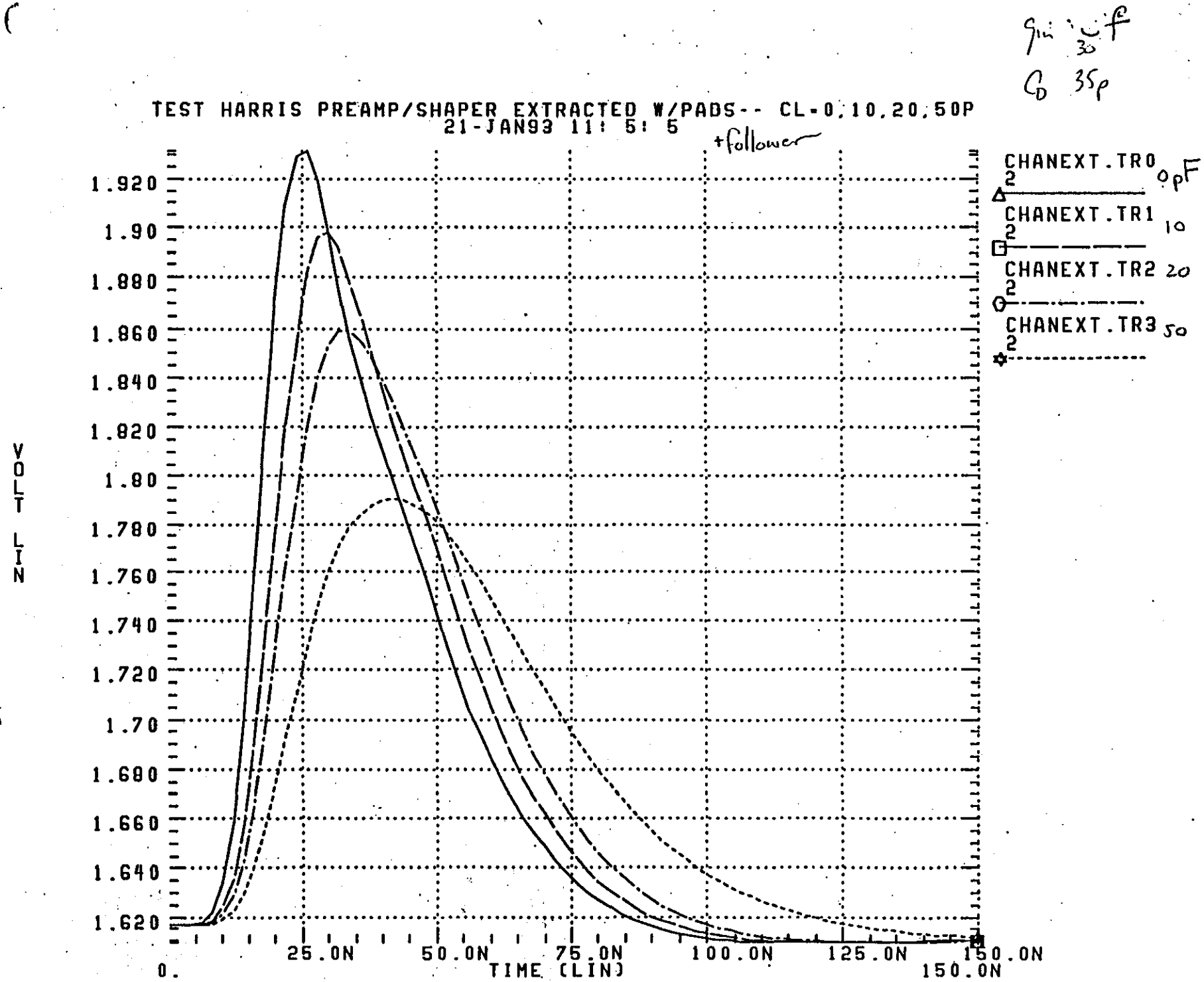
TEST HARRIS PREAMP/SHAPER EXTRACTED W/PADS-- CL=0,10,20,50P
21-JAN93 11: 5: 5
+follower
CHANEXT.TR0 0pF
CHANEXT.TR1 10
CHANEXT.TR2 20
CHANEXT.TR3 50
VOLT LIN
1.920
1.90
1.880
1.860
1.840
1.820
1.80
1.780
1.760
1.740
1.720
1.70
1.680
1.660
1.640
1.620
0.
25.0N
50.0N
75.0N
100.0N
125.0N
150.0N
150.0N
TIME (LIN)

Fig. 10

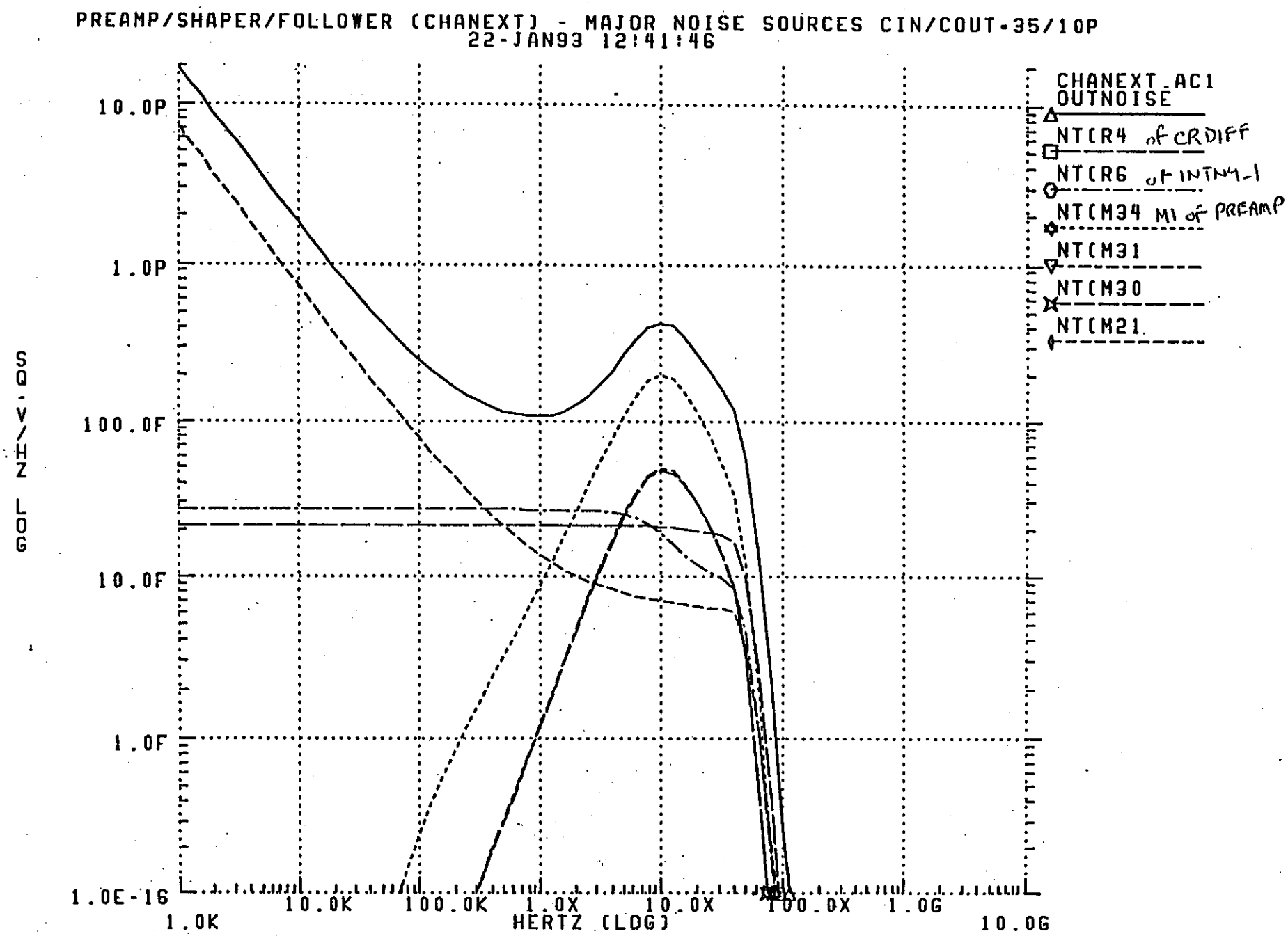
PREAMP/SHAPER/FOLLOWER (CHANEXT) - MAJOR NOISE SOURCES CIN/COUT=35/10P
22-JAN93 12:41:46
CHANEXT.AC1
OUTNOISE
NT(R4 of CRDIFF
NT(R6 of INTN4-1
NT(M34 M1 of PREAMP
NT(M31
NT(M30
NT(M21
10.0P
1.0P
100.0F
10.0F
1.0F
1.0E-16
SQ.V/HZ LOG
1.0K
10.0K
100.0K
1.0X
10.0X
100.0X
1.0G
10.0G
HERTZ (LOG)

Fig. 11

Q_{in} = 30fC
C_L = 10pF
C_D = 35pF

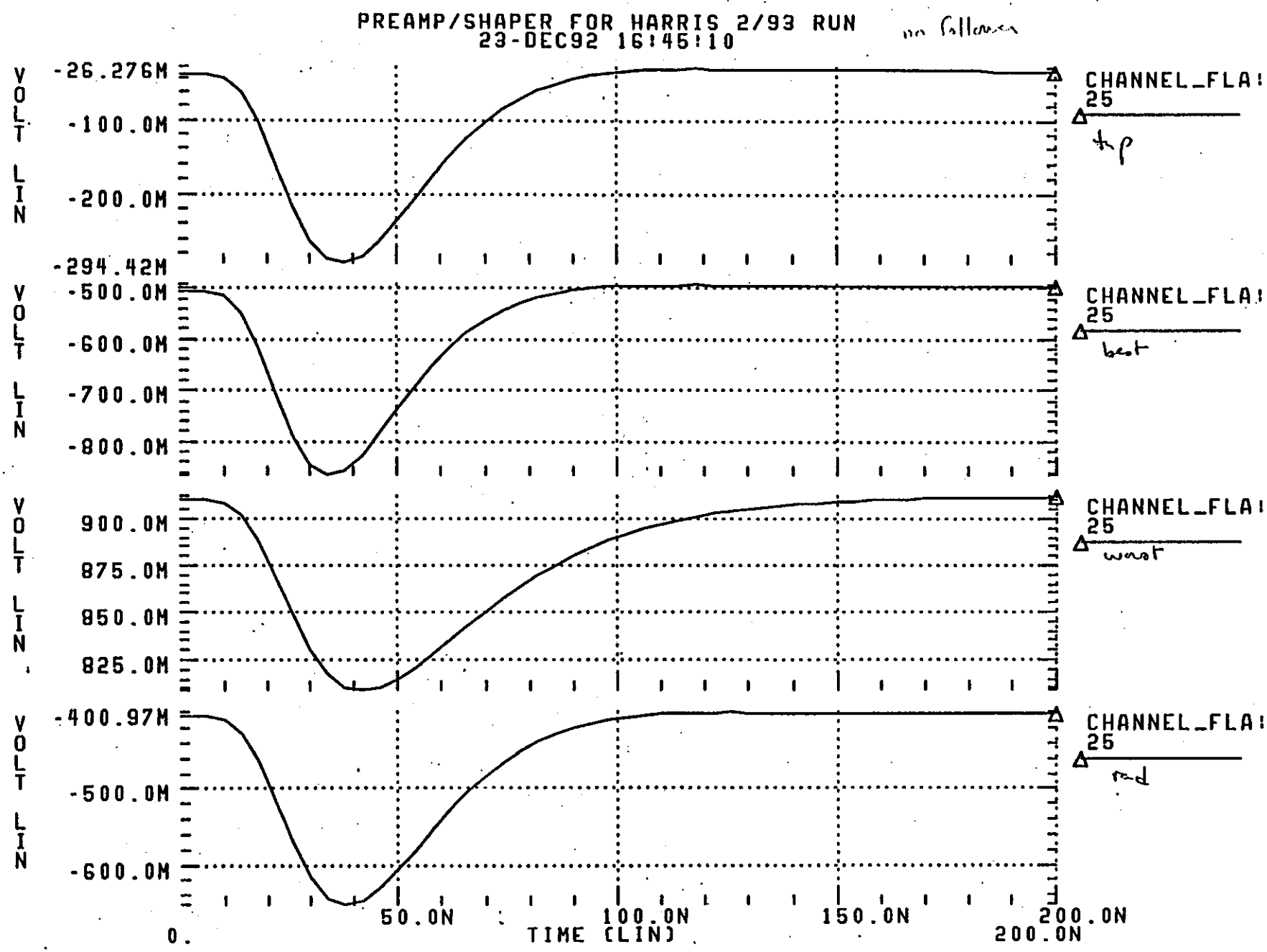

Fig. 12

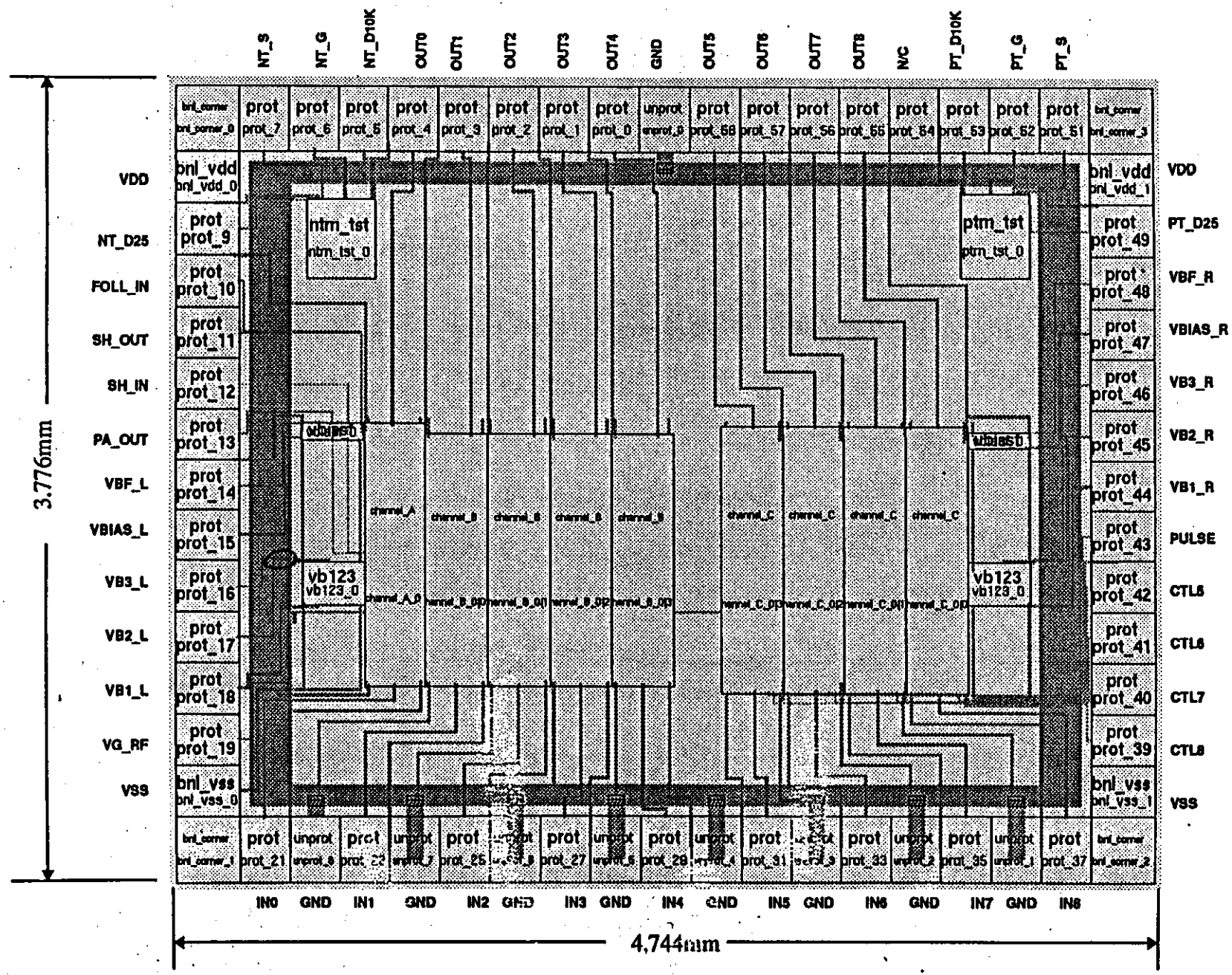
NT_S
NT_G
NT_D10K
OUT0
OUT1
OUT2
OUT3
OUT4
GND
OUT5
OUT6
OUT7
OUT8
N/C
PT_D10K
PT_G
PT_S
VDD
NT_D25
FOLL_IN
SH_OUT
SH_IN
PA_OUT
VBF_L
VBIAS_L
VB3_L
VB2_L
VB1_L
VG_RF
VSS
PT_D25
VBF_R
VBIAS_R
VB3_R
VB2_R
VB1_R
PULSE
CTL5
CTL6
CTL7
CTL8
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
3.776mm
4.744mm

Fig. 13