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CSC Barrel Timing and Staggering

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Abstract:

Timing characteristic of CSC barrel was investigated as a function of incident angle and number of layers. The result shows staggering is necessary to get 100% trigger efficiency.

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1. PURPOSE

In CSC, if wire spacing = 2.5mm and drift velocity = 50mm/μs, the range of drift time $T_{d,max}$=25ns > 16ns. Is it possible to get the earliest signal from the 6 layers with $T_{d,min}$ < 16ns for 100% of the tracks? There have been some works on the timing capability of CSC endcap and barrel. They investigated the integral timing characteristic in the full range of incident angle. Here we try to investigate the timing characteristic as a function of incident angle and find the best wire staggering scheme for the baseline.

2. THE SIMULATION

In the simulation, 10000 tracks were generated which uniformly distributed over $2^0 < \phi < 12^0$ and $0.10 < \eta < 1.33$ ($29.5^0 < \theta < 84.3^0$). Because the chamber tilted an angle of 8^0 or 6^0, the radially incident tracks have $\phi = 6^0$ or 8^0. MWPC type electric field and ionization clustering were considered. Uniform drift velocity of 50mm/μs and a Lorentz angle of 8^0 were taken. The intersection on layer 1 was randomly distributed within +/-SPACING.

In staggering scheme A, the wires of all 6 layers are aligned. Its overall timing behavior is shown in Fig. 1. The number near the curves represent the number of layers used for extracting the minimum drift time $T_{d,min}$. Fig. 2 shows the percentage of tracks with $T_{d,min}$ > 16ns (inefficiency). The result of outer superlayer is basicly the same.

3. STAGGERING IS NECESSARY

Fig. 3 a),b) show that the tracks with $T_{d,min}$ > 16ns mainly come from some specific discrete θ angles and when the tracks pass through around the middle of two wires in the first layer. Fig. 3 c) shows their correlation. The inefficiency is appreciable at these points (Fig. 4) and it is independent of ϕ angle.

It can be explained as follows. If the wires of the 6 layers are all aligned, they form a 'crystalline'. At certain incident angles, a track passing through

the middle of two wires in the first layer will pass through the middle of wires in all 6 layers. The $T_{d,min}$ will exceed 16ns. Therefore wire staggering is necessary. The principle of choosing staggering configuration is RANDOM.

4. OPTIMIZING THE STAGGERING CONFIGURATION

According to the result of a previous simplified study, we chose a configuration G with wire bias of (0, 0, 0.5, 0, 0.5, 0.5)*wire spacing. The overall timing behavior is shown in Fig. 5. For both middle and outer superlayers, when the Td,min is extracted by using 4, 5 or 6 layers, the inefficiency will be 0%. Comparing to Figs. 1 and 2, there is an apparent improvement.

5. WIDER SPACING

A wider spacing of 3mm was tried aiming to reduce the wire number. The timing of configuration G with 3mm spacing (Fig. 6) is still better than that of configuration A with 2.5mm spacing.

A previous study also show that:

(1) the results for GAP=5mm and GAP=4mm are identical,

(2) configuration B (0, 0.33, -0.33, 0, -0.33, 0.33) is the best one, which works even at spacing=3.5mm, while G is easier in manufacturing,

This calculation concerns only the CSC timing performance, not the space resolution. They should be considered coherently.

Ya-nan GUO

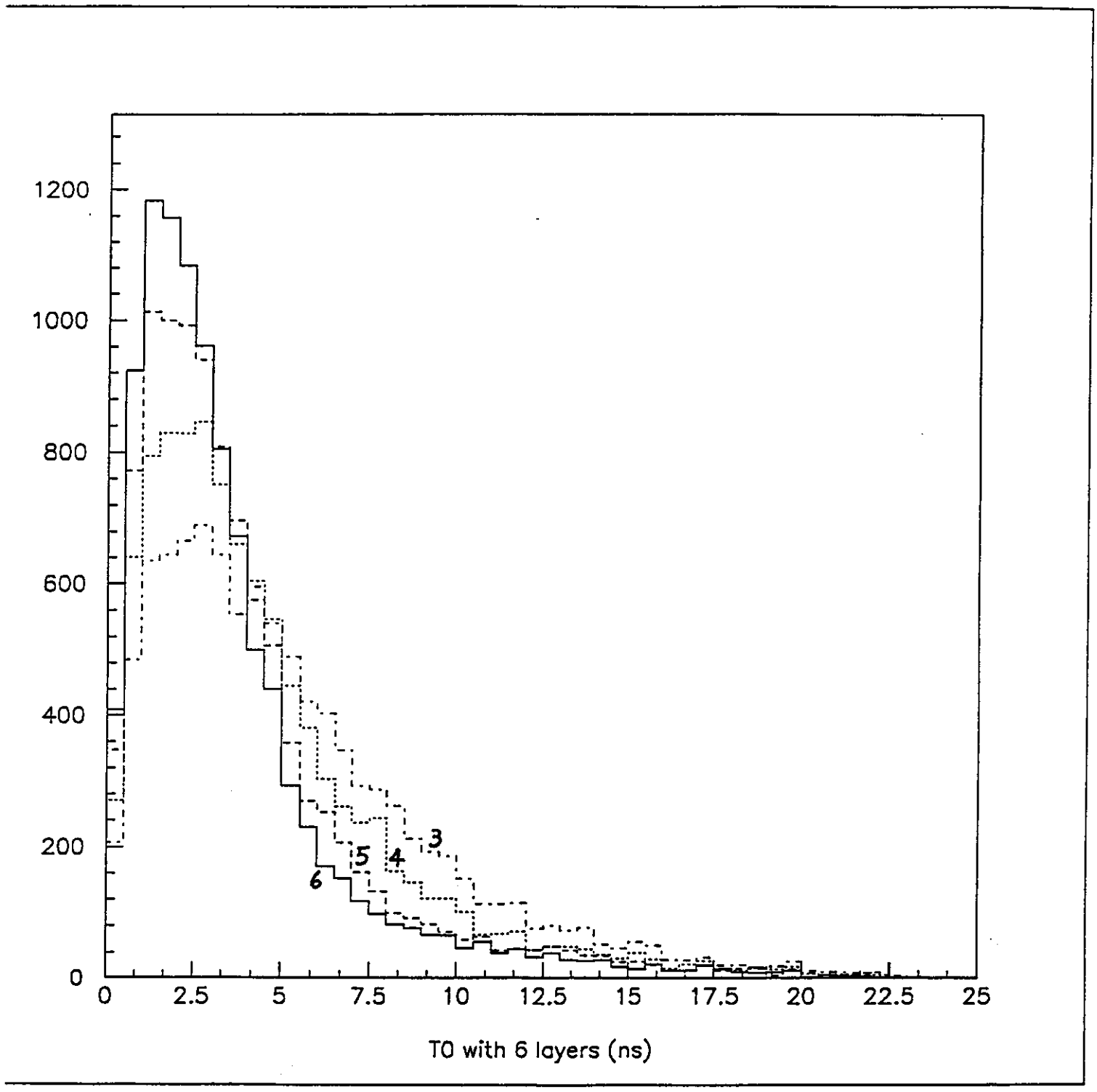

1200
1000
800
600
400
200
0
0
2.5
5
7.5
10
12.5
15
17.5
20
22.5
25
T0 with 6 layers (ns)
3
4
5
6

Fig. 1

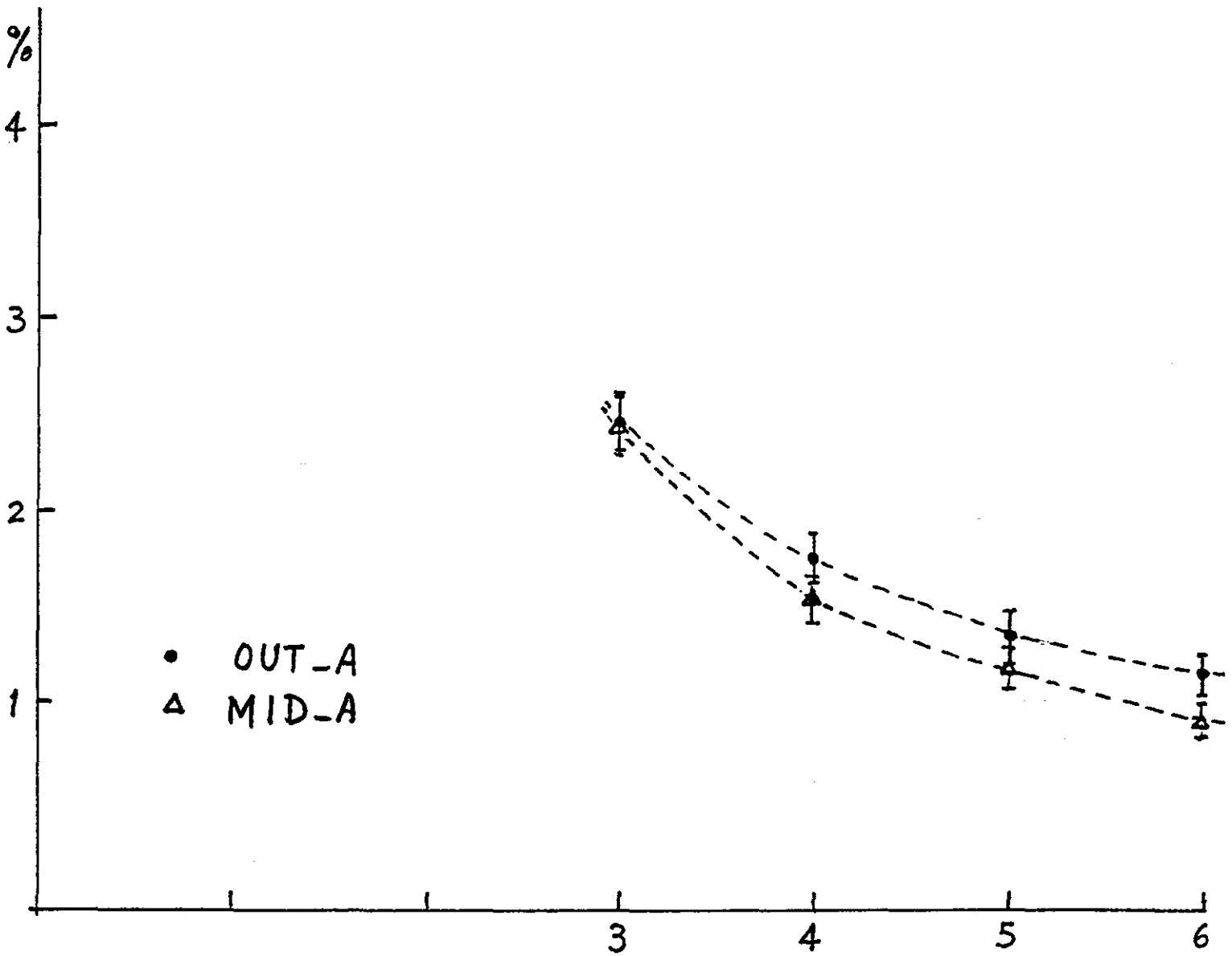


Fig. 2 # of Layers

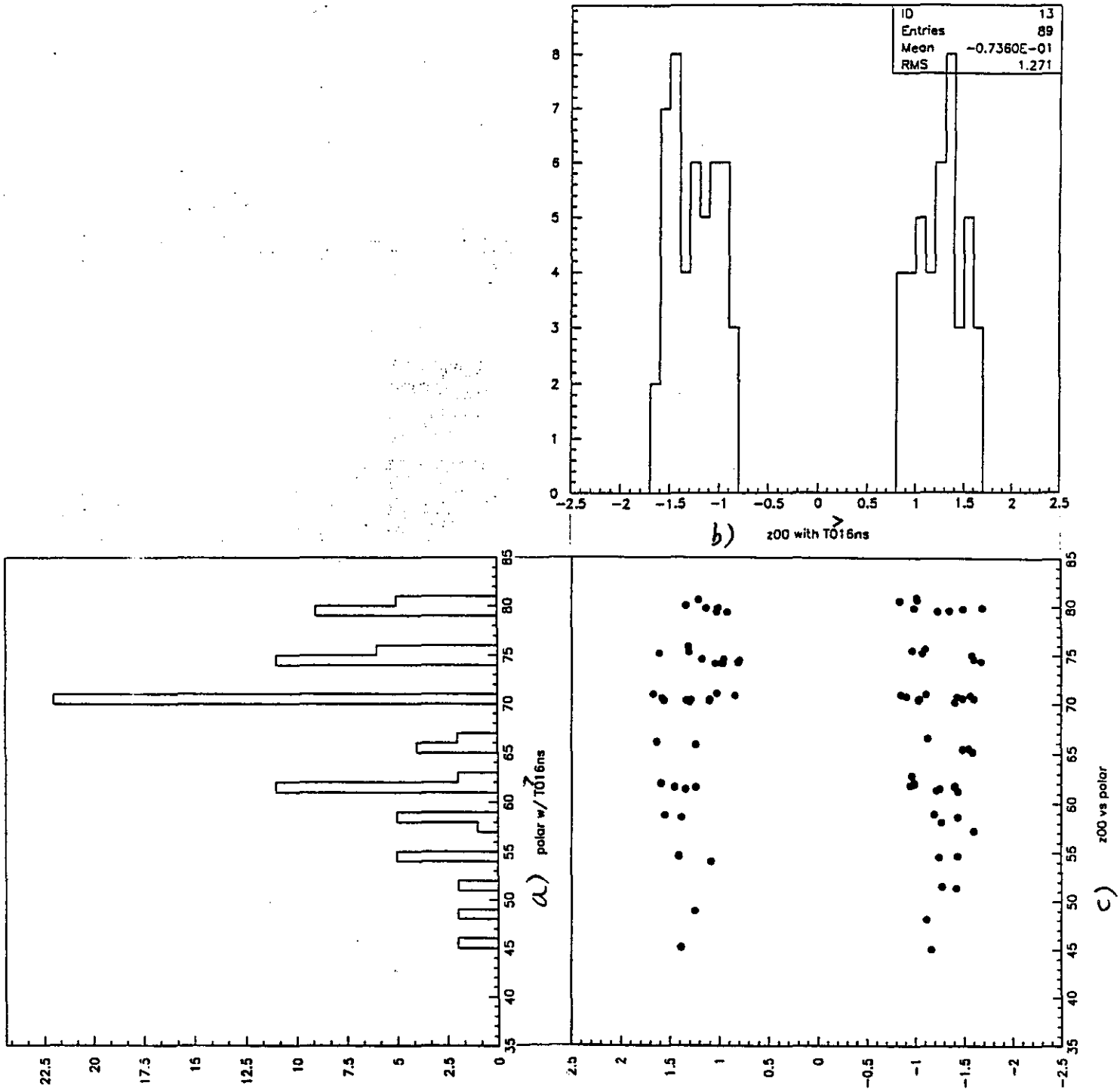

ID 13
Entries 89
Mean -0.7360E-01
RMS 1.271
b)
z00 with T016ns
a)
polar w/ T016ns
c)
z00 vs polar

Fig. 3

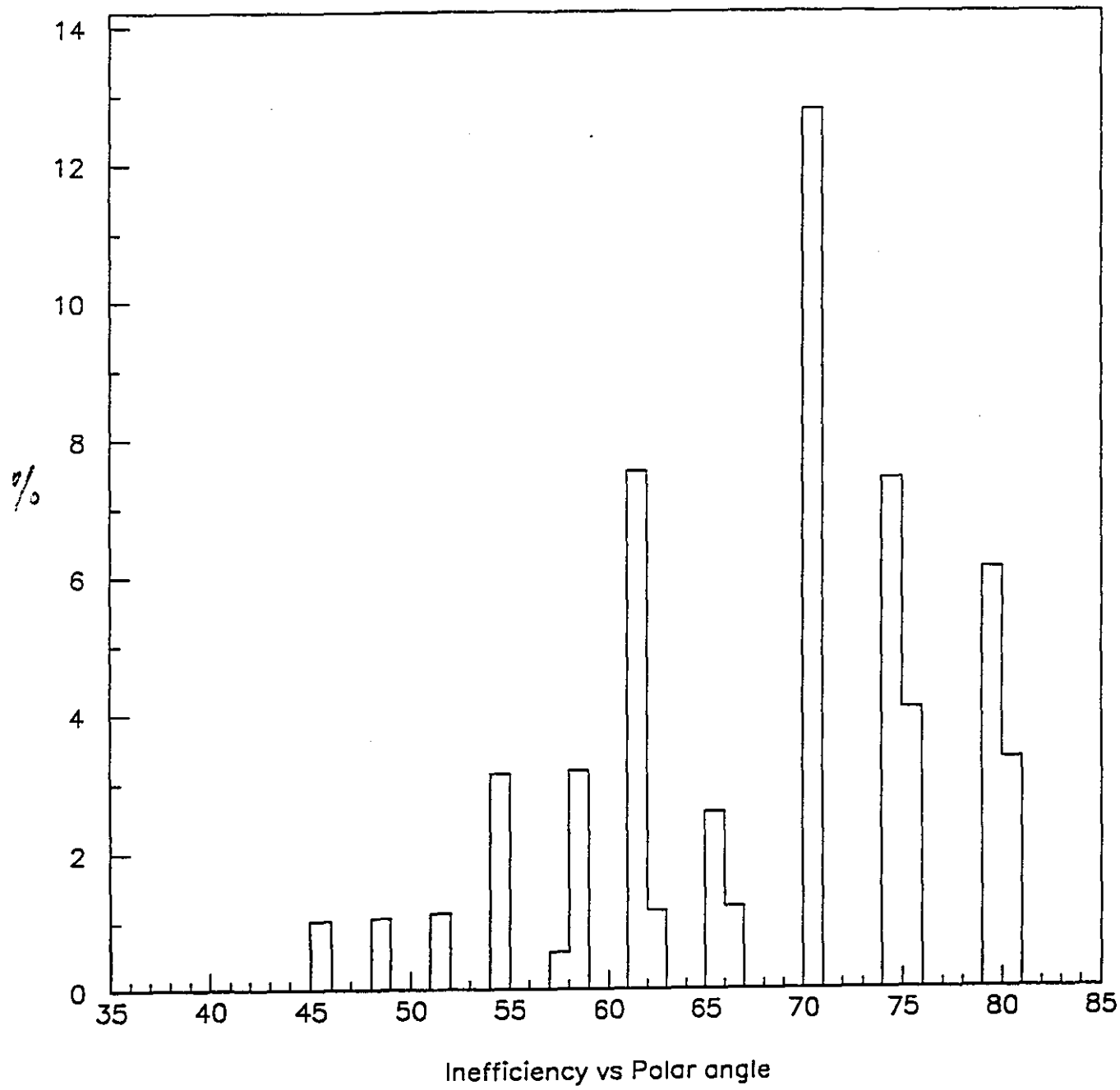
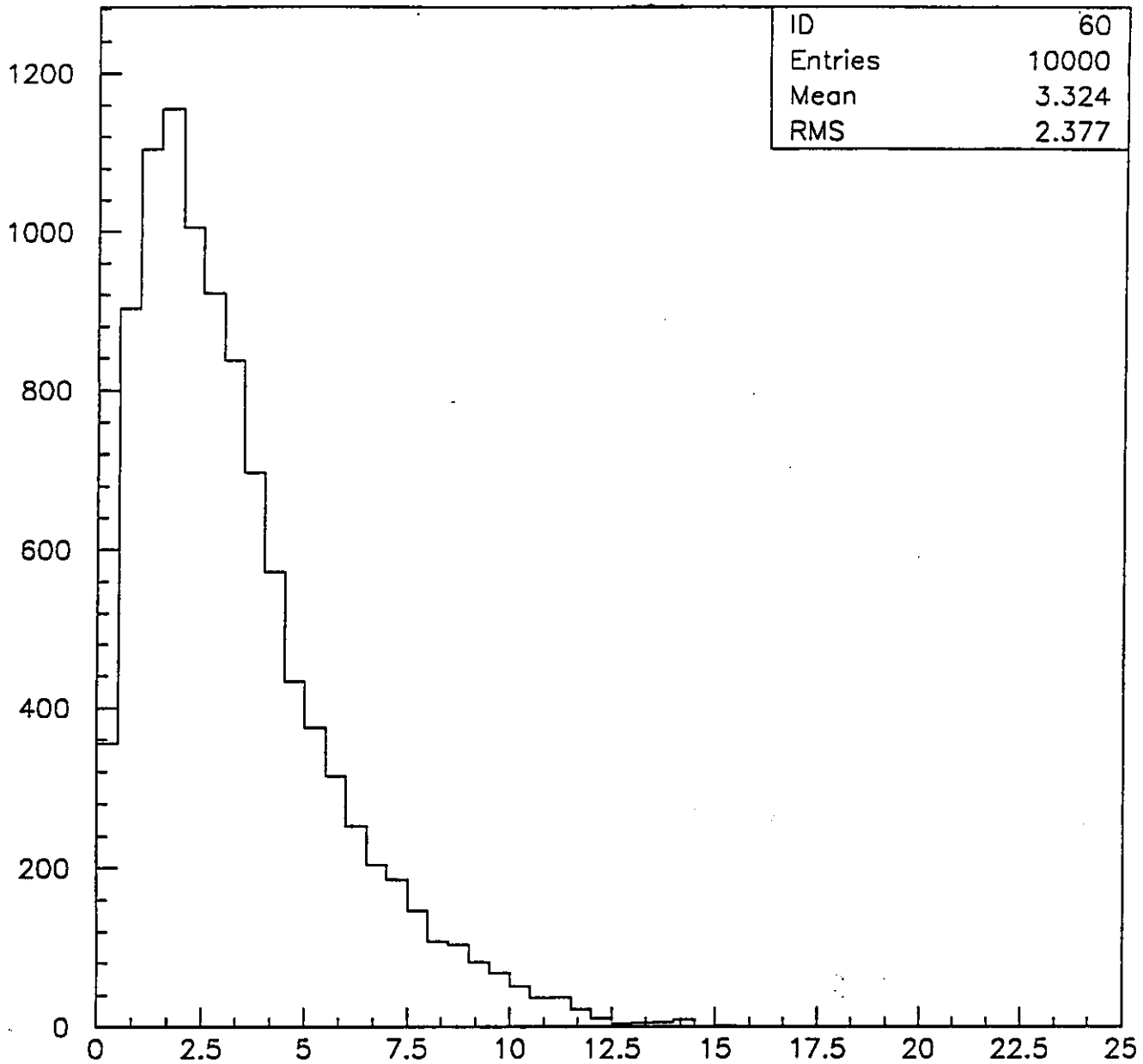

14
12
10
8
6
4
2
0
%
35
40
45
50
55
60
65
70
75
80
85
Inefficiency vs Polar angle

Fig. 4



a) T0 with 6 layers (ns)

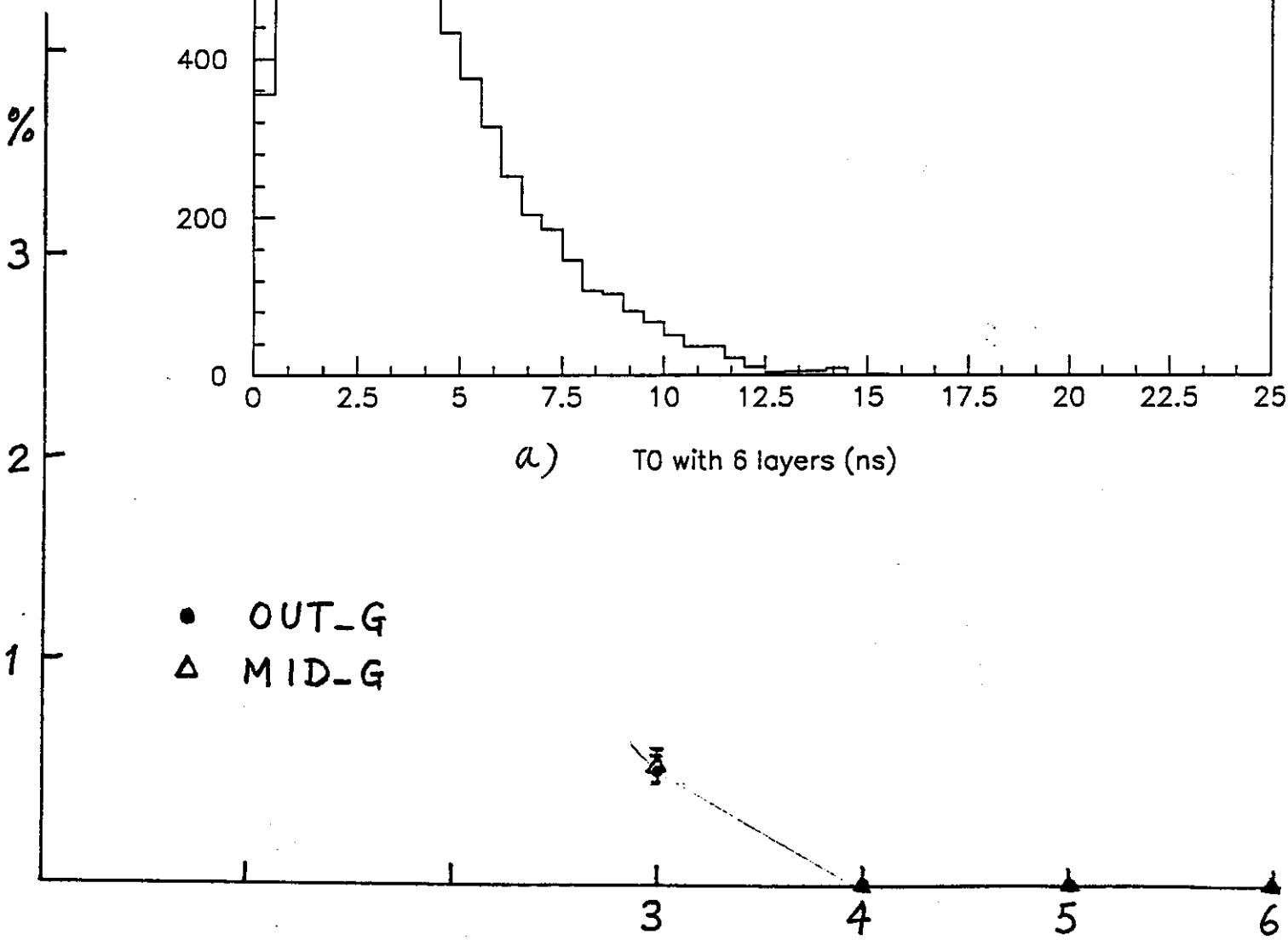


Fig 5 b) # of Layers

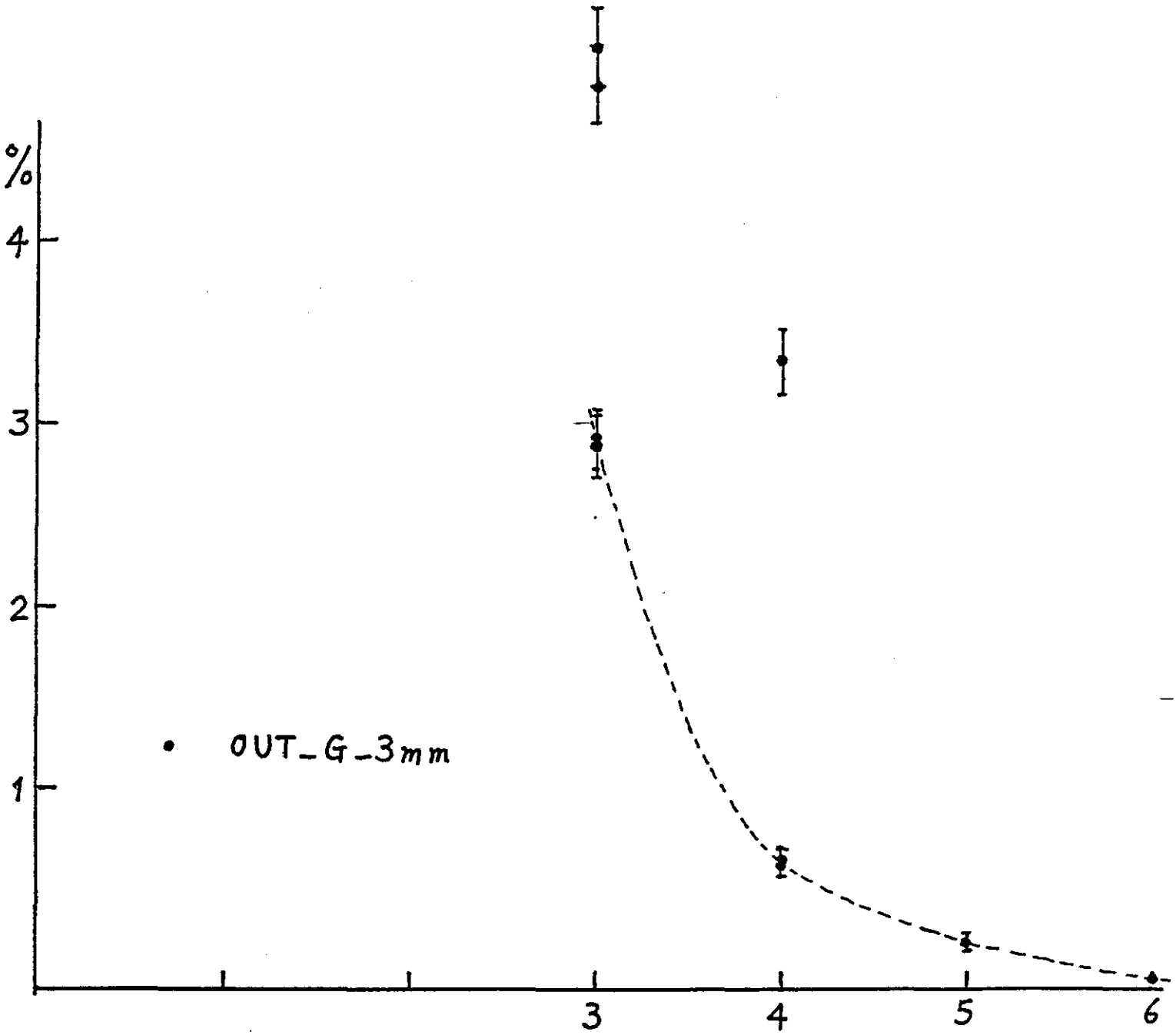


Fig. 6 # of Layers