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ADC Device Report: HS9008RH

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January 26, 1993

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This document presents results from tests performed on the HS9008RH ADC. These tests were performed primarily to evaluate the suitability of this device for use in the GEM Central Tracker at the SSC experiment. Basic performance characteristics and susceptibility of these characteristics to radiation were examined. Results indicate that the device is radiation hard to 6 Mrad of 1.25 MeV γ radiation from a ^{60}Co source with no degradation in performance, but that the base performance of the device worsens rapidly above a sampling rate of 15 MSPS. A description of the tests is found in the write-up "A Guide to the Ames ADC Tests, Version 2.0", IS-5086, available from the Ames Laboratory High Energy Physics group, 12 Physics, Iowa State University, Ames, Iowa, 50011 USA.

ADC Device Report

HS9008RH

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Manufacturer: Harris Semiconductor
Lot No.: DV SAMPLE T22816-0
Manufacturer's Serial Nos: 50, 51, 53, 54, 55
Dates of Tests: December 15, 1992 – January 10, 1993
Date of Report: January 26, 1993

ABSTRACT

This document presents results from tests performed on the HS9008RH ADC. These tests were performed primarily to evaluate the suitability of this device for use in the GEM Central Tracker at the SSC experiment. Basic performance characteristics and susceptibility of these characteristics to radiation were examined. Results indicate that the device is radiation hard to 6 Mrad of 1.25 MeV γ radiation from a ^{60}Co source with no degradation in performance, but that the base performance of the device worsens rapidly above a sampling rate of 15 MSPS. A description of the tests is found in the write-up "A Guide to the Ames ADC Tests, Version 2.0", IS-5086, available from the Ames Laboratory High Energy Physics group, 12 Physics, Iowas State University, Ames, Iowa, 50011 USA.

1 Device Description

The HS9008RH is an eight-bit conventional flash analog-to-digital convertor (FADC) rated at a maximum sampling rate of 25 megasamples per second (MSPS). It is fabricated in a radiation hard process called AVLSIIRA by the manufacturer and described as a "dual level, twin well, thin EPI, 1.25 μm bulk CMOS process". It operates with a single fixed reference voltage, although a tap point at midscale is provided. The device requires a single +5V supply for power. All output signals are TTL compatible.

2 Evaluation Board Description

The device was tested with an evaluation board designed and built at the University of Michigan. The input signal was unbuffered and the ADC outputs were translated from TTL to ECL levels on the evaluation board. A digital-to-analog convertor (DAC) provided an analog signal for monitoring.

3 Test Conditions

We tested the device at the following sample rates: 10, 15, 20, and 25 MSPS using a symmetric clock. Some additional tests were performed on serial numbers (S/N) 50 and 51 at 17.5 MSPS. Not all tests were done at all sample rates. For these tests the device was biased such that the input signals were kept within the range of 0.0 to 2.5 V. The data record length was 1024 samples and the analysis window covered samples 8 to 1022, inclusively. The midscale tap point was not used to set a bias, but tests showed that a 15μF capacitor improved the integral non-linearity (INL) near the tap point. Attempts to decrease the INL by tuning the tap point changed the shape of the FADC response but not the magnitude of the INL.

4 Results

At the start of testing the Harris Corporation had not completely tested the device at sample rates greater than 10 MSPS. The results of these tests were a surprise to them, and they performed their own similar tests to confirm our results. Recent communications with Harris indicate that they have obtained similar results.

Many of the results are shown in the accompanying set of figures. A description and outline of these results follows.

4.1 Linearity

This device showed very peculiar behavior in the DC tests. At 10 MSPS it had excellent linearity, both integral and differential. As we progressed to 15, 20 and 25 MSPS the shape changed dramatically and the worst case INL climbed to more than 1 percent of full scale. This can be seen in the ten-plot figure, which shows the difference between the data and a linear fit (figure 1). At 25 MSPS the worst values are wrong by more than 3.0 least significant bits (lsb), equivalent to one count or "code." Close examination of the plots shows clearly that the response curve is broken into four very linear quadrants at each sample rate. This effect should be possible to correct for in software. However, since at each sampling rate the response shape is different, the response curves at the particular operating sample rate must be measured to insure proper correction. This limits the use of the FADC to the few measured sample rates.

The rms width of the codes was about 0.20 lsb (figure 2). However, a histogram of the 255 widths shows strong spikes which became very pronounced as the sampling rate increases (figure 3).

The differential nonlinearity was excellent at low sampling rates and stayed that way for most codes even up to 25 MSPS. However, at the higher sampling rates a few codes, usually near a quadrant boundary, became bad and drove the worst case differential non-linearity (DNL) up to about 1 lsb.

Despite this low DNL, the INL increased dramatically with sample rate due to the arrangement of the DNL. Within each quadrant the code widths were very uniform, but there was a significant variation of the average width from quadrant to quadrant. A string of narrower than average codes accumulated over one quadrant are corrected for by a string of wider than average codes in another quadrant. The INL clearly shows the quadrant to quadrant average code width variations.

No problems were observed with monotonicity or hysteresis.

4.2 Resolution

The number of effective bits was 7.9 for a low frequency input at 10 MSPS and decreased to about 6.0 at 25 MSPS for all input frequencies. The measured effective bits at the higher sampling rate are limited by the increasing nonlinearity discussed in the previous section. We also observed a loss of resolution with increasing signal frequency for fixed sample rate. This behavior is normal for flash ADCs, but the size of the effect was larger than for many other devices tested. We also observed that the total harmonic distortion became worse (i.e. the THD parameter decreased) at higher sample rates (figure 4). Since the ratio of input frequency to sample rate is held constant, a higher sample rate means a higher input frequency, so this decrease in THD is related to the loss of effective bits with increasing frequency.

The random noise from the triangle test was extremely low, less than 0.1 lsb (figure 4) at all sampling rates.

4.3 False Codes

The qualified error level for this device was set to 2 counts, which means that steps of three or more counts were flagged as errors. We ran the word error rate test (figure 4) with an automatic stop at 100 errors or 2.0×10^7 samples, whichever came first. If no errors were found, we assumed 1 ± 1 error(s) within the number of samples taken. At low sample rates there were

no word errors, but at 20 MSPS and above errors began to appear. A brief attempt to clock the chip at 30 MSPS (above the rated specification of 25 MSPS maximum) resulted in a 50% word error rate. In general, the errors were spread evenly among the ADC codes, but the size of the errors clustered around values that are powers of two (figure 5), suggesting an incorrect bit in the answer to be the cause of the error.

One of the devices (S/N 51) had a weak code (number 69), which got worse as the sampling rate increased. At 25 MSPS this code was effectively dead and caused a large word error rate. An estimate of the word error rate could still be obtained by setting the qualified error level (QEL) flag to 3 counts, eliminating the errors flagged when the bad code was skipped. With the increased QEL the word error rate was comparable to that of the other devices.

4.4 Analog Bandwidth

The analog bandwidth test was done only at 10 MSPS and showed the gain to be constant to within ten percent up to a 5 MHz input signal frequency. (Note: 5 MHz is the Nyquist frequency for 10 MSPS. Higher input frequencies are not sampled frequently enough for tests utilizing a sine wave input to be meaningful.)

4.5 Transient Response

The short term settling time at 25 MSPS was measured to be less than 70 ns. This must be treated as an upper bound because of limitations on the step signal source.

The maximum slew rate observed was 51 mV/ns. This should be regarded as a lower bound on the true value.

Sampling time jitter was measured at the 10 MSPS rate only due to the inability to fit a clean sine wave to the output at faster sampling rates (larger

INL). The measurment places an upper limit of 0.337 ns on the sampling time jitter.

The overvoltage recovery time was not measured due to technical difficulties with the test setup. However, observations from other tests indicate that the device recovers from slight ($\approx$ 10-20 mV) overvoltage within one sample period.

4.6 Power Consumption

The power consumption of the chips was measured to see the effect of sample rate and radiation dose as well as quantify chip–to–chip variations. Power was measured by monitoring the voltage drop V_R across a precision 2Ω resistor placed in series with the 5V power supply voltage. The power consumption of the chip was then determined as $P = (5 - V_R)V_R/2$. For the five chips purchased, the average power required at 15 MSPS with a sine wave input covering the 10% to 90% code levels was 406.1 ± 22.2 mW (figure 6). Power consumption is very linear with sample rate between 10 and 25 MSPS (figure 7).

5 Radiation Tests

Two of the devices were tested for radiation hardness utilizing a ^{60}Co source at the University of Michigan Pheonix Reactor. This source is able to deliver 2 Mrad per hour of radiation consisting chiefly of 1.25 MeV gamma rays. Tests were conducted at six irradiation steps: 0, 1.01. 2.04, 3.05, 4.24, and 6.0 Mrads.

The tests showed that the devices are quite radiation hardened. They were able to withstand 6 Mrad of radiation without significant degradation. The performance of the device showed essentially no change after each irradiation step. If anything, the argument could be made that performance improved after 1 Mrad, then settled back to its original value after 2 Mrad.

The SSC environment around the GEM central tracker at 40 cm radius is expected to receive 0.5 Mrad per SSC year. These devices are capable of working with no degradation for at least 12 SSC years at low luminosity ($10^{33}/cm^2/s$) or slightly more than one year at high luminosity ($10^{34}/cm^2/s$).

The power consumed by the chip did not change significantly with exposure to radiation. Figure 8 shows measurements of the power consumption of chip 50 with increasing dose.

Both the effective bits and the total harmonic distortion were measured as as function of radiation dose. No changes were observed. Note that at higher sampling rates both of these parameters are limited by the INL.

It is extremely significant that the word error rate did not increase with radiation dose. Also, for chip S/N 51, no change in the behavior of the bad code was noticed as dose level increased.

6 Conclusion

At 10 MSPS this device performed excellently. The INL, DNL, and effective number of bits were outstanding and there were no false codes in 2.0×10^7 digitizations. By 25 MSPS, however, the performance was terrible. The INL was at the level of 3 lsb and the effective number of bits had dropped to 6.0. The false code rate had climbed to one error per 10^5 digitizations. While the change in measured INL between sample rates was fairly consistent between chips, the mode of the change followed no simple pattern. Therefore it is probably not possible to predict the INL for a particular sample rate from data of surrounding sample rates.

The device is incredibly radiation hard. It showed no significant changes in performance after 6 Mrads of 1.25 MeV γ radiation from ^{60}Co.

7 Future Tests

Sensitivity to neutron irradiation will be tested next. The Harris Corporation has been informed in the results of these tests and is looking into performing a redesign in order to eliminate or at reduce the dependence of the performance with sampling rate. If a redesign occurs, the new devices will be tested in the same manner as these have been, although it is clear from these tests that the AVLSIIRA process enables the device to withstand high ionizing radiation doses. Tests will continue using the ^{60}Cobalt source in radiation steps equivalent to one SSC year in the IPC region at the $10^{34}/cm^2/s$ high luminosity (5 Mrad/year).

Difficulties with the over-voltage recovery test must be overcome and this test performed.

Figure 1: The measured INL for HS9008 S/N 50 and 51 at 10, 15, 17.5, 20, and 25 MSPS in the DC tests. Note the changing response with sample rate.

Figure 2: Various measured parameters of the HS9008 S/N 51. *From top left:* Peak DNL (in lsb) as measured in the DC tests, peak DNL from the triangle wave tests, INL (DC tests) in lsb, RMS code width deviation (DNL), peak error in sine fit to a data record (normalized to 3 standard deviations), and a bound on the sampling time jitter.

Figure 3: A series of histograms of the 255 code widths measured in the DC tests at different sampling rates. Note how with increasing sampling rate the histograms develop sharper separate peaks.

Figure 4: Various parameters measured as a function of sampling rate for HS9008RH S/N 51. *From top left:* Total harmonic distortion (a larger value means less distortion), effective bits near Nyquist limit, random noise measurement with the triangle wave test (in lsb), and the word error rate (from 2×10^7 samples, zero errors plotted as $1/(2 \times 10^7)$.

Figure 5: Distribution of word error values. Note that values are clustered about powers of 2, suggesting that word errors are bit errors in the device.

Figure 6: Measured power consumption of the 5 purchased FADCs at 15 MSPS.

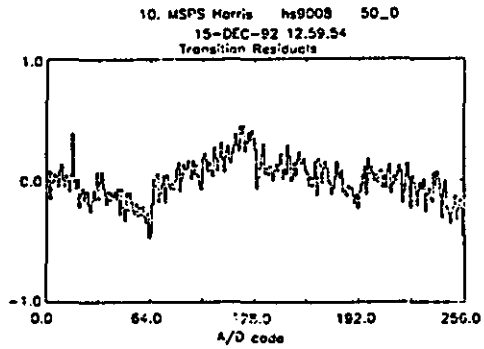
Figure 7: Power consumption as a function of sample rate with a sine wave input for S/N 50.

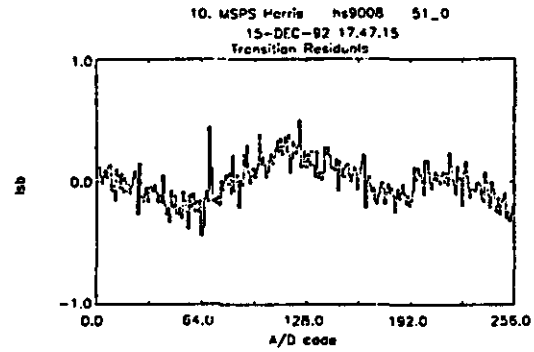
Figure 8: Power consumption as a function of radiation dose for S/N 50 with a sample rate of 15 MSPS and a 2 MHz sine wave input.

HS 9008

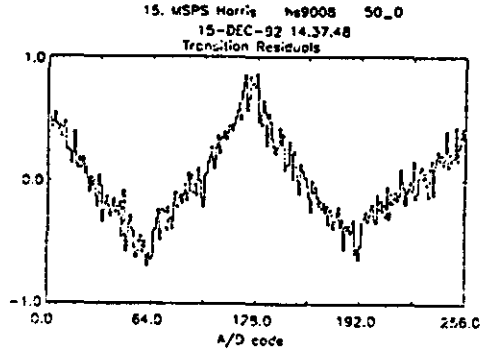
S/N 50 | S/N 51

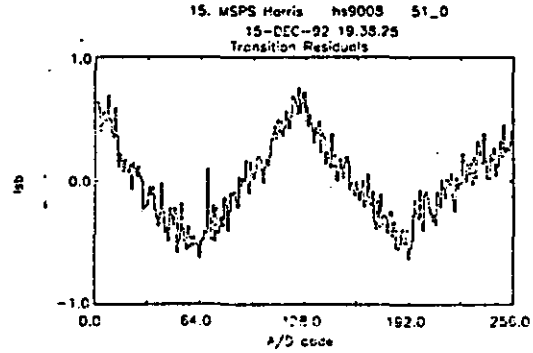
10 MSPS



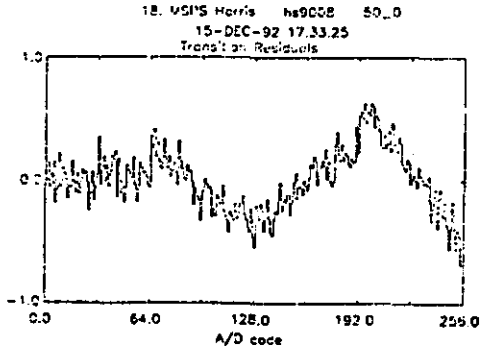


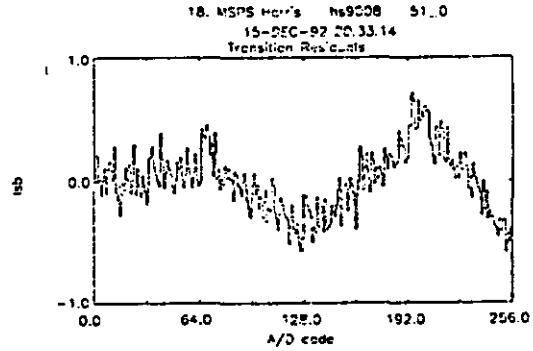
15 MSPS



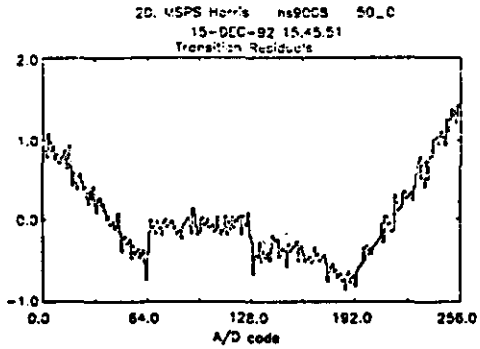


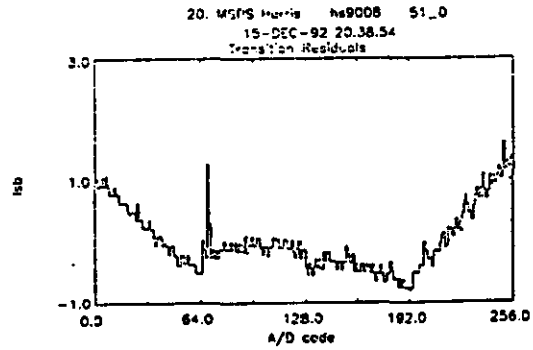
17.5 MSPS



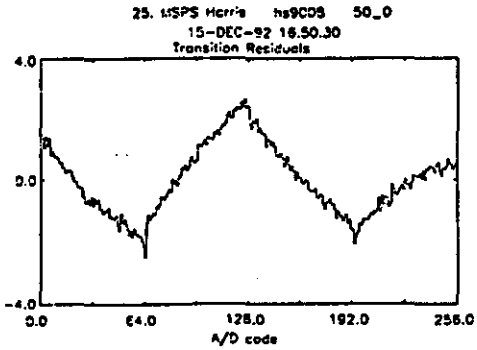


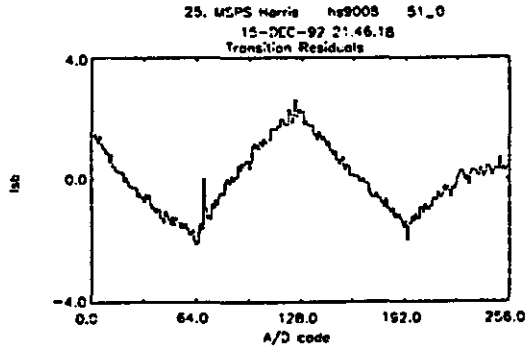
20 MSPS

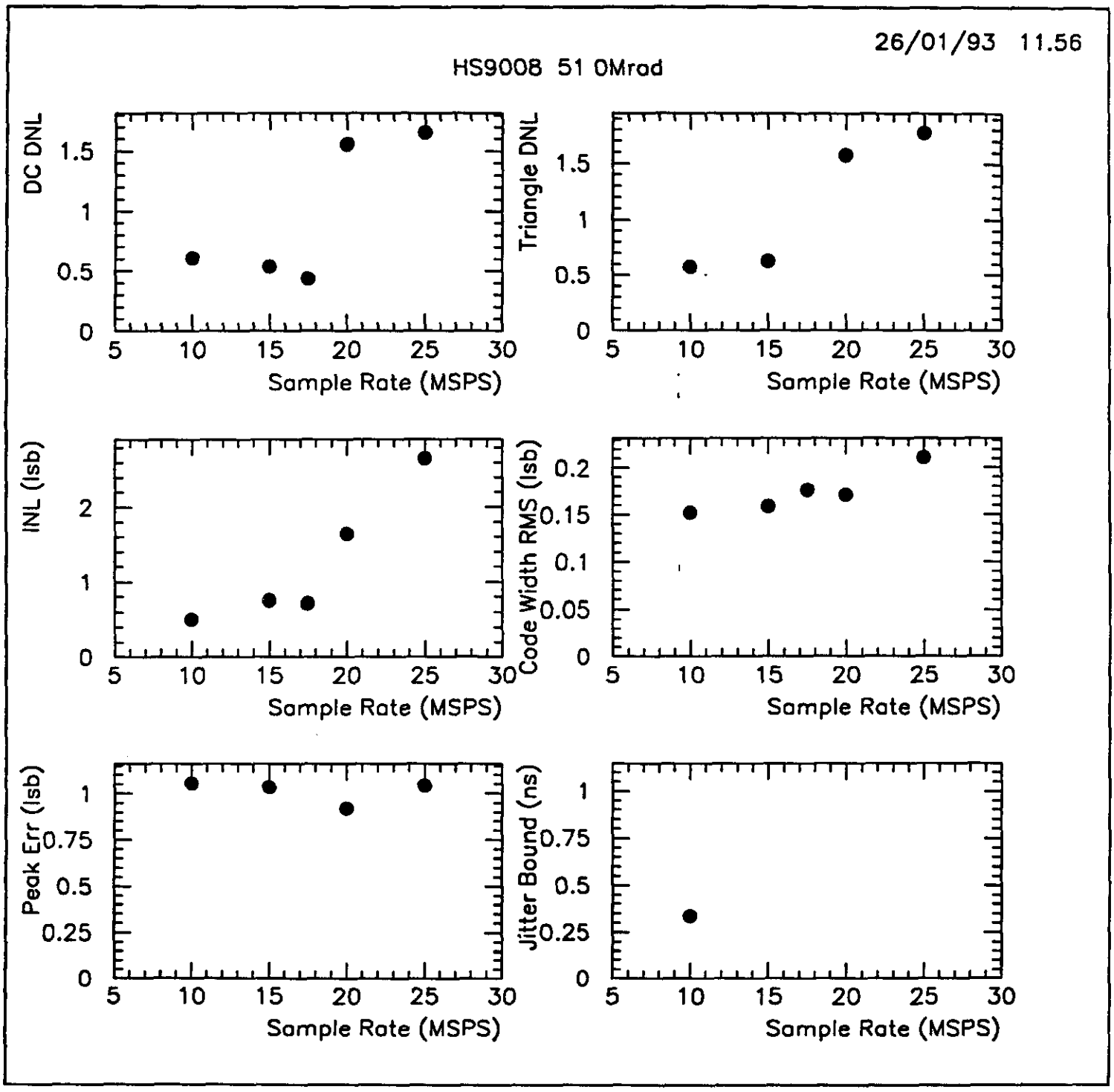




25 MSPS

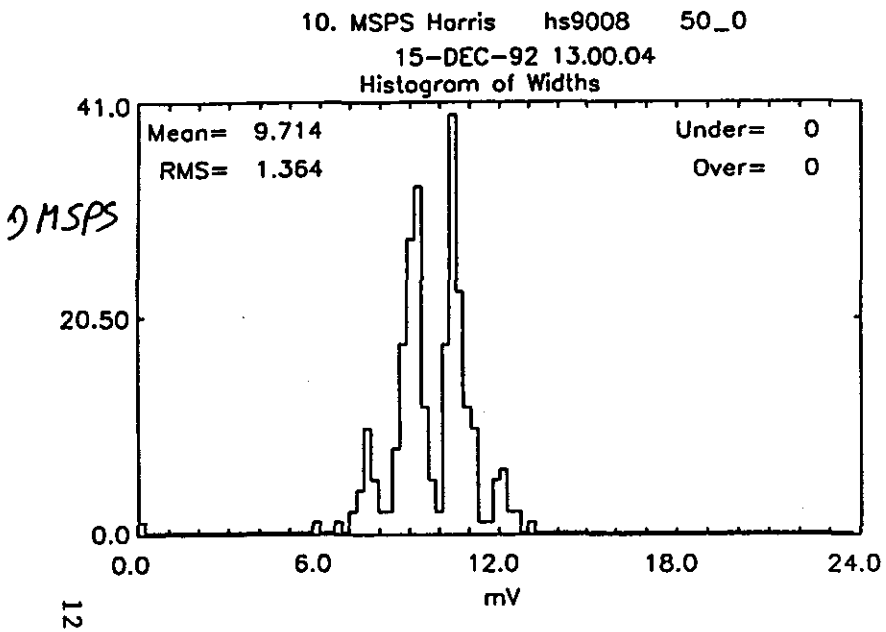


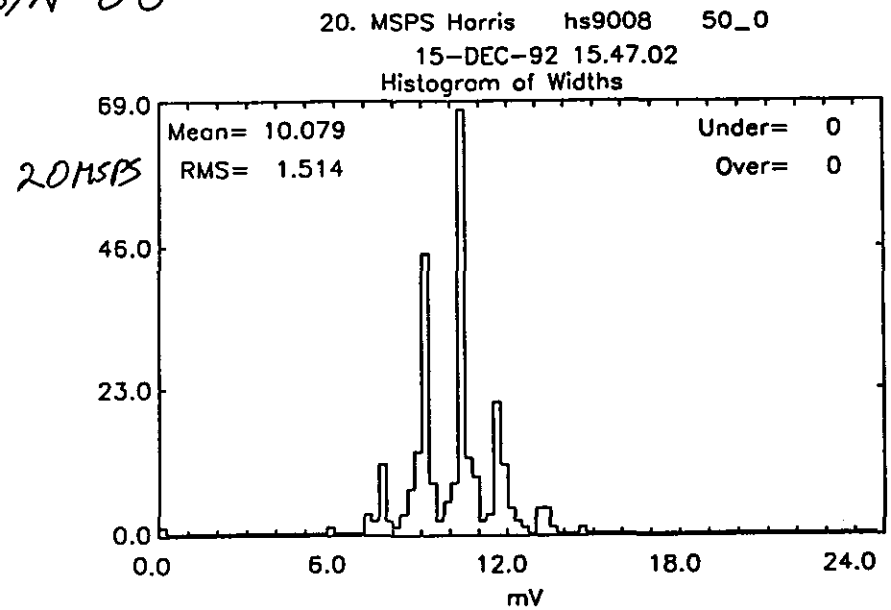


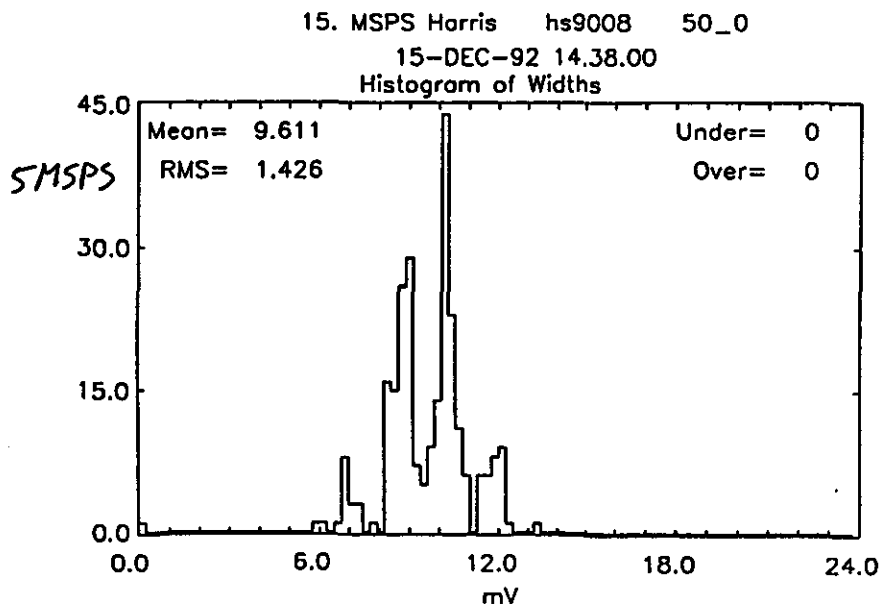

26/01/93 11.56
HS9008 51 0Mrad
DC DNL
Triangle DNL
INL (lsb)
Code Width RMS (lsb)
Peak Err (lsb)
Jitter Bound (ns)
Sample Rate (MSPS)

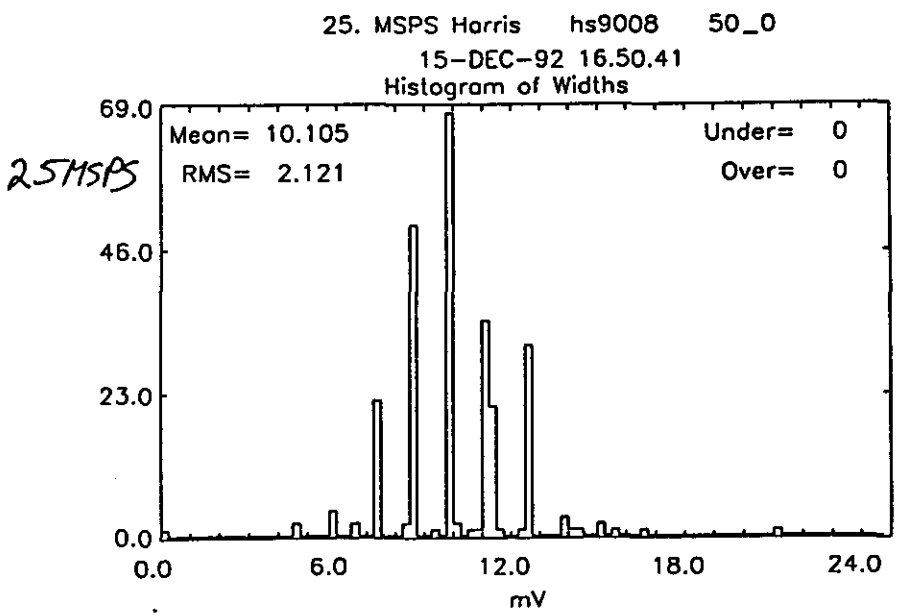
HS9008

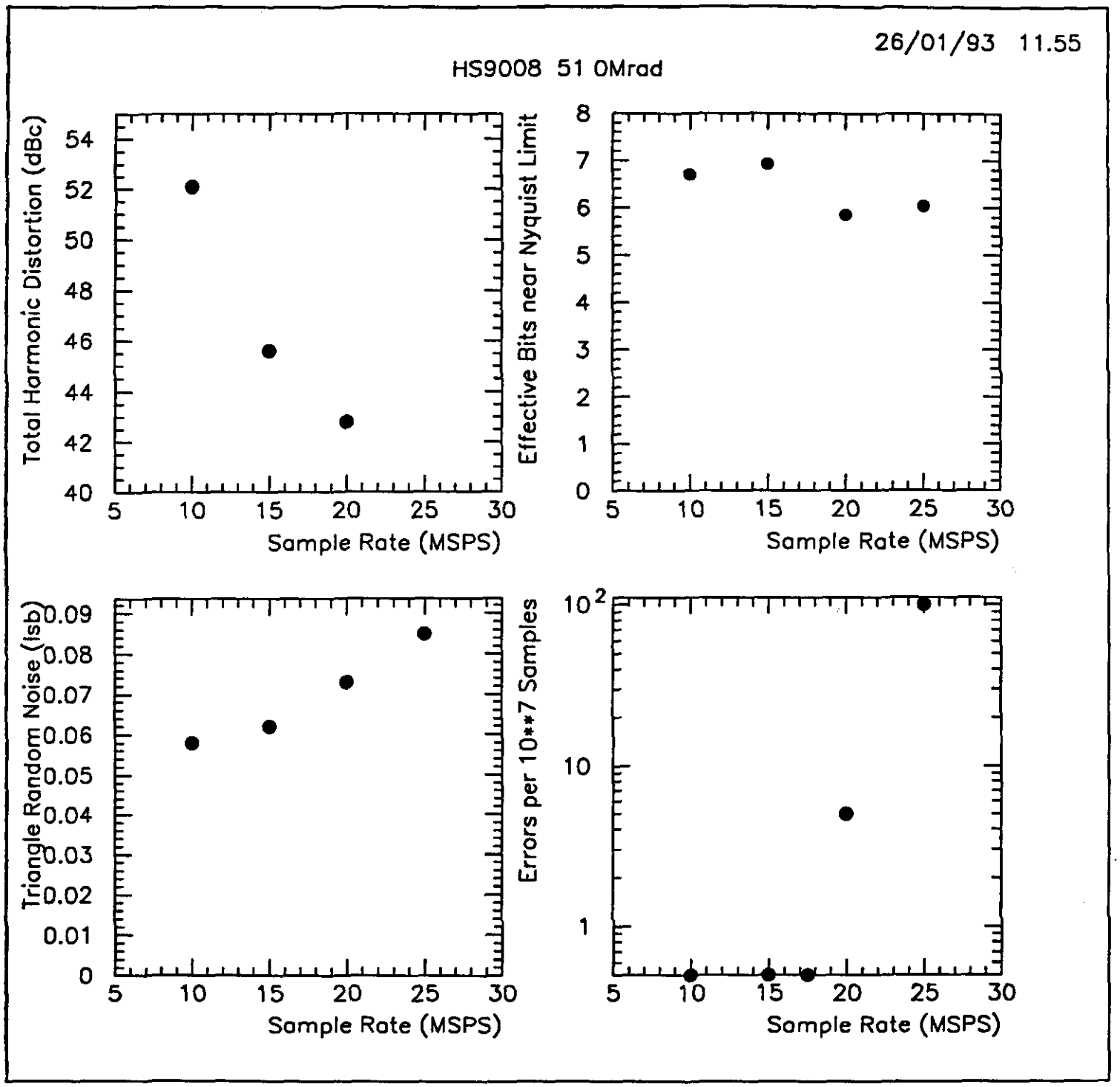
S/N 50


10. MSPS Harris hs9008 50_0
15-DEC-92 13.00.04
Histogram of Widths
Mean= 9.714
RMS= 1.364
Under= 0
Over= 0
9 MSPS
41.0
20.50
0.0
0.0
6.0
12.0
18.0
24.0
mV

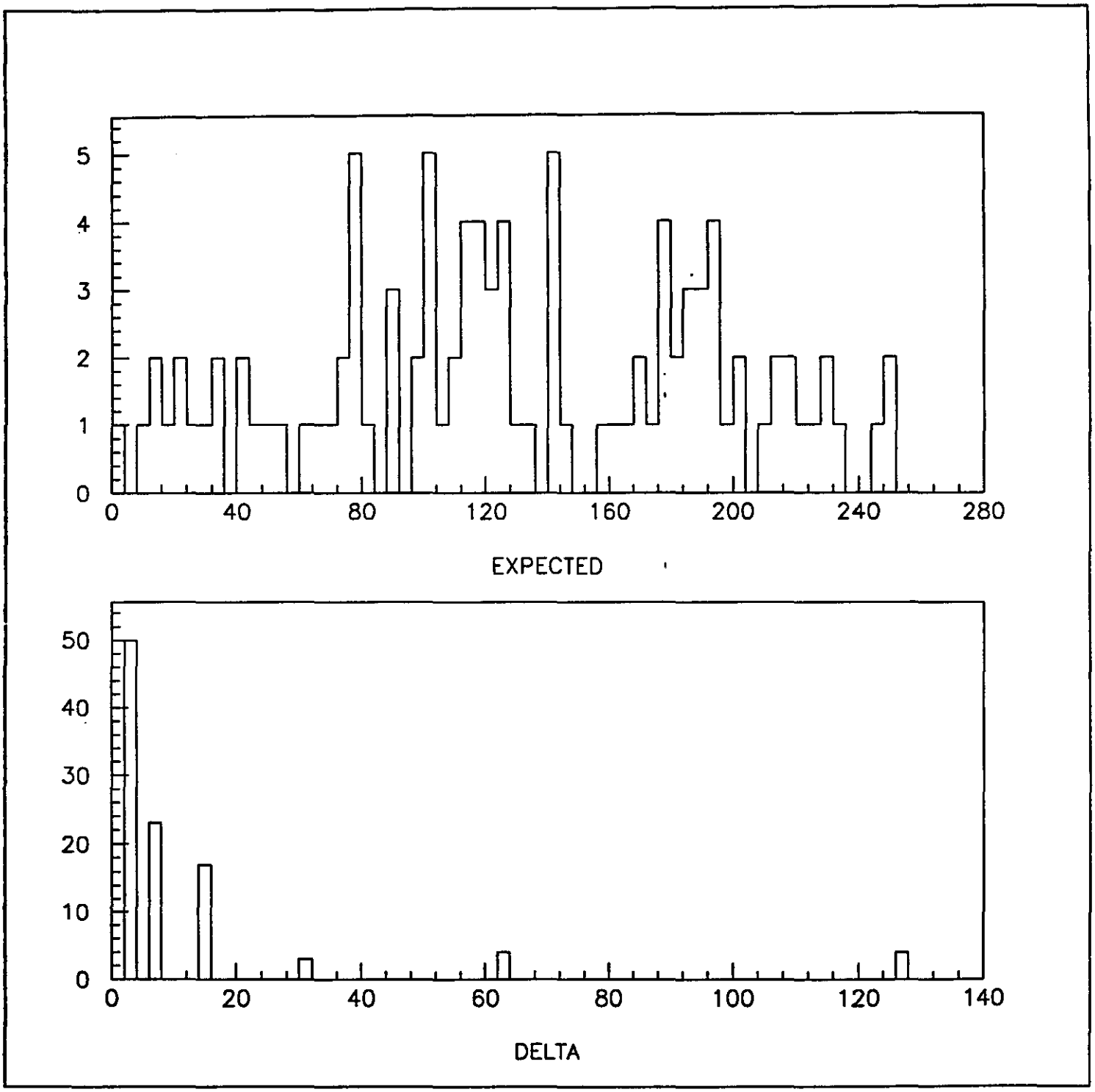

20. MSPS Harris hs9008 50_0
15-DEC-92 15.47.02
Histogram of Widths
Mean= 10.079
RMS= 1.514
Under= 0
Over= 0
20MSPS
69.0
46.0
23.0
0.0
0.0
6.0
12.0
18.0
24.0
mV

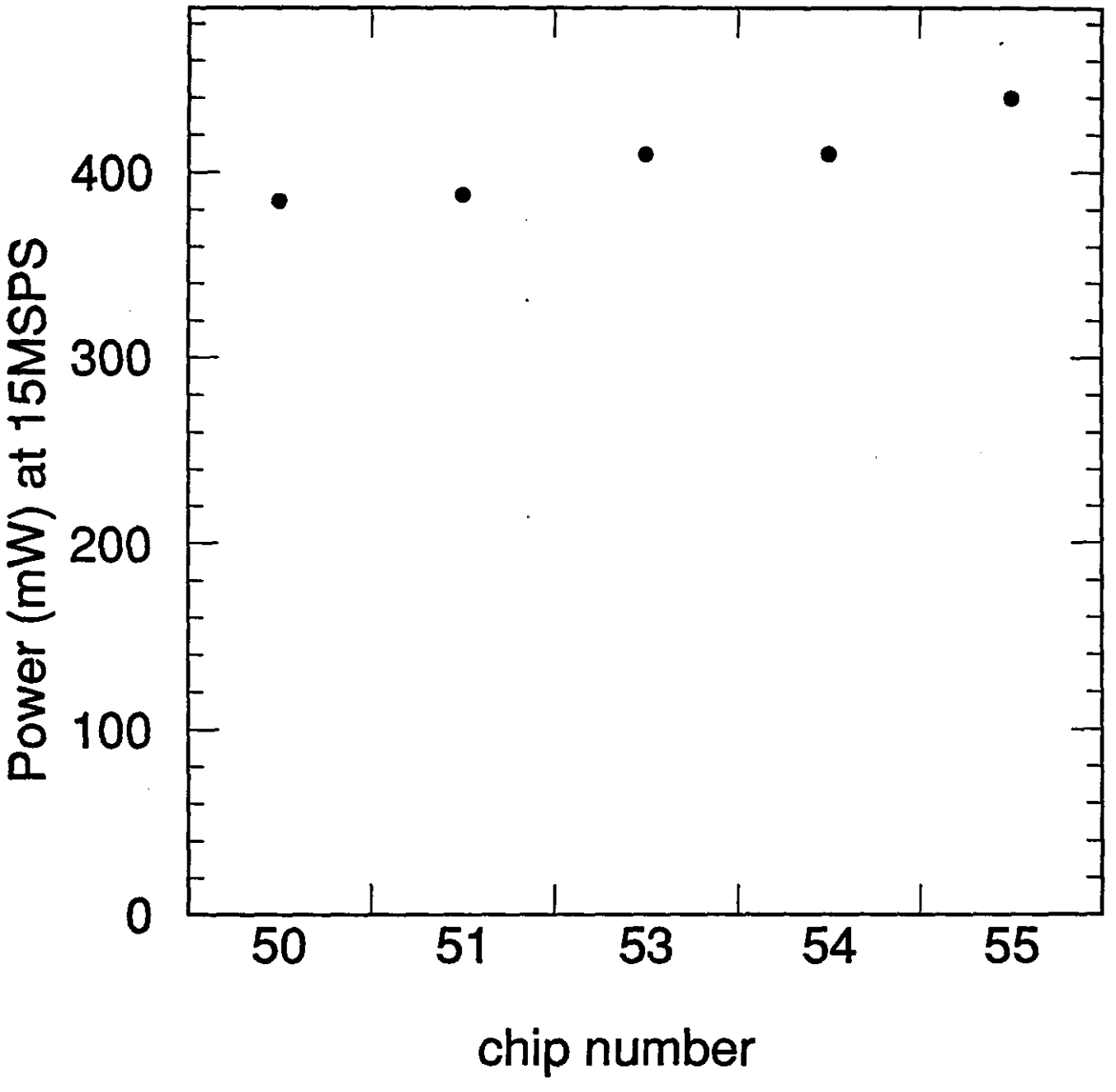

15. MSPS Harris hs9008 50_0
15-DEC-92 14.38.00
Histogram of Widths
Mean= 9.611
RMS= 1.426
Under= 0
Over= 0
5MSPS
45.0
30.0
15.0
0.0
0.0
6.0
12.0
18.0
24.0
mV

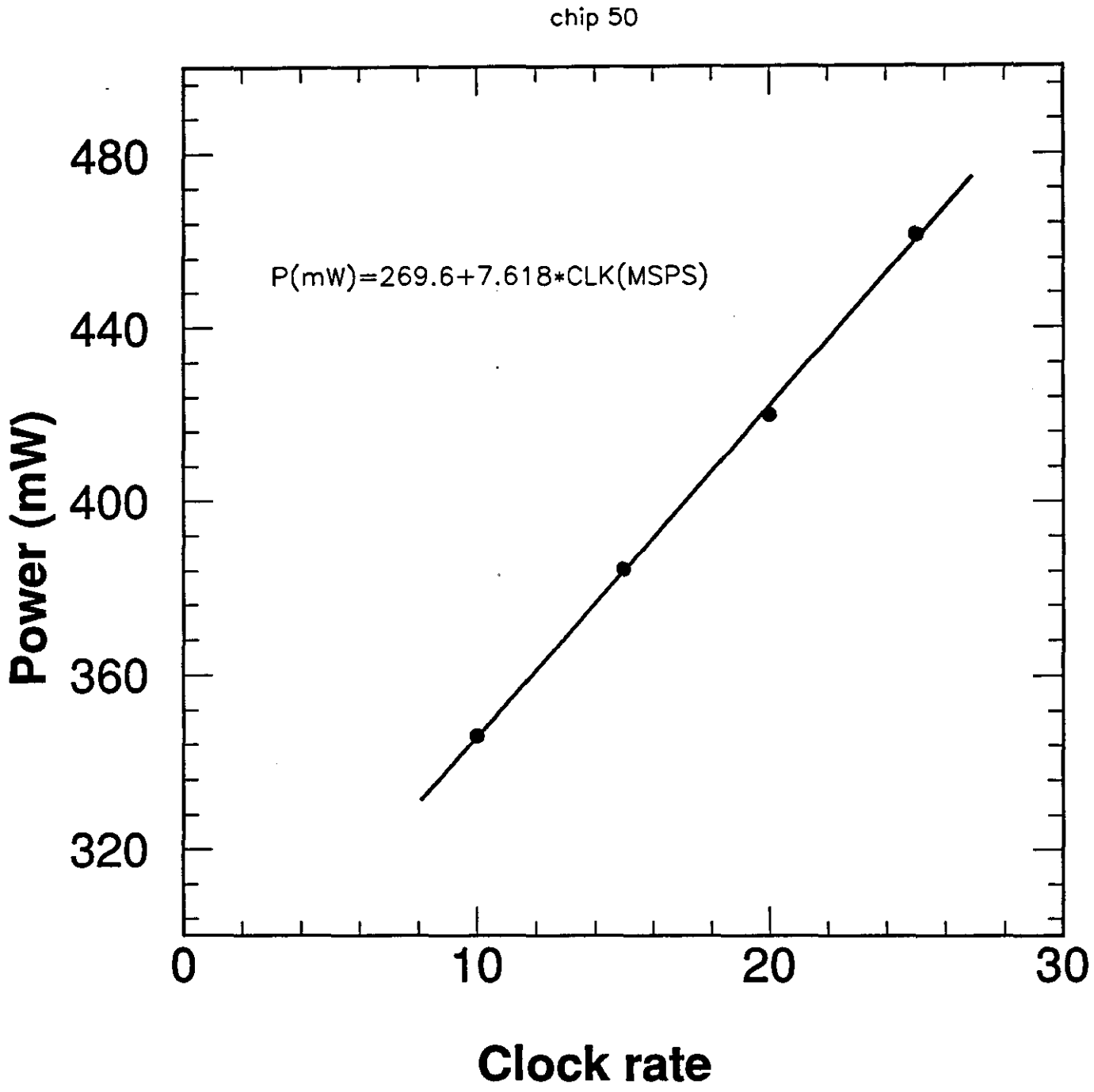

25. MSPS Harris hs9008 50_0
15-DEC-92 16.50.41
Histogram of Widths
Mean= 10.105
RMS= 2.121
Under= 0
Over= 0
25MSPS
69.0
46.0
23.0
0.0
0.0
6.0
12.0
18.0
24.0
mV

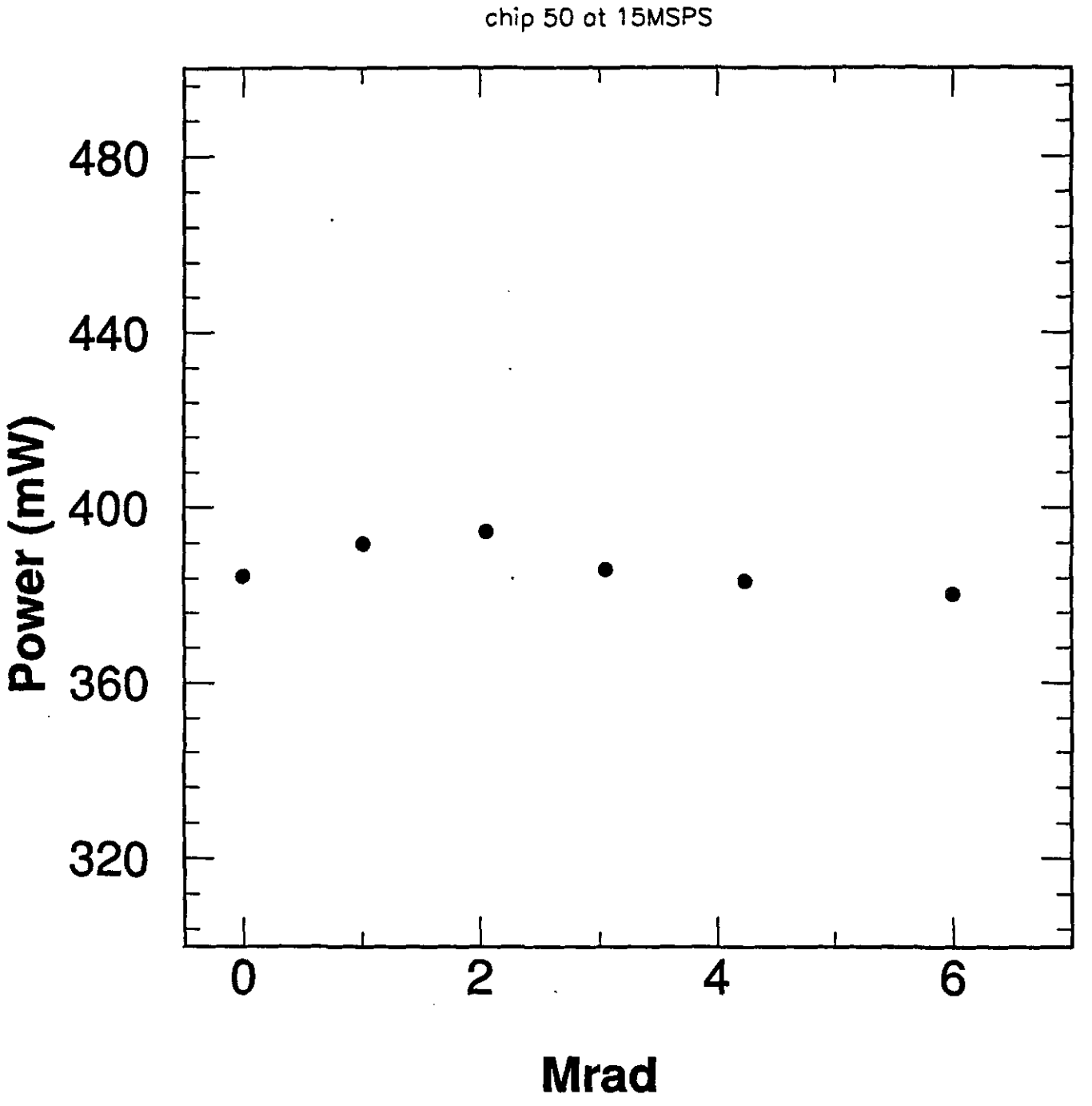

26/01/93 11.55
HS9008 51 0Mrad
Total Harmonic Distortion (dBc)
54
52
50
48
46
44
42
40
5
10
15
20
25
30
Sample Rate (MSPS)
Effective Bits near Nyquist Limit
8
7
6
5
4
3
2
1
0
5
10
15
20
25
30
Sample Rate (MSPS)
Triangle Random Noise (lsb)
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
5
10
15
20
25
30
Sample Rate (MSPS)
Errors per 10**7 Samples
10^2
10
1
5
10
15
20
25
30
Sample Rate (MSPS)

HS9008 53 OMR 25 MSPS QEL=2




Power (mW) at 15MSPS
400
300
200
100
0
50
51
53
54
55
chip number


chip 50
P(mW)=269.6+7.618*CLK(MSPS)
480
440
400
360
320
Power (mW)
0
10
20
30
Clock rate


chip 50 at 15MSPS
480
440
400
360
320
Power (mW)
0
2
4
6
Mrad