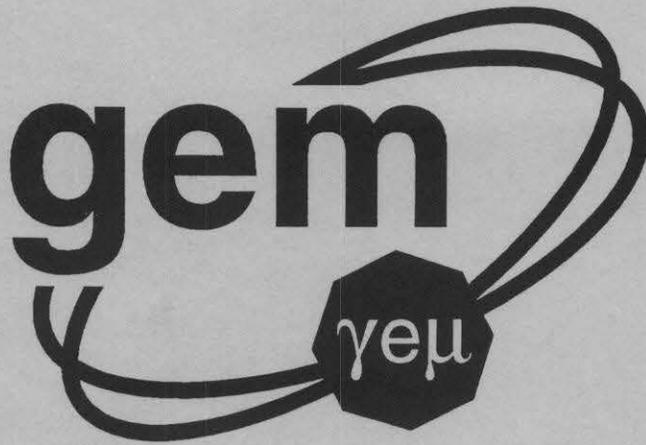


GEM TN-92-255



Electronics Engineering Meeting

December 16 & 17, 1992

Abstract:

Agenda, attendees, and presentations of the GEM Electronics Engineering Meeting held at Princeton University on December 16 & 17, 1992.

Session I: Wednesday December 16, 1992 (9:00 AM)

Status Reports: Speakers should report on the status of their technical work and on the status their cost & schedule work. Time includes talk and Q&A. If at all possible, please bring a Xerox copy of your slides.

9:00	Welcome	Marlow	(10 min)
	Overview of Costing	Fischer/Aguirre	(20 min)
	Silicon Vertex Detector Readout	Hahn/Cooke	(30 min)
	IPC Readout	Musser	(30 min)
10:30	Coffee Break		(30 min)
	Calorimeter Readout: Preamps, Sampler, ADC, etc	Parsons Rescia	(25 min) (20 min)
	Calorimeter Trigger (technical only)	Cleland	(20 min)
12:30	Lunch at Student Center		(90 min)
2:00	CSC Readout	Wixted	(30 min)
	Muon Trigger	Atiya	(30 min)
	Data Acquisition	Bowden	(30 min)
3:30	Coffee Break		(30 min)
4:00	Standard Racks & Power Supplies Integration	Freeman Lau	(30 min) (30 min)
5:00	Feedback on Cost & Schedule Work	Fischer/Aguirre	(30 min)
6:00	Dinner at Local Restaurant		
8:30	Refreshments & Conversation at the Wixted's		

Session II: Thursday December 17, 1992 (9:00 AM)

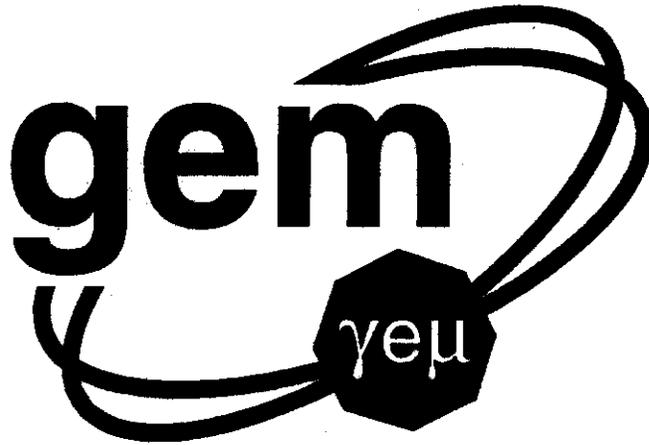
9:00	Grounding and Shielding Plan for GEM Discussion	Lau all	(30 min) (60 min)
10:30	Coffee		(30 min)
11:00	Parallel Sessions (Rooms to be announced)		(90 min)
	--- IC Design		
	--- Level 1 Calorimeter Trigger		
	--- Racks, Crates, Power Supplies, and Cooling		
12:30	Lunch at Student Center		(90 min)
2:00	Electronics Placement Issues Plans for TDR, Cost & Schedule Work	Lau Marlow	(30 min) (30 min)
	Adjourn in time for 5:00 PM flights		

12/16/92

GEM ELECTRONICS ENGINEERING MEETING

ATTENDEE LIST

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Presentation by:

Richard Fischer

Information Flow



GEM COST ESTIMATE DETAILS

30.02.2.1.3

ASSEMBLY (Barrel Region)

LINE ITEM	ITEM CODE	ITEM DESCRIPTION	QUANTITY	UNIT MEAS	COST BASIS	MATERIAL		LABOR					TOTALS	
						UNIT COST	TOTAL MAT'L,\$	CRAFT/TEAM	HOURLY RATE	MH/UNIT	TOTAL HOURS	UNIT COST	TOTAL LABOR,\$	MAT'L+LABOR,\$
1	M&S	MISC. OFFICE SUPPLIES FOR ADMINISTRATION	1.00	LS	BU	5,000	5,000		0	0	0	0	0	5,000
2	M&S	PC/MAC/WORKSTATION CHARGES	1.00	LS	BU	8,000	8,000		0	0	0	0	0	8,000
3	I&A	OVERSIGHT OF ASSY EQUIP. PURCHASE ACTIVITY FROM WEINSTEIN/OSBORNE ESTIMATE: (COST OF PRODUCT.)	0.25	MY	BU	0	0	NA10	70	1,900	475	133,000	33,250	33,250
4	I&A	OVERSIGHT OF ASSY ACTIVITY FROM WEINSTEIN/OSBORNE ESTIMATE:	1.00	NOTE	BU	0	0		0	0	0	0	0	0
5	I&A	WIRING MACHINE	2.00	MY	BU	0	0	NA10	70	1,900	3,800	133,000	266,000	266,000
6	P/F	AUTOMATIC SOLDER	1.00	NOTE	BU	0	0		0	0	0	0	0	0
7	P/F	AUTOMATIC WIRE CUTTER	1.00	LS	BU	40,000	40,000		0	0	0	0	0	40,000
8	P/F	MAC II, MAC, SCOPE, MCA, AMPS, HV	1.00	LS	BU	18,000	18,000		0	0	0	0	0	18,000
9	P/F	ASSUMED MISC. NUTS/BOLT, PINS, ETC:	1.00	LS	BU	5,000	5,000		0	0	0	0	0	5,000
10	P/F	WIRE MACHINE SET-UP	1.00	LS	BU	292,000	292,000		0	0	0	0	0	292,000
11	P/F	AUTOMATIC SOLDERER SET-UP	1.00	LS	BU	50,000	50,000		0	0	0	0	0	50,000
12	ASSBLY	AUTOMATIC WIRE CUTTER	0.50	MY	BU	0	0	NA10	70	1,900	950	133,000	66,500	66,500
13	ASSBLY	MISC OFFICE SUPPLIES FOR INSTALL/ASSY	0.33	MY	BU	0	0	NA10	70	1,900	627	133,000	43,890	43,890
14	ASSBLY	WIRE MACHINE SET-UP	0.17	MY	BU	0	0	NA10	70	1,900	323	133,000	22,610	22,610
15	ASSBLY	ASSEMBLY	1.00	LS	BU	24,000	24,000		0	0	0	0	0	24,000
16	ASSBLY	ASSEMBLY	0.50	MY	BU	0	0	NA08	56	1,900	950	107,008	53,504	53,504
17	ASSBLY	ASSEMBLY	0.33	MY	BU	0	0	NA08	56	1,900	627	107,008	35,313	35,313
18	ASSBLY	ASSEMBLY	0.17	MY	BU	0	0	NA08	56	1,900	323	107,008	18,191	18,191
19	ASSBLY	ASSEMBLY	10.00	MY	BU	0	0	NA08	56	1,900	19,000	107,008	1,070,080	1,070,080
20	ASSBLY	ASSEMBLY	8.00	MY	BU	0	0	NA09	43	1,900	15,200	82,004	656,032	656,032

SUBTOTAL - 30.02.2.1.3

ASSEMBLY

\$442,000

42,275

\$2,265,370

\$2,707,370

DESIGN GROWTH ALLOWANCE 30.00%

\$812,211

COST PLUS DGA

\$3,519,581

COST MATRIX

	ENG/DES	M&S	INSP/ADM	PROC/FAB	ASSBLY	INSTALL
LABOR	0	0	299,250	0	1,966,120	0
MATERIAL	0	13,000	0	405,000	24,000	0
TOTAL, \$	0	13,000	299,250	405,000	1,990,120	0
MANHOURS	0	0	4,275	0	38,000	0

LABOR

TOUCH LABOR =	\$1,966,120
EDIA LABOR =	\$299,250

RISK FACTORS

	FACTOR	DGA
Technical Risk	5.33	16.00 %
Cost Risk	3.00	6.00 %
Schedule Risk	8.00	8.00 %

GEM COST ESTIMATE DETAILS

40.03.1.2.3 VESSEL SUPPORT STRUCTURES

LINE ITEM	ITEM CODE	ITEM DESCRIPTION	QUANTITY	UNIT MEAS	COST BASIS	MATERIAL		LABOR					TOTALS	
						UNIT COST	TOTAL MAT'L,\$	CRAFT/ TEAM	HOURLY RATE	MH/ UNIT	TOTAL HOURS	UNIT COST	TOTAL LABOR,\$	MAT'L+ LABOR,\$
1	I&A	COORDINATOR SUPPT DURING CONST	3.00	MM	BU	0	0	INSPAD	58	147	441	8,532	25,597	25,597
2	M&S	WELD INSPEC QA TIME	0.50	MY	BU	94,000	47,000		0	0	0	0	0	47,000
3	P/F	SADDLES 304L SS W/ 8% WASTE	262.00	TON	BU	4,000	1,048,000		0	0	0	0	0	1,048,000
4	P/F	SUPPORT BLOCKS 304L SS	80.00	TONS	BU	4,000	320,000		0	0	0	0	0	320,000
5	P/F	TRANSPORTATION	20.00	LOADS	BU	2,500	50,000		0	0	0	0	0	50,000
6	P/F	PLATE SECTION BURNING	120.00	SECTION	BU	600	72,000		0	0	0	0	0	72,000
7	P/F	WEB SECTION BURNING	8.00	WLDMNTS	BU	1,750	14,000		0	0	0	0	0	14,000
8	P/F	WELD FIXTURING & ALIGNMNET	1.00	LS	BU	40,000	40,000		0	0	0	0	0	40,000
9	P/F	WELDING	8.00	WLDMNTS	BU	10,000	80,000		0	0	0	0	0	80,000
10	P/F	BLASTING	16.00	WLDMNTS	BU	2,500	40,000		0	0	0	0	0	40,000
11	P/F	RIGGING	1.00	LS	BU	100,000	100,000		0	0	0	0	0	100,000
12	P/F	HYDRAULIC JACKING SYSTEM	1.00	LS	BU	200,000	200,000		0	0	0	0	0	200,000
13	P/F	TRANSPORTER GREASE PADS	24.00	EA	BU	8,330	199,920		0	0	0	0	0	199,920

SUBTOTAL - 40.03.1.2.3	VESSEL SUPPORT STRUCTURES	\$2,210,920	441	\$25,597	\$2,236,517
	PRIME CONTRACTOR MARKUP 8.79%				\$196,633
					\$2,433,150
	DESIGN GROWTH ALLOWANCE 18.00%				\$437,967
	COST PLUS DGA				\$2,871,117

COST MATRIX

	ENG/DES	M&S	INSP/ADM	PROC/FAB	ASSBLY	INSTALL
LABOR	0	0	25,597	0	0	0
MATERIAL	0	47,000	0	2,163,920	0	0
TOTAL, \$	0	47,000	25,597	2,163,920	0	0
MANHOURS	0	0	441	0	0	0

LABOR

TOUCH LABOR =	\$0
EDIA LABOR =	\$25,597

RISK FACTORS

	FACTOR	DGA
Technical Risk	2.00	6.00 %
Cost Risk	4.00	8.00 %
Schedule Risk	4.00	4.00 %

GEM COST ESTIMATE DETAILS

40.03.2.1 FORWARD FIELD SHAPERS

LINE ITEM	ITEM CODE	ITEM DESCRIPTION	QUANTITY	UNIT MEAS	COST BASIS	MATERIAL		LABOR					TOTALS	
						UNIT COST	TOTAL MAT'L,\$	CRAFT/ TEAM	HOURLY RATE	MH/ UNIT	TOTAL HOURS	UNIT COST	TOTAL LABOR,\$	MAT'L+ LABOR,\$
1	I&A	CONTRACT ADMINISTRATION	2.00	MM	BU	0	0	INSPAD	58	147	294	8,532	17,064	17,064
2	I&A	ADMIN OVERHEAD	2.00	MM	BU	0	0	INSPAD	58	147	294	8,532	17,064	17,064
3	I&A	COORDINATOR SUPPORT	3.00	MM	BU	0	0	INSPAD	58	147	441	8,532	25,597	25,597
4	M&S	CASTING X-RAY INSPECTION	0.50	MY	BU	105,000	52,500		0	0	0	0	0	52,500
5	P/F	CONES (2 EA) W/20% WASTE	2400.00	TON	BU	2,200	5,280,000		0	0	0	0	0	5,280,000
6	P/F	CASTING TOOLING ALLOWANCE	1.00	LS	BU	1,000,000	1,000,000		0	0	0	0	0	1,000,000
7	P/F	ASSUME EACH CONE IS CONST FROM 20 CASTING OF EQUAL WEIGHT	1.00	NOTE	BU	0	0		0	0	0	0	0	0
8	P/F	SHIP CASTINGS	40.00	LOADS	BU	10,000	400,000		0	0	0	0	0	400,000
9	P/F	CASTING STRESS RELIEF/HEAT TREATMENT	40.00	PARTS	BU	3,200	128,000		0	0	0	0	0	128,000
10	P/F	CASTING CLEANUP/BEAD BLASTING	320.00	MH	BU	100	32,000		0	0	0	0	0	32,000
11	P/F	MACHINING (40 PARTS)	1600.00	MH	BU	100	160,000		0	0	0	0	0	160,000
12	P/F	BORE HOLES FOR TIE RODS (50 HOLES/PLATE)	4000.00	MH	BU	100	400,000		0	0	0	0	0	400,000
13	P/F	TIE RODS FOR POLE PIECES	1.00	LS	BU	100,000	100,000		0	0	0	0	0	100,000
14	ASSBLY	CONE ASSEMBLY (2 ENDS)	16.00	MM	BU	0	0	ASSBY	20	158	2,528	3,117	49,864	49,864
15	ASSBLY	INSTALL END POLE FIELD SHAPER IS IN WBS 1.3.1.8.1	1.00	NOTE	BU	0	0		0	0	0	0	0	0

SUBTOTAL - 40.03.2.1

FORWARD FIELD SHAPERS

\$7,552,500

3,557

\$109,590

\$7,662,089

PRIME CONTRACTOR MARKUP 8.79% \$673,647

\$8,335,736

DESIGN GROWTH ALLOWANCE 16.00% \$1,333,718

COST PLUS DGA \$9,669,453

COST MATRIX

LABOR

RISK FACTORS

	ENG/DES	M&S	INSP/ADM	PROC/FAB	ASSBLY	INSTALL
LABOR	0	0	59,725	0	49,864	0
MATERIAL	0	52,500	0	7,500,000	0	0
TOTAL, \$	0	52,500	59,725	7,500,000	49,864	0
MANHOURS	0	0	1,029	0	2,528	0

TOUCH LABOR =	\$49,864
EDIA LABOR =	\$59,725

	FACTOR	DGA
Technical Risk	2.00	6.00 %
Cost Risk	4.00	8.00 %
Schedule Risk	2.00	2.00 %

Work Breakdown Structure

(WBS)

ELECTRONICS

50	ELECTRONICS
50.01	Research and development
50.01.1	Si Vertex
50.01.1.1	Bipolar
50.01.1.2	CMOS I
50.01.1.3	CMOS II
50.01.1.4	MCM
50.01.1.5	Fiber optics
50.01.1.6	LVPS
50.01.1.7	Cable
50.01.1.8	Test station
50.01.2	IPC
50.01.2.1	HVPS
50.01.2.2	LVPS
50.01.2.3	Signal cable
50.01.2.4	Preamp IC
50.01.2.5	SCA IC
50.01.2.6	MUX/FADC IC
50.01.2.7	PCB/packaging
50.01.2.8	Fiber optics
50.01.2.9	Test beam support
50.01.3	Calorimeter front-end
50.01.3.1	HVPS
50.01.3.2	LVPS
50.01.3.3	Signal cable
50.01.3.4	Preamp IC
50.01.3.5	SCA IC
50.01.3.6	Readout ADC
50.01.3.7	Digital readout
50.01.3.8	PC board (packaging)
50.01.3.9	Test beam support
50.01.4	Muon front-end
50.01.5	Level 1 - trigger
50.01.5.1	Calorimeter
50.01.5.2	Muon
50.01.6	DAQ
50.02	Front-End
50.02.1	Muon
50.02.1.1	Resistive Plate Chamber
50.02.1.1.1	Design Documentation
50.02.1.1.2	Prototype
50.02.1.1.2.1	High Voltage

Work Breakdown Structure

(W B S)

50.02.1.1.2.1.1	Power Supply
50.02.1.1.2.1.2	Distribution
50.02.1.1.2.2	Low Voltage In-Detector
50.02.1.1.2.2.1	Power Supply
50.02.1.1.2.2.2	Distribution
50.02.1.1.2.3	Signal Cables
50.02.1.1.2.4	Active Components
50.02.1.1.2.4.1	Chronotron
50.02.1.1.2.5	Printed Circuit Board
50.02.1.1.2.5.1	Bend Plane Discriminator
50.02.1.1.2.5.2	Non Plane Discriminator
50.02.1.1.2.6	On-Detector Crate Complete
50.02.1.1.2.7	Control/Data Links
50.02.1.1.2.7.1	Receiver & Buffer
50.02.1.1.2.7.2	Optics
50.02.1.1.3	Production
50.02.1.1.3.1	High Voltage
50.02.1.1.3.1.1	Power Supply
50.02.1.1.3.1.2	Distribution
50.02.1.1.3.2	Low Voltage In-Detector
50.02.1.1.3.2.1	Power Supply
50.02.1.1.3.2.2	Distribution
50.02.1.1.3.3	Signal Cables
50.02.1.1.3.4	Active Components
50.02.1.1.3.4.1	Bend Plane Discriminator
50.02.1.1.3.4.2	Bend Plane Chronotron
50.02.1.1.3.4.3	Non Plane Discriminator
50.02.1.1.3.4.4	TDC Chip
50.02.1.1.3.5	Printed Circuit Board
50.02.1.1.3.5.1	Bend Plane Discriminator
50.02.1.1.3.5.2	Non Plane Discriminator
50.02.1.1.3.5.3	TDC
50.02.1.1.3.6	On-Detector Crate Complete
50.02.1.1.3.7	Control/Data Links (66 L)
50.02.1.1.3.7.1	Receiver & Buffer
50.02.1.1.3.7.2	Optics
50.02.1.1.3.7.3	Rack Slot
50.02.1.1.4	Installation & Test
50.02.1.2	RDT's
50.02.1.2.1	Design/Documentation
50.02.1.2.2	Prototype
50.02.1.2.2.1	High Voltage
50.02.1.2.2.1.1	Power Supply
50.02.1.2.2.1.2	Distribution
50.02.1.2.2.2	Low Voltage In-Detector
50.02.1.2.2.2.1	Power Supply
50.02.1.2.2.2.2	Distribution
50.02.1.2.2.3	Signal Cables
50.02.1.2.2.4	Active Components
50.02.1.2.2.4.1	Discriminator
50.02.1.2.2.4.2	Time Digital Converter
50.02.1.2.2.5	Printed Circuit Board
50.02.1.2.2.5.1	Discriminator
50.02.1.2.2.5.2	Time Digital Converter
50.02.1.2.2.6	On-Detector Crate Complete
50.02.1.2.2.7	Control/Data Links
50.02.1.2.2.7.1	Receiver & Buffer
50.02.1.2.2.7.2	Optics
50.02.1.2.3	Production
50.02.1.2.3.1	High Voltage
50.02.1.2.3.1.1	Power Supply

Work Breakdown Structure

(W B S)

50.02.1.2.3.1.2	Distribution
50.02.1.2.3.2	Low Voltage In-Detector
50.02.1.2.3.2.1	Power supply
50.02.1.2.3.2.2	Distribution
50.02.1.2.3.3	Signal cables
50.02.1.2.3.4	Active components
50.02.1.2.3.4.1	Discriminator
50.02.1.2.3.4.2	Time digital converter
50.02.1.2.3.5	Printed circuit board
50.02.1.2.3.5.2	Discriminator
50.02.1.2.3.5.3	Time digital converter
50.02.1.2.3.6	On-detector crate complete
50.02.1.2.3.7	Control/data links (44 lin
50.02.1.2.3.7.1	Receiver & buffer
50.02.1.2.3.7.2	Optics
50.02.1.2.3.7.3	Rack slot
50.02.1.2.4	Installation & test
50.02.1.3	CSC Wire (29K)
50.02.1.3.1	Design/documentation
50.02.1.3.2	Prototype
50.02.1.3.2.1	High voltage
50.02.1.3.2.1.1	Power supply
50.02.1.3.2.1.2	Distribution
50.02.1.3.2.2	Low voltage in-detector
50.02.1.3.2.2.1	Power supply
50.02.1.3.2.2.2	Distribution
50.02.1.3.2.3	Signal cables
50.02.1.3.2.4	Active components
50.02.1.3.2.4.1	Preamp
50.02.1.3.2.4.2	TDC
50.02.1.3.2.4.3	Discriminator
50.02.1.3.2.5	Printed circuit board
50.02.1.3.2.5.1	Discriminator
50.02.1.3.2.5.2	TDC
50.02.1.3.2.6	On-detector crate complete
50.02.1.3.2.7	Control/data links
50.02.1.3.2.7.1	Receiver & buffer
50.02.1.3.2.7.2	Optics
50.02.1.3.2.7.3	Rack slot
50.02.1.3.3	Production
50.02.1.3.3.1	High voltage
50.02.1.3.3.1.1	Power supply
50.02.1.3.3.1.2	Distribution
50.02.1.3.3.2	Low voltage in-detector
50.02.1.3.3.2.1	Power supply
50.02.1.3.3.2.2	Distribution
50.02.1.3.3.3	Signal cables
50.02.1.3.3.4	Active components
50.02.1.3.3.4.1	Preamp
50.02.1.3.3.4.2	Discriminator
50.02.1.3.3.4.3	TDC
50.02.1.3.3.5	Printed circuit board
50.02.1.3.3.5.1	Discriminator
50.02.1.3.3.5.2	TDC
50.02.1.3.3.6	On-detector crate complete
50.02.1.3.3.7	Control/data links
50.02.1.3.3.7.1	Receiver & buffer
50.02.1.3.3.7.2	Optics
50.02.1.3.3.7.3	Rack slot
50.02.1.3.4	Installation & test
50.02.1.4	CSC PAD (242K channels)

Work Breakdown Structure

(W B S)

50.02.1.4.1	Design/documentation
50.02.1.4.2	Prototype
50.02.1.4.2.1	High voltage
50.02.1.4.2.1.1	Power supply
50.02.1.4.2.1.2	Distribution
50.02.1.4.2.2	Low voltage in-detector
50.02.1.4.2.2.1	Power supply
50.02.1.4.2.2.2	Distribution
50.02.1.4.2.3	Signal cables
50.02.1.4.2.4	Active components
50.02.1.4.2.4.1	Preamp
50.02.1.4.2.4.2	Preamp test station
50.02.1.4.2.4.3	Discriminator
50.02.1.4.2.4.4	Digital pipeline
50.02.1.4.2.5	Printed circuit board
50.02.1.4.2.5.1	FIFO
50.02.1.4.2.6	On-detector crate complete
50.02.1.4.2.7	Control/data links
50.02.1.4.2.7.1	Receiver & buffer
50.02.1.4.2.7.2	Optics
50.02.1.4.2.7.3	Rack slot
50.02.1.4.3	Production
50.02.1.4.3.1	High voltage
50.02.1.4.3.1.1	Power supply
50.02.1.4.3.1.2	Distribution
50.02.1.4.3.2	Low voltage in-detector
50.02.1.4.3.2.1	Power supply
50.02.1.4.3.2.2	Distribution
50.02.1.4.3.3	Signal cables
50.02.1.4.3.4	Active components
50.02.1.4.3.4.1	Preamp
50.02.1.4.3.4.2	Preamp testing
50.02.1.4.3.4.3	Discriminator
50.02.1.4.3.4.4	FIFO
50.02.1.4.3.4.5	ADC
50.02.1.4.3.5	Printed circuit board
50.02.1.4.3.5.1	FIFO
50.02.1.4.3.6	On-detector crate complete
50.02.1.4.3.7	Control/data links (242 li
50.02.1.4.3.7.1	Receiver & buffer
50.02.1.4.3.7.2	Optics
50.02.1.4.3.7.3	Rack slot
50.02.1.4.4	Installation & test
50.02.2	Central Tracker
50.02.2.1	Si-tracker (3200 channels)
50.02.2.1.0	Bipolar
50.02.2.1.1	CMOS-1
50.02.2.1.2	CMOS-2
50.02.2.1.3	Multi-chip module
50.02.2.1.4	Fiber optics (2526 links)
50.02.2.1.5	Power supplies
50.02.2.1.6	Cables
50.02.2.1.7	Test station
50.02.2.1.8	Data acquisition
50.02.2.1.9	Clock distribution
50.02.2.2	IPC (400K ch.)
50.02.2.2.1	Design/documentation
50.02.2.2.2	Prototype
50.02.2.2.2.1	High voltage
50.02.2.2.2.1.1	Power supply

Work Breakdown Structure

(W B S)

50.02.2.2.2.1.2	Distribution
50.02.2.2.2.2	Low voltage in-detector
50.02.2.2.2.2.1	Power supply
50.02.2.2.2.2.2	Distribution
50.02.2.2.2.3	Signal cables
50.02.2.2.2.4	Active components
50.02.2.2.2.4.1	Preamp (EE)
50.02.2.2.2.4.2	SCA test station (EE)
50.02.2.2.2.4.3	SCA test station
50.02.2.2.2.4.4	Readout controller (EE)
50.02.2.2.2.5	Printed circuit board
50.02.2.2.2.6	On-detector crate complete
50.02.2.2.2.7	Control/data links
50.02.2.2.2.7.1	Receiver & buffer
50.02.2.2.2.7.2	Optics
50.02.2.2.3	Production
50.02.2.2.3.1	High voltage
50.02.2.2.3.1.1	Power supply
50.02.2.2.3.1.2	Distribution
50.02.2.2.3.2	Low voltage in-detector
50.02.2.2.3.2.1	Power supply
50.02.2.2.3.2.2	Distribution
50.02.2.2.3.3	Signal cables
50.02.2.2.3.4	Active components
50.02.2.2.3.4.1	Preamp
50.02.2.2.3.4.2	SCA
50.02.2.2.3.4.2	SCA test
50.02.2.2.3.4.3	MUX
50.02.2.2.3.5	Printed circuit board
50.02.2.2.3.6	On-detector crate complete
50.02.2.2.3.7	Control/data links (1563 I
50.02.2.2.3.7.1	Receiver & buffer
50.02.2.2.3.7.2	Optics
50.02.2.2.3.7.3	Rack slot
50.02.2.2.4	Installation & test
50.02.3	Calorimeter (86K channels)
50.02.3.1	Design/documentation
50.02.3.2	Prototype
50.02.3.2.1	High voltage
50.02.3.2.1.1	Power supply
50.02.3.2.1.2	Distribution
50.02.3.2.2	Low voltage in-detector
50.02.3.2.2.1	Power supply
50.02.3.2.2.2	Distribution
50.02.3.2.3	Signal cables
50.02.3.2.4	Active components
50.02.3.2.4.1	Preamp
50.02.3.2.4.2	Switch capacitor array
50.02.3.2.4.3	SCA test station
50.02.3.2.4.4	ADC
50.02.3.2.4.5	ADC test station
50.02.3.2.4.6	Calibration system
50.02.3.2.4.7	Shapen
50.02.3.2.5	Printed circuit board
50.02.3.2.5.1	DSP
50.02.3.2.5.2	Preamp calibration
50.02.3.2.5.3	SCA/ADC
50.02.3.2.5.4	FADC
50.02.3.2.6	On-detector crate complete
50.02.3.2.7	Control/data links

Work Breakdown Structure

(W B S)

50.02.3.2.7.1	Receiver & buffer
50.02.3.2.7.2	Optics
50.02.3.3	Production
50.02.3.3.1	High voltage
50.02.3.3.1.1	Power supply
50.02.3.3.1.2	Distribution
50.02.3.3.2	Low voltage in-detector
50.02.3.3.2.1	Power supply
50.02.3.3.2.2	Distribution
50.02.3.3.3	Signal cables
50.02.3.3.4	Active components
50.02.3.3.4.1	Preamp
50.02.3.3.4.2	SCA
50.02.3.3.4.3	SCA station
50.02.3.3.4.4	12 bit-ADC
50.02.3.3.4.5	ADC station
50.02.3.3.4.6	Trigger FADC
50.02.3.3.4.7	Calibration system
50.02.3.3.4.8	Shapen
50.02.3.3.5	Printed circuit board
50.02.3.3.5.1	DSP
50.02.3.3.5.2	Preamp/calibration
50.02.3.3.5.3	SCA/ADC
50.02.3.3.5.4	FADC
50.02.3.3.5.5	Intermediate driver
50.02.3.3.6	On-detector crate complete
50.02.3.3.7	Control/data links (86 lin
50.02.3.3.7.1	Receiver & buffer
50.02.3.3.7.2	Optics
50.02.3.3.7.3	Rack slot
50.02.3.4	Installation & test

50.03 Data Acquisition

50.04 Trigger

50.04.1	Level 1
50.04.1.1	Calorimeter (2960 channels
50.04.1.1.1	Design/documentation
50.04.1.1.2	Prototype
50.04.1.1.2.1	High voltage
50.04.1.1.2.1.1	Power supply
50.04.1.1.2.1.2	Distribution
50.04.1.1.2.2	Low voltage in-detector
50.04.1.1.2.2.1	Power supply
50.04.1.1.2.2.2	Distribution
50.04.1.1.2.3	Signal cables
50.04.1.1.2.4	Active components
50.04.1.1.2.4.1	SUM chip
50.04.1.1.2.4.2	ISOLATION chip
50.04.1.1.2.5	Printed circuit board
50.04.1.1.2.5.1	Energy SUM
50.04.1.1.2.5.2	Isolation
50.04.1.1.2.6	On-detector crate complete
50.04.1.1.2.7	Control/data links
50.04.1.1.2.7.1	Receiver & buffer
50.04.1.1.2.7.2	Optics
50.04.1.1.3	Production
50.04.1.1.3.1	High voltage

Work Breakdown Structure

(WBS)

50.04.1.1.3.1.1	Power supply
50.04.1.1.3.1.2	Distribution
50.04.1.1.3.2	Low voltage in-detector
50.04.1.1.3.2.1	Power supply
50.04.1.1.3.2.2	Distribution
50.04.1.1.3.3	Signal cables
50.04.1.1.3.4	Active components
50.04.1.1.3.4.1	SUM chip
50.04.1.1.3.4.2	ISOLATION chip
50.04.1.1.3.5	Printed circuit board
50.04.1.1.3.5.1	Energy SUM
50.04.1.1.3.5.2	Isolation
50.04.1.1.3.6	On-detector crate complete
50.04.1.1.3.7	Control/data links
50.04.1.1.3.7.1	Receiver & buffer
50.04.1.1.3.7.2	Optics
50.04.1.1.3.7.3	Rack slot
50.04.1.1.4	Installation & test
50.04.1.2	Muon
50.04.1.2.1	Design/documentation
50.04.1.2.2	Prototype
50.04.1.2.2.1	High voltage
50.04.1.2.2.1.1	Power supply
50.04.1.2.2.1.2	Distribution
50.04.1.2.2.2	Low voltage in-detector
50.04.1.2.2.2.1	Power supply
50.04.1.2.2.2.2	Distribution
50.04.1.2.2.3	Signal cables
50.04.1.2.2.4	Active components
50.04.1.2.2.4.1	Encoder in Encap
50.04.1.2.2.4.2	Memory in Encap
50.04.1.2.2.4.3	Digital chip in Barrel (10
50.04.1.2.2.4.4	Digital chip in Barrel (Ph
50.04.1.2.2.5	Printed circuit board
50.04.1.2.2.5.1	Programmable gate array
50.04.1.2.2.5.2	Sequencer
50.04.1.2.2.5.3	CAM
50.04.1.2.2.5.4	Digital chip in Barrel (10
50.04.1.2.2.5.5	Digital chip in Barrel (Ph
50.04.1.2.2.6	On-detector crate complete
50.04.1.2.2.7	Control/data links
50.04.1.2.2.7.1	Receiver & buffer
50.04.1.2.2.7.2	Optics
50.04.1.2.3	Production
50.04.1.2.3.1	High voltage
50.04.1.2.3.1.1	Power supply
50.04.1.2.3.1.2	Distribution
50.04.1.2.3.2	Low voltage in-detector
50.04.1.2.3.2.1	Power supply
50.04.1.2.3.2.2	Distribution
50.04.1.2.3.3	Signal cables
50.04.1.2.3.4	Active components
50.04.1.2.3.4.1	Encoder in Encap
50.04.1.2.3.4.2	Memory in Encap
50.04.1.2.3.4.3	CAM
50.04.1.2.3.4.4	Digital chip in Barrel (10
50.04.1.2.3.4.5	Digital chip in Barrel (Ph
50.04.1.2.3.5	Printed circuit board
50.04.1.2.3.5.1	PGA
50.04.1.2.3.5.2	Sequencer
50.04.1.2.3.5.3	CAM

Work Breakdown Structure

(W B S)

50.04.1.2.3.5.4	Digital chip in Barrel (10
50.04.1.2.3.5.5	Digital chip in Barrel (Ph
50.04.1.2.3.6	On-detector crate complete
50.04.1.2.3.7	Control/data links
50.04.1.2.3.7.1	Receiver & buffer
50.04.1.2.3.7.2	Optics
50.04.1.2.3.7.3	Rack slot
50.04.1.2.4	Installation & test
50.04.2	Level 2
50.04.2.1	Design/documentation
50.04.2.2	Prototype
50.04.2.2.1	High voltage
50.04.2.2.1.1	Power supply
50.04.2.2.1.2	Distribution
50.04.2.2.2	Low voltage in-detector
50.04.2.2.2.1	Power supply
50.04.2.2.2.2	Distribution
50.04.2.2.3	Signal cables
50.04.2.2.4	Active components
50.04.2.2.4.1	Programming effort
50.04.2.2.5	Printed circuit board
50.04.2.2.5.1	Processor
50.04.2.2.5.2	Memory
50.04.2.2.6	On-detector crate complete
50.04.2.2.7	Control/data links
50.04.2.2.7.1	Receiver & buffer
50.04.2.2.7.2	Optics
50.04.2.3	Production
50.04.2.3.1	High voltage
50.04.2.3.1.1	Power supply
50.04.2.3.1.2	Distribution
50.04.2.3.2	Low voltage in-detector
50.04.2.3.2.1	Power supply
50.04.2.3.2.2	Distribution
50.04.2.3.3	Signal cables
50.04.2.3.4	Active components
50.04.2.3.5	Printed circuit board
50.04.2.3.5.1	Calorimeter board
50.04.2.3.5.2	Processor board
50.04.2.3.6	On-detector crate complete
50.04.2.3.7	Control/data links
50.04.2.3.7.1	Receiver & buffer
50.04.2.3.7.2	Optics
50.04.2.3.7.3	Rack slot
50.04.2.4	Installation & test
50.04.3	Interface
50.04.3.1	Clock & control system
50.04.3.1.1	System design
50.04.3.1.2	PC design
50.04.3.1.3	PC design tech
50.04.3.1.4	IC
50.04.3.1.4.1	IC design
50.04.3.1.4.2	PC design
50.04.3.1.5	Rack slot
50.04.3.1.6	Fiber links
50.04.3.1.7	IC fabrication
50.05	Integration

Work Breakdown Structure

(W B S)

50.05.1	LVPS Development
50.05.2	Fiber Link Development
50.05.3	Facility Interface
50.05.4	Facility Development
50.06	Project Management
50.06.1	Project Mgt & Administration
50.06.2	Resource Mgt
50.06.3	ES&H
50.06.4	Quality Assurance
50.07	Preliminary & conceptual design

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

WBS No.: _____ **SAMPLE INSTRUCTIONS** _____

WBS Descript.: _____

Estimate Type: 7

WBS QTY: _____

WBS UM: _____

	RISK	
	Factors	Weight %
Technical	_____	_____
Cost	_____	_____
Schedule	_____	_____

Functional Activity: 1 Engineering/Design
2 Inspection/Administration
3 Procurement/Fabrication
4 Assembly
5 Installation

Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

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Item Description	Qty	Unit Meas (UM)	Craft/Team Resource Code	* Unit Productivity MH/UM	Mat'l Unit Cost
1	2	3	4	5	6
1: Describe line item cost.					
2: What is the quantity required or estimated for the line item?					
3: What is the unit of measure (UM) for the line item in which to express other line item components?					
4: The code descriptor for using a craft or team mix (crew) composite. It is imperative that the crafts and team/crew be supplemented in detail.					
5: Unit Productivity is how many man-hours per UM is estimated for the line item by using the craft or team/crew to provide the estimated effort required. For time unit conversions use: For example if UM is manmonths then MH/UM =173.3 (Actual Time); If UM is tons and you estimate 100 manhours per ton, then MH/UM (ton) =100.					
6: What is the material cost (k\$) per UM?					
7: Estimate Type is to be: Bottom Up (BU), Specific Analogy (SA), Parametric Study (PS), Review and update (RU), Trend Analysis (TA), Expert Opinion (EO).					

Notes:

GEM DETECTOR CRAFT CODES, TEAM CODES, RATES

LOS ALAMOS NATIONAL LABORATORY ESTIMATE

CRAFT RESOURCES **TABLE 1**

LOCATION	CRAFT CODE	LABOR DESCRIPTION
LOS ALAMOS	LANL1	MANAGER
LOS ALAMOS	LANL2	ENGINEER/PHYSICIST
LOS ALAMOS	LANL3	DESIGNER/COORDINATOR
LOS ALAMOS	LANL4	SENIOR TECHNICIAN
LOS ALAMOS	LANL5	JR. TECHNICIAN
LOS ALAMOS	LANL6	CRAFT
LOS ALAMOS	LANL7	SECRETARY

TEAM RESOURCES **TABLE 2**

TEAM CODE	DESCRIPTION	CRAFT CODE	TEAM MIX (Hr)
LAMGMT	MANAGEMENT		
	MANAGER	LANL1	.5
	ENGINEER/PHYSICIST	LANL2	.75
	DESIGN/COORDINATOR	LANL5	1
	TEAM RATE/YR		2.25
LADES	DESIGN		
	ENGINEER/PHYSICIST	LANL2	.25
	DESIGN/COORDINATOR	LANL3	1
	SR. TECHNICIAN	LANL4	.5
	SECRETARY	LANL7	.25
	TEAM RATE/YR		2.00
LAI&A	INSPECTION/ADMIN		
	SR. TECHNICIAN	LANL4	.5
	JR. TECHNICIAN	LANL5	1
	TEAM RATE/YR		1.50
LAASS	ASSEMBLY		
	SR. TECHNICIAN	LANL4	.25
	ELECT TECH (NAT AVG)	NA06	1
	TEAM RATE/YR		1.25
SSCINS	INSTALLATION		
	ENG/PHYSICIST (SSCL)	SSC2	.5
	SR. TECHNICIAN (SSCL)	SSC4	1
	JR. TECH (SSCL)	SSC5	1
	TEAM RATE/YR		2.50

NOTE: See "Gem Estimating Plan" "Gem Detector Craft Codes and Labor Rates for craft codes not found in this site specific resource table.

GEM Magnet
WBS Dictionary
Rev 4 - 11/16/92

40.0 Magnet Construction - This subsystem consists of all of the assemblies and elements required to provide the magnetic field in the interior of the detector. It includes the coils, coil forms, radiation shields, cold mass supports, vacuum vessels, end poles, current leads, cryogenic (LN and LHe) systems, and power and protection systems. It also includes components required to support the solenoid and end poles from the ground, the support for the central detectors, the attachment points for the muon and calorimeter subsystems, and any special tooling necessary to install any of these components. This subsystem does not include the building cranes, assembly buildings, or any concrete support features below the detector. Major interfaces are with: underground hall, above-ground facilities, muon subsystem, calorimeter subsystem, and the ring magnet system. This element also includes all R&D activities for the magnet as well as completion of the conceptual/preliminary design.

40.1 Magnet Subsystem R&D - This element covers research and development activities associated with the GEM magnet subsystem. This element does not include efforts to perform preliminary or detailed design of the magnet subsystem. It does include effort to develop tooling for conductor production, as well to conduct tests of proposed component concepts.

40.1.1 Conductor Development - This element covers all activities required to verify the design of the conductor. It includes efforts to fabricate short lengths of prototype conductor, and test the performance.

40.1.2 Joint Development - This element covers all R&D activities associated with the joints between superconducting cables in the magnet. It includes subscale tests to verify the concept, as well as full-scale tests of actual joint designs.

40.1.3 Winding Development - This element covers all activities required to develop and demonstrate the winding techniques for the magnet. It includes tests of the bending performance of the conductor and initial trial winding on short lengths of dummy conductor. It also includes the acquisition of key pieces of winding tooling.

40.1.4 Component Development - This element covers the development of special components for the magnet subsystem. It presently includes only the development and demonstration of cryogenic insulating breaks.

40.2 Design Completion - This element consists of all design activities required for the magnet subsystem after Authorization to Proceed with construction phase. It includes preliminary and final design, analysis, trade studies, refinement of design requirements, preparation of final drawings, and preparation of presentations for the System Requirements Review (SRR), the Preliminary Design Review (PDR), and the Critical Design Review (CDR). It also includes preparation of all deliverables associated with the design, including data, drawings, reports, and presentations. Design activities are defined as complete when the procurement package for a given component is ready for solicitation of bids. This element does not include the costs for soliciting bids or placing contracts or orders for fabrication. It also does not include any effort required during fabrication to monitor progress or provide technical oversight.

40.2.1 Coil Assemblies Design - This element consists of the design of all components which are physically a part of the completed coil assemblies; these assemblies are the parts which will be assembled above-ground and delivered for installation in the underground hall. This includes the coils, the thermal radiation shields, the vacuum vessels, the cold-mass supports, and all cryogenic piping and distribution and current bussing which are within the vacuum-vessel boundary. This does not include the components required to physically support the coil assemblies, the forward field shapers, or the central detector support. It also does not include local thermosyphon supply dewars or any cryogenic piping external to the vacuum vessel boundary. Major interfaces are with the underground hall, the above-ground facilities, the poles/pole supports, the muon subsystem, and the central detector support.

40.2.1.1 Cold Mass Subassemblies Design - This element consists of the design of two (approx) 15m long magnet coils only, which are made up of conductor wound on coil forms, with any required diagnostics installed. It includes the design of all parts and tooling required to produce the coils, as well as assembly of multiple short coil segments, if the coil is designed in that manner. This does not include the LHe thermosyphon or LHe forced-flow cryogenic piping/distribution. Design major interfaces are with the cold-mass supports, the vacuum vessels, the radiation shields, and the internal cryogenic systems.

40.2.1.1.1 Coil Form Design - This element comprises the design of the coil form within which the coil is wound. The coil form includes ribs to accept axial conductor loads, attachment points for the cold-mass supports, and ground-plane insulation.

40.2.1.1.2 Conductor Design - This element includes all of the design required to provide the conductor which makes up the coil. The conductor includes the SC wire, the protective sheath, and the passage for the forced-flow LHe. This element includes all of these parts, even if they are designed to be physically separate. The conductor is to be delivered on large spools, ready for winding into the coil forms.

40.2.1.1.3 Diagnostics Design - This element includes the design of all hardware and activities associated with any control or diagnostic elements which are actually installed on the coil subassembly. This includes voltage taps, temperature sensors, etc. This element does not include the electronics necessary to read out these sensors or to effect control.

40.2.1.1.4 Winding Tooling Design - This element includes the design of all of the tooling required to remove the conductor from the storage drums and wind it into final position in the coil form. Any tooling or hardware design required for gluing or otherwise affixing the conductor in place is included in this element.

40.2.1.1.5 Winding & Testing Design - This element covers the design of all of the processes and activities required to complete 24 ea 1.2m long coil segments, starting from the basic parts identified in 4.1.1.1.1-4. This includes the design of all processes required to prepare the coil form for winding, to actually remove the conductor from the storage drum and wind it into final position in the coil form, to install any diagnostics, sensors, or controls, to complete the electrical and fluid connections within the coil segments, and to perform tests as required to verify proper function at this level. This does not include any design required to stack or assemble the segments to form completed cold-mass halves, or to install the radiation shields, cold mass supports, or vacuum vessels. Because of the size of the completed coil subassemblies, all assembly effort take place on-site at SSCL.

only testing performed prior to installation of the internal detector subsystems; testing of the detector as a whole is included in operations.

40.3 Fabrication & Assembly - This element consists of all fabrication and assembly activities within the magnet subsystem. It includes all activities between assembly of procurement packages and beginning of installation. The first activity within this element is solicitation of bids for fabrication. The last activity included in this element is final inspection and checkout before installation begins. This element includes all labor and materials required for fabrication and assembly, including direct touch labor, first-line supervision, engineering oversight, inspection, purchasing, expediting, and engineering effort required to respond to discrepancies.

40.3.1 Coil Assemblies Fabrication & Assembly- This element consists of fabrication and assembly of all the components which are physically a part of the completed coil assemblies; these assemblies are the parts which will be assembled above-ground and delivered for installation in the underground hall. This includes the coils, the thermal radiation shields, the vacuum vessels, the cold-mass supports, and all cryogenic piping and distribution and current bussing which are within the vacuum-vessel boundary. This does not include the components required to physically support the coil assemblies, the forward field shapers, or the central detector support. It also does not include the local thermosyphon supply dewars or any cryogenic piping external to the vacuum vessel boundary. Major interfaces are with the underground hall, the above-ground facilities, the poles/pole supports, the muon subsystem, and the central detector support.

40.3.1.1 Cold Mass Subassemblies Fabrication & Assembly - This element consists of fabrication and assembly of the two (approx) 15m long magnet coils only, which are made up of conductor wound on coil forms, with any required diagnostics installed. It includes all activities, parts, and tooling required to produce the coils, as well as assembly of short coil segments, if the coil is designed in that manner. This does not include the LHe thermosyphon or LHe forced-flow cryogenic piping/distribution. Major interfaces are with the cold-mass supports, the vacuum vessels, the radiation shields, and the internal cryogenic systems.

40.3.1.1.1 Coil Form Fabrication & Assembly - This element comprises fabrication and assembly of the coil form within which the coil is wound. The coil form includes ribs to accept axial conductor loads, and attachment points for the cold-mass supports.

40.3.1.1.2 Conductor Fabrication & Assembly - This element includes fabrication and assembly of all activities required to provide the conductor which makes up the coil. The conductor includes the SC wire, the protective sheath, and the passage for the forced-flow LHe. This element includes all of these parts, even if they are designed to be physically separate. The conductor is to be delivered on large spools, ready for winding into the coil forms. This does not include the cost of facilities in which the work will be performed. It does include raw materials, conductor processing, storage drums, tooling, etc.

40.3.1.1.3 Diagnostics Fabrication & Assembly - This element includes fabrication and assembly of all hardware and activities associated with any controls or diagnostics elements which are actually installed on the coil subassembly. This includes voltage taps, temperature sensors, etc. This element does not include the electronics necessary to read out these sensor or to effect control.

40.3.8 Return-Field Mitigation Fabrication & Assembly - This element covers fabrication and assembly of all of the hardware required to shield individual components or small volumes from the return field of the magnet, or alternatively, the additional cost of over-specifying components so they will work properly in the field. This includes shielding for vacuum pumps, gages, etc, as well as shielding of local counting rooms and electronic racks below ground. It does not include hardware to shield the above-ground field.

40.3.9 Installation Tooling Fabrication & Assembly - This element covers fabrication and assembly of all of the hardware temporarily required for installation of magnet subsystem components into their final positions. It does not include any hardware which will be a permanent part of the installation. It also does not include provision of the cranes in the underground hall or the heavy-lift crane for lowering major assemblies down the access shaft.

40.3.9.1 Coil Assemblies Tooling Fabrication & Assembly - This element includes fabrication and assembly of all of the tooling required to handle the coil assemblies from the location at which they were tested above ground to their final position in the underground hall. It also includes any tooling required to anchor them and their support hardware in place and align them. This includes any tooling required to move parts to the access shaft, any specially-built rigging which connects the parts to the shaft crane, tooling to move the parts from below the crane to their installed position, and any tooling required for alignment measurement or alignment movement. This element includes only the specially-built tooling which is in addition to the coil and FFS transporters, and normal strongbacks which would be supplied by rigging companies.

40.3.9.2 Central Detector Tooling Support Fabrication & Assembly - This element covers fabrication and assembly of the tooling required to handle, align, and install the central detector support.

40.3.9.3 Forward Field Shapers Tooling Fabrication & Assembly - This element includes fabrication and assembly of all of the tooling required to move the pole assemblies from the surface to the underground hall and place them in position. If they are to be assembled in the underground hall, the tooling required for assembly is included here as well. This also covers tooling required to mount the supports, transporters, and align the poles.

40.3.9.4 Testing Equipment Fabrication & Assembly - This element covers fabrication and assembly of all of the equipment required for testing the magnet system after installation. The primary testing equipment will be a system for mapping the magnetic field inside the magnet.

40.4 Installation & System Testing- This element consists of all installation activities within the magnet subsystem. It includes all activities beginning when components are tested and ready for installation, and ending when they are in place, aligned, checked out, tested, and accepted. This element also includes preparation of all operating and maintenance documentation. This element includes all labor and materials required for these activities, including touch labor, supervision, surveying, engineering oversight, engineering/physics review of test data, preparation of test reports, and resolution of discrepancies during installation. It does not include project management activities.

40.4.1 Installation - This element covers all of the actual installation of magnet subsystem hardware on-site at SSCL. It includes installation of the magnet assemblies in the

Cost Estimating Guidelines for GEM Electronics Subsystems

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December 16, 1992

Version 1.1

Abstract

Guidelines for a bottom-up estimate of the electronics costs for the GEM detector are summarized. This document supplements the "GEM Cost Estimating Plan"[1].

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1 Introduction

In FY92 the GEM Electronics, Trigger, and Data Acquisition subgroup conducted a preliminary estimate of the electronics costs for GEM. That analysis[2], known as "The LeCroy Estimate" was based upon a parametric, or "top-down", approach. Now that our designs are better defined and engineering teams are in place for most of the electronics subsystems, we can move forward with a traditional bottom-up estimate in anticipation of the submission of the GEM Technical Design Report (TDR) and its attendant reviews. This document is intended to outline the plans and procedures to be followed in that undertaking.

Although it is expected that the precise form of the cost estimates will vary depending on the system being estimated and on the engineering team doing the estimates, it is hoped that where possible uniform formats and procedures will be followed. This will facilitate comparisons between subsystems and will help make duplications and omissions easier to spot.

This document is intended to supplement and not supersede the guidelines set forth in reference [1]. That document should be read carefully by all design teams performing electronics cost estimates.

2 Scope of WBS 50.

The GEM Electronics, Trigger, and Data Acquisition (ETDA) subsystem (WBS 50.) includes:

- All front-end electronics from the preamplifiers through to the event builder.
- The Level 1 trigger systems.
- The DAQ system.
- Crates, racks, high-voltage power supplies (HVPS), low-voltage power supplies (LVPS), and the cooling systems¹ that service them.

WBS 50 does *not* include:

- Readout devices such as phototubes.
- The Level 3 computers or the slow control system—i.e. ancillary systems. (By convention, sensors and actuators for the slow control are included as part of the subsystem that they serve. The electronics is consistent in this regard in that the actual sensors for, say, low-voltage readout, will be included as part of WBS 50, whereas the high-level software and hardware to process the data from these sensors will be included as part of the online computing & slow-control WBS tree.

¹The electronics chilled water system is restricted to what is usually termed "technical systems". The main supply of chilled water, a "conventional system", is not included. A similar boundary exists for the delivery of AC-power.

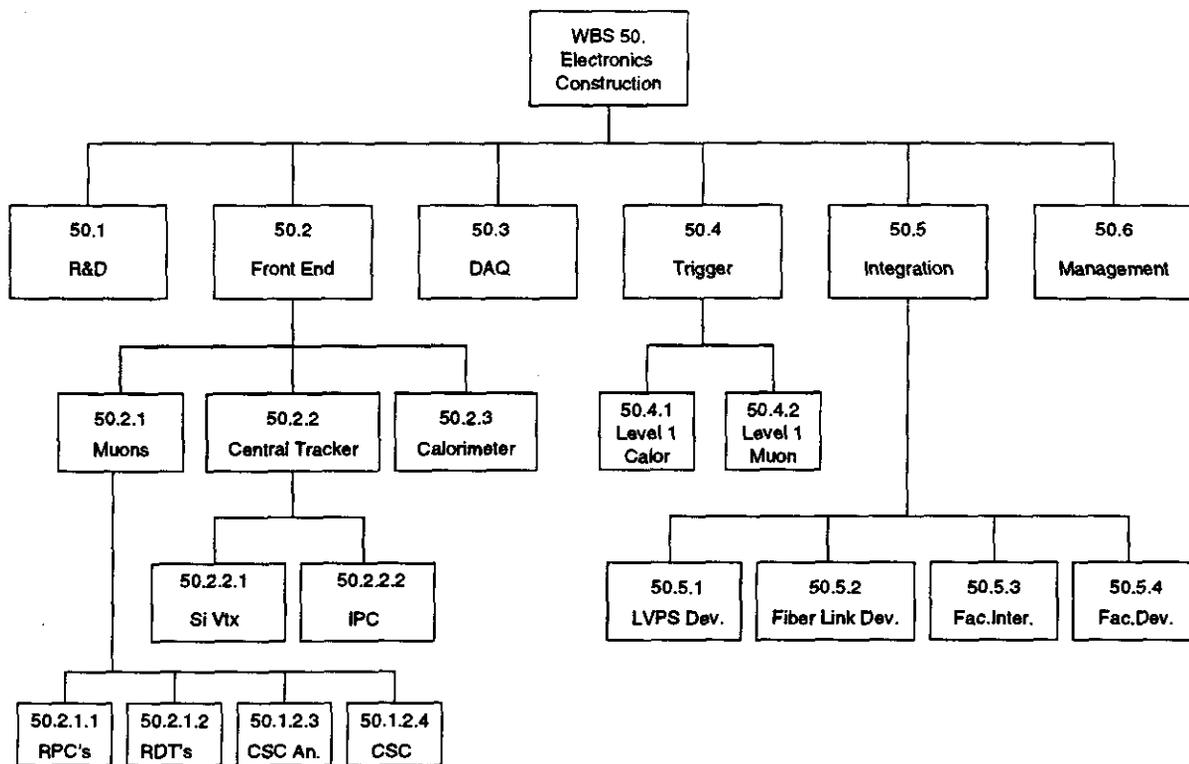


Figure 1: The overall structure of the electronics portion of the GEM WBS.

3 WBS Structure

The general structure of the GEM WBS 50 is shown in figure 1. There are three major subsystems: front end, trigger, and data acquisition. This format was chosen by SDC and was adopted by GEM in keeping with a general policy of adopting the SDC approach where there are no compelling reasons to do otherwise. Our current ideas call for the Level 2 trigger to be implemented as an integral part of the event builder and processor farm, in which case the block labeled "Level 2 Trigger" will actually be moved to the data acquisition portion of the WBS.

The R&D portion of WBS 50—i.e. WBS 50.1—includes all work aimed at the development of the final production electronics. Electronics bought or built to support *detector* development work—e.g. NIM or CAMAC modules for beam tests—will in general be included as part of the corresponding detector subsystem. The inevitable occurrences of cases in gray areas will be resolved on an ad-hoc basis.

3.1 Project Phases

Figure 2 shows the substructure that appears underneath each front-end subsystem.

Each subsystem is divided into four "phases":

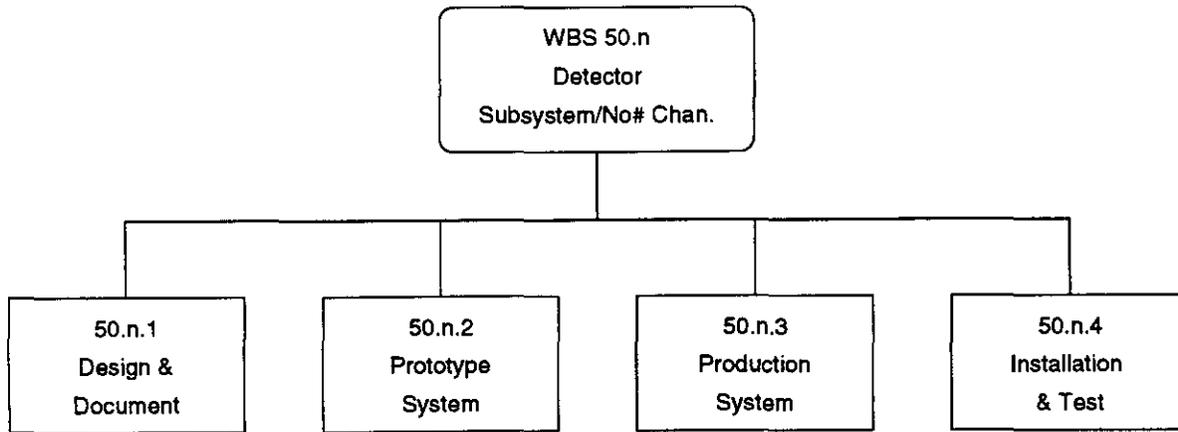


Figure 2: Suggested WBS structure for an electronics subsystem. Each major branch represents a “phase” of the project.

- **Documentation Package:** This part of the WBS includes the cost of preparing and reproducing a set of final design documents (conceptual design document, block diagrams, schematics, layouts, *etc.*) and updating them as the design work progresses. It is understood that much of the design package will result naturally from the R&D and prototype (see below) phases of the work; this WBS element reflects the direct costs of collecting the various documents and checking their accuracy and completeness as well as maintaining an up-to-date set of as-built drawings. Note that in the LeCroy report, there was a blanket assumption of 0.5 man-years for each subsystem. In this work a more realistic estimate should be attempted.
- **Prototype System:** This part of the WBS reflects the activity required to go from the R&D phase of a subsystem to a pre-production prototype system² In some sense it represents the cost of producing the first channel. In estimating the personnel and material expenses for the prototype system, one should assume that as a result of the R&D program the engineering team doing the design has a fairly good idea of what must be done, but is starting with a blank sheet of paper. Prototype system costs include the cost of the design team and the cost of an appropriate number of fabrication iterations for PCB’s and IC’s. The level of effort and expense will therefore depend on the degree of difficulty and uncertainty in the design. Much of what is now being done under the guise of “GEM Electronics R&D” is actually part of the prototype system WBS. This part of the WBS should also include the costs of any special-purpose test fixtures for IC’s and PCB’s.

The size of the prototype system will depend on the subsystem in question. As a general rule the number of channels in the prototype system will be the *smaller* of 1000 channels or 10% of the number of channels in the production system. Exceptions may arise, for example, in cases where more channels are needed to test prototype

²The designation “prototype”, which is employed for historical reasons, may be confusing to some; “pilot” or “pre-production” system is perhaps more descriptive.

detectors, or where the economics of IC fabrication dictate larger or smaller runs. In general much of the EDI&A for a given subsystem will occur in these branches of the WBS. Note that the roll-up of this part of the WBS represents a fixed cost that is (nearly) independent of the number of channels to be built.

- **Production System:** This part of the WBS contains the costs associated with the mass-production of the electronics. Since most of the labor associated with actual production—e.g. loading circuit boards—will be done by outside contractors, this category will be dominated by procurement and fabrication. There will, however, be EDI&A activities associated with managing the various procurements, verifying that vendor-supplied materials meet GEM specifications, and subassembly testing and rework. Costs associated with shipping and/or storing electronic subassemblies should be included here.
- **Installation:** This part of the WBS includes the costs associated with the installation of the electronics, starting with the delivery of the subassemblies to the detector site.

3.2 Standard Template

Experience with other projects has shown that electronics cost estimates tend to go awry not so much because particular items have been underestimated, but rather because some items have been omitted altogether. To help avoid such occurrences a standard “template” for the prototype and production phases of each subsystem has been established. The standard template is illustrated in block-diagram form in figure 3.

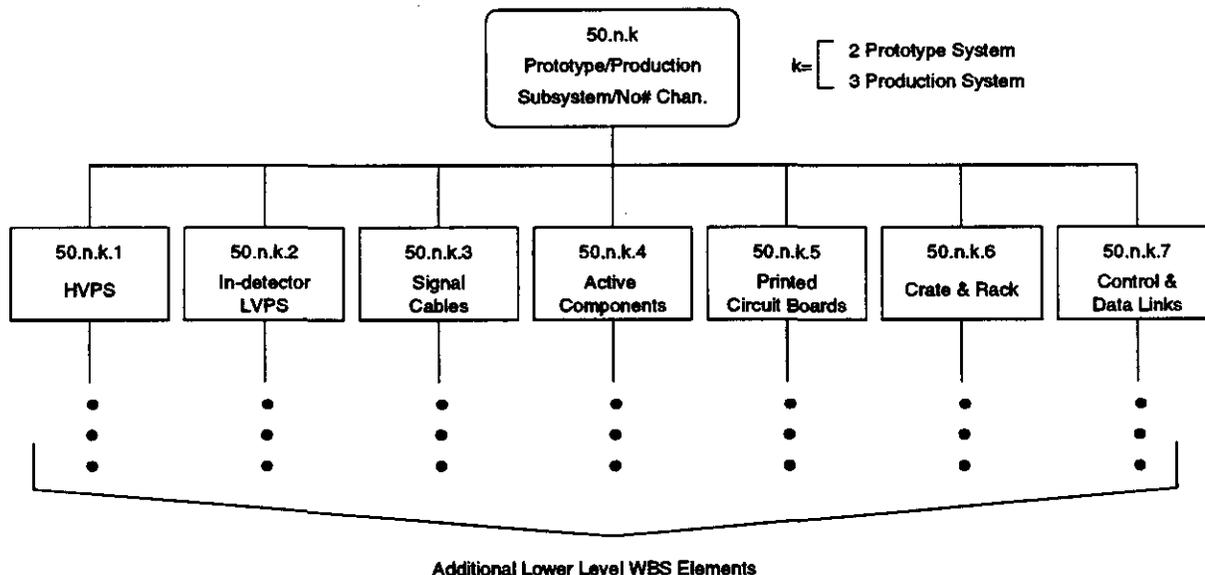


Figure 3: The “standard template” to be followed by each front-end subsystem.

This template will serve as a checklist. Some subsystems will not use one or more of the items on the list. In this case the corresponding lines in the WBS can be set to zero or

omitted entirely. In general there will be additional WBS levels below the template items, but since these will be highly dependent on the subsystem, they will not be spelled out in the list that follows. Table 13 of reference [1] shows the complete electronics WBS, which was derived from reference [2]. Although the WBS will no doubt evolve with time—particularly at the lowest levels—*unnecessary WBS changes should be avoided.*

The items in the standard template are listed below:

- **High Voltage Power Supply (HVPS):** This includes the cost of HVPS's and their attendant cabling. HV includes wire-chamber high-voltages and bias voltages for ionization devices.
- **In-detector Low Voltage Power Supplies (LVPS):** This includes the cost of LVPS's and their attendant cabling, cooling, and monitoring, for low-voltage power *delivered to in-detector (IND) elements.* Low-voltage power and cooling for rack-mounted electronics, whether they be in the electronics room (ER) or mounted on the detector (OND) is *not* included in this part of the WBS, but rather will be accounted for via a "slot charge", assessed for each board that plugs into a crate (see crate cost estimates below).
- **Signal Cables:** This includes the cost of all cables and their connectors running between the IND electronics and the OND electronics. Signal paths between the IND and OND areas and the ER are assumed to be fiber optics and will be accounted for in a different portion of the WBS.
- **Active Components:** This includes custom and semi-custom IC's and hybrids. Commercially available IC's that represent a non-negligible fraction of the overall cost—e.g. micro-processors, RAM's, high-performance op-amps, etc.—should also be included. The cost of acceptance testing of IC's should be included here.
- **Printed Circuit Boards (PCB's):** This includes all "substrates", such as standard fiber-glass epoxy boards or multi-chip modules (MCM). In addition to the substrate proper this includes the cost of miscellaneous low-cost commercially available IC's, and other such "common" parts— e.g. resistors, capacitors, board-mounted connectors, etc. It is anticipated that many designs will not be sufficiently evolved to allow one to account in detail for all such parts. In these cases a concerted effort should be made to identify and cost items that are likely to be cost drivers—e.g. connectors. Finally, this item includes the cost of assembling and testing the substrates, as well as any administrative expenses associated with procurement and QA.
- **Crate Costs:** It is anticipated that GEM will adopt a standard design for all OND and ER crates. A cost estimate for these crates—including mechanics, LVPS, cooling, monitoring, and controller (where appropriate), etc.—will be worked out separately by the GEM electronics integration group at the SSCL. The cost of these items will appear in the subsystems as a "slot charge" assessed for each module. Since the development of these crates will be carried out in common, the prototype-phase costs for these

items will be minimal for most subsystems. A modest allowance, however, should be made to allow the design times to acquire and test the standardized crates with their electronics. As a working hypothesis, designers should assume that these boards are 9U × 400 mm VME cards. Additional details will be made known as they become available.

The GEM DAQ group will augment the crate costs with a standard DAQ controller and data link cost to be included as part of the slot charge.

- **Control & Data Links:** In many cases these costs will be included as part of the controller portion of the slot charge discussed above. In some cases, for example rad-hard links between IND electronics and the OND area or the ER, special links will be needed in which case their cost should be reflected here.

3.3 WBS Assignments for Each Subsystem

The high-level WBS designations are shown on a subsystem-by-subsystem basis in table 1.

Table 1: High Level WBS Assignments

Major Branch	Subsystem	WBS Designation
Front End	Resistive Plate Chambers	50.2.1.1
	Round Drift Tubes	50.2.1.2
	CSC 2nd Coordinate	50.2.1.3.1
	CSC Cathode	50.2.1.3.2
	Silicon Tracker	50.2.2.1
	IPC	50.2.2.2
	Calorimeter	50.2.3
Data Acquisition	Substructure to be determined	50.3
Trigger	Level 1 Calorimeter Trigger	50.4.1.1
	Level 1 Muon Trigger	50.4.1.2

4 Personnel Costs

The cost estimate should reflect the cost of all personnel involved in the development, design, manufacturing, installation, and test of GEM electronics, *except* for physicists, who as a general rule are not included in detector cost estimates. Exceptions to the “no-physicist” rule may occur in cases where physicists have taken on full-time or nearly full-time engineering or management responsibilities (see the section on offsets below).

In cases where it is reasonably well known that a certain activity will take place at a particular *U.S.* institution the actual salaries and burdens for the team at that institution

should be used. In cases where this is not known, average rates should be employed as detailed in reference [1].

As noted, the costs of PCB assembly and other such labor-intensive tasks will likely appear as procurement costs since these jobs will probably be farmed out to assembly houses.

Since the conversion between person-hours and person-years varies from institution to institution, GEM has adopted a policy of calculating all labor in *hours*, as set forth in reference [1].

5 Foreign Contributions & Other Cost Offsets

The general procedure is to cost all aspects of the detector assuming that it will be built entirely in the U.S. using DoE OSSC funds. In practice we anticipate substantial foreign contributions of both a direct and an "in-kind" nature. These contributions will be accounted for as "cost offsets" in the GEM funding plan and are therefore beyond the scope of this estimate.

A similar principle applies in the case of U.S. engineers supported with non-SSC funds (i.e. DoE, NSF, TNRLC, etc.). The work to be done by these individuals should be included in the cost estimate even if it is known that they will not be supported by GEM. Their support will be included as a cost offset in the overall GEM funding plan.

As a consequence some items (for example, engineering or management functions performed by base-program funded physicists) appearing in the cost estimate will be cancelled by identical items appearing in the funding plan. An informal list of any such items identified during the course of the estimate should be included as an appendix to each design team's cost estimate; this information may prove useful to the spokesmen as they prepare the GEM funding plan.

6 Cost Estimate Deliverables

Each design team participating is expected to provide the following documents as part of their cost estimate.

6.1 Design Description

The design description should comprise:

1. A statement of the scope of the subsystem being estimated. This will be important in identifying possible areas of overlap and/or possible areas of incomplete coverage.
2. A table (or tables) that specifies the performance requirements for the subsystem in question. Where appropriate the table should be supplemented by notes, explaining the conditions under which the specifications are to be met.

3. A block diagram that clearly shows the functional blocks of the subsystem and their interconnections. The diagram should be supplemented with descriptive text and any timing diagrams, etc., that will be of help in establishing how the subsystem operates. Circuit diagrams should be included when available. As the estimate progresses and the WBS number assignments are fixed, functional blocks should, where possible, be labeled according to their WBS designations.
4. A mechanical drawing that indicates the physical layout of the system. The drawing should show the approximate outline of IC's and connectors and the assumed physical dimensions of the boards. Cables and connectors should also be shown. As the estimate progresses and the WBS number assignments are fixed, components should be labeled according to their WBS designations.

6.2 The WBS Dictionary

A WBS dictionary that clearly defines which elements of the system are included under a particular WBS element should be provided. In general the WBS should be structured according to the guidelines of section 3. In cases where this is not possible, variances from section 3 should be clearly noted. It is anticipated that WBS designations may in some cases be poorly defined at first and probably evolve with time. Design teams should do the best that they can in the early stages. Table 1 shows the current high-level WBS assignments.

6.3 Basis of Estimate & Backup Data

As part of the move from the top-down analysis to a full bottom-up approach, it is necessary to substantiate our costs to the greatest extent possible. In practice this means that whenever possible costs should be supported with vendor quotes. Copies of these quotes and any relevant information should be included in the cost documentation for each subsystem.

In areas of particularly rapid technological advance, cost estimates may be based on projections of historical trends. This should be done only for items that are cost drivers and only in areas that are generally recognized to be rapidly advancing—e.g. computers, memory, and communication links. The rationale for any such estimates should be set forth in the basis of estimate.

6.4 Cost Estimating Input Forms

The primary mode of information transfer between the subsystem designers and the team responsible for the overall rollup of GEM costs are the "SSCL GEM Detector Success Cost Estimating Input Forms". These summarize the costs associated with each WBS line item. Sample and blank forms are included as an appendix.

6.5 Channel Summary Data

Estimators for front end systems should provide a table summarizing which costs elements scale with the channel count and which cost elements correspond to fixed costs. For costs elements that scale with the channel count, cost-per-channel summaries should be provided. This information is needed to assess the impact of channel count on overall subsystem costs.

6.6 Informal List of Potential Cost Offsets

This applies mainly to U.S. universities. As noted in section 5, the cost estimates must include the cost of all labor and materials, regardless of their source. However, since the cost estimating process forces one to ponder what must be done and who might do it, it is a convenient time to identify and list potential U.S. cost offsets. This information may prove useful to the GEM spokesmen at a later date.

7 Standard Costs

Certain items, such as standard printed circuit boards, will occur in many places throughout the GEM electronics subsystems. To introduce some level of standardization and to avoid duplication of effort in determining these costs we will compile a menu of "standard" items and their associated costing rules. A preliminary version of that menu follows.

7.1 Printed Circuit Board Manufacture

Surveys of vendors and comparisons with other cost estimates reveal that the cost of standard multi-layer printed circuit boards in large quantities is reasonably well approximated by

$$\text{Cost} = \$0.25 \times N_{\text{pair}} \times A$$

where N_{pair} is the number of layer-pairs and A is the area of the board expressed in in^2 . For example, in quantity, an eight-layer FASTBUS board would cost $\$0.25 \times 4 \times (14.4 \times 15.9)\text{in}^2 = \$ 229$.

7.2 Printed Circuit Board Assembly

Based on discussions with United Mfg. Corp. in New Castle, Delaware it appears that the cost of loading and soldering circuit boards is given by the following rules:

- 1) Assembly cost of \$ 0.03 per lead
- 2) Material parts at cost +20%
- 3) The cost of test fixtures is about \$ 17 K - \$ 20 K. This eliminates the need for other types of inspection. Running of the tests is built into the \$ 0.03 per pin of item 1.

7.3 Integrated Circuit Costs

Rule-of-thumb cost data[3] for a typical 4-inch wafer CMOS process are shown in table 2. In addition to the production costs, mask charges of \$ 25 K per set and test set-up charges of \$ 5 K per chip must be included. These numbers can be used for general-purpose CMOS IC's, although as their work progresses, designers should attempt to obtain quotes that are tailored to their particular application. Clearly these numbers are *not* suitable for bipolar or rad-hard IC's. Also, these data should be refined through vendor quotes in cases where IC production costs are cost drivers.

Table 2: Rule-of-thumb costing data for CMOS IC's. The tabulated costs do *not* include mask charges of \$ 25 K per set and test fixture setup charges of about \$ 5 K.

Size	Area	Yield	Fab.	Pkg	Test	Total
Tiny	6.8 mm ²	70%	\$ 2.05	\$ 1.00	\$ 7.50	\$ 10.55
Small	35 mm ²	65%	\$ 11.17	\$ 1.50	\$ 8.00	\$ 20.67
Medium	50 mm ²	60%	\$ 17.65	\$ 2.00	\$ 8.50	\$ 28.15

8 Glossary of Abbreviations

CSC Cathode Strip Chamber

DoE Department of Energy

EDIA Engineering, Design, Inspection, and Administration.

ER Electronics Room. The forward electronics room, which is located in a shaft near the detector hall. Equipment in this room will be accessible with the beam on, with the possible exception of very-high luminosity running.

IC Integrated Circuit, assumed to be monolithic unless stated otherwise.

IND IN-Detector electronics—i.e. electronics that is mounted within the magnet volume and is therefore fairly inaccessible.

IPC Interpolating Pad Chamber

HVPS High Voltage Power Supply. Used to bias wire chambers, phototubes and ionization devices.

LVPS Low Voltage Power Supply. Used to power electronics.

OND ON-Detector electronics—i.e. electronics that is mounted on or near the magnet in the experimental hall. This electronics is accessible when the collider is off.

OSSC Office of the SSC.

PDT Presurized Drift Tube (now called RDT).

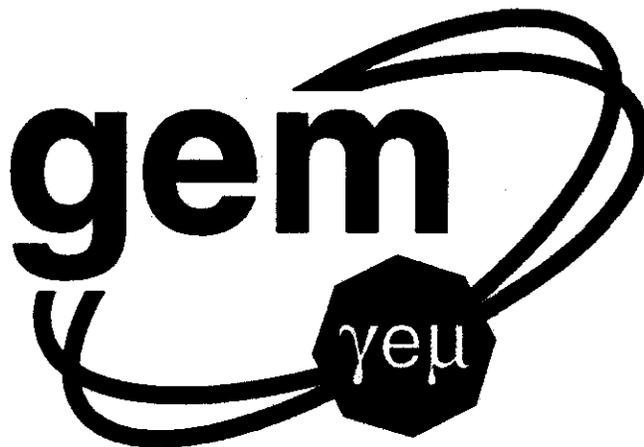
RDT Round Drift Tube (formerly PDT).

QA Quality Assurance.

WBS Work Breakdown Structure.

References

- [1] "GEM Cost Estimating Plan", Rev. F, October 1992.
- [2] "Electronics Cost Estimate", N. Lau, D. Marlow, & R. Sumner, GEM IN-92-12 (Rev-A), June 1992.
- [3] "Calorimeter and Shower Max Electronics: 1992 Progress Report on Conceptual Design, Cost, Schedule, and Critical R&D", SDC Note prepared for the SDC Calorimeter Electronics Review Committee, (unpublished) Sept. 1992.



Silicon Vertex Electronics

Brad Cooke

DIGITAL STORAGE AND COMPRESSION

GENERAL SPECIFICATIONS:

- 60-62 MHz CLOCK
- RADIATION (PER YEAR) (LEE & WATERS)
 - i) HADRONS: FLUX = $1.5 \times 10^{13} / \text{cm}^2$, 0.4 MRADS (Si) @ 10 cm
 - ii) NEUTRONS (BACKSCATTER BORON-POLY): < 100 KeV FLUX = $3.3 \times 10^{12} / \text{cm}^2$,
> 100 KeV FLUX = $1.9 \times 10^{12} / \text{cm}^2$
 - iii) GAMMA:
- SEU TOLERANT (CIRCUIT), LATCH-UP RESISTANT (DEVICE)
- NUMBER OF ASSEMBLIES (1/2 LADDERS) = ~ 1250
- STRIP-DETECTORS/ASSEMBLY/SIDE = 640/3.3 cm (PITCH = 50 microns)
- MEAN TRACK/ASSEMBLY/SIDE/16 ns = 1 @ $10^{33} / 18 \text{ cm}$, 2 @ $10^{34} / 18 \text{ cm}$
- MEAN STRIPS-HIT/TRACK/ASSEMBLY/SIDE/16ns = 2 @ $10^{33} / 18 \text{ cm}$, 2 @ $10^{34} / 18 \text{ cm}$
- MAXIMUM TRIGGER RATE (LEVEL 1) = 100 KHz

SYSTEM PERFORMANCE:

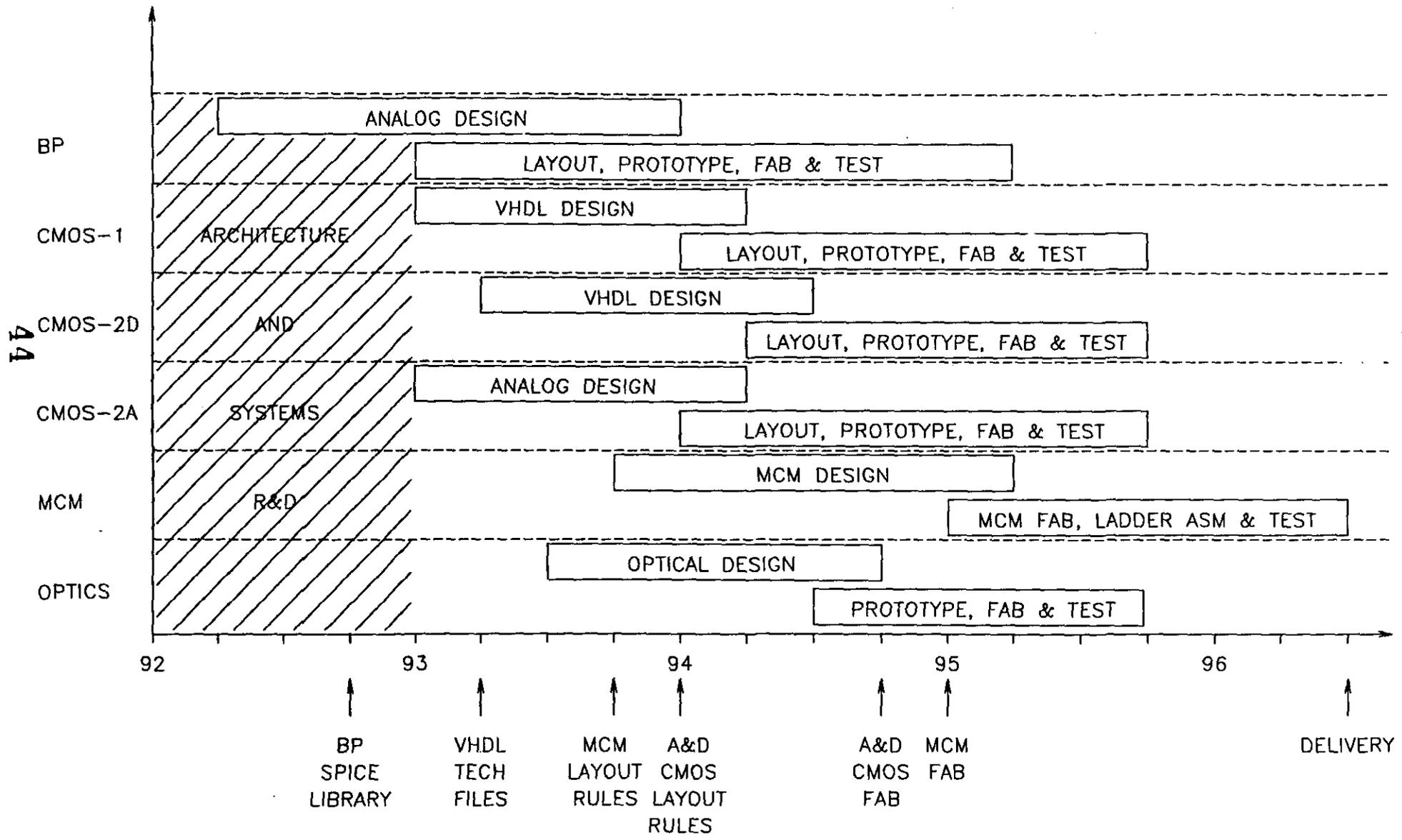
- RESET FREE
- PHASED CLOCK (BETWEEN LOCAL AND MASTER)
- PROGRAMMABLE INPUT LATCH (RISING OR FALLING EDGE)
- TRIGGER LATENCY = $128 \times 16 \text{ ns}$ ~~or $288 \times 16 \text{ ns}$~~ (~ 2 ~~microseconds~~ microseconds)
- PROGRAMMABLE TRIGGER APERTURE (0 - 4 X 16 ns)
- CONSECUTIVE TRIGGERS = 2
- DATA DRIVEN STORAGE EFFICIENCY = $99.9\% \times 6$ @ ~~1~~ LEVELS, (TRGL = $128 \times 16 \text{ ns}$)
- COMPRESSION DELAY = 2 microseconds
- MEAN COMPRESSED BW = 7.5 - 10 Mbits/s @ 10^{33} , 15-20 Mbits/s @ 10^{34} per 640

- TESTABILITY

- DEPENDENCY

SSC/GEM SILICON ELECTRONICS

MILESTONES



GEM SILICON-TRACKER READOUT ARCHITECTURE

I. SUMMARY

The GEM silicon-tracker readout electronics architecture presented here is an optimized system-level design composed of the following subsystems: i) Multi-chip-carrier (MCM). ii) Analog amplifier, waveshaper and discriminator. iii) Digital storage, compression and control. iv) Optical readout, clock and trigger distribution. The system design balances and distributes the design requirements amongst the above subsystems. The design requirements, in addition to specifications and cost, include ease of realization, assembly complexity and testability.

The basic 24/36 cm ladder assembly is shown in Figure 1. The base assembly unit is composed of 12/18 cm half ladder. A single MCM will provide the interface electronics for both the top 640 and bottom 640 strip detector channels. A blow-up of the MCM is illustrated in Figure 2 while Figure 3 shows the chip-layout. The role of the MCM is dual in that it provides an efficient electro-mechanical interface between the electronic and mechanical systems. The strip-detector wafer is supported by the MCM through a thermally-insulating spacer bridge, while the MCM itself is mounted (glued) to the cooling ring (heat spreader is optional). Note that all mechanical contacts in this design straddle the thermal symmetry axes in order to minimize positional drifts due to thermal expansion and contractions. Power and the digital-slow-control-bus are connected to the cooling-ring cabling through an edge connector, while the clock and trigger are brought in through 100-ohm micro-cables from the 1:8 phase-locked optic to coax distribution modules situated on the cooling ring. Data from the MCM is transmitted through the fibre optic link that also runs along the space frame/cooling ring.

The single MCM assembly represents a self-contained modular unit. The modularity is due to the integration of the digital control circuits (CMOS-2) and Input/output (slow control bus and optical driver) with the main analog and digital signal processing circuits. Advantages of modularity include improved electronic system integration, reduction in assembly labor and, of great importance, a significant increase in reliability and testability (through on-board automated testing). Because of the increased testability, the amount of time, labor and equipment required to test the system are significantly reduced.

Analog signals from the strip detectors are coupled through the MCM extension flex-cables into the analog chips for amplifying, waveshaping and discriminating. Hits detected by the amplifier are passed on to digital data-processing.

The digital data-processing design consists of a latch, data storage and compressor. The data latch accepts a non-synchronized (relative to the system clock) analog pulse of random duration and generates a single, synchronized 16-ns digital pulse. Information is then stored for the duration of the trigger extraction cycle using data driven architecture. Triggered data is then passed on for data compression through both clustering and single hit extraction and then transmitted out. It is important to note that the SSC inner-detector strip occupancy is sparse and the trigger attenuation is high, allowing for both time and data compression. Based on the data flux, strip occupancy and trigger specifications stated below, the architecture will require a mean data bandwidth of < 20 Mbits/sec/1280 strips (luminosity $= 10^{33}$). A single, time-division-multiplexed (TDM), 62 Mbits/sec LED channel is provided. Figure 3 shows the general digital architecture. There are 10 storage/compressor CMOS-1 chips (5 for each 640

strips), 1 controller CMOS-2D chip, 1 TDM BP-2 chip, and 1 62 Mbits/sec LED. Each CMOS-1 chip contains 128 channels, hence 5 chips are used for the "top" 640 strip and 5 chips for the "bottom" 640 strips. Both sets of chips use the same CMOS-2D chip and optical channel (31 Mbits/sec bandwidth per chip-set).

II. SPECIFICATIONS

II.A.1 GENERAL SPECIFICATIONS

- i) 62.5 MHz clock.
- ii) 5 MRads (Si) total dose over 10 years. (40% 1MeV Neutrons, 40% 1GeV Protons, 20% >1Mev Gamma).
- iii) Single Event Upset (SEU) tolerant, Reset free.
- iv) Number of assemblies (1/2 ladders): ~1250 .
- v) Strip-detectors/assembly/side: 640/3.3 cm (pitch = 50 microns).
- vi) Mean tracks/assembly/side/16 ns: 1 @ $10^{33}/18$ cm, 2 @ $10^{34}/18$ cm.
- vii) Mean strips-hit/track/assembly/side/16 ns: 2 @ $10^{33}/18$ cm, 2 @ $10^{34}/18$ cm.
- viii) Maximum trigger rate (Level 1): 100 KHz.
- ix) Trigger latency: 256 X 16 ns (~ 4 micro-seconds).

II.B.1 MULTI-CHIP-MODULE

- i) Dimensions: W = 33 mm, L = 61 mm, t = < 1mm.
- ii) IC dimensions (W x L x t) and quantity per MCM:
 - BP-1 (Analog BiPolar): 5.85 mm x 6.2 mm x 250 microns, 10.
 - CMOS-1 (Digital CMOS): 5.85 mm x 10 mm x 250 microns, 10.
 - CMOS-2D (Digital CMOS): 7.5 mm x 10 mm x 250 microns, 1.
 - CMOS-2A (Analog CMOS): 5 mm x 5mm x 250 microns, 1.
 - TDM (Digital BiPolar): 5 mm x 5mm x 250 microns, 1.
- iii) Buried resistors or capacitors :
 - 5 V Digital 1000 pico: W mm x L mm x Z mm, 10.
 - 1.5 V Analog 1000 pico: W mm x L mm x Z mm, 20.
- iv) Surface mount device dimensions (W x L x h) and quantity per MCM:

- LED (GaAs): 5 mm x 5mm x 2.5 mm, 1.
- Edge connector: 5 mm x 15 mm x 2.5 mm, 1.

- Surface mount capacitors:
 - 5 V Digital 1 - 5 micro: W mm x L mm x Z mm, 1.
 - 1.5 V Analog 1 - 5 micro: W mm x L mm x Z mm, 2.
 - 1.5 V Analog XX micro: W mm x L mm x Z mm, 20.
 - 300 V Bias 0.1 micro: W mm x L mm x Z mm, 1 (cable mounted ?).

- 50 -100 Ohm Coax: D = 2.5 mm, 2.

II.C.1 ANALOG SPECIFICATIONS

i) BP-1 (Analog amplifier, waveshaper, discriminator):

- Quantity: 10 X number of assemblies.
- Dimensions: (W X L): 5.85 mm X 6.2 mm X 250 microns.
- Number of channels/chip: 128 @ 45 micron pitch.

ii) CMOS-2A (Analog A/D, D/A):

- Quantity: 1 X number of assemblies.
- Dimensions: (W X L): 5 mm X 5mm X 250 microns.

II.D.1 DIGITAL STORAGE, COMPRESSION, AND CONTROL

i) CMOS-1 (Latch, storage, compressor):

- Quantity: 10 X number of assemblies.
- Dimensions (W X L): 5.8 mm X 10 mm X 250 microns.
- Number of channels/chip: 128 @ 45 micron pitch.

ii) CMOS-2D (Controller):

- Quantity: 1 X number of assemblies.
- Dimensions (W X L): 7.5 mm X 10 mm X 250 microns.

iii) TDM (Time-division-multiplexed, LED driver):

- Quantity: 1 X number of assemblies.
- Dimensions (W X L): 5mm X 5mm X 250 microns.

II.E.1 OPTICAL READOUT, CLOCK AND TRIGGER SPECIFICATIONS

i) Clock: 62.5 MHz, 50% Duty Cycle, RT = 1 ns, FT = 1 ns, Jitter < 0.5ns.

ii) Trigger: 8 ns Pulse, 16 ns Period, RT = 1 ns, FT = 1 ns, Jitter < 1 ns.

iii) Readout: Transmission Format = NRZ, 62.5 MHz, 50% Duty Cycle, RT < 2ns, FT < 2ns, Jitter < 2ns.

iv) Number of Fibre Optic Links Required:

- Readout = #Assemblies.
- Clock + Trigger = #Assemblies/6 or 8.

v) Receiver Specifications:

- Optical Wavelength = 820-850 nm.
- GaAs PIN.
- Minimum Sensitivity ~ 50-100 microWatts.
- Bandwidth ~ 150 MHz.

vi) Readout Transmitter Specifications:

- Optical Wavelength = 820-850 nm.
- GaAs LED.
- Minimum Fibre Coupled Power > 5 mW.
- Bandwidth ~ 62-124 MHz.

v) Fibre Specifications:

- Maximum Fibre Length = 100 m.
- Multimode.
- Outer Fibre Diameter = 500 microns.
- Inner Fibre Diameter = 200 microns.
- Bandwidth > 150 MHz @ 830 nm & 100 m.
- Interconnect Losses < 1 dB/connection.

vi) Noise & Error Rate: TBD

III. FABRICATION, ASSEMBLY AND TESTABILITY

III.A.1 FABRICATION

III.A.2 MCM

III.A.3 ANALOG

III.A.4 DIGITAL STORAGE, COMPRESSION AND CONTROL

III.A.5 OPTICAL READOUT, CLOCK AND TRIGGER

III.B.1 ASSEMBLY

- i) Deliver pre-tested IC chips, strip detector wafers (sawed) and mechanical supports.
- ii) Assemble wafers into 24/36 cm ladders using tape-bonding technology, test ladders.
- iii) Laminate wafers into double sided ladders, test ladders.
- iv) Fabricate MCM, test.
- v) Mount MCM to wafer ladder for finished ladder assembly.
- vi) Final assembly test.

III.C.1 TESTABILITY

TBD

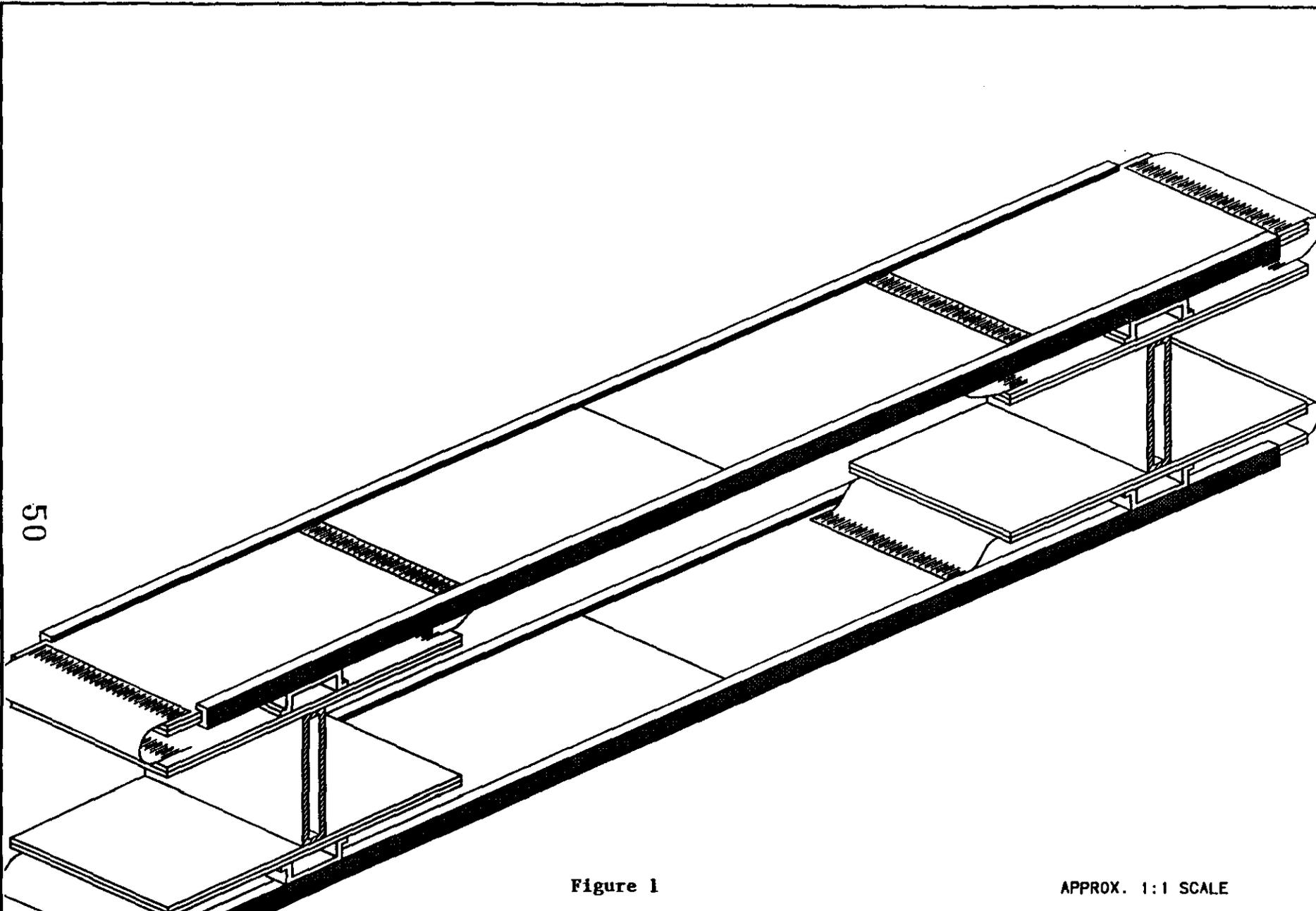


Figure 1

APPROX. 1:1 SCALE

GEM SILICON TRACKER. HDI 12cm LADDER ASSEMBLY.

B.C. / G.R. / M.J.K. MCDL, SST-11. GEM4.

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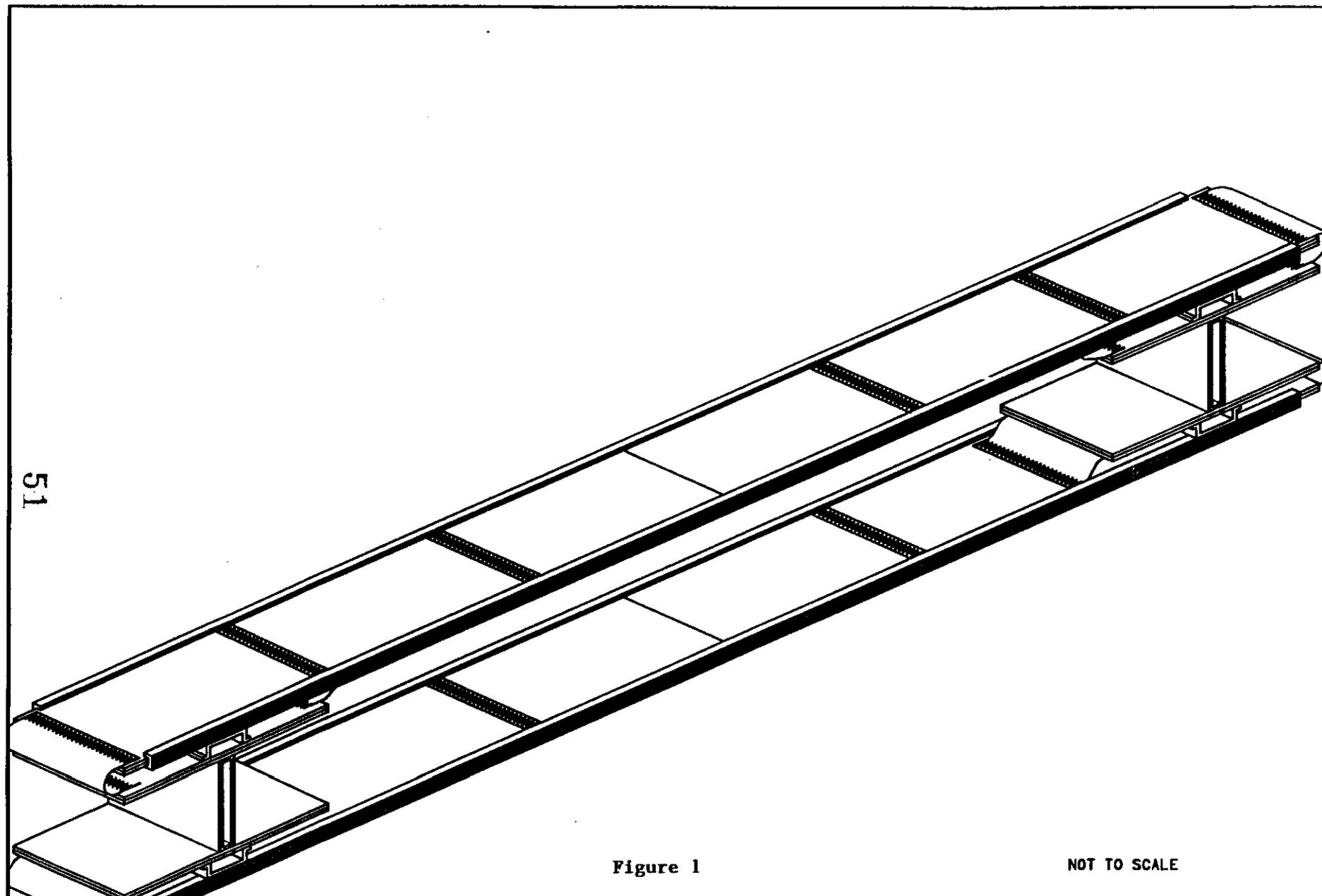


Figure 1

NOT TO SCALE

GEM SILICON TRACKER. HDI 18cm LADDER ASSEMBLY.

B.C. / G.R. / M.J.K. MCDL, SST-11. GEM5.

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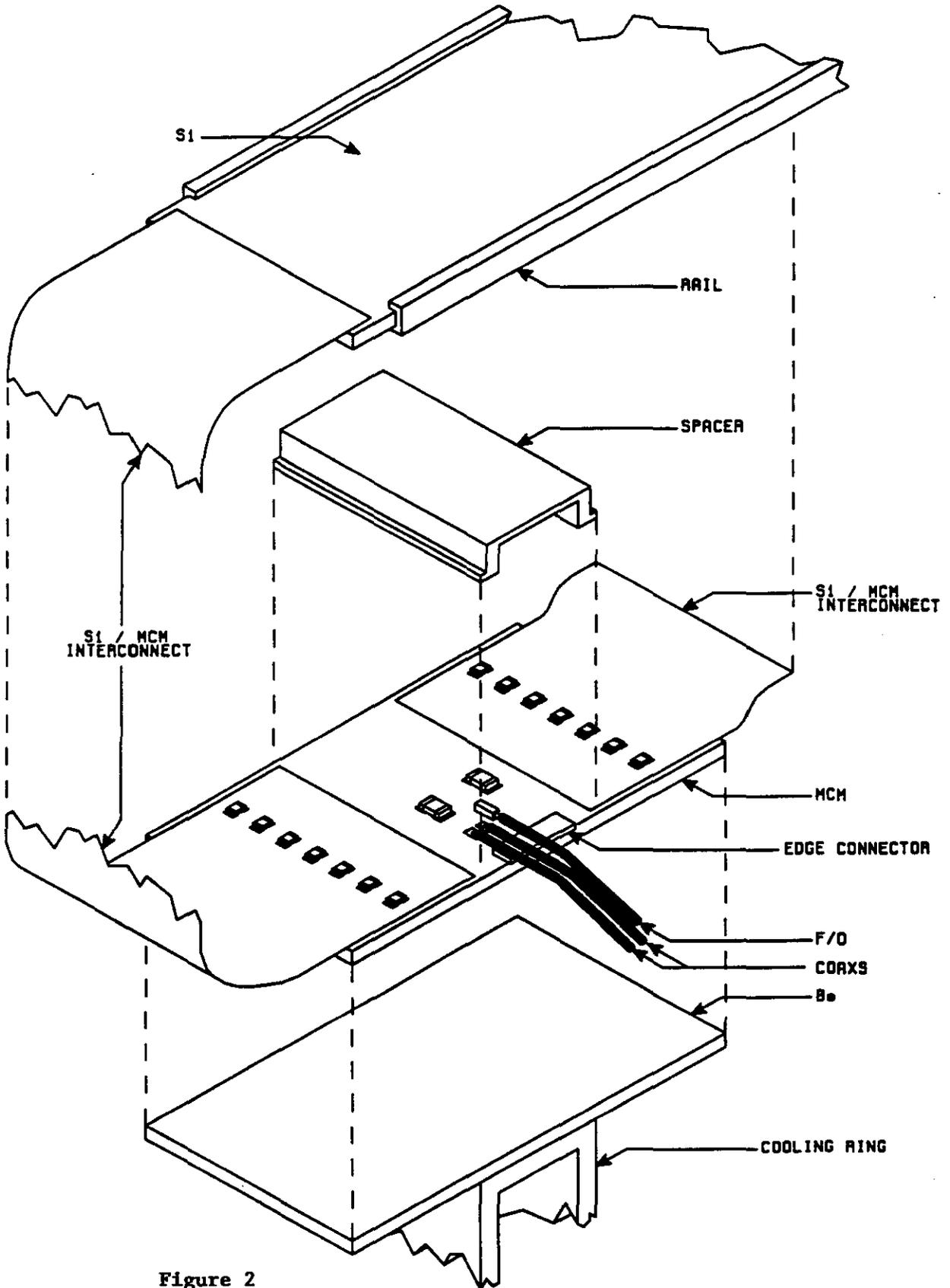


Figure 2

GEM SILICON TRACKER. DETECTOR ASSEMBLY W/SPACER

NOT TO SCALE.

B.C. / G.R. / M.J.K. 4/28/82. DRAWN: M.J.K. 11/18/82.

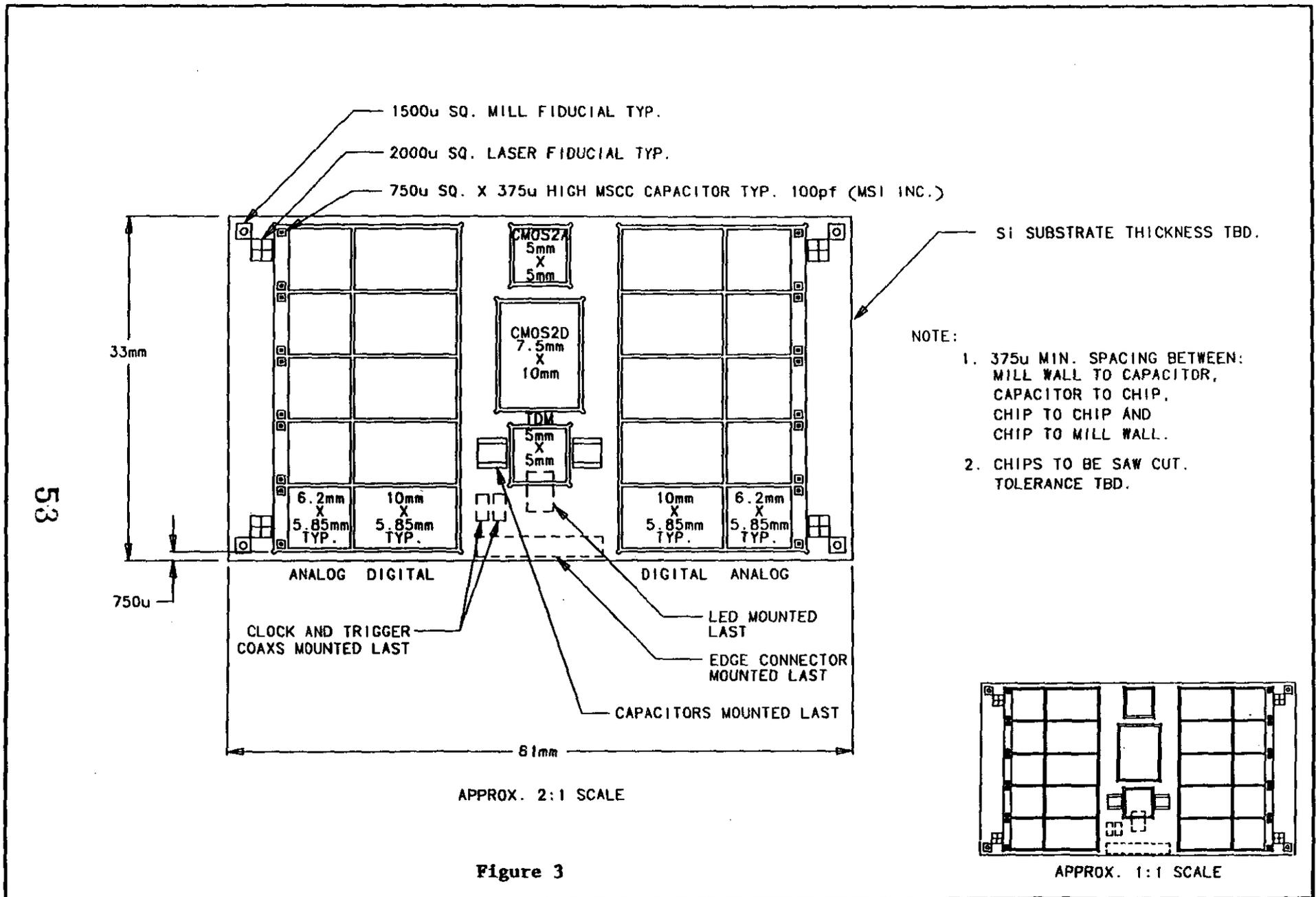


Figure 3

GEM SILICON TRACKER. PRELIMINARY DESIGN LAYOUT.

B.C. / G.R. / M.J.K. MCDL, SST-11. GEML3.

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MULTI-CHIP MODULE (MCM)

I. SUMMARY

The MCM, embedded in half of a 24/36 cm ladder assembly, is shown in Figure 1. A single MCM will provide the interface electronics for both the top 640 and bottom 640 strip detector channels. A blow-up of the MCM is illustrated in Figure 2.

An important role of the MCM is that it provides an efficient electro-mechanical interface between the electronic and mechanical systems. The strip-detector wafer is supported by the MCM through a thermally-insulating spacer bridge, while the MCM itself is mounted (glued) to the cooling ring (heat spreader is optional). Note that all mechanical contacts in this design straddle the thermal symmetry axes in order to minimize positional drifts due to thermal expansion and contractions. Power and the digital-slow-control-bus are connected to the cooling-ring cabling through an edge connector, while the clock and trigger are brought in through 100-ohm micro-cables from the 1:8 phase-locked optic to coax distribution modules situated on the cooling ring. Data from the MCM is transmitted through the fibre optic link that also runs along the space frame/cooling ring.

From the electronics systems perspective, a single MCM represents a self-contained modular unit. The modularity is due to the integration of the digital control circuits (CMOS-2) and input/output (slow control bus and optical driver) with the main analog and digital signal processing circuits. The advantages of modularity include improved electronic system integration, reduction in assembly labor and, of great importance, a significant increase in reliability and testability (through on-board automated testing). Because of the increased testability, the amount of time, labor and equipment required to test the system are significantly reduced.

Other expected advantages of using the single MCM over the double MCM structure, shown in Figures 1 and 2, include the following: a) improved thermal management, b) improved radiation length, due to a single MCM for both top and bottom strip detectors, c) a factor of two reduction in the number of fibre-optic channels, cable connectors, CMOS-2A,D controller chips and MCM's, d) improved ease of assembly and e) minimization of spurious radiation (noise) due to power supply and digital switching.

II. MCM SPECIFICATIONS

Refer to Figure 3 for the following specifications.

- i) Quantity:
- ii) Dimensions: $W = 33 \text{ mm}$, $L = 61 \text{ mm}$, $t = < 1 \text{ mm}$
- iii) IC dimensions ($W \times L \times t$) and quantity per MCM:

BP-1 (Analog BiPolar): 5.85 mm x 6.2 mm x 250 microns, 10

CMOS-1 (Digital CMOS): 5.85 mm x 10 mm x 250 microns, 10

CMOS-2D (Digital CMOS): 7.5 mm x 10 mm x 250 microns, 1

CMOS-2A (Analog CMOS): 5 mm x 5mm x 250 microns, 1

TDM (Digital BiPolar): 5 mm x 5mm x 250 microns, 1

iv) Buried resistors or capacitors

5 V Digital 1000 pico: W mm x L mm x Z mm, 10

1.5 V Analog 1000 pico: W mm x L mm x Z mm, 20

v) Surface mount device dimensions (W x L x h) and quantity per MCM:

LED (GaAs): 5 mm x 5mm x 2.5 mm, 1

Edge connector: 5 mm x 15 mm x 2.5 mm, 1

Surface mount capacitors:

5 V Digital 1 - 5 micro: W mm x L mm x Z mm, 1

1.5 V Analog 1 - 5 micro: W mm x L mm x Z mm, 2

1.5 V Analog XX micro: W mm x L mm x Z mm, 20

300 V Bias 0.1 micro: W mm x L mm x Z mm, 1 (cable mounted ?)

50 -100 Ohm Coax: D = 2.5 mm, 2

III. MCM CIRCUITRY

The MCM circuit is broken into a digital schematic (Figure 4) and an analog schematic (Figure 5). The digital schematic contains the 5 x 128 storage/compressor chips (CMOS-1), the digital control chip (CMOS-2A), the TDM driver chip and LED, and the cabling inputs. Figure 5 shows the 5 x 128 analog amplifier/waveshaper/discriminator and the analog CMOS-2A. The expanded IC pin-outs are shown in Figures 6A-E.

Slow control or house keeping is accomplished through the slow-control bus interface with the cabling. External personal computers (PC's) systematically monitor the state of the analog and digital circuits on the MCM through the 10-Bit bus + R/W/E lines and CMOS-2D,A.

IV. LAYOUT

The layout shown in Figures 3 and 6A-B utilize the General Electric/Texas Instruments High-Density-Interconnect (HDI) process. The process imbeds the IC chips into the substrate and builds the interconnect layers above the chips. This technology maximizes heat transfer

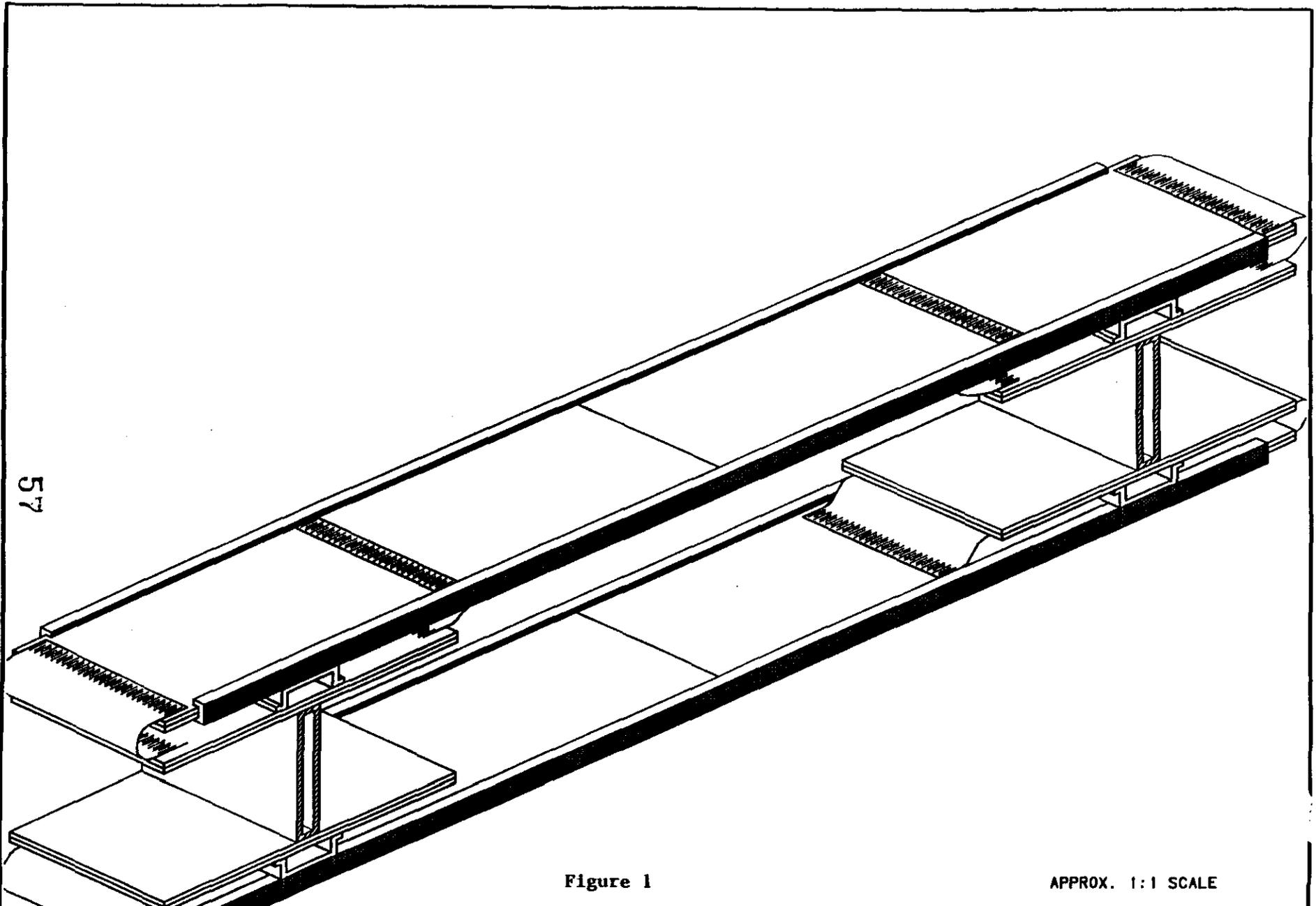
from the chip to the MCM and from the MCM to the cooling ring and minimizes spurious radiation due to digital switching and power supply coupling by maintaining quasi-TEM modes in its signal paths. Several of the important specifications are listed below:

- i) Substrate: Aluminum Nitride or Silicon.
- ii) Number of metalization layers: 5.
- iii) Line pitch: 100 microns.
- iv) Radiation tolerance: 40 MRad (Si), particle spectrum unknown.
- v) Minimum substrate thickness: unknown (Substrate thickness will probably determined by thermal conductance requirements).
- vi) Process yield: 6 sigma (3-5 defects per million).
- vii) Cost ? : TI claims a target cost of 1/3 of current industrial MCM costs.

V. ASSEMBLY

Current assembly plans include the following steps:

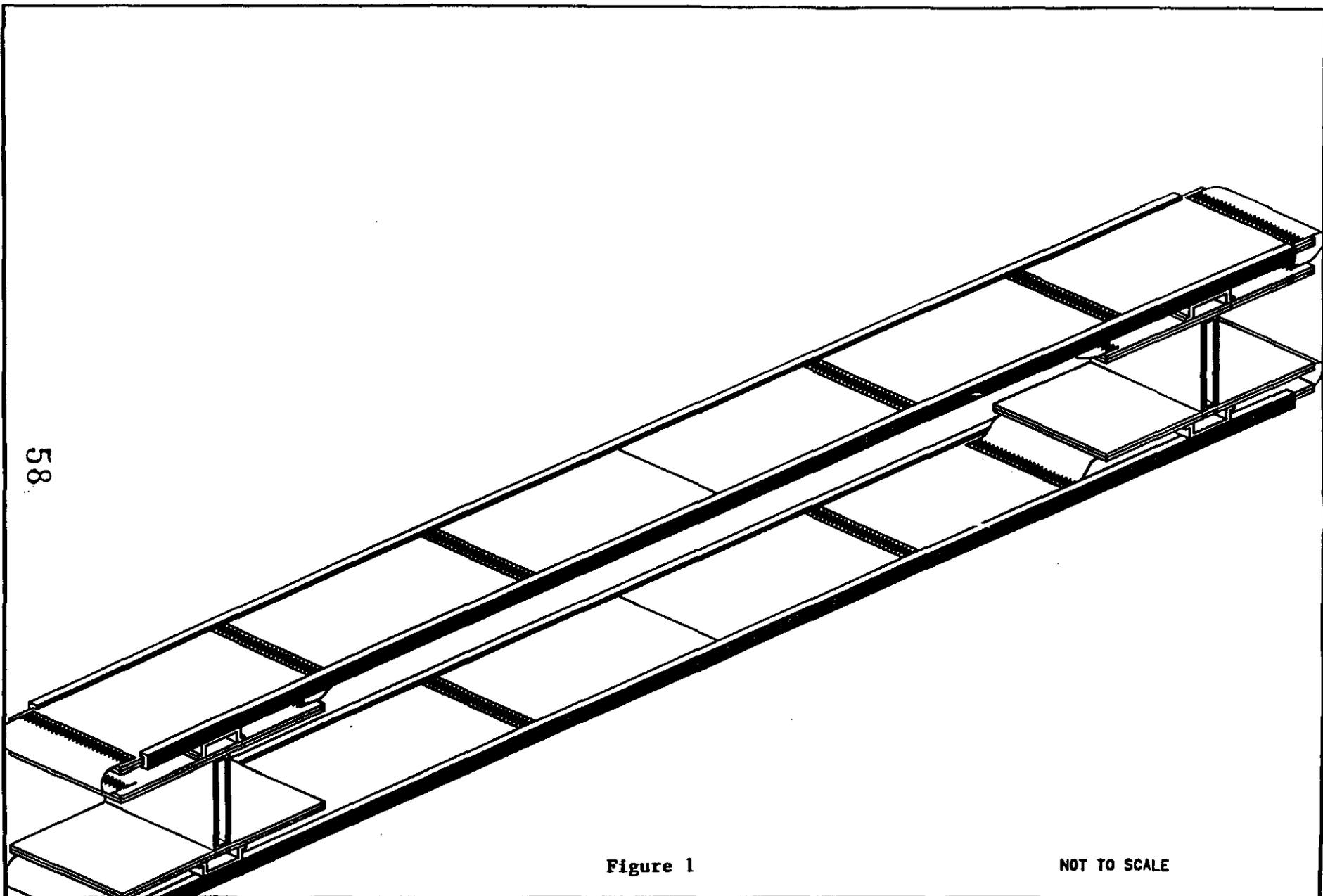
- i) Deliver pre-tested IC chips, strip detector wafers (sawed) and mechanical supports.
- ii) Assemble wafers into 24/36 cm ladders using tape-bonding technology, test ladders.
- iii) Laminate wafers into double sided ladders, test ladders.
- iv) Build MCM, test.
- v) Mount MCM to wafer ladder for finished ladder assembly.
- vi) Final assembly test.



GEM SILICON TRACKER. HDI 12cm LADDER ASSEMBLY.

B.C. / G.R. / M.J.K. MCDL, SST-11. GEM4.

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Figure 1

NOT TO SCALE

GEM SILICON TRACKER. HDI 18cm LADDER ASSEMBLY.

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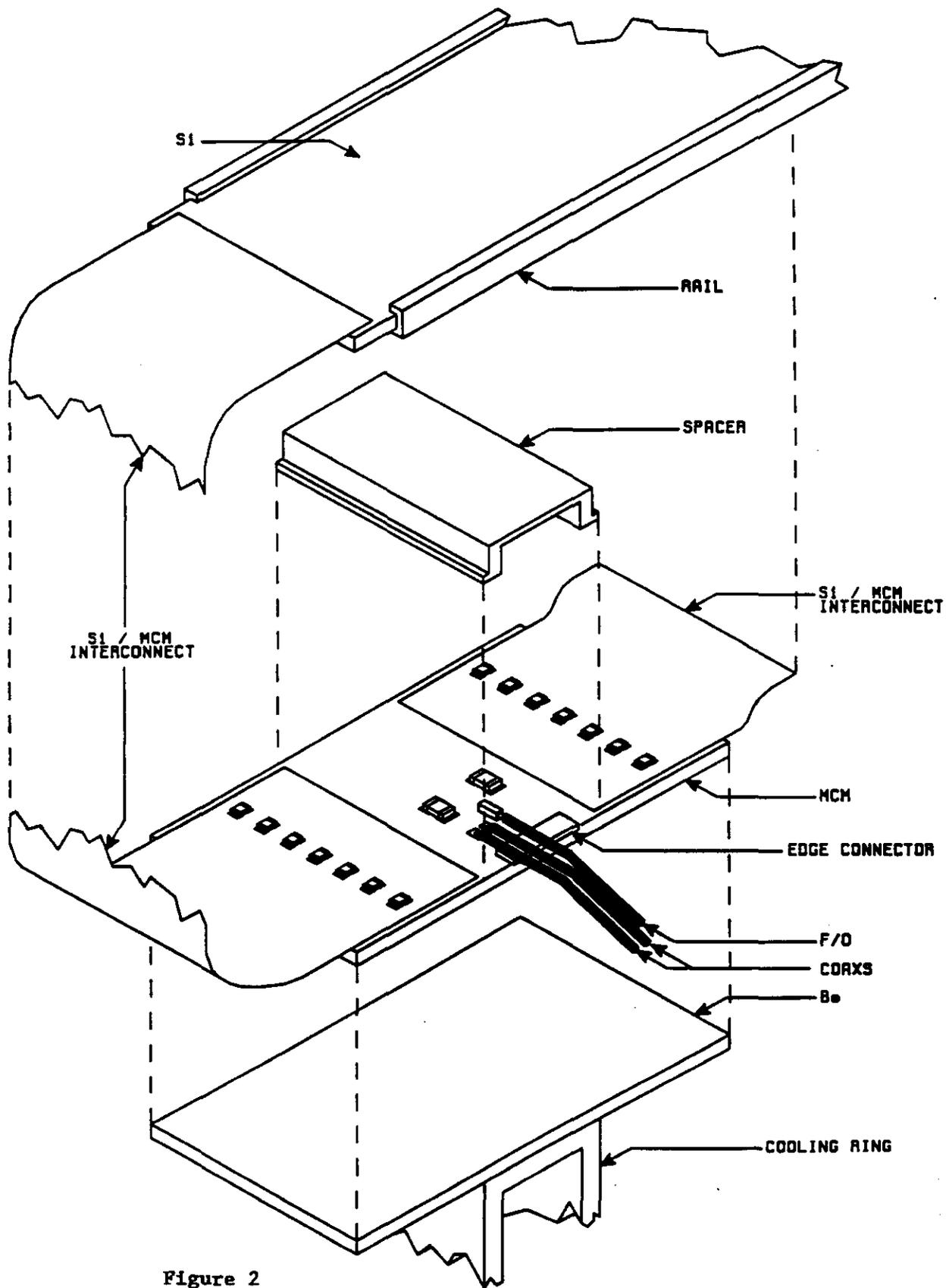


Figure 2

GEM SILICON TRACKER. DETECTOR ASSEMBLY W/SPACER

NOT TO SCALE.

B.C. / G.R. / M.J.K. 4/28/92. DRAWN: M.J.K. 11/18/92.

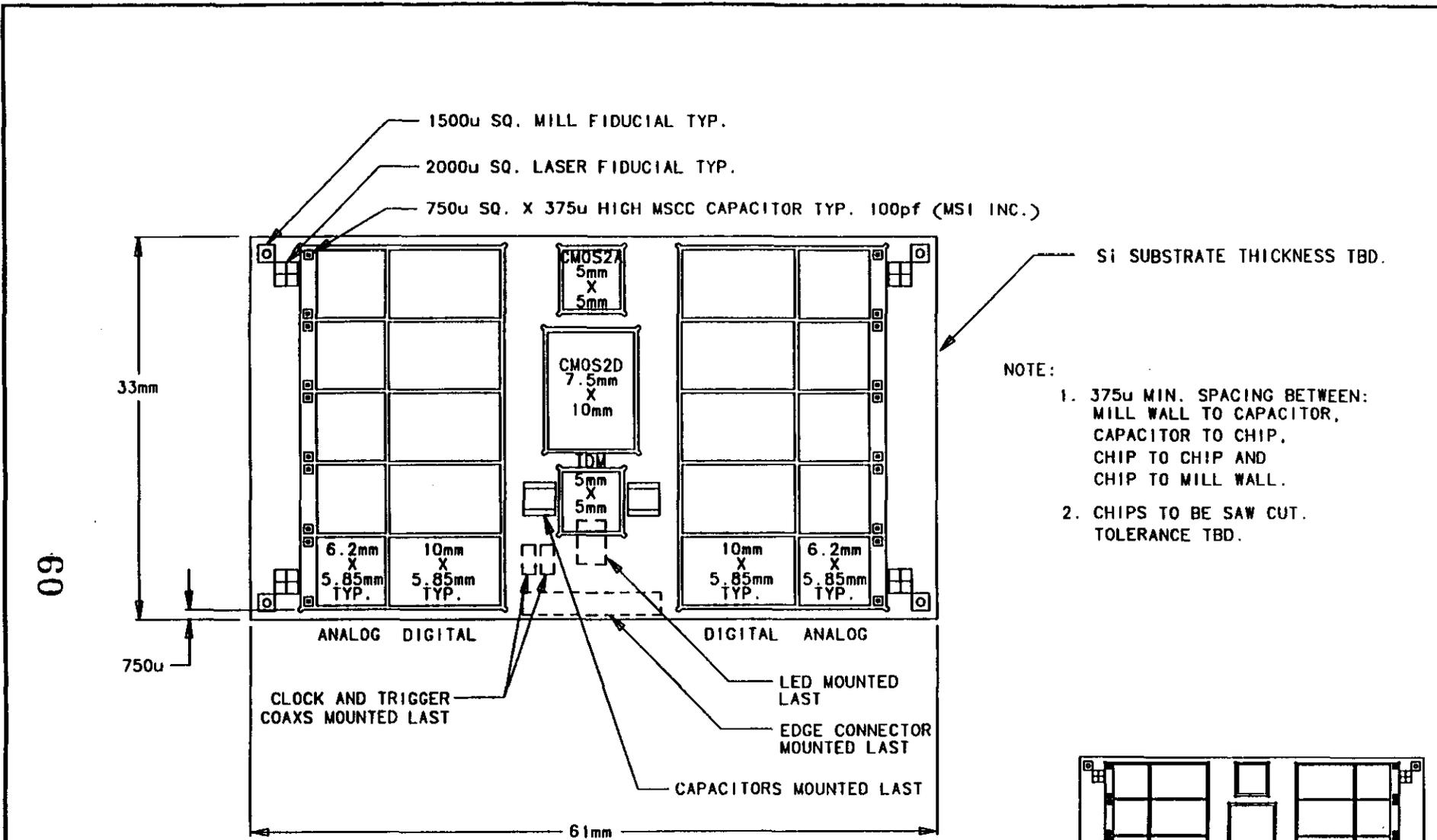


Figure 3

GEM SILICON TRACKER. PRELIMINARY DESIGN LAYOUT.

B.C. / G.R. / M.J.K. MCDL, SST-11. GEML3.

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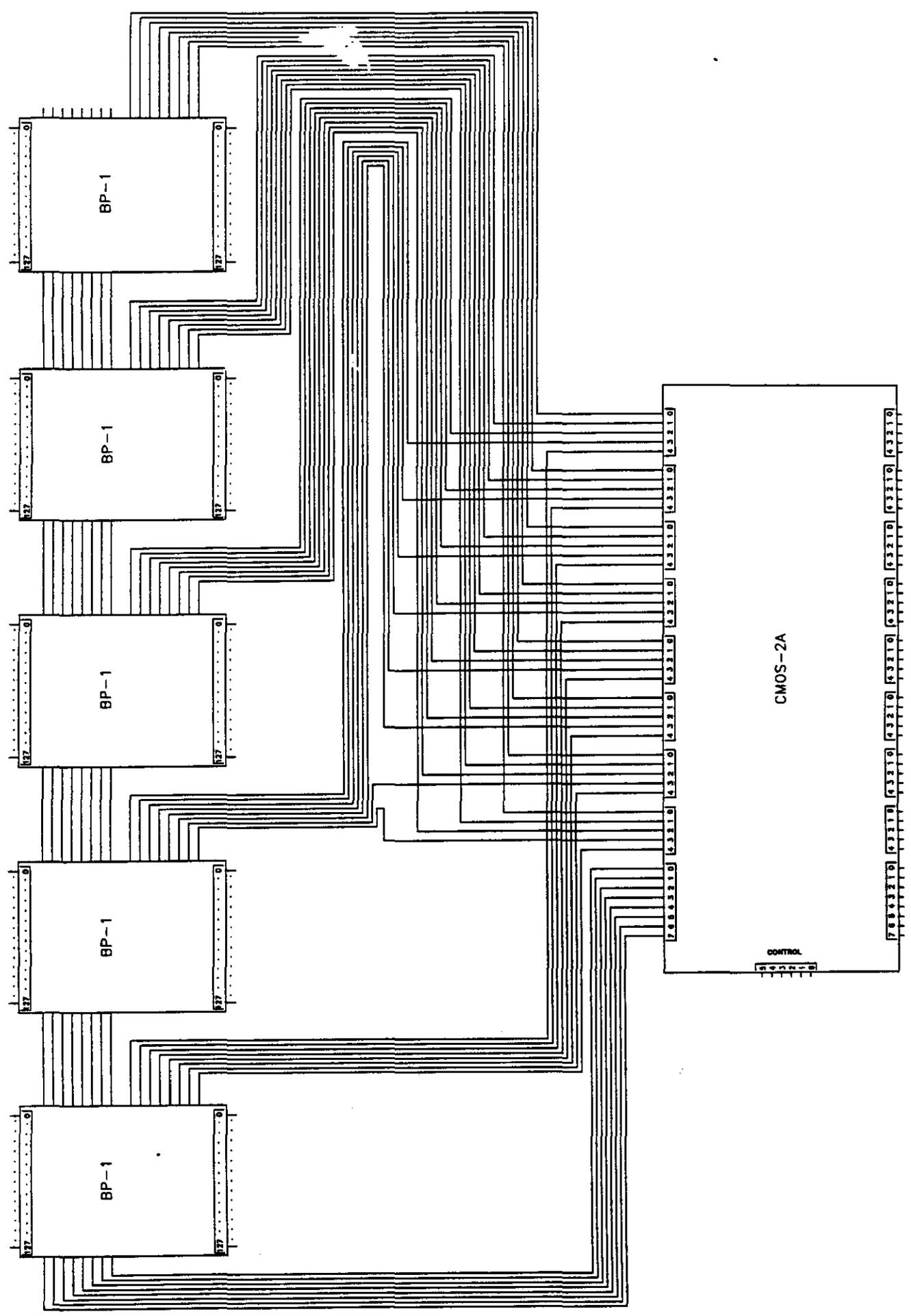


Figure 5

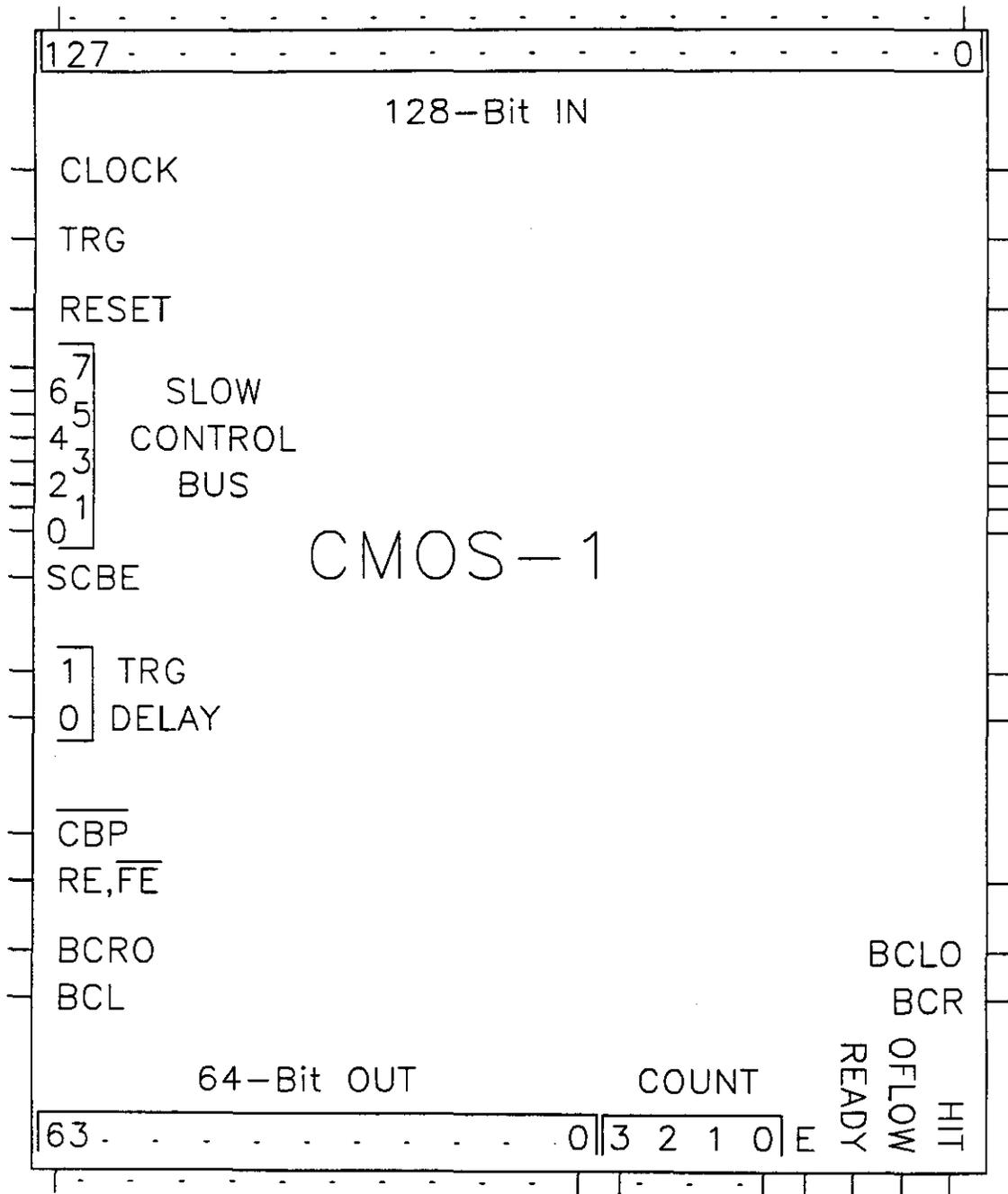
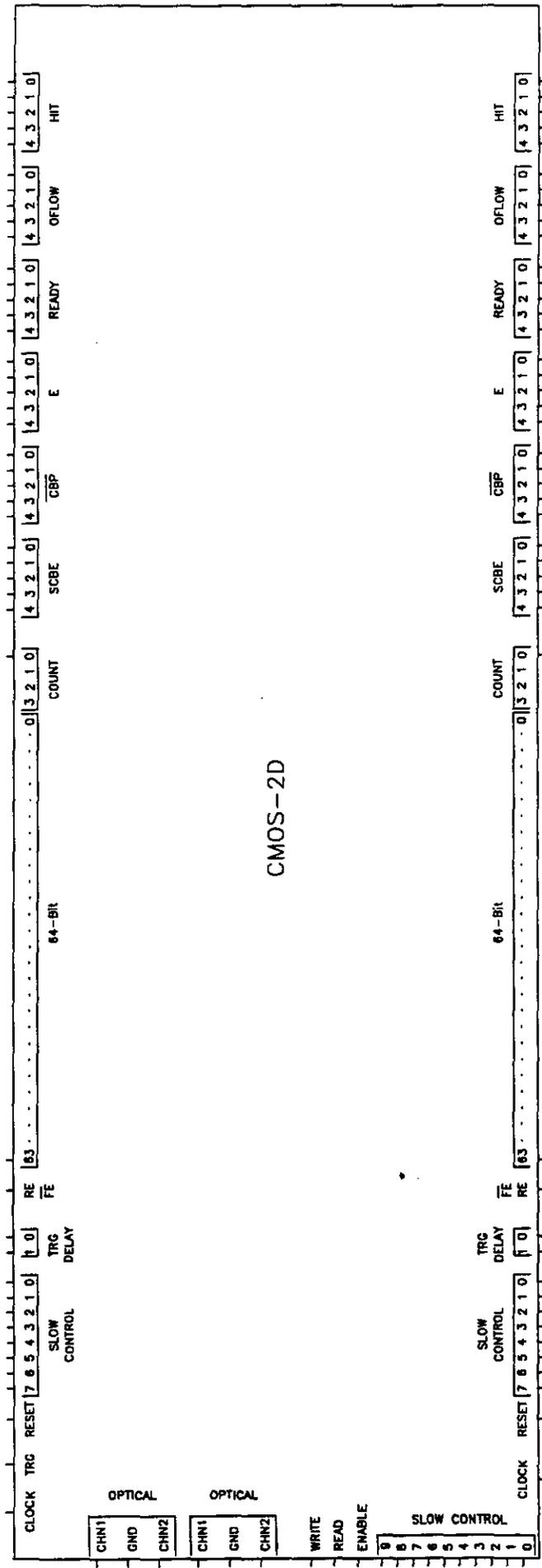


Figure 6A

ACOST

1/73



CMOS-2D

Figure 6B

36/1

11/02

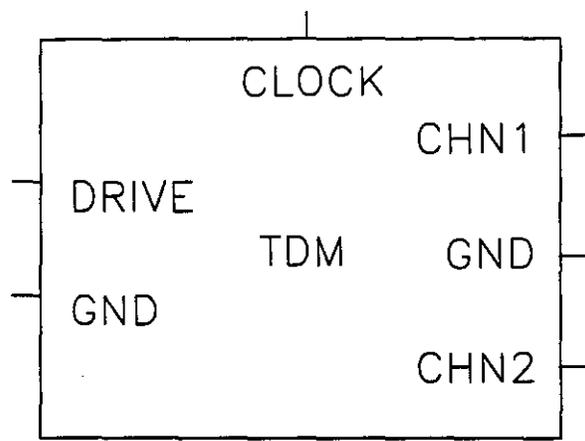


Figure 6C

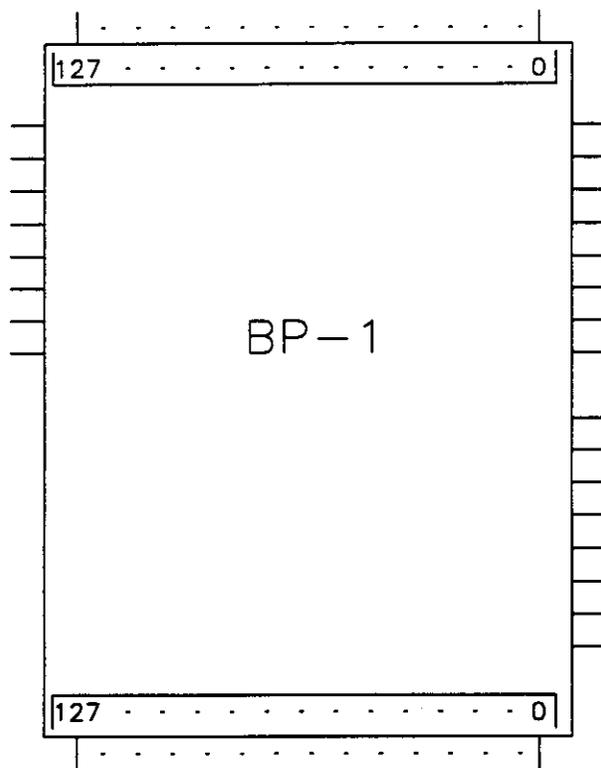


Figure 6D

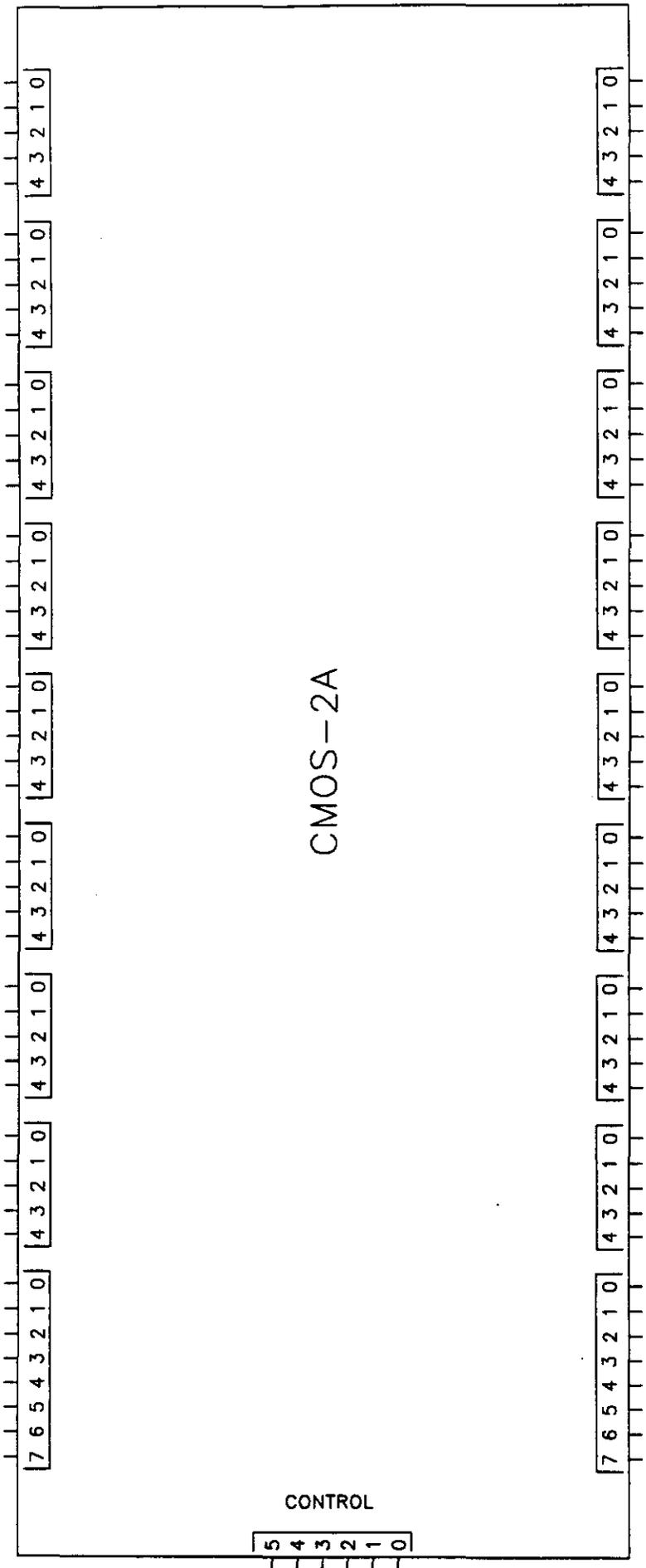


Figure 6E

DIGITAL STORAGE , COMPRESSION AND CONTROL

I. SUMMARY

The basic superconducting super collider (SSC) detector unit considered here is a silicon PIN-diode strip detector consisting of 640 strip/channels. A particle traversing a wafer will activate a cluster of strips. The amplified strip signals provide the information on the position of a particle(s) in one dimension. The data acquisitions task is to extract the locations of the activated strips and transmit this information to an external data-processing unit that can integrate the information of many strip detectors.

The proposed design consists of a latch, data storage and compressor. The data latch accepts a non-synchronized (relative to the system clock) analog pulse of random duration and generates a single, synchronized 16-ns digital pulse. Information is then stored for the duration of the trigger extraction cycle using data driven architecture. Triggered data is then passed on for data compression through both clustering and single hit extraction and then transmitted out. It is important to note that the SSC inner-detector strip occupancy is sparse and the trigger attenuation is high, allowing for both time and data compression. Based on the data flux, strip occupancy and trigger specifications stated below, the architecture will require a mean data bandwidth of < 20 Mbits/sec/1280 strips. A single, time-division-multiplexed (TDM), 62 Mbits/sec LED channel is provided.

Figure 1 shows the general chip architecture. There are 10 storage/compressor CMOS-1 chips (5 for each 640 strips), 1 controller CMOS-2D chip, 1 TDM BP-2 chip, and 1 62 Mbits/sec LED. Each CMOS-1 chip contains 128 channels, hence 5 chips are used for the "top" 640 strip and 5 chips for the "bottom" 640 strips. Both sets of chips use the same CMOS-2D chip and optical channel (31 Mbits/sec bandwidth per chip-set).

GENERAL SPECIFICATION

- 62.5 MHz clock.
- 5 MRads (Si) total dose over 10 years. (40% 1MeV Neutrons, 40% 1GeV Protons, 20% >1Mev Gamma)
- Single Event Upset (SEU) tolerant, Reset free.
- Number of assemblies (1/2 ladders): .
- Strip-detectors/assembly: 640/3.3 cm (pitch = 50 microns).
- Mean tracks/assembly/16 ns: 1 @ $10^{33}/18$ cm, 2 @ $10^{34}/18$ cm.
- Mean strips-hit/track/16 ns: 2 @ $10^{33}/18$ cm, 2 @ $10^{34}/18$ cm.
- Trigger rate (max ?): 100 KHz.

- Trigger delay: 256 X 16 ns (~ 4 micro-seconds).

CMOS, BiPolar, LED SPECIFICATIONS

- CMOS-1 (Latch, storage, compressor)
 - Quantity: 10 X number of assemblies.
 - Dimensions (W X L): 5.8 mm X 10 mm.
 - Number of channels/chip: 128 @ 45 micron pitch.
- CMOS-2D (Controller)
 - Quantity: 1 X number of assemblies.
 - Dimensions (W X L): 7.5 mm X 10 mm.
- TDM (Time-division-multiplexed, LED driver)
 - Quantity: 1 X number of assemblies.
 - Dimensions (W X L): 5mm X 5mm
- LED (GaAs)
 - Quantity: 1 X number of assemblies.
 - Dimensions (W X L): 5mm X 5mm

II. DATA LATCH

When a strip detector is hit by a particle, the resulting charge generated is collected, amplified and wave-shaped by the analog amplifier. Variations in the time and amplitude envelope of the charge waveform due to particle type, trajectory and position can produce a time jitter (time walk) at the output of the amplifier. Hence, the total time delay involved in a particle traversing a strip to when the analog stage produces a digital output is represented by a fixed delay plus a random component (time jitter). In addition, the same time and amplitude variations in the charge envelope produces a strong return-to-zero time-jitter (several beam crossings) at the output of the analog stage. Therefore, the requirements expected of the latch are the generation of a single, synchronous (relative to the system clock), pulse independent of the rise and fall time jitter of the analog stage.

Figure 2 shows a sequential latch circuit that will accomplish the above requirements. The latch is a two state circuit and will generate a single 16 ns pulse only when the clocked sequence contains a one - zero combination (rising edge) or zero - one combination (falling edge).

III DATA STORAGE

The storage algorithm makes use of the sparse nature of the data. The expected SSC inner-detector strip occupancy is very low (see above GENERAL SPECIFICATIONS), allowing for

the implementation of data driven storage^{1,2,3}. In data driven storage, only the hit channels initiate the data processing. This is as opposed to clock driven storage where channel data is stored at every clock cycle regardless of the state of the channel. In essence, a certain level of intrinsic storage compression is achieved when a data driven architecture is used with sparse data sets. In addition, since the relative processing activity in a good data driven storage architecture is directly proportional to the strip-detector channel occupancy, a significant reduction in data processing volume is expected (as compared to a clock driven shift register architecture). A reduction in the data processing volume leads to lower power dissipation and eases some of the problems involved in high speed integrated circuit (IC) chip design. Indeed, in the architecture presented major portions of the chip circuitry are dormant because only hit strips are processing and power is dissipated only during data shifts and pointer increments (discussed below).

III.A.1. CONCURRENT POINTER TRACKING DATA STORAGE

A brief description of the algorithm follows. Referring to Figure 3, when an analog rising or falling edge is detected and latched, the current count of COUNTER is copied into the register pointed to by WP (REG3 in this case). WP is then incrementing to the next register (REG4) for the next latched edge. Simultaneously, the count of COUNTER and the contents of the register pointed to by RP (REG1 in Figure 3) are continuously compared (note that the contents of REG1 and the counter always lag by 2^n , where n is the number of counter bits and $2^n \times 16$ ns is the trigger delay). When the contents are equal and a trigger is present, OUT=1 and RP is incremented to the next register (REG2). If the contents are equal and no trigger is present, OUT=0 and RP is still incremented to the next register.

Of primary importance is the constant updating of the read pointer so that prompt readout of the appropriate tagged-hit is initiated in the event of a matching trigger. The key to the success of the data driven storage technique is that the read pointer is guaranteed to point to the address of the only possible event candidate when the corresponding trigger is processed. This requires that all read pointers are concurrently updated by the counter and trigger relative to the pointers contents, and relative to the write pointer. Figure 4 illustrates the cyclic relations between the read pointer (RP) and the write pointer (WP). The absolute locations of the read and write pointers is irrelevant, only their relative positions are important. Note that the read pointer is always trying to "catch" up to the write pointer. It should be noted that the read pointer value can only be equal-to or less-than the write pointer and action on a read pointer is always delayed one cycle (clock) behind the write pointer action for a given position on the ring. In addition to the above mentioned restrictions, a read pointer location is current only until the COUNTER value equals the tag pointed to by the read pointer. To repeat, when this occurs, the read pointer is advanced to the next location (provided that it does not pass the write pointer). If no events have recently occurred and the write pointer has been idle, the circuit goes dormant until a hit arrives.

Other points worth mentioning include:

- i) Only the relative clock phasing between the system clock and any other counter (like COUNTER) is important (note that 250,000 - 500,000 counters will be distributed throughout the architecture). If a phased clock is used (in GEM this represents 256 counts \times 16 ns), the trigger is always timed to arrive 256 counts later (relative to an event) independent of the contents of COUNTER. This implies that the trigger can be sent down a single fibre as a pulse and system-clock resets are not required.

ii) Each single-bit circuit is a self-contained autonomous cell, that is errors tend to be confined to a single or few cells (each cell represents a single bit). The cells can also be made to be self-correcting in the event of a single-event-upset (SEU) of logic 'glitch'. This is possible due to the concurrent pointer technique combined with sparse data and the 100 KHz trigger rate (on average, COUNTER will cycle through all the 'garbage' and re-align RP and WP well before the next hit or trigger occurs).

iii) The trigger aperture can be adjusted.

iv) All logic is pipelined (there is no feedback).

v) The cell goes dormant and dissipates very little power when no hits are registered.

III.B.1. DATA STORAGE CIRCUIT

The circuit synthesis of the architect shown in Figure 3 is given in Figure 5. The circuit is a single-bit cell and consists of the latching circuit (shown in Figure 2), an 8 X N bit multi-port R/W static ram array (a CMOS ram cell is shown in Figure 6), the RP/WP shift-register stacks & control circuitry and the counter and the comparator. The depth N of the static-ram is determined by the occupancy rate, the required trigger delay (4 microseconds) and the trigger rate. A depth of N=8 has been selected for the preliminary design. The data storage circuit component of CMOS-1 is composed of 128 single-bit cells (see COUNTER sharing below).

The circuit input/output lines are:

i) IN: Analog input.

ii) SET: Part of the test circuitry. Digitally sets the cell to a logic 1 for test purposes.

iii) RE, NOT(FE): Selects analog rising or falling edge.

iv) RESET: Cell reset. Pointers are set to REG0, COUNTER = 0, LATCH = 0 and 8 X N RAM may or may not need resetting.

v) CLOCK: 62 MHz clock pulse.

vi) TRIGGER: Single line, variable aperture trigger.

vii) OUT: Cell output.

Several observations follow:

i) COUNTER can be shared by multiple single-bit cells to reduce component count. A single counter can service 8 to 16 cells. Note that not only is the counter expected to run non-synchronized with the master clock (as described above), but if the counter "skips" due to an SEU or circuit error, the counter/8-16 single-bit cell circuit will recover within at worst 256 counts (~ 4 microseconds). The odds of passing bad data is proportional to the number of single-bit cells per counter, the SEU and/or circuit error rate, the occupancy rate and the

trigger rate all which are extremely low.

ii) The WP and RP shift-register stacks are independently designed to reset to logic 0 when a logic 1 is shifted into the REG0 pointer. This provides a means of removing multiple pointers activated by SEU. In addition, if an SEU or circuit error erases the logic 1 pointer, the circuit in Figure 5 automatically generates a new pointer at REG0.

iii) Based on i and ii above and other criteria to be presented later, the circuit can be operated without the need for periodic global resets.

iv) TRIGGER is a pulse whose aperture is variable from a single beam-crossing up to 4 beam-crossings. The aperture is set by CMOS-2D, TRG DELAY (see MC), while the trigger delay is externally set. Hence, if vectors from the previous, current and next beam-crossings are to be sent up in a single vector, the trigger pulse is advanced by 1 beam-crossing and TRG DELAY is set to (1,0). The CMOS-1 trigger circuit is shown in Figure 7.

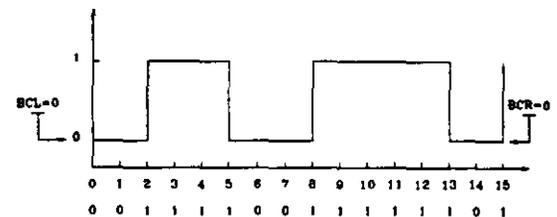
v) A write cycle to a register requires both the WP and a LATCH pulse to enable the counter to register write. The WP is always statically enabling (pointing to) the correct register but the LATCH pulse is what dynamically initiates the transfer. This data transfer technique minimizes power consumption.

IV DATA COMPRESSION

The trigger latches the 128-bit data vector out of the data storage and initiates the data compression cycle. Data compression is accomplished by transmitting both cluster and single hit information. The algorithm proceeds as follows: The uncompressed data retrieved from storage is edge-detected for either single hit or cluster edges. Then, the relative positional offsets of the edge boundaries are found. The resulting compressed data vector is then composed of the number of edges and the positional offsets of each edge (relative to the CMOS-1 boundary in this design).

IV.A.1. ALGORITHM

An illustration of the algorithm follows. A fictitious 16 bit (strip) detector with two boundary conditions $BCL=BCR=0$, two clusters and a single hit. The binary data vector is shown immediately below. As the data vector is "passed through" a shift-register/counter, the edge offsets and the number of edges are counted. The decimal encoding of the two clusters and single hit in terms of shift register clock, edge count and accumulated offset count reduce to the following:



16-Bit Detector With Two Clusters And A Single Hit.

<u>Clock</u>	<u># Edges</u>	<u>Offset</u>	<u>Single Hit (YES=1)</u>
0	0	0	NA
1	0	1	NA
2	1	2/	0
3	1	2/3	NA
4	1	2/4	NA
5	2	2/5/	0
6	2	2/5/6	NA
7	2	2/5/7	NA
8	3	2/5/8/	0
9	3	2/5/8/9	NA
10	3	2/5/8/10	NA
11	3	2/5/8/11	NA
12	3	2/5/8/12	NA
13	4	2/5/8/13/	0
14	4	2/5/8/13/14	NA
15	5	2/5/8/13/15/	1.

Note that the "/" denotes the edge boundary. Since the largest possible edge is 16 or less, the edges can be encoded with 4+1 bit words where the leading bit encodes a single-hit. The resulting binary representation of the encoded vector is:

Edges = 101

Offset = 00010_00101_01000_01101_11111.

Admittedly, using 23-bits to encode a 16-bit number is rather inefficient. A practical implementation would generate an overflow and transmit the original un-encoded vector.

The above compression algorithm is useful only for sparse single-hit/clustered data. The GEM data set is extremely sparse even at high luminosity (see specifications above) and hence, is suitable for edge compression. Figure 8 shows the compressor architecture for a 128-Bit chip. When a trigger is detected, the compressor is first reset, and then accepts the 128-Bit vector, stores one copy and passes another to the 130-Bit shift register (the 0 and 129 register contain BCL and BCR respectively). The vector is serially shifted synchronously with the OFFSET counter. When an edge is detected, the contents of the offset counter are transferred to the 8-Bit register pointed to by the edge counter. If the edge detected is a cluster, then MSB=0, however, if the edge is a single hit, then MSB=1. The process continues until the offset counter = 128, or until the edge counter detects an overflow (too many edges). If the edge counter overflows, the original vector is passed on.

IV.B.1. COMPRESSOR CIRCUIT

The compressor circuit realization of the architecture in Figure 8 is shown in Figure 9. Note that up to 16 edges (16 single-hit, or 8 clusters or any combination less than 16) can be accommodated before an overflow is generated. When greater than 16 edges (16 edges X 8-Bits = 128-Bits) are detected, the original vector is passed on for transmission

The input/output lines are:

- i) BCL: Boundary condition left. Defines left-most edge boundary.
- ii) BCR: Boundary conditions right. Defines right-most edge boundary.
- iii) RESET: Resets the compressor. A reset is performed before every compression cycle.
- iv) CLOCK: 62 MHz clock.
- v) ENABLE: Initiates compressor. After the reset is strobed and the 128-Bit vector is received, ENABLE is set high to start compression.
- vi) READY: When compression is successfully completed, READY = 1. When the 7-Bit offset counter reaches 127, READY = 1.
- vii) OVERFLOW: Indicates more than 16 edges were detected. When more than 16 edges are detected (edge counter overflow) , compression is suspended.

IV.C.1. COMPRESSOR EFFICIENCY

The overall compression efficiency for all 640 channels can be understood by referring back to Figure 1. The full 640 channel compression architecture is composed of the 5 X 128-Bit segments corresponding to the five CMOS-1 chips and half of the CMOS-2D controller (the other half handles the opposing 640 channels). The data is passed from CMOS-1 to CMOS-2D through a common 64-Bit + 4-Bit bus plus the independent lines READY, ENABLE, HIT and OVERFLOW. A brief description follows :

- i) R (READY): Flags the CMOS-2D controller when a given segment compression is complete. The flag originates from the corresponding CMOS-1 chip.
- ii) E (ENABLE): After compression READY flags are received, the CMOS-2D controller sequentially enables the 5 CMOS-1 chips.
- iii) H (HIT): If the corresponding CMOS-1 chip registers a hit (edges are detected) then the CMOS-2D controller is flagged by HIT =1 for sequential enabling. If no edges are detected (HIT = 0) then that particular segment (CMOS-1 chip) is skipped. Note that on average, only one or two of the five 128-Bit segments are hit.
- iv) O (OVERFLOW): If more than 16 edges are detected in a segment, then that particular CMOS-1 chip generates an OVERFLOW =1 flag for the controller. This signals the controller that a 128-Bit uncompressed vector is to be sent.
- v) BUS: The 64-Bit edge + 4-Bit edge count bus.

When a CMOS-1 chip is enabled, the edge count + first 8 edges (4 + 64-Bits) are placed on the bus and transferred to CMOS-2D. If more than 8 edges are compressed or an OVERFLOW flag is present, the remaining 64-Bits are transferred.

Note: A detailed layout schematic is given in the MC section.

The combined 5 X CMOS-1 and CMOS-2D architecture produces the following transmittable vector:

[01234][01234][XXXX...][XXXX...][XXXX...][XXXX...][XXXX...]

or,

[HITS][OVERFLOW][EDGES₀ ...][EDGES₁ ...][EDGES₂ ...][EDGES₃ ...][EDGES₄ ...].

where 0,1,2,3,4 represent the five 128-Bit segments of the 5 X CMOS-1 chips.

The header is composed of ten bits. The first five contain hit information (hit segments), while the remaining five contain overflow information. The remaining data stream consists of segment data. If a segment contains hits, the first four bits sent represents the number of edges, followed by the bit stream of #edges X 8-Bits. The compressed vector bit count of the transmittable vector is given by:

$$n = 10 + \sum_i [(4U(S_i, C_i) + 8(S_i + 2C_i)) \text{ IF } > 132, \text{ THEN } 128]$$

where i is the segment index (0,1,2,3,4), and the number single hits and clusters are given by S_i and C_i , respectively. Note that if the number of single hits and clusters exceeds 132-Bits, then only 128-Bits are transmitted (the 4-Bit edge count is not required and is striped). Several bit counts for various combinations follow.

S	C	i	n
0	0	0	10
1	0	1	22
0	1	1	30
1	1	1	38
2	0	1	30
2	0	2	34
0	2	2	50
1	1	2	42
2	2	2	66
>16	>8	1	138
>16	>8	5	650
16 or 8	8	5	670

The minimum required bandwidth is then given by n times the maximum mean trigger rate (this does not include overhead). Based on the specifications given earlier, conservative bandwidth requirements (including overhead and noise estimates) are:

7.5 - 10 Mbits/sec for beam luminosity = 10^{33}
 15 - 20 Mbits/sec for beam luminosity = 10^{34}

Referring to Figure 1, the optical channel is a 62 Mbits/sec LED/fibre-optic link. The "top" and

"bottom" 640-channels are time-division-multiplexed into 31 MBits/sec channels through CMOS-2D. Hence, the optical channel is adequate with sufficient bandwidth for excessive noise and increased trigger rate transients.

An interesting example is the encoding of all 640 channels. The resulting transmission vector is given by the following unique encoding

[10001][00000][0001 00000000][0001 01111111].

V CONTROLLER

The controller chip (CMOS-2D) handles both the top and bottom 640 data channels as described above. In addition, all test and register settings (for example, rising or falling edge latching, trigger aperture etc) are programmed through the slow control bus. The architecture of the controller has been constrained by the system requirements.

V.A.1. DATA CONTROL ARCHITECT

TBD

V.B.1. SLOW CONTROL ARCHITECT

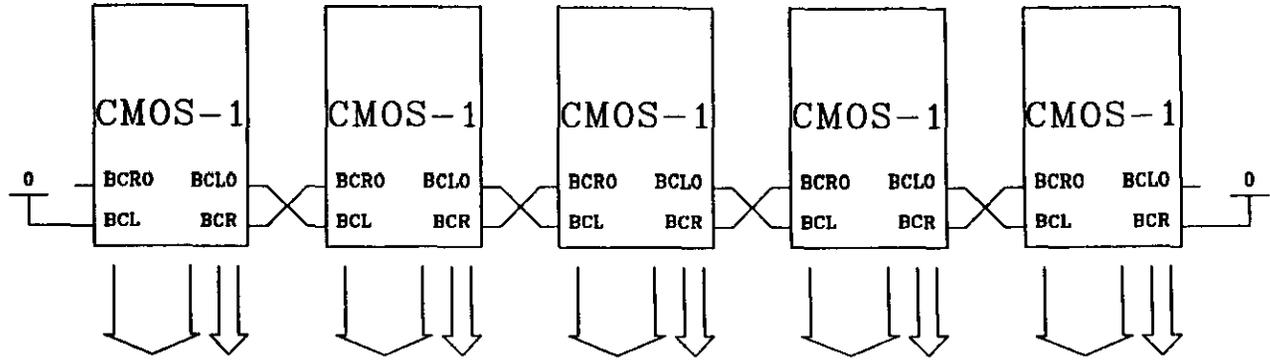
TBD

REFERENCE

1. V. Cook, P. M. Mockett, "A Precision Vertex Chamber For EMPACT," Symposium on Detector R&D for the SSC, Fort Worth, Texas, Oct 15-18, pp. 136-138.
2. O. Barkan, E. L. Atlas, W. L. Marking, S. Worley, G. Y. Yacoub, G. Kramer, J. F. Arens, J. G. Jernigan, S. L. Shapiro, D. Nygren, H. Spieler, M. Wright, "Development of a Customized SSC Pixel Detector Readout for Vertex Tracking," Symposium on Detector R&D for the SSC, Fort Worth, Texas, Oct. 15-18, 1990, pp. 142-144.
3. R&D Report on Double-Sided Silicon Detectors and Associated Electronics, Sept. 1990, 62-78.

640-CHANNEL ANALOG IN

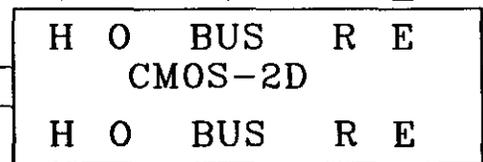
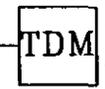
"TOP"



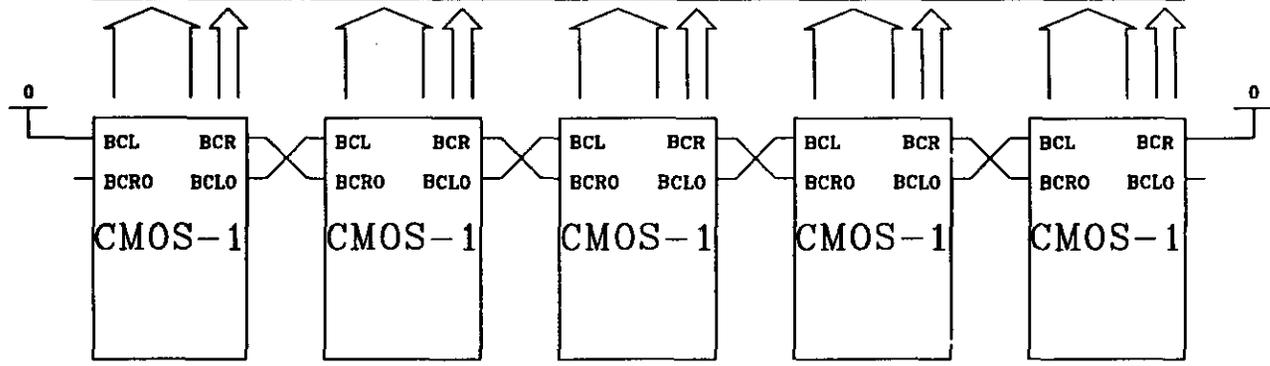
TRIGGER →

F/O OUT ←

CLOCK →



"BOTTOM"



640-CHANNEL ANALOG IN

78

Figure 1

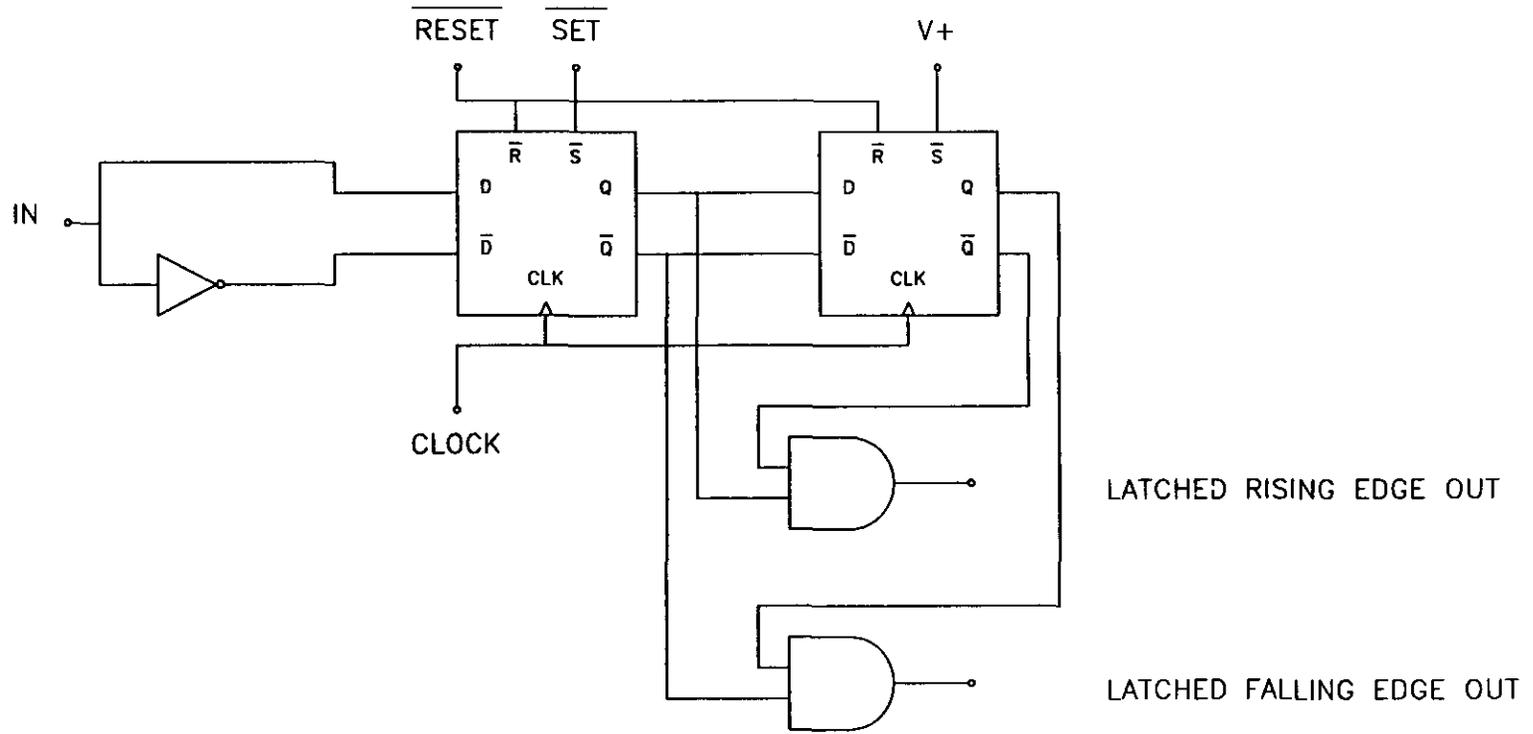


Figure 2

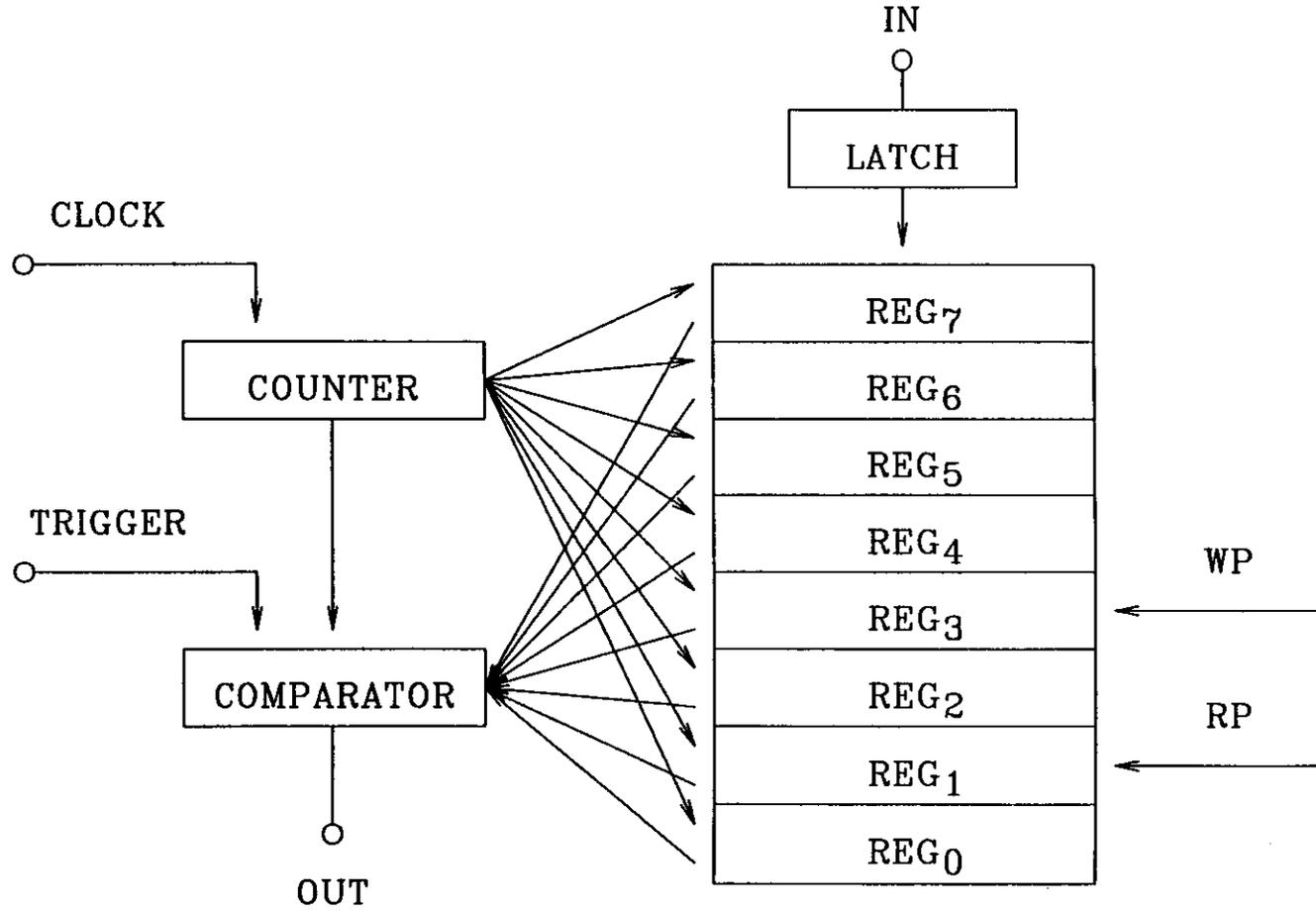
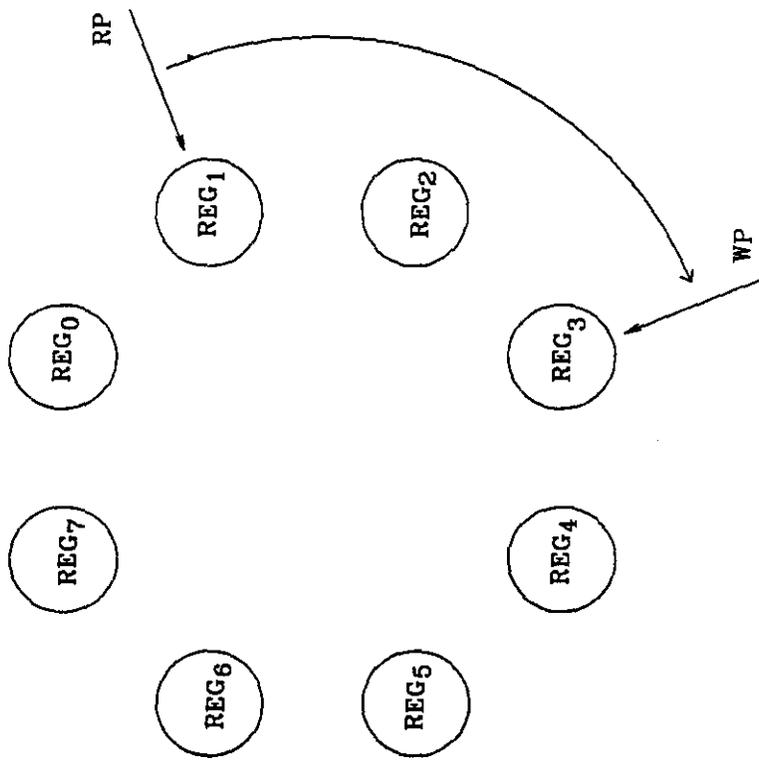


Figure 3



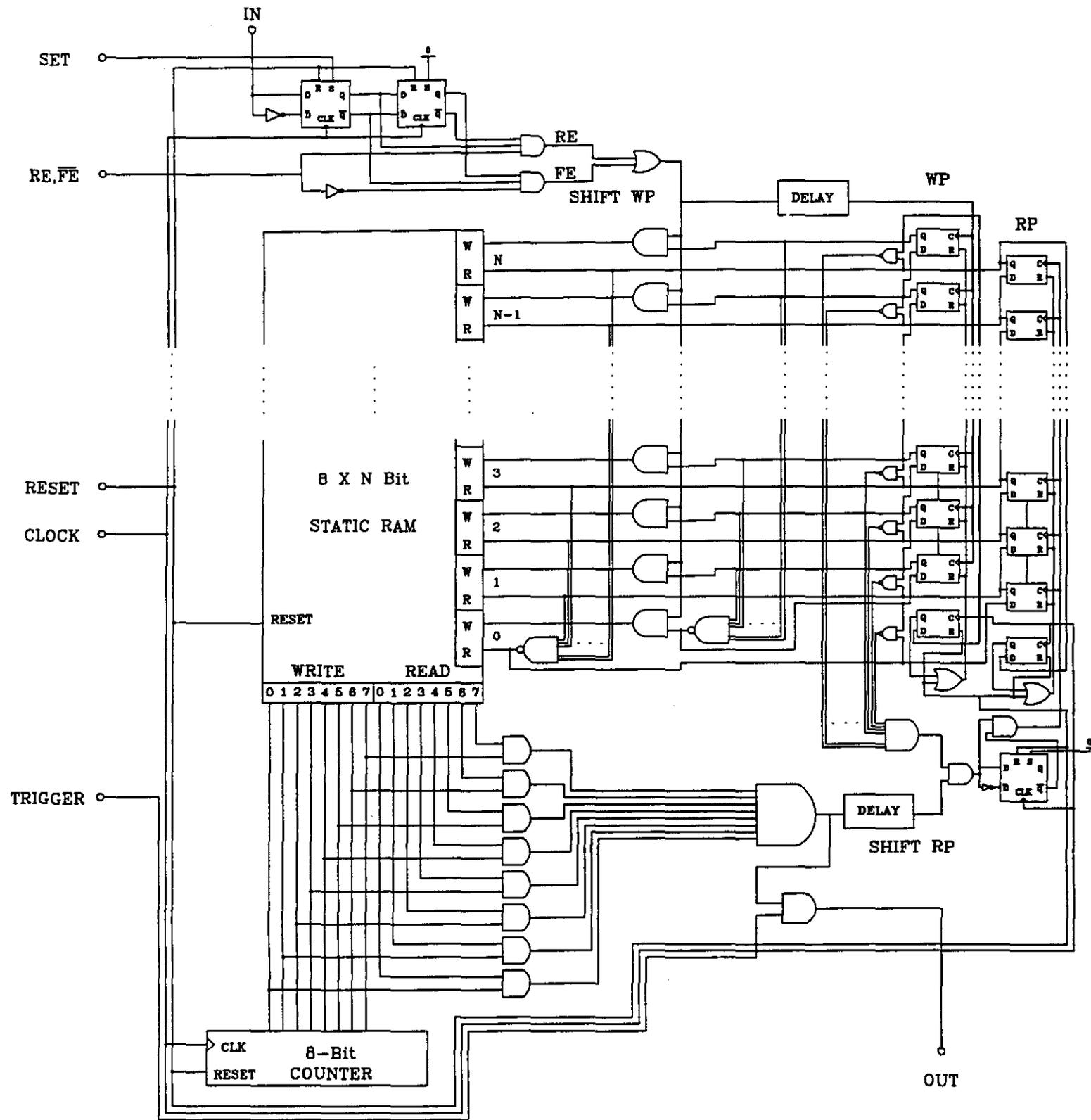
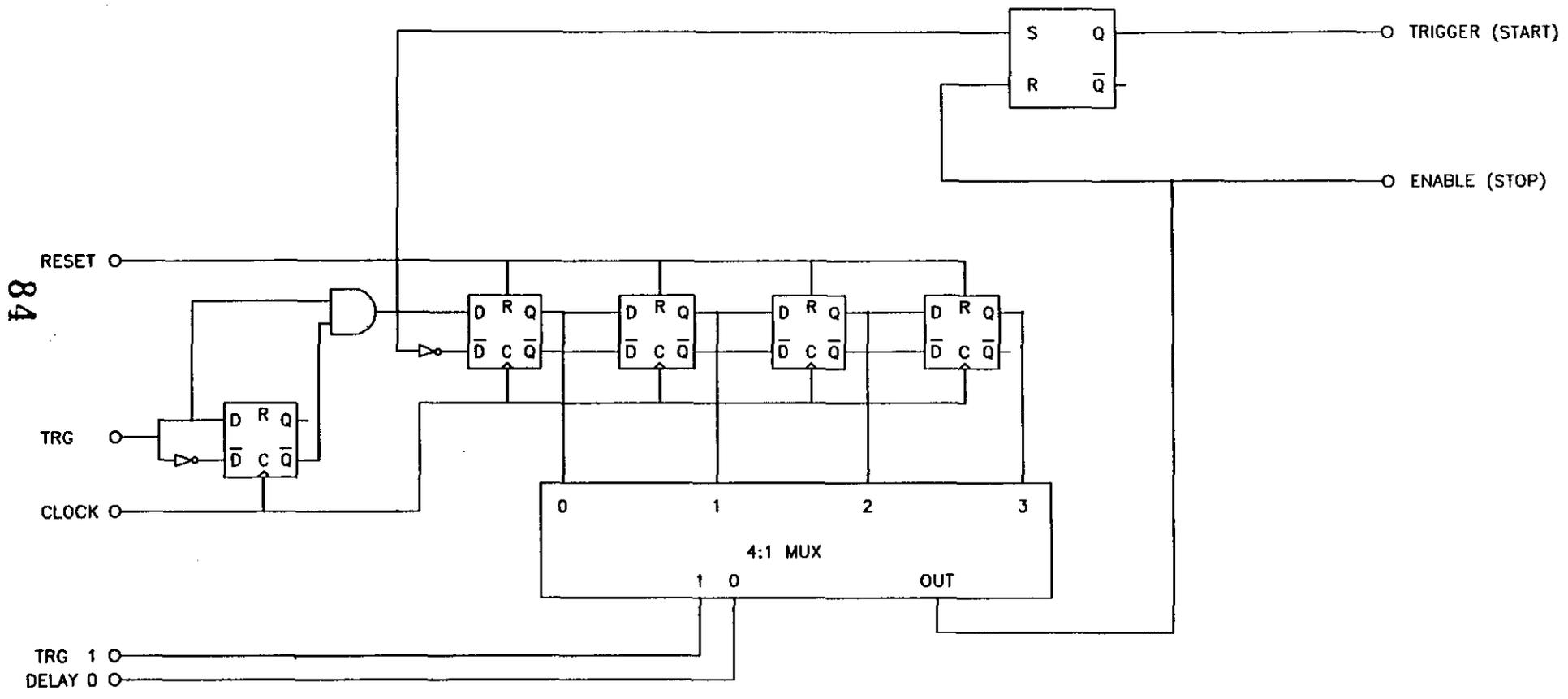


Figure 5



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Figure 7

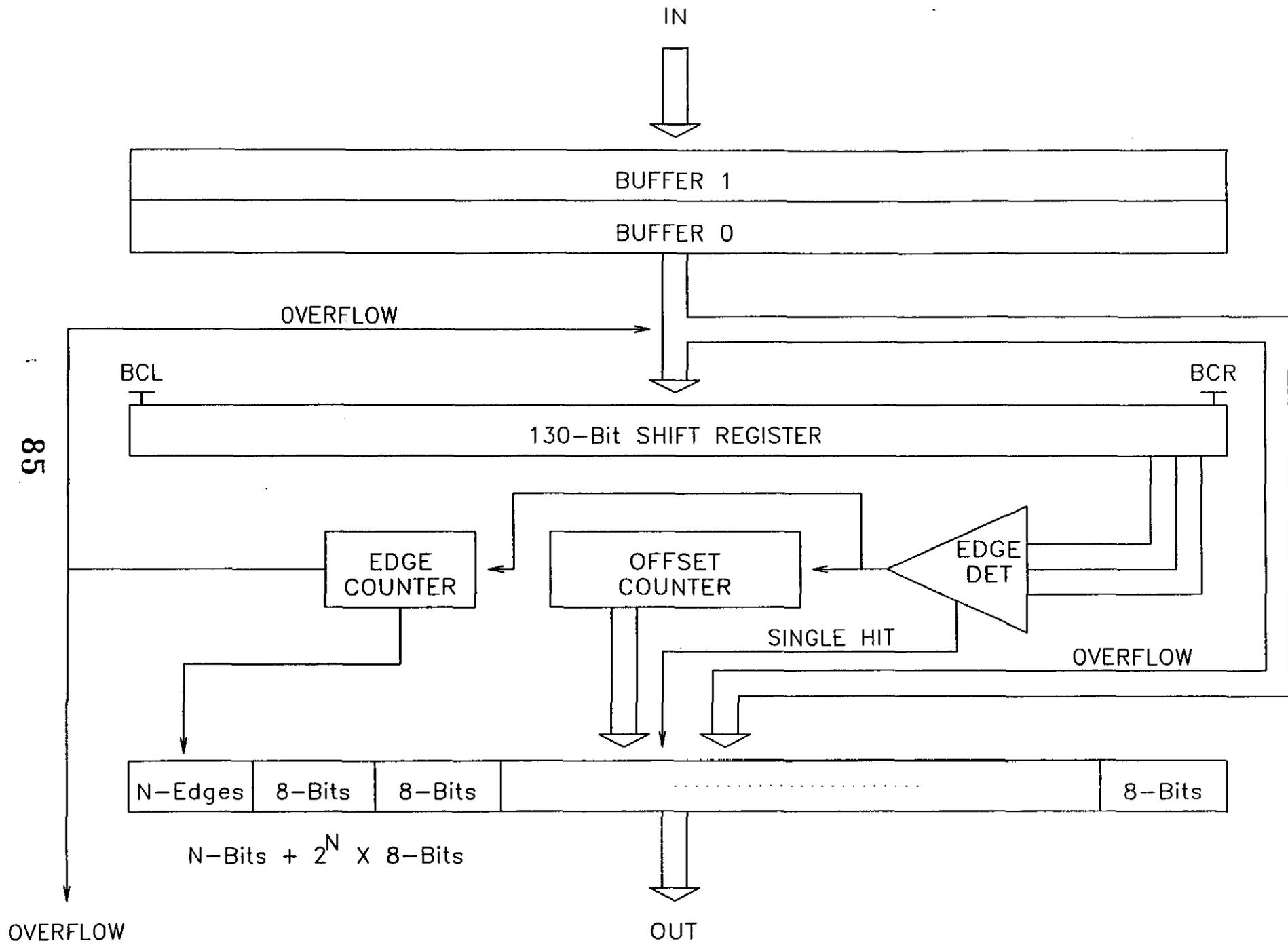


Figure 8

Model

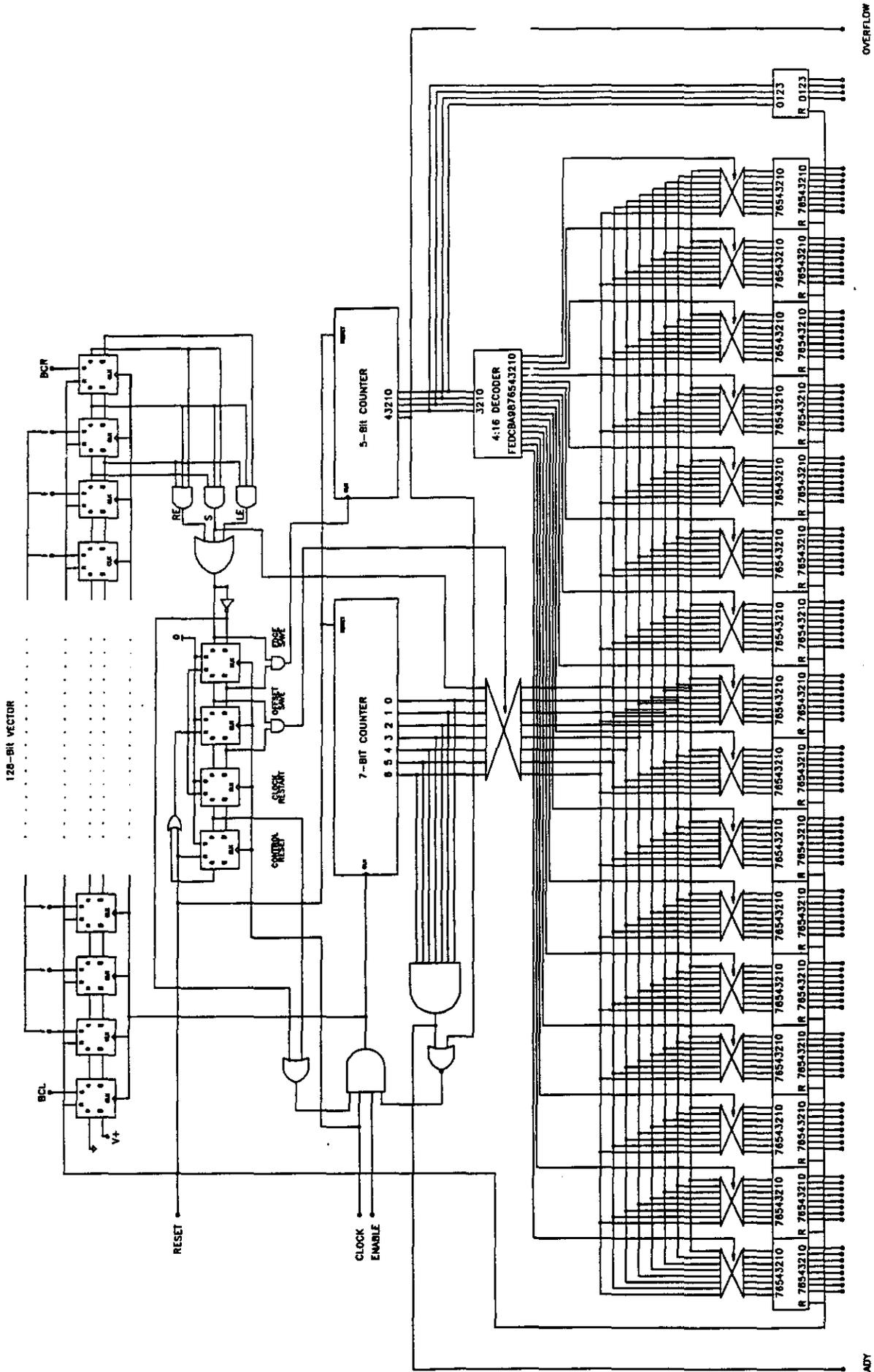


Figure 9

OPTICAL READOUT, CLOCK, TRIGGER

1. SUMMARY

Figure 1 shows the general electronics assembly architecture. The high-bandwidth items of interest to this section are the fibre-optic readout, clock distribution and trigger distribution. The optical readout is the MCM's dedicated data link that transmits hit information. The clock and trigger are brought onto the MCM through microcoax from a central optical receiver. Currently, six to eight assemblies are serviced for every clock/trigger optical receiver with the clock and trigger sharing the same optical link.

SPECIFICATION SUMMARY

- Clock: 62.5 MHz, 50% Duty Cycle, RT = 1 ns, FT = 1 ns, Jitter < 0.5 ns.
- Trigger: 8 ns Pulse, 16 ns Period, RT = 1 ns, FT = 1 ns, Jitter < 1 ns.
- Readout: Transmission Format = NRZ, 62.5 MHz, 50% Duty Cycle, RT < 2 ns, FT < 2 ns, Jitter < 2 ns.
- Total dose: 5 MRads (Si) total dose over 10 years. (40% 1 MeV Neutrons, 40% 1 GeV Protons, 20% >1 MeV Gamma)
- Single Event Upset (SEU) tolerant.
- Number of Assemblies (Strip detector + MCM = 1/2 ladders): ~ 1250.
- Number of Fibre Optic Links Required.
 - Readout = #Assemblies.
 - Clock + Trigger = #Assemblies/6 or 8.
- Receiver Specifications
 - Optical Wavelength = 820-850 nm.
 - GaAs PIN.
 - Minimum Sensitivity ~ 50-100 microWatts.
 - Bandwidth ~ 150 MHz.
- Readout Transmitter Specifications
 - Optical Wavelength = 820-850 nm.
 - GaAs LED.
 - Minimum Fibre Coupled Power > 5 mW
 - Bandwidth ~ 62-124 MHz

- Fibre Specifications

- Maximum Fibre Length = 100 m.
- Multimode.
- Outer Fibre Diameter = 500 microns.
- Inner Fibre Diameter = 200 microns.
- Bandwidth > 150 MHz @ 830 nm & 100 m.
- Interconnect Losses < 1 dB/connection.

- Noise & Error Rate: TBD

II. READOUT

A detailed block diagram of the readout optical link is shown in Figure 2. The figure illustrates many of the interface and electronic blocks design requirements. The discussion in this section primarily focuses on the design issues up to the detector/amp assembly (primarily in terms of optical compatibility and noise/error rates). An 850 nm optical link is shown in Figure 3. The design calls for the use of a large numerical aperture (NA) fibre (ID = 200 microns), a surface mount LED and a TDM driver.

i) A large numerical aperture fibre (ID = 200 microns) allows for lower-loss insertion (more light is couple from the diffused LED source into the fibre) and cheaper fibre connections (cleave & weld, bulk connector, etc.) for both matched and unmatched fibers (see Figure 4 from Ensign-Bickford), then do lower aperture fibers (ID < = 50-100 microns). The larger fibre size (OD = 500 microns) also provides easier handling characteristics then do smaller fibers. It is important to note that a great deal of the optical-link costs are found in the assembly phase (primarily in the fibre interconnects). In addition, inexpensive bulk-head connectors can be manufactured by drilling 500 micron holes into matched lucite blocks. The blocks are bolted together to form the evanescent field coupled connections (losses from fibre positional mismatch and coupling is minimized due to the large numerical aperture of the fibre).

ii) An LED is a diffused, non-coherent source (lambertian) and optical coupling into a fibre is optimized if a) the fibre has a high numerical aperture and b) a lens on the LED focuses a larger amount of power into the fibre. A surface mount LED (important for inexpensive MCM mounting) is shown in Figure 5. The surface mount LED is under development at Honeywell and can be mounted with a lens. Note that the LED needs to be rotated by 90 degrees for flat mounting (the SDC is currently pursuing this option with Honywell). If a lens cannot be inexpensively mounted, sufficient power can be coupled into a 200 micron (ID) for satisfactory performance.

iii) The Time-Division-Multiplexed (TDM) chip not only provides the multiplexing between the two CMOS-2D channels but also provides the appropriate buffering. A bipolar TDM multiplexed is shown in Figure 6. The circuit is fairly common and an appropriate off-the-shelf part should be available. Note that driving a device with high-current requirements at 31 MHz (let alone 62 MHz) with straight CMOS circuitry without bipolar buffering is very difficult. If the incoming clock (see below) needs buffering, an additional buffer can be provided on the TDM chip.

III. CLOCK AND TRIGGER DISTRIBUTION

The clock and trigger are carried on the same fibre by phase locking the clock. The clock/trigger distribution block-diagram is shown in Figure 7. The clock is fed into a phase-locked-loop (PLL) and distributed to the MCM assemblies through microcoax. The trigger is sent when a clock pulse is deliberately left out. When the PLL generates the missing pulse (and hence detected) a trigger pulse is generated and distributed through a second set of microcoax. An important observation is that the signal to noise ratio of the optical link remain high enough to maintain the integrity of the trigger. GaAs PLL clock distribution chips are available from both Vitesse and Tri-Quinn (see spec sheet in Figure 8). The PLL/distribution chip and receiver/amplifier pair are mounted on the inside of the cooling ring and metal 50-100 ohm microcoax are used to distribute the signal. A similar packaged circuit from Honeywell is shown in Figure 9 (with their DMUX chip replaced with the PPL/distribution chip).

06

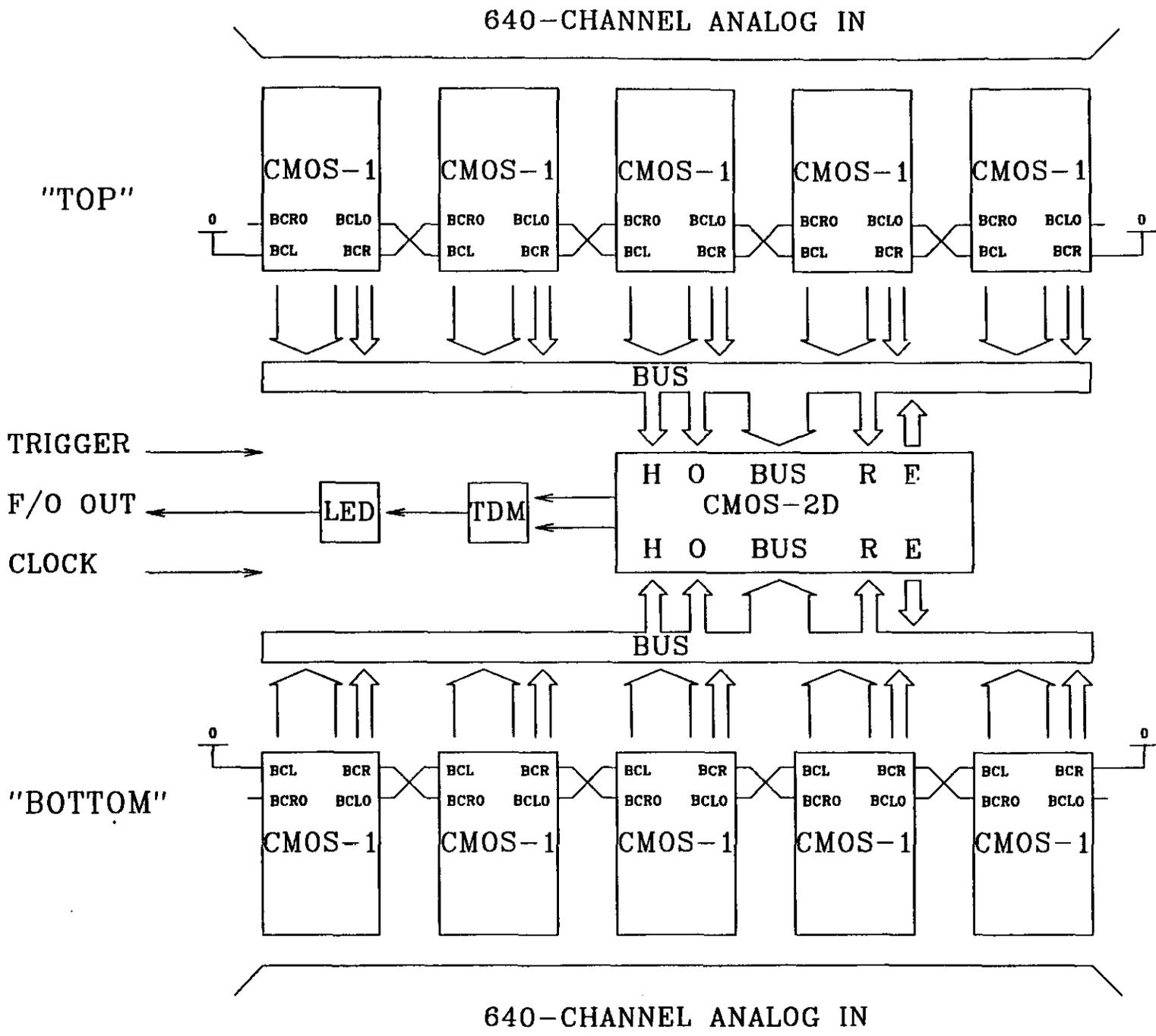
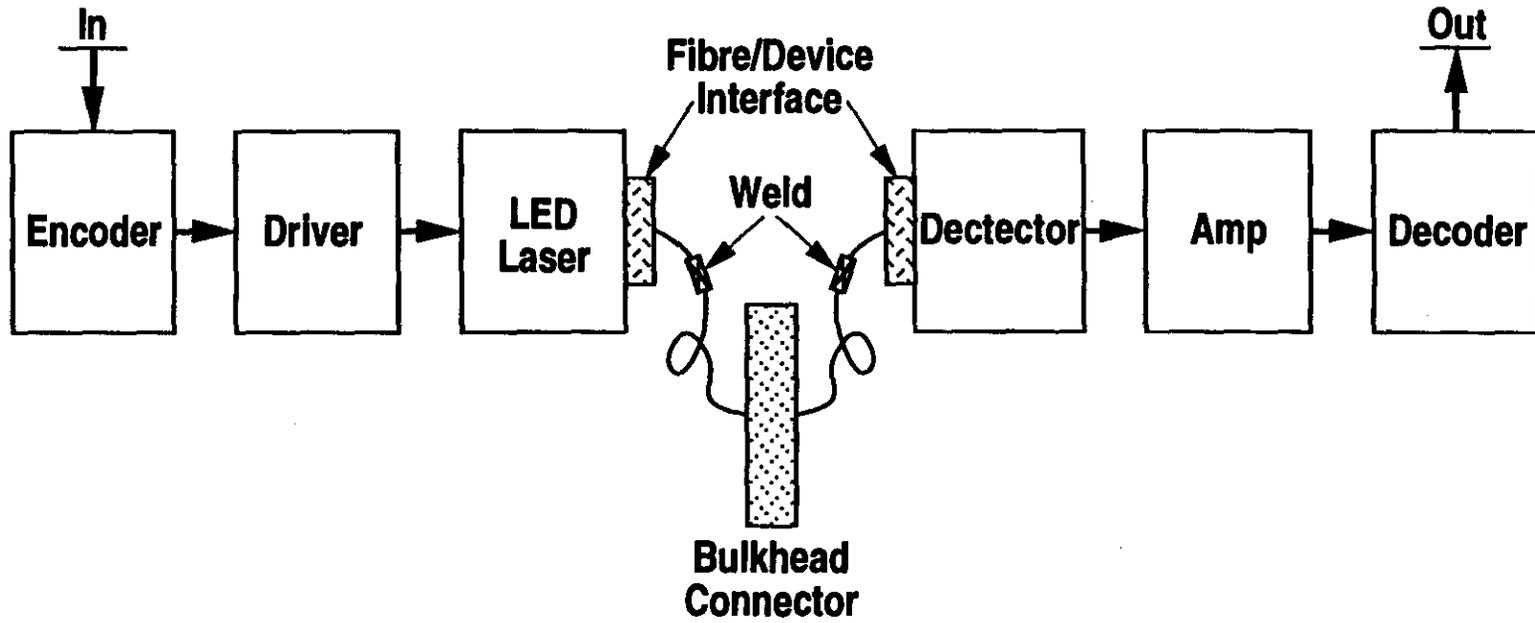


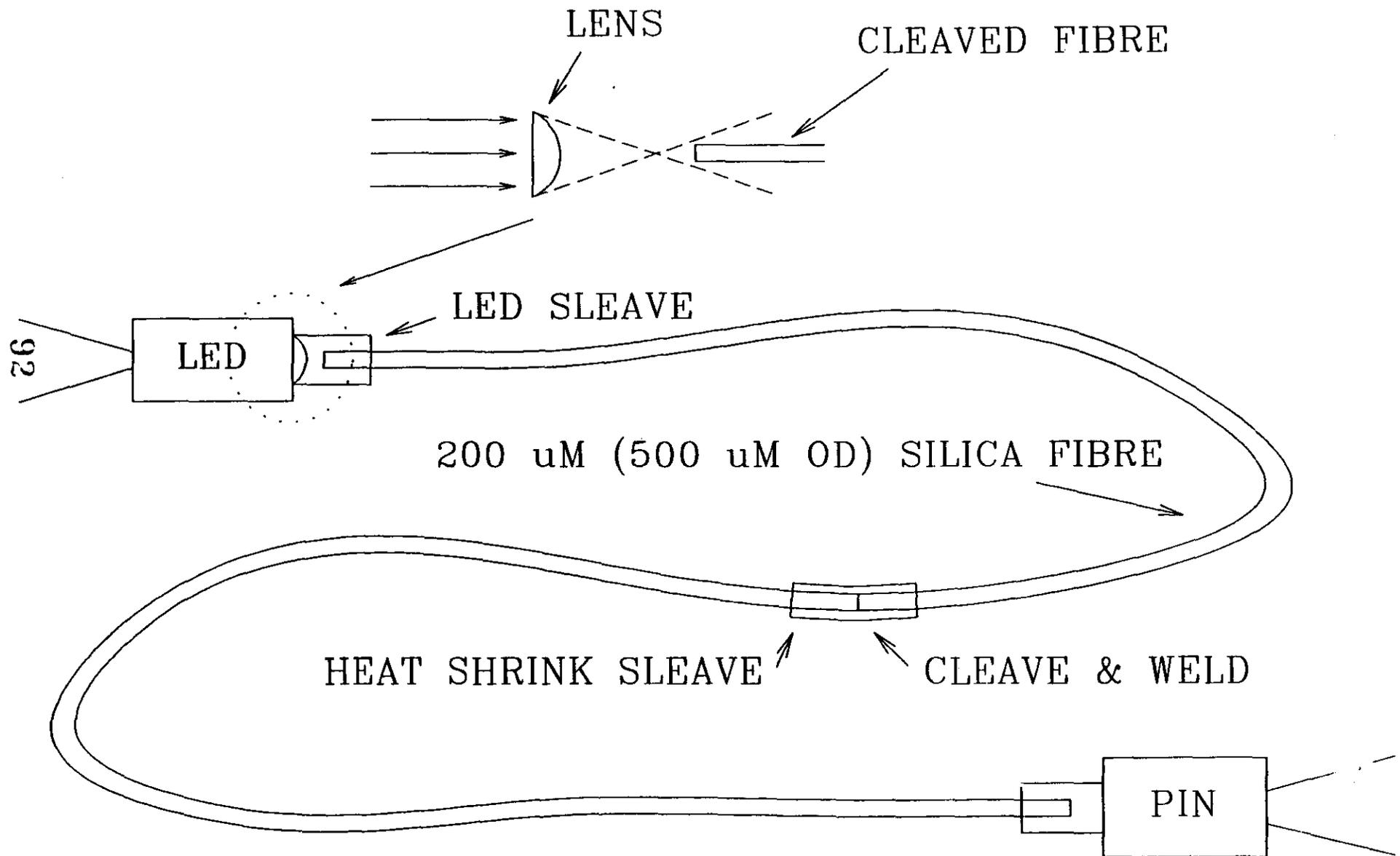
Figure 1

Optical Link



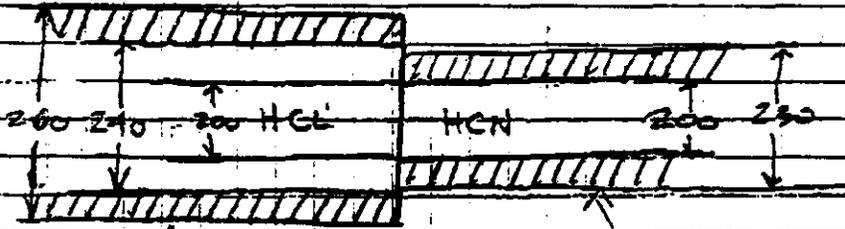
91

850 nm FIBRE OPTIC INTERCONNECT



DESIGN CONCEC

PROBLEM: CONNECTING DISSIMILAR FIBER SIZES

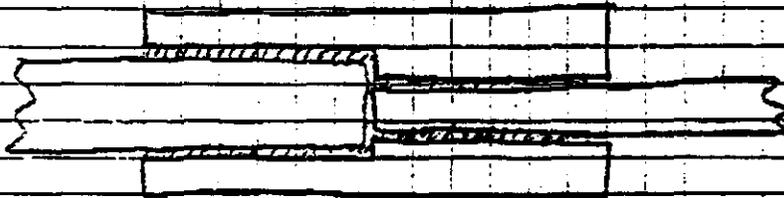


POLYMER COATING

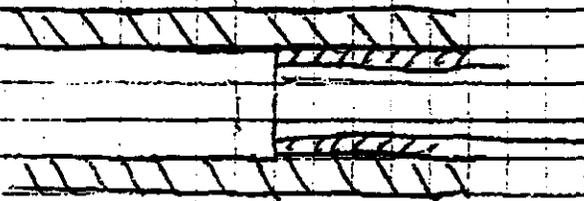
POLYMER COATING (SERVES AS CLADDING AS WELL)

DESIGN SUGGESTIONS

- 1) FUSION SPLICE AND THEN RECOAT WITH A SUITABLE EPOXY/POLYMER.
- 2) FABRICATE A MECHANICAL ALIGNMENT SLEEVE AND THEN EPOXY CLEAVED FIBERS IN PLACE



- 3) USE SHRINK TUBING TO BRING THE SMALLER DIAMETER FIBER UP TO 200 micrometers, THEN ATTACH WITH A SECOND PIECE



Fiber-cladding polymer

A polymer developed for termination cladding of quartz and plastic optical fibers is designed to prevent light loss. Epo-Tek 394 is a single-component system that cures at room temperature, through solvent evaporation, in only 30 seconds. Shore hardness is 80 and viscosity between 150-200 cp, with a glass-transition temperature of 40°C. The material provides >95% transmission through a thickness of 0.0005 in. from 2600-9000 Å, resulting in superior performance in UV-type light guides. Most optical epoxies will adhere well to the final fiber-optic connector termination. Epoxy Technology Inc., 14 Fortune Dr., Billerica, MA 01821.

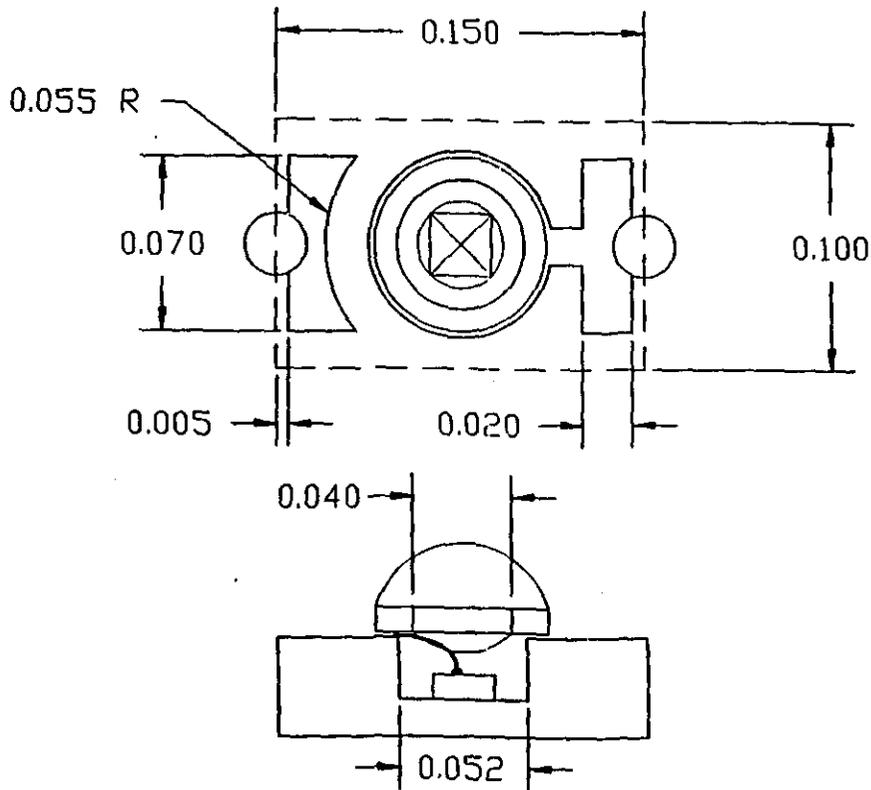
Circle Reader Service No. 316

4

3

2

1



Roger R. Ady
 Regional Programs Manager
 Special Products
 Optoelectronics Division

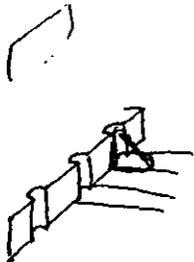
MICRO SWITCH
 Honeywell Inc.
 830 East Arapaho Road
 Richardson, TX 75081
 214 470-4267
 214 470-4417 Fax
 910 867-4757 Tex

BRAD,

THE BEAD LENS
 IS 12 MILS DIA AND WOULD
 SIT DIRECTLY ON THE LED
 SURFACE. THE LENS SHOWN
 WOULD NOT BE USED,

R

16

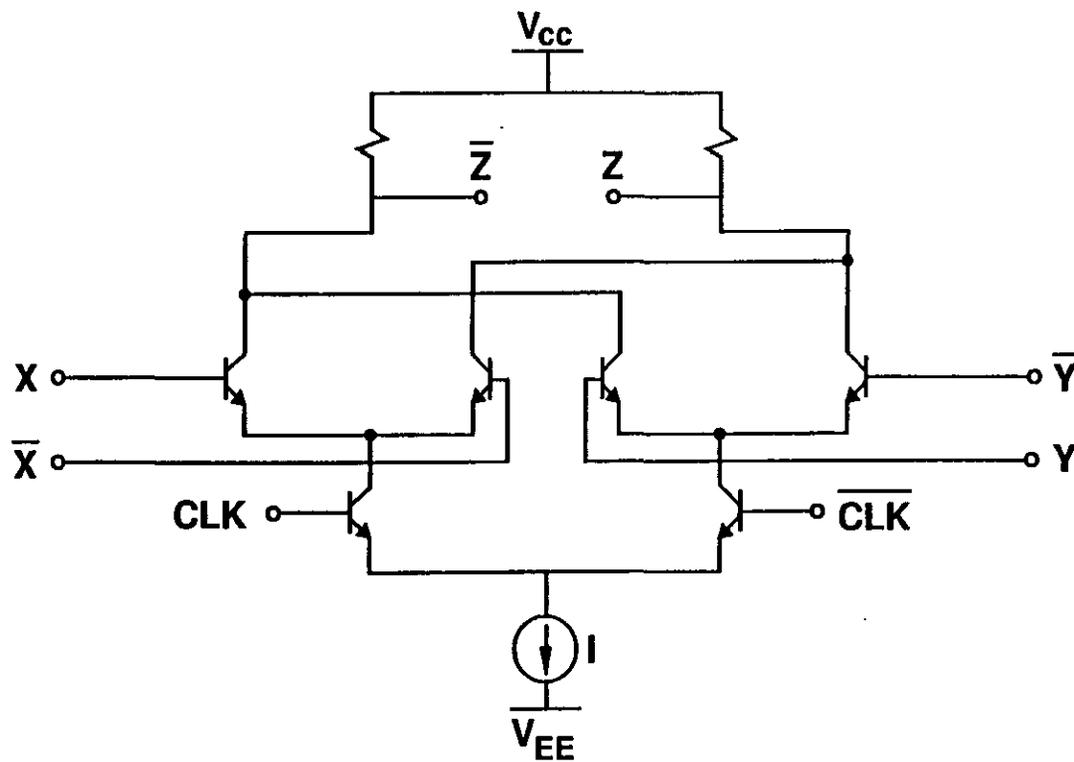


Honeywell Proprietary

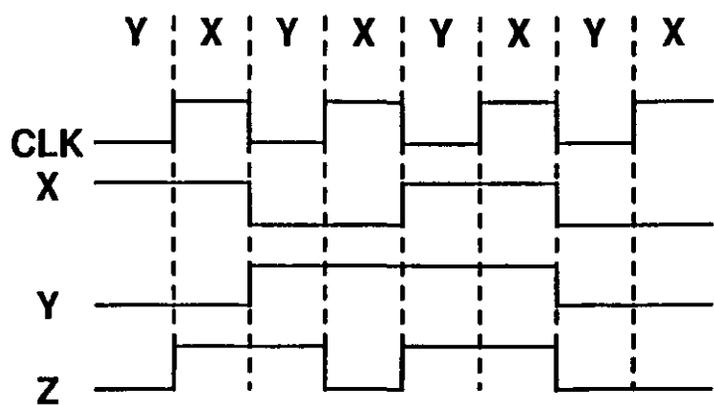
-FILENAME-				MATERIAL		D/E		HONEYWELL	
DOCUMENTATION CONTROL						D/C		OPTOELECTRONICS	
CLASS	EFFECT. DATE	APPROV.				D/C#		TITLE	
A						APPL.			
B						D/C#L. NO.			
C						DESIGN ACTIVITY			
D						D/E			
E						D/A			
				NEXT ASSY		USER DN		SIZE B	
								DWG. NO.	
								CALC	

Figure 5

2:1 TIME DIVISION MULTIPLEXER:



95

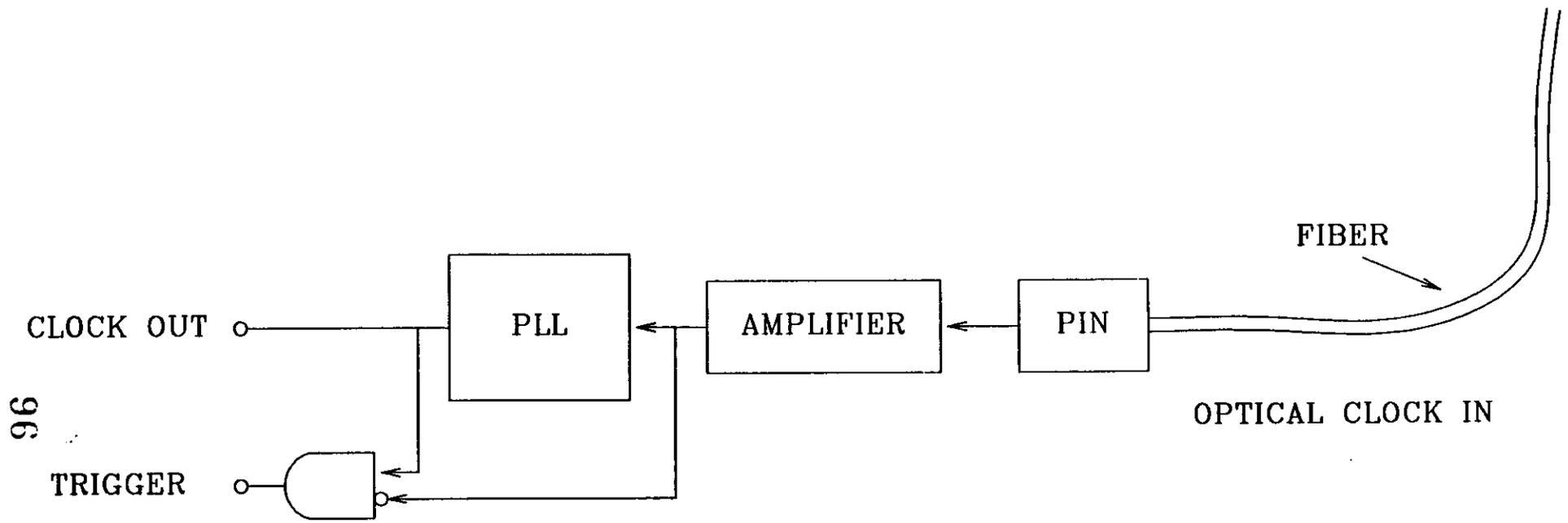


CLK = 1 → X
 CLK = 0 → Y

X	Y	CLK	Z̄	Z
0	0	0	1	0
0	0	1	1	0
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

Figure 6

CLOCK/TRIGGER DISTRIBUTION



96

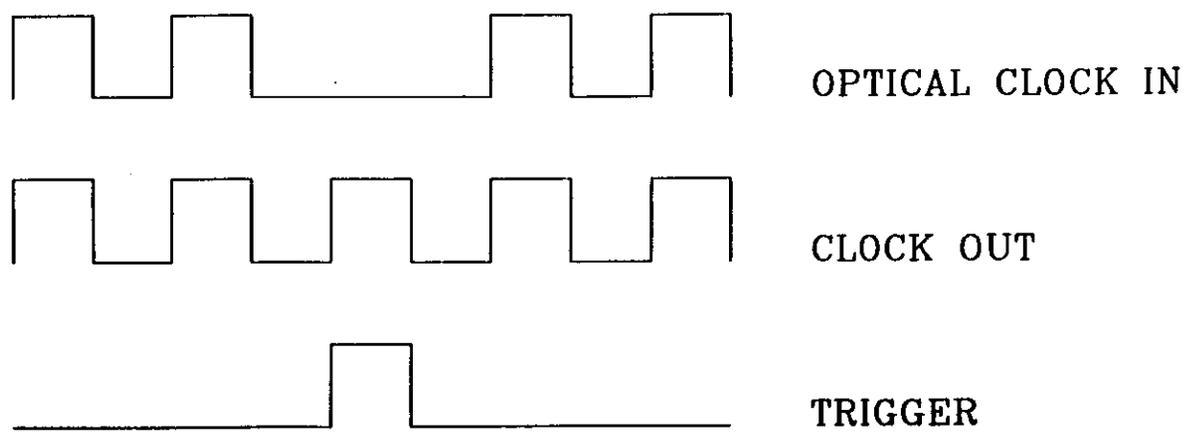


Figure 7

FEATURES

- Six outputs (Q) with maximum output-to-output skew of 500 ps
- Duty cycle: 50% \pm 10%
- Input reference clock frequency range from 25 to 100 MHz
- Additional outputs: Q6, Q7 at 1X, 2X, 4X the Q0-Q5 frequency
- TTL compatible inputs and outputs
- $I_{OL} = 24$ mA at $V_{OL} = 0.5$ V, $I_{OH} = -24$ mA at $V_{OH} = 3.0$ V
- Single +5V supply
- 400 mA supply current (max)
- 0°C to 70°C ambient operating temperature
- 28 pin MQAD™ package
- 200 ps effective delay

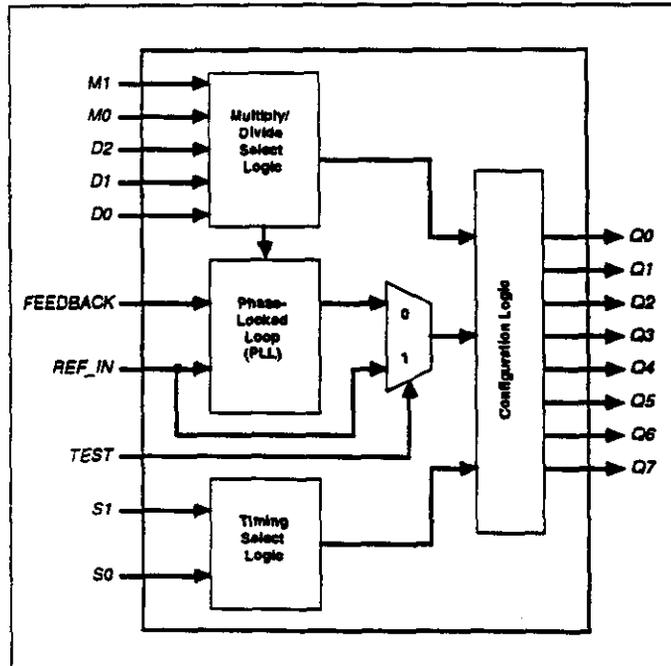
FUNCTIONAL DESCRIPTION

The VSL4485 clock driver chip is a Low-Skew TTL I/O Clock Driver which controls the phase and frequency of the output clocks through the use of an internal Phase-Locked-Loop (PLL) which operates at between 6X and 24X the input reference clock frequency. By feeding back one of the output clocks (to the FEEDBACK input), the PLL can maintain a fixed relationship between the input reference clock (REF_IN) and all outputs. The VSL4485 can also be used as a 2X and 4X

frequency multiplier by using one of the Q0-Q5 outputs as the FEEDBACK input and configuring the multiplier pins (M1, M0). The Q6, Q7 outputs will then run at multiples of the REF_IN frequency. The VSL4485 can also generate multiple phase relationships between the clocks. These output phase relationship configurations can be selected by the choice of the output used as the feedback input and the state of the select pins (S1, S0). In addition, the width of the phase increment can be varied from 4% to 16% of the Q output clock period by using the divider pins (D2:D0).

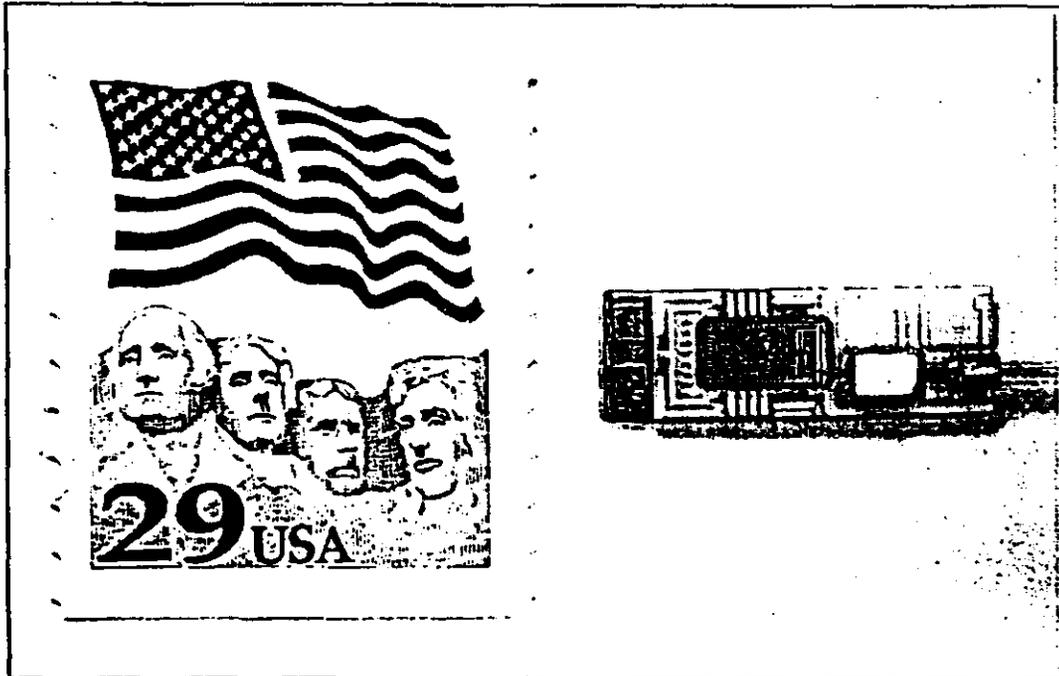
The VSL4485 is ideal for providing and distributing system clocks in advanced microprocessor based systems requiring clock frequencies in excess of 50MHz.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



Self-Contained Optical Receiver SCORE

86



Features:

Fully Monolithic Receiver including:

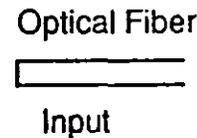
- Photodetector
- Amplifiers
- Link status monitor
- Clock recovery circuit
- 1:10 DMUX with 4B/5B decoder

- Broadband operation
- Burstmode capability
- Optical or electrical inputs
- Addressable
- Foundry produced
- Military qualifiable sub-assembly

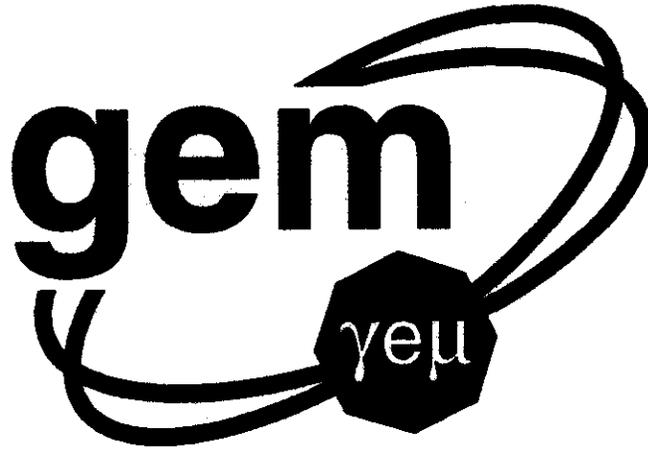
Specifications:

- Die size: .215" x .109"
- Serial data rate: 10 – 400 Mbit/s
- Input: (optical) 780 nm – 820 nm
- Sensitivity: < 50 uW
- Outputs: CMOS-TTL
- Power supply: -5V @ 200 mA
- Power dissipation: 1W

Address	DMUX with 4B/5B Decoder	Clock Recovery	Link Status Monitor
		Amplifiers	Opt. Detector



Honeywell



IPC Electronics

Jim Jusser

GEM
IPC Front End Electronics
Cost Estimate

12/92

Jim Musser

Indiana University

IPC Front End Requirements

- $S_{tot}/N > 200$

Set by 50 micron Position Resolution Req.

Pad Width = 2.5 mm

$$\frac{\sigma_x}{2.5mm} \cong \sqrt{3} (s_{tot}/n)^{-1}$$

- High Density

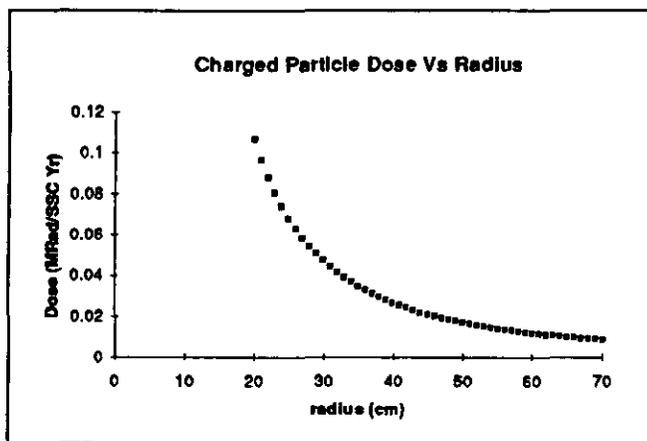
400,000 channels (1600 channels/IPC)

R/O Board area = 3-6 cm x 200 cm

2 ch/cm²

IPC Front End Requirments

- Rad-Hard



- Ionizing
Radiation

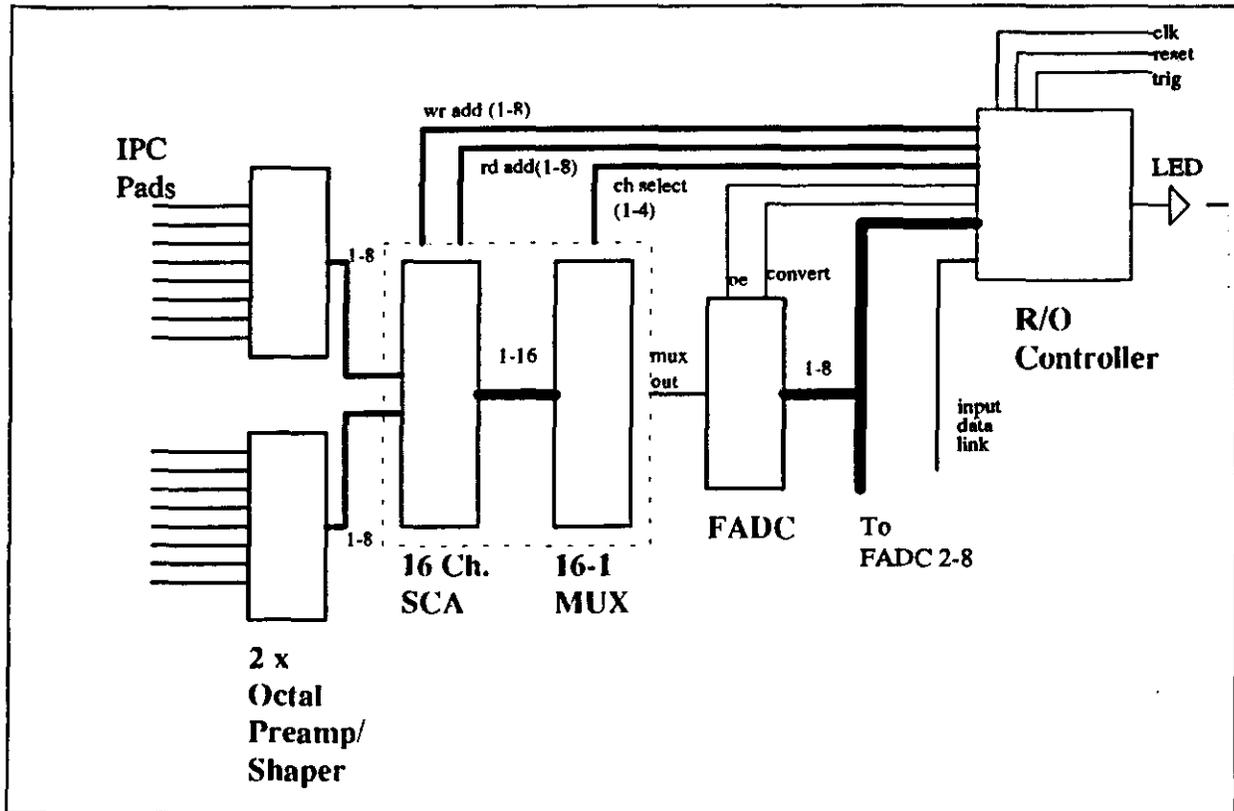
Dose = 0.025 Mrad/SSCY
@ 40 cm

2 Mrad = 80 SSC Yr

- Neutrons

2×10^{14} N/cm² = 100 SSCY

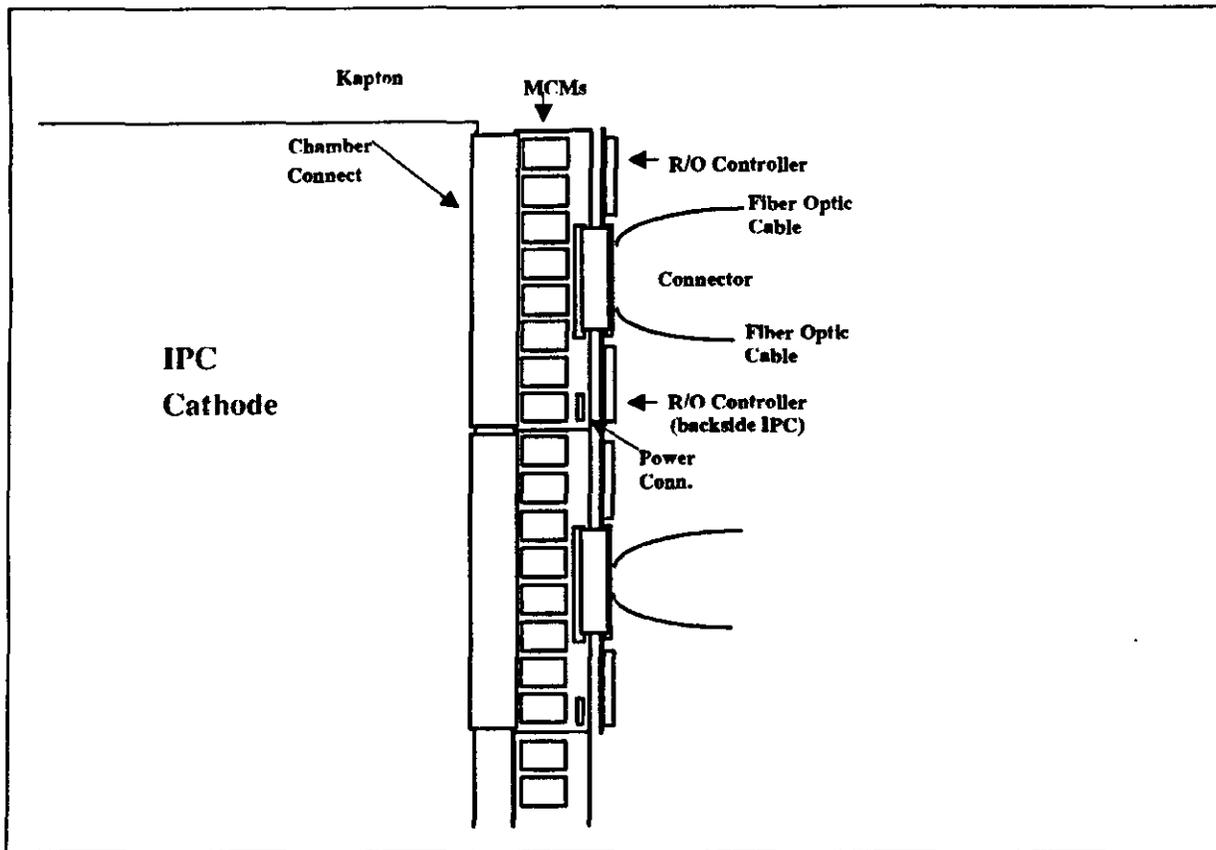
IPC Front End Architecture



WBS Dictionary

Preamp/Shaper	50.2.2.2.3.4.1
SCA/MUX	50.2.2.2.3.4.2
FADC	50.2.2.2.3.4.3
R/O Controller	50.2.2.2.3.4.4
LED/ fiber link	50.2.2.2.3.7.2

IPC Front End Electronics Layout

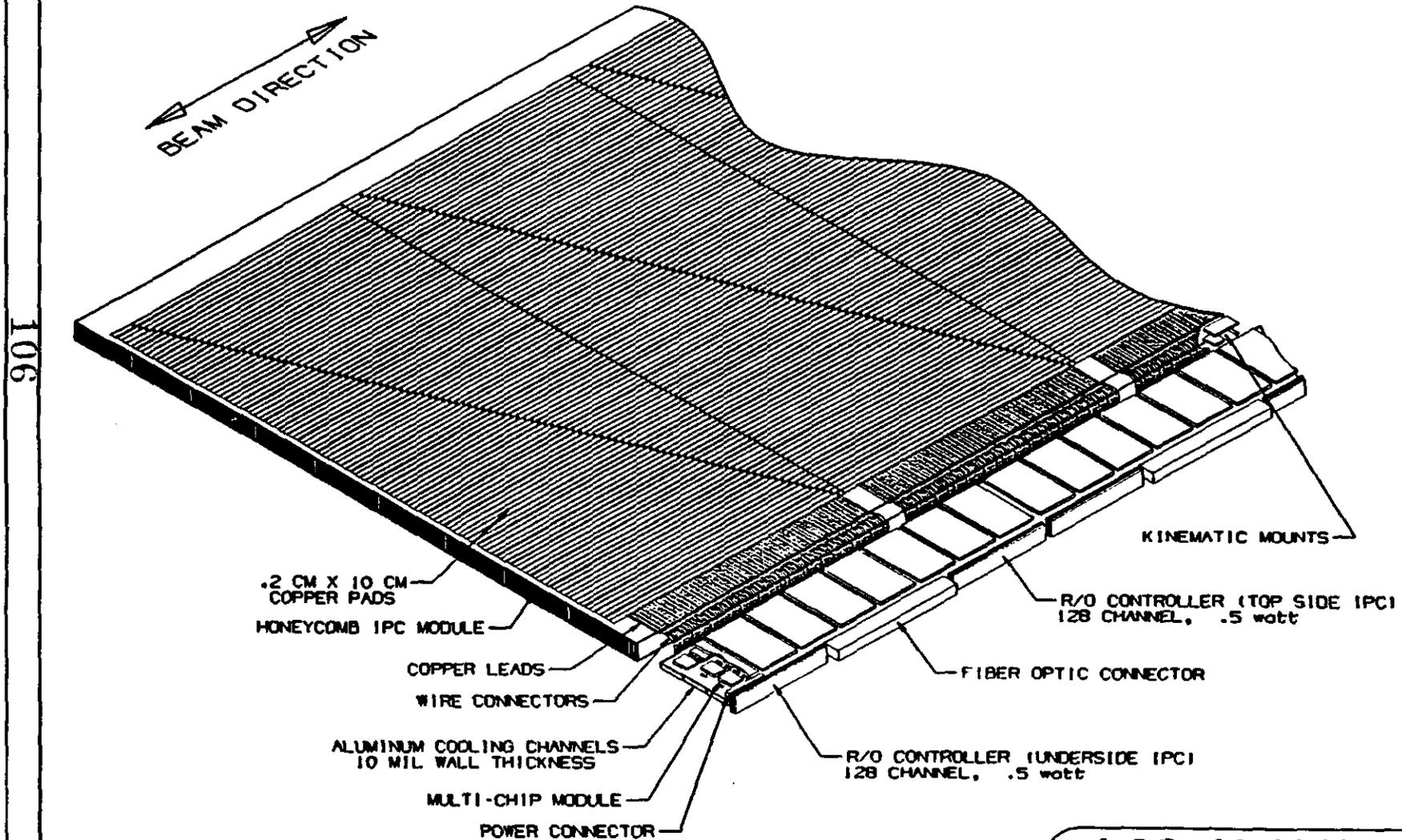


WBS Dictionary

R/O PC Board	50.2.2.2.3.5.1
Controller PC Board	50.2.2.2.3.5.2
R/O Controller	50.2.2.2.3.4.4
Low Voltage	50.2.2.2.3.2
High Voltage	50.2.2.2.3.1
MCM	50.2.2.2.3.5.3
Fiber Link	50.2.2.3.7.2

GEM IPC TRACKER

IPC MODULE ASSEMBLY

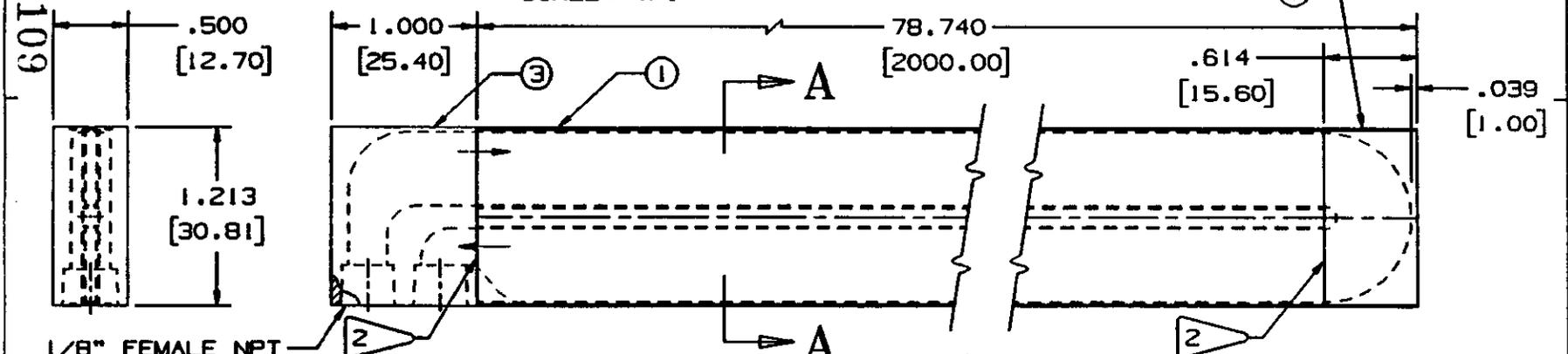
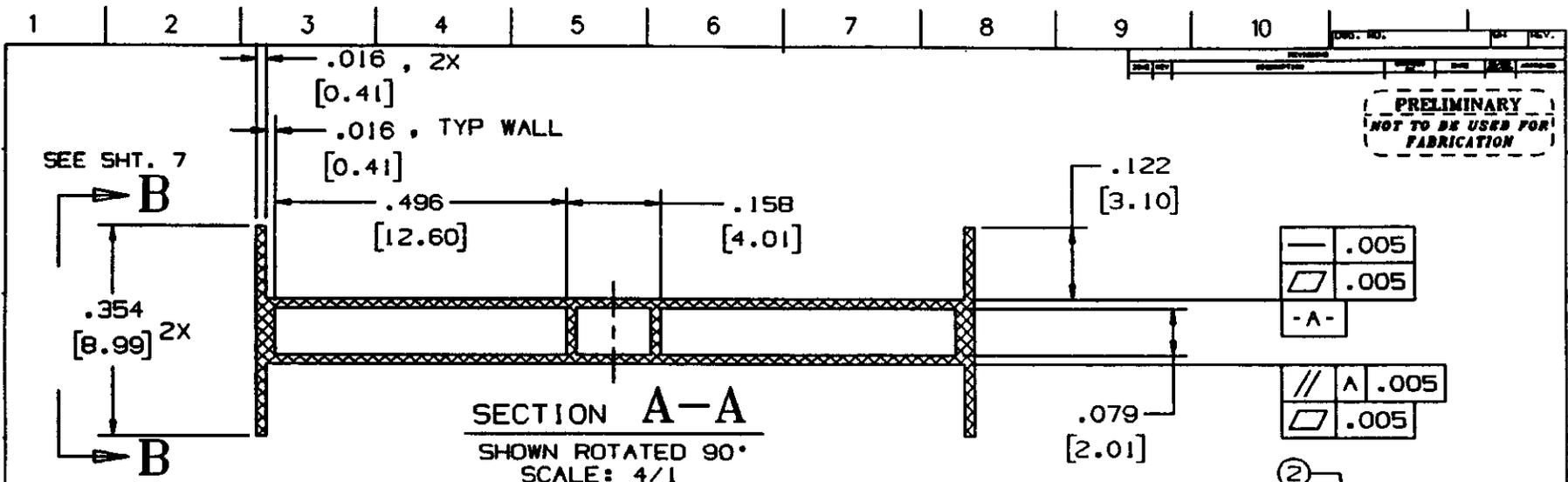


ALL DIMENSIONS ARE IN mm

LOS ALAMOS

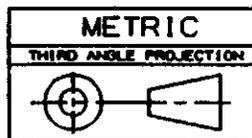
MEE-12
MECHANICAL AND ELECTRONIC
ENGINEERING DIVISION

JRYCOOLASBY 8-31-82



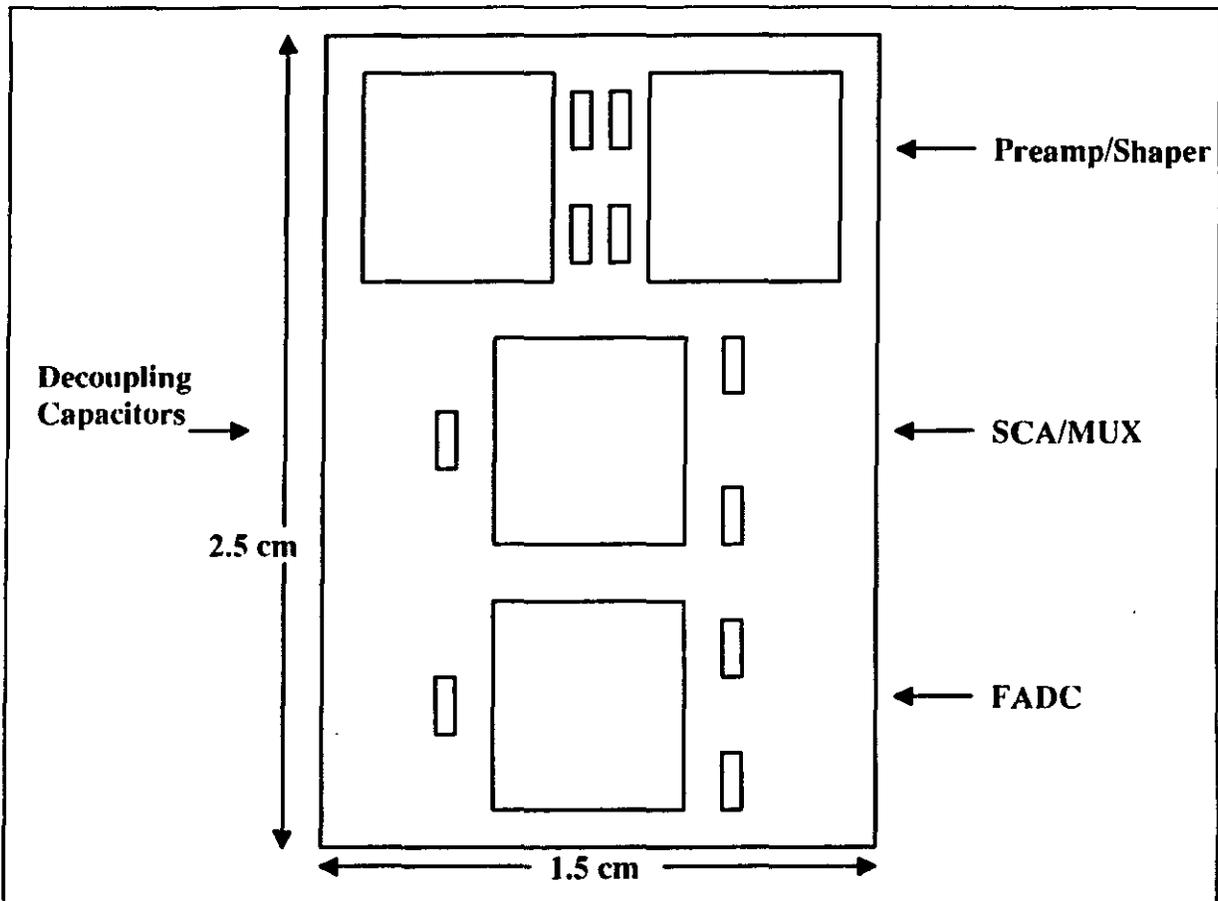
- NOTES:
- PART MATERIAL TO BE GRAPHITE/EPOXY PREPREG TAPE P75/054-3 OR K130/054-3. NOMINAL PER PLY THICKNESS .001 INCHES. QUASI-ISOTROPIC LAY-UP OF 8 PLYS REPEATED X 2 SUB-GROUPS.
 - PARTS TO BE BONDED TOGETHER WITH THE FOLLOWING ADHESIVE. DIMENSIONS ARE SHOWN IN INCHES & (MILLIMETERS). DEXTER HYSL ROOM TEMPERATURE CURE EA930 OR EQUIV. ADHESIVE BOND LINE THICKNESS TO BE .002".

1/4"	ADHESIVE	SEE NOTE #2	4
1	END CONNECTOR	ALUMINUM	3
1	RETURN LOOP	ALUMINUM	2
1	COOLING CHANNEL	SEE NOTE #1	1
-1	PLATE	ALUMINUM	12



Los Alamos MANUFACTURING
 GEM IPC TRACKER
 IPC ELECTRONICS
 WATER COOLING CHANNEL
 AI SK-GEM12-050
 6

Multi-Chip Module (MCM) IPC Front End

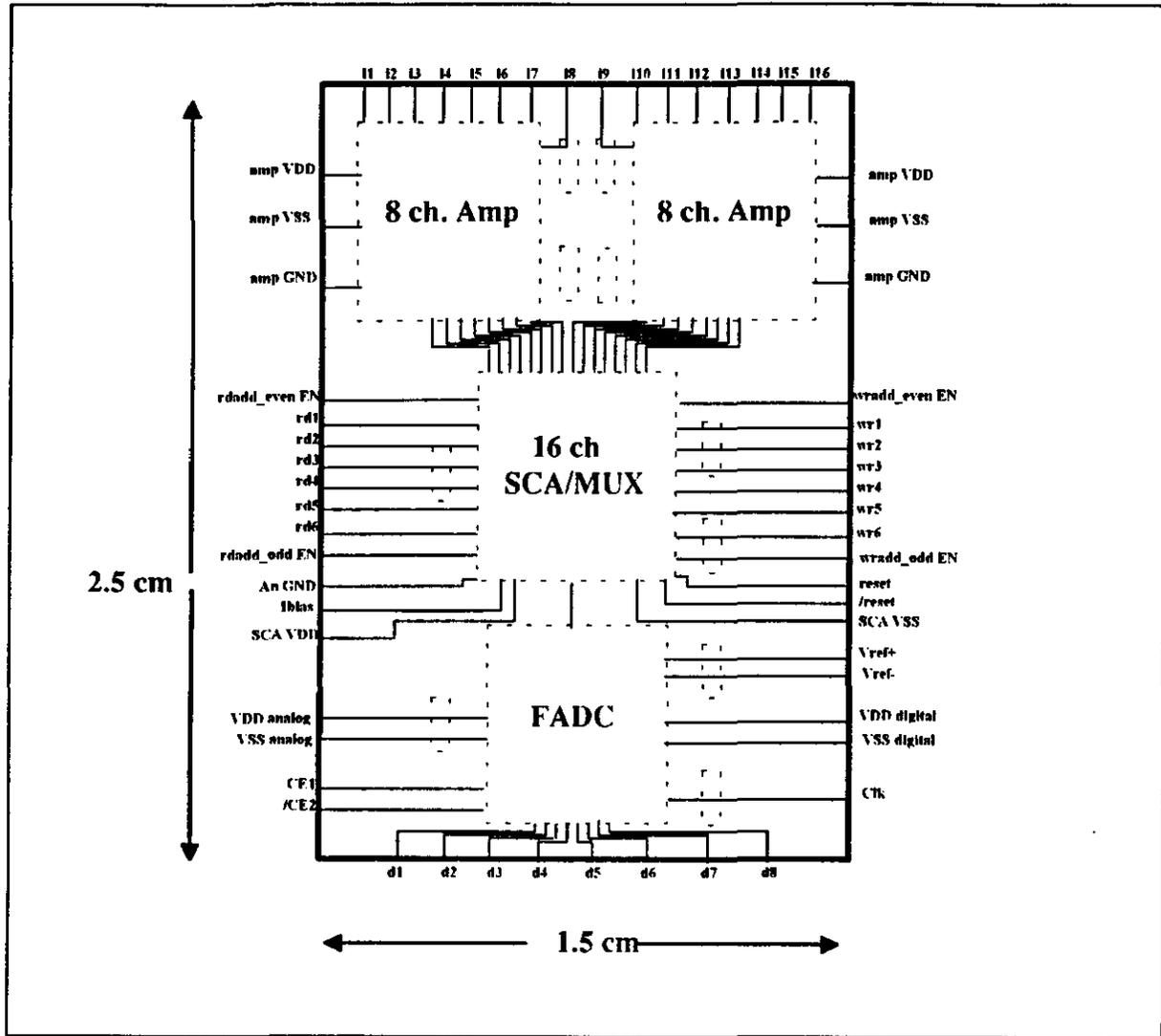


1 MCM/Hybrid per 16 IPC Channels

Components:

Octal Preamp/shaper	1 per 8 ch.s
16 Channel SCA/MUX	1 per 16 ch.s
8 bit FADC	1 per 16 ch.s

IPC Interconnects



Preamp/Shaper Cost Estimate

R&D

3 rad-hard fab. runs - shared with SCA
\$85K per run
1 FTE engineer/tech. through 1994 @\$139K/yr

E&D

0.5 FTE engineer
\$42K Pre-production fab run

I&A

50 MD

Proc/Fab - based on Harris quote

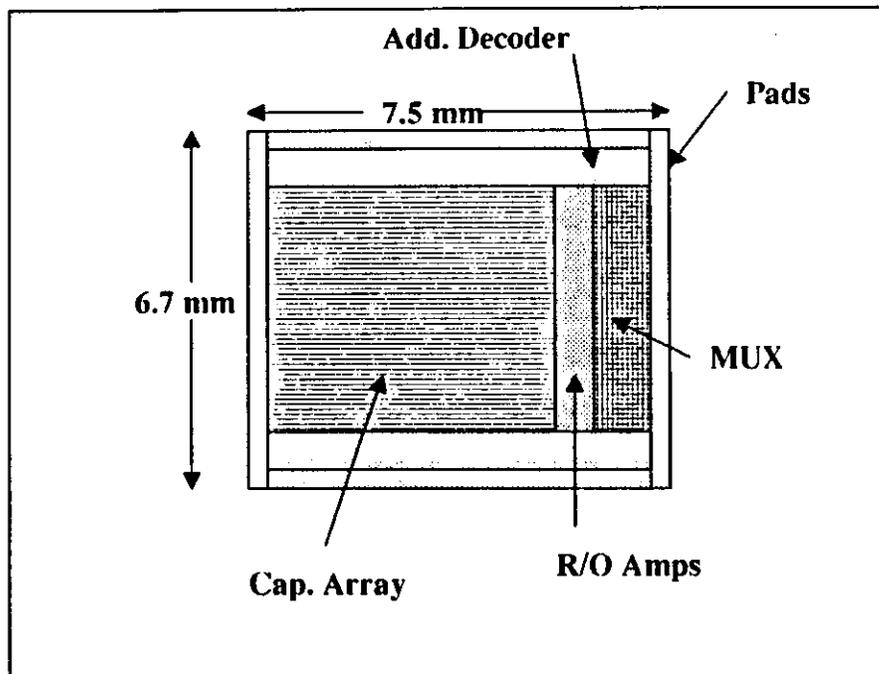
\$3000/ 4 inch wafer
die size = 5.6 mm²
80% yield
\$2.68/ good die + \$10.00/die testing+\$88K NRE

Cont.

39 %

SCA Specifications

- 8 Bit Dynamic Range
- Single bucket R/O time < 500 ns
- Simultaneous Read/Write Capability
- 60 Mhz clocking rate
- Integrated 16-1 multiplexer
- length > level 1 latency period
- local level 1 buffering
- rad-hard - 2 Mrad



SCA

Cost Estimate

R&D

3 rad-hard fab. runs - shared with Amp

\$85K per run

1 FTE engineer/tech through 1994 @\$139K/yr

E&D

0.5 FTE-engineer

\$42K pre-production fab run

Test Station - \$50K

I&A

60 MD

Proc/Fab - based on Harris quote

\$3000/ 4 inch wafer

die size = 50 mm²

40% yield

\$50.00/ good die + \$10.00/die testing+\$88K NRE

Cont.

39 %



HARRIS

HS - 9008RH

CMOS 8-Bit Flash Analog-to-Digital Converter

Preliminary

Features

- Excellent noise rejection - Fully differential design
- Superior linearity (0.5 LSB Typical)
- Single reference supply
- CA3318 pin compatible option available
- Low power (400 mW Typical)
- 25 MHz sampling rate (40 ns conversion time)
- Total Dose Hardness to 300 KRad

General Description

The Harris HS-9008RH is a CMOS 8 Bit Flash Converter designed for space applications where relatively low power, exceptional accuracy and very fast conversion speeds are a necessity.

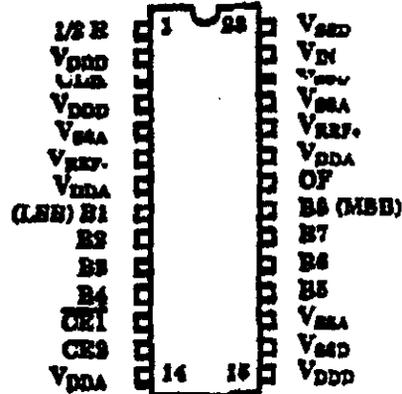
The HS-9008RH design differs substantially from most other available Flash Converters as it employs fully differential analog input sampling networks and amplifiers, as well as regenerative, offset nulled (error correcting) comparators. These circuit techniques improve noise performance and render the circuit much less sensitive to process and radiation induced device parametric shifts. Outstanding integral and differential linearity error is achieved through the use of a metal film resistor network which exhibits >10 bit linearity without trim. As a result of these innovations, the device operates with a single fixed reference supply as opposed to the multiple, adjustable references used in similar devices.

The HS-9008RH is fabricated in Harris' new AVLSI1RA process, which is dual level, twin well, thin EPI, 1.25 uM bulk CMOS process. The capacitors are metal to metal with a nitride dielectric and have a negligible attenuation factor.

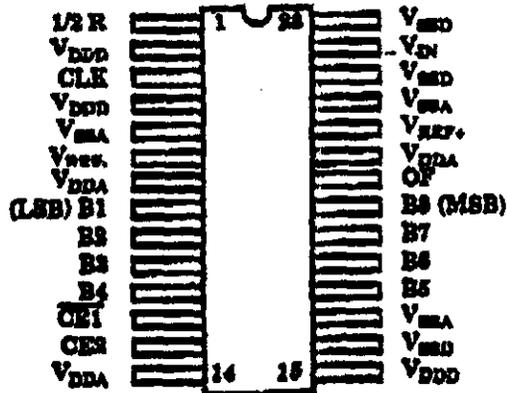
This combination of factors makes the HS-9008RH one of the best 8 Bit Flash Converters available in the Commercial, Military or Rad Hard mar-

Pinouts

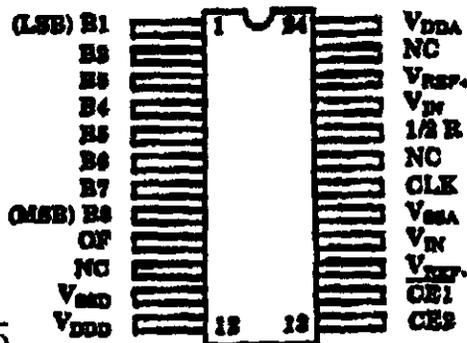
**28 Pin DIP
(HS1-9008RH)**



**28 Flatpack
(HS9-9008RH)**



**24 Flatpack *
(HS9A-9008RH)**



FADC Cost Estimate

Harris HA9008 quote

I&A

30 MD

Proc/Fab

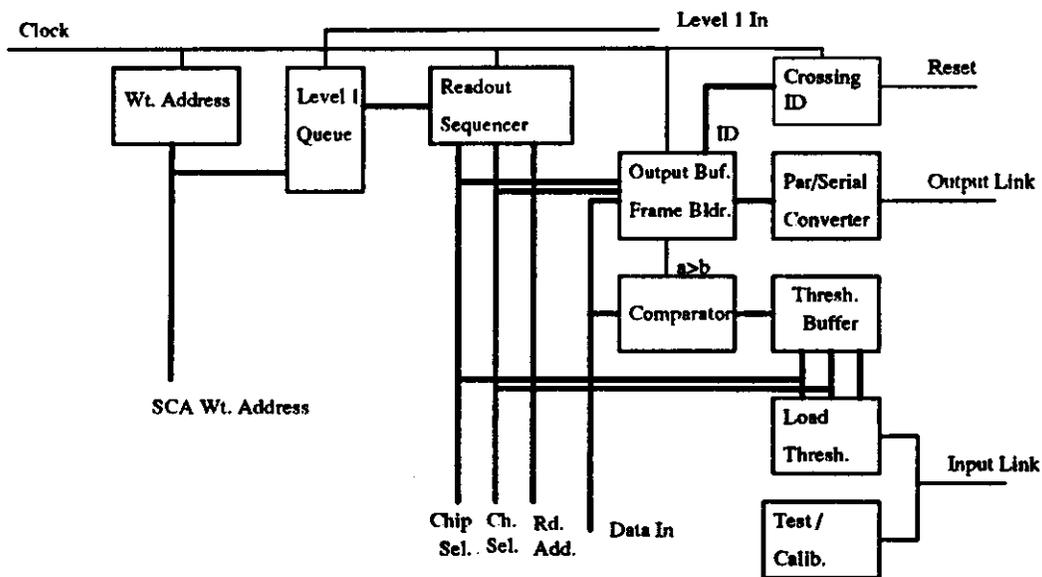
\$50.00 /die + \$10.00/die testing

Cont. :

39 %

R/O Controller

- ◆ Generates SCA read/wr ite addresses
- ◆ Controls readout sequence
- ◆ Zero suppresses non-hit channels
- ◆ Builds data packet and queues for output - provides serial stream to data link.
- ◆ Calibration/Test
- ◆ Rad-Hard - 2 Mrad



**RHASIC
LRH20000
Radiation
Hardened Series
Preliminary**

20051

Description

RHASIC is the LSI Logic family of radiation hardened application-specific integrated circuits. The LRH20000

RHASIC Series is a Channel Free™ gate array technology offering superior speed performance and high gate counts. The device is processed using 1.0 micron, 2-layer metal, epitaxial bulk silicon HCMOS technology. Densities from 14,000 to 170,000 equivalent gates are offered. Usable gate capacities from 5000 to 70,000 gates, and up to 348 signal I/Os can be implemented.

The speed and range of gate counts available in the LRH20000 Series make it ideally suited for achieving system-to-silicon integration. Sophisticated algorithms incorporated in LSI Logic's proprietary Concurrent

Modular Design Environment™ (CMDE[®]) development software allow a circuit designer's modular hierarchy to be utilized to its maximum potential. By performing an optimized functional placement of these building blocks, and then collapsing and compacting them to minimum size, substantial benefits are realized in both speed and silicon area utilization.

Output buffer drive strengths of 0.8, 1.6, 3.2, 4.8, 6.4 and 9.6 mA are available and determined by the user during the design phase. Also available is output slew rate control that allows dV/dt of each output to be tailored to individual load conditions.

Overview

- Guaranteed total dose specification 3E6 rad (Si)
- Upset resistant for dose rates up to 1E9 rad(Si)/sec
- Latch-up resistant to dose rate $\geq 1E^{12}$ rad(Si)/sec
- SEU 2E-10 errors/bit-day measured at room temperature on a latch type memory structure without cross-coupled resistors. Actual value will be design and layout dependent.
- No SEU latchup for 320MeV Au ions, LET=200MeV/mg/cm²
- Silicon-gate 1.0 micron (0.7 micron effective), 2-layer metal HCMOS technology
- Up to 348 signal I/O capability
- Speed performance of 0.40nS through 2-input NAND gate, standard load =2
- Extensive macrocell, macrofunction and megafunction library elements (directly compatible with industry standard LCA10000 series)
- Seven array sizes from 5,000 to 50,000 usable gates (to 70,000 gates in early 1992)
- High reliability gate oxide isolation
- Fully supported by CMDE software for verification, simulation and layout
- Spice based library for pre- and post- radiation simulations
- Channel-Free architecture for maximum layout flexibility
- Configurable output drive up to 9.6 mA with slew rate control capability
- Inputs and outputs protected from over-voltage and electrical latchup
- TTL/CMOS I/O compatibility
- Efficient implementation of large logic blocks
- Advanced packaging available
- Can be processed to Level S Reliability requirements
- On board process monitor circuit included in all designs
- Radiation Hardness test data available through Mil/Aero Marketing under ITAR restrictions

R/O Controller Cost Estimate

R&D

2 fab. runs LSI Logic
\$25K per run 50 parts each
\$76K NRE
1 FTE engineer through 1994 @\$78K/yr

E&D

0.5 FTE engineer

I&A

30 MD

Proc/Fab

\$104.00/part + \$76K NRE

Cont. :

15 %

R/O Link & Reciever Cost Estimate

R&D

10 prototype links @ \$143.00/link
100 MD design & test - primary R&D by LANL
1 prototype Reciever board fab - \$3K
120 MD Reciever board design

E&D

120 MD Eng. - Link

I&A

\$10.00/link testing

Proc/Fab

Optics - \$143.00/link (LED+cable)
Reciever - 32 channel board @ \$2.8K/board
6 9Ux400 mm VME Crates @ \$2.5K/crate

Cont. :

19 %

Power System Cost Estimate

E&D

Low Voltage System

100 MD Eng

Hi Voltage System

100 MD Eng.

Proc/Fab

Low Voltage System

150 300W switching supplies @ \$500/supply

4 - 30 m shielded 12 gauge wire per chamber

High Voltage System

LeCroy 1449 mainframe + 20 LeCroy 1443 pods

\$45.9K

Distribution - 80 m cable runs x 320 chambers

@ \$60/cable

Installation

80 MD - High Voltage System

80 MD - Low Voltage System

Cont. : 8 %

PC Board/Packaging Cost Estimate

R&D

Fab. 500 MCMs @ \$45.00/MCM + \$50K NRE
1.5 MY MCM design/testing
Fab. & stuff 50 R/O boards @ \$250.00/board
1 MY R/O board design/test
Fab. & stuff 25 Controller boards @ \$250.00/board
1 MY R/O board design/test

E&D

0.5 MY MCM design
0.5 MY R/O board design
0.5 MY Controller board design

I&A

90 MD

Proc/Fab

MCM - \$12.00/cm² + \$10.00/MCM test
R/O Board - 4 layer Kapton flexboard -
\$2.00/in² + \$15.00/board stuff & test + \$20K NRE
Controller Board - 4 layer Kapton flexboard
\$2.00/in² + \$15.00/board stuff & test + \$20K NRE

Installation:

1 MY

Cont. :

22 %

FADC Specification

- ◆ 8 Bit
- ◆ 25 Mhz convert rate
- ◆ <1 LSB integral linearity
- ◆ <1 LSB differential linearity
- ◆ < 0.5 W total power consumption
- ◆ rad-hard 2 Mrad

**Deliverables and Milestones in IPC Electronics R&D Effort
(from Jan. 93 to April. 95)**

**J. Musser
12/3/92**

Item	Milestones	Date
Amp IC	Submission of first Rad-Hard fab	Jan 93
	Testing begins	April 93
	Design revision start	June 93
	2nd prototype fab run submission	Sept 93
	3rd prototype fab run submission	April 94
	Pre-production fab run submission	Nov 94
	Full production start	April 95
SCA IC	Submission of first Rad-Hard fab	Jan 93
	Testing begins	April 93
	Design revision start	June 93
	2nd prototype fab run submission	Sept 93
	3rd prototype fab run submission	April 94
	Pre-production fab run submission	Nov 94
	Full production start	April 95
FADC	Testing of Harris HA4008	Jan 93
	Is HA4008 usable?	Feb 93
Readout Controller	Xilinx Prototype complete	Jan 93
	Prototype tests complete	Sept 93
	Specifications finalized	Sept 93
	Rad-Hard gate array (LSI LOGIC) design started	Sept 93
	Pre-Production rad-hard Controller available	April 94
	Production fab started	Jan 95
MCM	Technology demo fabrication	Oct 93
	Full design rules available	June 94
	Pre-production prototypes available	Sept 94
	Final design for production fab release	April 95

**Deliverables and Milestones in IPC Electronics R&D Effort
(from Jan. 93 to April. 95)**

**J. Musser
12/3/92**

Page 2 of 2

Fiber Optics	Engineering demo of rad-hard links Final Design for production release	Oct 93 Oct 94
System Tests	Prototype system tests start Pre-Production system test	Aug 93 Jan. 95

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.1.1
 WBS Descript: Prod. High Voltage Supplies
 WBS QTY: 320
 WBS UM: channels

	Risk	
	Factors	Weight %
Technical	1	2
Cost	1	1
Schedule	2	1

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

127

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- Lecroy 1449 Mainframe	2	crates			5.9
4- Lecroy 1443 High Voltage Pods	20	modules			2
3- Checkout	60	MD	SSC05	0.0045	
6- Installation	20	MD	SSC05	0.0045	

Notes:
Prepared B.J. Musser

sub. 63.68
sub+cont. 66.2272

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.3.2.1.2
 WBS Descript: High Voltage Distribution
 WBS QTY: 320
 WBS UM: channels

	Risk	
	Factors	Weight %
Technical	2	2
Cost	4	4
Schedule	2	2

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

128

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product MY/UM	Mat'l Unit Cost
4- Cable	25000	meters			0.0005
4 - Connectors	640	cable ends			0.01
1- Cable Run Design	100	MD	SSC02	0.0045	
2- Fabrication	40	MD	SSC05	0.0045	
6- Installation	60	MD	SSC05	0.0045	
3- I/A	15	MD	SSC05	0.0045	
4- misc . hardware (cable ties, labels)					5

Notes:
Prepared B.J. Musser

sub. 67.0275
sub+cont. 72.3897

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.2.1
 WBS Descript: Low Voltage Supply
 WBS QTY: 30000
 WBS UM: Watts

	Risk	
	Factors	Weight %
Technical	1	2
Cost	1	1
Schedule	2	2

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

129

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product MY/UM	Mat'l Unit Cost
4- 300 W Switching Regulators	150	supplies			0.5
4- Rack /mounting	4	racks			0.75
4- monitoring system - 150 ch CAMAC-based scanning ADC	1	system			89
3- Checkout	10	MD	SSC05	0.0045	
6- Installation	20	MD	SSC05	0.0045	

Notes: monitor cost based on Kinetic Systems crate, controller, and 25 32 ch scanning ADCs sub. 171.455
 Prepared E.J. Musser sub+cont. 180.02775

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.2.2
 WBS Descript: Prod. Low Voltage Distribution
 WBS QTY: 320
 WBS UM: chambers

	Risk	
	Factors	Weight %
Technical	1	2
Cost	1	1
Schedule	2	2

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

130

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product MY/UM	Mat'l Unit Cost
4- Wire (two 30 m lengths of 2 cond. shielded 12 gauge per cham)	19.2	km			3.25
4- misc hardware (cable ties, labels)	1				5
1- Cable Run Design	100	MD	SSC02	0.0045	
6- Installation	60	MD	SSC05	0.0045	
3- I/A	15	MD	SSC05	0.0045	

Notes:
Prepared E.J. Musser

sub. 109.5875
sub+cont. 115.066875

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.4.1
 WBS Descript: Prod. Preamp/Shaper
 WBS QTY: 400000
 WBS UM: channels

	Risk	
	Factors	Weight %
Technical	8	32
Cost	3	3
Schedule	4	4

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

131

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- 8 channel preamp/shaper die	50000	die			0.0027
1- final design/simulation	0.5	MY	ORNL1	1	
3- bid pkg	30	MD	NL05	0.0045	
4- Testing and Verification	50000	die			0.01
4- Testing and Verification (NRE)	1				130

Notes: Harris bid - assume 80% yield
 Prepared E.J. Musser

sub. 850.43
 sub+cont. 1182.0977

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.4.2
 WBS Descript: Prod. Switched Cap Array
 WBS QTY: 400000
 WBS UM: channels

	Risk	
	Factors	Weight %
Technical	8	32
Cost	3	3
Schedule	4	4

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

132

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- 16 channel SCA die	25000	die			0.05
1- final design/simulation	0.5	MY	ORNL1	1	
3- bid pkg	30	MD	NL05	0.0045	
4- Wafer Level Testing and Verification	25000	die			0.01
4- Wafer level Testing and Verification (NRE)	1				130

Notes: Harris bid - assume 40% yield
 Prepared B.J. Musser

sub. 1715.43
 sub+cont. 2384.4477

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.4.3
 WBS Descript: Prod. FADC
 WBS QTY: 25000
 WBS UM: channels

	Risk	
	Factors	Weight %
Technical	8	32
Cost	3	3
Schedule	4	4

- Functional Activity: 1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

133

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- HA4008 Rad-Hard 8 bit FADC - unpackaged	25000	die			0.05
				1	
3- bid pkg	30	MD	NL05	0.0045	
4- Wafer Level Testing and Verification	25000	die			0.01
4- Wafer level Testing and Verification (NRE)	1				130

Notes: Harris bid - assume 40% yield
 Prepared B.J. Musser

sub. 1645.93
 sub+cont. 2287.8427

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.4.4
 WBS Descript: Prod. R/O Controller
 WBS QTY: 3125
 WBS UM: ICs

	Risk	
	Factors	Weight %
Technical	4	8
Cost	3	3
Schedule	4	4

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

134

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- LSI Logic LRH20051 Gate Array	3125	ICs			0.104
3- bld	10	MD	IUENG1	0.0045	
3- test	0.5	MY	IUENG2	1	
1- design	0.5	MY	IUENG1	0.0045	

Notes:
Prepared E.J. Musser

sub. 359.1855
sub+cont. 413.063325

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.5.1
 WBS Descript: Prod. R/O Board
 WBS QTY: 3840
 WBS UM: boards

	Risk	
	Factors	Weight %
Technical	4	8
Cost	4	4
Schedule	2	2

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

135

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- 16x3 cm 4 layer flexible Kapton pc boards	28600	square in			0.002
				1	
3- bid pkg	30	MD	IUENG1	0.0045	
1- Design/Layout	120	MD	IUENG1	0.0045	0.01
5- Stuff with MCMs & test	3820	boards			0.015
5- Testing Fixture	1				20
6- Installation on chamber	100	MD	SSC05	0.0045	

Notes: assume 500 pins/board
 Prepared E.J. Musser

sub. 203.2
 sub+cont. 231.648

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.5.2
 WBS Descript: Prod. Controller Board
 WBS QTY: 1920
 WBS UM: boards

	Risk	
	Factors	Weight %
Technical	4	8
Cost	4	4
Schedule	2	2

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

136

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- 16x3 cm 4 layer flexible Kapton pc boards	14300	square in			0.002
				1	
3- bid pkg	30	MD	IUENG1	0.0045	
1- Design/Layout	120	MD	IUENG1	0.0045	0.01
5- Stuff with Controllers/regulators/fiber connectors & test	1920	boards			0.006
5- Testing Fixture	1				20
6- Installation on chamber	100	MD	SSC05	0.0045	

Notes: assume 200 pins/board
 Prepared B.J. Musser

sub. 128.82
 sub+cont. 146.8548

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.5.3
 WBS Descript: Prod. MCMs
 WBS QTY: 25000
 WBS UM: chips

	Risk	
	Factors	Weight %
Technical	6	12
Cost	6	6
Schedule	4	4

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

137

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- 2.5x1.5 cm Multi-Chip Module	94000	square cm			0.012
				1	
3- bid pkg	30	MD	ORN1	0.0045	
1- Design	120	MD	ORN1	0.0045	
4- Test/Qualification	25000	chips			0.009
4- Test Fixture	1				10

Notes:
Prepared E.J. Musser

sub. 1456.825
sub+cont. 1777.3265

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.3.5.7.1
 WBS Descript: Prod. Receiver Board
 WBS QTY: 3125
 WBS UM: channels

	Risk	
	Factors	Weight %
Technical	4	8
Cost	4	4
Schedule	2	2

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

138

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- 32 channel on 9U/400mm VME	100	boards			2.8
6- Installation	60	MD	SSC05	0.0045	
3- I/A	30	MD	SSC05	0.0045	

Notes: Assume E/D costs shared by all subsystems, and included in unit cost
 Prepared E.J. Musser

sub. 293.365
 sub+cont. 334.4361

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.3.7.2
 WBS Descript: Prod. Fiber Data Links
 WBS QTY: 3125
 WBS UM: links

	Risk	
	Factors	Weight %
Technical	6	12
Cost	3	3
Schedule	4	4

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

139

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- LED driver/LED/80 m multimode cable	3125	links			0.143
3- bid pkg	30	MD	IUENG1	0.0045	
1- design	120	MD	IUENG2	0.0045	0.01
3- testing	3125	links			0.01
6- installation	1	MY	SSC05	1	

Notes: Prepared E.J. Musser

sub. 555.795
sub+cont. 661.39605

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.3.7.4
 WBS Descript: Prod. Clock/Trigger Links
 WBS QTY: 160
 WBS UM: links

	Risk	
	Factors	Weight %
Technical	6	12
Cost	3	3
Schedule	4	4

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

141

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- Reciever/80 m multimode cable - clock/trigger links	160	links			0.143
1- design	120	MD	IUENG1	0.0045	
3- testing	160	links			
6- installation	100	MD	SSC05	0.0045	

Notes: 1 links per 2 chambers clock (trigger=missing clock)
 Prepared E.J. Musser

sub. 79.85
 sub+cont. 95.0215

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.3.7.5
 WBS Descript: Prod. Slow Control
 WBS QTY: 160
 WBS UM: links

	Risk	
	Factors	Weight %
Technical	6	12
Cost	3	3
Schedule	4	4

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

142

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- slow control cable - 12 conductor shielded twisted pair/w termin	1	km			7
4- slow control system	1				24
1- design	120	MD	IUENG1	0.0045	
3- testing	60	MD	IUTECH1	0.0045	
6- installation	60	MD	SSC05	0.0045	
1 slow control cable/superlayer					
slow control = VME crate + 380n0 computer + 12 VME slow control cards					

Prepared B.J. Musser

sub. 93.91
 sub+cont. 111.7529

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.1.2.2.2.4.1
 WBS Descript: prototype amplifier IC
 WBS QTY: _____
 WBS UM: _____

	Risk	
	Factors	Weight %
Technical	2	8
Cost	2	2
Schedule	8	8

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

143

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
1- Rad-Hard prototype 1 design	2	MY	BNL1	1	
4- 1/2 cost of 3 Harris fab runs (shared with SCA)	1				150
3- bid	20	MD	BNL1	0.0045	
3- testing	1	MY	BNL2	1	

Notes: run product - 3 4 inch wafers/ ICs tested and packaged
 Prepared B.J. Musser

sub. 558.51
 sub+cont. 659.0418

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.1.2.2.2.4.3
 WBS Descript: SCA Test Station
 WBS QTY: 1
 WBS UM: _____

	Risk	
	Factors	Weight %
Technical	2	4
Cost	4	4
Schedule	8	8

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

145

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product MY/UM	Mat'l Unit Cost
4- ASIC Test Station	1				50
3- bld	5	MD	ORNL1	0.0045	

Notes: run product - 3 4 inch wafers/ ICs tested and packaged
 Prepared B.J. Musser

sub. 53.1275
 sub+cont. 61.6279

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.2.7.2
 WBS Descript: prototype Data Link
 WBS QTY: 10
 WBS UM: link

	Risk	
	Factors	Weight %
Technical	4	8
Cost	4	4
Schedule	8	8

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

150

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- LED driver/LED/80 m cable	10	links			0.143
3- bid	10	MD	IUENG1	0.0045	
3- test	50	MD	IUENG2	0.0045	
1- design	50	MD	IUENG1	0.0045	

Notes: Prepared E.J. Musser

sub. 36.215
sub+cont. 43.458

**SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM**

Subsystem: Outer Tracker

Estimate Type BU

WBS. No: 50.2.2.2.7.1
 WBS Descript: prototype Reciever
 WBS QTY: 1
 WBS UM: board

	Risk	
	Factors	Weight %
Technical	4	8
Cost	4	4
Schedule	8	8

- Functional Activity:
1. Engineering/Design
 2. Materials & Services
 3. Inspection/Administration
 4. Procurement/Fabrication
 5. Assembly
 6. Installation

151

Item Description	QTY	Unit Meas (UM)	Craft/Team Resource Code	Unit Product. MY/UM	Mat'l Unit Cost
4- fab 1 Reciever prototype	1	board			3
3- bid	10	MD	IUENG1	0.0045	
3- test	30	MD	IUENG2	0.0045	
1- design	90	MD	IUENG1	0.0045	

Notes: sub. 46.335
 Prepared E.J. Musser sub+cont. 55.602

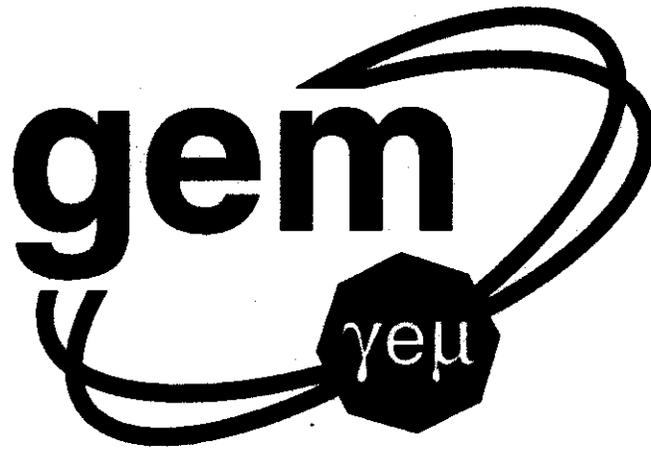
1	SSC05	33
2	SSC02	69
3	ORNL1	139
4	NL05	118
5	IUENG1	78
6	IUENG2	61
7	IUTECH1	44
8	BNL1	139
9	BNL2	118

- 10
- 11
- 12
- 13
- 14
- 15

152

1	33
1	33

Prod. Total		786
		7457.8022
ProductionTotal+Cont.	100 2	9693.051275
R&D Total		1764.4175
R&D Total + Cont.		2131.2705



Calorimeter Readout

John Parsons

GEM CAL Readout Boards

- Functions:
- receive differential CAL signals
 - apply bipolar shaping
 - sample shaped signals @ 60 MHz
 - digitize (either @ 60 MHz or at 100 kHz)

- After L1
- buffer relevant data
 - zero suppress?
 - choose gain scale
 - process samples (apply calib. constants, calc. E & T, ...)
 - format data for data-driven L2

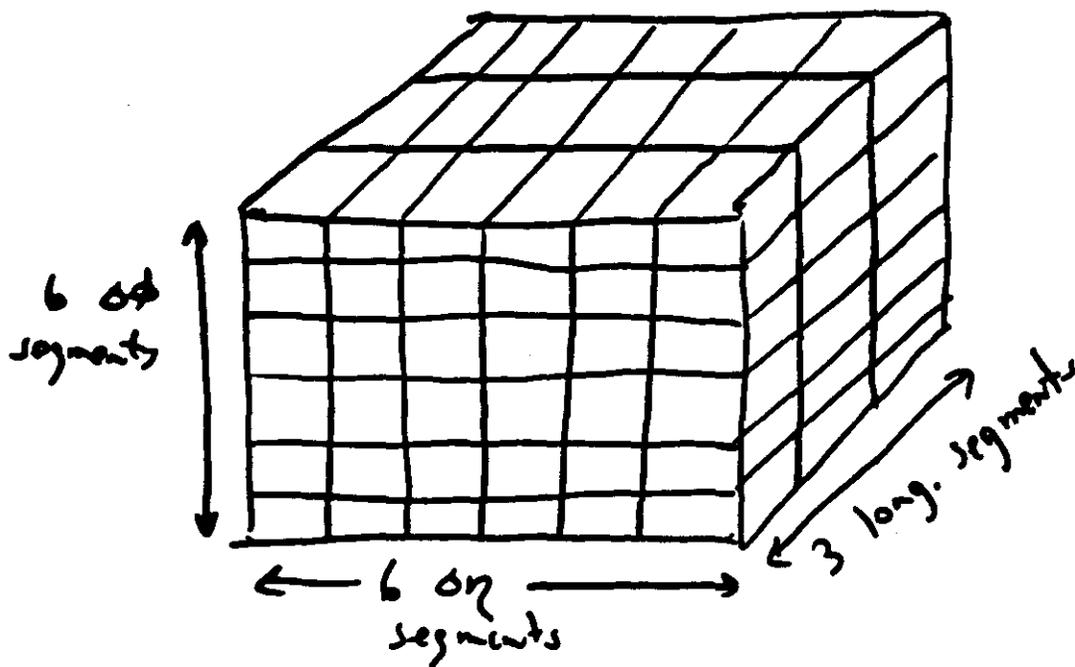
- Other Tasks
- calibration (eg. AMU, ADC)
 - DQM

- formation of L1 analog sums (or at least intermediate sums)



would like to "map" board onto trigger tower.

CAL EMC Trigger Tower



$$\Rightarrow 1 \text{ trigger tower} = 6 * 6 * 3 = \underline{108 \text{ channels}}$$

AMU Approach

→ maybe can get 54 chan/board = $\frac{1}{2}$ (trigger tower)

→ can no doubt get 36 chan/board = $\frac{1}{3}$ (" ")

All-Digital Approach

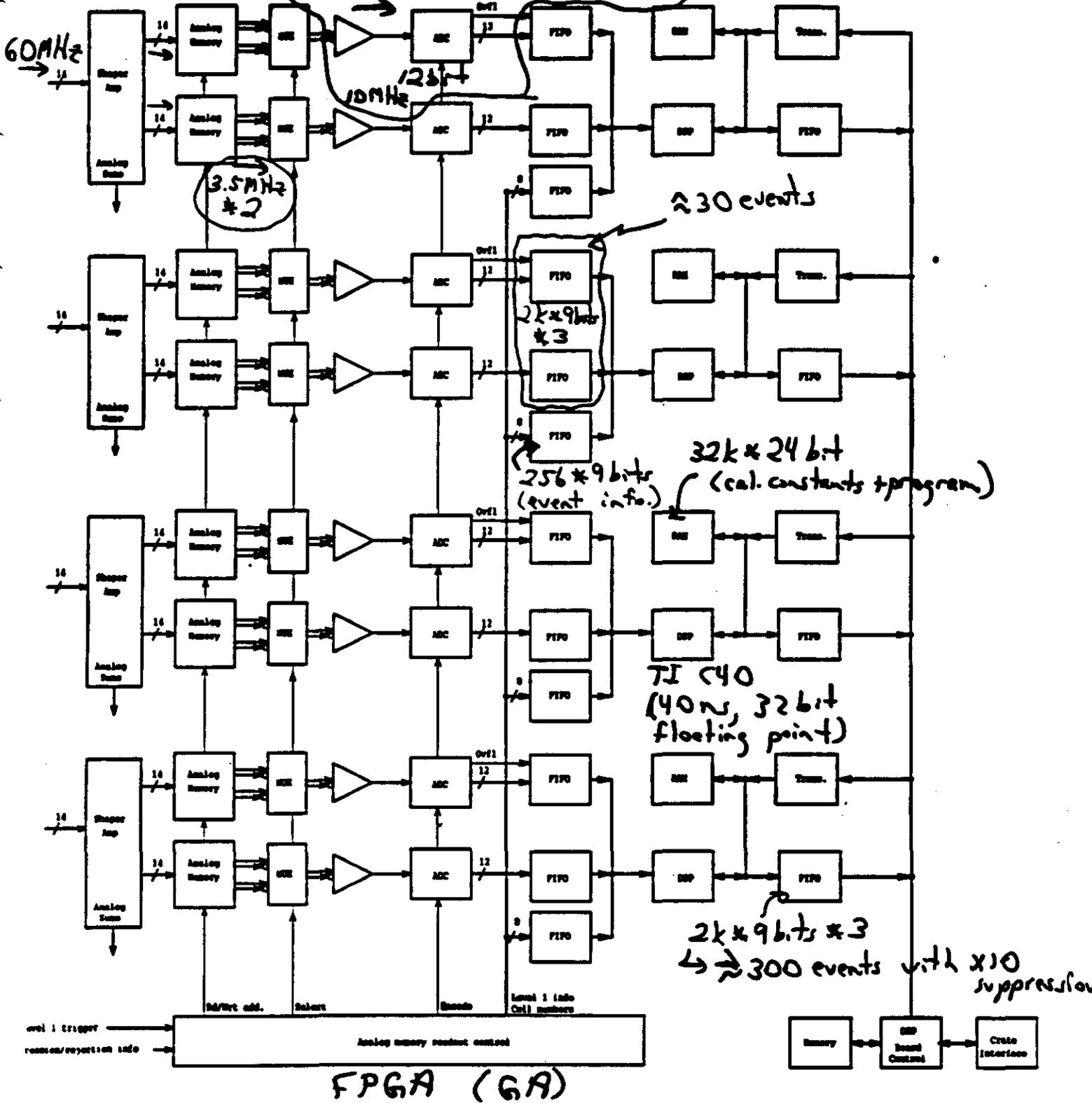
→ can get ≈ 10 chan/board (12 possible ??)

In any case, overlapping sums (which require "row" and "column" intermediate sums) are a headache!

54 Channel Module (2222 boards for 120k channels)

GEM Calorimeter Readout Card

$14 \times 5 \times 100k \text{ Samples} \rightarrow 7 \text{ MHz}$

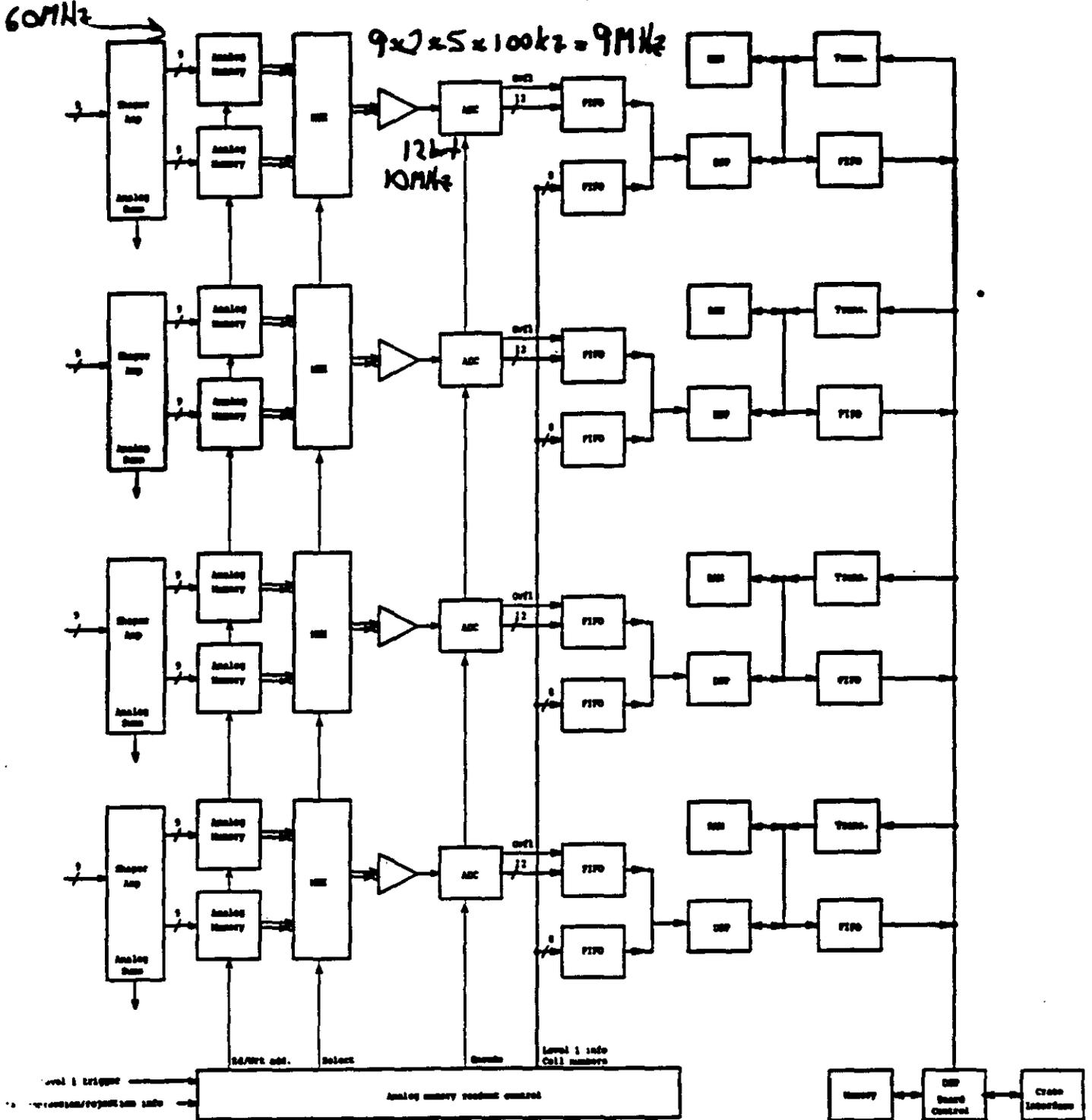


08L704 12/2/90

36 Channel Module

(3333 boards for 120k channels)

GEM Calorimeter Readout Card



GEM/PS 12/11/90

FIRST LOOK AT COST, POWER

FOR 50 CHANNEL MODULE

GEM CALORIMETER READOUT CARD - COST/POWER ESTIMATE

14-DEC-92

ITEM #	DESCRIPTION	PART NO.	POWER RATING W	POWER DENSITY W/CM ²	PACKAGE/FORM	AREA CM ²	QTY PER STRIP	# CHANNELS PER STRIP	TOTAL # STRIPS	UNIT COST	TOTAL COST
1	RAM - 512KB - CMOS - 35N. CLOCK TIME	SDT71856L89Y	15/185mA	13.5	SOJ/0.9"X0.8"	3.2	20	25	500	2.60	140.00
2	FIFO - 2KR9 - CMOS - 45N5 CLOCK TIME	SDT72291L89Y	15/85mA	4.5	PLCC/0.5"X0.6"	3.6	12	32	384	12.60	151.20
3	DSP - 40MHZ -	TMS320C406R10	16/350mA	8.75	PGA/1.8"X1.8"	3.5	5	325	1625	252.00	1250.00
4	ADC - 12BIT/10KHZ	SPT8910SCT	2.5/150mA 2.5/150mA	0.8 0.8	SOJ/0.8"X1.6"	9.7	8	32	256	95.00	600.00
5	MUX - 6CHNL DATA - CMOS - BANK .01%	MS3-0518-5	2.5/150mA 2.5/150mA	0.8 0.8	DIP/0.6"X1.45"	14.00	16	25	400	4.00	250.00
6	OUTPUT FIF - 1KR9 - CMOS - 45N5 CLOCK	SDT7221L95Y	15/85mA	1.5	PLCC/0.5"X0.6"	1.2	4	82	128	12.00	50.40
7	ANU - 150 CHNL X 10CHNL - 0.5% BLY	5N/25K-1.0N-WELL	2.5/12.8mA 2.5/12.8mA	1.0 0.42	PLCC/0.8"X0.7"	8.84	16	65	1056	23.80	352.00
8	ANU - CONTROL - CMOS LOGIC/MEM	MEMOKEY LOGIC	2.5/100mA 2.5/100mA	1.0 0.5	SOJ/0.8"X0.7" SOJ/0.8"X0.7"	6.82 1.2	3 10	25 16	38 160	4.80	14.00
9	CMOS MICROPROCESSOR LOGIC	LOGIC	2.5/120mA	5.0	SOJ/0.5"X0.3"	1.5	10	20	200	1.00	20.00
10	CONNECTORS 3 - 54 PIN, 1 - 40 PIN 4 - 26 PIN	---	---	---	1.8/0.22/0.66	7.8	7	12+14+10	336	2.50	17.50
11	SWITCHES OF, PLS, MISC.	---	---	---	0.7"X0.1"	2.4	120	2	240	0.05	12.00
12	P.C. BOARD (9U) 15.75" X 0.8" QUARTZ	---	---	---	15.95"X0"	159.5	1	---	1209	5.000	320.00
13	ASSEMBLY	---	---	---	---	---	1	---	---	4.10	4.10
14	SIMPLEX AMP'L	---	2.5/150mA 2.5/150mA	?	70.5"X0.5"	13.06	52K	14	728	?	?
14A	ADC OUTPUT LEVEL SHIFTER	MC16125	2.5/150mA 2.5/150mA	4.2	SOJ/0.5"X0.3"	1.15	24	16	384	1.00	27.00

Not included

\$5075.90

TOTAL POWER (EXCLUDING SIMPLEX AMP'L) = 68.0 W

POWER DENSITY = $\frac{68.0}{15.95 \times 10 \times 0.6} = 0.93 \text{ W/CM}^2$ ASSUMING 0.6" CAPD PITCH

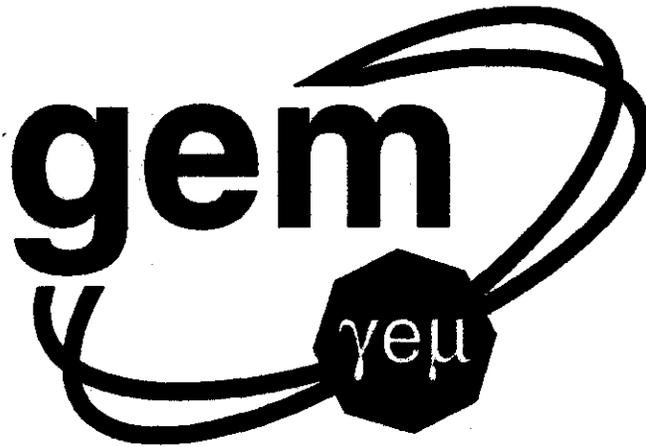
ASSUMING 24 CARDS / CRATE - POWER / CRATE = 1.65 KW EXCLUDING OTHER CABLE MODULES & SIMPLEX AMP'L (100 CARDS)

COMPONENT TOTAL AREA = 66.21 CM²

TOTAL COST EXCLUDING SIMPLEX AMP'L = \$5075.90 OR \$63.00 / CHANNEL (52 CHANNELS / CRATE)

Power \approx 1.5 W/channel, Cost \approx \$70-100/channel

161



Calorimeter Preamps & Drivers

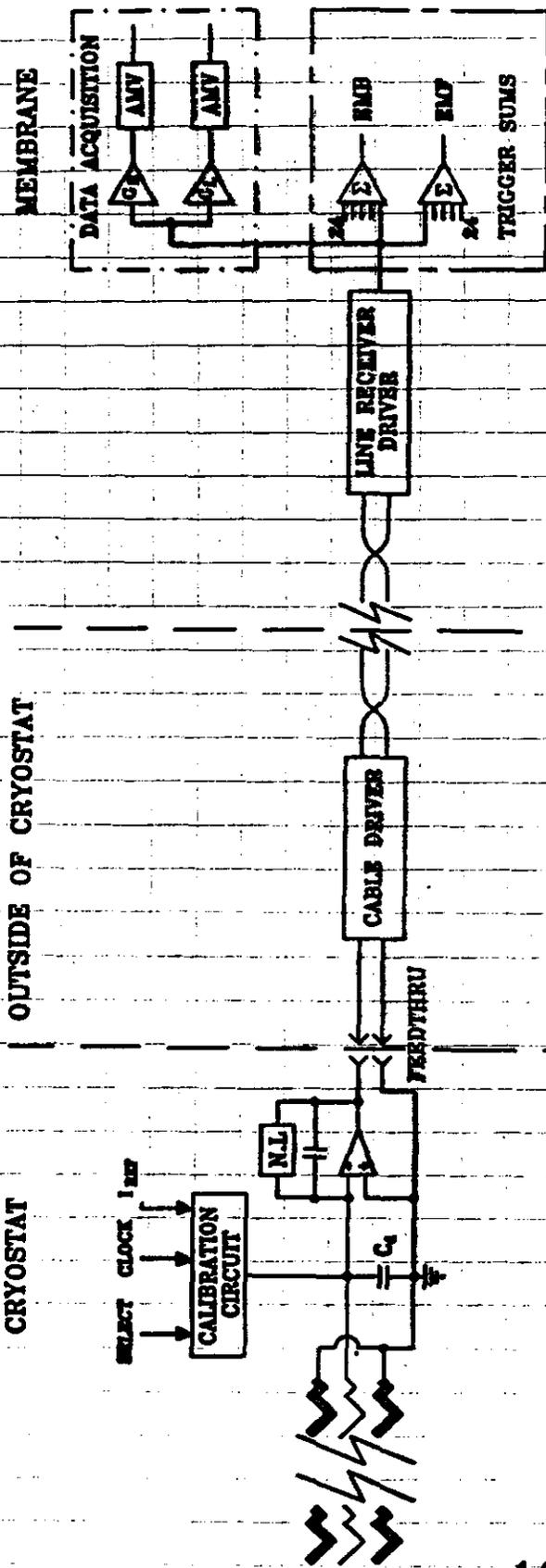
Sergio Rescia

AIM: Design of a charge sensitive preamplifier for Liquid Argon preamplifier for cryogenic ionization chamber calorimeters (Liquid Argon, Krypton) at hadron collider experiments (SSC, LHC).

ENVIRONMENT T=90 K
(10 years of operation) Neutron Flux: 10^{14} N/cm²
Dose: 30 Mrad

SPECIFICATIONS Low Noise (trigger sums)
 $C_D=100$ pF-1 nF
 $t_p=15-50$ ns
High g_m , g_m/C_{iss} , g_m/I_{DSS}
 $C_D/10 < C_{iss} < C_D/2$
 $W=10^4$ μ m (1 cm)

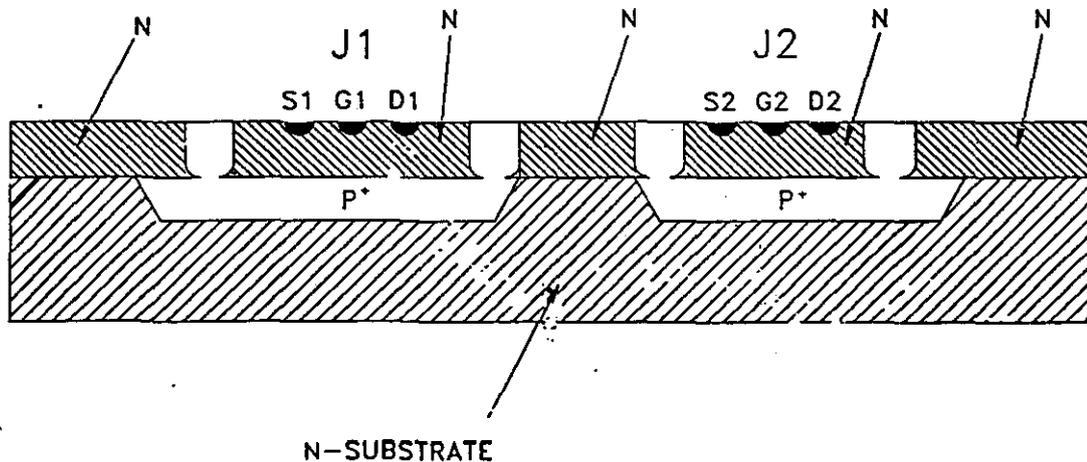
TECHNOLOGY Epitaxial-channel JFETs meet all these requirements and are manufactured with a mature, well-proven technology. Hybrid preamplifiers using discrete JFETs have been built and successfully operated up to three years. To achieve monolithic integration interdevice isolation must be obtained *while preserving the characteristic of discrete JFETs.*

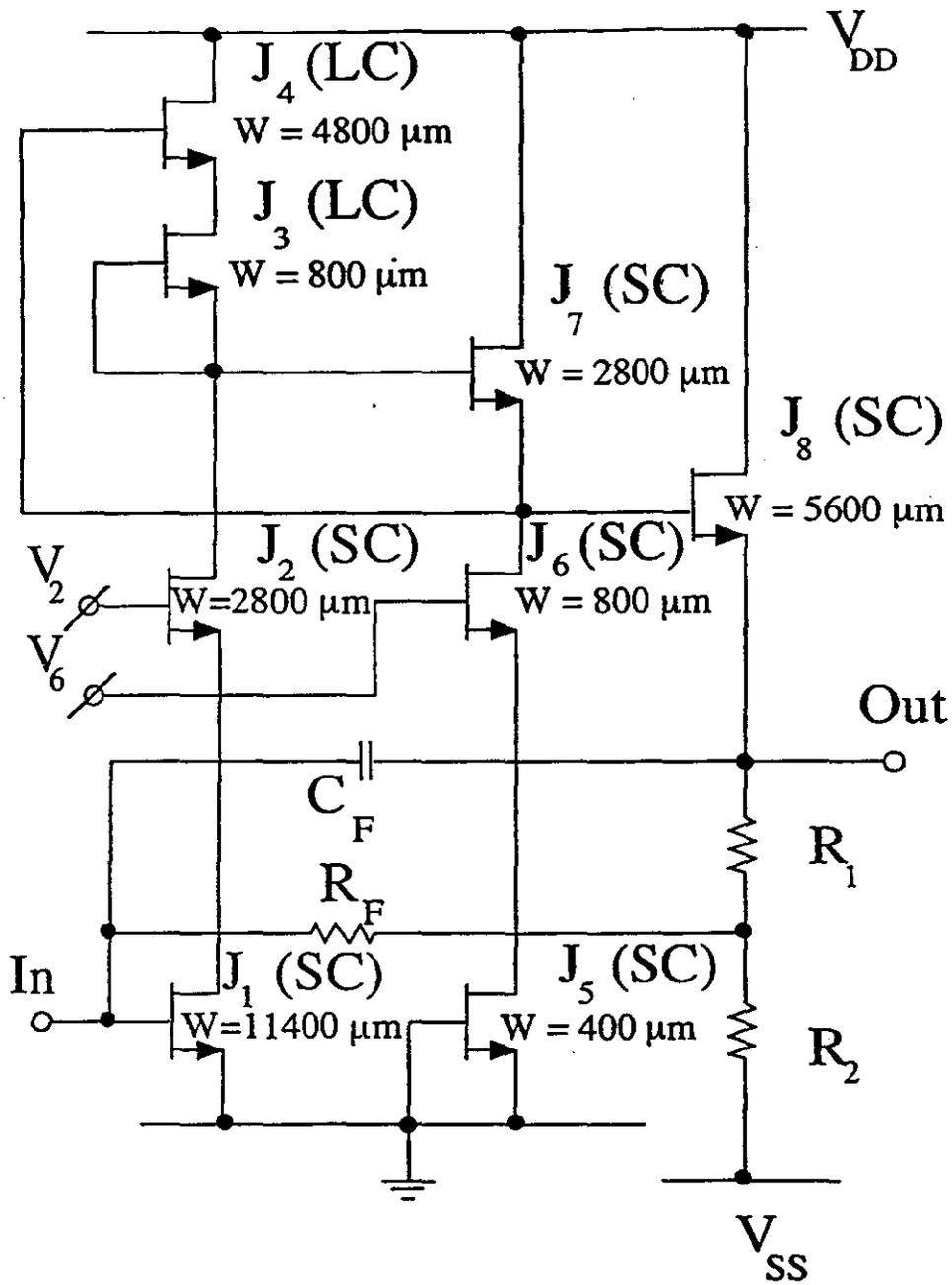


BURIED LAYER TECHNOLOGY

To achieve interdevice insulation a junction-insulated technology based on a diffused P⁺-type buried layer which acts as a back gate has been developed. It uses an epi channel and diffused gate, source and drain to achieve an optimum noise performance.

- $\rho_{\text{subs}}=0.5 \Omega\text{cm}$
- $\rho_{\text{buried}}=0.002 \Omega\text{cm}$
- $\rho_{\text{epi}}=0.5-2 \Omega \text{ cm}$
- $t_{\text{epi}}=4-7 \mu\text{m}$
- isolation ring doping: $>10^{18} \text{ cm}^{-3}$ at the surface to prevent surface inversion





P	FEATURES	I_d [mA]	$Z_m \left[\frac{\text{mA}}{\text{V}} \right]$	$\text{SW}_e \left[\frac{\text{nV}}{\sqrt{\text{Hz}}} \right]$	$\text{SW}_t \left[\frac{\text{nV}}{\sqrt{\text{Hz}}} \right]$	$\frac{\text{SW}_e}{\text{SW}_t}$	GBW [MHz]
1	TEST PADS ADDED (ceramic carrier)	9.2	48.3	0.57	0.49	1.16	200
2	TEST PADS ADDED (ceramic carrier)	1.9	22	0.76	0.72	1.05	112
3	TEST PADS ADDED (ceramic carrier)	2	23	0.75	0.70	1.07	127
4	NO TEST PADS (TO-78)	3	26	0.73	0.68	1.07	194
5	TEST PADS ADDED (ceramic carrier)	4	32	0.66	0.60	1.10	136
6	NO TEST PADS (TO-78)	5	31	0.68	0.61	1.11	200

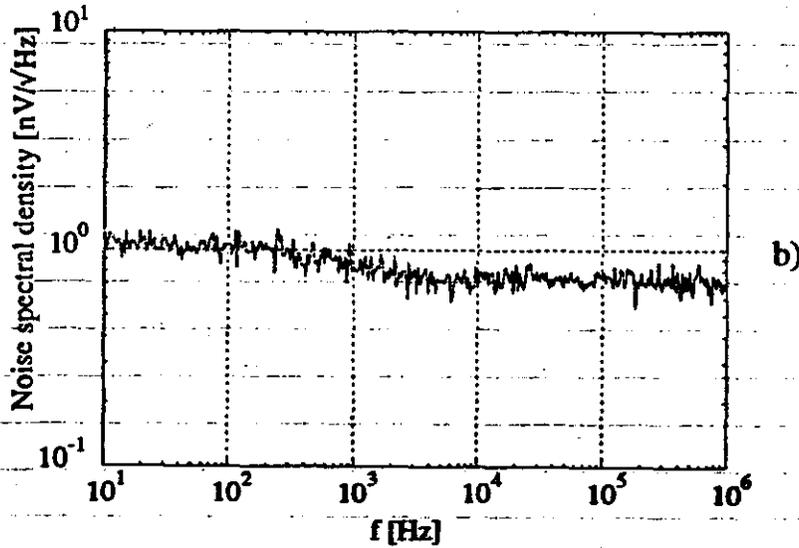
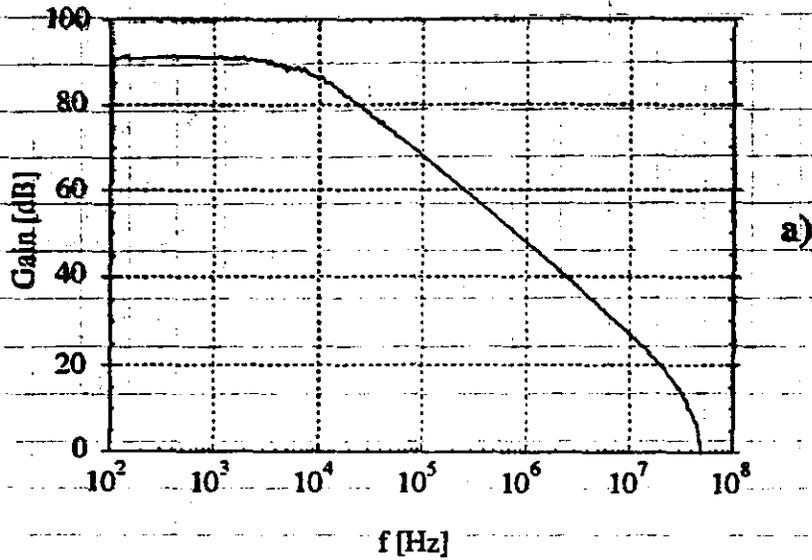
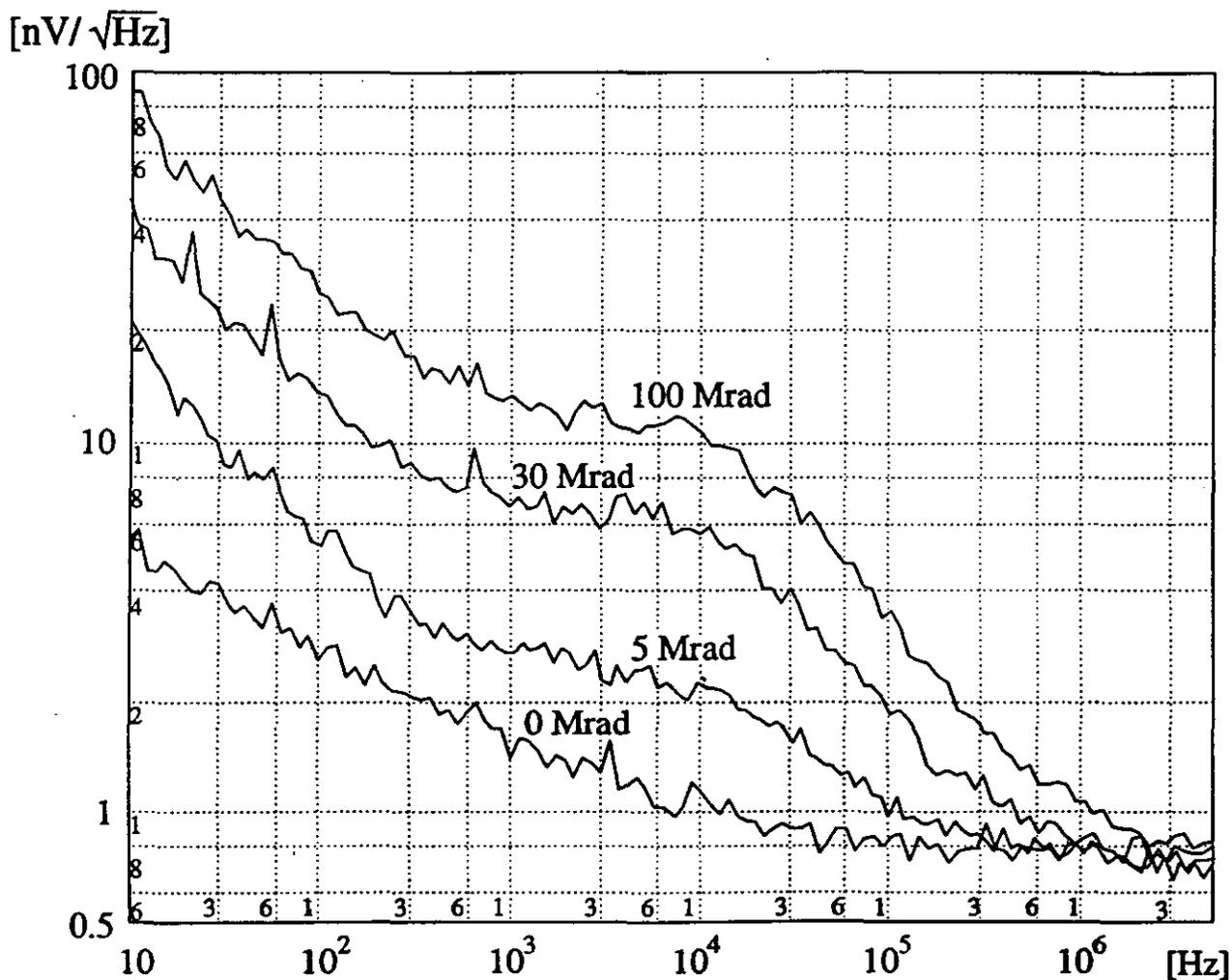


Fig. 2 - Characteristics of the preamplifier labelled 4 in Table I.
 (a) Open-loop gain-frequency dependence.
 (b) Spectral density of the noise voltage referred to the preamplifier input as a function of frequency.

JFET RADIATION EFFECTS

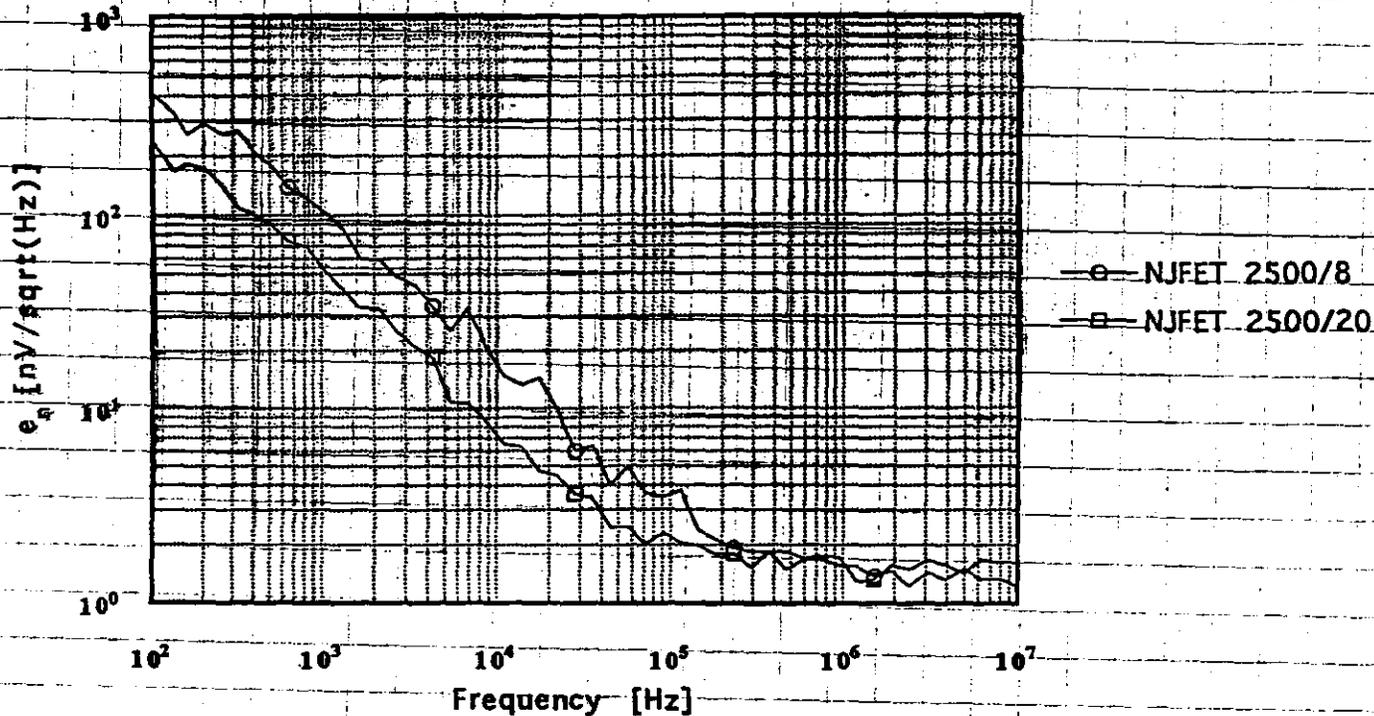
(^{60}Co)

NOISE SPECTRUM

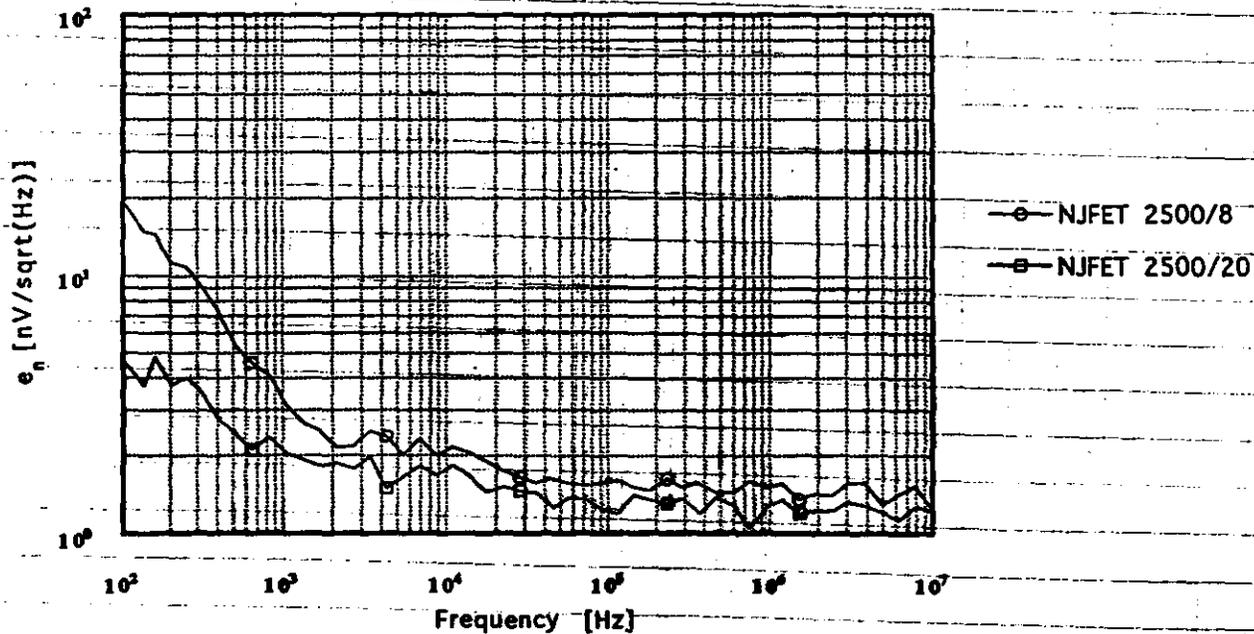


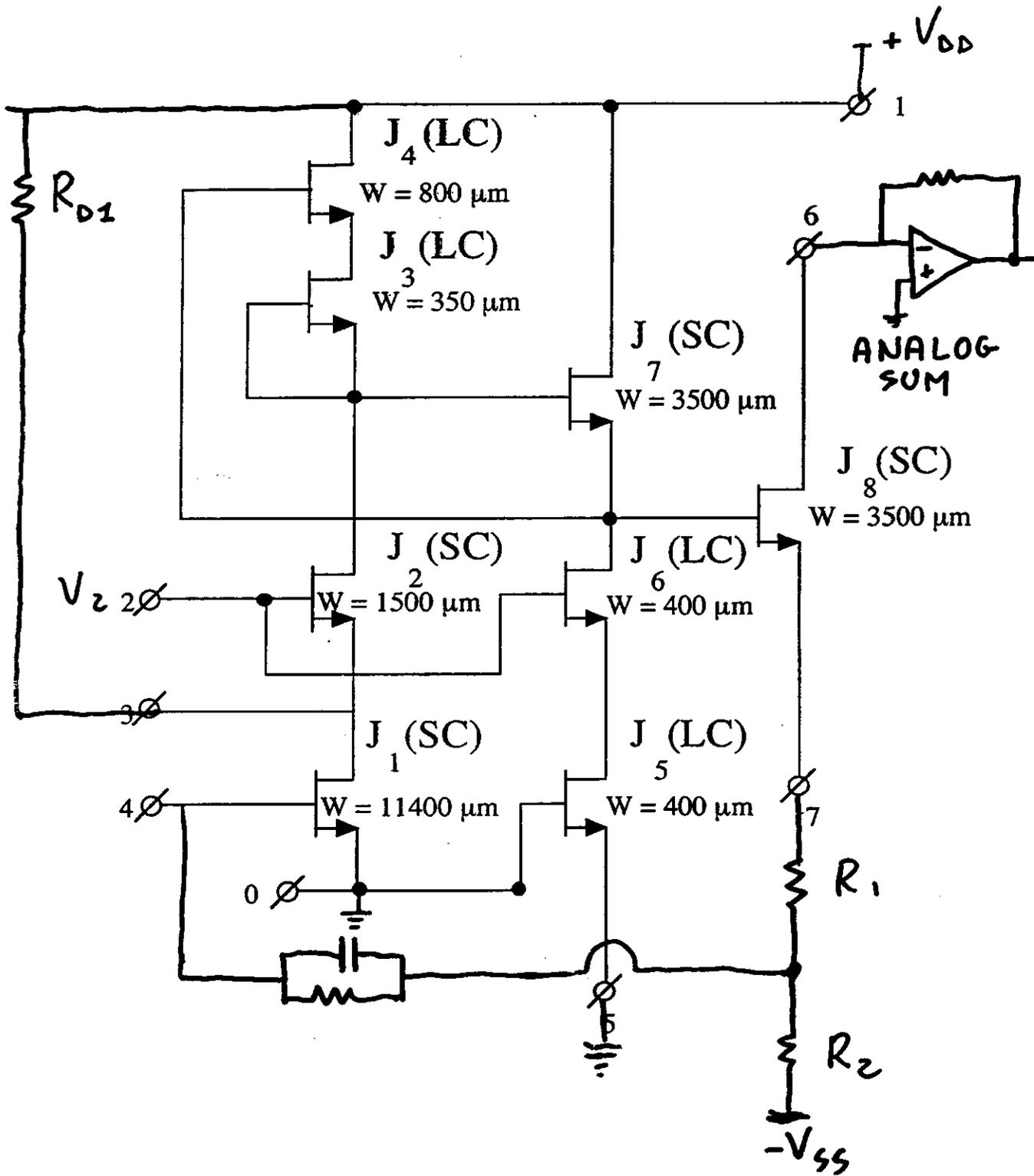
SHORT CHANNEL JFETs : NOISE

Noise Spectra - Room Temperature

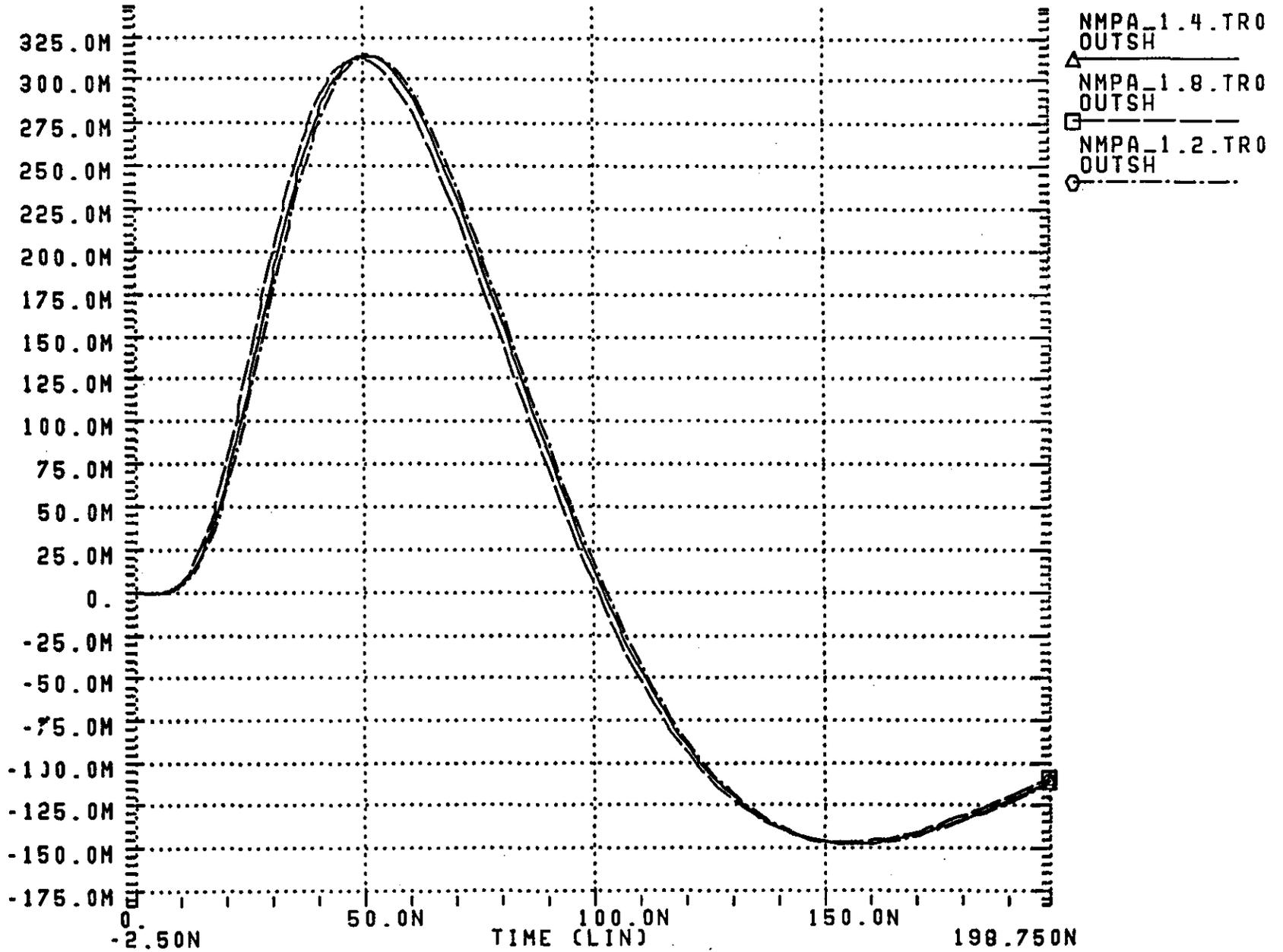


Noise spectra - Liquid Argon temperature





**NEW MON PA . 40NS SHAPER --- VTO--1.2V
7-JUL92 15:45:37

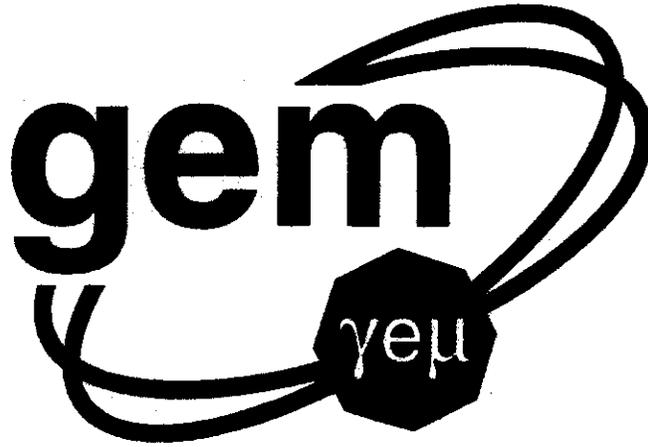


175

VOLT IN

TIME (LIN)

198.750N



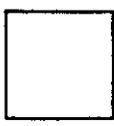
Level 1 Cal Trigger

Bill Cleland

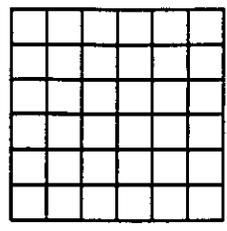
EM cell
(.027x.027)



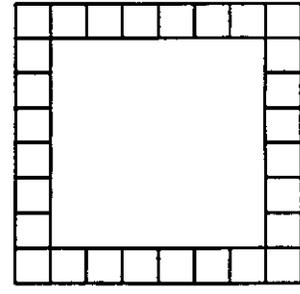
HAD cell
(.08x.08)



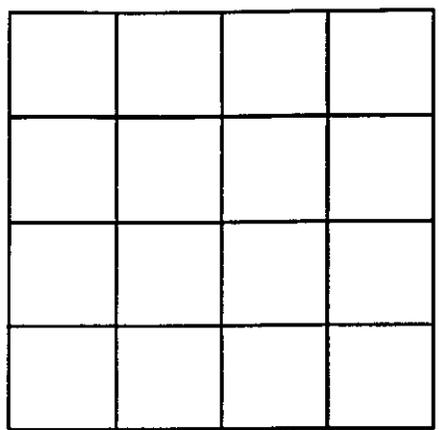
EMF=6x6 EM
(.16 x .16)



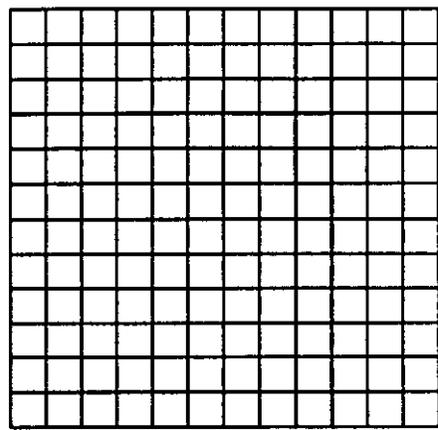
EMB (border)
(.21 x .21)



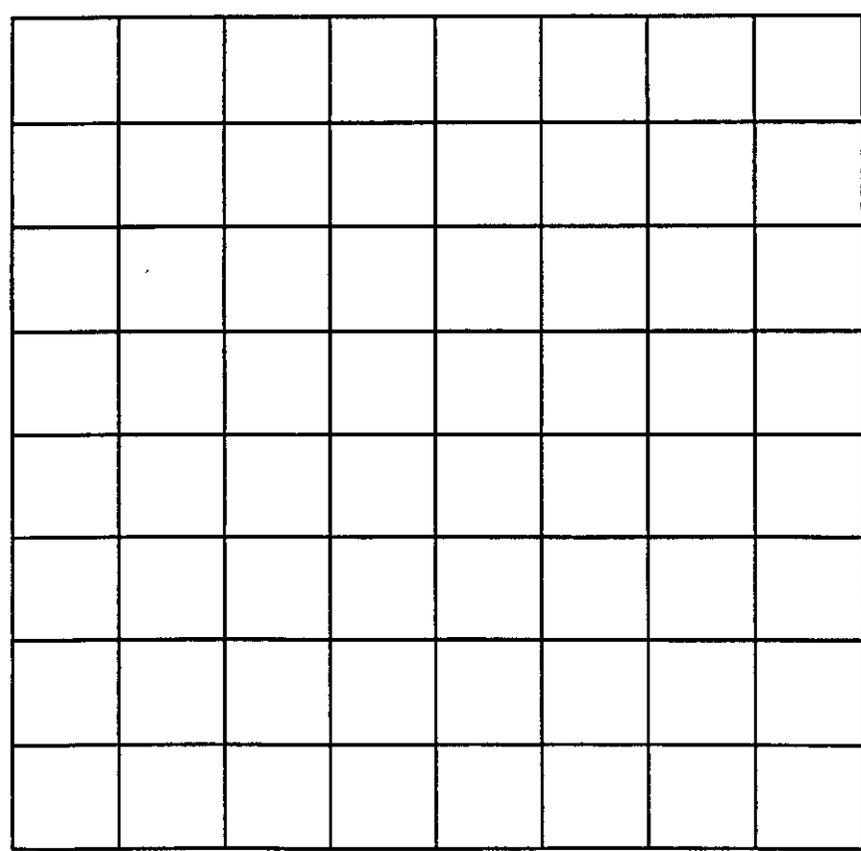
SP = 4x4 HAD
(.32 x .32)



SPEM = 2x2 EMF
(.32 x .32)

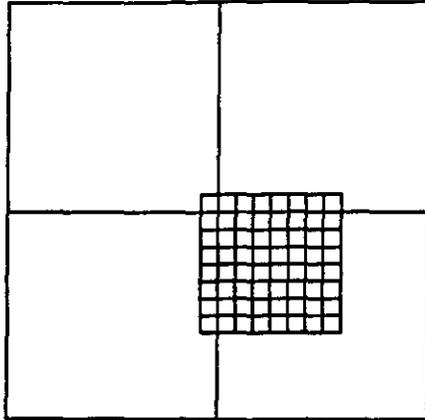


JET = 2x2 SP
(.64 x .64)

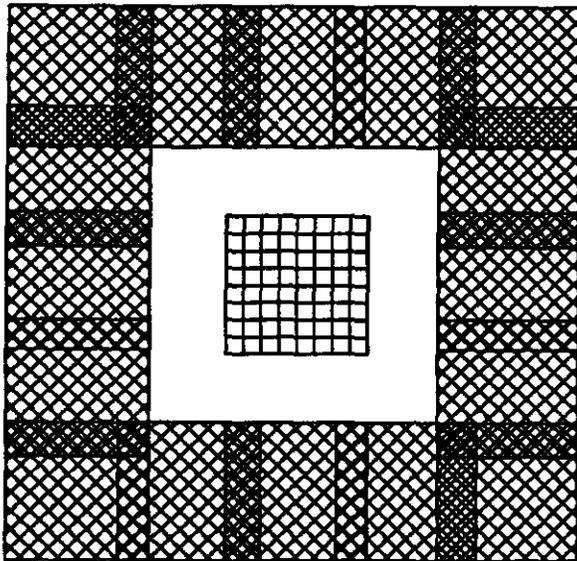


GEM Isolated Gamma Trigger

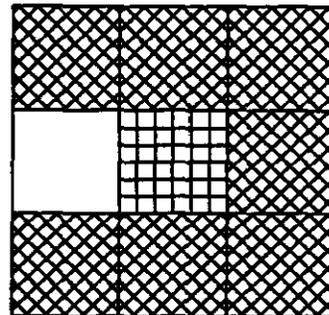
EM with hadronic veto
(Level 1)

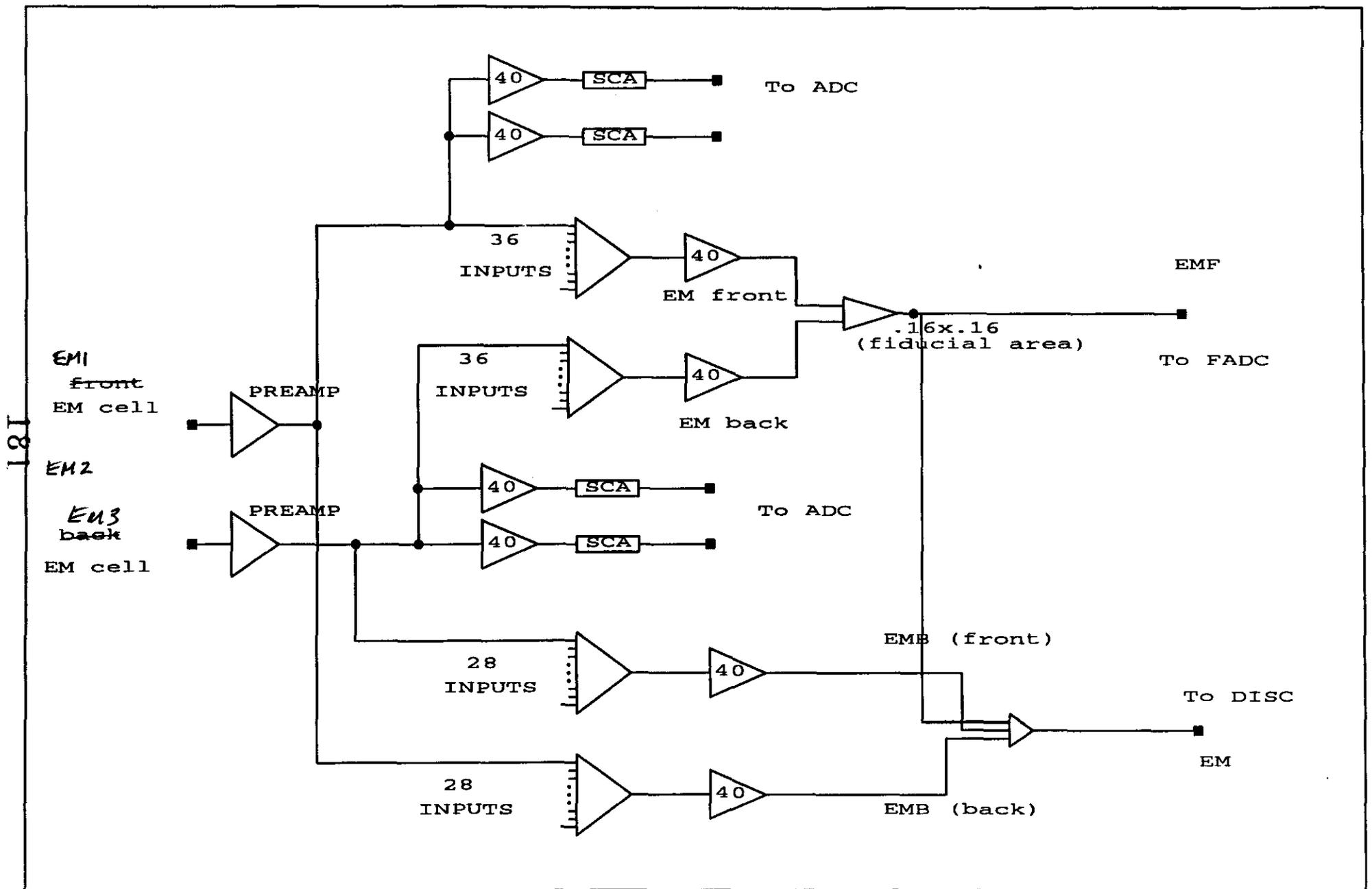


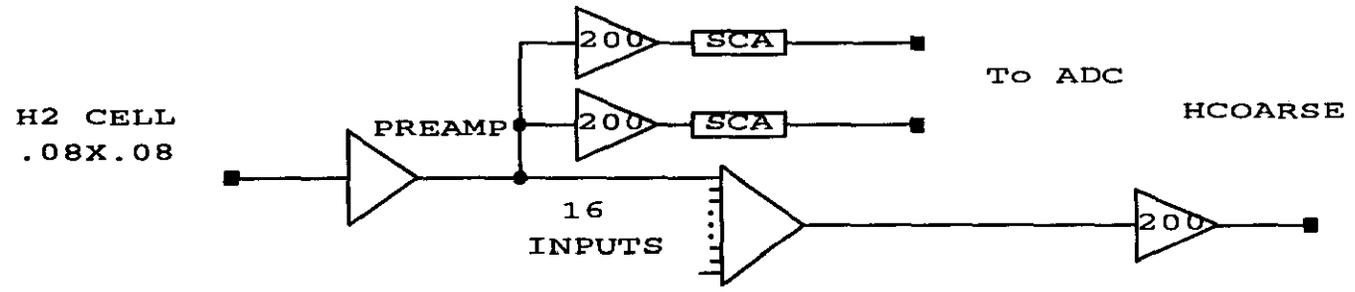
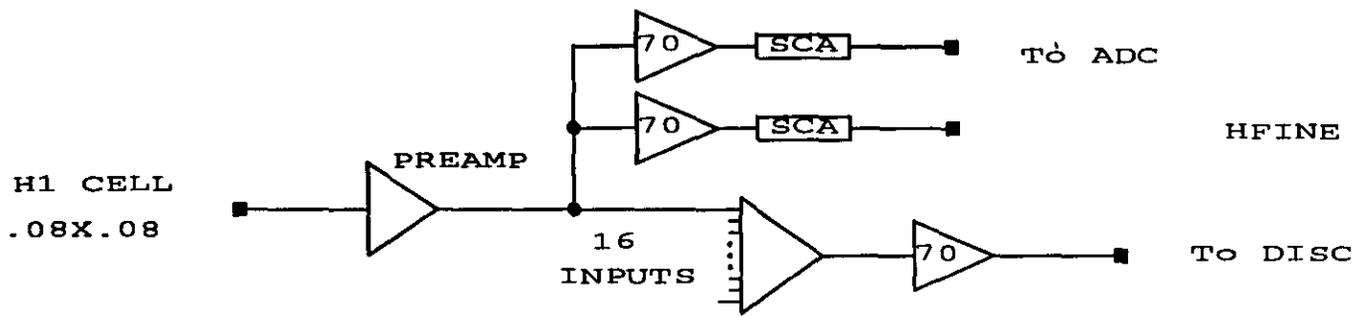
EM with EM veto
(Level 1)



EMF with EMF veto
(Level 2a)

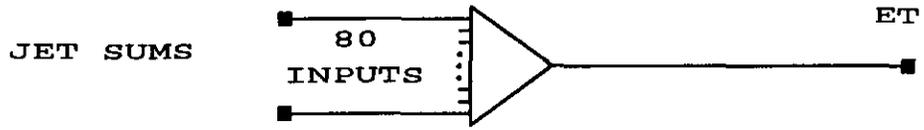
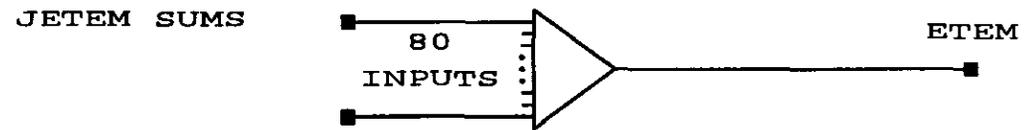
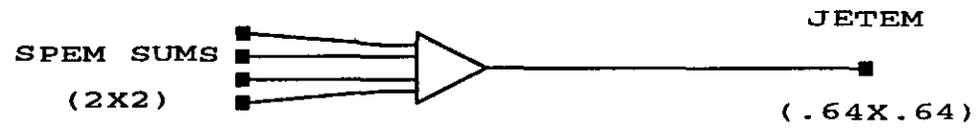
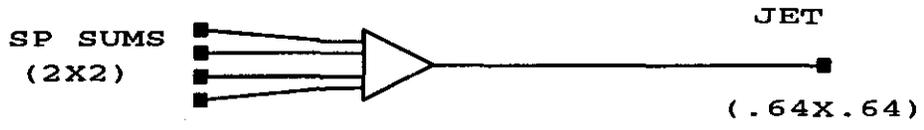
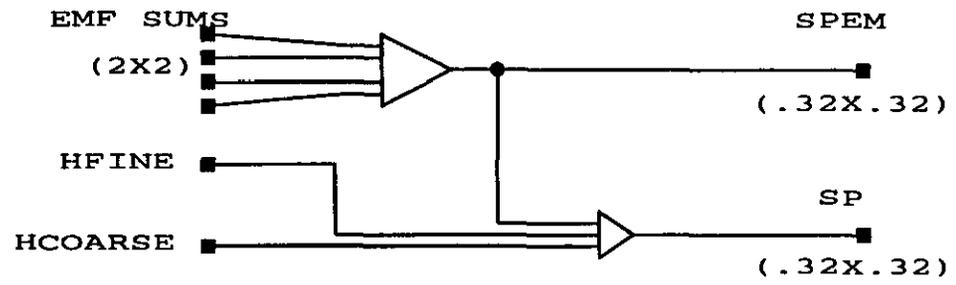






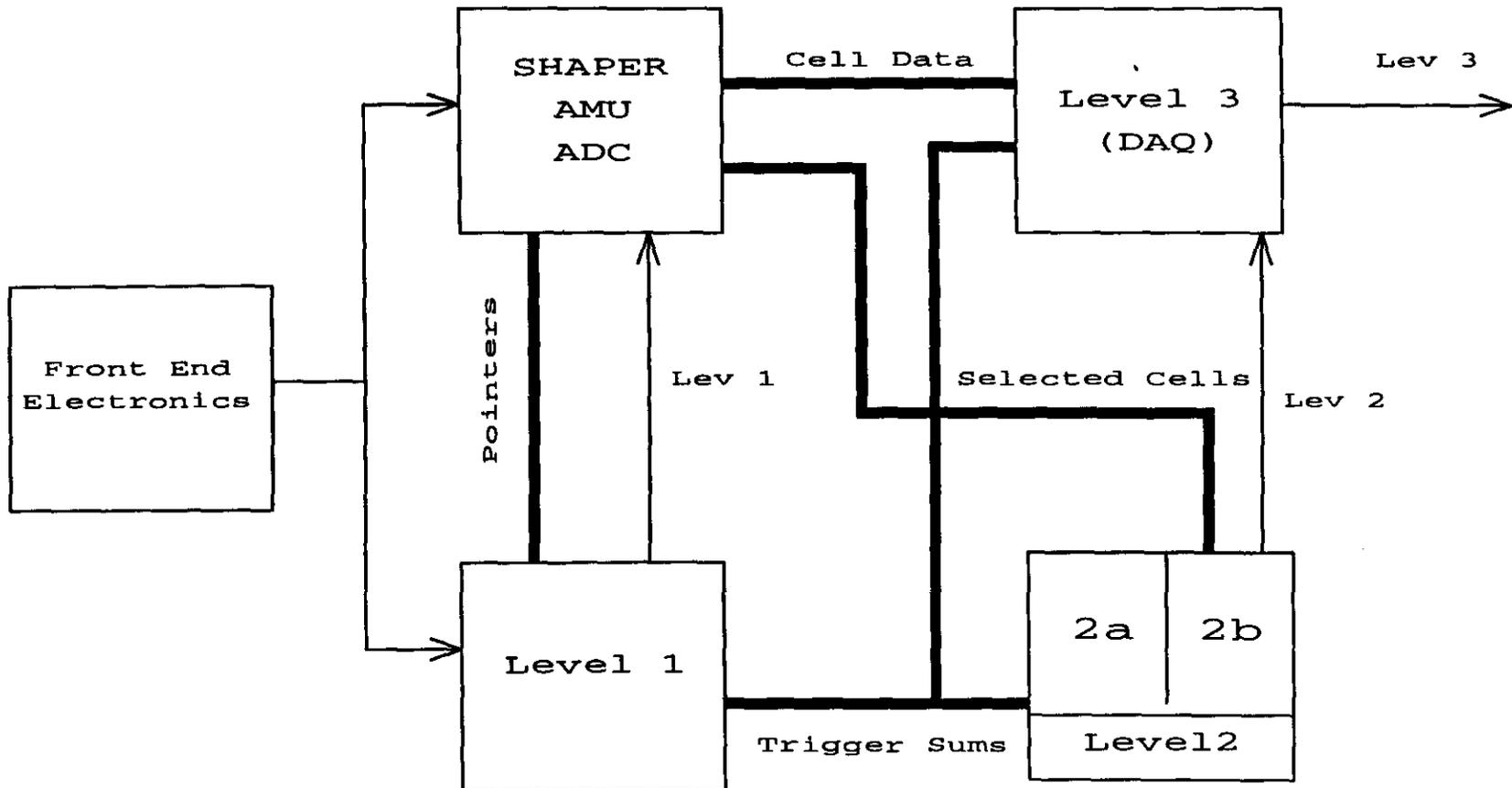
182

4

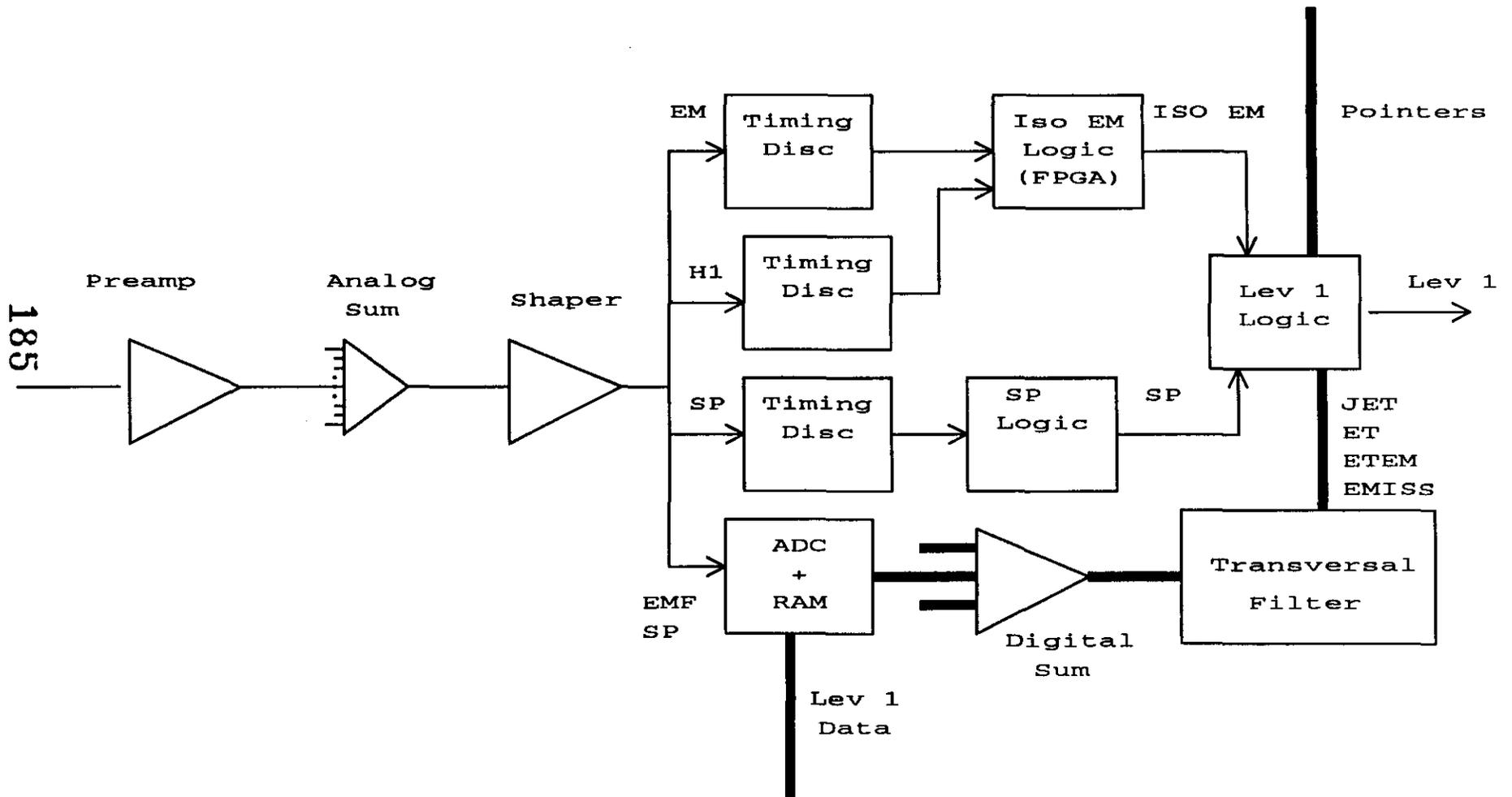


CALORIMETER TRIGGER

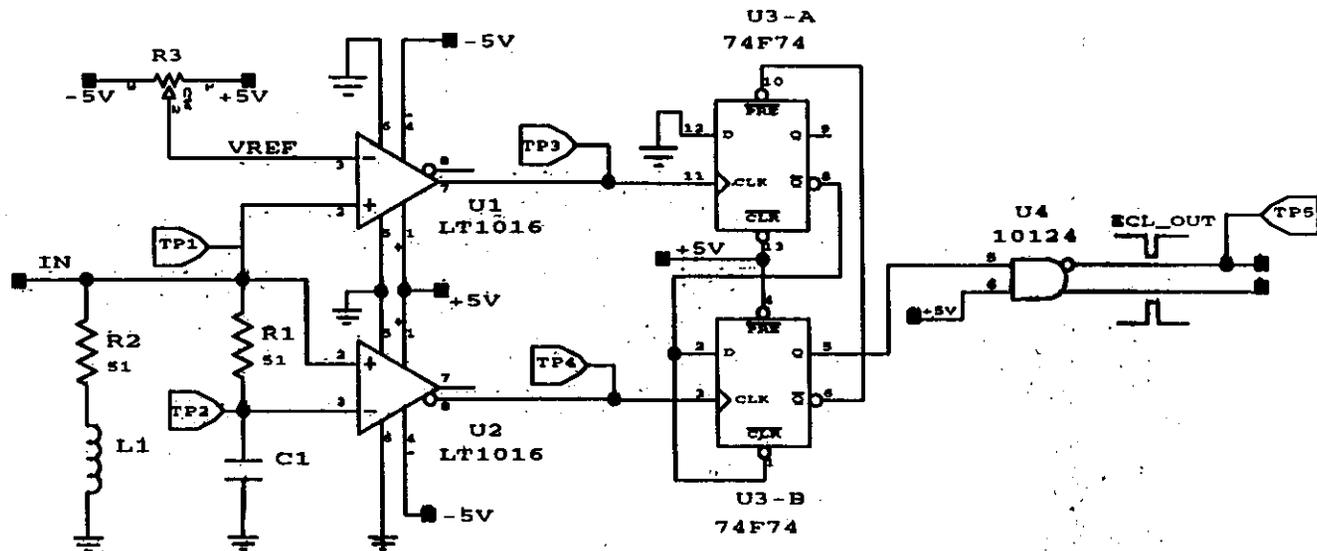
184



LEVEL 1 CALORIMETER TRIGGER



Timing Discriminator



Status: Tested in beam in 7/92

Multi level version under development

Expect ≥ 48 channels (FB-signal module), 6-8 levels/channel

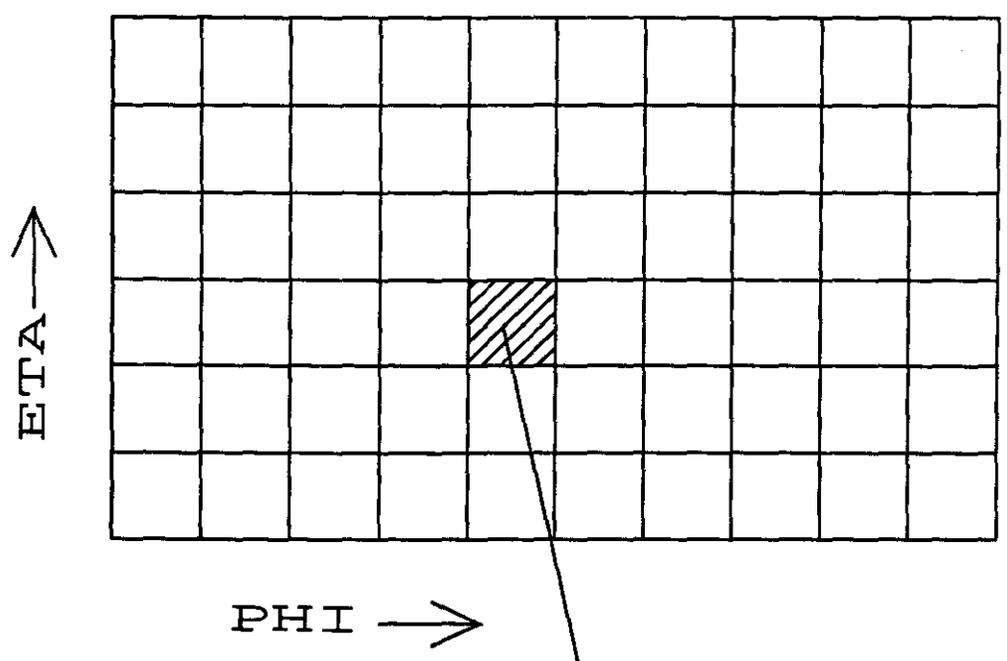
No. channels required (beam only)

EM: 960

H1 160

SP 160

EM ISOLATION LOGIC



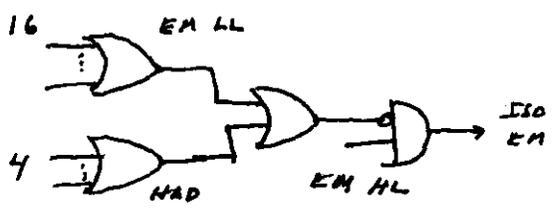
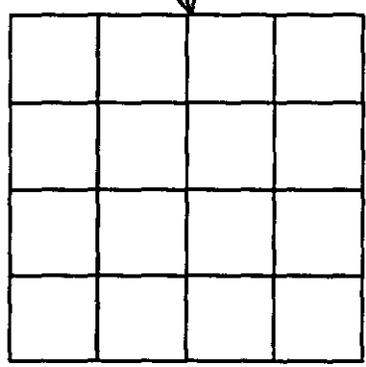
Logic Module

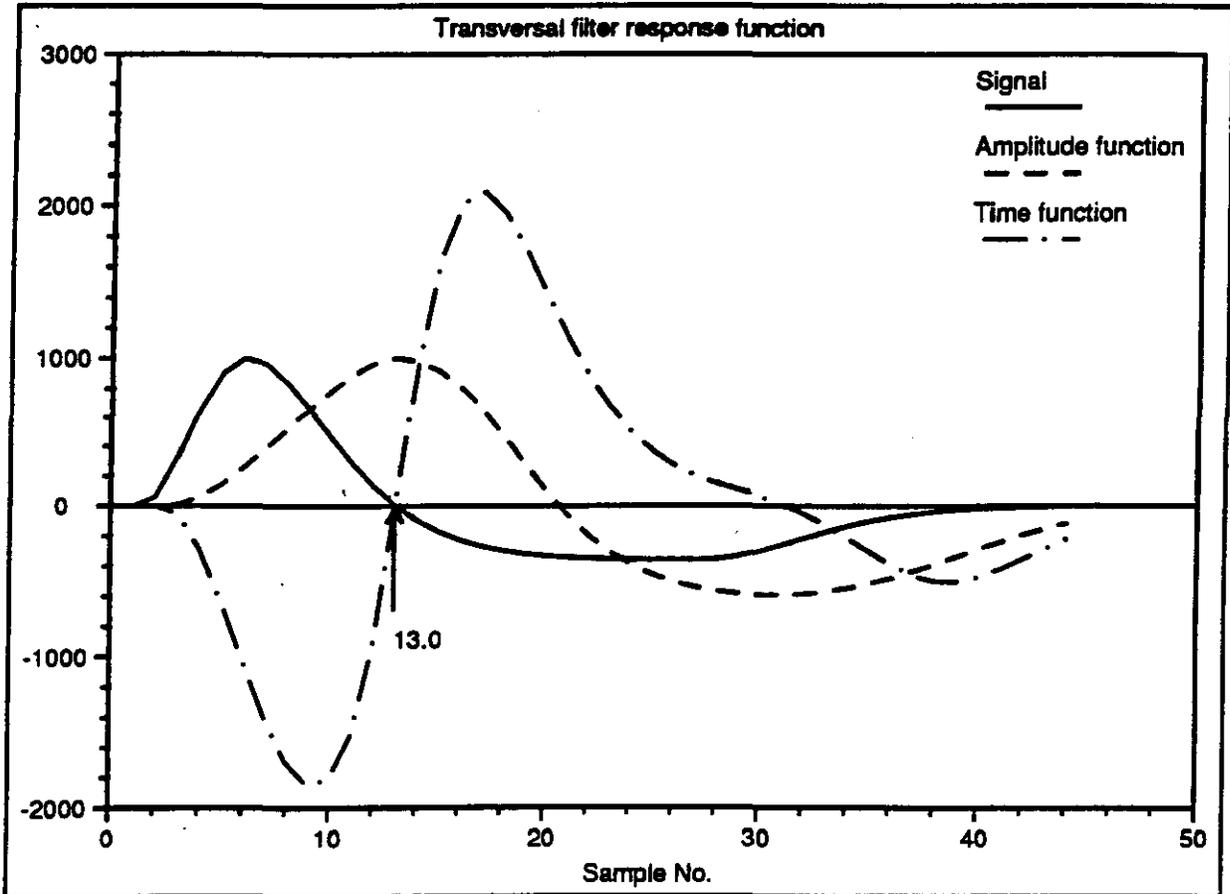
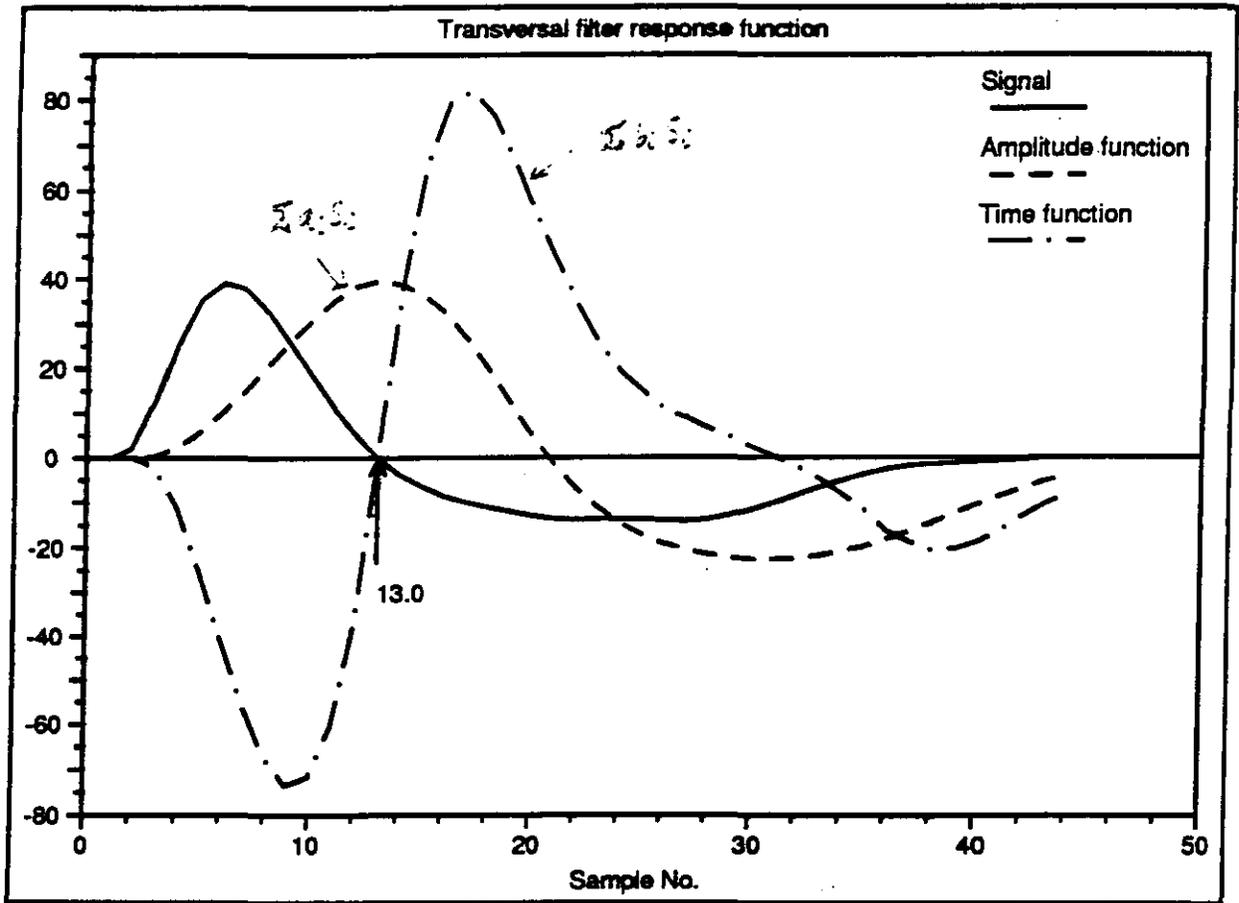
Inputs

- 16 HL EM
- 64 LL EM
- 16 LL HAD

Outputs

- 16 ISO EM





188
Fig 1.7

TRANSVERSAL FILTER

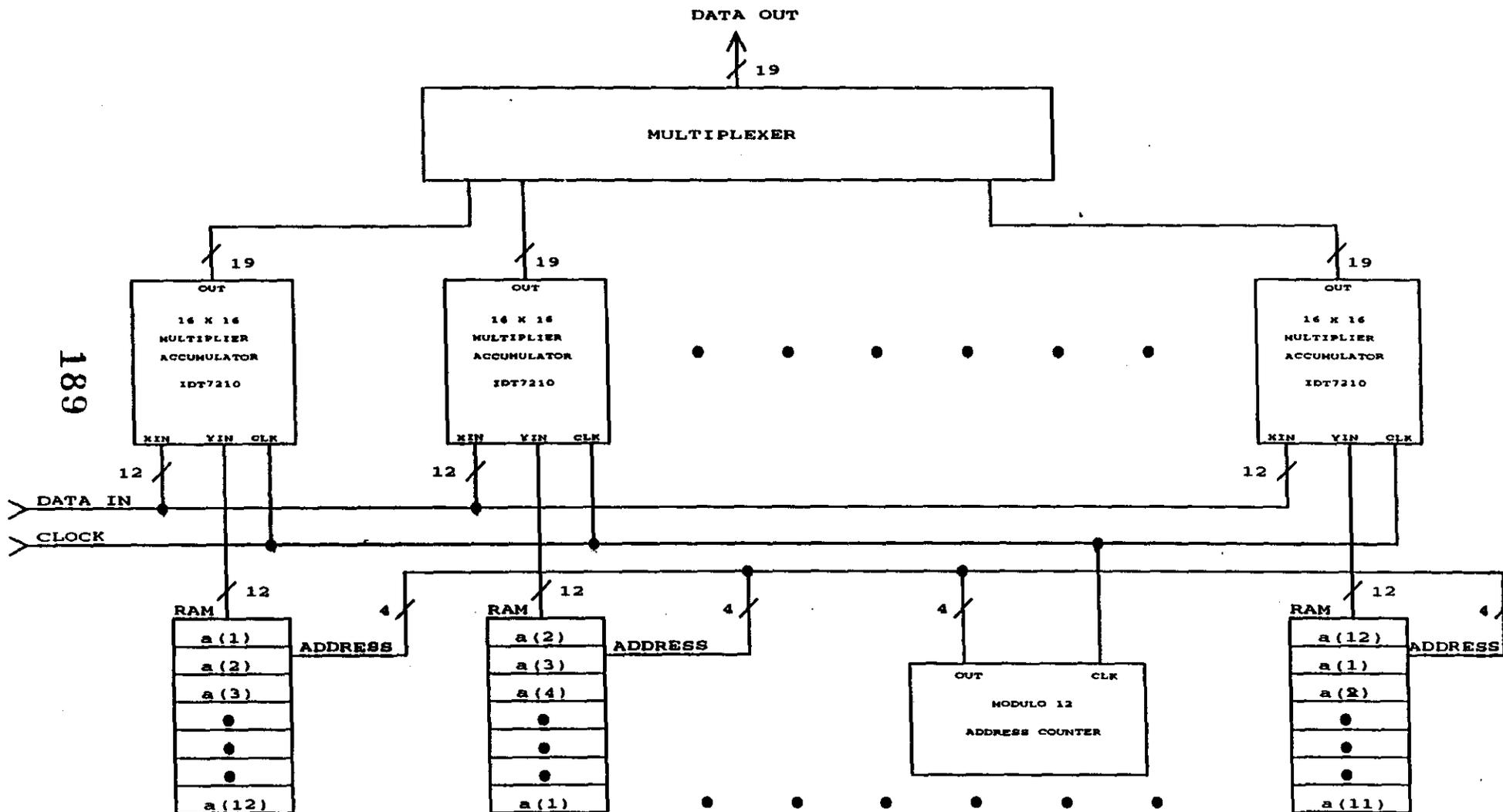
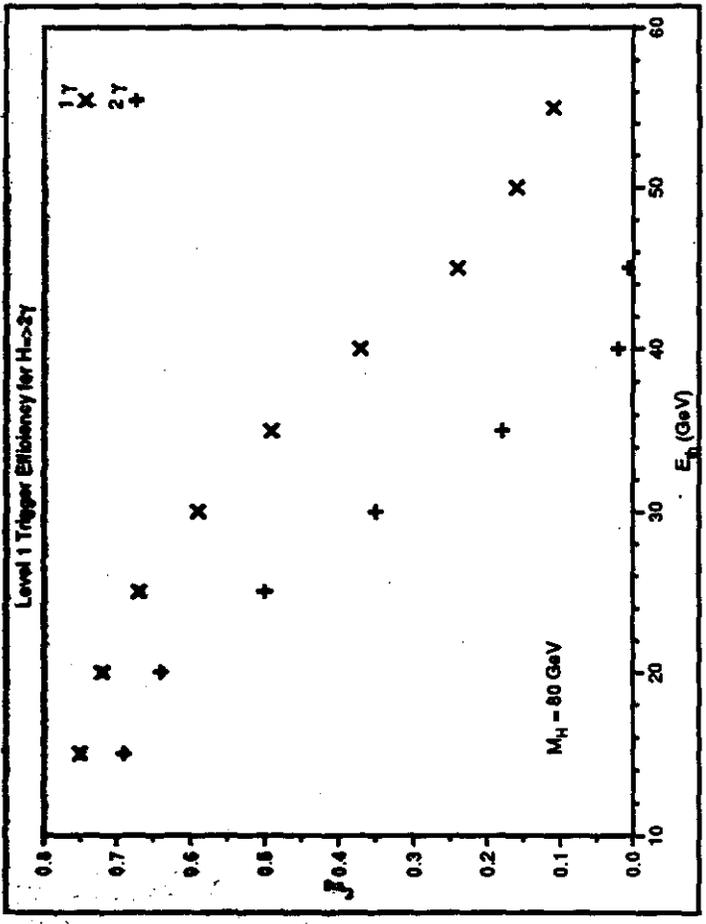
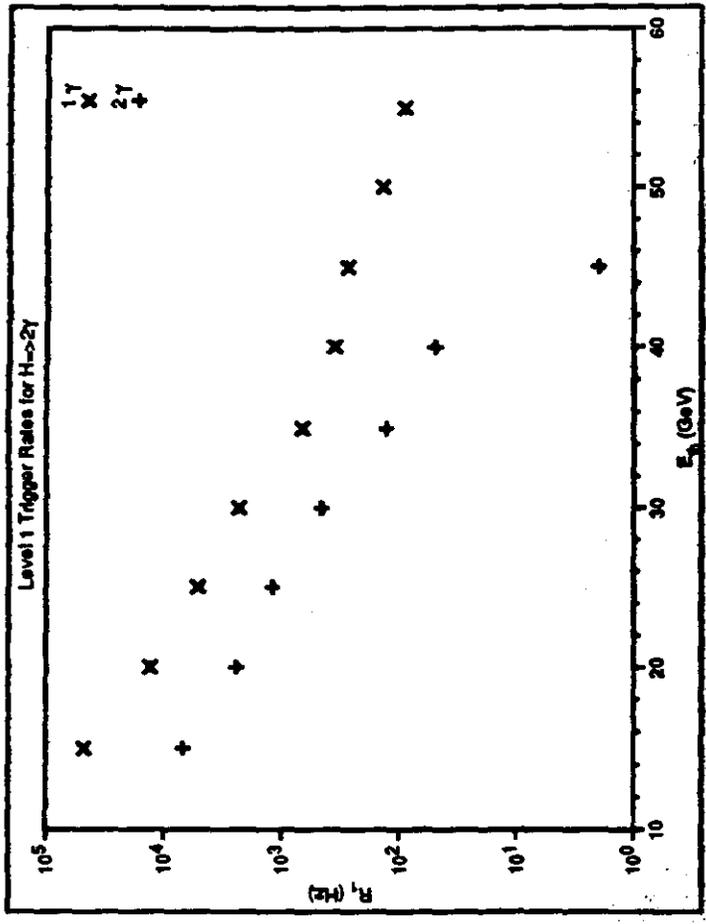


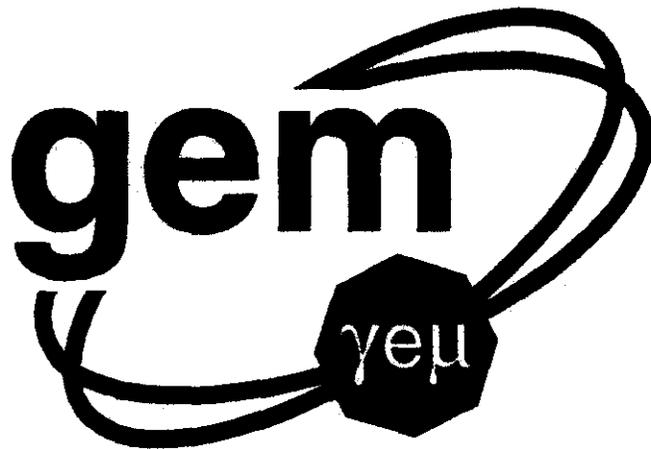
Fig 1.6

$H \rightarrow 2\gamma$ Trigger rate studies

- Rate estimates from 2 QCD jets of 10 GeV/c $\leq E_T \leq 640$ GeV/c
- Level 1: Analog sums followed by discriminators
 1. EM shower energy: ^{8x8} ~~7x7~~ EM sum above threshold E_{th}
 2. Hadronic isolation: each 4x4 hadronic sum behind central EM sum ≤ 5 GeV
 3. Lateral isolation: each of ¹⁶ ~~25~~ ^{8x8} ~~7x7~~ EM sums (far neighbors) ≤ 1 GeV

- Level 2: (a) digitized trigger sums and (b) selected EM and HAD cells
 1. Shower position: all ^{6x6}5x5 near neighbor sums lower than central ^{6x6}5x5 sum
 2. Lateral isolation: second highest ^{6x6}5x5 near neighbor EM sum less than 1 GeV
 3. Shower shape: 3x3/5x5 ratio (centered on maximum individual EM cell) greater than $R \approx 0.95$ (under study)
 4. Hadronic Isolation: Highest hadronic cell behind central cell $\leq E_{max} \approx 1$ GeV (under study)





CSC Readout

Bob Wixted

CSC Costing Status Summary

17 December 1992

Robert L. Wixted

OUTLINE

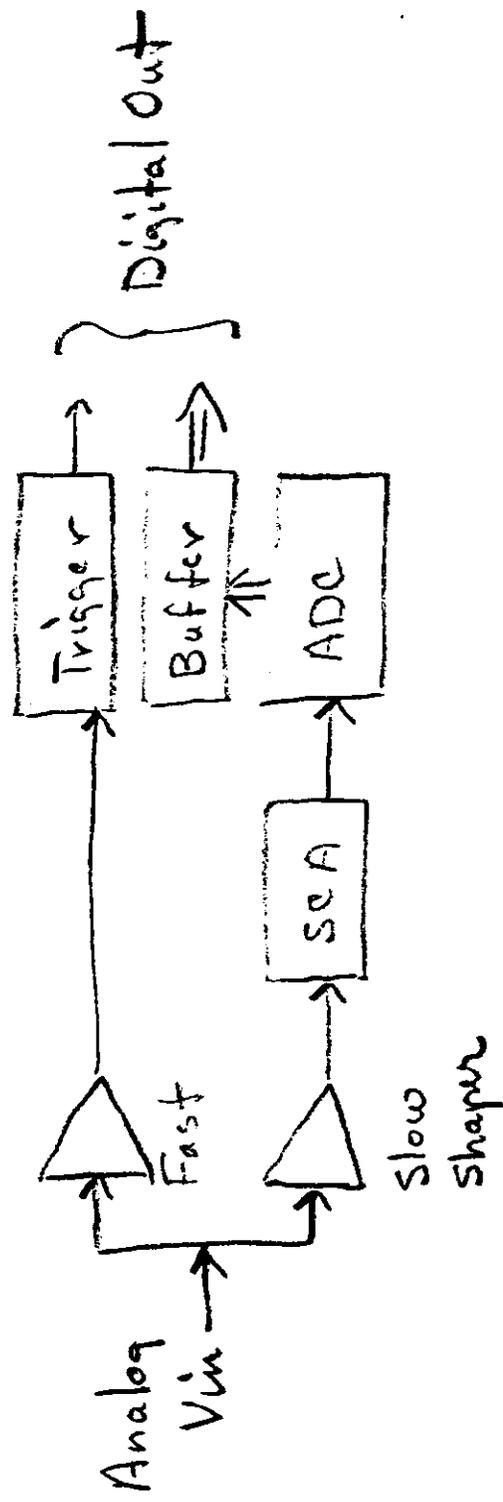
CHIP FLOORPLAN AND AMPLIFIER LAYOUT

COSTING METHODOLOGY REVIEW

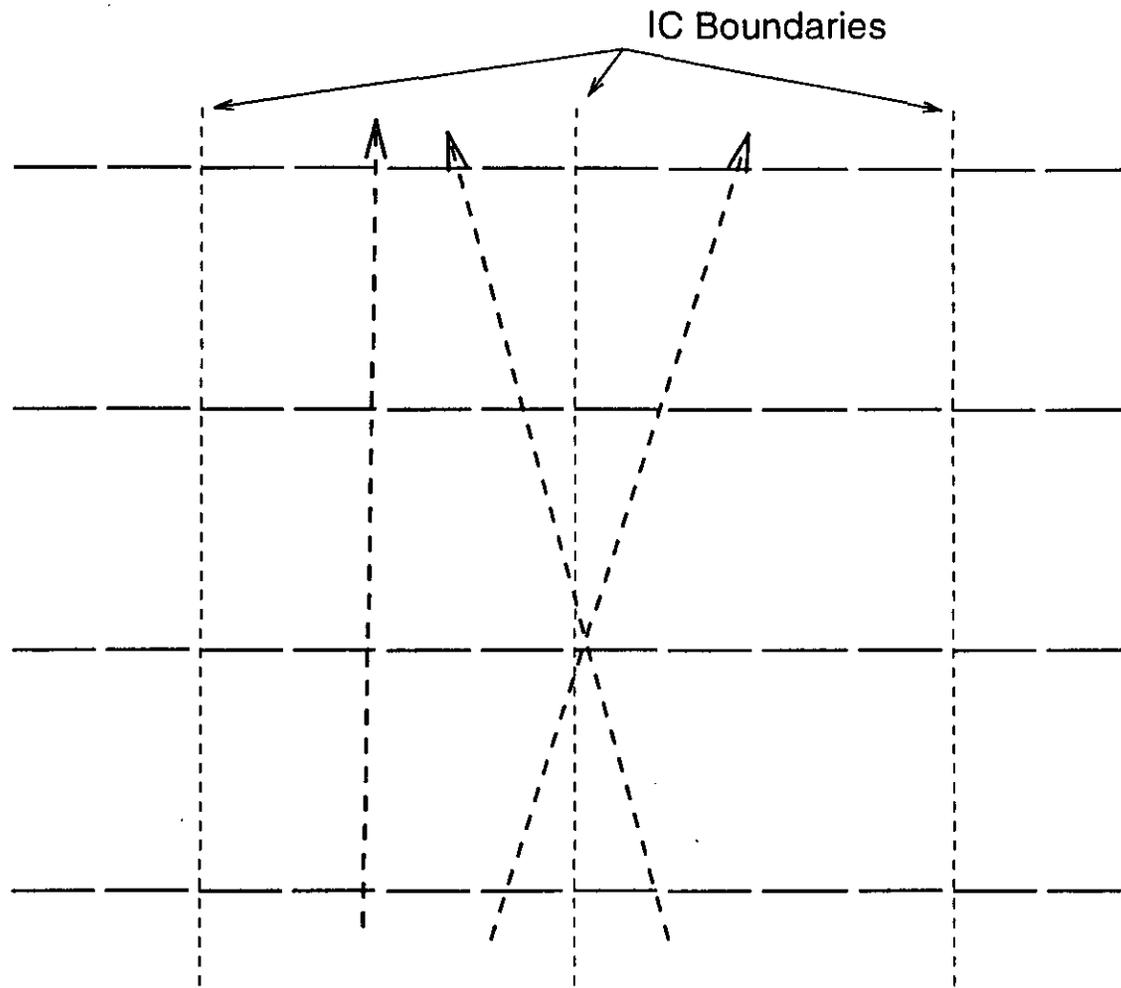
REVISED CSC CHIP COST ESTIMATE

CSC

READOUT BLOCK DIAGRAM

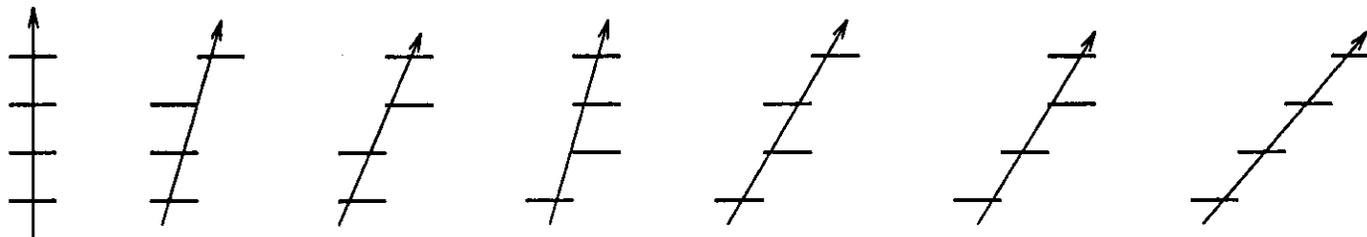


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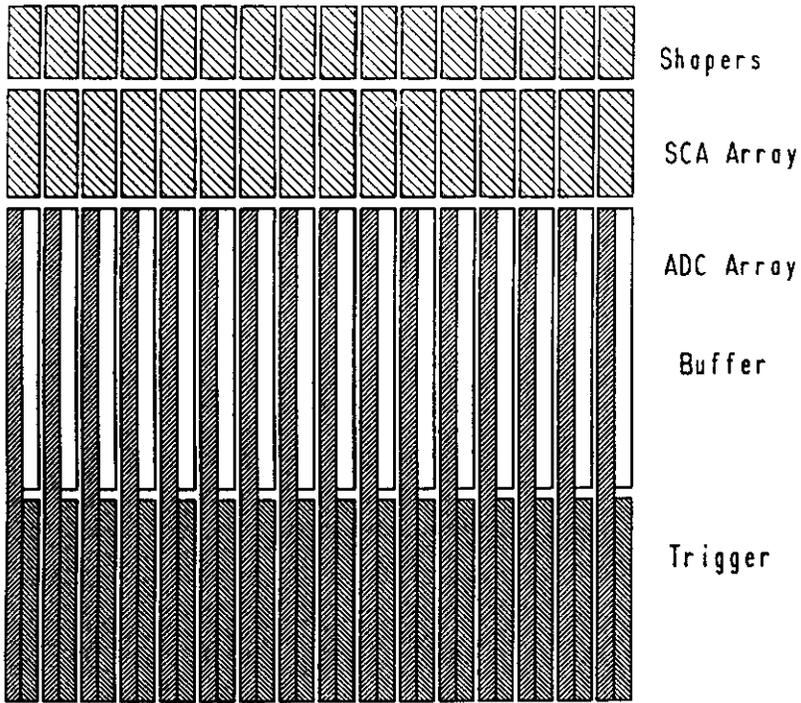
Each SCA/ADC Chip
Services 16 strips:
4 each in the 4 layers
that comprise a superlayer

Each chip must feed
across eight strips

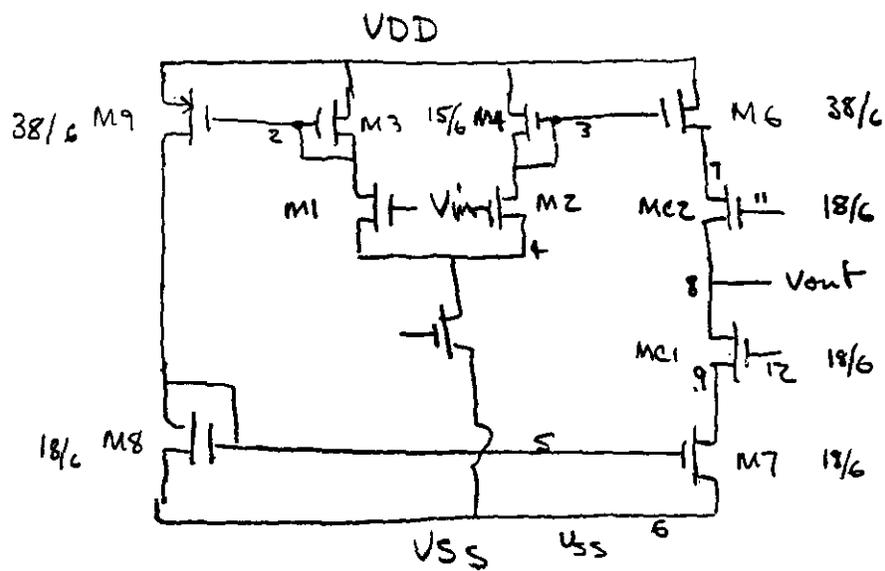


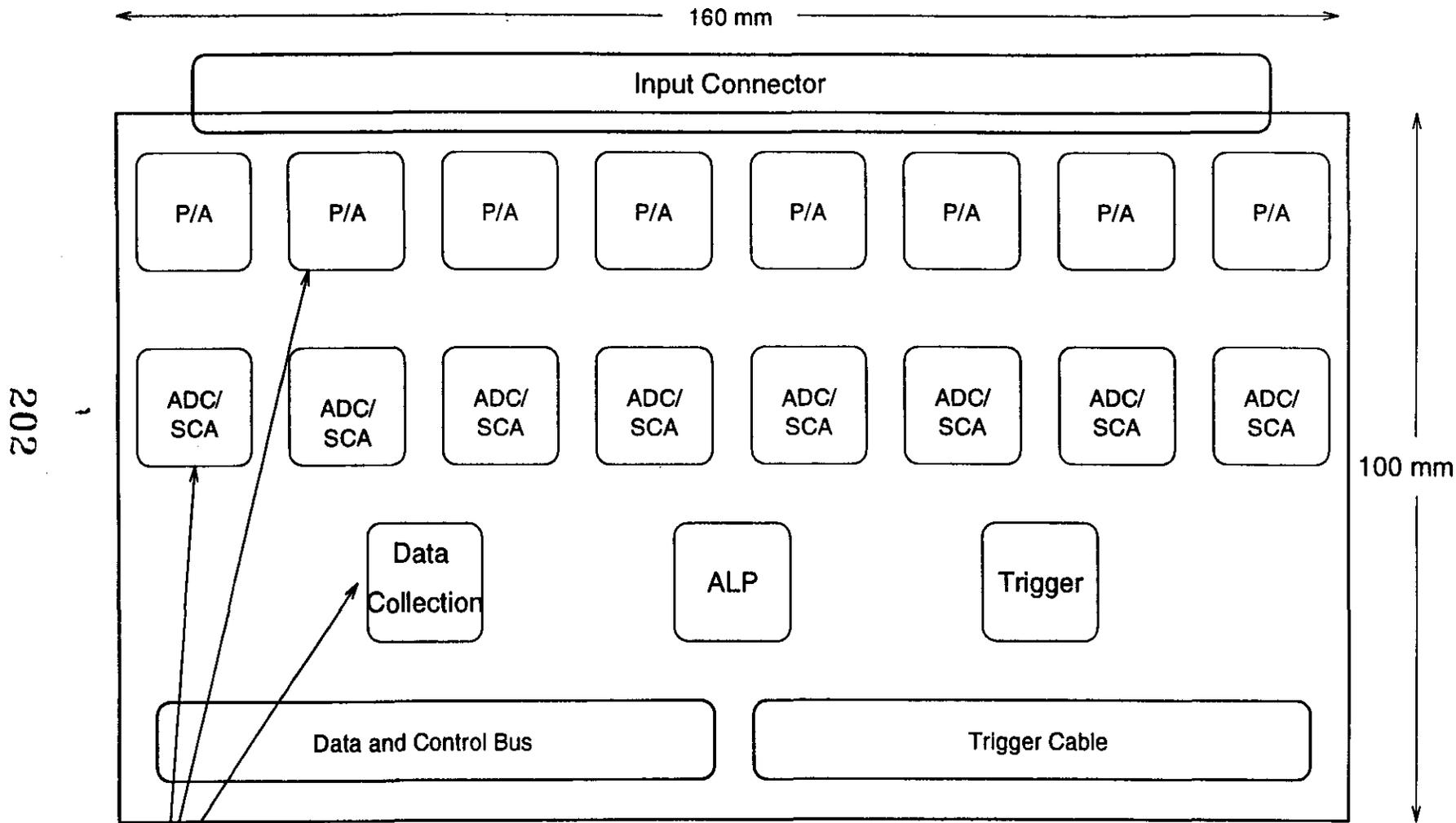
$$4 \times [(2 \times 6) + 1] = 52 \text{ Combinations per chip}$$

CSC Readout Chip



OP-AMP SCHEMATIC

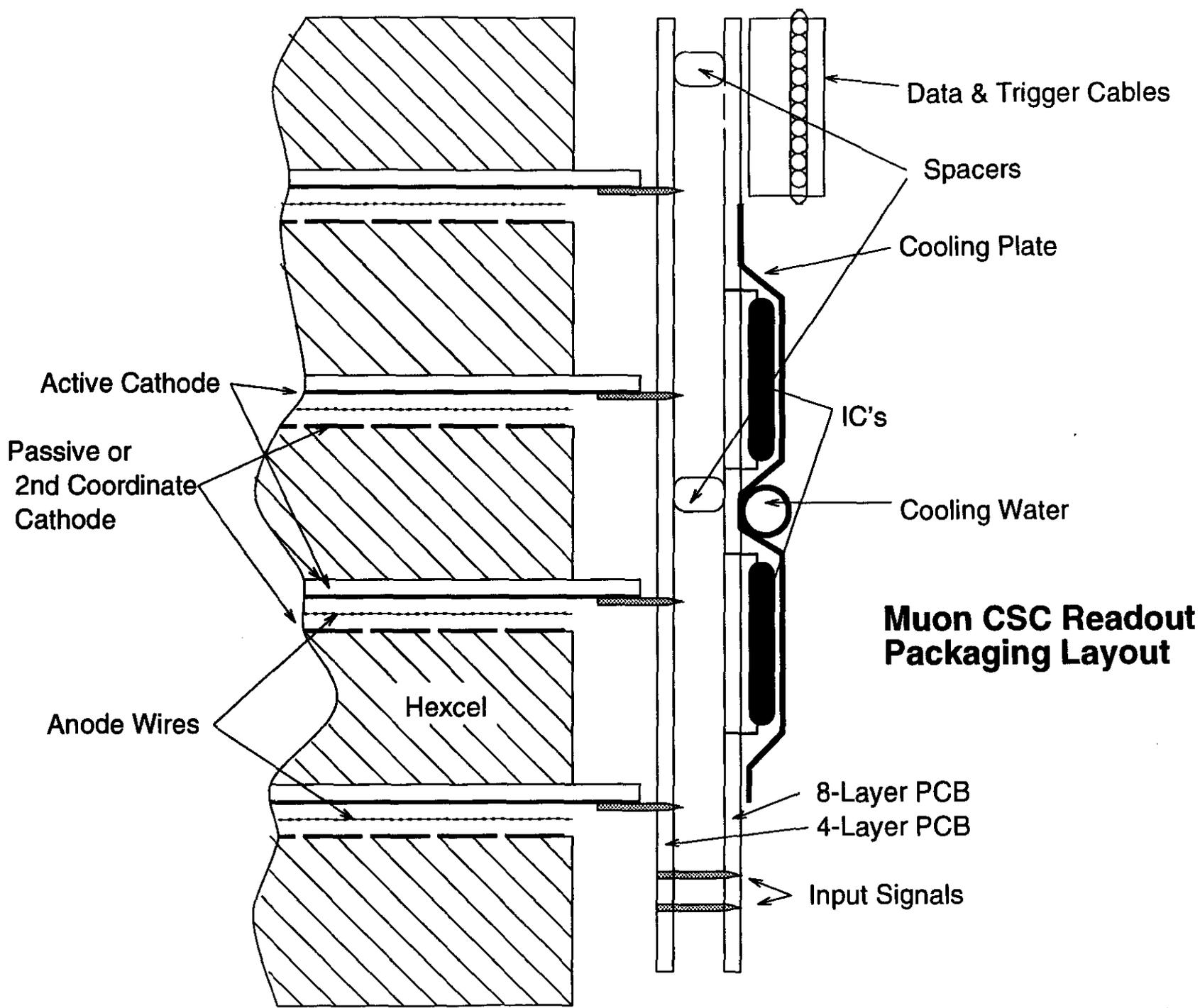




84-pin PQFP (typ)

**CSC Chamber Board Layout
128 Channel Version**

203



Muon CSC Readout Packaging Layout

Electronics Cost Estimate

Item	\$/Board	\$/Chan	Note	Revision
IC's (see summary table)	\$ 281	\$ 4.39	1	A
PCB Fab. (0.15 \$/cm ²)	\$ 48	\$ 0.75	2	B
Connectors (Male & Female)	\$ 64	\$ 1.00	3	C,D
Misc. Parts (W.A.G.)	\$ 20	\$ 0.32	4	B
Assy (1500 leads at \$ 0.06/lead)	\$ 90	\$ 1.41	5	B,D
Q/A (20 min)	\$ 10	\$ 0.16	6	B
Test (1 man-hour)	\$ 30	\$ 0.47	7	B
Rework (20% at 2 hrs/ea)	\$ 12	\$ 0.19	8	B
LVPS (200 mW/chan at \$ 5.00/W)	\$ 64	\$ 1.00	9	D,E
Mounting Hardware (W.A.G)	\$ 20	\$ 0.31	4	D,F
Packing & Shipping	\$ 20	\$ 0.31	4	B
Subtotal	\$ 659	\$ 10.30		
Contingency (30%)	\$ 198	\$ 3.08	10	
Grand Total	\$ 857	\$ 13.40		

- Assumptions

- 64 channel board of area 32 × 10 cm² (8 layers)
- Includes P/A shaper, SCA/ADC, DCC, & 1st Level Trigger
- SDC chip costing rules
- PC costs based on discussions with U.S. & Canadian vendors
- Assume SMT for automated assembly
- Fixed costs of R&D, EDIA, & NRE not included

Notes on CSC Costs

1. IC costs are based on a cost model employed by an SDC group from LBL. The model is summarized in the accompanying tables.
2. Assumes an eight-layer board of dimension $32 \times 10 \text{ cm}^2$ and \$ 0.25/in² per layer-pair. The latter figure is based on detailed discussions with U.S. and Canadian PCB vendors. Various groups within SDC have independently come to the same conclusion.
3. Based on costs of the input and output connectors used in prototype electronics. Actual costs may be lower due quantity purchase and due to careful choice of an economical connector.
4. Engineering judgement.
5. Assumes 1500 leads per board at \$ 0.06 per lead. Although our discussions with vendors indicated a cost of \$ 0.03 per lead, we have adopted the higher value used by SDC.
6. Assumes 20 minutes per board at \$ 30/hour.
7. Assumes one hour per board at \$ 30/hour.
8. Assumes that 20% of boards will require rework and that the average rework time will be two hours at \$ 30/hour.
9. Assumes 200 mW/channel at \$ 5/W delivered to the chambers. This is the value assumed in the LRS estimate.
10. A detailed element-by-element contingency analysis has not been performed.

Comments on PC Board Costs from Phase 2 Analysis

- A) A reanalysis of the SCA/ADC chip, which now contains the shaping amplifiers as well the first layer of trigger elements, yields similar results to the first analysis.
- B) The design now under consideration calls for 128 channels per board. Thus many of the fixed costs will be amortized over twice the number of channels. However, the increased density may result in modest increases in the per-board costs.
- C) A new connector scheme has evolved. No new estimate of the cost has been made.
- D) These items will benefit from additional work. In particular more detailed designs will allow us to obtain vendor quotes, which will increase our confidence in the estimated costs.
- E) The original cost estimate is generous in terms of cost per watt, but makes no allowance for the problems of on-detector cooling. An apparently inexpensive scheme for water cooling has been proposed, but it needs additional study.
- F) Work to be carried out in collaboration with GEM mechanical engineers should help to better define the cost of mounting hardware.

IC Cost Summary

SDC IC Costing Rules						
Size	Area	Yield	Fab.	Pkg	Test	Total
Tiny	6.8 mm ²	70%	\$ 2.05	\$ 1.00	\$ 7.50	\$ 10.55
Small	35 mm ²	65%	\$ 11.17	\$ 1.50	\$ 8.00	\$ 20.67
Medium	50 mm ²	60%	\$ 17.65	\$ 2.00	\$ 8.50	\$ 28.15

Non-recurring expenses (NRE):

- \$ 25K per design for masks
- \$ 5K per design for testing setup

CSC IC's				
Description	Type	Chans/Pkg	\$/Chan	Revision
P/A Shaper	Tiny	8	\$ 1.32	A
SCA/ADC	Medium	16	\$ 1.75	B
ALP	Medium	64	\$ 0.44	C
DCC	Medium	64	\$ 0.44	C,D
Trig	Medium	64	\$ 0.44	C,D
Total			\$ 4.39	

Comments on IC Costs from Phase 2 Cost Analysis

- A) It should be possible to implement sixteen channels per package, resulting in somewhat reduced costs.
- B) A second analysis using ORBIT pricing data more detailed chip-area estimates yields comparable costs.
- C) In the current design, the ALP, DCC, and Trigger chips will service 128 channels each.
- D) The function and design of these chips is not well understood at this point. Additional R&D effort is needed to better define their requirements.

CSC System Cost Summary

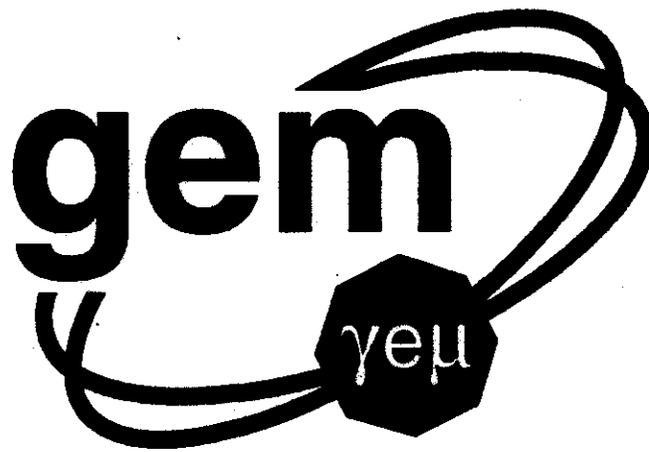
- Additional Front End WBS Elements (added cost per 1000-channel-module)
 - HVPS & Cable \$ 200
 - Fiber Data Links \$ 370
 - Trigger Cable \$ 120
 - Total additional per channel (w. 30% contingency) \$ 0.90
- Grand total per channel: $\$13.40 + \$0.90 = \$14.30$
- Channel Count
 - 1050 K fine cathodes
 - 160 K anodes (or coarse cathodes)
 - 1210 K total
- Fixed cost of R&D, prototypes, etc. \$ 2760 K (from LRS report)
- Total Front End Cost

$$\$2760 \text{ K} + 1210 \text{ K} \times \$14.30 = \$20.1 \text{ M}$$

- There is an additional \$ 6.6 M in the LRS report for the Level 1 trigger.

CSC Chip Revised Preliminary Costing

Chip Size 5.1 by 5.7 mm	29 sqmm
4 inch wafers	270 chips
80% litho yield	229 chips
60% test yield	137 chips
\$750/wafer	\$5.44 per chip
Package	\$1.45 ea
Testing	\$10.00 ea
Total cost	\$16.89 per chip
Cost per Channel (\$1.75)	\$1.05



Calorimeter Trigger

Dario Crosetto

GEM Trigger meeting

December 11, 1992

L1 Trigger 3D-Flow system, boards, cables.

D. Crosetto

Tranparencies

On request by the audience
at the presentation of Dec. 11, 1992

3D-FLOW SYSTEM POWER CONSUMPTION DISSIPATION

WRITTEN COST ESTIMATES from SEVERAL INDUSTRIES have calculated the power consumption of a "3D-Flow" processor from 200 to 250 mW.

(This calculation included the Multiply Accumulate (MAC) Unit that is not strictly necessary for pattern recognition algorithm, but is essential if it is desired to have a digital filter on the input digitalized signal. By dropping the MAC unit, the power consumption will drop considerably)

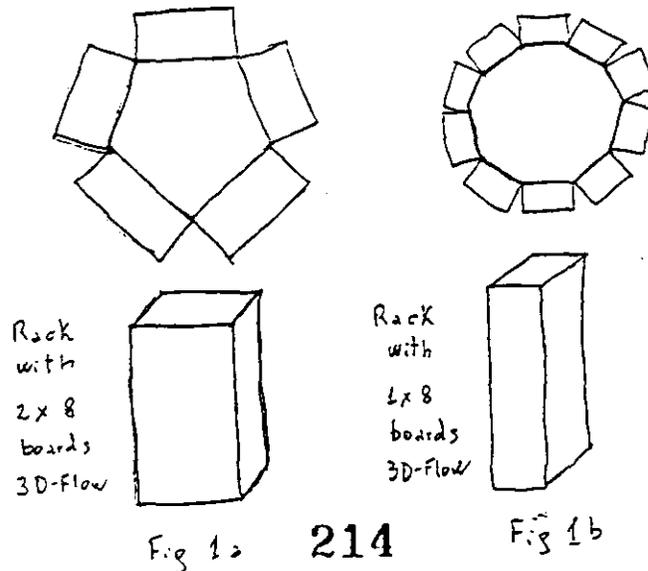
Based on the power consumption of a 3D-Flow chip with MAC unit = 200 mW, the total power consumption will be:

- One 3D-Flow board with 16 x 3D-Flow processors = 3.2 W
- One stage with 1280 "3D-Flow" processors = 256 W
- Several stages can be assembled, assuming a system with 16 stages = 4,096 W

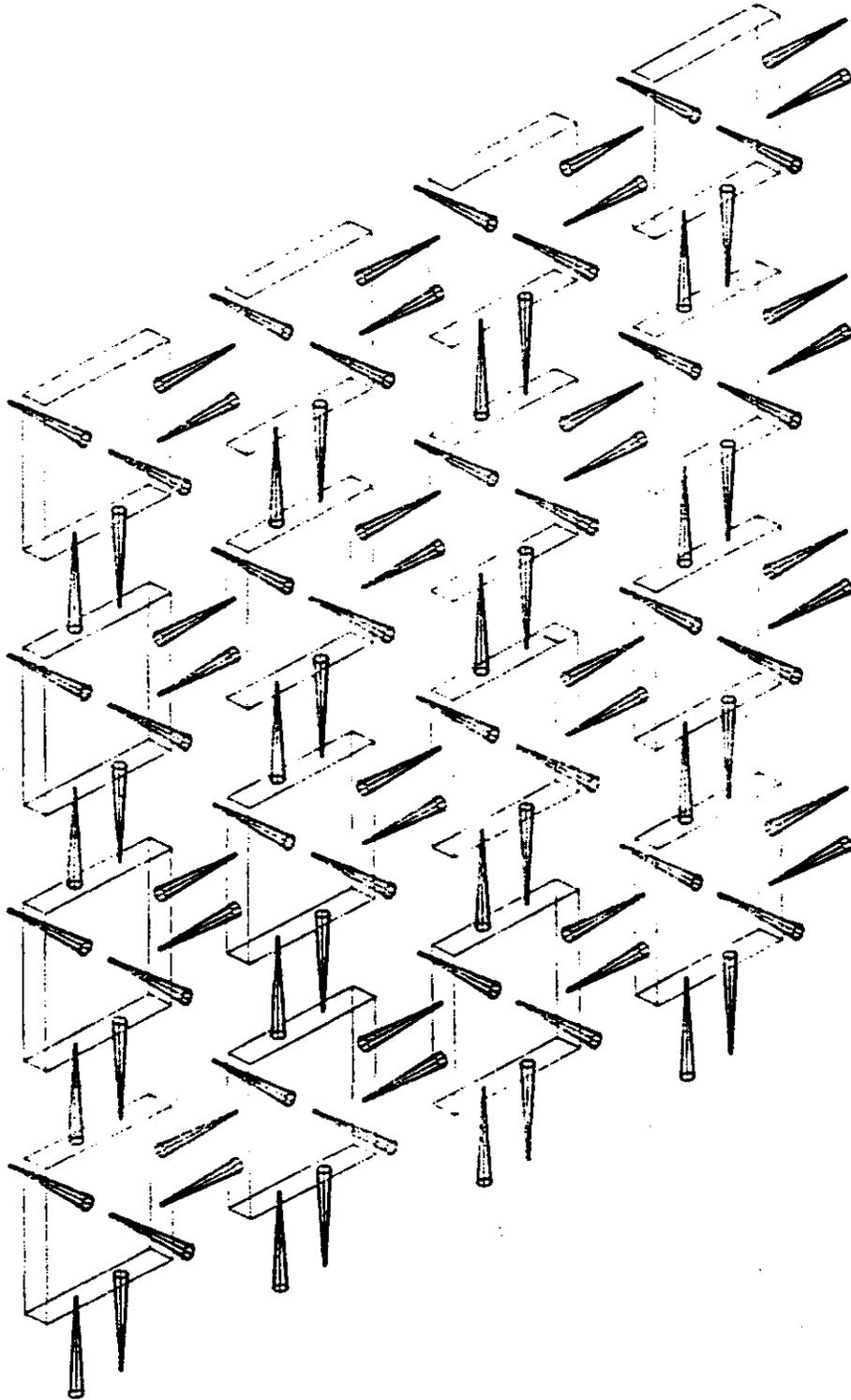
- Different rack assemblies can be made:

- subdividing the system in a pentagon racks (as shown in Fig. 1a), 2 boards in the row and 8 boards in the column will be accommodated for each stage, this will give 16 boards per stage per rack = 51.2 W. In the case of a 16 stage system, the power per rack will be 819.2 W.
- subdividing the system into a 10-sided cylinder racks (as shown in Fig. 1b); a system with 16 stages will have a rack dissipation of 409.6 W.

Connectors on the board can be alligned vertically in the two side (left and right) of the board, allowing air flow from bottom to top on the 3D-Flow chips.



Interconnection between Front-End Processors (FEP)
(1 FEP array layer in perspective view)



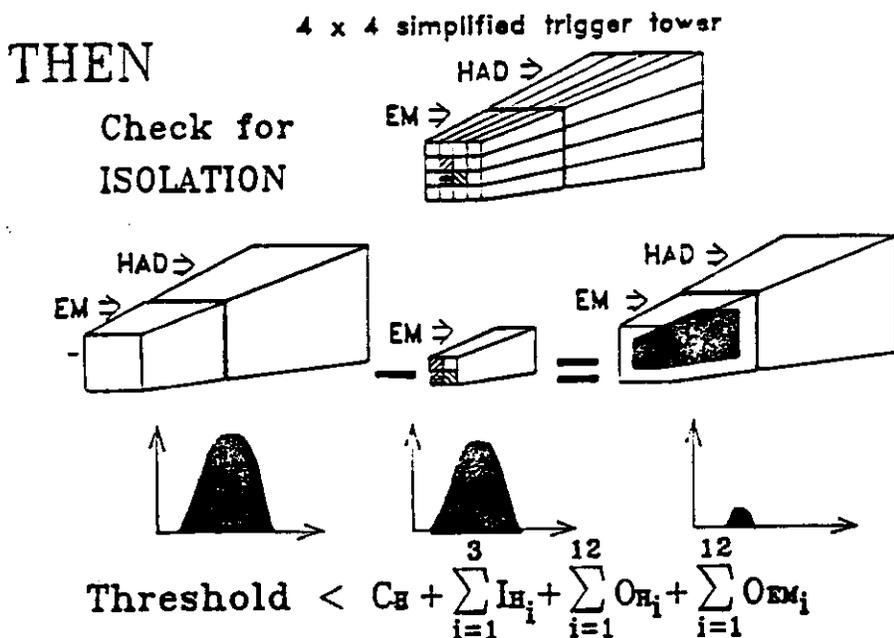
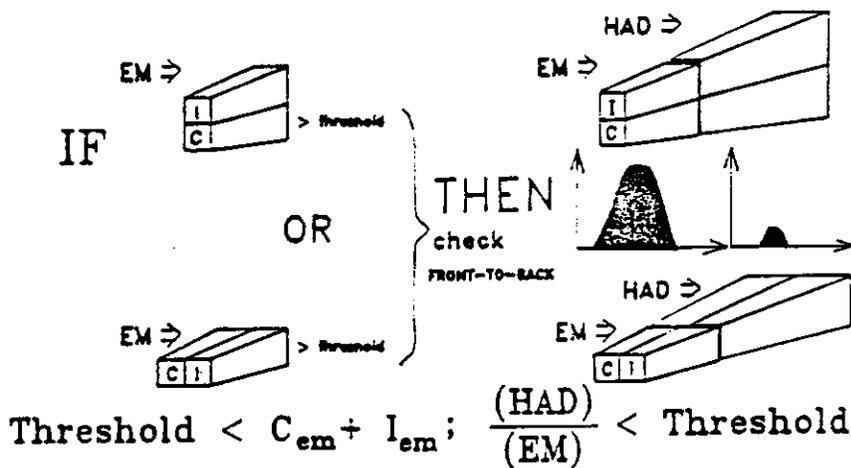
3rd Int. Conf. on Advance Technology. Como. June 25, 1992.

Dario Crosetto

Local maximum

I	I	I
I	C	I
I	I	I

 $C > I_i$ for $i = 1, \dots, 8$.
 Threshold $< \sum_{i=1}^8 I_i + C$.



Jet finding

 Threshold $< \sum_{i=1}^{16} E_{EM_i} + \sum_{i=1}^{16} E_{R_i}$

15 steps

Any algorithm type and length

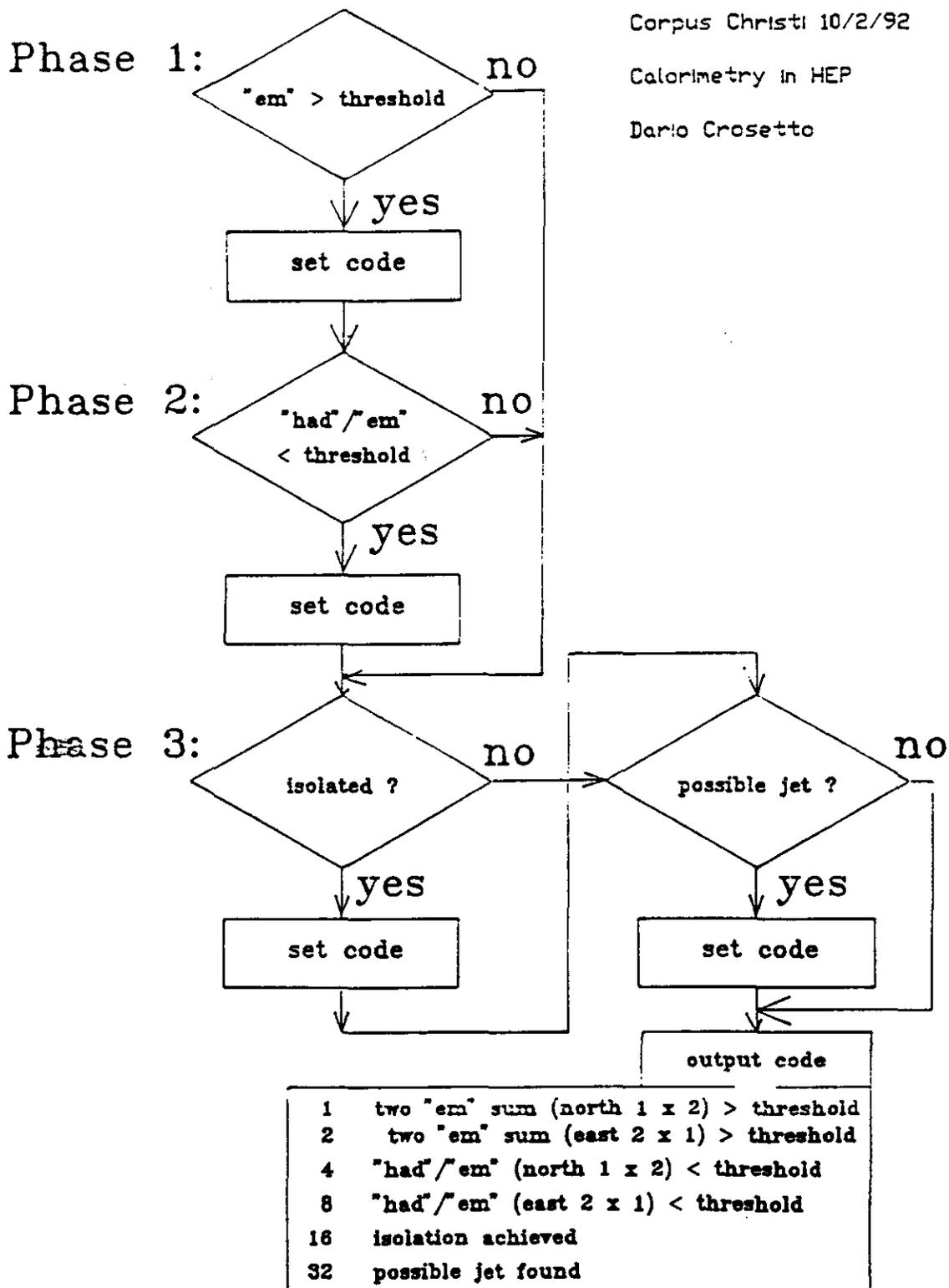
31 steps

Algorithm flow-chart

Corpus Christi 10/2/92

Calorimetry in HEP

Dario Crosetto



e.g. A "FEP" may return a code = 37 (1+4+32) stating:

- a possible electron was found,
- but it was not isolated from the surrounding energy,
- and that cell may be part of a 4 x 4 jet.

3D-FLOW processor clock speed = 8 ns
 Number of steps of Algorithm = 16

Algorithm execution time = 128 ns

1 stage
 sustain 7.8 MHz input data rat

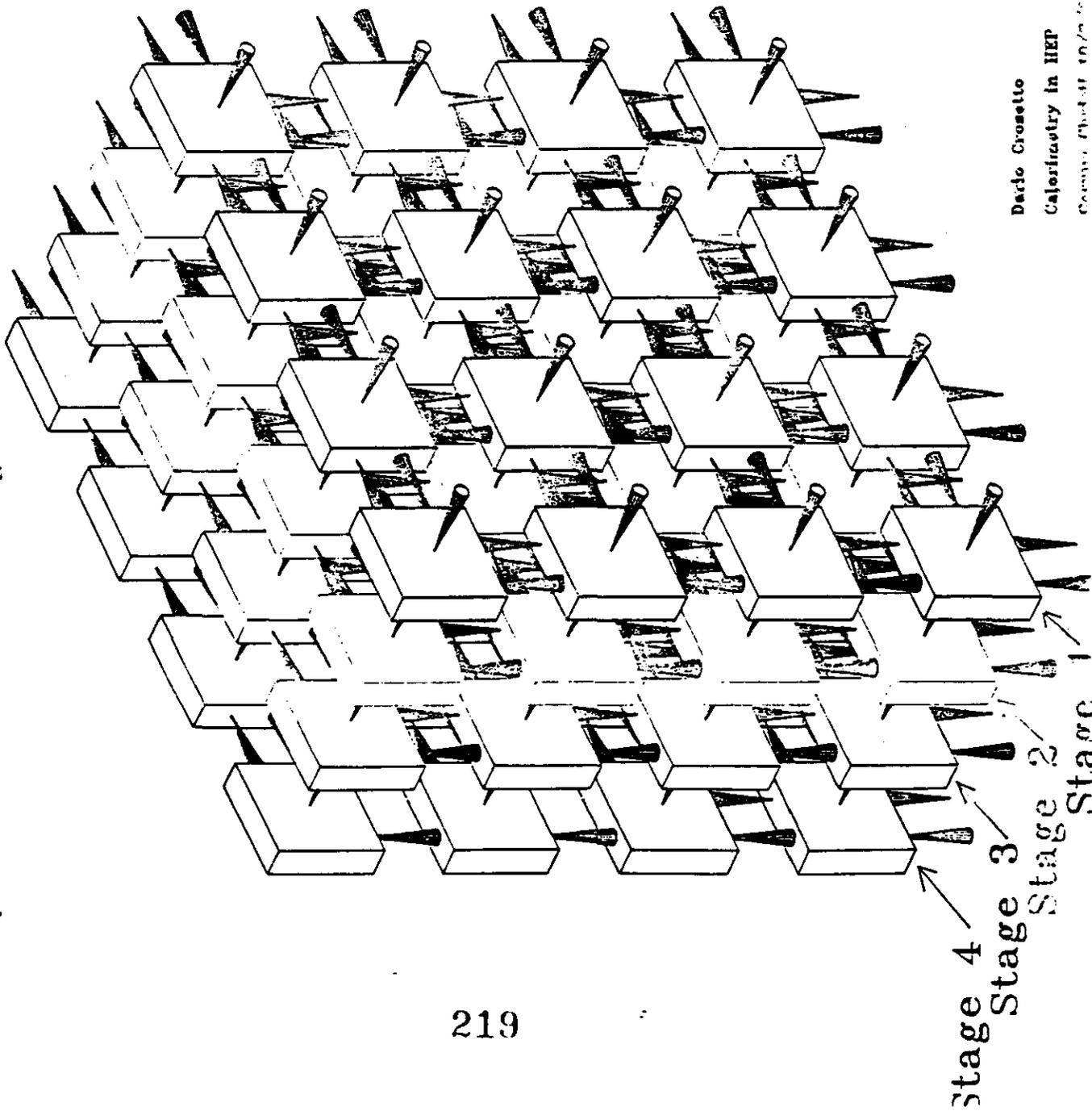
two stages
 sustain 15.6 MHz " " "

three stages
 sustain 23.4 MHz " " "

⋮ ⋮ ⋮ " " "

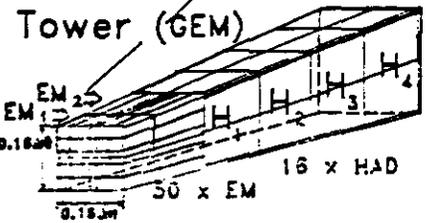
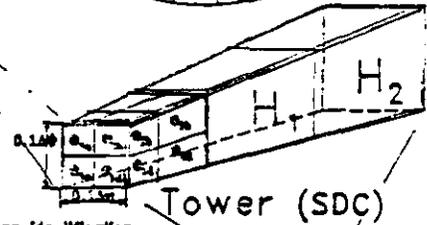
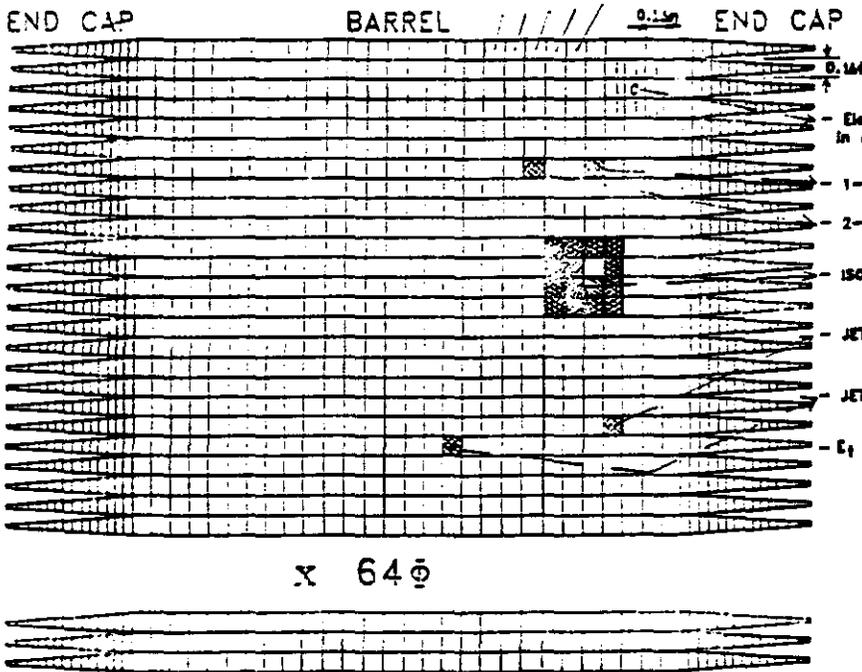
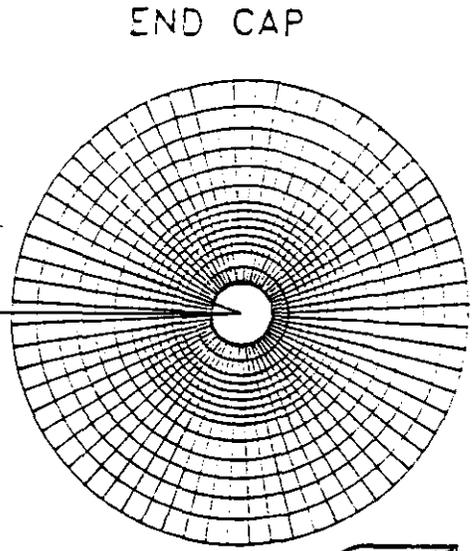
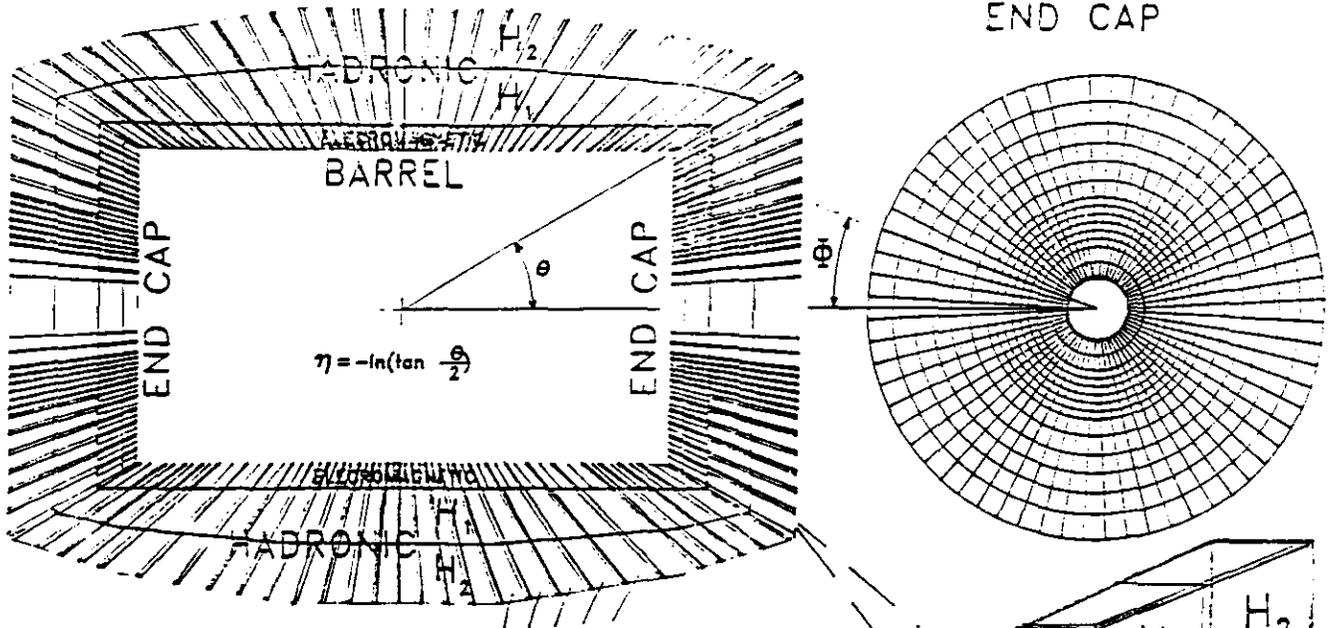
8 stages
 sustain 62.5 MHz " " "

Decentralized Parallel Processing architecture.



Dario Grosseto
Calderini in HEP
CERN, March 1978

CALORIMETER CROSS-SECTION



Unrolled "Barrel" + unfolded END CAP = Towers processor array

ONE TOWER = ONE PROCESSOR

l level trigger granularity		examples
Experiment	$\Delta\eta \Delta\phi$	Number of processors
GEM	0.16 x 0.16	1250
SDC	0.1 x 0.1	3584

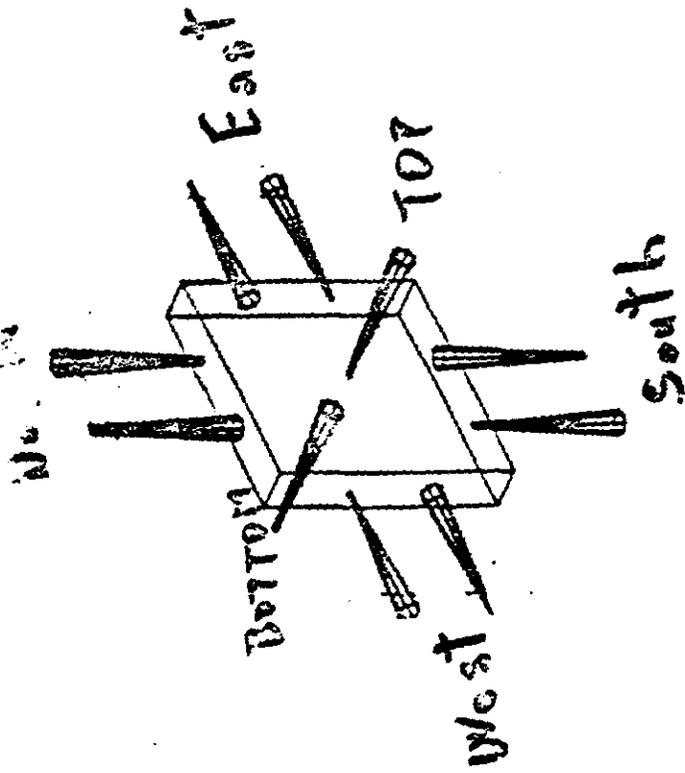


FIGURE 5. 3D-Flow processor

6.0 3D-FLOW CHIP ASSEMBLY

A price/performance market study led to design an economical 3D-Flow processor chip with only four 3D-Flow processor cells. This will require from 50,000 to 80,000 gates (depending on the technological process used and functionality of the processor).

Among the more economical packaging are available the Quad Flat Packs (QFPs) and the Land Grid Package (LGA).

A 3D-Flow chip accomodating four 3D-Flow processors could be packaged in a 25 mm x 25 mm LGA.

222

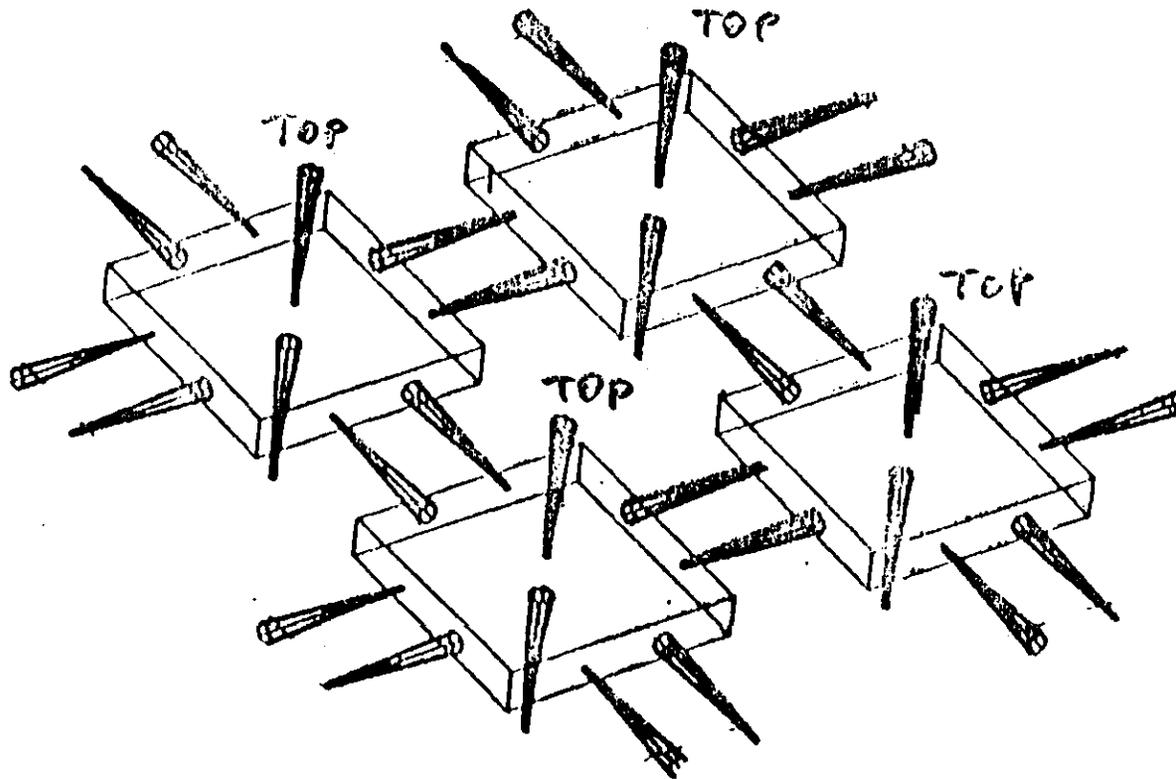


FIGURE 7. Functional scheme of a chip with 4 x 3D-Flow processors.

7.0 3D-FLOW BOARD LAYOUT

The basic element for the construction of a programmable Level-1 trigger suitable for different calorimeter sizes and with different event rates, is a PCB board with 16 x 3D-Flow processors (4 in. x 4 in.) or a PCB board with 64 x 3D-Flow processors (5 in. x 5 in.)

223 The difference in using one of the two boards is the following. The PCB board (5 in. x 5 in.) with 64 x 3D-Flow processor, will have an higher cost but it will allow to build an equivalent system as with the 16 x 3D-Flow PCB boards in almost half size in diameter and height as shown in Figure 13 and Figure 14.

Edge connectors of PCB board of Fig. 9 and Fig 10 have 120 contacts each (spaced 0.050 in), while edge connectors in Fig. 11 and Fig. 12 have 240 contacts each (spaced 0.025 in). Other connectors are surface mounting with contacts spaced 0.050 in. The 3D-Flow chips assembled on the 16 x 3D-Flow processor board can be packaged in QFP or in LGA, while the 3D-Flow chips assembled on the 64 x 3D-Flow processor board can use the Multi Chip Module (MCM) or the Tape Automated Bonding (TAB) technique.

1161 x 3D-Flow Processors per board

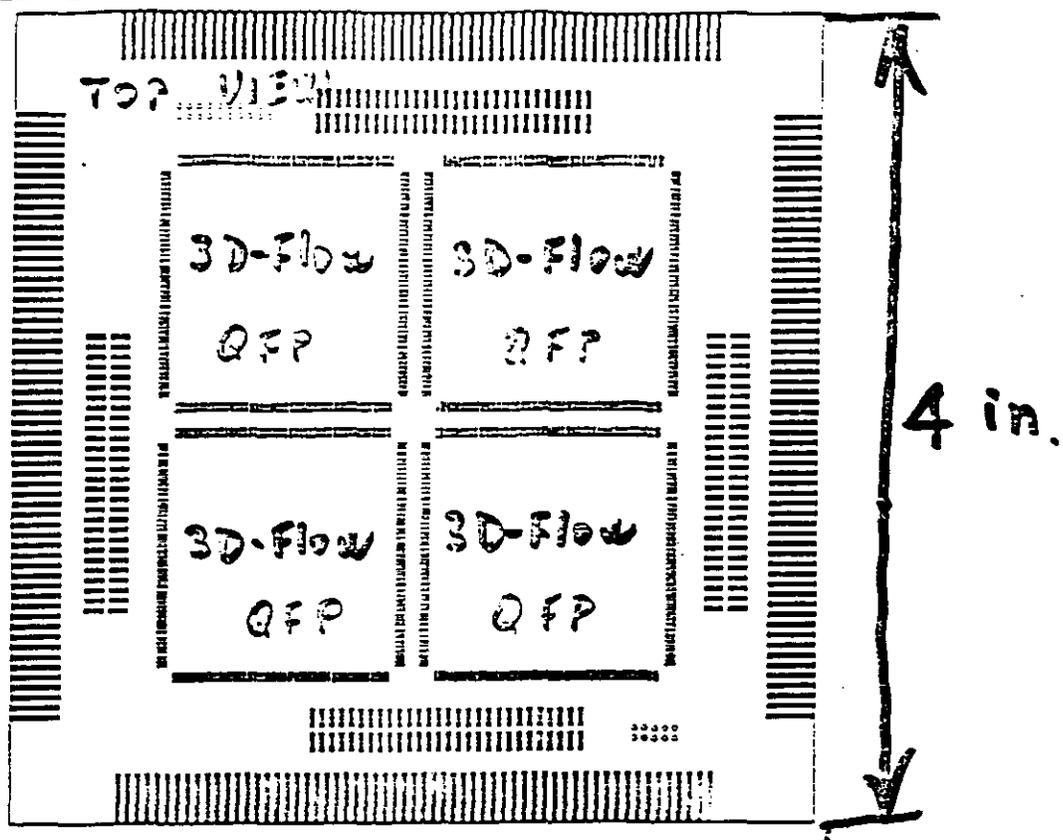


FIGURE 8. Board layout of four 3D-Flow chips each containing 4 x 3D-Flow processors (Top view)

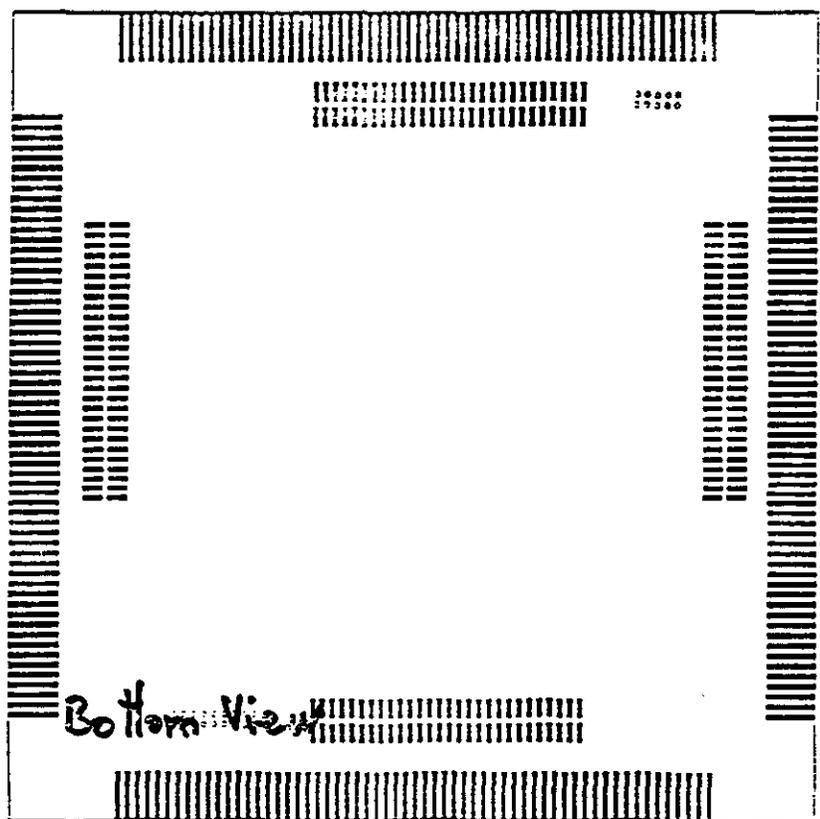


FIGURE 9. Board layout of four 3D-Flow chips each containing 4 x 3D-Flow processors (Bottom view)

CONTACT (NEARSIDE) #1
CONTACT (FARSIDE) LAST

SEE DETAIL C

.250 MIN.
(BOTH SIDES)

R.053 (2X)

.200 ± .002
(BOTH SIDES)

(.053) CTC X NO. OF SPACES = (DIM. "L")
TOLERANCE NON-ACCUMULATIVE

DIM. "M" ± .002

.040 (REF)
(BOTH SIDES) [2]

45°
(2X)

.320

THIS AREA TO BE
FREE OF SOLDERMASK
(BOTH SIDES)

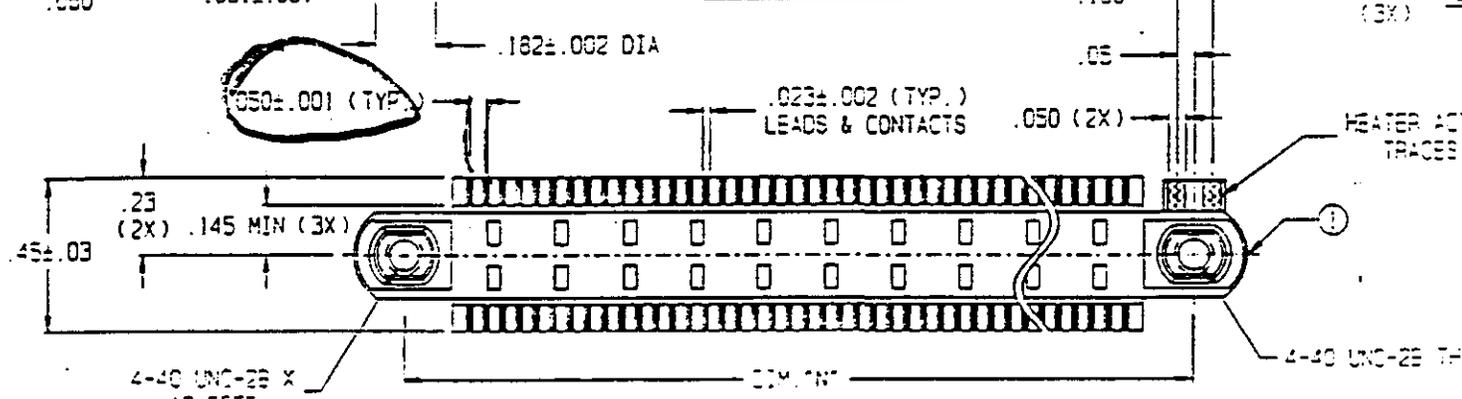
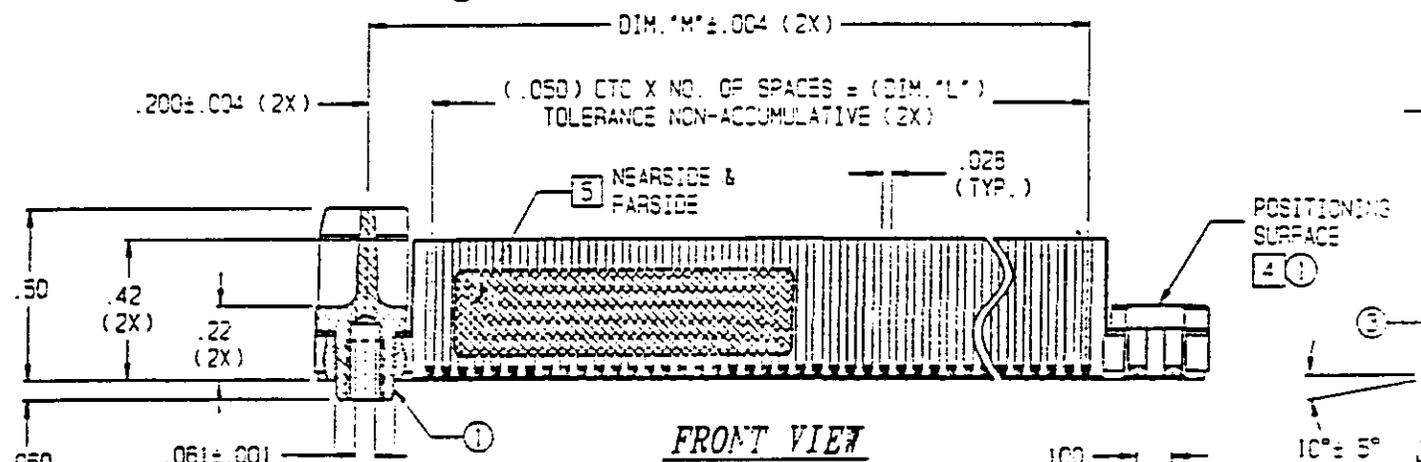
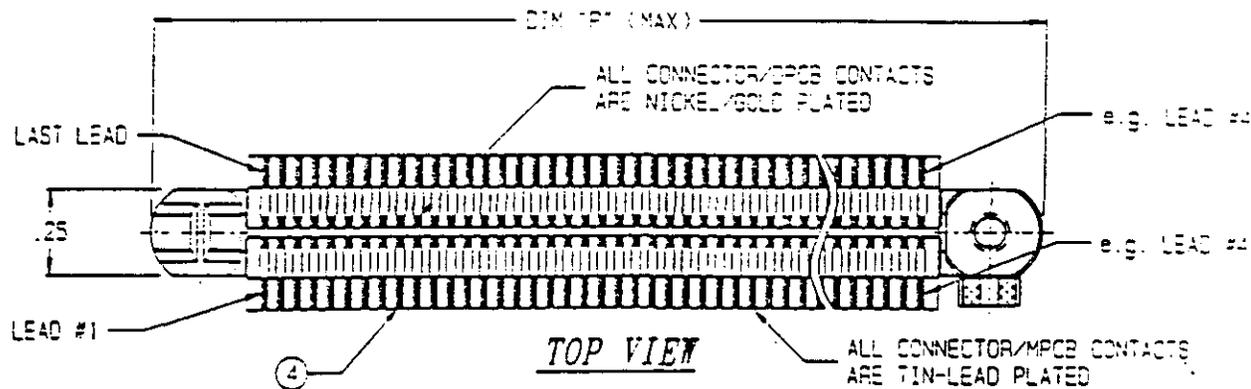
.050 ± .001
(TYP.)

[2] (BOTH SIDES)

.0625 ± .005
[1] ± .005

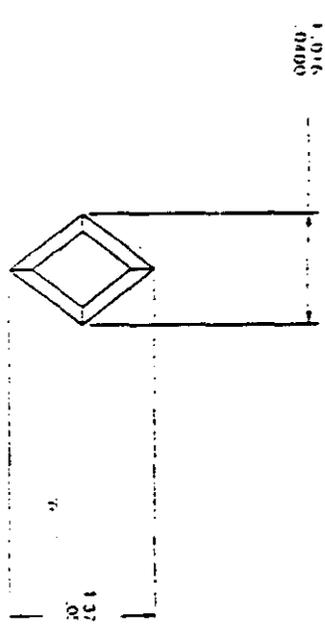
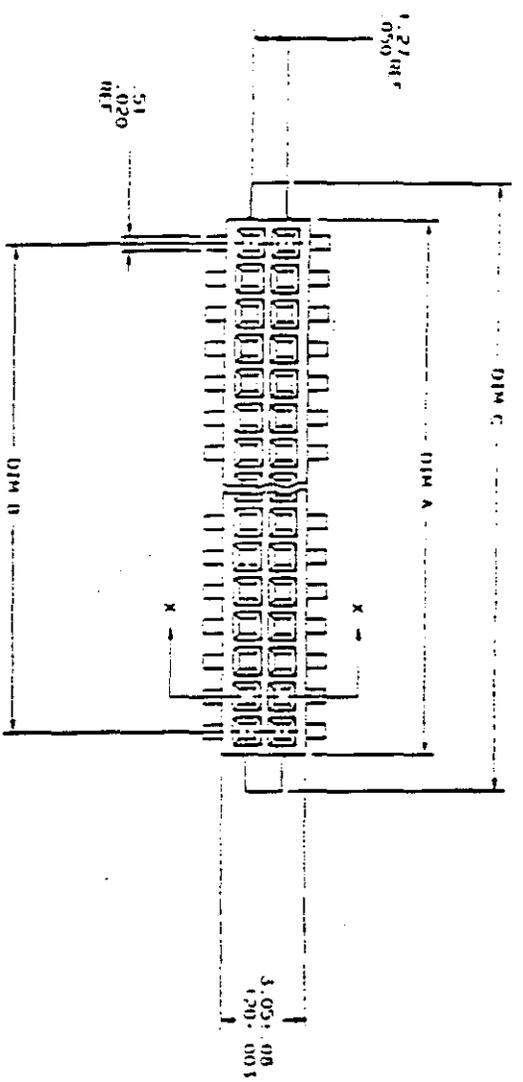
.030 ± .001 (TYP.)
[1] ± .005

DETAIL C
SCALE NONE

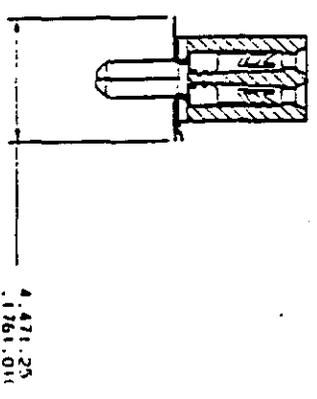
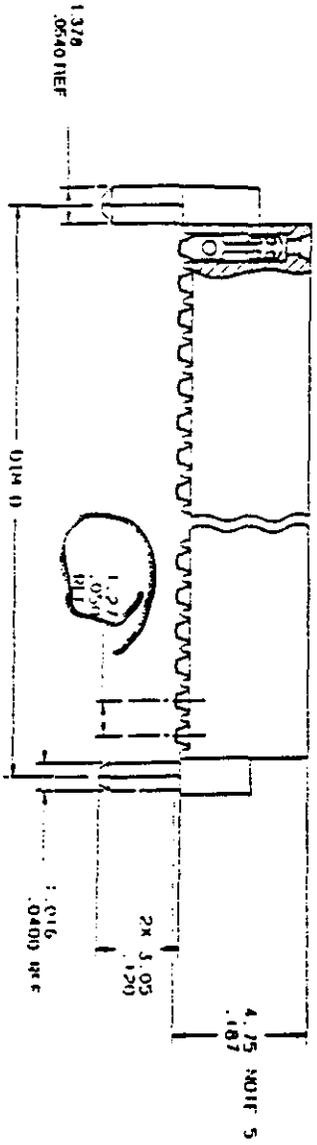


PART ORDERING INFORMATION				BOARD THICKNESS RANGE	GAP DIM. "K"
PC	- X	- 050	- XXX	- X	
	LENGTH	TRACE SPACING	NUMBER OF CONTACTS	BOARD THICKNESS RANGE	
					SEE TABLE
				A =	
				B =	
				C =	.058 - .058
				E =	.040
				F =	.067 - .099
					.070

FIGURE 1 (cont.)
SEE PART I



VIEW E
SCALE 40/1



SECTION X-X

REV	DATE	BY	CHKD	DESCRIPTION
1				INITIALS
2				NOTES
3				DATE
4				SCALE
5				UNIT
6				PROJ
7				DEPT
8				COMP
9				REV
10				DATE
11				SCALE
12				UNIT
13				PROJ
14				DEPT
15				COMP
16				REV
17				DATE
18				SCALE
19				UNIT
20				PROJ
21				DEPT
22				COMP
23				REV
24				DATE
25				SCALE
26				UNIT
27				PROJ
28				DEPT
29				COMP
30				REV
31				DATE
32				SCALE
33				UNIT
34				PROJ
35				DEPT
36				COMP
37				REV
38				DATE
39				SCALE
40				UNIT
41				PROJ
42				DEPT
43				COMP
44				REV
45				DATE
46				SCALE
47				UNIT
48				PROJ
49				DEPT
50				COMP
51				REV
52				DATE
53				SCALE
54				UNIT
55				PROJ
56				DEPT
57				COMP
58				REV
59				DATE
60				SCALE
61				UNIT
62				PROJ
63				DEPT
64				COMP
65				REV
66				DATE
67				SCALE
68				UNIT
69				PROJ
70				DEPT
71				COMP
72				REV
73				DATE
74				SCALE
75				UNIT
76				PROJ
77				DEPT
78				COMP
79				REV
80				DATE
81				SCALE
82				UNIT
83				PROJ
84				DEPT
85				COMP
86				REV
87				DATE
88				SCALE
89				UNIT
90				PROJ
91				DEPT
92				COMP
93				REV
94				DATE
95				SCALE
96				UNIT
97				PROJ
98				DEPT
99				COMP
100				REV



Traditionally, system houses that need to quickly implement technology-intensive, high-complexity boards would turn to full-service board vendors, application-specific board vendors, or their own in-house board manufacturing. But now with products requiring mixed assembly technologies, choosing a board manufacturing solution is more complicated. High-volume, mixed-technology assembly is a capital-intensive proposition that requires a \$20-30 million investment in equipment, a cost that's out of reach for most assembly houses and smaller companies that do their own manufacturing. Equipment delivery, set-up and operational learning curves are additional details to consider. System houses can avoid all this, by employing the services of S-MOS Systems' BLP business unit.

BLP injects advanced technology and offers improved design flexibility, product yield and turn-around time. By using BLP's full-service module manufacturing capability and advanced technology, designers can bring multiple technology modules to market quickly.

Advanced Packaging Technology

	Current	Future
QFP		
Pin count	208 pin	376 pin
Inner lead pitch	120µm	130µm
Outer lead pitch	0.5mm	0.3mm
Body thickness	3.35mm	1.0mm
COB		
Pin count	168 pin	256 pin
Pad pitch	130µm	100µm
Body thickness	1.0mm	0.8mm
TAB		
Pin count	200 pin	500 pin
Inner lead pitch	120µm	80µm
Outer lead pitch	180µm	140µm
Body thickness	1.3mm	0.8mm



64 x 3D-Flow Processors per board

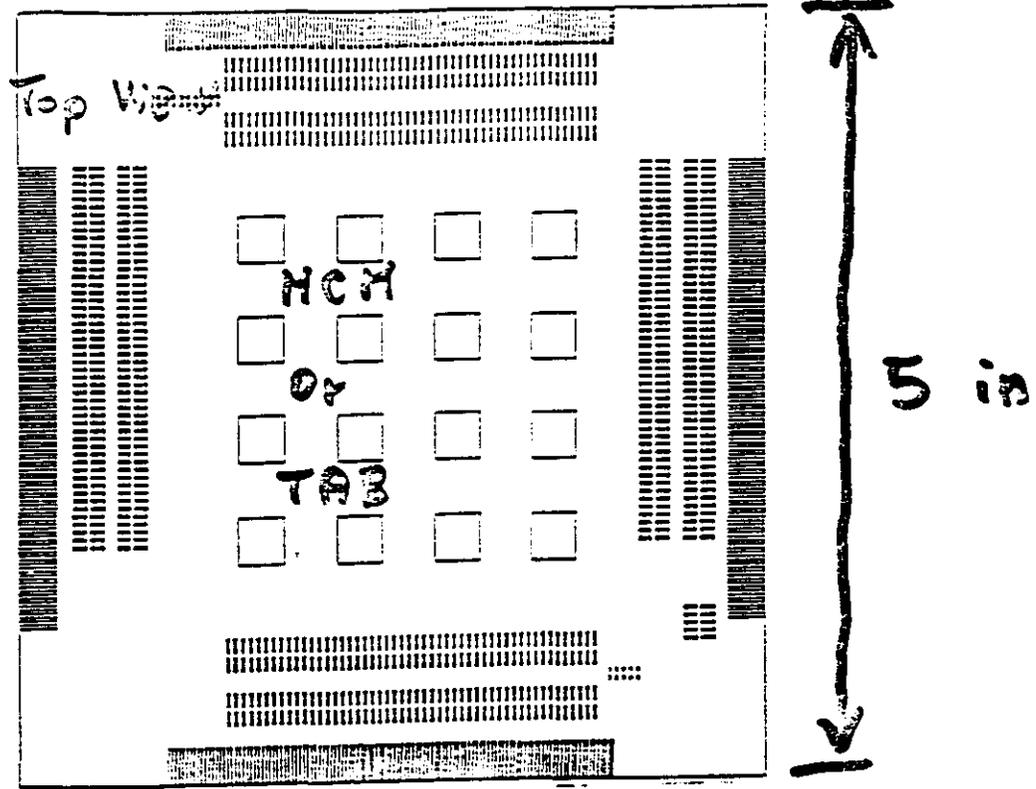


FIGURE 10. Board layout of sixteen 3D-Flow chips each containing 4 x 3D-Flow processors (Top view)

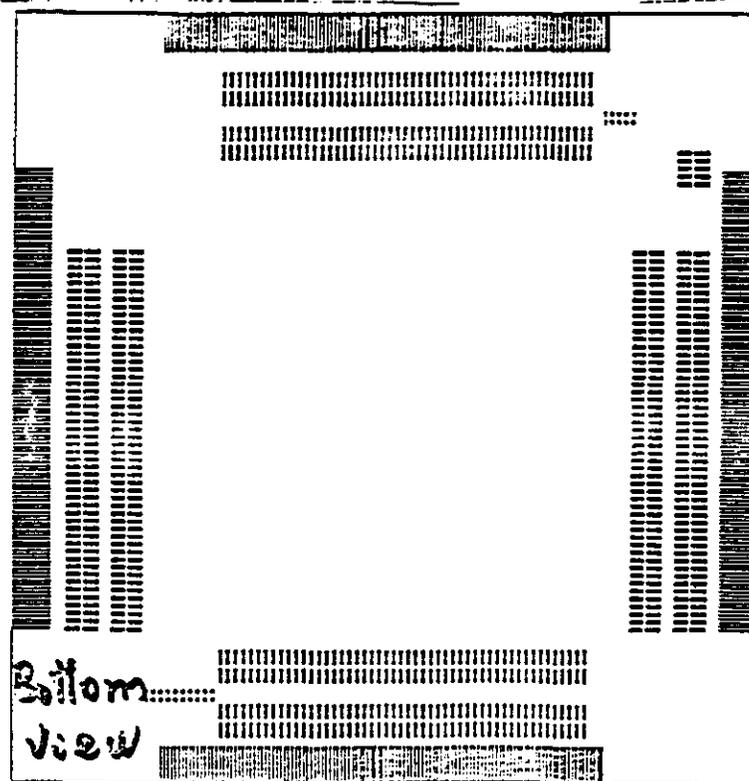


FIGURE 11. Board layout of sixteen 3D-Flow chips each containing 4 x 3D-Flow processors (Bottom view)

8

7

6

5

4

SEE DETAIL C
CONTACT (NEARSIDE) #1
CONTACT (FARSIDE) LAST

.250 MIN.
(BOTH SIDES)

R.063 (2X)

.200 ± .002
(BOTH SIDES)

(.025) CTC X NO. OF SPACES ± (DIM. "L")
TOLERANCE NON-ACCUMULATIVE (2X)

DIM. "M" ± .002

.040 (REF)
(BOTH SIDES) [2]

45°
(2X)

.320

THIS AREA TO BE
FREE OF SOLDERMASK
(BOTH SIDES)

.025 ± .001
(TYP)

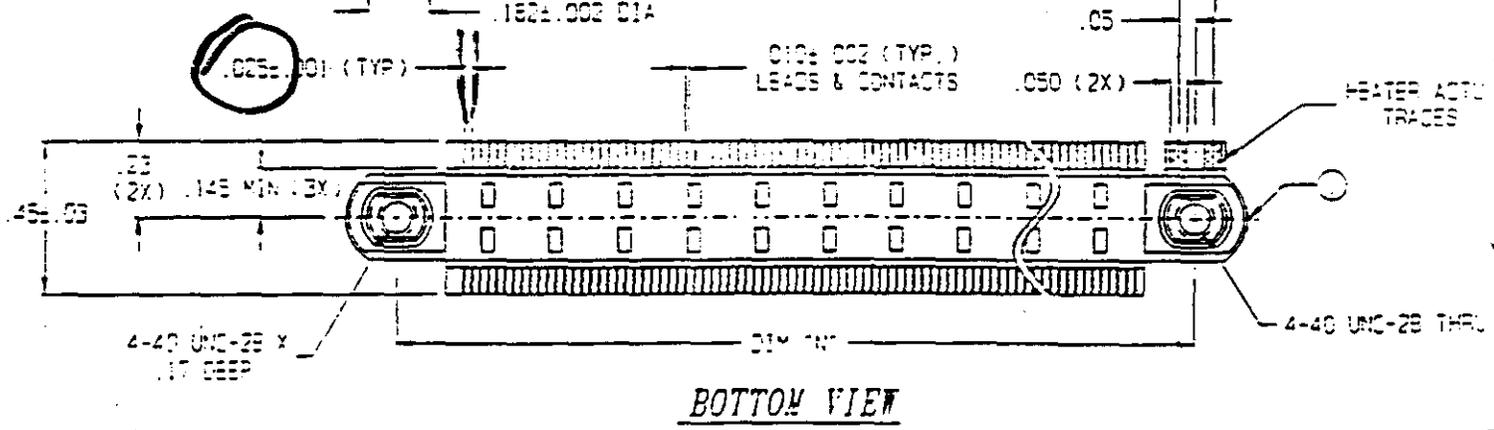
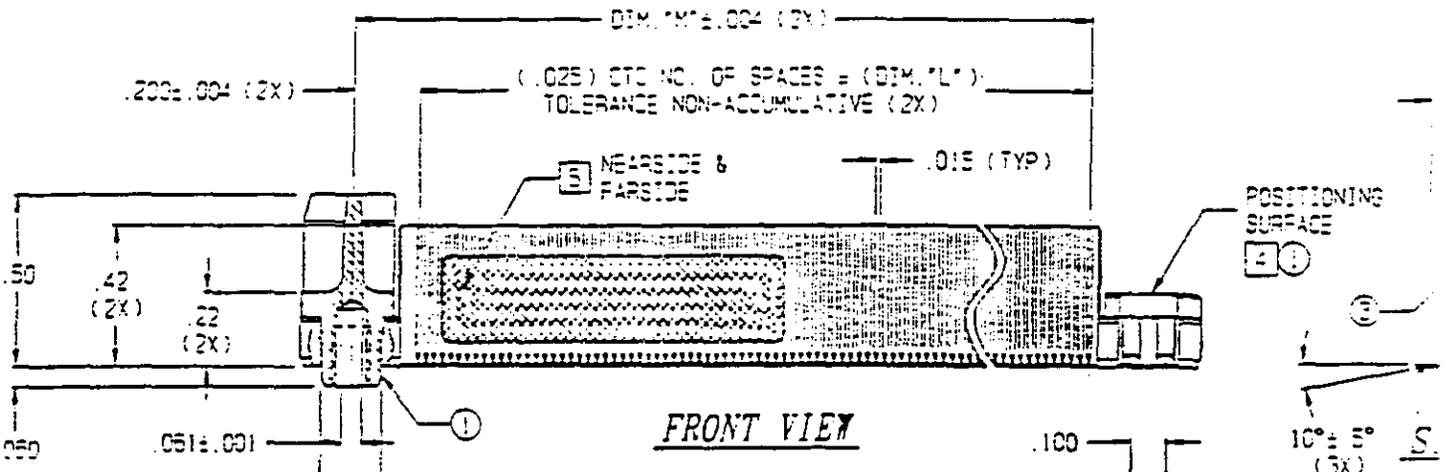
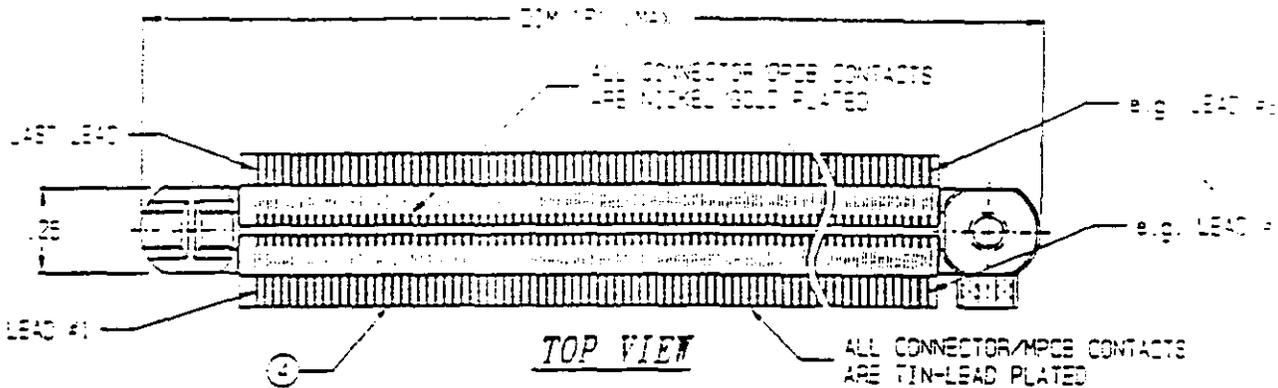
[2] (BOTH SIDES)

.0525 ± .0005
[2] ± .0005

.015 ± .001 (TYP)
[2] ± .0005

DETAIL
SCALE:

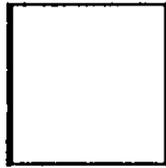
DETAIL C
SCALE NONE



PART ORDERING INFORMATION				BOARD THICKNESS RANGE	GAP DIM. "K"
PC	X	C25	177		
LENGTH	TRACE SPACING	NUMBER OF TRACES	BOARD THICKNESS	0.064 - 0.080	0.40
232					

COMPARISON, QFP WITH LGA

METRIC STANDARD
ARRAY CARRIER



21 mm BODY
1 mm pitch
324 I/Os, MAX.

0.8 mm pitch
444 I/Os, MAX.
AREA 0.62 In. sq.



Nickel

U.S. Five Cent Piece
21 mm Diameter



METRIC STANDARD
QFP

32 mm BODY
0.65 mm pitch
188 I/Os, MAX.

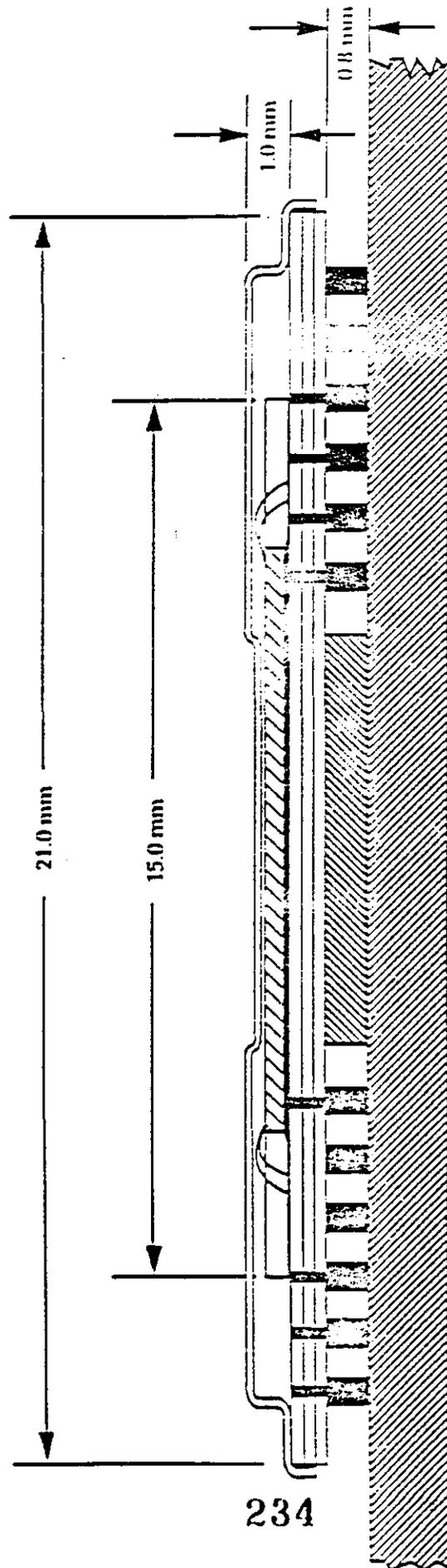
0.4 mm pitch
304 I/Os, MAX.
AREA 1.86 In. sq.

233

6 ROW DESIGN. 12 CORNER TERMINALS NOT USED

Figure 2

CROSS SECTION, 21 mm LGA



234

Figure 10

EFFECTIVENESS OF AREA ARRAY I/O'S

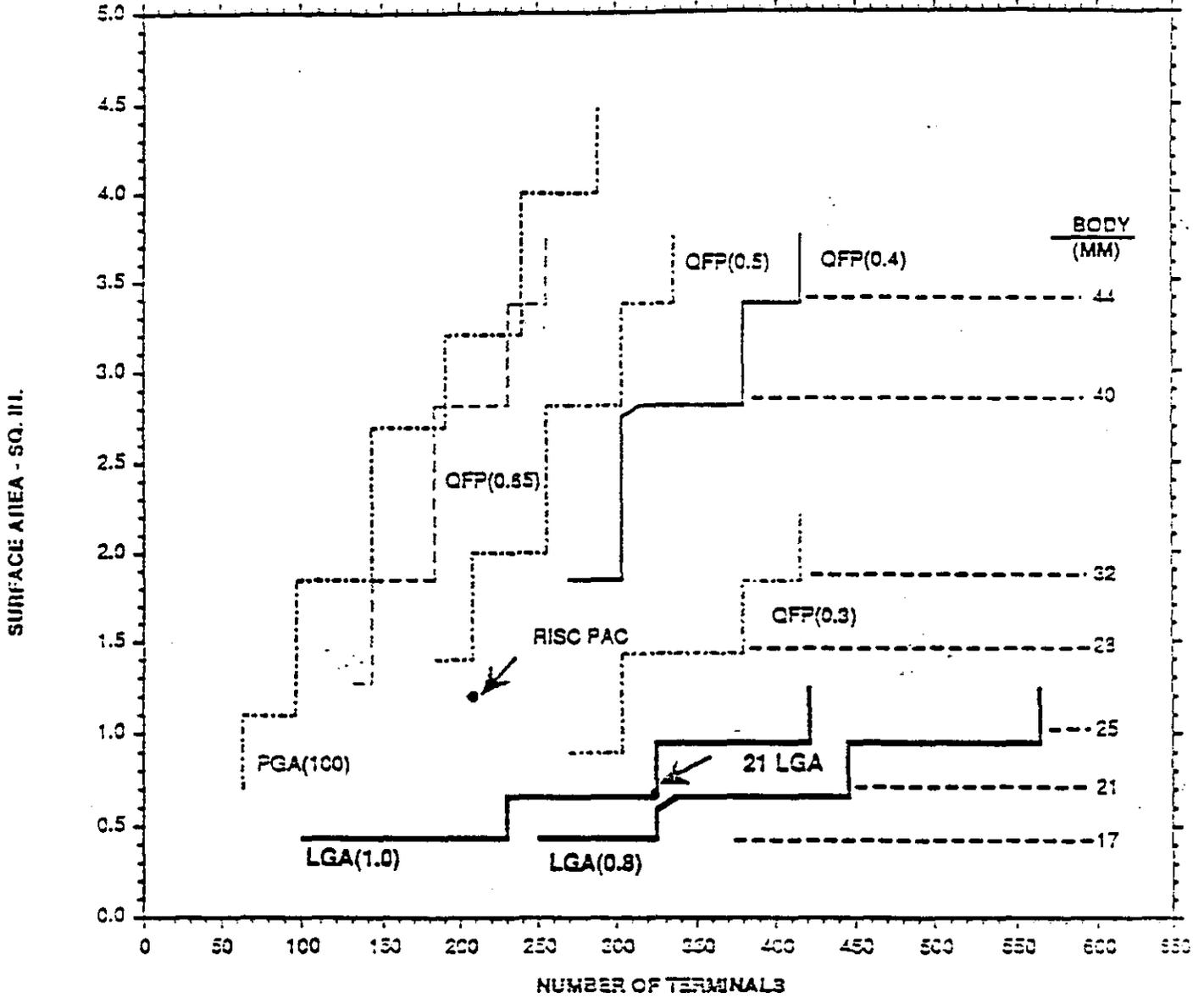


Figure 1
235

LAND GRID ARRAY SIGNAL CAPACITANCE

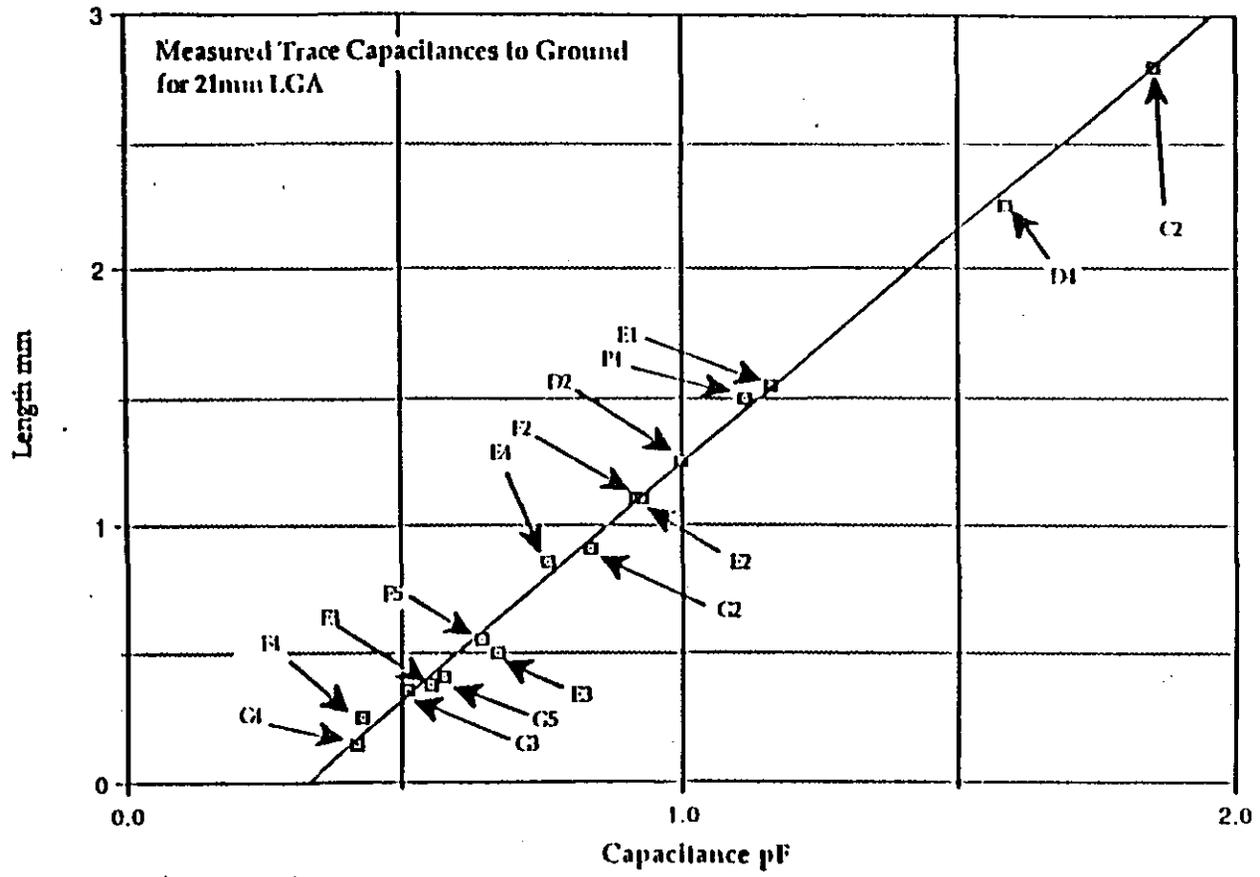


Figure 4

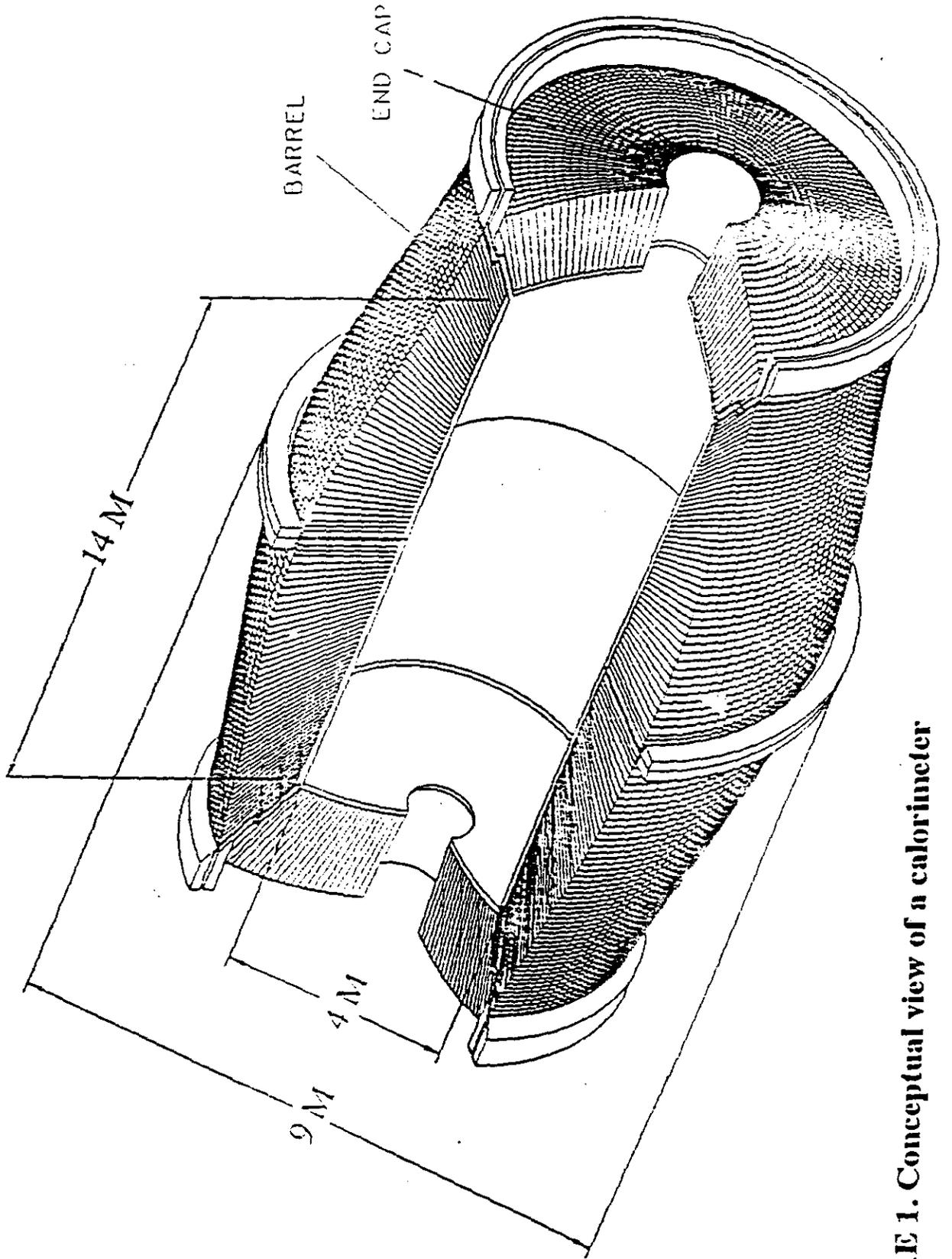


FIGURE 1. Conceptual view of a calorimeter

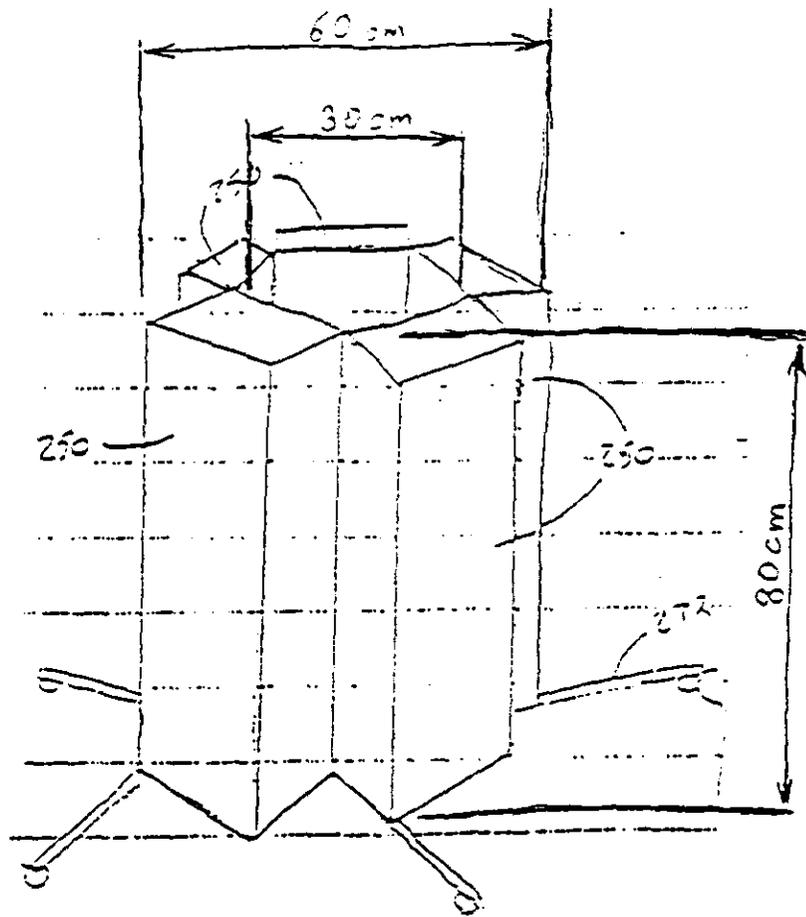


FIGURE 13. Dimension of a complete programmable Level-1 trigger for 1250 "Trigger Towers" using the 16 x 3D-Flow processors board assembly of Figures 8 and 9.

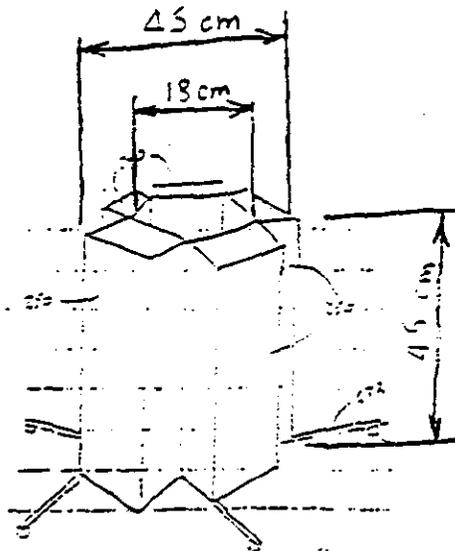
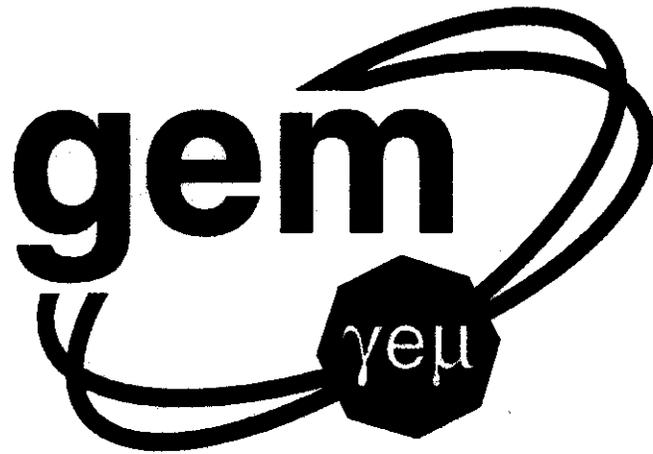


FIGURE 14. Dimension of a complete programmable Level-1 trigger for 1250 "Trigger Towers" using the 64 x 3D-Flow processors board assembly of Figures 10 and 11.



Muon Trigger

Maged Atiya

Comments on Muon Trigger Electronics Costing

- Approximate estimate of hardware
- Costing methodology
- Proposal for continuation of cost estimates

We will do only barrel and then multiply by some factor to be determined (but of order 2)

CSC Facts

The CSC chambers come in a stack of 4 chambers.

SL1 = 2 stacks of 4 each (irrelevant for the trigger)

SL2, SL3 = 1 stack each.

The average chamber is ~120 cm wide by ~300 cm long

Each chamber has 256 cathode strips ($\Delta\phi$)

Each chamber has 128 anode gangs (T0)

Assuming 48 sectors then each sector in SL2 and SL3 has an "average" chamber in stacks of 4 (in reality they are different in size and a bit smaller)

Assume that each of SL2 and SL3 has 8 chambers in Z

Note that the 48 sector is under consideration still by the mechanical engineers.

General comments on the muon trigger

Need to determine two parameters at the Level 1 trigger

- $\Delta\phi$ at the level of 2.0 cm in the barrel and 0.5 cm in the Endcap
- T0 (beam crossing time)

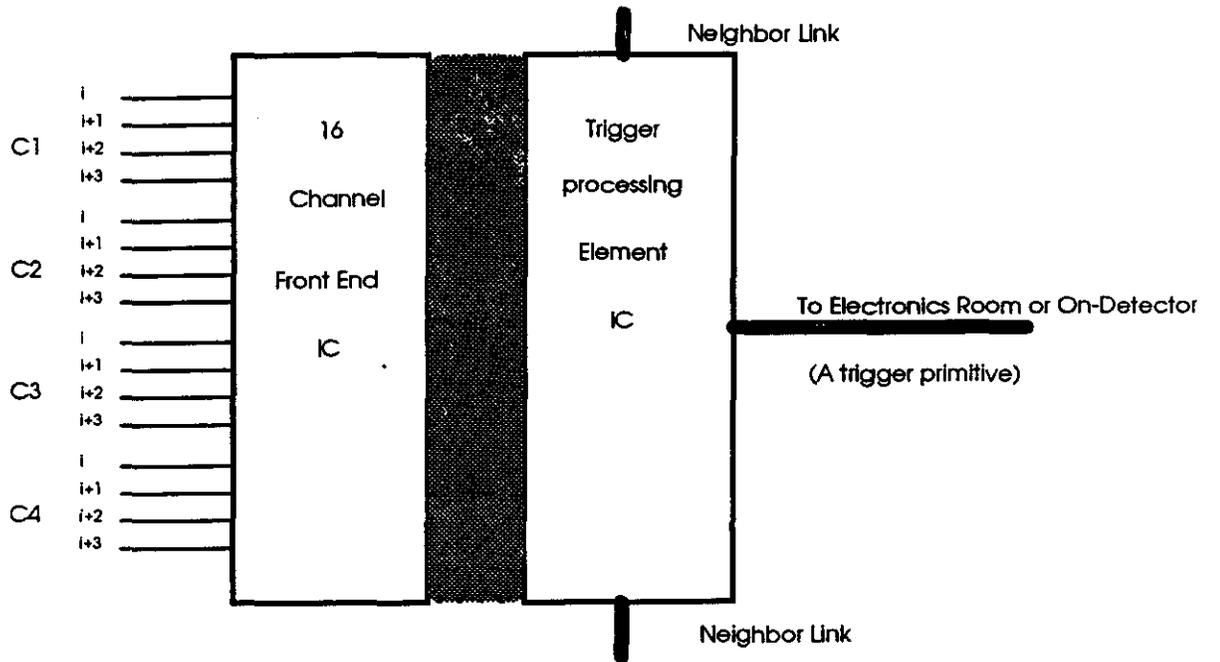
The number of barrel trigger segments is about 16000 and 20000

$$SL2 = (600*2*3.14)/2. = 2000*8 = 16000$$

$$SL3 = (800*2.*3.14)/2. = 2500*8 = 20000$$

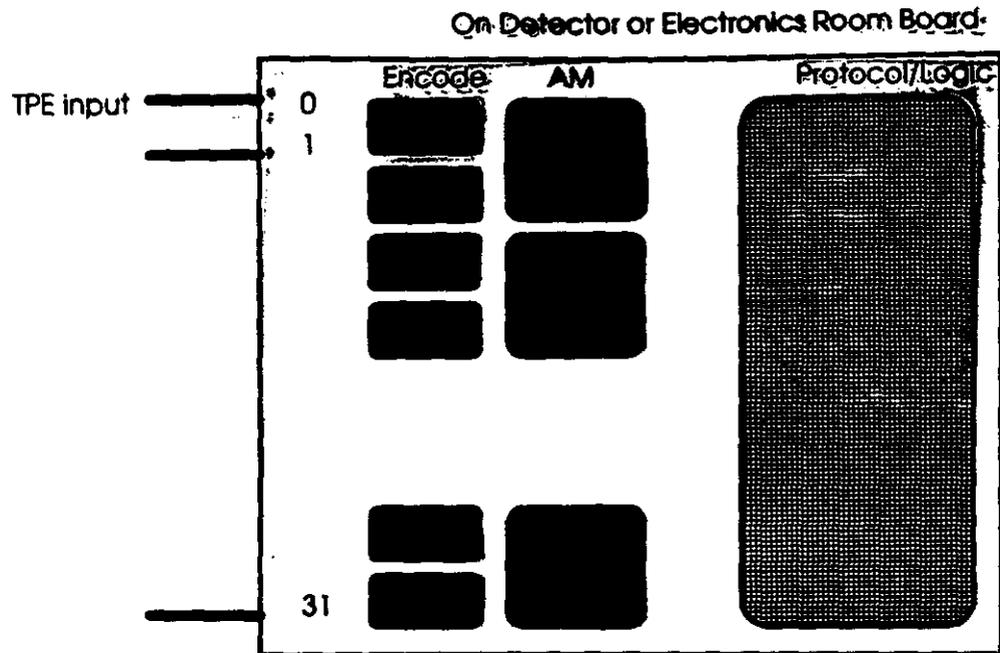
(assuming SL2 and SL3 triggers at 2.0 cm segments and 3/4 coincidence)

On Chamber Trigger Processing Unit (TPU)



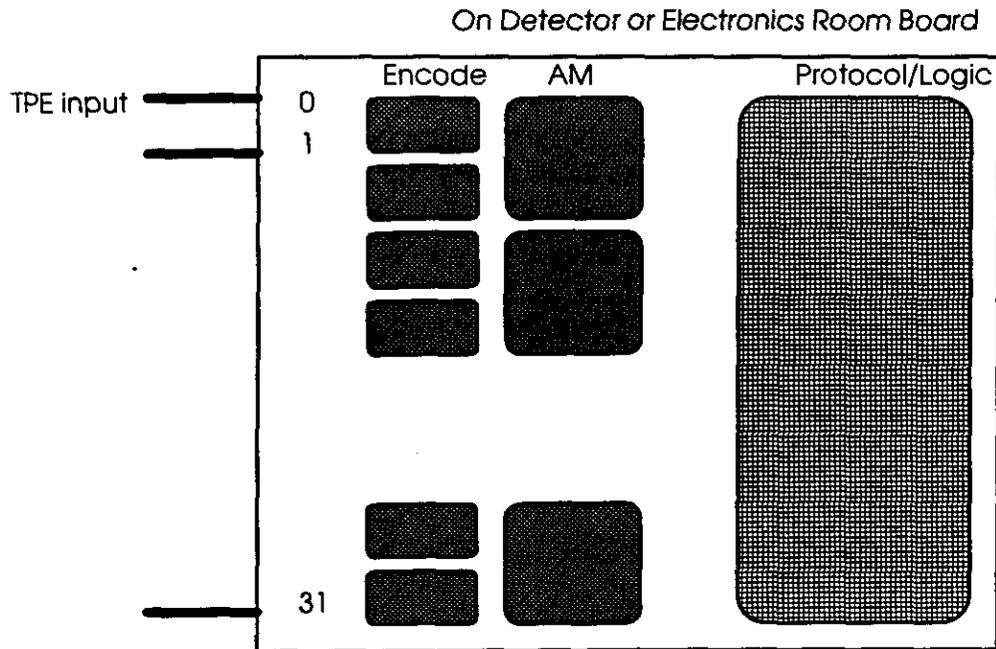
Total Count for TPU ~ 32,000

On Detector or Electronics Room Trigger Boards (TB)



Total count for TB = $32,000/32 \sim 1024$

On Detector or Electronics Room Trigger Boards (TB)



Total count for TB = $32,000/32 \sim 1024$

TB boards

1 crate per sector (48 crates).

Each crate has 22 boards (total ~1024)

Crate overhead

Crate

+5,-5,+2 V supplies

Crate Controller (Never in the history of HEP less than 5-10K)

Cost of complex Digital PC board (see graph)

Number of IC's on each TB board (*yet to be done*)

Miscellaneous logic (*yet to be done*)

System control and monitors (*yet to be done*)

Testing and debugging fixtures (*yet to be done*)

OOPS

T0 logic (?)

Cathode/anode correlation (?)

Level 1 overhead handling

DAQ overhead handling

TB boards

1 crate per sector (48 crates)

Each crate has 22 boards (total ~1024)

Crate overhead

Crate

+5,-5,+2 V supplies

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Cost of complex Digital PC board (see graph)

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System control and monitors (*yet to be done*)

Testing and debugging fixtures (*yet to be done*)

OOPS

T0 logic (?)

Cathode/anode correlation (?)

Level 1 overhead handling

DAQ overhead handling

The "Unofficial" costing rules

*Based entirely on recent experience with complex logic boards
Production runs 10-100*

Assume 4 years for design and construction
(FY 94-98)

Overhead

8 FTE Senior Engineers
12 FTE Junior Engineers
24 FTE interns
12 FTE technicians
Design Station support for 4 years

Design

6 month cycles per design
Overhead on a design is small (< \$100K)
A design is either an IC or a board.

Components

TPU is a small IC (or part of a medium IC)
TPU cable is 80 feet per 16 signals or \$5/signal
TPU connectors are \$4 per 16 signals

The "Unofficial" costing rules

*Based entirely on recent experience with complex logic boards.
Production runs 10-100*

Assume 4 years for design and construction
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24 FTE interns
12 FTE technicians
Design Station support for 4 years

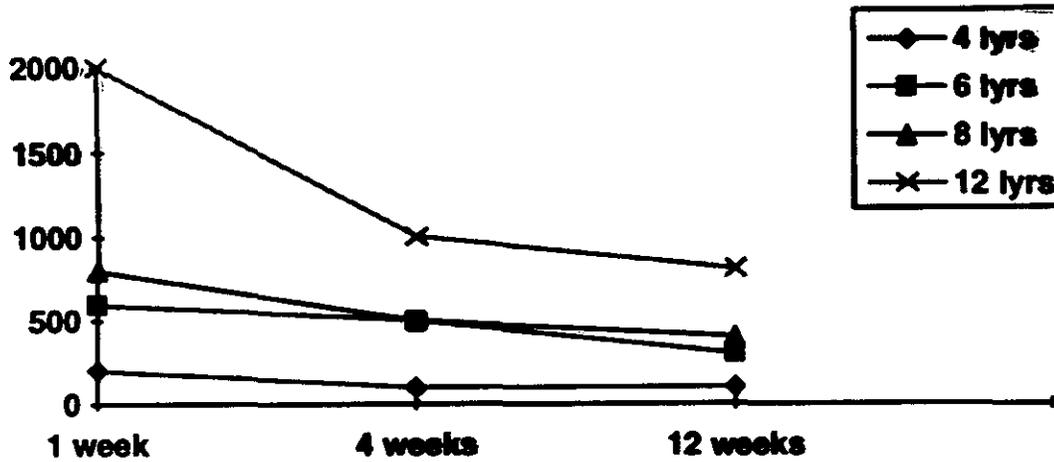
Design

6 month cycles per design
Overhead on a design is small (\ll \$100K) Typically 10K.
A design is either an IC or a board.

Components

TPU is a small IC (or part of a medium IC)
TPU cable is 80 feet per 16 signals or \$5/signal
TPU connectors are \$4 per 16 signals

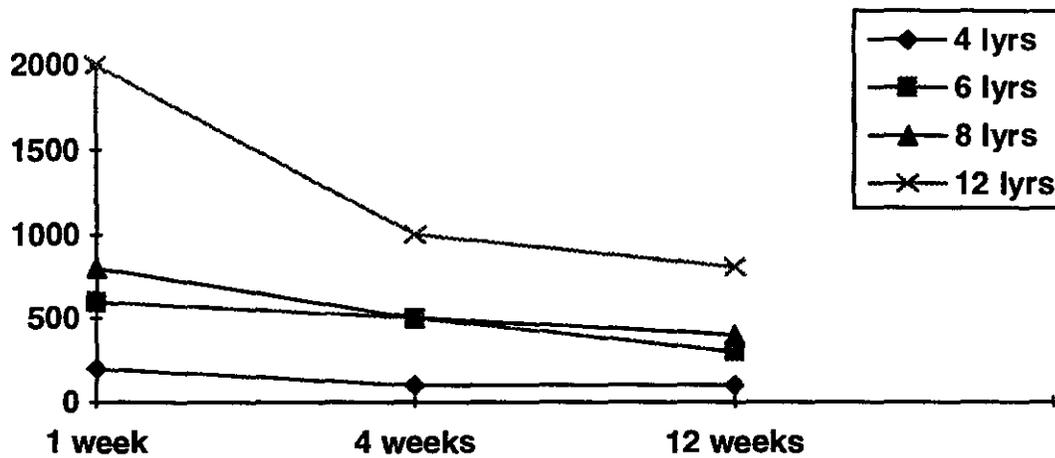
Cost of a FastBus size PC board (EDR V3.0)



Assembly costs for complex digital boards

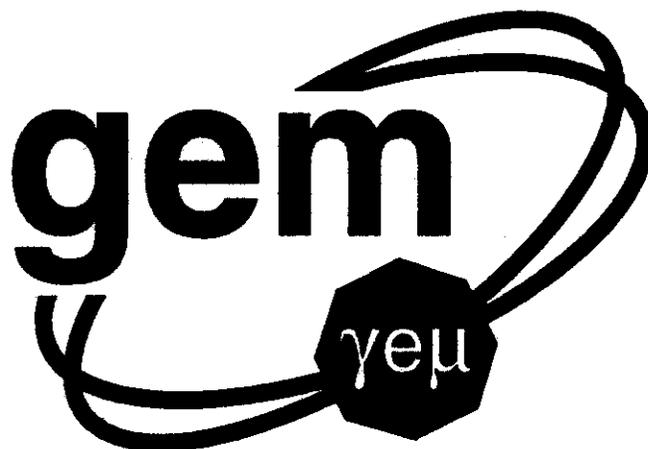
Automatic Soldering	\$200/FastBus size board
DC testing	0.25 FTE days/board
Functional testing	0.5-1 FTE days/board
Full debugging	0.2 FTE days/board
Mechanical + Misc.	0.2 FTE days/board

Cost of a FastBus size PC board (EDR V3.0)



Assembly costs for complex digital boards

Automatic Soldering	\$200/FastBus size board
DC testing	0.25 FTE days/board
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Mechanical + Misc.	0.2 FTE days/board



DAQ

Mark Bowden

6.x GEM Data Acquisition and Second Level Trigger Systems

6.x.1 Introduction

The Data Acquisition System is responsible for bringing the data for the relevant physics events to mass storage in an efficient way. It also provides the context in which the level 2 and level 3 triggers run and brings the data to these triggers.

A design goal specific to the GEM DAQ system is that all front-end chips are read after each level 1 trigger. This way no data has to be stored on the front-end chips during the level 2 decision. Only buffers of moderate size will be needed to de-randomize the level 1 trigger rate fluctuations. It also allows for level 2 implementations with large latency.

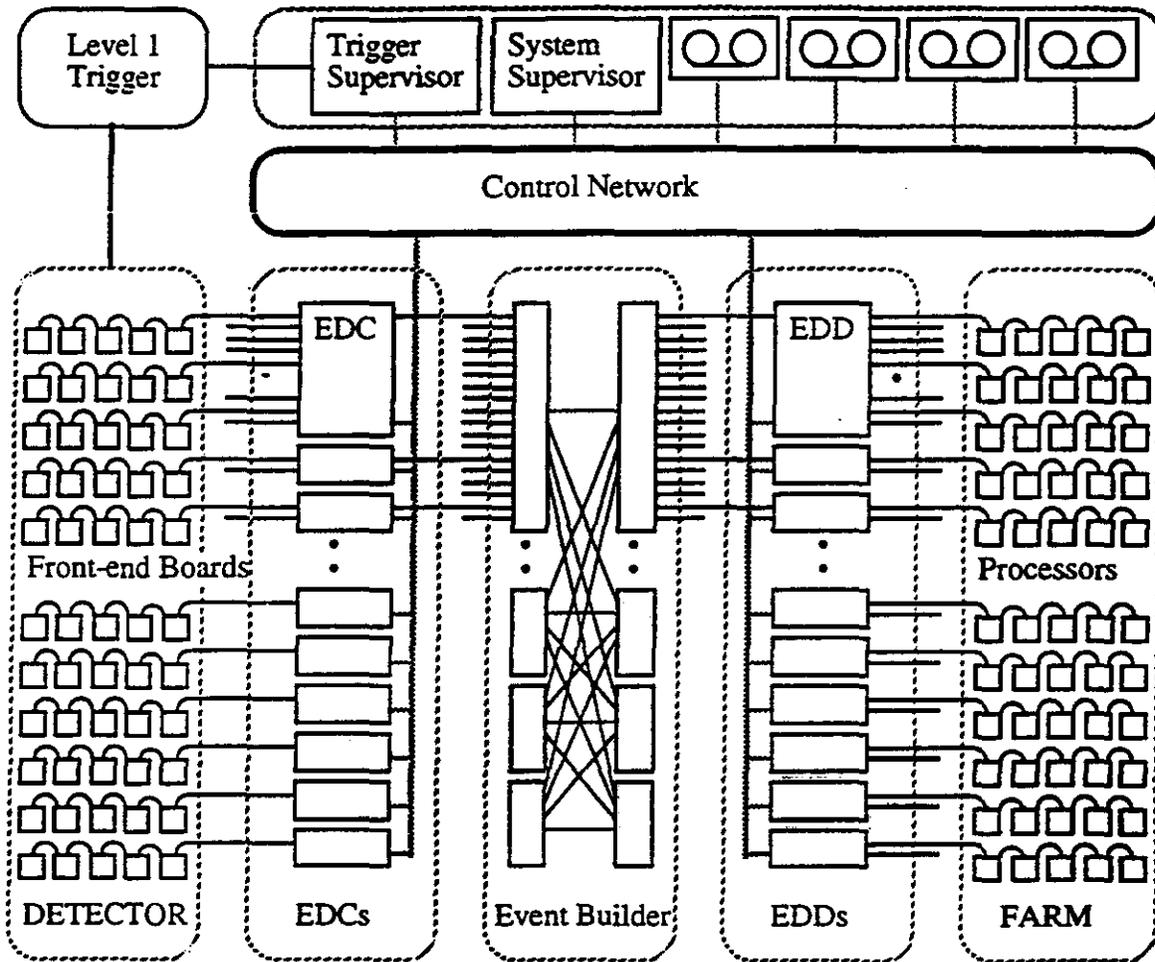
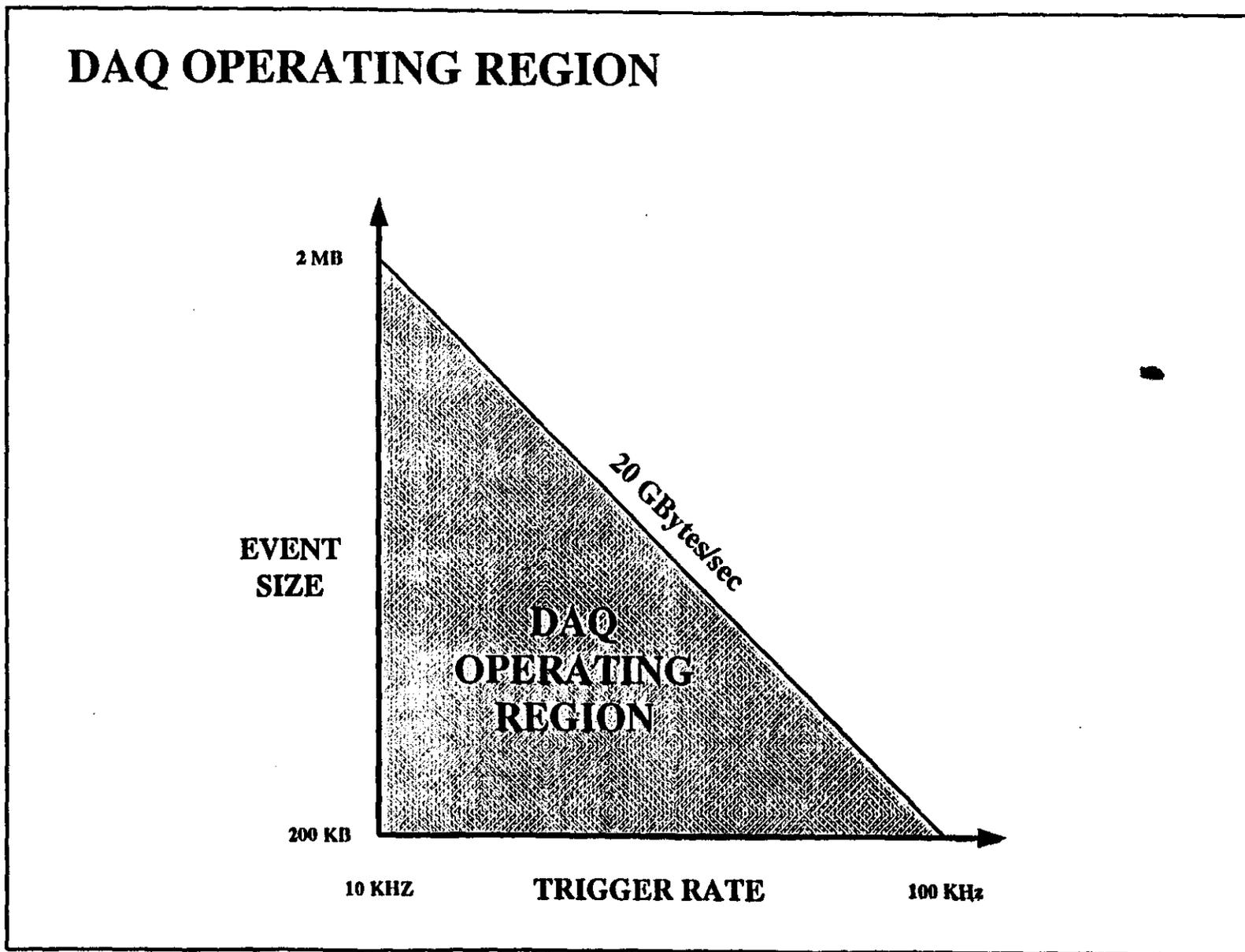
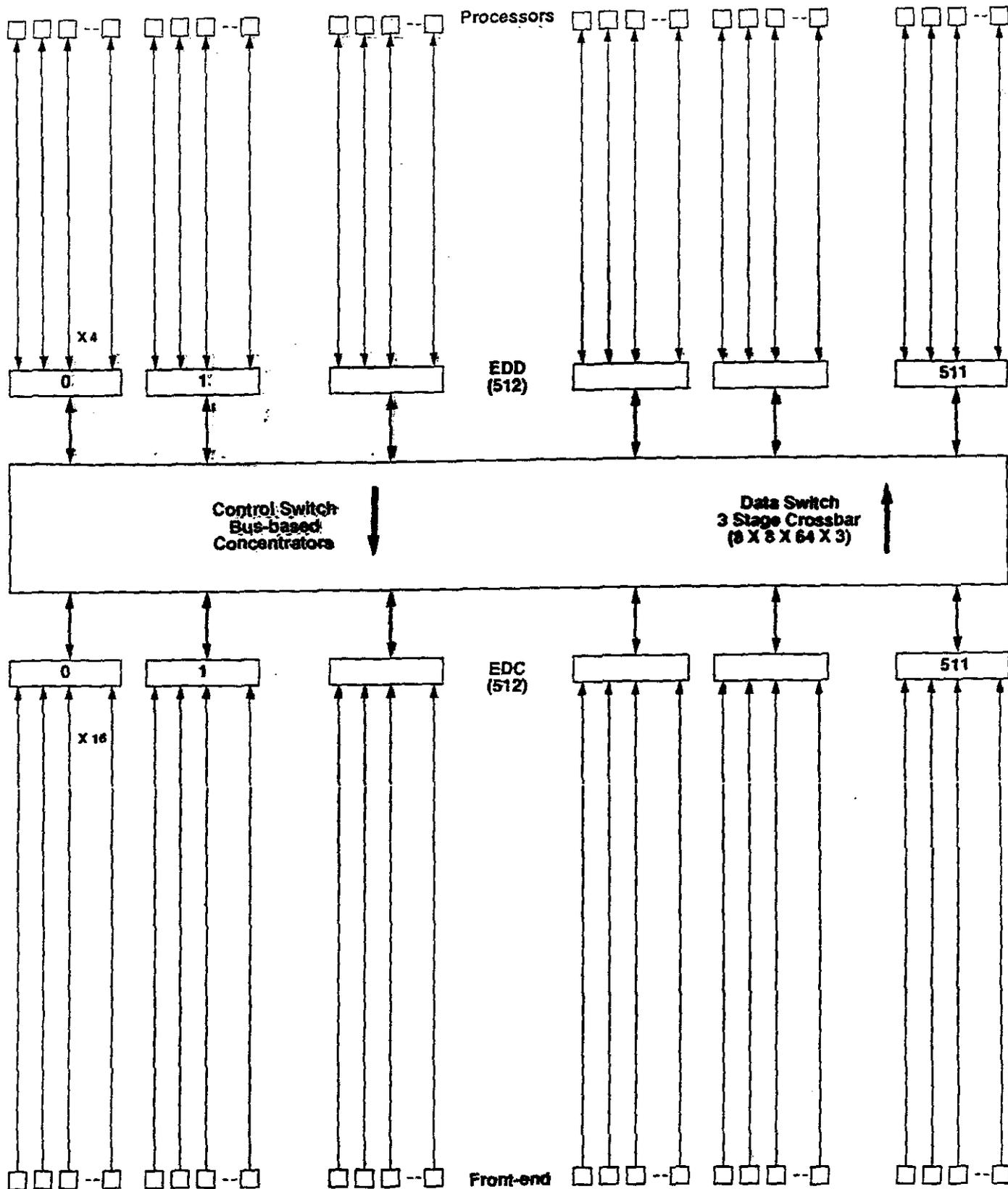


Figure 1. Overview of the GEM DAQ system

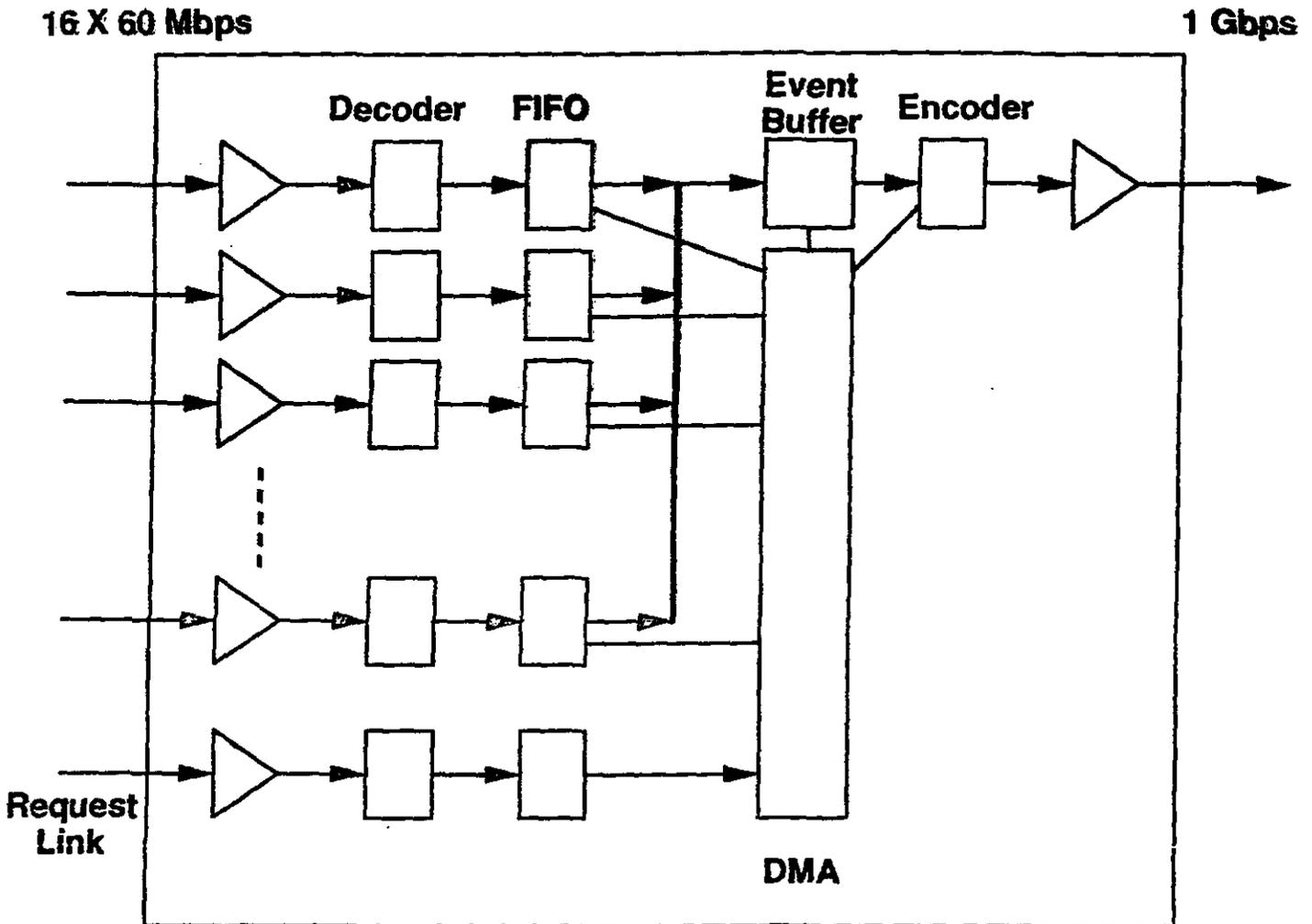
The level 2 and 3 algorithms will be executed in the general purpose processors of the on-line farm. Hence, the event data must be transported to the farm at rates up to the maximum specified level 1 trigger rate of 100 kHz. It also means that there are basically





Crossbar DAQ System (20 GByte/sec)

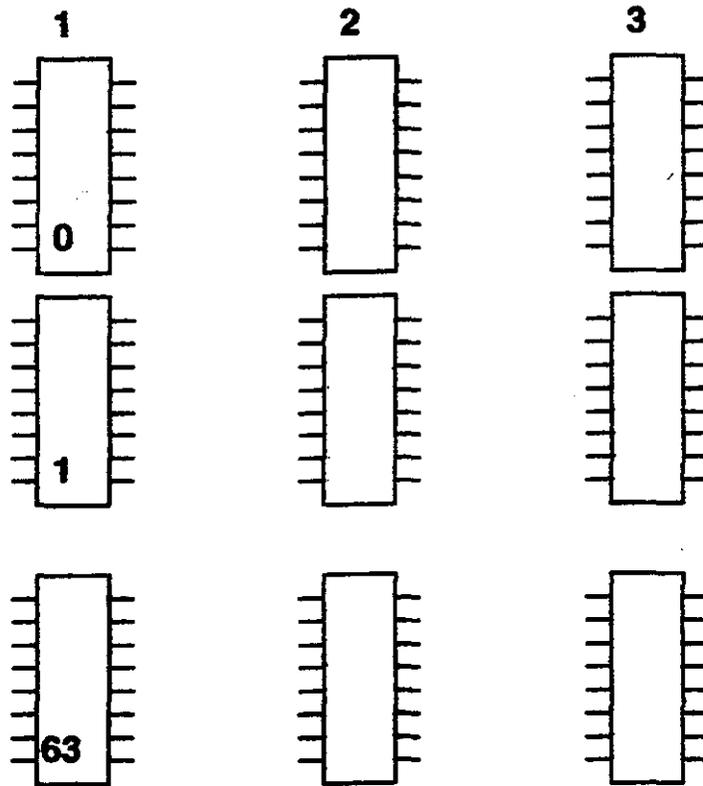
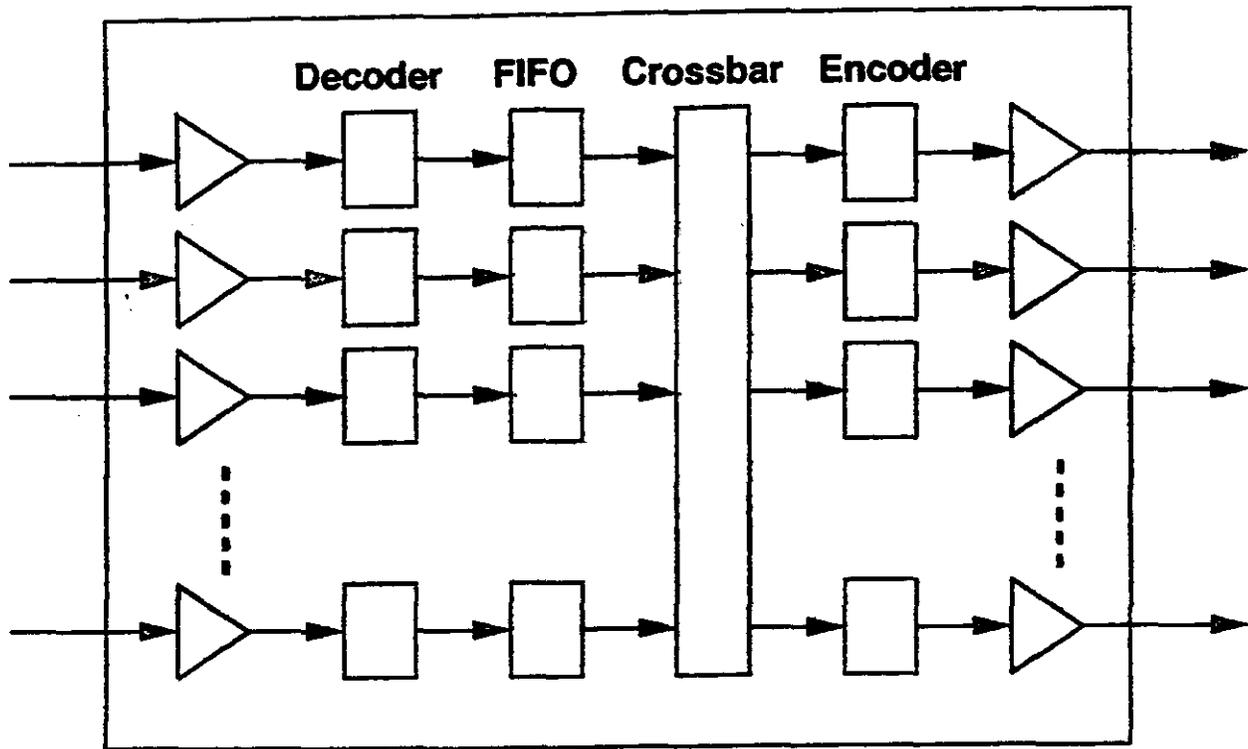
Event Data Collector



Event Buffer

$600 \text{ Bytes} \times 100 \text{ KHz} \times 1 \text{ sec} = 60 \text{ Mbytes (64 MBytes)}$

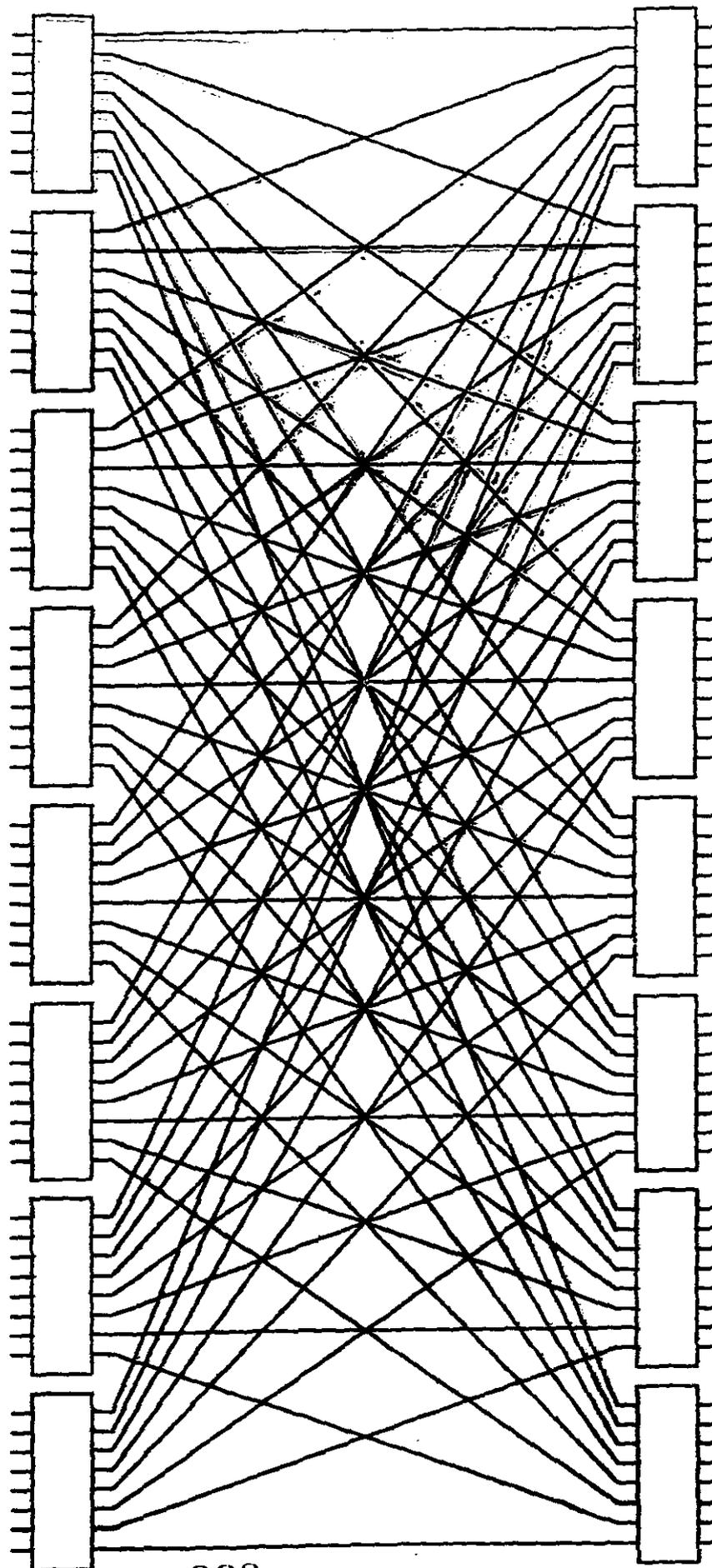
Crossbar Switch



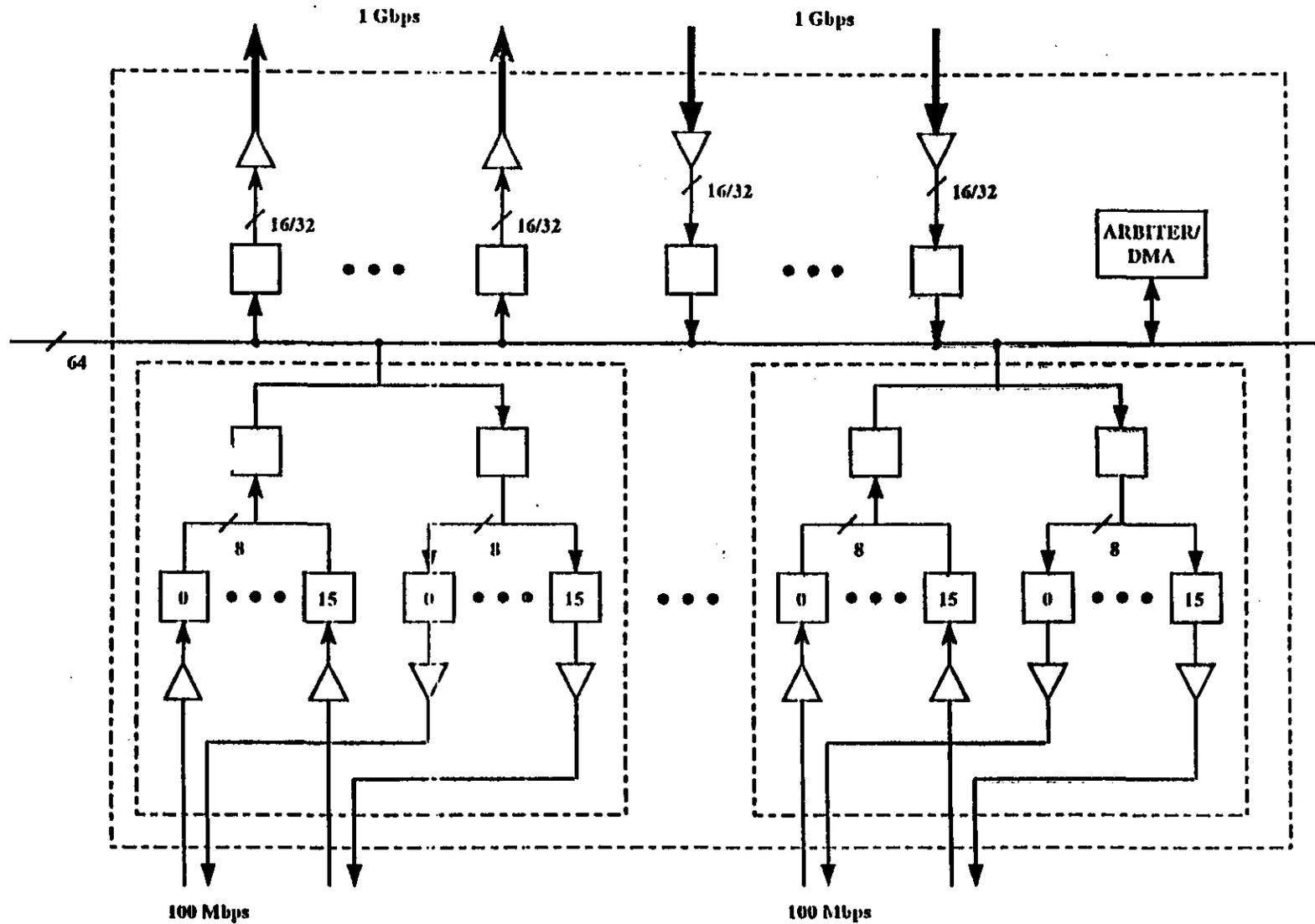
**512 X 512
= 192 Modules**

261

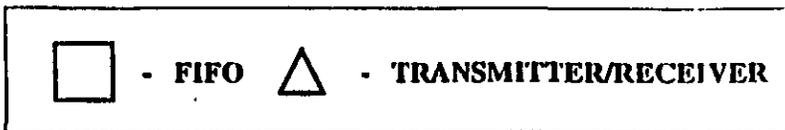
64 X 64 Switch



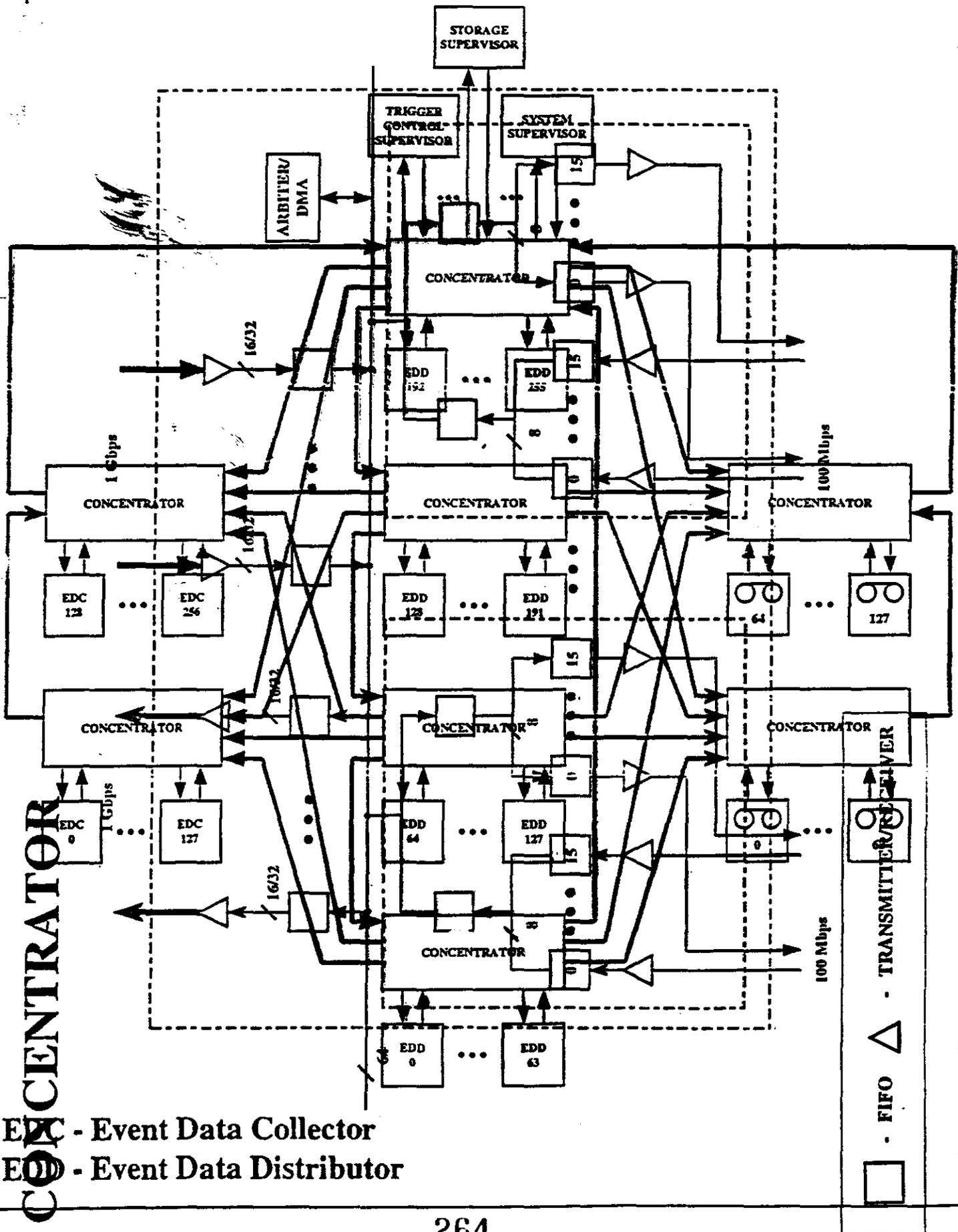
CONCENTRATOR



263



CONTROL NETWORK



VERY PRELIMINARY

265

	Funct Code	Item Description	QTY	UM	CRAFT	RATE	LAB(m)	LABOR	MATERIAL	L&M	TYPE
50.3.		XBAR DAQ System								9513.25	
50.3.x.y	ENG	Design & Simulation	1.5	MY		113	1.5	169.5	0	169.5	
50.3.x.y	M&S	Design & Simulation	1	LS		0	0	0	40	40	
50.3.x.y	ENG	Layout	0.5	MY		113	0.5	56.5	0	56.5	
50.3.x.y	M&S	Layout	1	LS		0	0	0	30	30	
50.3.x.y	ENG	Bld Package	0.25	MY		44	0.25	11	0	11	
50.3.x.y	M&S	Bld Package	1	LS		0	0	0	2	2	
50.3.x.y	P/F	Procurement	1	LS		0	0	0	2633	2633	
50.3.x.y	ENG	Software Development	1	MY		69	1	69	0	69	
50.3.x.y	M&S	Software Development	1	LS		0	0	0	40	40	
50.3.x.y	I&A	Testing	0.75	MY		69	0.75	51.75	0	51.75	
50.3.x.y	P/F	Testing	1	LS		0	0	0	40	40	
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75	
50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	15	15	
50.3.x		EDC TOTAL					4.75	442.5	2800	3242.5	
50.3.x.y	ENG	Design & Simulation	1.5	MY		113	1.5	169.5	0	169.5	
50.3.x.y	M&S	Design & Simulation	1	LS		0	0	0	20	20	
50.3.x.y	ENG	Layout	0.5	MY		113	0.5	56.5	0	56.5	
50.3.x.y	M&S	Layout	1	LS		0	0	0	10	10	
50.3.x.y	ENG	Bld Package	0.25	MY		44	0.25	11	0	11	
50.3.x.y	M&S	Bld Package	1	LS		0	0	0	2	2	
50.3.x.y	P/F	Procurement	1	LS		0	0	0	815	815	
50.3.x.y	ENG	Software Development	1	MY		69	1	69	0	69	
50.3.x.y	M&S	Software Development	1	LS		0	0	0	25	25	
50.3.x.y	I&A	Testing	0.75	MY		113	0.75	84.75	0	84.75	
50.3.x.y	P/F	Teating	1	LS		0	0	0	40	40	
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75	

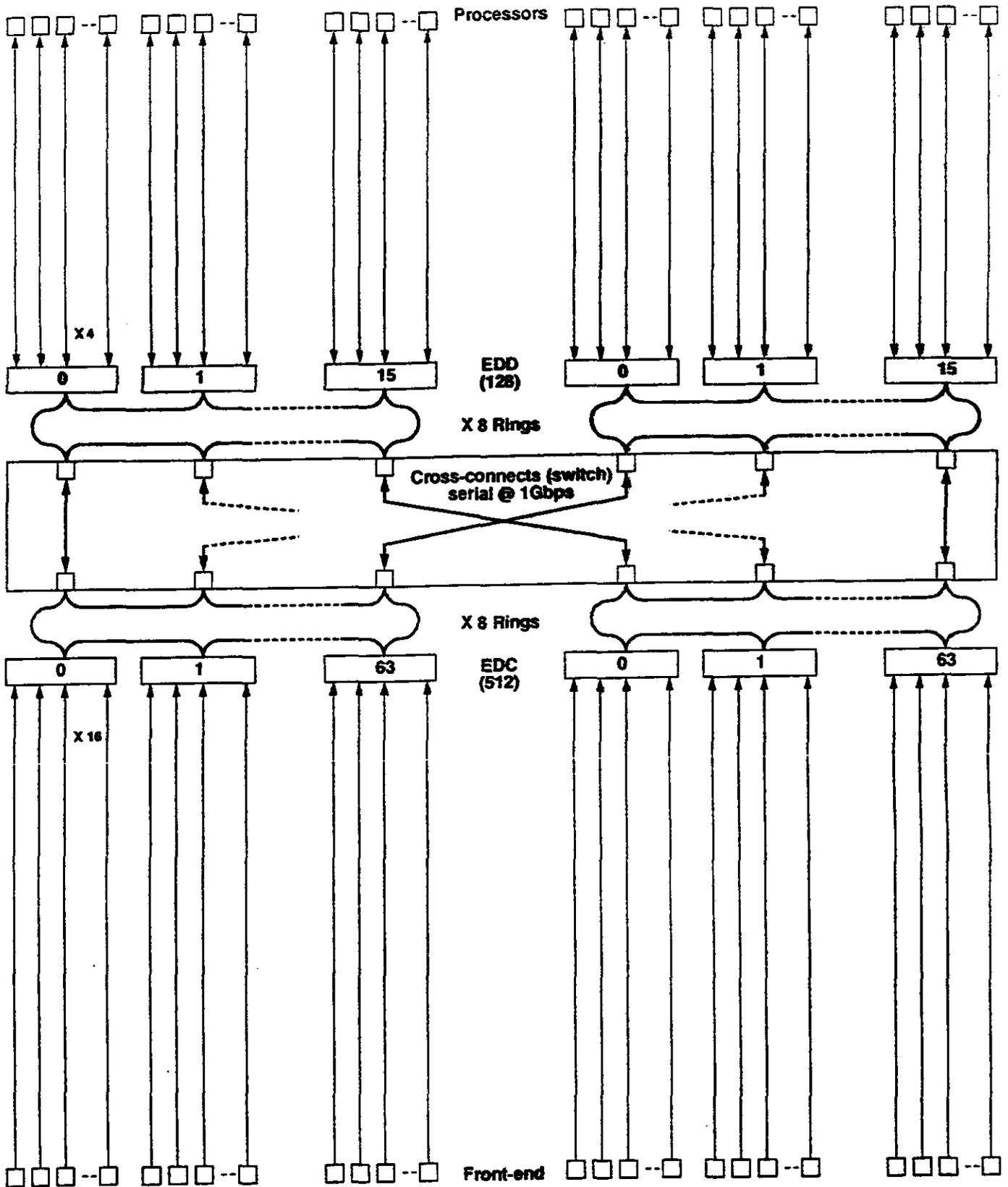
GEM (XBAR) DAQ WBS

266

50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	15	15
50.3.x		Switch TOTAL					4.75	475.5	927	1402.5
50.3.x.y	ENG	Design & Simulation	1.5	MY		113	1.5	169.5	0	169.5
50.3.x.y	M&S	Design & Simulation	1	LS		0	0	0	20	20
50.3.x.y	ENG	Layout	0.5	MY		113	0.5	56.5	0	56.5
50.3.x.y	M&S	Layout	1	LS		0	0	0	10	10
50.3.x.y	ENG	Bld Package	0.25	MY		44	0.25	11	0	11
50.3.x.y	M&S	Bld Package	1	LS		0	0	0	2	2
50.3.x.y	P/F	Procurement	1	LS		0	0	0	2633	2633
50.3.x.y	ENG	Software Development	1	MY		69	1	69	0	69
50.3.x.y	M&S	Software Development	1	LS		0	0	0	25	25
50.3.x.y	I&A	Testing	0.75	MY		113	0.75	84.75	0	84.75
50.3.x.y	P/F	Testing	1	LS		0	0	0	40	40
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75
50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	15	15
50.3.x		EDD TOTAL					4.75	475.5	2745	3220.5
50.3.x.y	ENG	Design & Simulation	0.5	MY		113	0.5	56.5	0	56.5
50.3.x.y	M&S	Design & Simulation	1	LS		0	0	0	0	0
50.3.x.y	ENG	Software Development	1	MY		69	1	69	0	69
50.3.x.y	M&S	Software Development	1	LS		0	0	0	1	1
50.3.x.y	I&A	Testing	0.75	MY		113	0.75	84.75	0	84.75
50.3.x.y	P/F	Testing	1	LS		0	0	0	5	5
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75
50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	5	5
50.3.x		Trig Supervisor TOTAL					3	295	11	306
50.3.x.y	ENG	Design & Simulation	0.5	MY		113	0.5	56.5	0	56.5
50.3.x.y	M&S	Design & Simulation	1	LS		0	0	0	0	0
50.3.x.y	P/F	Procurement	1	LS		0	0	0	40	40
50.3.x.y	ENG	Software Development	2	MY		69	2	138	0	138

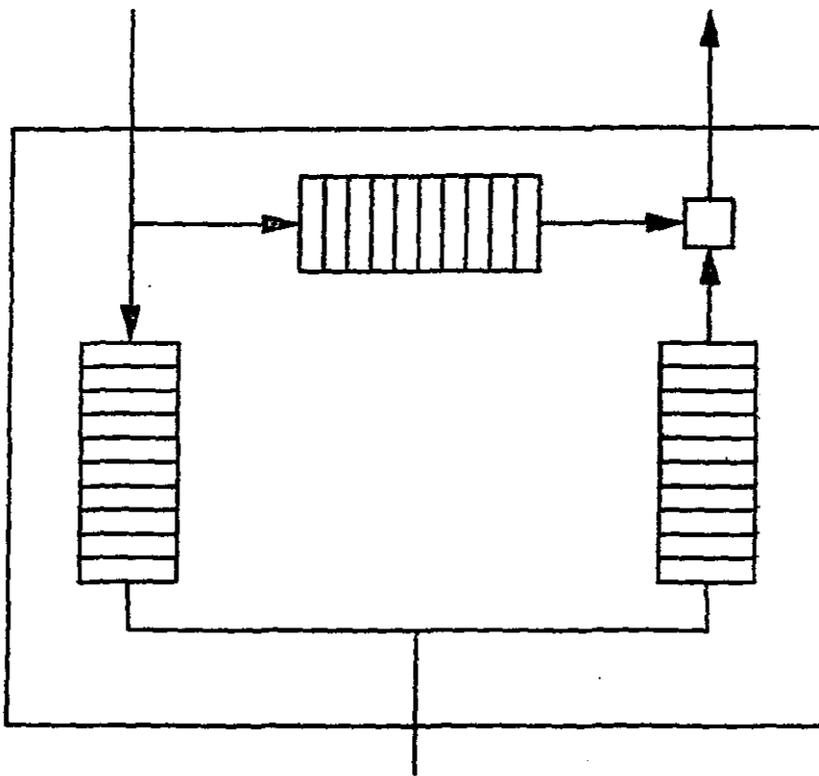
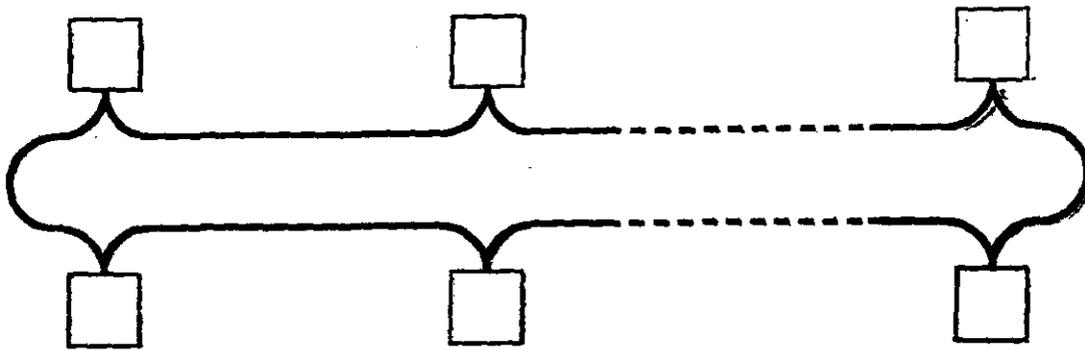
GEM (XBAR) DAQ WBS

50.3.x.y	M&S	Software Development	1	LS		0	0	0	1	1
50.3.x.y	I&A	Testing	1	MY		113	1	113	0	113
50.3.x.y	P/F	Testing	1	LS		0	0	0	5	5
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75
50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	5	5
50.3.x		Control System TOTAL					4.25	392.25	51	443.25
50.3.x.y	ENG	Design & Simulation	1.5	MY		113	1.5	169.5	0	169.5
50.3.x.y	M&S	Design & Simulation	1	LS		0	0	0	20	20
50.3.x.y	ENG	Layout	0.5	MY		113	0.5	56.5	0	56.5
50.3.x.y	M&S	Layout	1	LS		0	0	0	10	10
50.3.x.y	ENG	Bid Package	0.25	MY		44	0.25	11	0	11
50.3.x.y	M&S	Bid Package	1	LS		0	0	0	2	2
50.3.x.y	P/F	Procurement	1	LS		0	0	0	311	311
50.3.x.y	ENG	Software Development	1	MY		69	1	69	0	69
50.3.x.y	M&S	Software Development	1	LS		0	0	0	25	25
50.3.x.y	I&A	Testing	0.75	MY		113	0.75	84.75	0	84.75
50.3.x.y	P/F	Testing	1	LS		0	0	0	40	40
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75
50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	15	15
50.3.x		Data Req Network TOTAL					4.75	475.5	423	898.5



SCI DAQ System (5 GByte/sec)

SCI Interface



Request Latency (empty ring)

First Ring.....72 Nodes X 16 Bytes X 1 nsec/Byte = 1.2 μ sec

Cross-connect.....16 Bytes X 10 nsec/Byte = 0.2 μ sec

Second Ring.....72 Nodes X 16 Bytes X 1 nsec/Byte = 1.2 μ sec

GEM (SCI) DAQ WBS

	Funct Code	Item Description	QTY	UM	CRAFT	RATE	LAB(m)	LABOR	MATERIAL	L&M	TYPE
50.3.		SCI DAQ System								6133.75	
50.3.x.y	ENG	Design & Simulation	1.5	MY		113	1.5	169.5	0	169.5	
50.3.x.y	M&S	Design & Simulation	1	LS		0	0	0	40	40	
50.3.x.y	ENG	Layout	0.5	MY		113	0.5	56.5	0	56.5	
50.3.x.y	M&S	Layout	1	LS		0	0	0	30	30	
50.3.x.y	ENG	Bid Package	0.25	MY		44	0.25	11	0	11	
50.3.x.y	M&S	Bid Package	1	LS		0	0	0	2	2	
50.3.x.y	P/F	Procurement	1	LS		0	0	0	2483	2483	
50.3.x.y	ENG	Software Development	1	MY		69	1	69	0	69	
50.3.x.y	M&S	Software Development	1	LS		0	0	0	40	40	
50.3.x.y	I&A	Testing	0.75	MY		69	0.75	51.75	0	51.75	
50.3.x.y	P/F	Testing	1	LS		0	0	0	40	40	
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75	
50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	15	15	
50.3.x		EDC TOTAL					4.75	442.5	2650	3092.5	
50.3.x.y	ENG	Design & Simulation	1.5	MY		113	1.5	169.5	0	169.5	
50.3.x.y	M&S	Design & Simulation	1	LS		0	0	0	20	20	
50.3.x.y	ENG	Layout	0.5	MY		113	0.5	56.5	0	56.5	
50.3.x.y	M&S	Layout	1	LS		0	0	0	10	10	
50.3.x.y	ENG	Bid Package	0.25	MY		44	0.25	11	0	11	
50.3.x.y	M&S	Bid Package	1	LS		0	0	0	2	2	
50.3.x.y	P/F	Procurement	1	LS		0	0	0	435	435	
50.3.x.y	ENG	Software Development	1	MY		69	1	69	0	69	
50.3.x.y	M&S	Software Development	1	LS		0	0	0	25	25	
50.3.x.y	I&A	Testing	0.75	MY		113	0.75	84.75	0	84.75	
50.3.x.y	P/F	Testing	1	LS		0	0	0	40	40	
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75	

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		cost	number	total
50.3.	SCI DAQ System			
50.3.x	EDC	4850	512	2483200
50.3.x.y	Link Receiver	50	16	800
50.3.x.y	Link Decoder	30	16	480
50.3.x.y	Link FIFO	60	16	960
50.3.x.y	Link DMA	30	16	480
50.3.x.y	SCI Interface	400	1	400
50.3.x.y	SCI DMA	80	1	80
50.3.x.y	SCI Control	200	1	200
50.3.x.y	Buffer DRAM	100	8	800
50.3.x.y	PC Board	200	1	200
50.3.x.y	SCI Cable	50	1	50
50.3.x.y	crate/power	6400	0.0625	400
50.3.x	SCI Switch	434560	1	434560
50.3.x.y	Link Decoder	200	256	51200
50.3.x.y	Link Encoder	200	256	51200
50.3.x.y	SCI Interface	400	512	204800
50.3.x.y	SCI FIFO	100	512	51200
50.3.x.y	SCI DMA	80	512	40960
50.3.x.y	PC Board	200	64	12800
50.3.x.y	SCI Cable	50	64	3200
50.3.x.y	crate/power	6400	3	19200
50.3.x	EDD	5330	128	682240
50.3.x.y	Link Transceiver	500	4	2000
50.3.x.y	Link FIFO	100	8	800
50.3.x.y	Link DMA	50	8	400
50.3.x.y	SCI Interface	400	1	400
50.3.x.y	SCI DMA	80	1	80
50.3.x.y	SCI Control	200	1	200
50.3.x.y	PC Board	200	1	200
50.3.x.y	SCI Cable	50	1	50
50.3.x.y	Fiber	1	800	800
50.3.x.y	crate/power	6400	0.0625	400

GEM (SCI) DAQ WBS

50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	15	15
50.3.x		Switch TOTAL				4.75	475.5		547	1022.5
50.3.x.y	ENG	Design & Simulation	1.5	MY	113	1.5	189.5	0		189.5
50.3.x.y	M&S	Design & Simulation	1	LS	0	0	0	20		20
50.3.x.y	ENG	Layout	0.5	MY	113	0.5	56.5	0		56.5
50.3.x.y	M&S	Layout	1	LS	0	0	0	10		10
50.3.x.y	ENG	Bld Package	0.25	MY	44	0.25	11	0		11
50.3.x.y	M&S	Bld Package	1	LS	0	0	0	2		2
50.3.x.y	P/F	Procurement	1	LS	0	0	0	682		682
50.3.x.y	ENG	Software Development	1	MY	69	1	69	0		69
50.3.x.y	M&S	Software Development	1	LS	0	0	0	25		25
50.3.x.y	I&A	Testing	0.75	MY	113	0.75	84.75	0		84.75
50.3.x.y	P/F	Testing	1	LS	0	0	0	40		40
50.3.x.y	ENG	Prototype Setup	0.75	MY	113	0.75	84.75	0		84.75
50.3.x.y	M&S	Prototype Setup	1	LS	0	0	0	15		15
50.3.x		EDD TOTAL				4.75	475.5		794	1269.5
50.3.x.y	ENG	Design & Simulation	0.5	MY	113	0.5	56.5	0		56.5
50.3.x.y	M&S	Design & Simulation	1	LS	0	0	0	0		0
50.3.x.y	ENG	Software Development	1	MY	69	1	69	0		69
50.3.x.y	M&S	Software Development	1	LS	0	0	0	1		1
50.3.x.y	I&A	Testing	0.75	MY	113	0.75	84.75	0		84.75
50.3.x.y	P/F	Testing	1	LS	0	0	0	5		5
50.3.x.y	ENG	Prototype Setup	0.75	MY	113	0.75	84.75	0		84.75
50.3.x.y	M&S	Prototype Setup	1	LS	0	0	0	5		5
50.3.x		Trig Supervisor TOTAL				3	295		11	306
50.3.x.y	ENG	Design & Simulation	0.5	MY	113	0.5	56.5	0		56.5
50.3.x.y	M&S	Design & Simulation	1	LS	0	0	0	0		0
50.3.x.y	P/F	Procurement	1	LS	0	0	0	40		40
50.3.x.y	ENG	Software Development	2	MY	69	2	138	0		138

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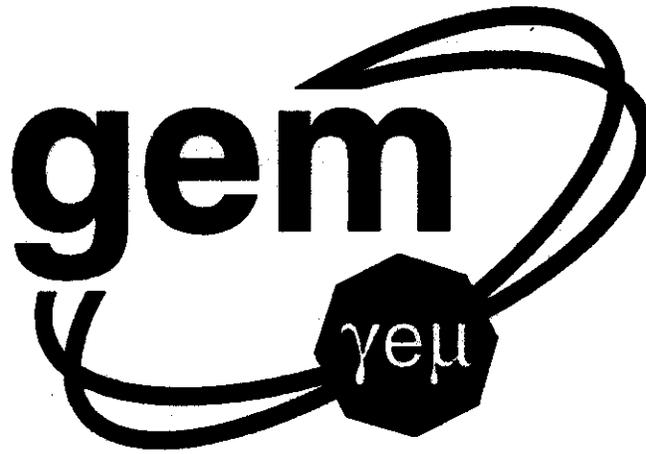
GEM (SCI) DAQ WBS

50.3.x.y	M&S	Software Development	1	LS		0	0	0	1	1
50.3.x.y	I&A	Testing	1	MY		113	1	113	0	113
50.3.x.y	P/F	Testing	1	LS		0	0	0	5	5
50.3.x.y	ENG	Prototype Setup	0.75	MY		113	0.75	84.75	0	84.75
50.3.x.y	M&S	Prototype Setup	1	LS		0	0	0	5	5
50.3.x		Control System TOTAL					4.25	392.25	51	443.25

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ISSUES

- DAQ EXTENT?
- DIAGNOSTICS? / SLOW CONTROL?
("MANDATE JTAG") / P1394
- PROCESSOR FARM - LZ?
- L1 DATA VOLUME FROM
EACH SUBSYSTEM?
- APPROACH TO SCALING...
@ FE OR DAQ?



Rack & Power Supply Status

Ken Freeman

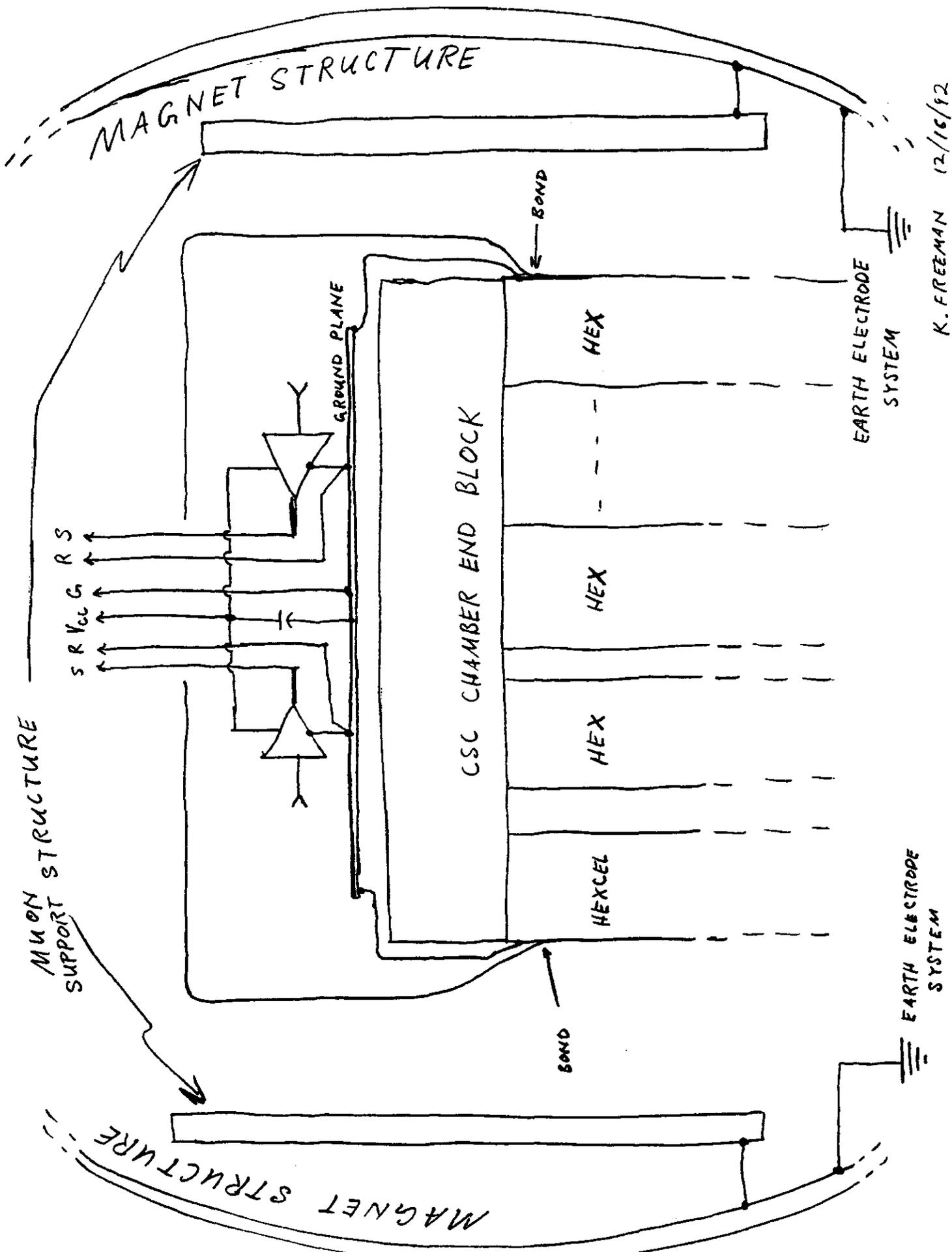
RACK & POWER SUPPLY
STATUS

- AC Power Supply Update
- Rack Design Issues
- Rack Cooling Concepts
- Rack Cost / Slot Cost
- Magnetic Field Issue

AC POWER SUPPLY UPDATE

- GEM ELECTRONICS HAS DEDICATED 12.5 KV FEEDER
- 3.2 MVA REQUESTED FOR ELECTRONICS
 - 1.8 MVA IN HALL
 - 1.3 MVA IN CABLE ELECTRONICS SHAFT
- ESTIMATE CONTAINS EFFICIENCY AND CONTINGENCY
- POWER REVISION REQUIRED IN 10 MONTHS
 - DISTRIBUTION INPUTS FOR PB/MK
 - EFD MAY TAKE OVER DESIGN

MUON SHIELD/GROUND CONCEPT - after Y. KIRYUSHIN



K. FREEMAN 12/16/92

RACK DESIGN REQUIREMENTS + ISSUES

REQUIREMENTS

- SUPPORT and PROTECT ELECTRONICS IN GEM ENVIRONMENTS

Provide power + cooling

Detect and report hazards, maintaining safety

Wheel through a 2.5 meter doorway

Cable Electronics Shaft - Crate / Subrack loads

- 9U VME basis, 2 or 3 per rack
- Standard SMPS useable
- MCHW cooling (20% leak to air)
- Host Slow Control Crate (6U VME)

Detector Hall location - MAGNETIC FIELD ISSUE

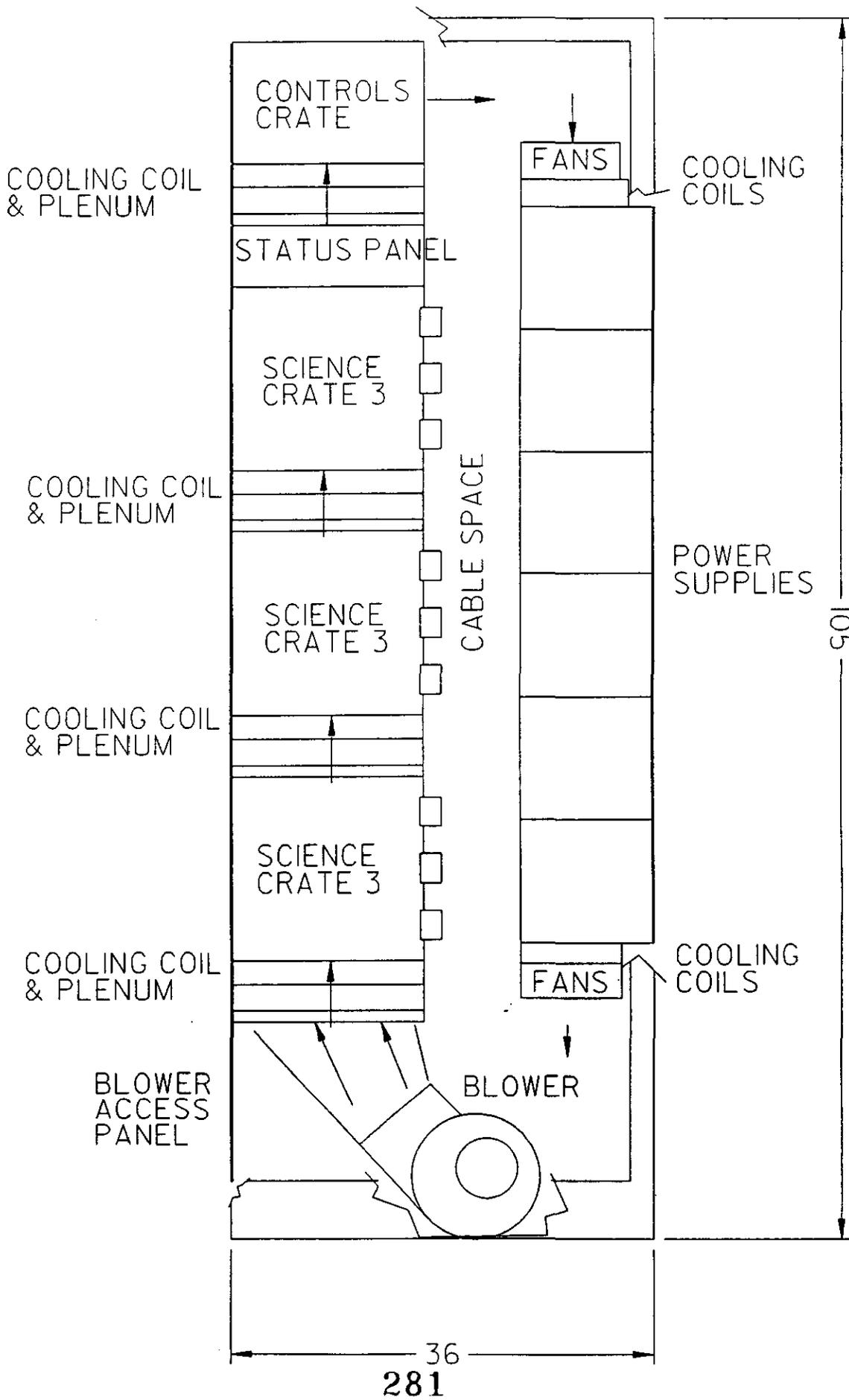
- Crate loads as in C/E Shaft
- Power loads provide power to IND
- EM Interference may become significant
- Increased radiation environment

COSTING BASIS IS A CABLE ELECTRONICS SHAFT RACK

19" x 78" front, 36" depth

MCHW / FORCED AIR COOLING, 10 → 12 kW

2 CRATES, PLUS SLOW CONTROL CRATE



PRELIMINARY RACK SYSTEM HARDWARE

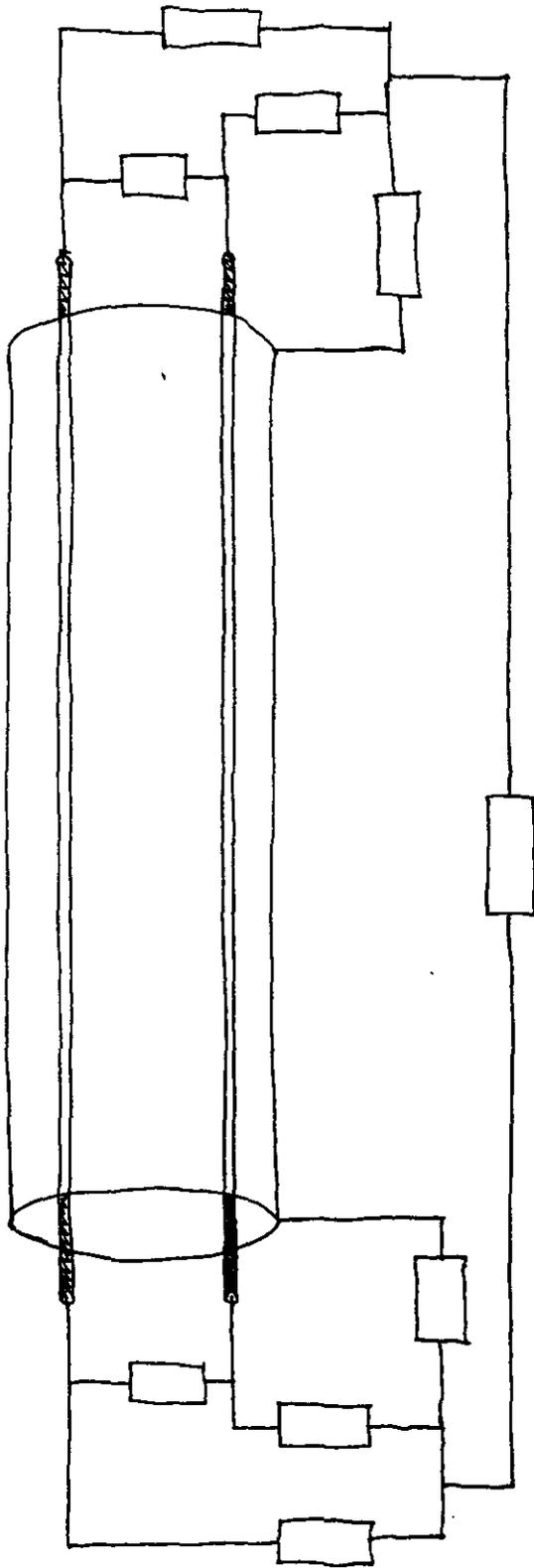
RACK FRAME	375.00
DOORS, SIDES, PANELS	707.00
ACCESSORIES	315.00
<hr/>	
SUBTOTAL	<u>1492.00</u>
FANS (3 trays)	1085.00
HEAT EXCHANGERS (3)	600.00
PIPING	100.00
9U VME SUBRACK (2)	3000.00
STANDARD CONTROLLER + LINK (2)	2400.00
POWER SUPPLIES (5550w x \$.75/w)	4200.00
FIRE, ETC. SENSORS (est.)	350.00
POWER WIRING	<u>150.00</u>
RACK HARDWARE COST TOTAL	<u>13,387.00</u>
ASSEMBLY, TEST, INSTALLATION (80 hr, \$50/hr) (ALLOWANCE)	4,000.00
<hr/>	
RACK TOTAL	\$ 17,387.00

SLOT CHARGE : 20 MODULES
 $\frac{\$17,400}{20} \approx \underline{\underline{\$870 \text{ ea}}}$ ←

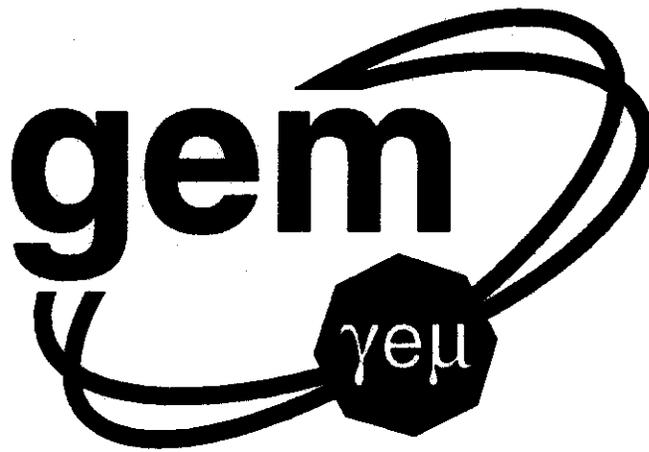
40 MODULES
 $\frac{\$17,400}{40} \approx \underline{\underline{\$435 \text{ ea}}}$ ←

MAGNETIC FIELD UPDATE

- MEASURED TRANSFORMER PERFORMANCE AT JOSEPH HENRY CYCLOTRON
VARIED: \vec{B} , ORIENTATION, PRIMARY VOLTAGE, LOADED/UNLOADED, SMALL/LARGE
- RESULTS: ① ORTHOGONAL ORIENTATION IS BEST.
 - ② NO PROBLEM BELOW 500 GAUSS IN TRANSFORMER MODE. (INDUCTORS MORE SENSITIVE!)
 - ③ INDUCTANCE SLIGHTLY REDUCED AT 500 G.
 - ④ LOAD CABLE SUBJECT TO LORENTZ FORCE.
 - ⑤ CORE VIBRATES WHEN SATURATED.
 - ⑥ CORE HEATS WHEN SATURATED.
 - ⑦ FIELD GRADIENT CAUSES SIGNIFICANT FORCE.
- IMPACTS - DESIGN OPTIONS
 - ① AVOID 500 → 1000 GAUSS OR MORE, INsofar AS POSSIBLE.
 - ② USE OVERSIZED TRANSFORMERS @ 60 HZ, CONTINUE TO INVESTIGATE HIGHER FREQUENCIES.
 - ③ USE AIR-CORE MAGNETICS AT VERY HIGH FREQUENCIES. (COOKE / LANL)
 - ④ MUST INVESTIGATE FANS, RELAYS, ETC.
 - ⑤ MUST TEST PROPOSED POWER SUPPLIES.



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Electronics Integration

Norm Lau



GEM Integration Status - Ken Freeman and Norman Lau (Dec. 1992)

GEM Facility - interface to EFD, CCD and BP/MK

GEFUR - Conventional and technical facility ground

Electrical load

A/C power distribution

Cooling

Title II - Electronics Rooms

Electronics Shop

Cable tunnel #5 and #6

Installation plan - Racks in the Electronics Rooms and detector hall

Electronics Rooms lay-out

Cabling between the Operation Center, Electronics Rooms and the detector hall

GEM Electronics - interface to GEM Project Planning team and subsystem groups

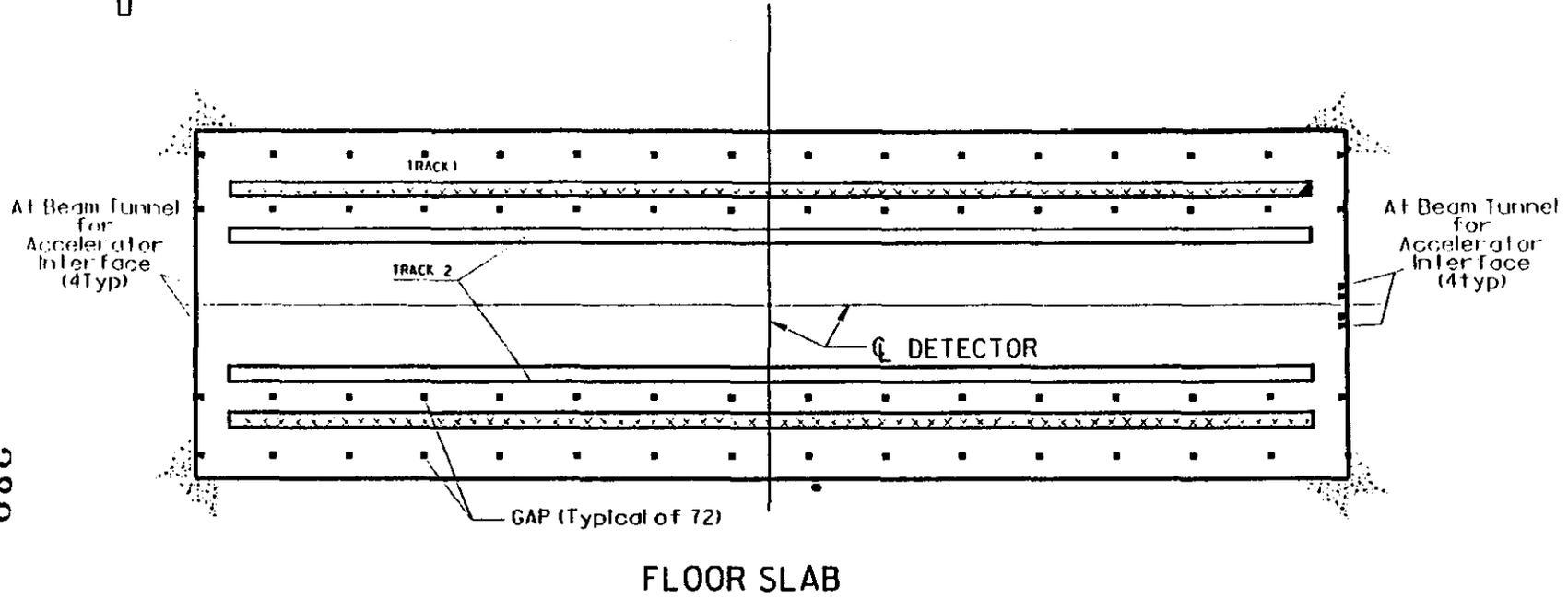
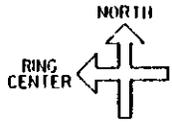
Maintain Baseline document

Maintain WBS

Co-ordinate with the Project Planning team and subsystem groups for establishing schedules and bottoms-up estimates.

Investigate commercial fiber link to meet radiation requirement, collaborate with SDC, discuss with subsystem groups for common data link

Establish electronic requirements



See Fig 4-19 for the Location of Tracks 1 and 2

Symbol	Description
■	Symbol indicates a Grounding Access Point (GAP) for connection to the Facility Ground Grid. Coordinate exact placement/location of GAPs with structural foundations/columns, Detector/Beamline support structures, and Detector Load Paths.

Figure 18-5 GEM Grounding Access Points Locations

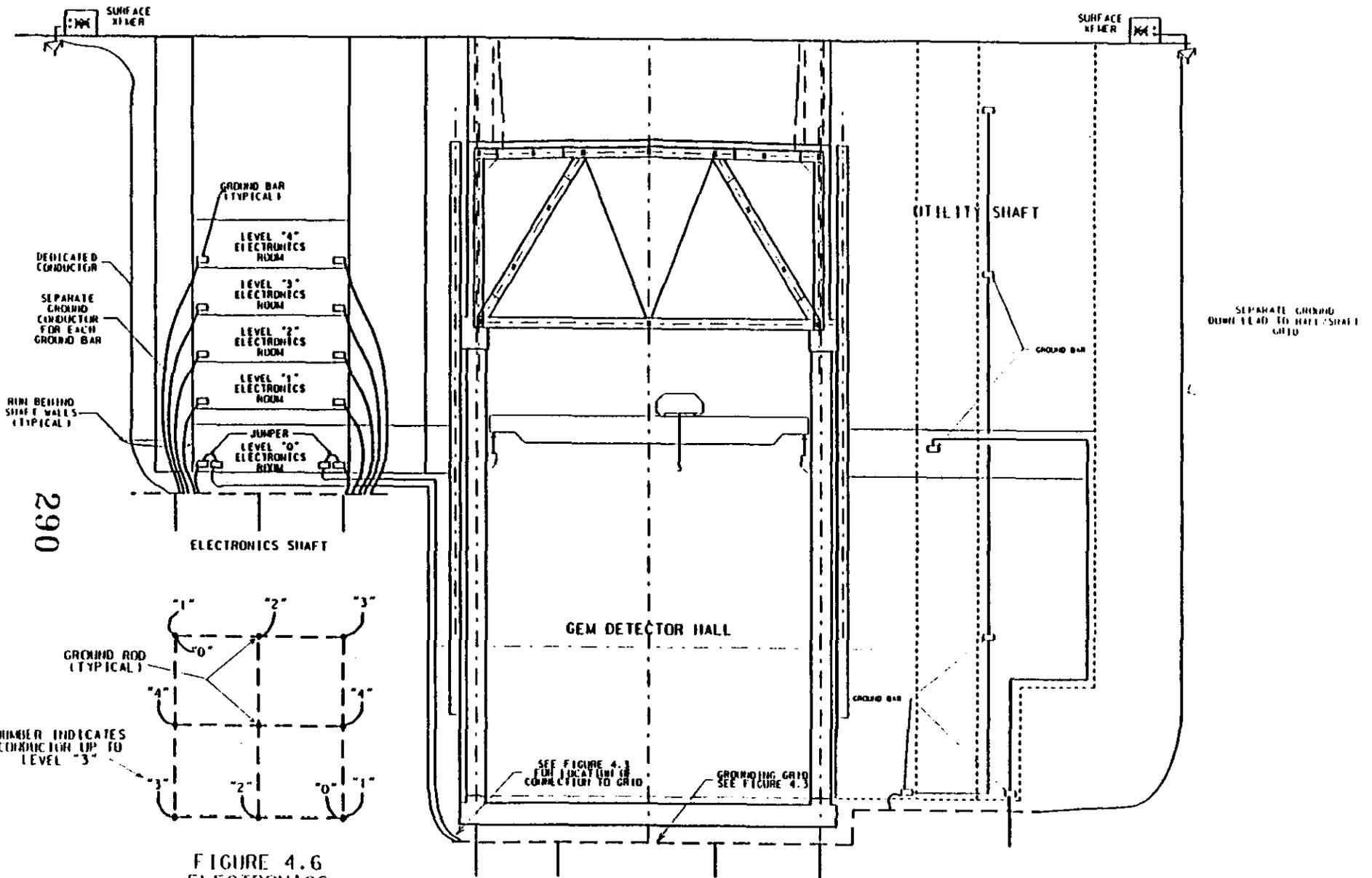


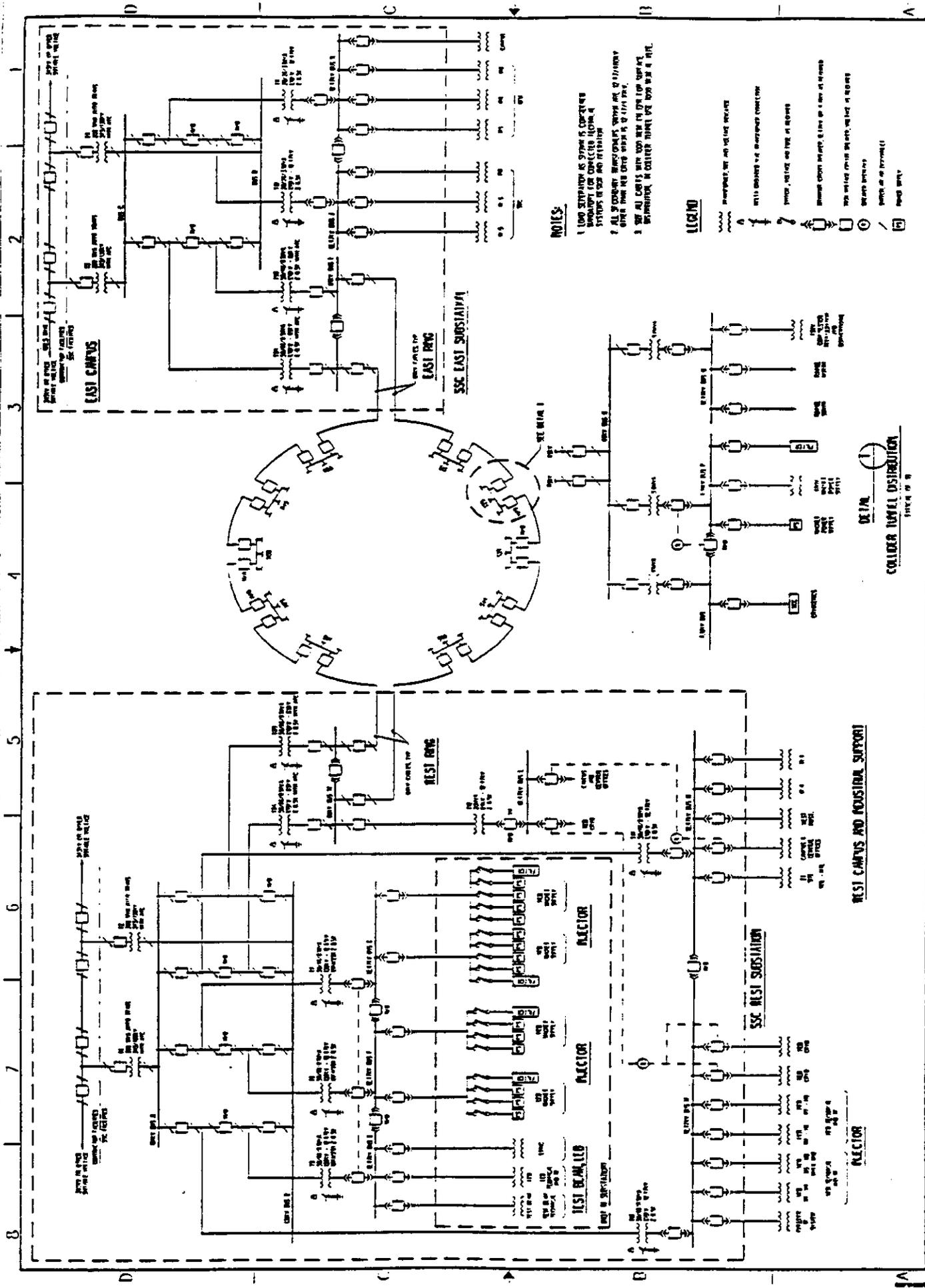
FIGURE 4.6
ELECTRONICS
GROUNDING GRID
(PLAN VIEW)

FIGURE 4.5
GEM UNDERGROUND GROUNDING



Electrical Load

Maximum construction power to June 1996 for GEM & SDC	9.5MVA
GEM's power requirement for the year of 1995	8.3MVA
SDC's power requirement for the year of 1995	3.2MVA
GEM's requirement from Jan to June of 1996	10.6MVA
SDC's requirement from Jan to June of 1996	6.3MVA
Total power allocation for GEM after June 1996	14.5MVA
Clean power allocated for electronics load	1.3MVA
Estimated clean power for underground electronics load	3.2MVA
In-detector and On-detector electronics	1.9MVA
Electronics Rooms (Level 1 to 4)	1.3MVA



NOTES:

1. LOAD ESTIMATION IS SHOWN IN COMPLETE SCHEDULE FOR COMPLETE SYSTEM. (SEE A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z, AA, AB, AC, AD, AE, AF, AG, AH, AI, AJ, AK, AL, AM, AN, AO, AP, AQ, AR, AS, AT, AU, AV, AW, AX, AY, AZ, BA, BB, BC, BD, BE, BF, BG, BH, BI, BJ, BK, BL, BM, BN, BO, BP, BQ, BR, BS, BT, BU, BV, BW, BX, BY, BZ, CA, CB, CC, CD, CE, CF, CG, CH, CI, CJ, CK, CL, CM, CN, CO, CP, CQ, CR, CS, CT, CU, CV, CW, CX, CY, CZ, DA, DB, DC, DD, DE, DF, DG, DH, DI, DJ, DK, DL, DM, DN, DO, DP, DQ, DR, DS, DT, DU, DV, DW, DX, DY, DZ, EA, EB, EC, ED, EE, EF, EG, EH, EI, EJ, EK, EL, EM, EN, EO, EP, EQ, ER, ES, ET, EU, EV, EW, EX, EY, EZ, FA, FB, FC, FD, FE, FF, FG, FH, FI, FJ, FK, FL, FM, FN, FO, FP, FQ, FR, FS, FT, FU, FV, FW, FX, FY, FZ, GA, GB, GC, GD, GE, GF, GG, GH, GI, GJ, GK, GL, GM, GN, GO, GP, GQ, GR, GS, GT, GU, GV, GW, GX, GY, GZ, HA, HB, HC, HD, HE, HF, HG, HH, HI, HJ, HK, HL, HM, HN, HO, HP, HQ, HR, HS, HT, HU, HV, HW, HX, HY, HZ, IA, IB, IC, ID, IE, IF, IG, IH, II, IJ, IK, IL, IM, IN, IO, IP, IQ, IR, IS, IT, IU, IV, IW, IX, IY, IZ, JA, JB, JC, JD, JE, JF, JG, JH, JI, JJ, JK, JL, JM, JN, JO, JP, JQ, JR, JS, JT, JU, JV, JW, JX, JY, JZ, KA, KB, KC, KD, KE, KF, KG, KH, KI, KJ, KK, KL, KM, KN, KO, KP, KQ, KR, KS, KT, KU, KV, KW, KX, KY, KZ, LA, LB, LC, LD, LE, LF, LG, LH, LI, LJ, LK, LL, LM, LN, LO, LP, LQ, LR, LS, LT, LU, LV, LW, LX, LY, LZ, MA, MB, MC, MD, ME, MF, MG, MH, MI, MJ, MK, ML, MM, MN, MO, MP, MQ, MR, MS, MT, MU, MV, MW, MX, MY, MZ, NA, NB, NC, ND, NE, NF, NG, NH, NI, NJ, NK, NL, NM, NN, NO, NP, NQ, NR, NS, NT, NU, NV, NW, NX, NY, NZ, OA, OB, OC, OD, OE, OF, OG, OH, OI, OJ, OK, OL, OM, ON, OO, OP, OQ, OR, OS, OT, OU, OV, OW, OX, OY, OZ, PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT, PU, PV, PW, PX, PY, PZ, QA, QB, QC, QD, QE, QF, QG, QH, QI, QJ, QK, QL, QM, QN, QO, QP, QQ, QR, QS, QT, QU, QV, QW, QX, QY, QZ, RA, RB, RC, RD, RE, RF, RG, RH, RI, RJ, RK, RL, RM, RN, RO, RP, RQ, RR, RS, RT, RU, RV, RW, RX, RY, RZ, SA, SB, SC, SD, SE, SF, SG, SH, SI, SJ, SK, SL, SM, SN, SO, SP, SQ, SR, SS, ST, SU, SV, SW, SX, SY, SZ, TA, TB, TC, TD, TE, TF, TG, TH, TI, TJ, TK, TL, TM, TN, TO, TP, TQ, TR, TS, TT, TU, TV, TW, TX, TY, TZ, UA, UB, UC, UD, UE, UF, UG, UH, UI, UJ, UK, UL, UM, UN, UO, UP, UQ, UR, US, UT, UY, UZ, VA, VB, VC, VD, VE, VF, VG, VH, VI, VJ, VK, VL, VM, VN, VO, VP, VQ, VR, VS, VT, VU, VV, VW, VX, VY, VZ, WA, WB, WC, WD, WE, WF, WG, WH, WI, WJ, WK, WL, WM, WN, WO, WP, WQ, WR, WS, WT, WU, WV, WW, WX, WY, WZ, XA, XB, XC, XD, XE, XF, XG, XH, XI, XJ, XK, XL, XM, XN, XO, XP, XQ, XR, XS, XT, XU, XV, XW, XX, XY, XZ, YA, YB, YC, YD, YE, YF, YG, YH, YI, YJ, YK, YL, YM, YN, YO, YP, YQ, YR, YS, YT, YU, YV, YW, YX, YY, YZ, ZA, ZB, ZC, ZD, ZE, ZF, ZG, ZH, ZI, ZJ, ZK, ZL, ZM, ZN, ZO, ZP, ZQ, ZR, ZS, ZT, ZU, ZV, ZW, ZX, ZY, ZZ.

LEGEND:

- 1. LOAD ESTIMATION IS SHOWN IN COMPLETE SCHEDULE FOR COMPLETE SYSTEM. (SEE A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z, AA, AB, AC, AD, AE, AF, AG, AH, AI, AJ, AK, AL, AM, AN, AO, AP, AQ, AR, AS, AT, AU, AV, AW, AX, AY, AZ, BA, BB, BC, BD, BE, BF, BG, BH, BI, BJ, BK, BL, BM, BN, BO, BP, BQ, BR, BS, BT, BU, BV, BW, BX, BY, BZ, CA, CB, CC, CD, CE, CF, CG, CH, CI, CJ, CK, CL, CM, CN, CO, CP, CQ, CR, CS, CT, CU, CV, CW, CX, CY, CZ, DA, DB, DC, DD, DE, DF, DG, DH, DI, DJ, DK, DL, DM, DN, DO, DP, DQ, DR, DS, DT, DU, DV, DW, DX, DY, DZ, EA, EB, EC, ED, EE, EF, EG, EH, EI, EJ, EK, EL, EM, EN, EO, EP, EQ, ER, ES, ET, EU, EV, EW, EX, EY, EZ, FA, FB, FC, FD, FE, FF, FG, FH, FI, FJ, FK, FL, FM, FN, FO, FP, FQ, FR, FS, FT, FU, FV, FW, FX, FY, FZ, GA, GB, GC, GD, GE, GF, GG, GH, GI, GJ, GK, GL, GM, GN, GO, GP, GQ, GR, GS, GT, GU, GV, GW, GX, GY, GZ, HA, HB, HC, HD, HE, HF, HG, HH, HI, HJ, HK, HL, HM, HN, HO, HP, HQ, HR, HS, HT, HU, HV, HW, HX, HY, HZ, IA, IB, IC, ID, IE, IF, IG, IH, II, IJ, IK, IL, IM, IN, IO, IP, IQ, IR, IS, IT, IU, IV, IW, IX, IY, IZ, JA, JB, JC, JD, JE, JF, JG, JH, JI, JJ, JK, JL, JM, JN, JO, JP, JQ, JR, JS, JT, JU, JV, JW, JX, JY, JZ, KA, KB, KC, KD, KE, KF, KG, KH, KI, KJ, KK, KL, KM, KN, KO, KP, KQ, KR, KS, KT, KU, KV, KW, KX, KY, KZ, LA, LB, LC, LD, LE, LF, LG, LH, LI, LJ, LK, LL, LM, LN, LO, LP, LQ, LR, LS, LT, LU, LV, LW, LX, LY, LZ, MA, MB, MC, MD, ME, MF, MG, MH, MI, MJ, MK, ML, MM, MN, MO, MP, MQ, MR, MS, MT, MU, MV, MW, MX, MY, MZ, NA, NB, NC, ND, NE, NF, NG, NH, NI, NJ, NK, NL, NM, NN, NO, NP, NQ, NR, NS, NT, NU, NV, NW, NX, NY, NZ, OA, OB, OC, OD, OE, OF, OG, OH, OI, OJ, OK, OL, OM, ON, OO, OP, OQ, OR, OS, OT, OU, OV, OW, OX, OY, OZ, PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT, PU, PV, PW, PX, PY, PZ, QA, QB, QC, QD, QE, QF, QG, QH, QI, QJ, QK, QL, QM, QN, QO, QP, QQ, QR, QS, QT, QU, QV, QW, QX, QY, QZ, RA, RB, RC, RD, RE, RF, RG, RH, RI, RJ, RK, RL, RM, RN, RO, RP, RQ, RR, RS, RT, RU, RV, RW, RX, RY, RZ, SA, SB, SC, SD, SE, SF, SG, SH, SI, SJ, SK, SL, SM, SN, SO, SP, SQ, SR, SS, ST, SU, SV, SW, SX, SY, SZ, TA, TB, TC, TD, TE, TF, TG, TH, TI, TJ, TK, TL, TM, TN, TO, TP, TQ, TR, TS, TT, TU, TV, TW, TX, TY, TZ, UA, UB, UC, UD, UE, UF, UG, UH, UI, UJ, UK, UL, UM, UN, UO, UP, UQ, UR, US, UT, UY, UZ, VA, VB, VC, VD, VE, VF, VG, VH, VI, VJ, VK, VL, VM, VN, VO, VP, VQ, VR, VS, VT, VU, VV, VW, VX, VY, VZ, WA, WB, WC, WD, WE, WF, WG, WH, WI, WJ, WK, WL, WM, WN, WO, WP, WQ, WR, WS, WT, WU, WV, WW, WX, WY, WZ, XA, XB, XC, XD, XE, XF, XG, XH, XI, XJ, XK, XL, XM, XN, XO, XP, XQ, XR, XS, XT, XU, XV, XW, XX, XY, XZ, YA, YB, YC, YD, YE, YF, YG, YH, YI, YJ, YK, YL, YM, YN, YO, YP, YQ, YR, YS, YT, YU, YV, YW, YX, YY, YZ, ZA, ZB, ZC, ZD, ZE, ZF, ZG, ZH, ZI, ZJ, ZK, ZL, ZM, ZN, ZO, ZP, ZQ, ZR, ZS, ZT, ZU, ZV, ZW, ZX, ZY, ZZ.

<p>PROJECT NUMBER E200-38</p>	
<p>DATE 10/21/59</p>	<p>SCALE D</p>
<p>PROJECT NAME S'COL SCHEME 305/19/67/12 27KV DISTRIBUTION SHEET 19E DISTRAM</p>	
<p>CONTRACT NO. DE-A-33-68-0000</p>	
<p>DESIGNER SSC STRUCTURAL STEEL CONSTRUCTION</p>	
<p>CONVENTIONAL CONSTRUCTION DANSON</p>	
<p>DATE 10/21/59</p>	
<p>BY [Signature]</p>	
<p>CHECKED BY [Signature]</p>	
<p>APPROVED BY [Signature]</p>	

293

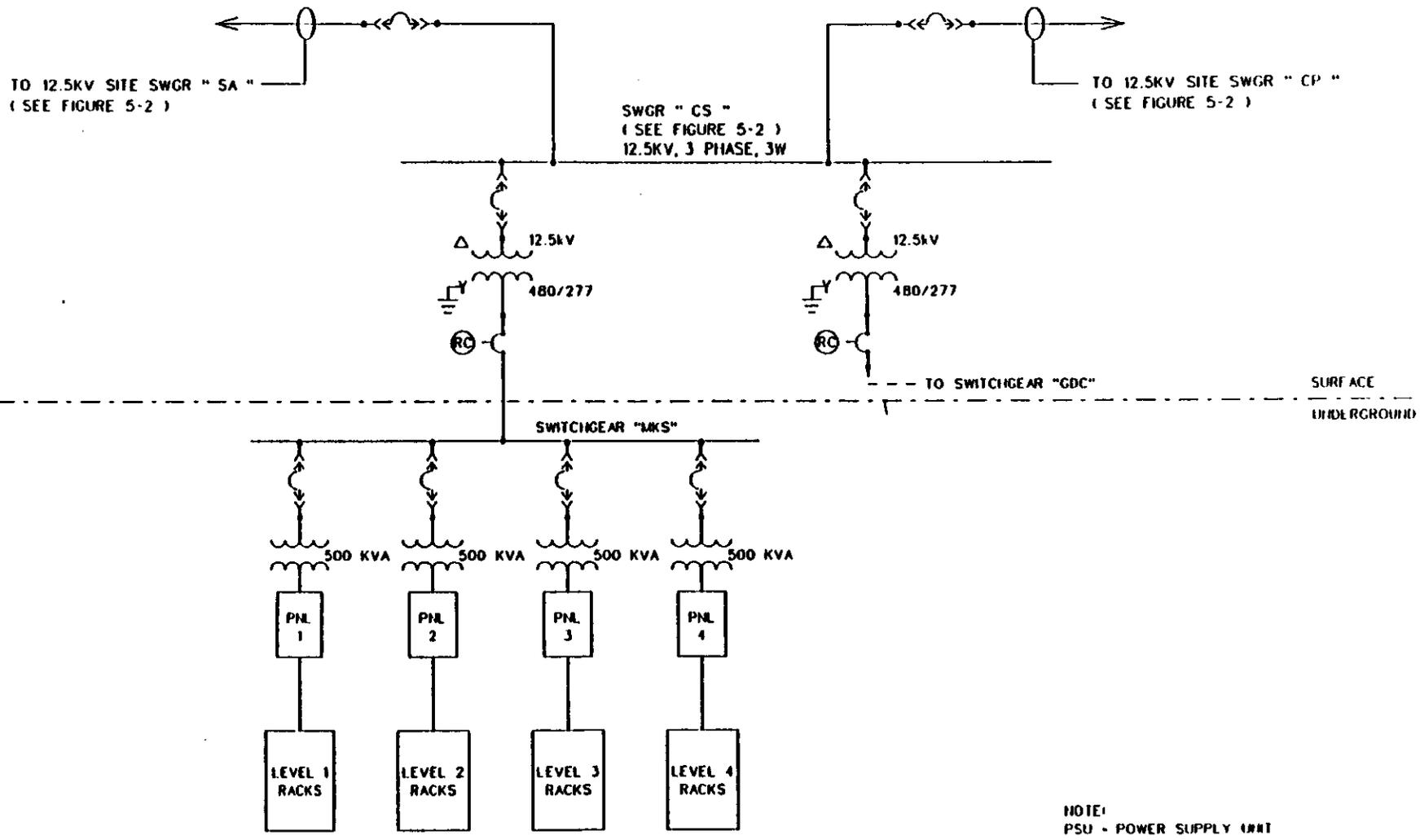
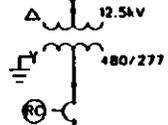
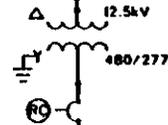


FIGURE 3.5
CABLE ELECTRONICS SHAFT POWER DISTRIBUTION

TO 12.5KV SITE SWGR "SA"
(SEE FIGURE 5-2)

SWGR "CS"
(SEE FIGURE 5-2)
12.5KV, 3 PHASE, 3W

TO 12.5KV SITE SWGR "CP"
(SEE FIGURE 5-2)

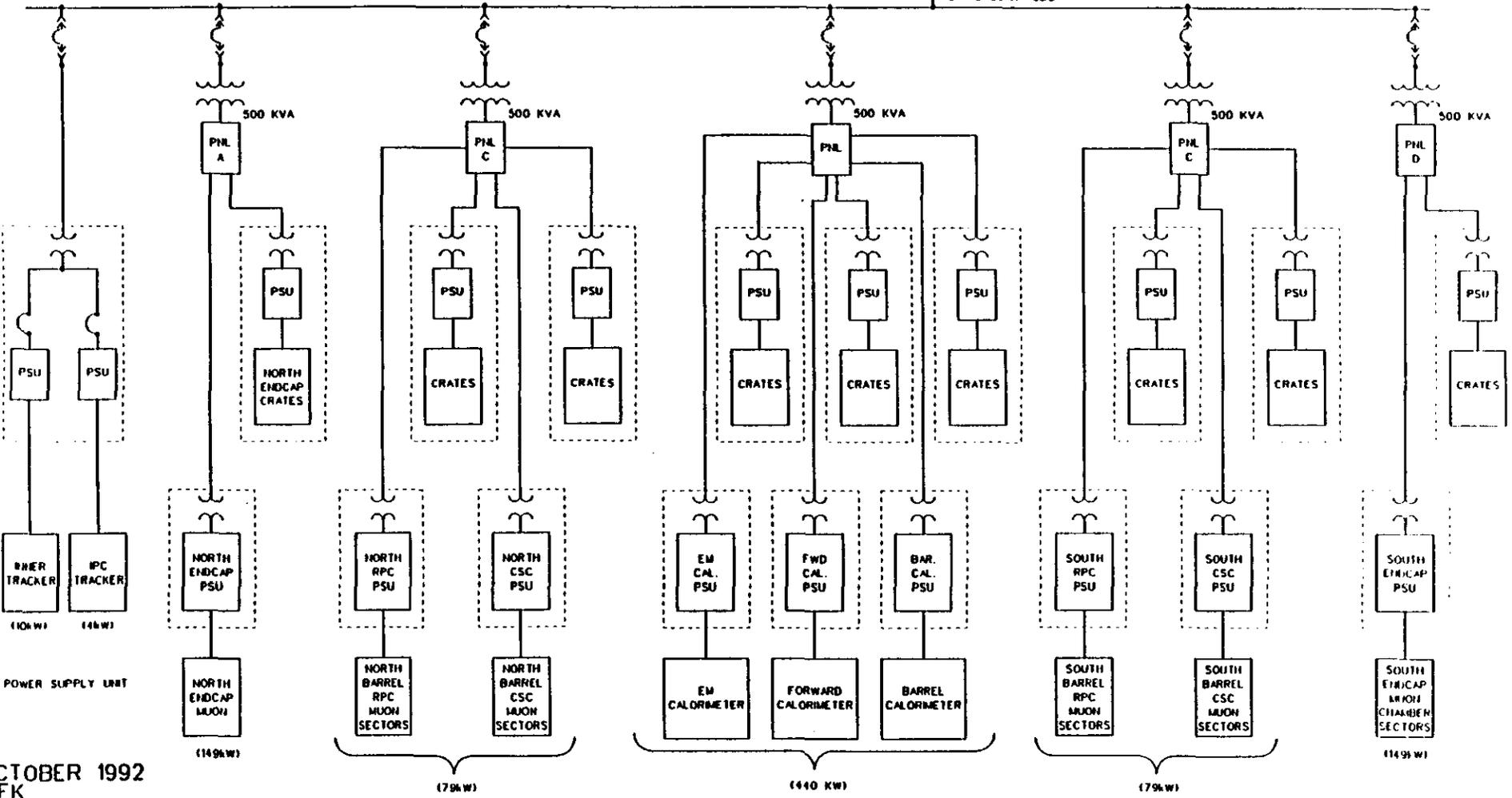


TO SWITCHGEAR "MKS"

SWITCHGEAR "GDC"

SURFACE
UNDERGROUND

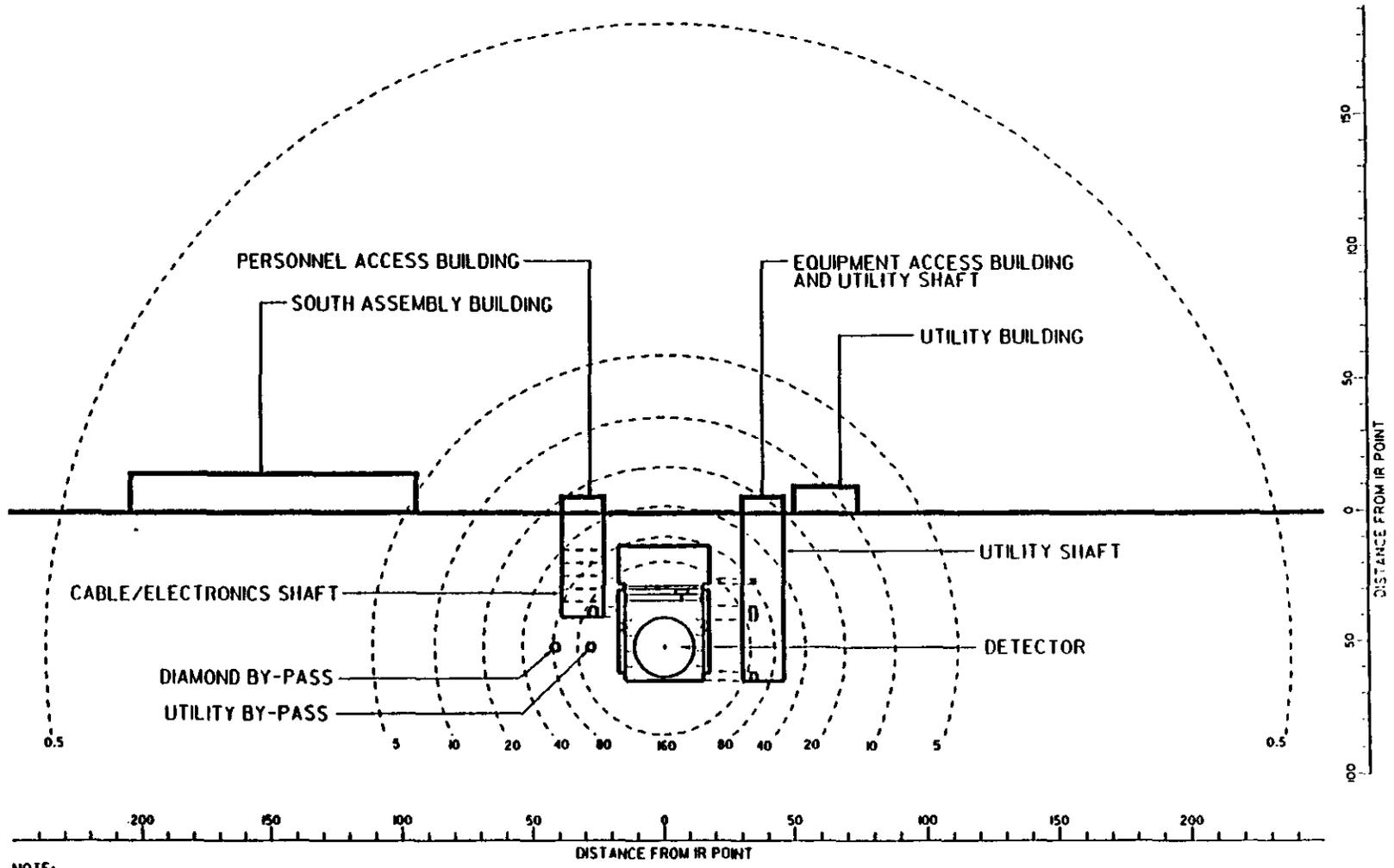
294



NOTE:
PSU - POWER SUPPLY UNIT

4 OCTOBER 1992
JDC/FK

FIGURE 3.4
EXPERIMENTAL HALL ELECTRICAL DISTRIBUTION DIAGRAM

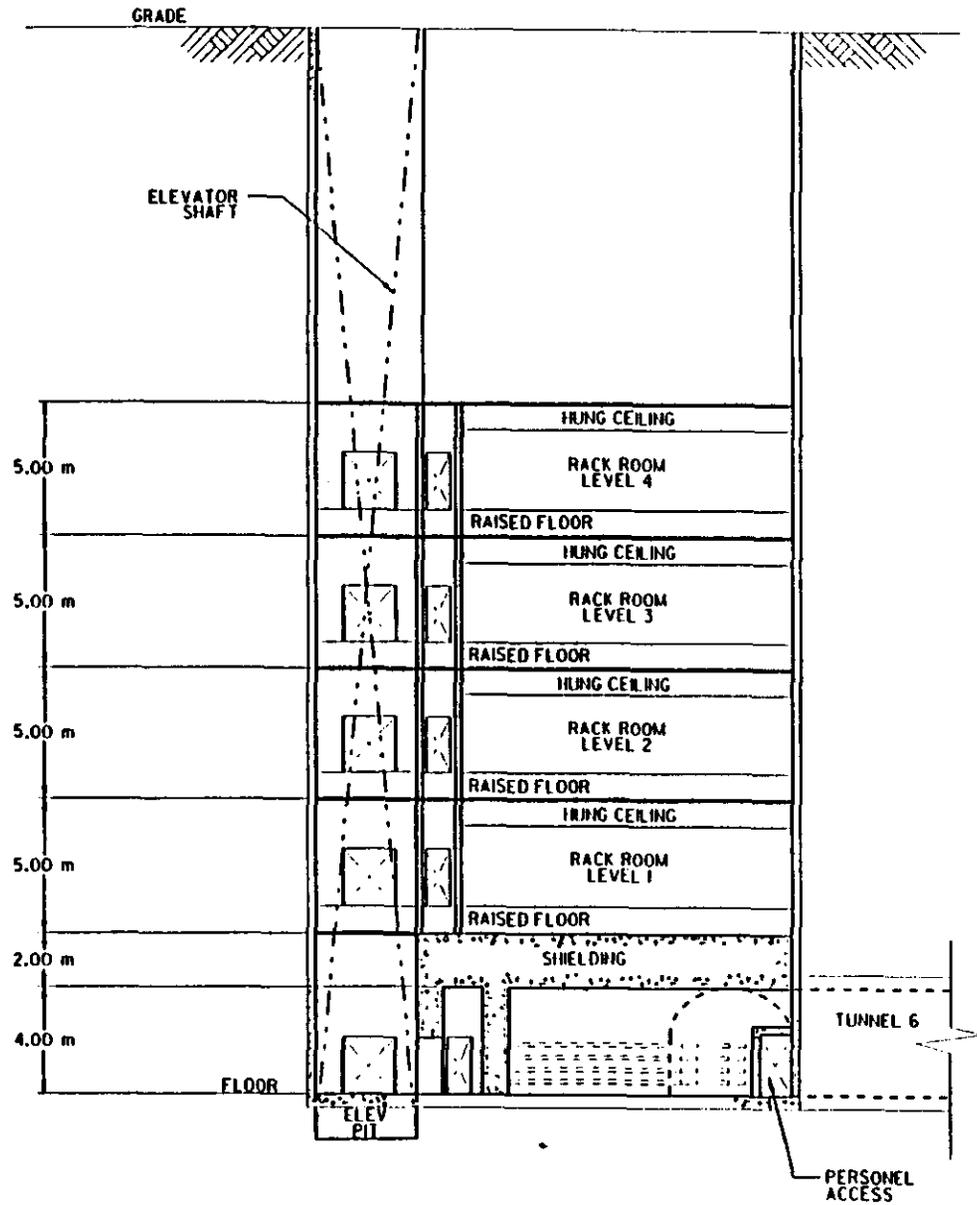


NOTE:

EARTH'S GEOMAGNETIC FIELD LEVEL (0.56 G) WAS NOT INCLUDED IN CALCULATING THE FIELD PATTERNS SHOWN.

gcd000156.b
REF. FILE(S): gcd000155
10 NOV 1992
RW/KH

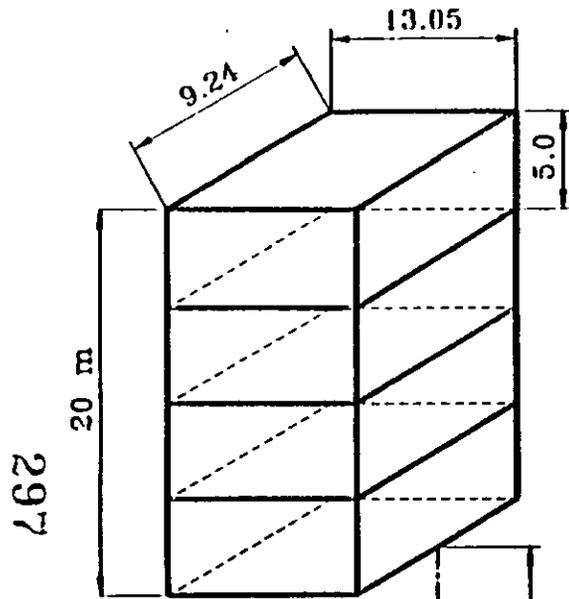
Figure 1-2 IR-5 Magnetic Field Pattern Section at IP



gcd000233.c
REF. FILE SH: gcd000234.b009
11/05/92
WILLIAM R. PETERSON

Figure 4-3A Experimental Hall Cable Electronics Shaft Detail

Electronic Rack Room Iron Shield (for max B < 50 G)



Thicknesses of the shield's walls (low carbon steel)

Easterly facing - 5 cm

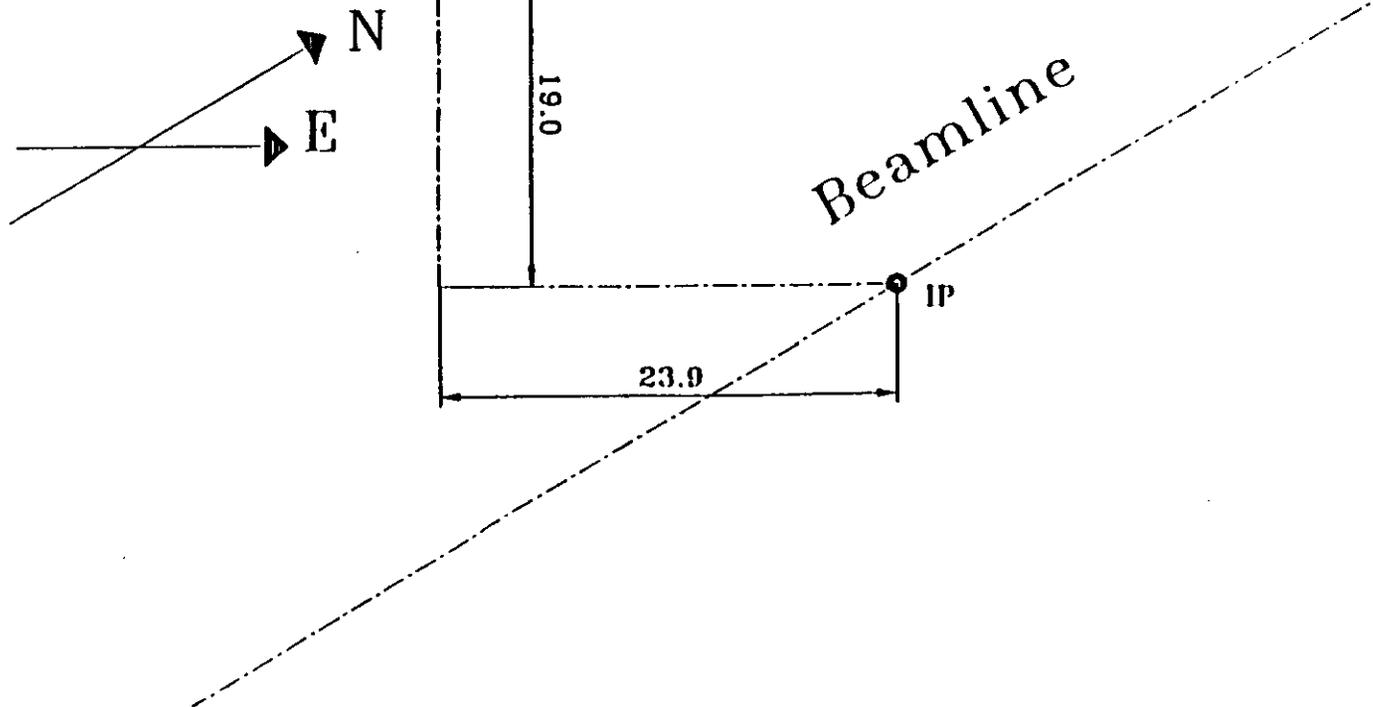
Westerly facing - 2.5 cm

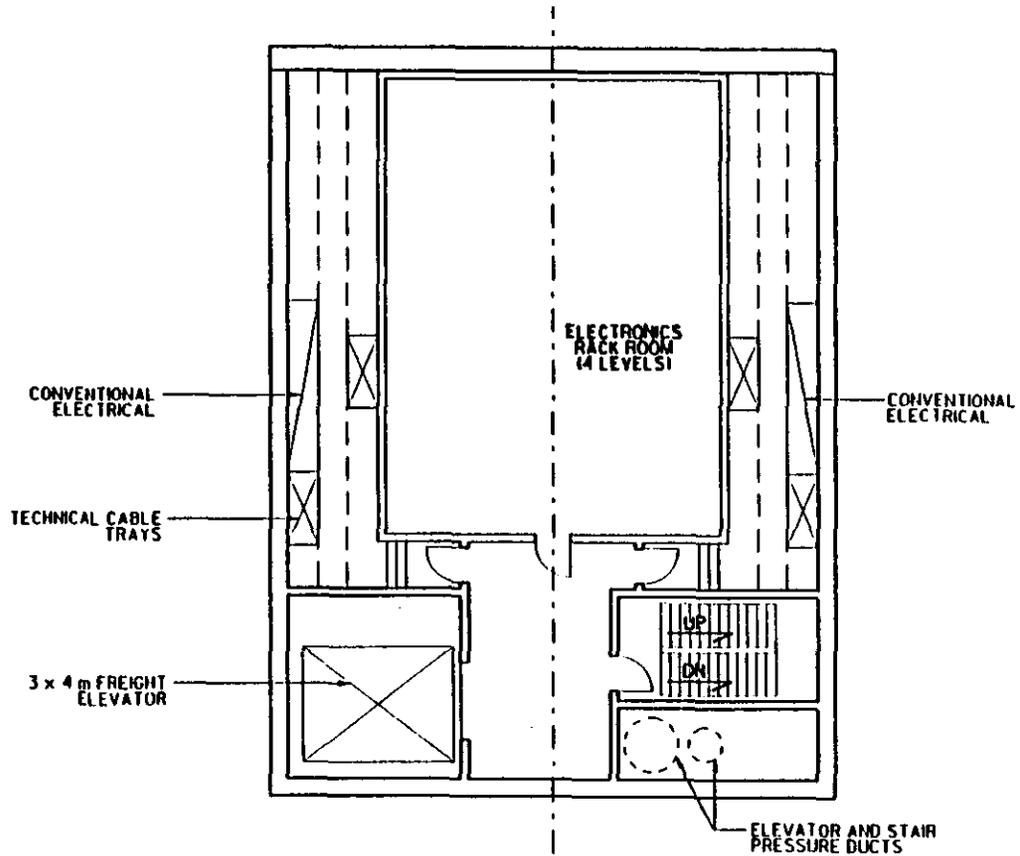
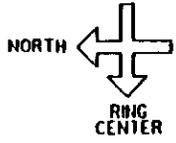
North and South - 2.5 cm

ERR bottom floor - 7.6 cm

No steel on any level Ceiling

Total weight of the shield 207 000 kg

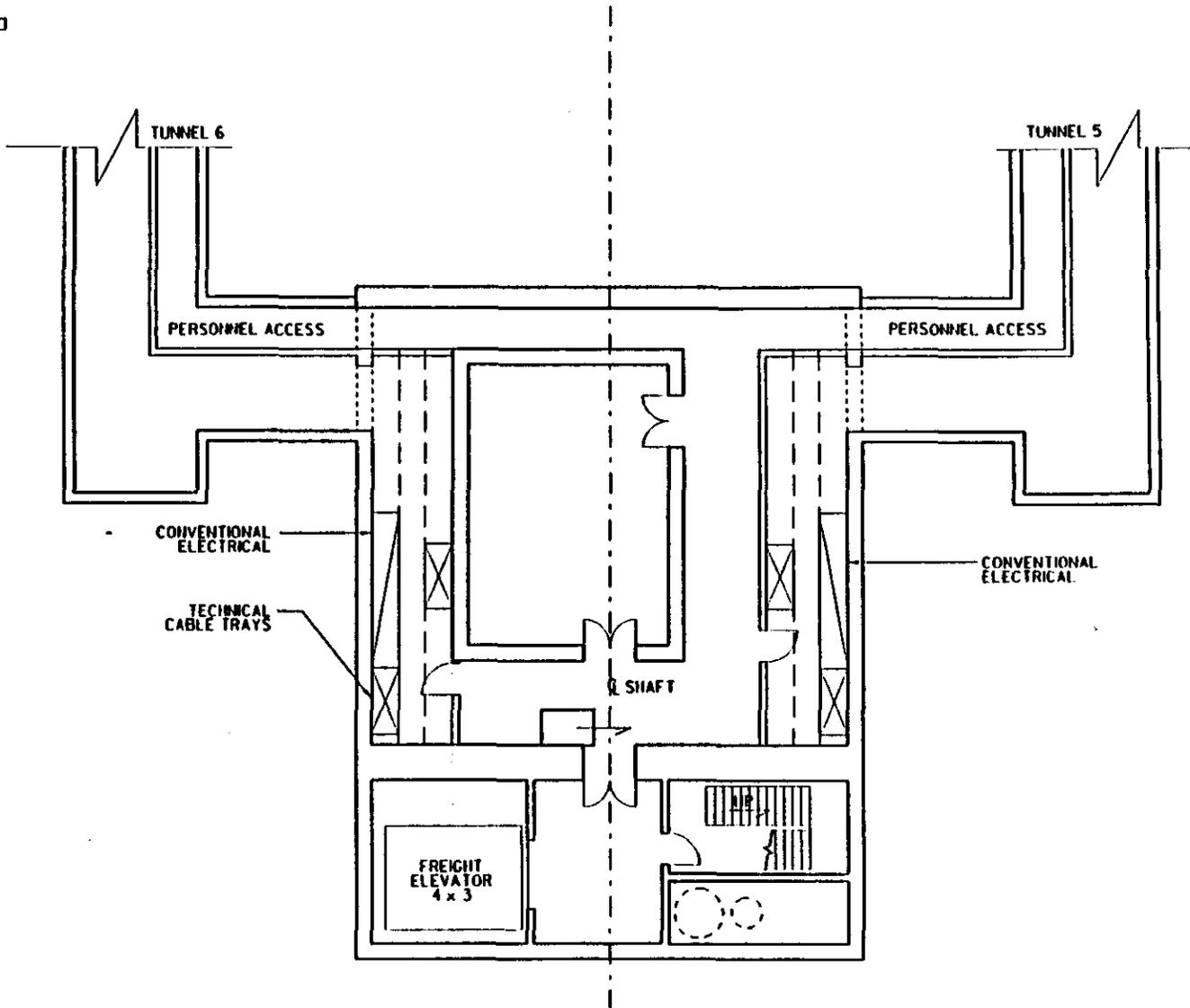
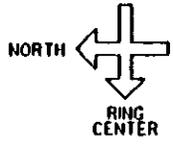




gcd000231.c
REF. FILE(S)gcd000232.b009
11/06/92
WILLIAM R. PETERSON

Figure 4-11A Experimental Hall Cable Electronics Shaft Typical Rack Room Plan

GCT-00001

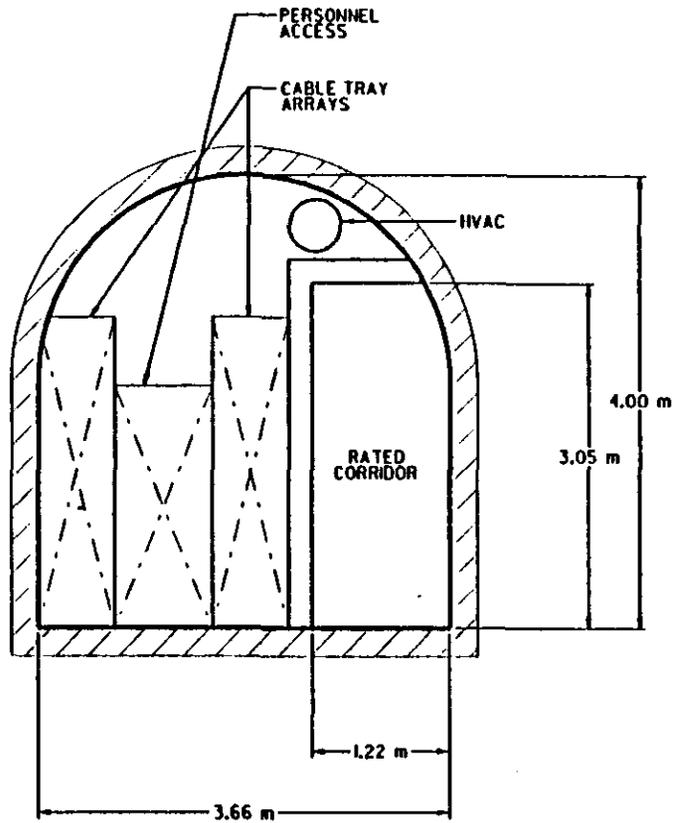


4-20
299

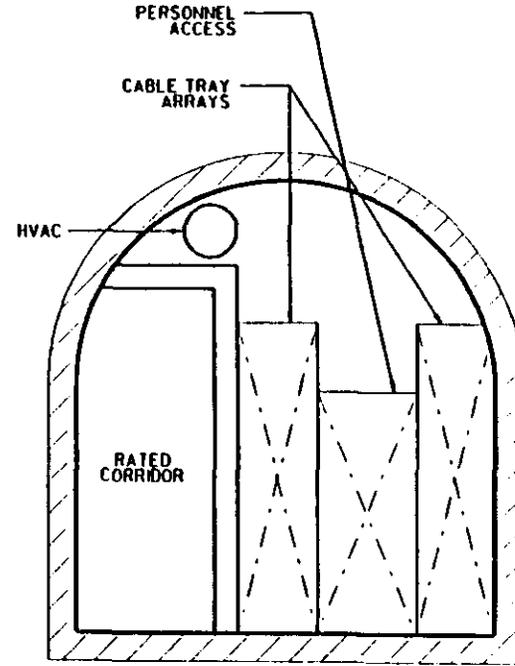
Revision C.

gcd000229.c
REF. FILE(S):gcd000230.b009
8/06/92
WILLIAM R. PETERSON

Figure 4-11 Experimental Hall Cable Electronics Shaft Plan At Tunnels 5 & 6

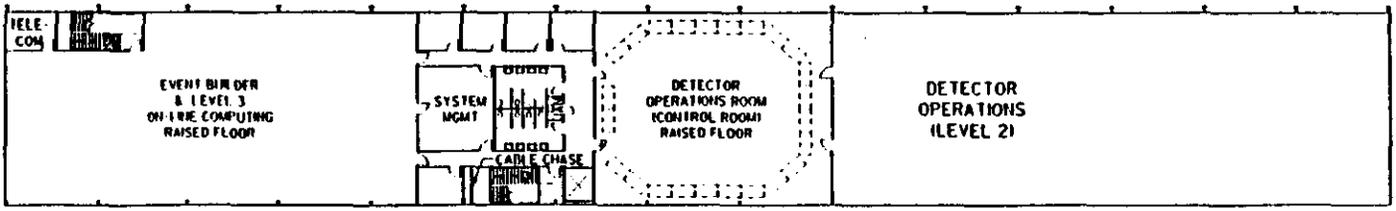
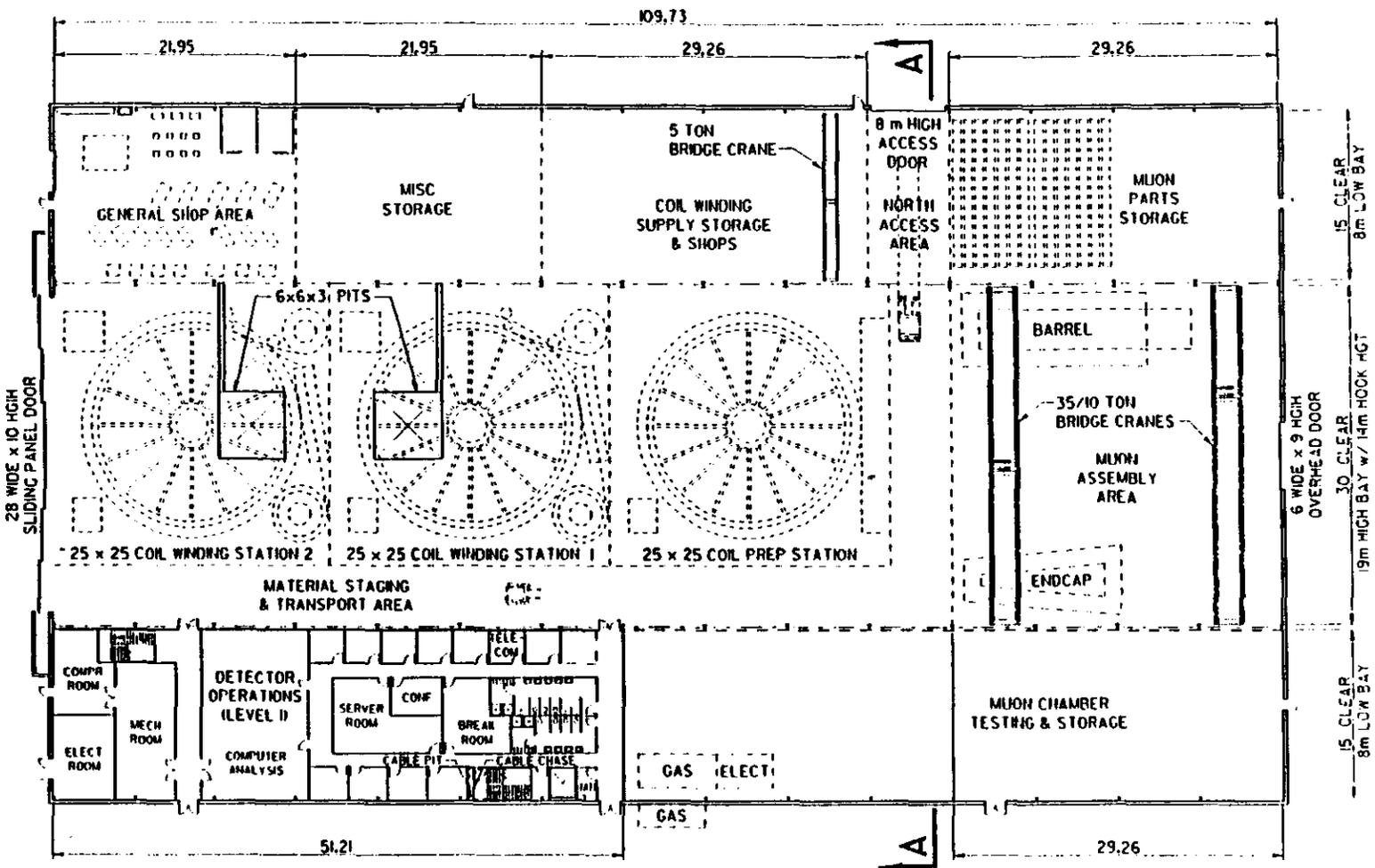


TUNNEL 6



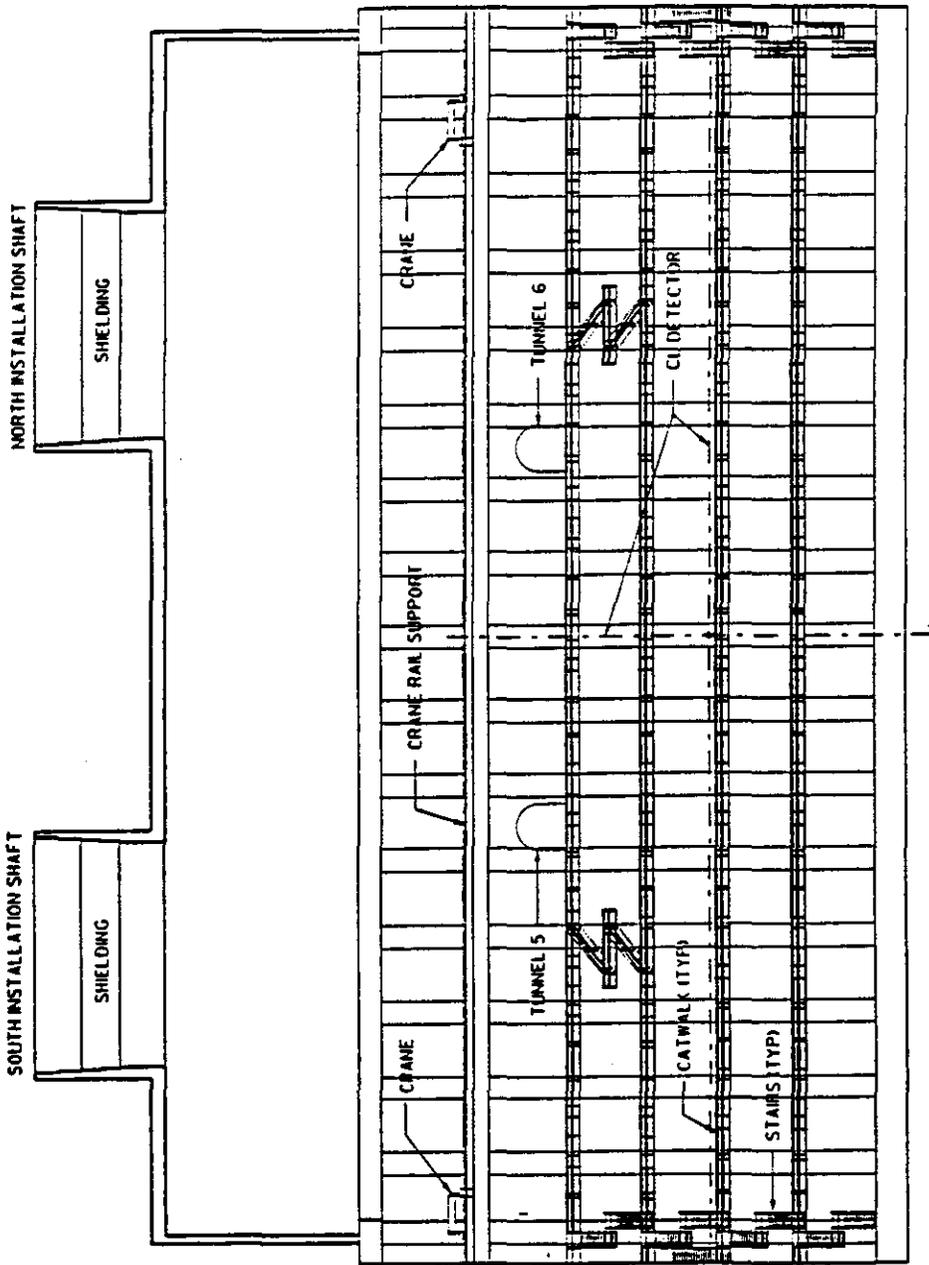
TUNNEL 5

Figure 4-12 Experimental Hall Cable Electronics Shaft Tunnels 5 & 6 Sections



gcd000201.b
 REF: gcd000236
 11-10-92
 H HAZLETT

Figure 6-2 South Assembly Building Floor Plan



9CG000184.C
REF. FILE(S): 9CG000263.B009
5 NOV 1992
HAWKES

Figure 4-6 Experimental Hall Section D-D

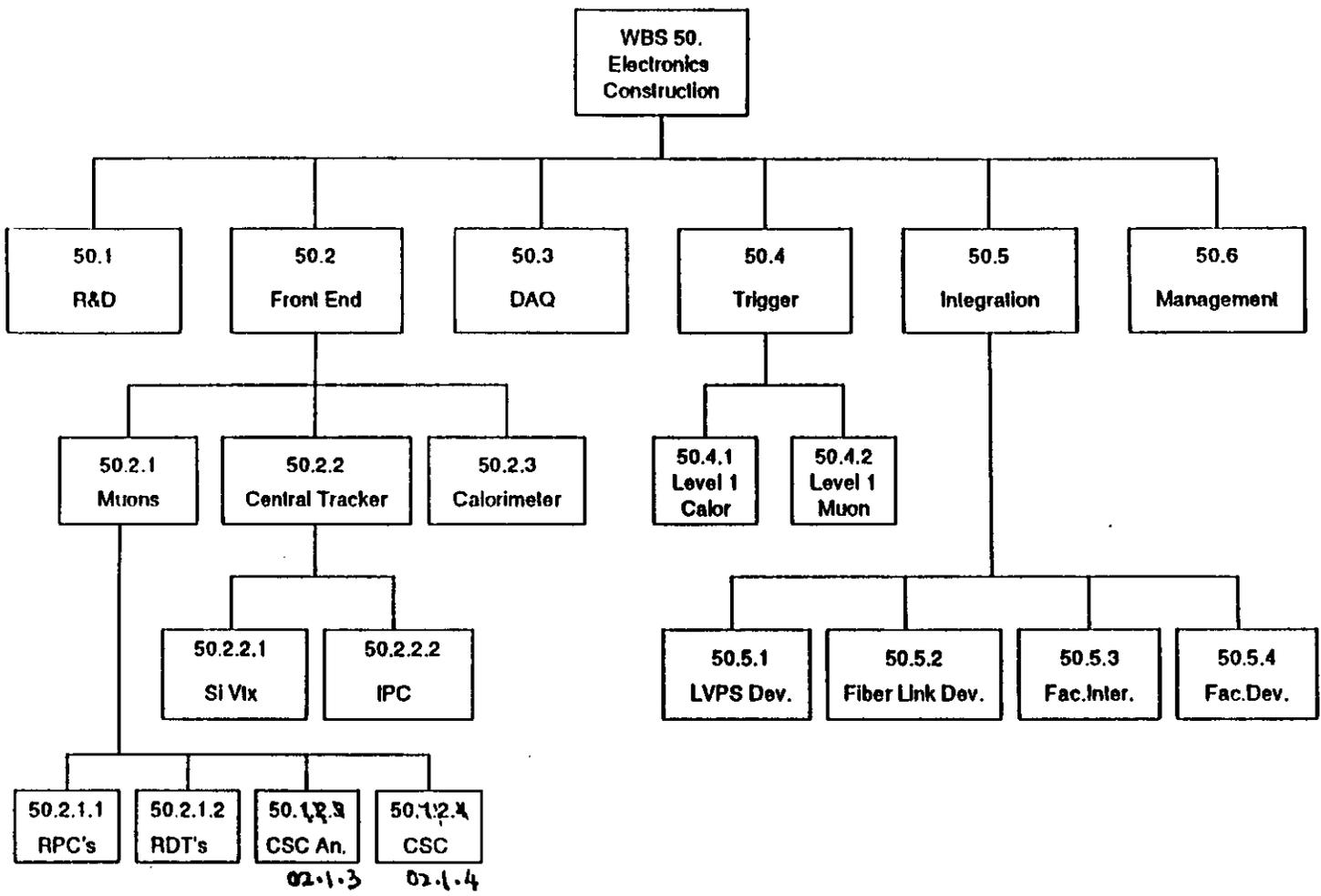


Figure 1: The overall structure of the electronics portion of the GEM WBS.

SUBSYSTEM: Integration

SSCI GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS No.: 50.05.2

WBS Descript.: Fiber link development

Estimate Type: BU

WBS QTY: _____

WBS UM: _____

Functional Activity: 1 Engineering/Design

2 Material & Services

3 Inspection/Administration

4 Procurement/Fabrication

5 Assembly

6 Installation

Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

	RISK	
	Factors	Weight %
Technical	<u>1</u>	_____
Cost	<u>2</u>	_____
Schedule	<u>4</u>	_____

304

Item Description	Qty	Unit Meas (UM)	Craft/Team Resource Code	* Unit Productivity MI/UM	k # Mat'l Unit Cost
1. Collaborate with SDC, investigate commercial fiber link to meet radiation requirements, discuss with subsystem groups for common data link	1.5	MY	SSC02	1772	
2. Travel	10	Trip			2

Notes:

Prepared by: _____

Sheet _____

SUBSYSTEM: Integration

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS No.: 50.05.3

WBS Descrip.: Facility interface

Estimate Type: BU

WBS QTY: _____

WBS UM: _____

	RISK	
	Factors	Weight %
Technical	<u>1</u>	_____
Cost	<u>2</u>	_____
Schedule	<u>2</u>	_____

Functional Activity: 1 Engineering/Design

Circle One if entire form pertains to only one category or provide description lines with appropriate code 1 - 5.

- 2 Material & Services
- 3 Inspection/Administration
- 4 Procurement/Fabrication
- 5 Assembly
- 6 Installation

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Item Description	Qty	Unit Meas (UM)	Crall/Team Resource Code	* Unit Productivity MI/UM	K # Mat'l Unit Cost
1. Interface to different groups which provide safety, reliability, radiation, magnetic field study, EFD, CCD, PB/MK, pedicement, etc.	3.0	MY	SSC04	1772	
2. Travel	5	Temp			2

Notes:

SUBSYSTEM: Integration

SSCL GEM DETECTOR
SUCCESS COST ESTIMATING INPUT FORM

WBS No.: 50.05.4

WBS Descript.: Facility development

Estimate Type: BU

WBS QTY: _____

WBS UM: _____

	RISK	
	Factors	Weight %
Technical	<u>1</u>	_____
Cost	<u>2</u>	_____
Schedule	<u>2</u>	_____

Functional Activity: 1 Engineering/Design

2 Material & Services

3 Inspector/Administration

4 Procurement/Fabrication

5 Assembly

6 Installation

Circle One if entire form pertains to only one category or precede description lines with appropriate code 1 - 5.

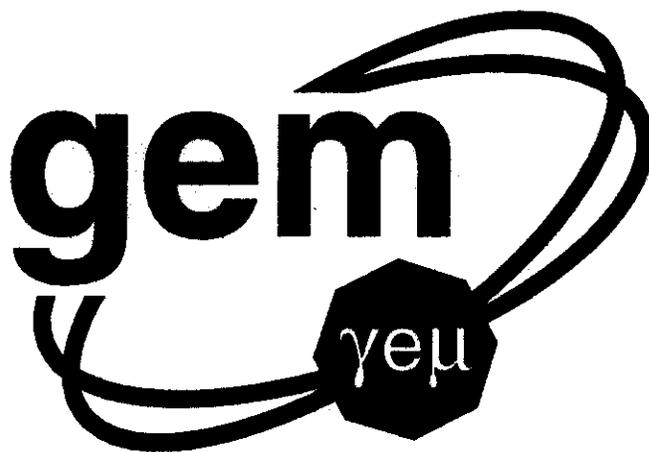
306

Item Description	Qty	Unit Meas (UM)	Craft/Team Resource Code	* Unit Productivity MI/UM	k # Mat'l Unit Cost
1. Rack design and layout, electronic room layout, cabling routing in the hall and electronic room, AC/DC power distribution	3.0	MY	SSC04	1772	
2. Travel	5	Trlp			2

Notes:

Prepared by: _____

Sheet _____



**Grounding, Shielding
& Signal Reference**

Norm Lau

Grounding, Power Distribution and Signal Reference
for
The GEM Detector

Gerald Chessmore

Ken Freeman

Norman Lau

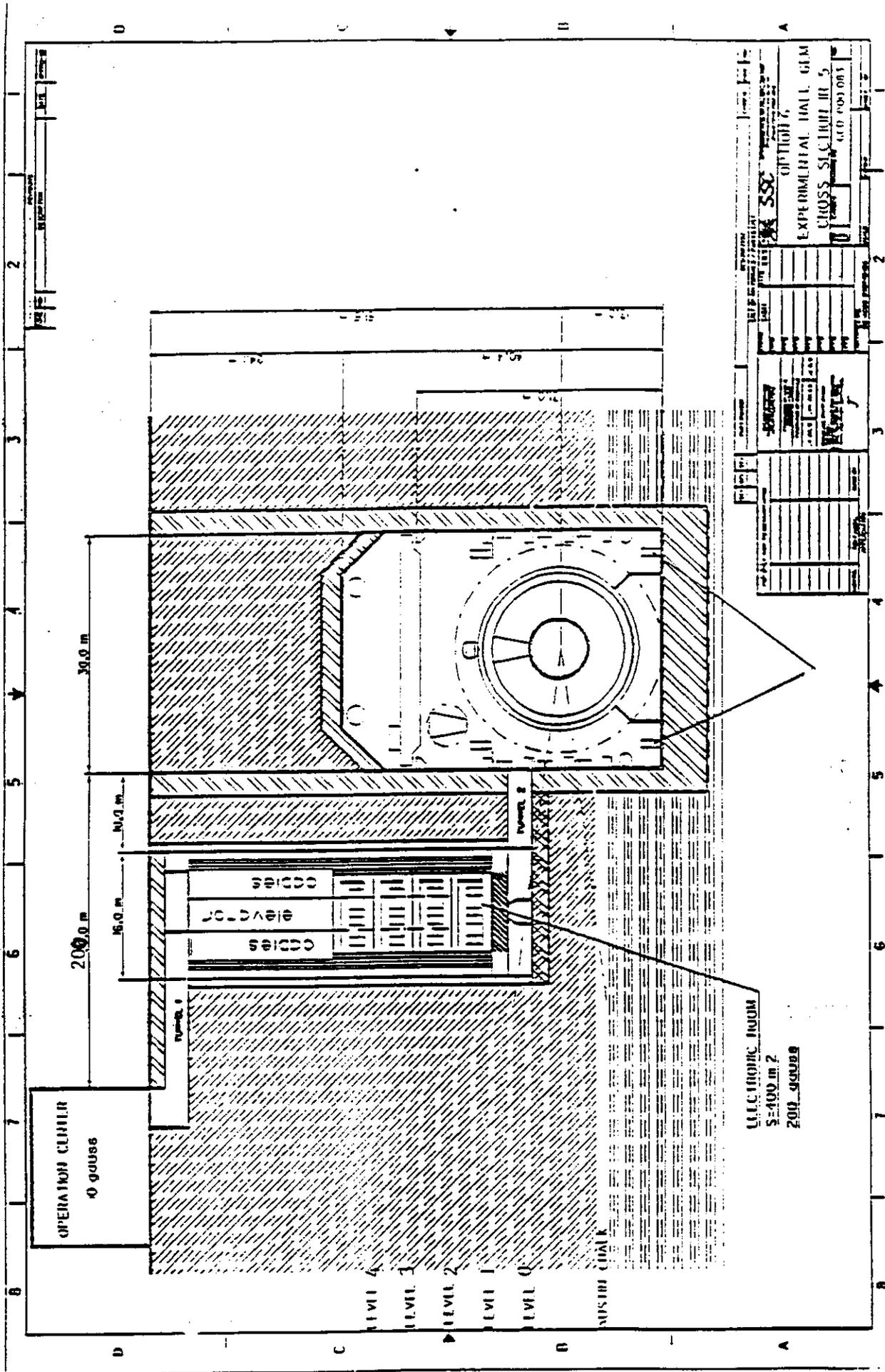
Physics Research Division

Superconducting Super Collider Laboratory



TOPICS

- o System Overview
- o Power Distribution
- o Facility Grounding System
- o Signal Reference
 - o Single Point Ground
 - o Multi Point Ground
 - o Signal Ground in the Electronics Rooms
 - o Signal Ground in the Detector Hall



OPTION 6
 EXPERIMENTAL HALL GEM
 CROSS SECTION III 5
 GEO. CONDITIONS

Operation Center
Level 3 Trigger

SURFACE

100 fibers
(134m)

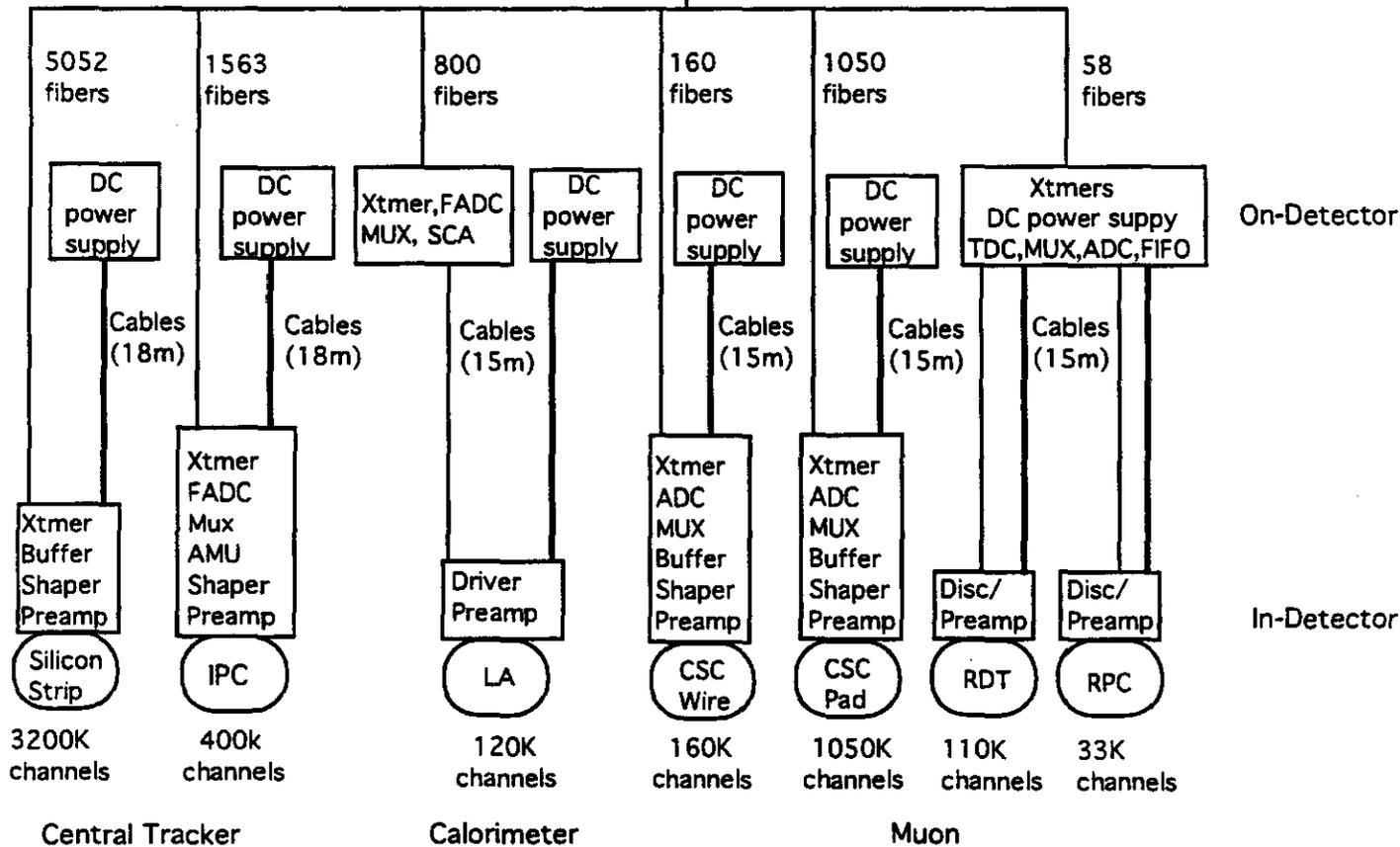
Electronic Room
Level 1 & 2 Triggers
Data Acquisition System

SHAFT

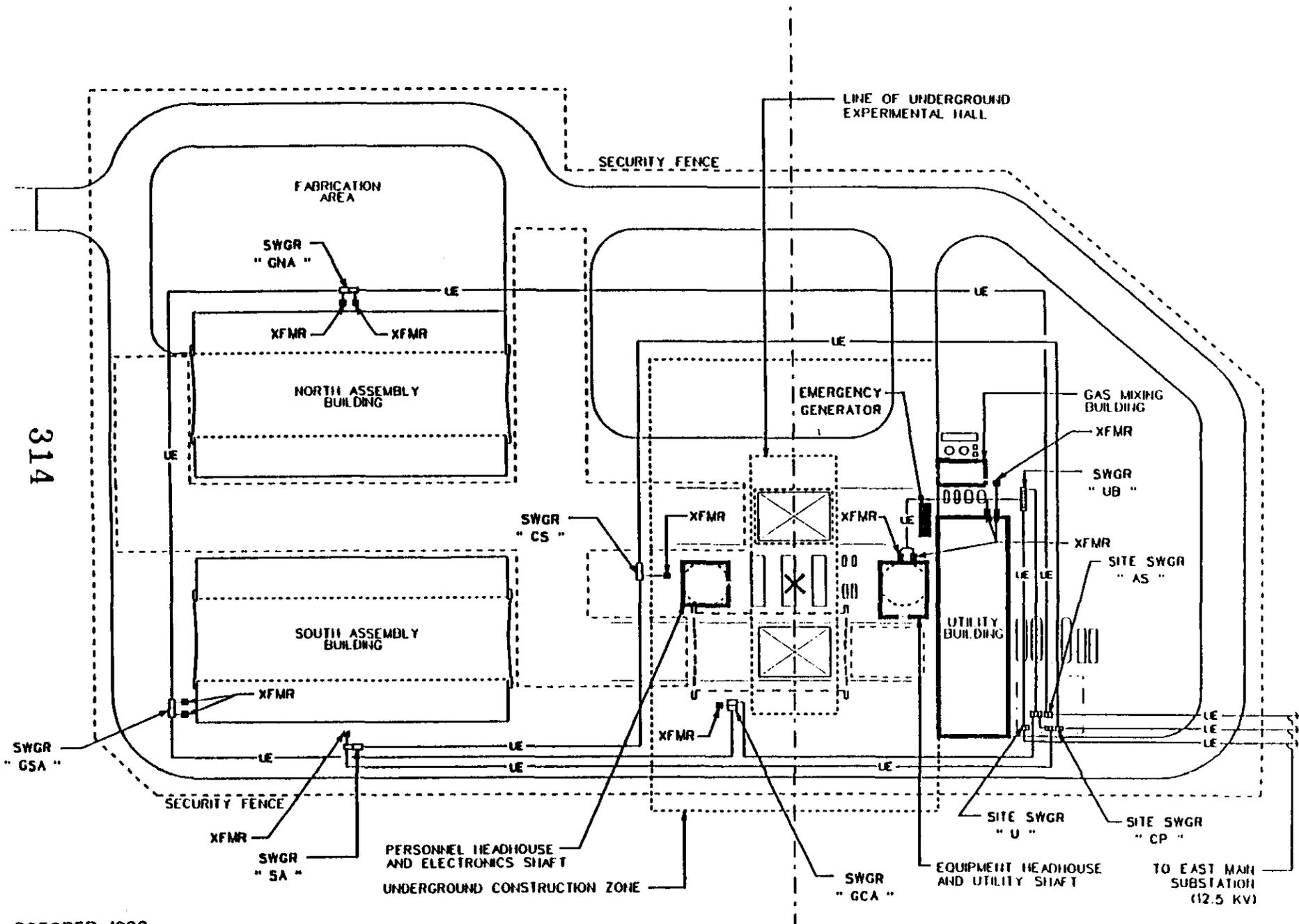
(60-100m)

HALL

Fiber Optic Cables



Electronics System Layout (November 18, 1992)



14 OCTOBER 1992
GDC/FK

FIGURE 3.1
IR-5 SITE ELECTRICAL PLAN VIEW

315

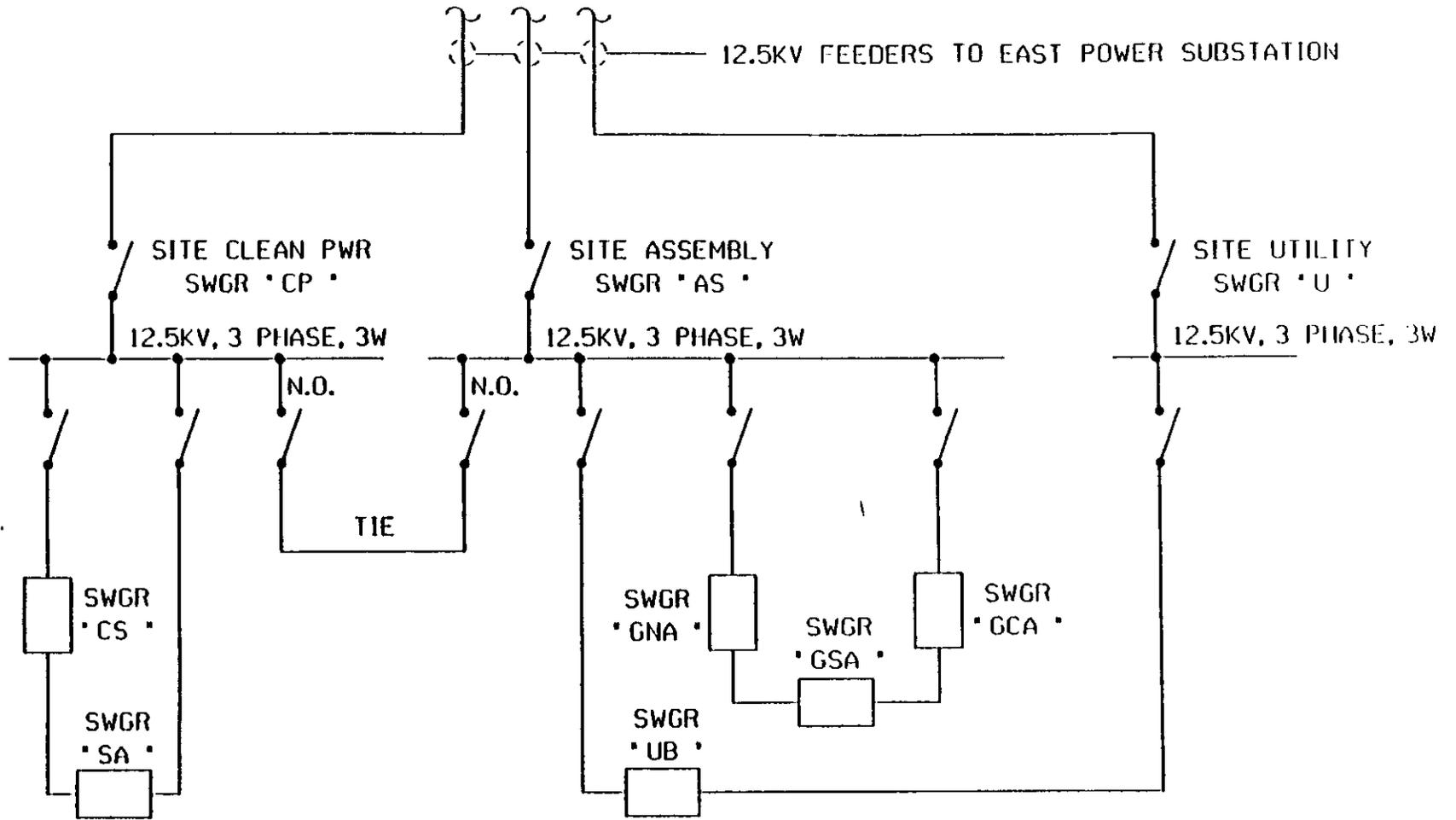


FIGURE 3.2
SITE 12.5KV PRIMARY DISTRIBUTION DIAGRAM

316

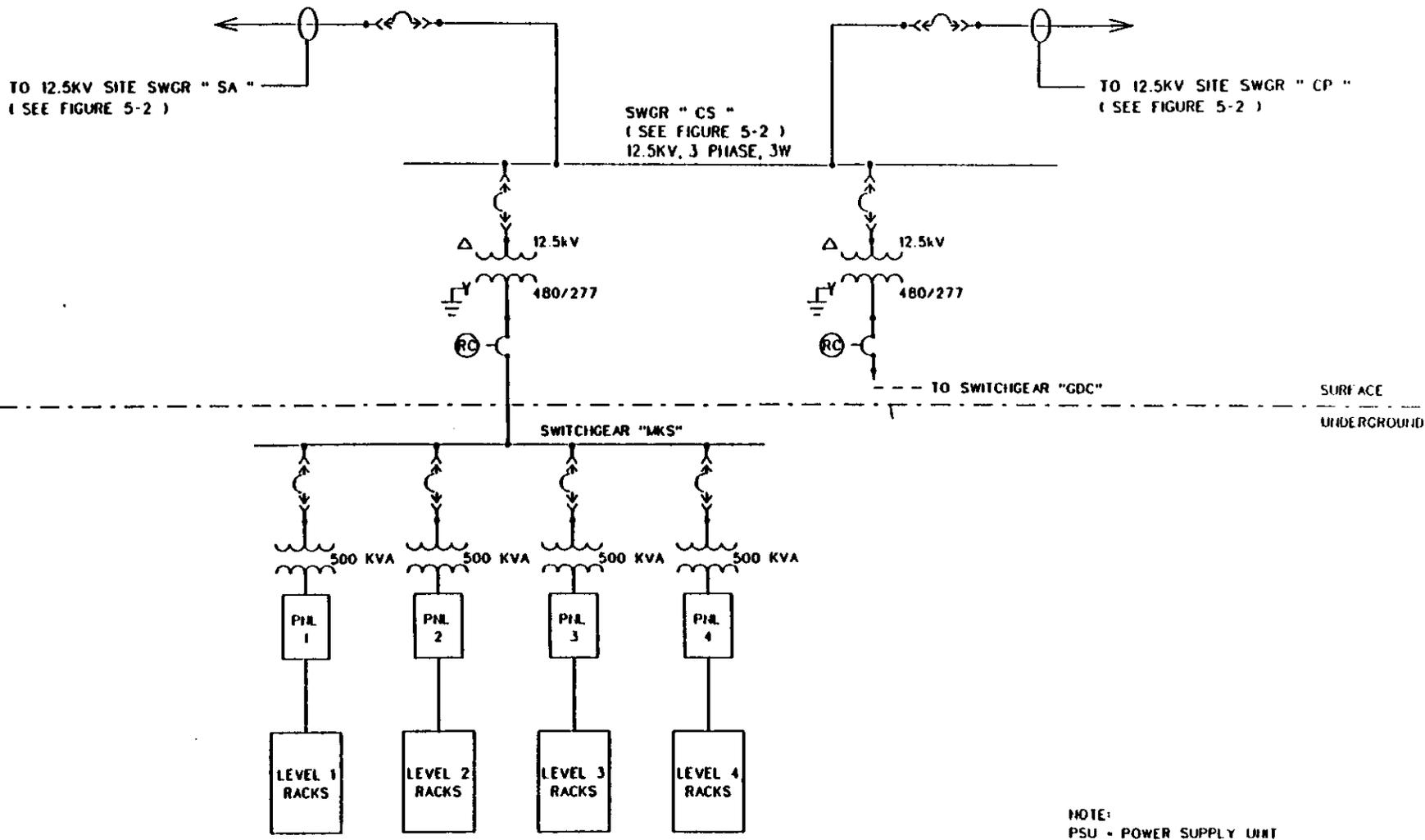
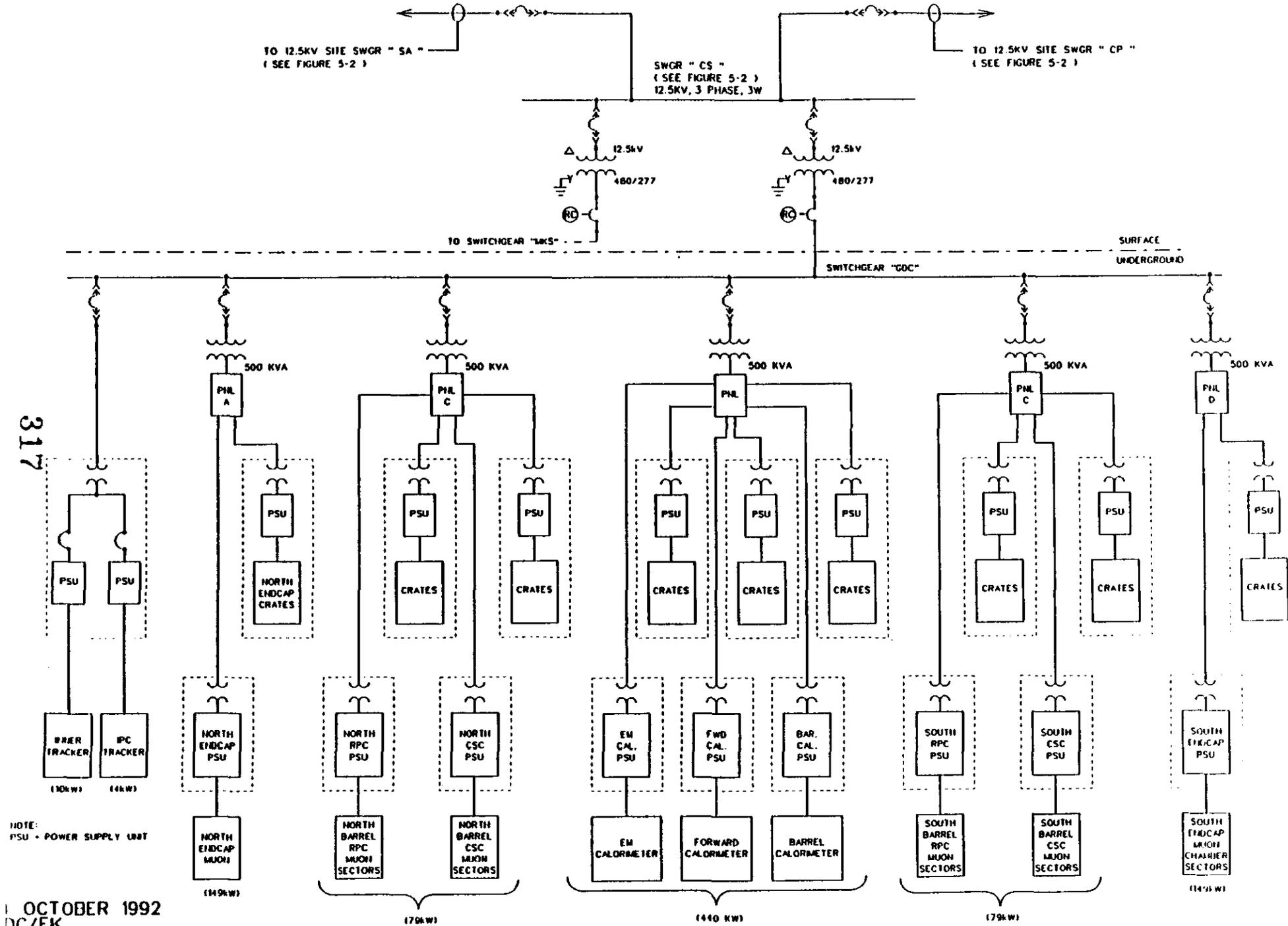


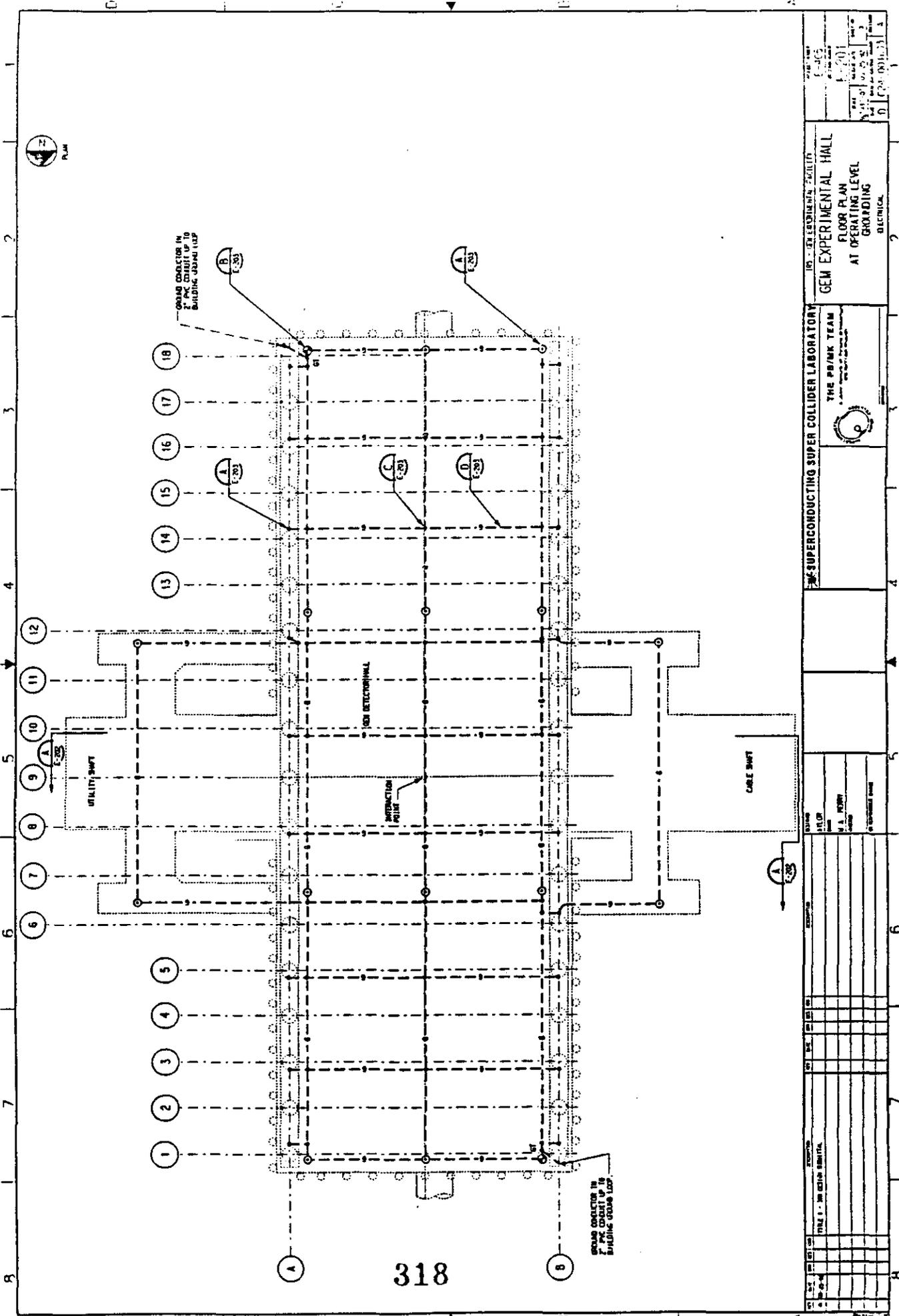
FIGURE 3.5
CABLE ELECTRONICS SHAFT POWER DISTRIBUTION

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1 OCTOBER 1992
DC/FK

FIGURE 3.4
EXPERIMENTAL HALL ELECTRICAL DISTRIBUTION DIAGRAM



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THE SUPERCONDUCTING SUPER COLLIDER LABORATORY THE P8/P8K TEAM		SSCL DETECTOR HALL FLOOR PLAN AT OPERATING LEVEL GRIDING		ELECTRICAL	
TITLE: SSCL DETECTOR HALL U.S. PATENT U.S. PATENT		DATE: 10/1/88 DRAWN BY: [Name] CHECKED BY: [Name]		PROJECT NO.: [Number] DRAWING NO.: [Number]	
SCALE: AS SHOWN		SHEET NO.: [Number]		TOTAL SHEETS: [Number]	

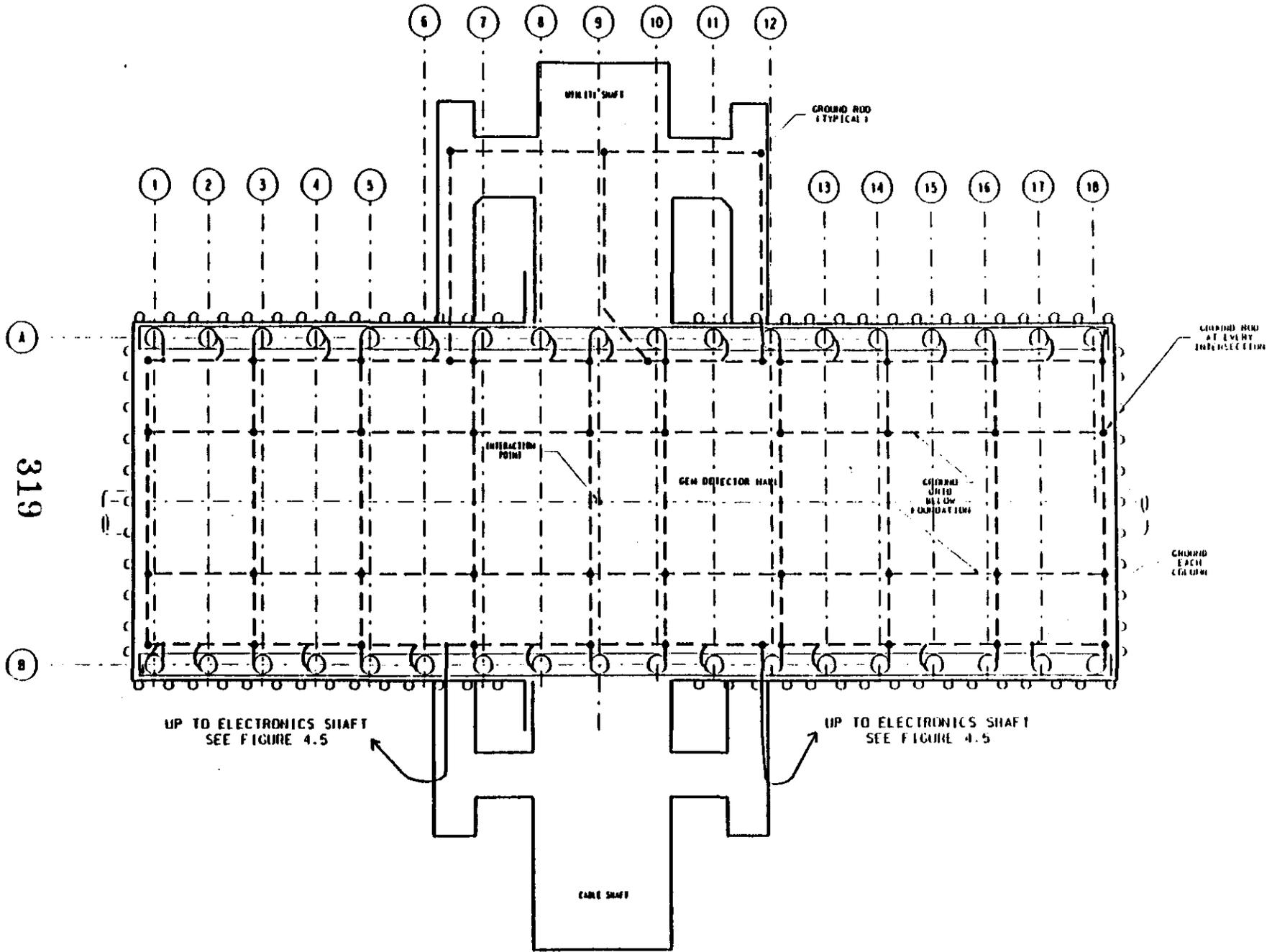
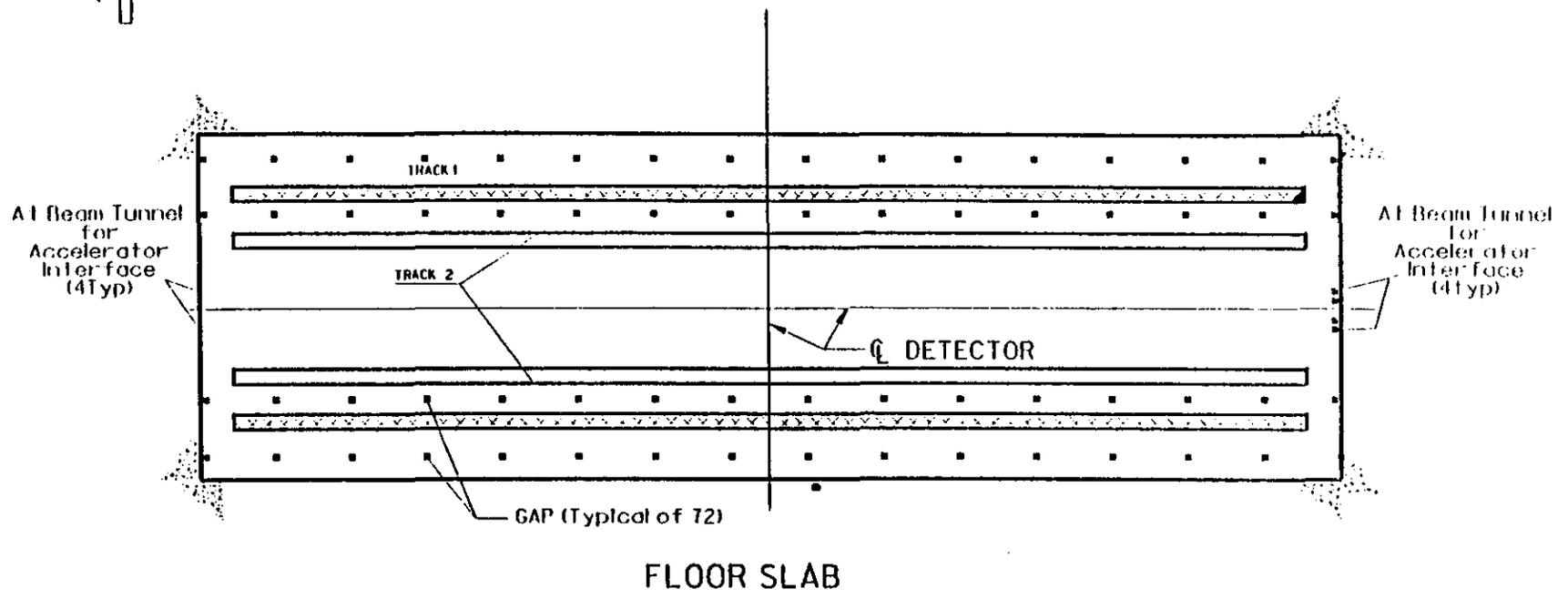
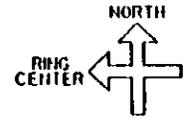


FIGURE 4.3
GEM HALL GROUNDING GRID



See Fig 4-19 for the Location of Tracks 1 and 2

Symbol	Description
■	Symbol Indicates a Grounding Access Point (GAP) for connection to the Facility Ground Grid. Coordinate exact placement/location of GAPs with structural foundations/columns, Detector/Beamline support structures, and Detector Load Paths.

gcd000366
 REF. FILE(S): NONE
 11-24-92
 F. RIBAT

Figure 18-5 GEM Grounding Access Points Locations

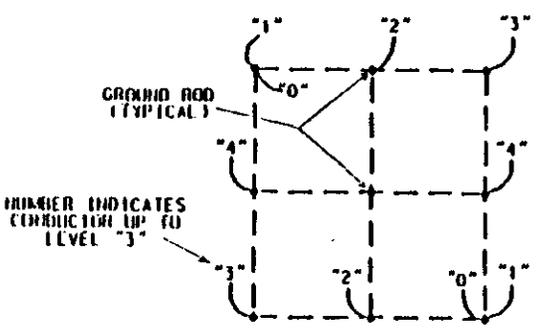
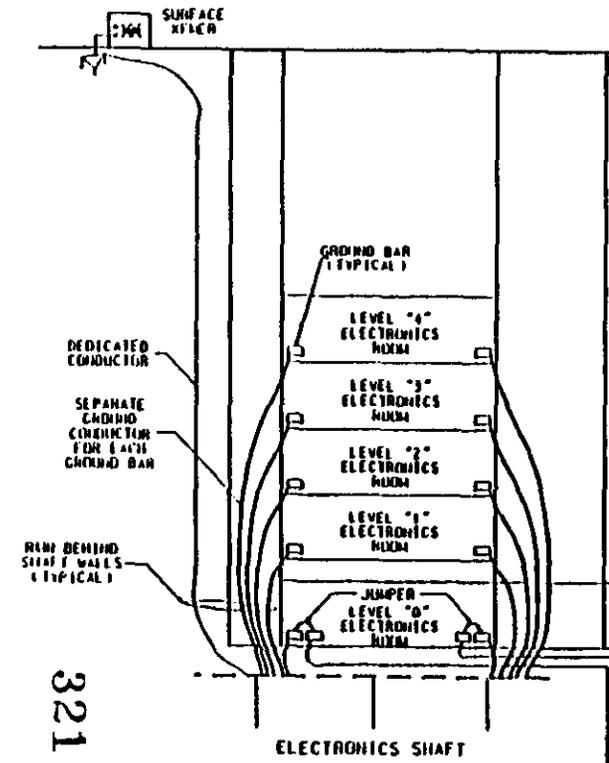


FIGURE 4.6
ELECTRONICS
GROUNDING GRID
(PLAN VIEW)

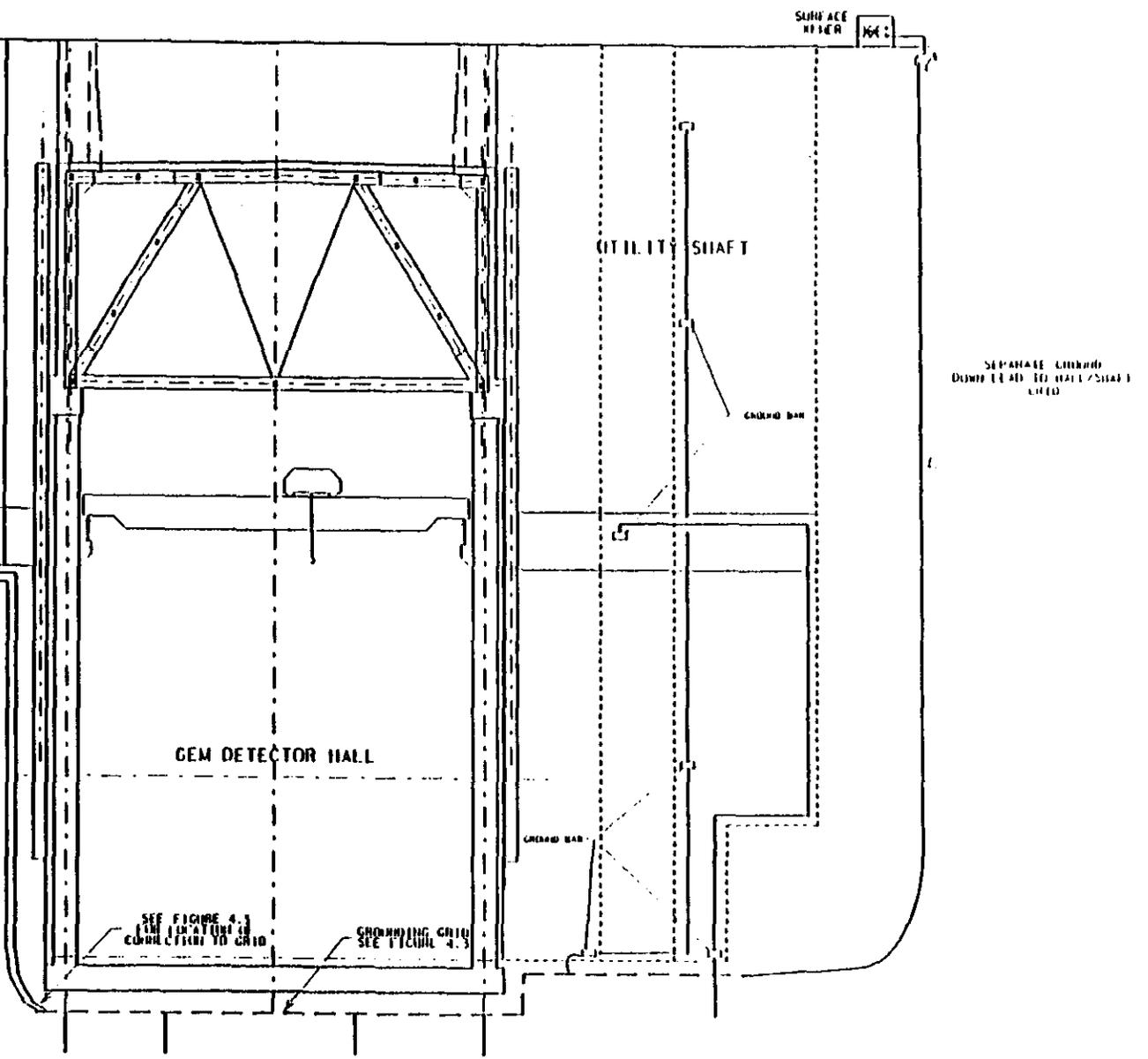
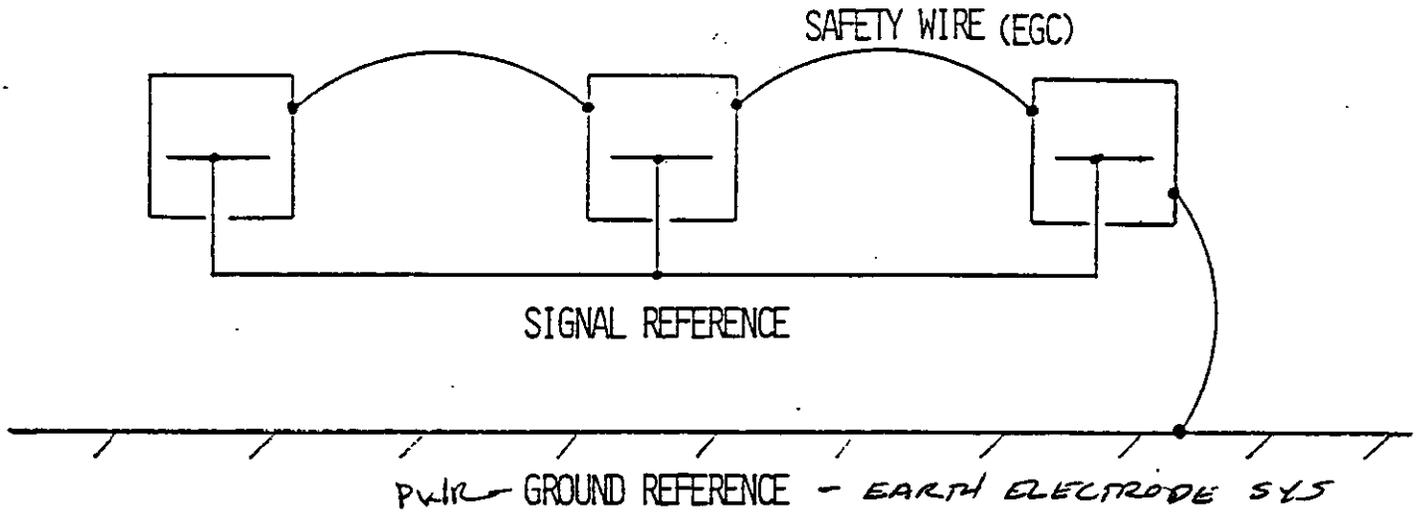


FIGURE 4.5
GEM UNDERGROUND GROUNDING

SIGNAL
IDEAL FLOATING GROUND



POWER GROUND REFERENCE - EARTH ELECTRODE SYS
- BUILDING STEEL
- PIPING
- ETC

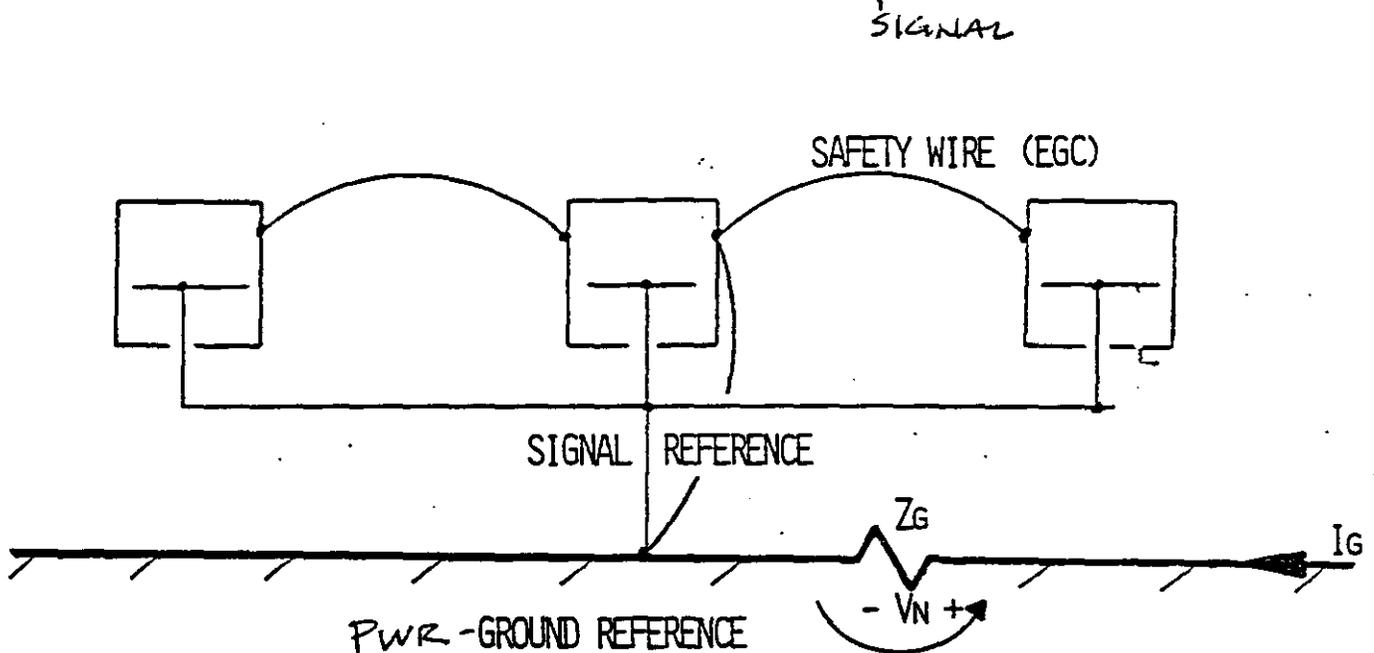
ADVANTAGES/USES

1. GROUND REFERENCE NOISE IS ISOLATED FROM SIGNAL REFERENCE.
2. USED IN SMALL ELECTRONICS EQUIPMENT.

DISADVANTAGES

1. DIFFICULT TO ACHIEVE IN LARGE SYSTEMS.
2. ESD BUILD-UP ON ISOLATED SIGNAL CIRCUITS (ESPECIALLY WHEN LOCATED NEAR HIGH VOLTAGE POWER LINES).
3. FLASHOVER BETWEEN CHASSIS AND SIGNAL REFERENCE DURING LIGHTNING.

IDEAL SINGLE-POINT GROUND



- EXAMPLES: 1. 60 Hz POWER DISTRIBUTION SYSTEM.
2. TELEPHONE CO. C O GROUND.

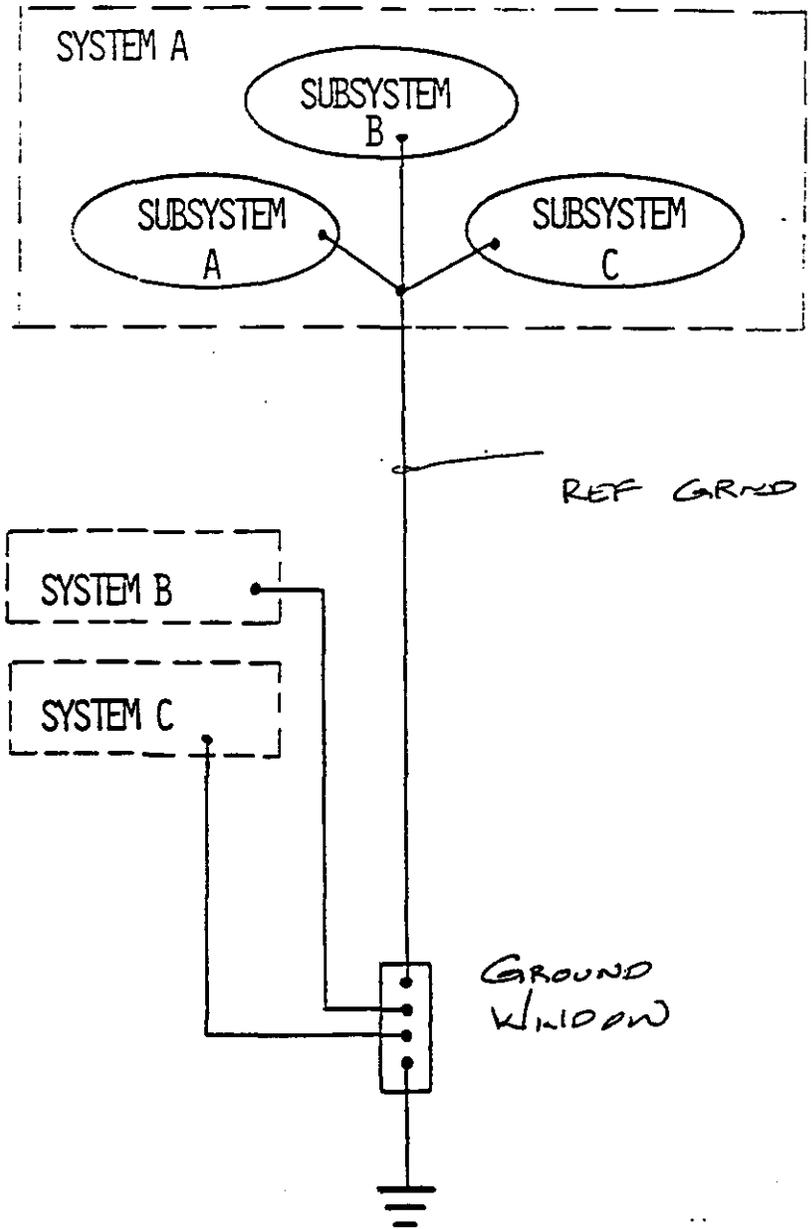
ADVANTAGES:

1. LOW FREQUENCY APPLICATIONS ONLY.
2. REDUCES CONDUCTIVELY-COUPLED NOISE BY ELIMINATING GROUND LOOPS (COMMON Z COUPLING).
3. NO ESD BUILD-UP

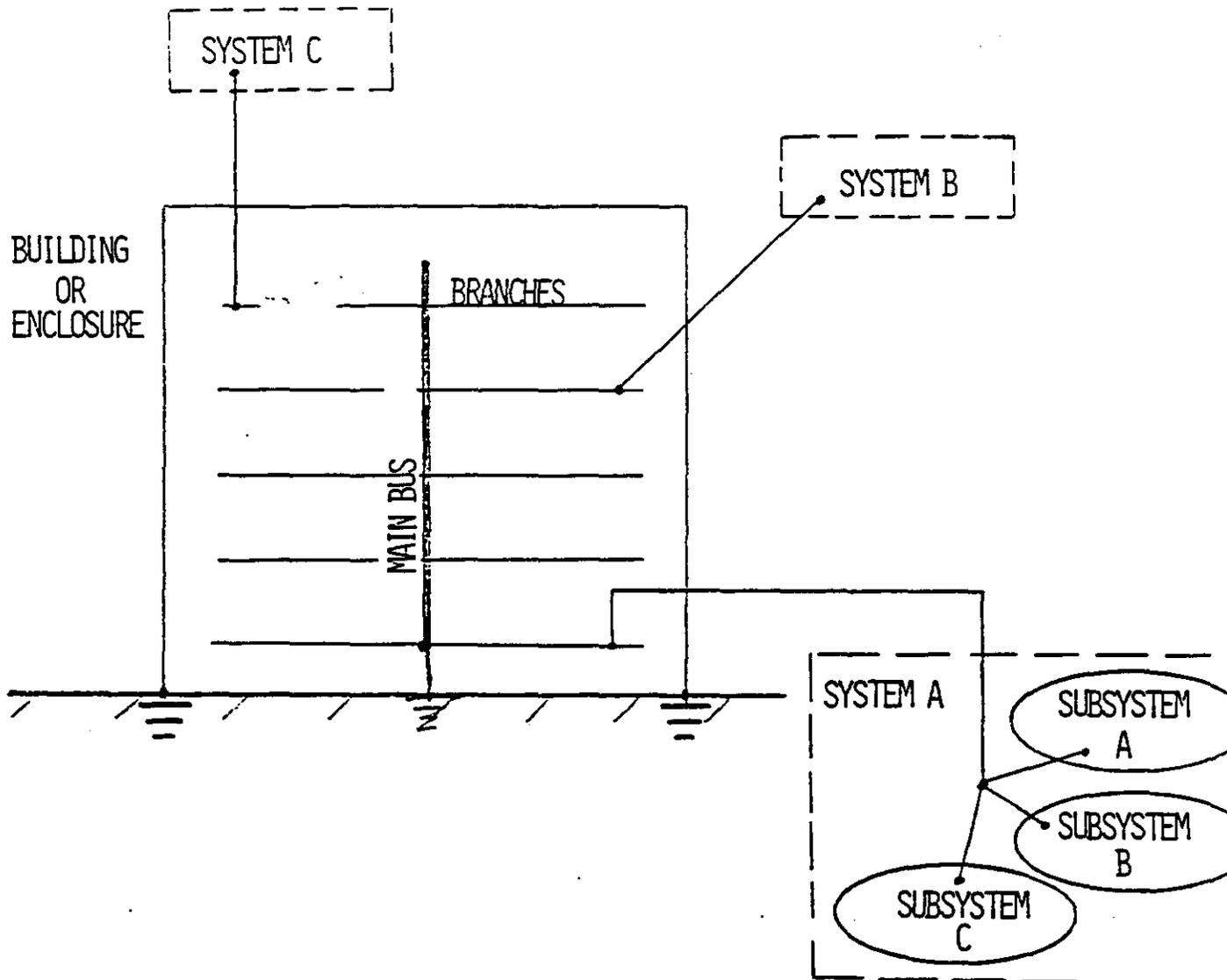
DISADVANTAGES:

1. LARGE NUMBER OF CONDUCTORS.
2. LONG CONDUCTORS.
3. BREAKS DOWN AT HIGH FREQUENCIES DUE TO ITEM 2.
4. CEASES TO EXIST AT HIGH FREQUENCIES DUE TO PARASITIC CAPACITANCE.
5. DIFFICULT TO MAINTAIN ONLY ONE CONNECTION.

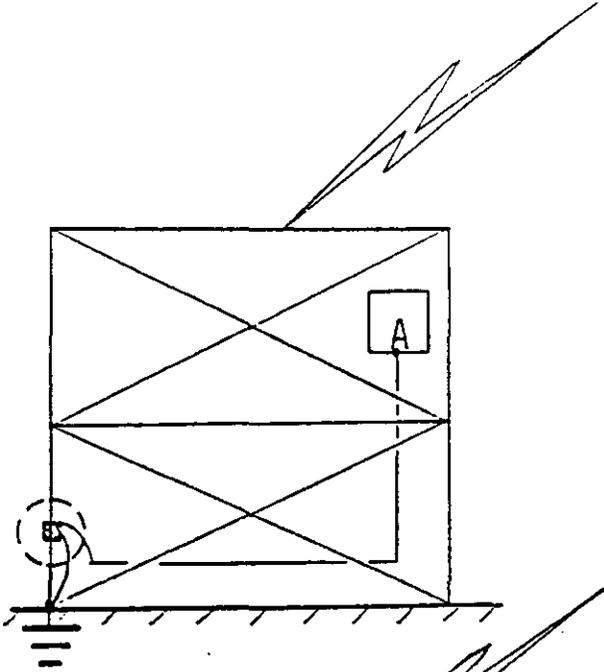
LARGE SYSTEM SINGLE-POINT GROUND
(SEPARATE RISERS)



LARGE SYSTEM SINGLE-POINT GROUND
(COMMON BUS)

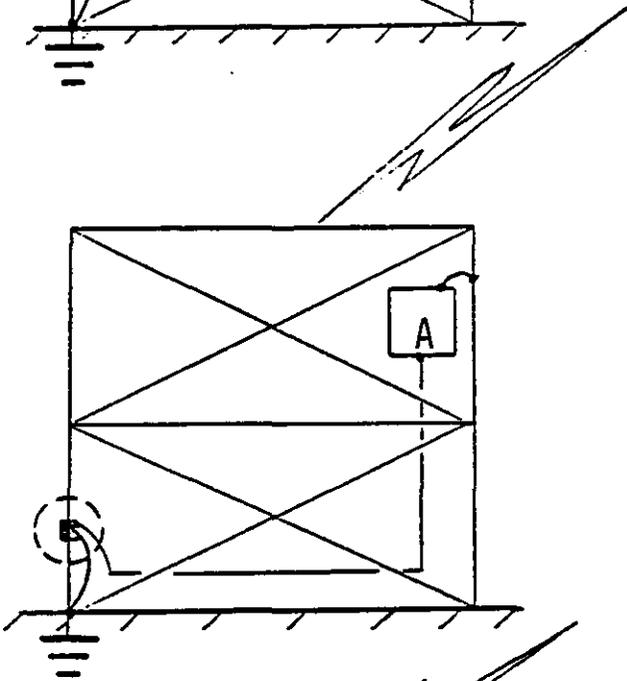


GROUND WINDOW CONCEPT



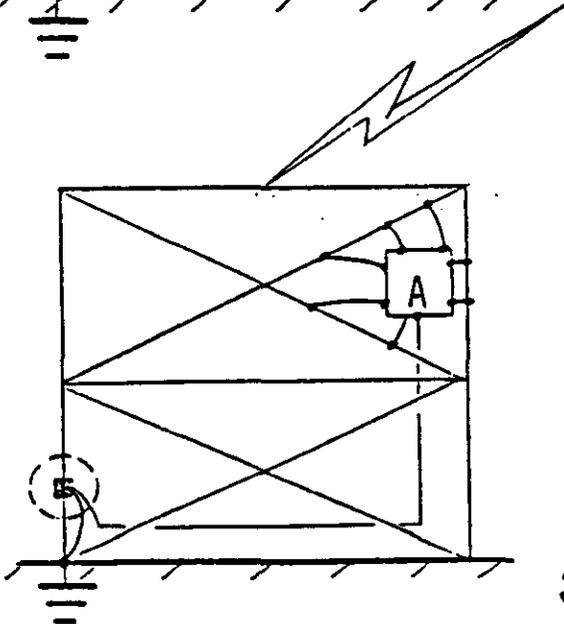
SINGLE-POINT GROUND

NO CURRENT IN COMPONENTS OF A . . .
NO V_I BETWEEN COMPONENTS.



SINGLE-POINT GROUND WITH ONE VIOLATION

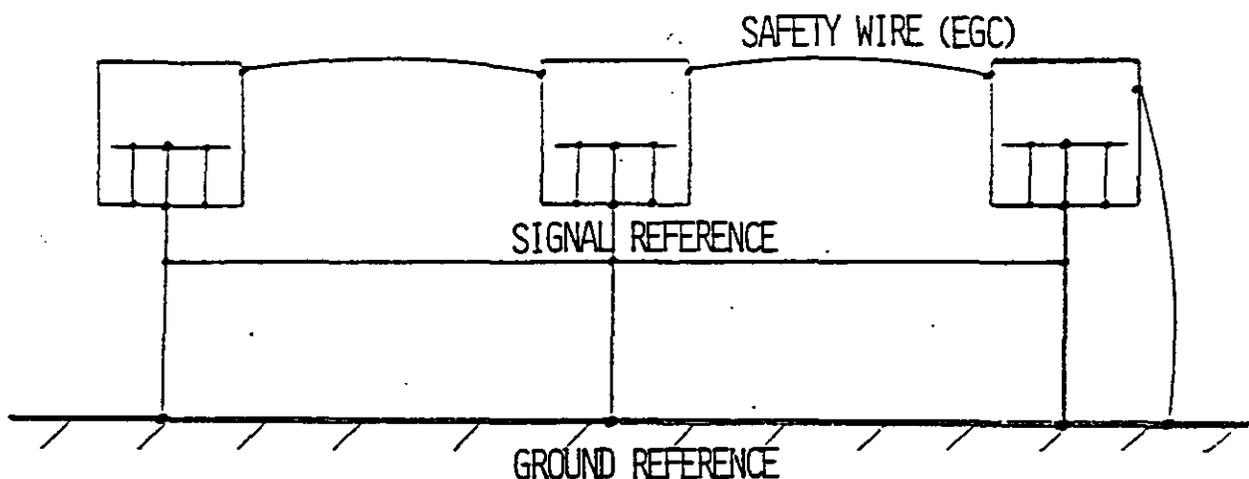
V_I PRODUCED DUE TO CURRENT FLOW.



MULTIPLE-POINT GROUND

CURRENT IS EQUALIZED THROUGH MANY
PATHS. LOW V_I ACROSS COMPONENTS
IS DEVELOPED DUE TO MANY PARALLEL
PATHS OF CURRENT FLOW.

IDEAL MULTIPPOINT GROUNDING



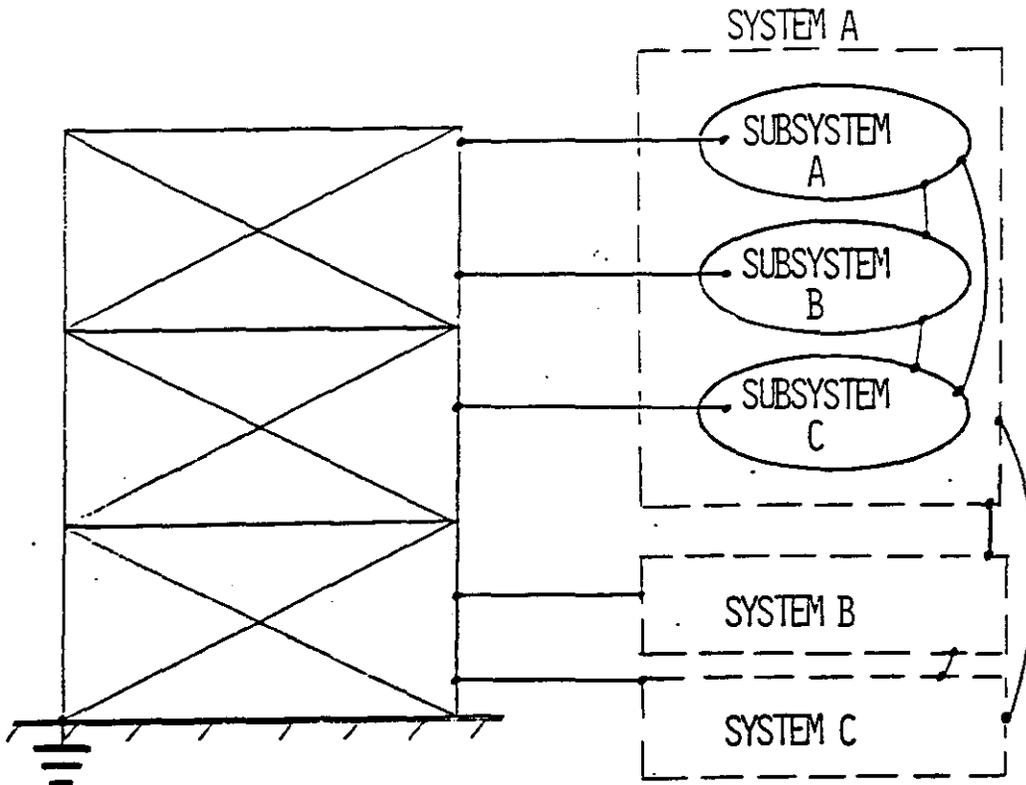
ADVANTAGES/USES

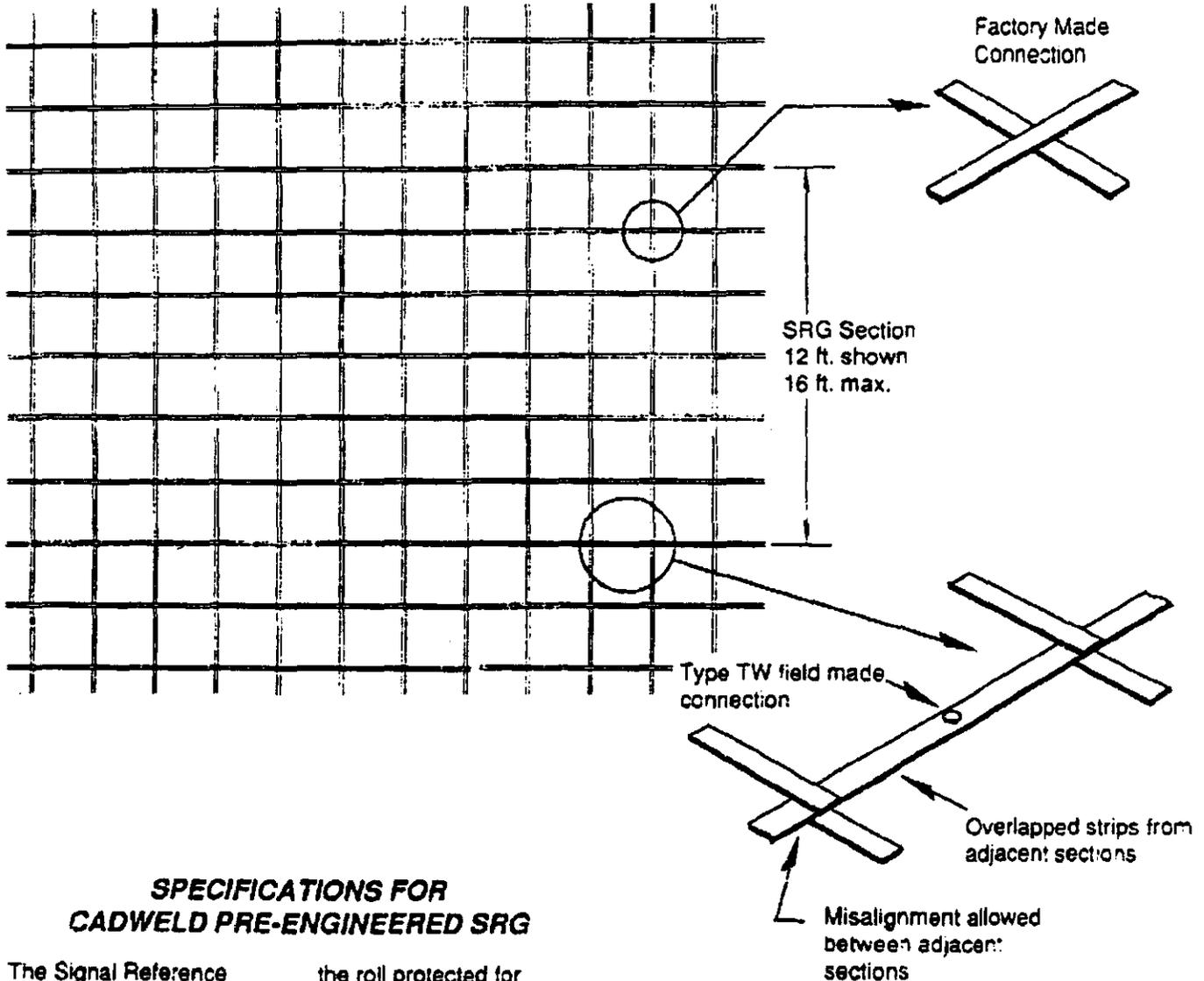
1. SIMPLIFIES CIRCUIT CONSTRUCTION FOR COMPLEX EQUIPMENTS.

DISADVANTAGES

1. REQUIRES EQUIPOTENTIAL GROUND PLANE.
2. GROUND LOOPS ARE CHARACTERISTIC. INCREASES CHANCE OF RADIATION PICK-UP.
3. 60Hz AND LOW-FREQUENCY NOISE CAN CONDUCTIVELY COUPLE INTO SIGNAL GROUND.
 - o IMPROPER WIRING SUCH AS N-G CONNECTIONS.
 - o FILTER LEAKAGE CURRENT.
 - o INSULATION LEAKAGE

LARGE SYSTEM MULTI-POINT GND SYSTEM





SPECIFICATIONS FOR CADWELD PRE-ENGINEERED SRG

The Signal Reference Grid (SRG) shall be manufactured from 2 inch wide by 26 AWG gage (0.0159 inch thick) copper strips on 2 foot centers. All crossovers shall be joined by welding. The SRG shall be furnished 4 to 16 feet wide. The sections shall be rolled on tubes with the outside of

the roll protected for shipment.

NOTES:

1. Other strip sizes are available.
2. Other spacing is available.
3. Roll weight usually limited to about 200 pounds gross weight for convenience (1200 sq. ft.).

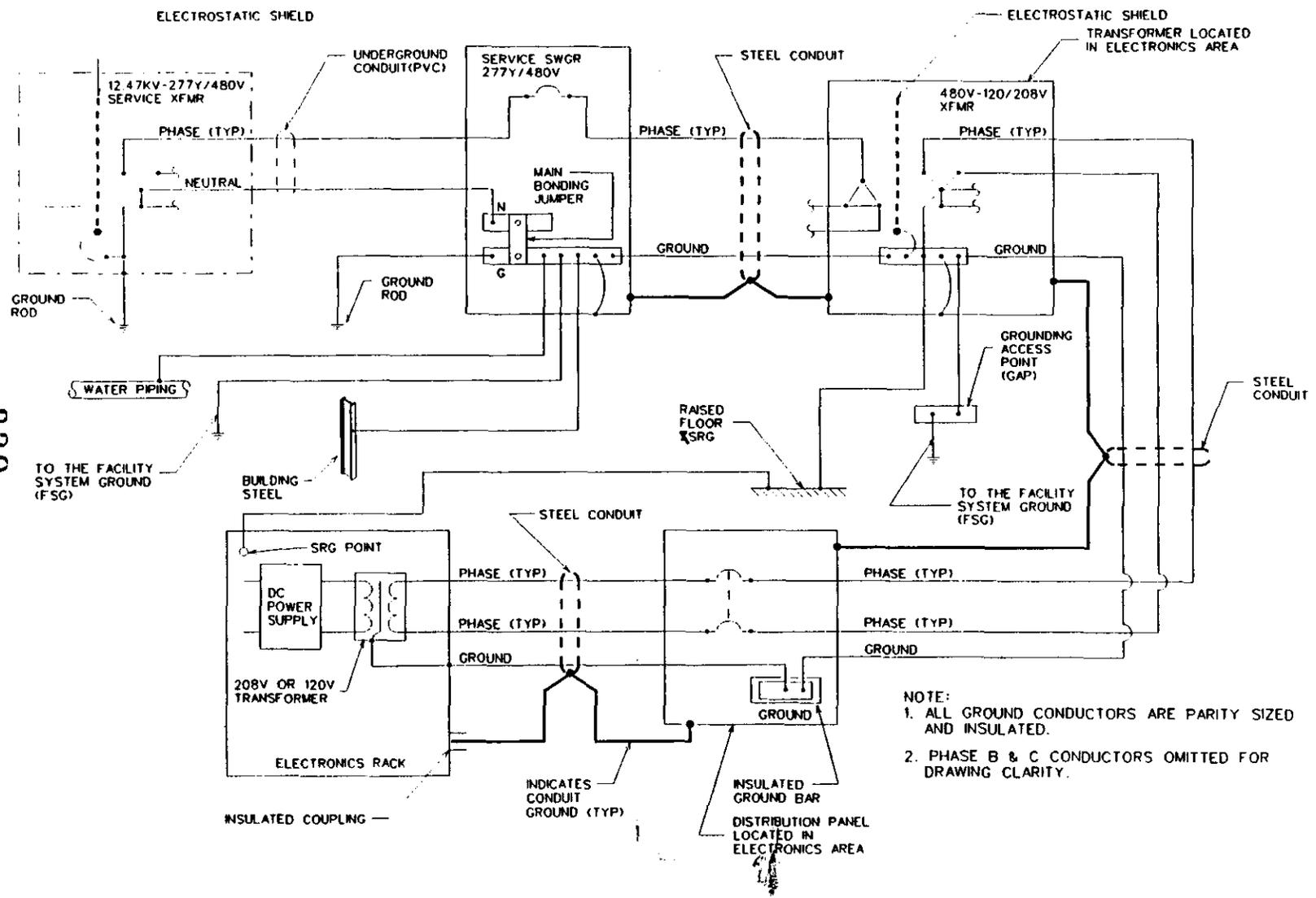
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CLEVELAND, OHIO 44139

CADWELD[®]

1-800-248-WELD
FAX (800)462-4797

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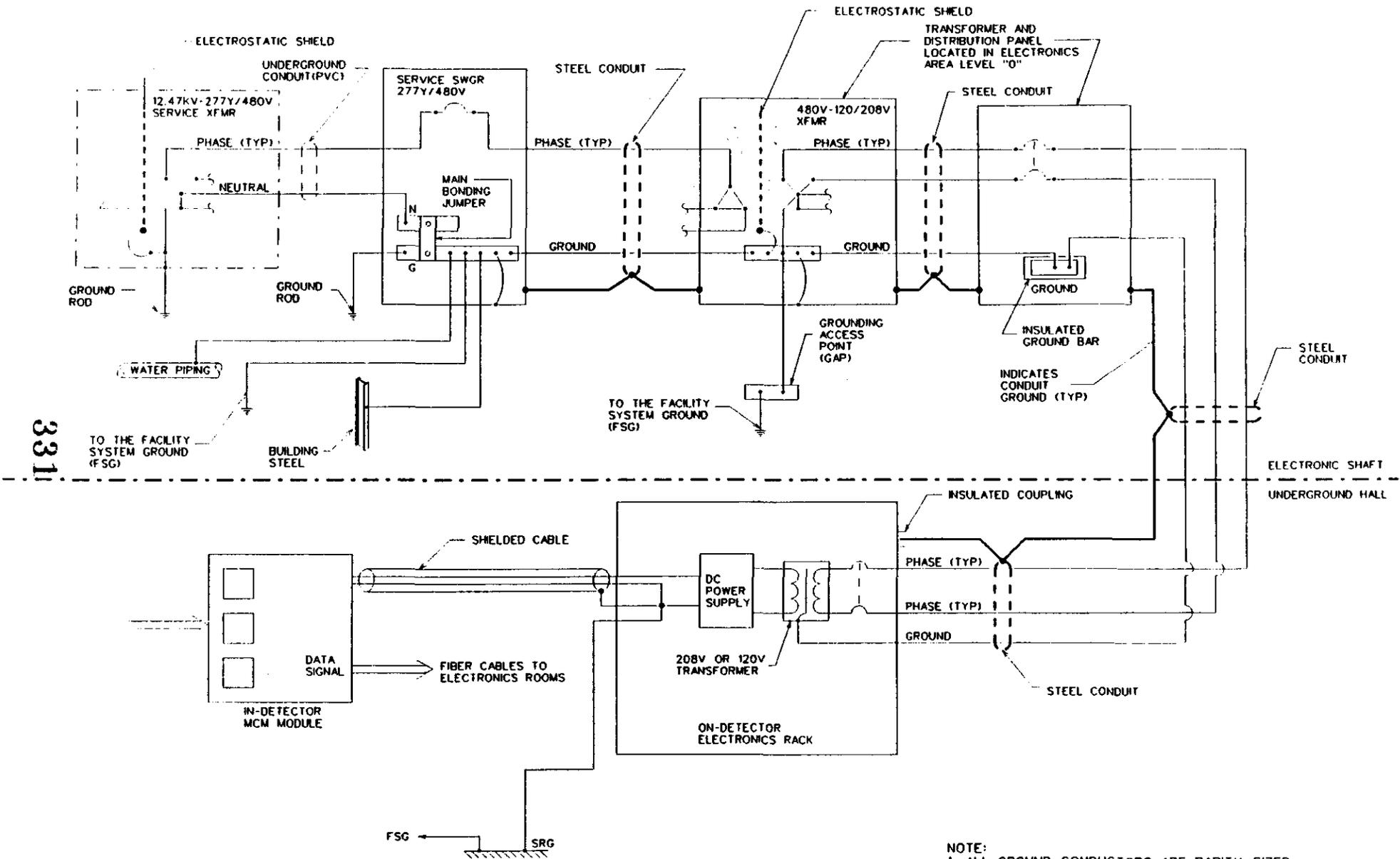


NOTE:
 1. ALL GROUND CONDUCTORS ARE PARITY SIZED AND INSULATED.
 2. PHASE B & C CONDUCTORS OMITTED FOR DRAWING CLARITY.

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 FK

gemERG

Figure 13.5 ELECTRONICS ROOM GROUNDING DIAGRAM



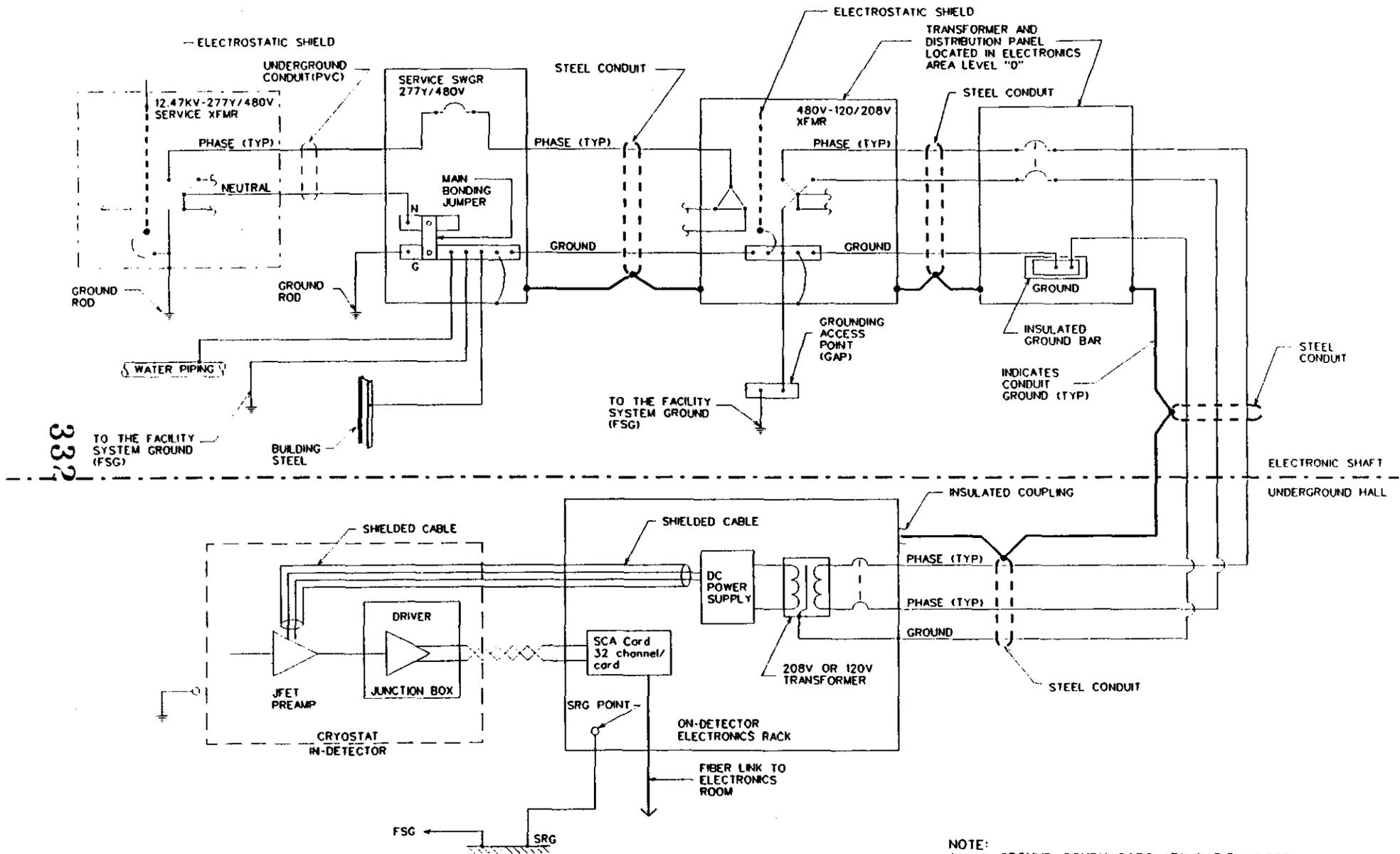
331

- NOTE:
1. ALL GROUND CONDUCTORS ARE PARITY SIZED AND INSULATED.
 2. PHASE B & C CONDUCTORS OMITTED FOR DRAWING CLARITY.

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UNDERGROUND HALL GROUNDING DIAGRAM



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NOTE:
1. ALL GROUND CONDUCTORS ARE PARITY SIZED AND INSULATED.
2. PHASE B & C CONDUCTORS OMITTED FOR DRAWING CLARITY.

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UNDERGROUND HALL GROUNDING DIAGRAM