Abstract:

Use of an innovative parallel-processing system architecture together with an instruction set allows identification of objects (particles) among the data coming from a calorimeter in a programmable manner, utilizing the information related to their shape in two- or three-dimensional form, rather than applying only a programmable threshold proportional to their energy. The architecture is flexible, allowing execution of simple algorithms as well as complex pattern recognition algorithms. It is scalable in the sense that the same hardware can be used for small or large calorimeters having a slow or fast event rate. The simple PCB board (accommodating either 16 x 3D-Flow processors or 64 x 3D-Flow processors) on a 5 in. x 5 in. board described herein will use the same hardware to build a large Level-1 programmable trigger (by interconnecting many boards in a matrix array) and capable of implementing simple or complex pattern recognition algorithms at different event input rates (by cascading boards one on top of the other). With a modular and flexible hardware one can build a scalable (a granularity of 1250 trigger towers chosen today may change in a higher granularity segmentation in the future or in a more complex pattern recognition algorithm, without throwing away the invested money) Level-1 trigger system sustaining the input rate of 60 million event per second.
1.0 INTRODUCTION

The Superconducting Super Collider is being built for the study of high-energy physics. Every 16 ns proton beams will collide, and the particles produced by the collisions must be identified and studied. Many detectors will be used to detect and identify the particles. The calorimeter (shown in Figure 1) is one of the sub-detectors used at the SSC. The two proton beams will collide in the center of the calorimeter, sending particles to the calorimeter towers in the barrel and end caps. The amount of energy can then be transferred through channels to digital processors, where the identification of particles is begun in Level-1 triggering.

Since processor technology is advancing rapidly, it is now feasible to have real-time, programmable algorithms down to the Level-1 trigger.

This report describes the hardware implementation of a scalable, programmable, parallel-processing system architecture for the Level-1 trigger.

Each processor in the pipelined system executes entirely the algorithm of pattern recognition.

Data distribution of the information sent by the calorimeter, as well as the flow of results to the output (to the XILINX Field Programmable Gate Array), is controlled by a program sequence instruction rather than from a multiplexer.

FIGURE 1. Conceptual view of a Calorimeter
2.0 PROCESSOR ARRAY VERSUS CALORIMETER ARRAY

2.1 Present calorimeter segmentation for GEM experiment

Figure 2 shows lengthwise cross section and a side view of the end caps of the same calorimeter (seen in Figure 1), is shown in Figure 2. In the GEM experiment at the SSC, each individual tower of the calorimeter is divided into fifty "em" sections and sixteen "had" sections (see bottom right of Figure 2), for the purpose of the Level-1 trigger, the "em" sections are combined into one value, and the "had" sections are combined (see below).

The geographical representation of the calorimeter can be related to a processor array. Each calorimeter tower (consisting of an “em” part and a “had” part) has a one-to-one correspondence with a processor cell in the processor array (see bottom left of Figure 2). A description of GEM trigger tower as it relates to the simplified towers is shown on the right of Figure 2. The size of the processor array depends on the segmentation and granularity of the calorimeter.

Figure 2 shows the types of possible investigations that can be done on such a processor array in order to identify particles and obtain the relevant information. A listing to the right of the matrix is provided.

<table>
<thead>
<tr>
<th>Experiment</th>
<th>Subsystem</th>
<th>$\Delta\eta \times \Delta\phi$</th>
<th>Total number of channels at full granularity</th>
<th>Macro-granularity for Level 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>GEM</td>
<td>EM</td>
<td>0.032 x 0.032</td>
<td>30,000 x 2</td>
<td>1250</td>
</tr>
<tr>
<td>HAD</td>
<td>0.8 x 0.8</td>
<td>5000 x 4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
\[ \eta = -\ln(\tan \frac{\theta}{2}) \]

**FIGURE 2. Processor Array versus Calorimeter array.**
3. PROGRAMMABLE TRIGGER ALGORITHM EXAMPLES

Figure 3 shows a few examples of programmable trigger algorithms. The 3D-Flow system is not limited to the execution of these examples, but any algorithms can be implemented by executing in the 3D-Flow processor a sequence of steps that are part of the 3D-Flow instruction set. Figure 4 shows a flow chart of an algorithm.

Local maximum

\[
\begin{array}{c}
\text{C > I}_i \text{ for } i = 1, \ldots, 8. \\
\text{Threshold} < \sum_{i=1}^{8} \text{I}_i + C.
\end{array}
\]

**FIGURE 3. Trigger algorithms examples.**
Phase 1:  
- "em" > threshold  
  - yes: set code  
  - no:  

Phase 2:  
- "had"/"em" < threshold  
  - yes: set code  
  - no:  

Phase 3:  
- isolated?  
  - no: possible jet?  
  - yes: set code  

Output code:  
1. two "em" sum (north 1 x 2) > threshold  
2. two "em" sum (east 2 x 1) > threshold  
4. "had"/"em" (north 1 x 2) < threshold  
8. "had"/"em" (east 2 x 1) < threshold  
16. isolation achieved  
32. possible jet found

FIGURE 4. Algorithm flowchart. For example, a 3D-Flow processor may return a code 37 (1+4+32) stating that a possible electron was found, but it was not isolated from the surrounding energy, and that cell may be part of a 4 x 4 jet.
4. 3D-FLOW PROCESSOR CELL ARCHITECTURE

The architecture of the 3D-Flow processor cell is shown in Figure 5. The core of the cell of the 3D-Flow processor is identical for the entire 3D-Flow array processor system.

The 3D-Flow operates on a data-driven principle. Program execution is controlled by the presence of the data at the five ports (North, East, West, South, and Top) according to the instructions being executed. A clock running at a frequency of 60 (or 120) MHz synchronizes the operation of the cells. At each input port of the 3D-Flow processor there is a FIFO that is derandomizing the data from the calorimeter to the processor array. North, East, West and South ports are bidirectional on separate lines for input and output, while Top port is input only and the Bottom port is output only.

At each clock, a three-ring bus system allows input of data from a maximum of two ports and to output a maximum of five ports. During the same cycle, results from the internal units (ALU, etc.) may be sent through the internal ring bus to a maximum of five ports. Each 3D-Flow cell may execute different 64-line code programs. When it is issued an input instruction from a 3D-Flow cell and the data is not present, that particular 3D-Flow cell waits until the data becomes available before resuming execution.

FIGURE 5. 3D-Flow processor
5. LOGICAL LAYOUT OF THE PROGRAMMABLE LEVEL-1 TRIGGER

The overall layout of the GEM programmable digital Level-1 calorimeter trigger with its related timing is shown in Figure 6. Signals arrive from the calorimeter through optical fibers after approximately 951 ns at a rate of 60 MHz (six signals for each trigger tower covering an area of approximately 0.16 μm x 0.16 μm). The 3D-Flow parallel-processing system with timing information is shown in Figure 7. The signals arriving from the calorimeter are converted from optical to electrical (at right of figure), are processed in the 3D-Flow programmable parallel-processing system (center part of figure), are sent to the total Et, Ex, Ey, number of jets, etc., logic (left part of figure) and sent to the global Level-1 trigger (shown in the Figure 6).

![Diagram of Programmable Digital Level-1 Trigger Logical Layout](image)

**FIGURE 6.** Logical Layout of the Programmable Digital Level-1 Trigger

5.1. 3D-Flow Pipelined parallel-Processing Architecture.

In the pipelined parallel-processing architecture (see Figure 7), each processor executes entirely the algorithm of pattern recognition. Data distribution of the information sent by the calorimeter, as well as the flow of results to the output, is controlled by a sequence of instructions residing in the program memory of each processor.
The program execution at stage 1 (center part of Figure 7) must not only route the new incoming data from the calorimeter to the next stage in the pipeline staging (stage 2), but must also execute its trigger algorithm. It then sends its results to the stage 2 processor, which passes it on. At this point the stage 1 processor begins to reexecute its algorithm: receiving the electromagnetic and hadronic values from the calorimeter and processing those values. The output results from all processors flow (like the input data) through the different processor stages. The last processor will output the results from all processors at the rate of 16 ns.

FIGURE 7. General scheme of the pipelined parallel-processing architecture using 3D-Flow processors.
6. PHYSICAL LAYOUT OF THE PROGRAMMABLE LEVEL-1 TRIGGER

Figure 8 shows the path of the signals for a Level-1 trigger associated with its timing and its physical position.

7.0 3D-FLOW CHIP ASSEMBLY

A price/performance market study led to design of an economical 3D-Flow processor chip with only four 3D-Flow processor cells (Figure 9). This will require 50,000 to 80,000 gates, depending on the technological process used and functionality of the processor.

Among the more economical packages available are the Quad Flat Packs (QFPs) and the Land Grid Package (LGA). A 3D-Flow chip accommodating four 3D-Flow processors could be packaged in a 25 mm x 25 mm LGA.
8. 3D-FLOW BOARD LAYOUT

The basic element for the construction of a programmable Level-1 trigger suitable for different calorimeter sizes and with different event rates is a PCB board with 16 x 3D-Flow processors (4 chips in 4 in. x 4 in.) or a PCB board with 64 x 3D-Flow processors (16 chips in 5 in. x 5 in.).

The difference in using one of the two boards is the following. The PCB board (5 in. x 5 in.) with 64 x 3D-Flow processor will cost more but it will allow us to build a system equivalent to the 16 x 3D-Flow PCB boards in almost half size in diameter and height.

Edge connectors of the PCB board of Fig. 10 have 120 contacts each (spaced 0.050 in.). The board-to-board signal transmission is made through button contacts of the type shown in Fig. 11. The 3D-Flow chips assembled on the 16 x 3D-Flow processor board can be packaged in QFP or in LGA, while the 3D-Flow chips assembled on the 64 x 3D-Flow processor board can use the Multi Chip Module (MCM) or the Tape Automated Bonding (TAB) technique.
FIGURE 10. Board Layout of Four 3D-Flow chips Each containing 4 x 3D-Flow Processors

FIGURE 11. 3D-Flow boards assembly
9. 3D-FLOW SYSTEM ASSEMBLY

Different programmable Level-1 trigger systems can be built for different calorimeter sizes and event rates. If the number of trigger towers increases (for larger calorimeters), the diameter of the electronic trigger racks will increase. If the complexity of the pattern recognition algorithm increases and more steps are required for a refined identification of particles, the number of 3D-Flow PCB boards stacked (cascaded) one on top of the other will increase (see Figure 11).

Figure 12 shows details of the 3D-Flow programmable parallel processing system crate assembly. Figure 13 shows the layout and dimensions of the complete digital Level-1 trigger system for GEM calorimeter during assembly and Figure 14 shows the same system during operation.

The input data as shown in Figures 14, will travel from the calorimeter through optical fibers, to a receiver circuit (converting serial data to parallel digital data) that is accommodated at the external part of the 3D-Flow rack cylinder. The reduced output data (e.g., from 60 MHz to 100 KHz) will be correlated by an array of XILINX (Field Programmable Gate Array) circuits accommodated in the internal part of the 3D-Flow rack cylinder.

FIGURE 12. 3D-Flow crate details.
FIGURE 13. 3D-Flow crate during assembly.
FIGURE 14. 3D-Flow crate during operation