GEM TN-92-239

Electronics Meeting - Brookhaven National Laboratory

Session Chairs: M. Shaevitz, D. Marlow

November 5, 1992

Abstract:

Agenda and presentations of the GEM Electronics Subgroup Meeting held at Brookhaven National Laboratory on November 5, 1992.

Preliminary Agenda ...
Collaboration Meeting at BNL
Thursday, November 5, 1992

Time	Topic	Speaker/ Discussion Leader
8:30	Introductory Remarks	Marlow/Shaevitz
entral Tracker		
8:35	Si Vtx Electronics	Mills*
8:45	IPC Electronics: Status and Front-End Simulation Study	Musser
9:15	IPC Preamp Status	O'Connor
alorimeter Readout I		
9:30	Update on Dynamic Range and Zero-Suppression Studies	Prebys
9:40	LKr Preamplifier/Cable Driver Status	Rescia*
9:55	LKr/LAr Timing Results	Takai
0:10	FEP-based Level 1 Trigger Status	Crosetto
	(Coffee Break)	
Joint Session with Muon Group (proposed)		
.0:30-12:00		
	Comments on Muon Triggering	Shaevitz
	Electronics Costs	tbd
	Discussion	
12:00	Lunch	
Calorimeter Readout II		
1:00	Status of ADC Readout Work at Nevis	Sippach
1:45	Cal FPGA Status	Gara
	Readout Requirements for HCAL	tbd
Muon Electronics (Electronics Group only)		
2:00	Muon Front-End work at BNL	O'Connor
2:15	CSC Readout Requirements & Options	Wixted
System Integration		
2:30	Early results on transformers in magnetic fields	Freeman
2:45	Grounding and Shielding in GEM	Lau*
DAQ		
3:00	Virtual Level 2 Trigger/DAQ Scheme	Dorenbosch
3:30	Discussion	
Plan for TDR		
3:45	Work Assignments & Schedule for Drafts	Marlow/Shaevitz
Plan for Cost & Schedule Work (Optional for some)		
4:15	Overall Plan for GEM	Fischer et al.
4:30	Electronics Cost Estimating Plan & Work Assignments	Marlow
5:00	Adjourn (the meeting may run somewhat later than this, but it will definitely finish by 6:00 PM)	

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Presentation by:

S. Hahn

11-4-92
S. Hahn

Si-Tracker Electronics

MCM

GE/TI - High Density Interconnect
Sample layout started

CMOS

UTMC, Harris: device library installed
Architecture being settled
Subcircuits being simulated
LANL/SNLA/LSI Logic CRADA being initiated on

Bipolar

Presentation at Yellowstone
Poster session at IEEE-NSS '92
AT&T contract to be signed (tile-array)
12 cm vs. 18 cm

12 cm vs. 18 cm

Cost

Less number of channels

Noise

Capacitance

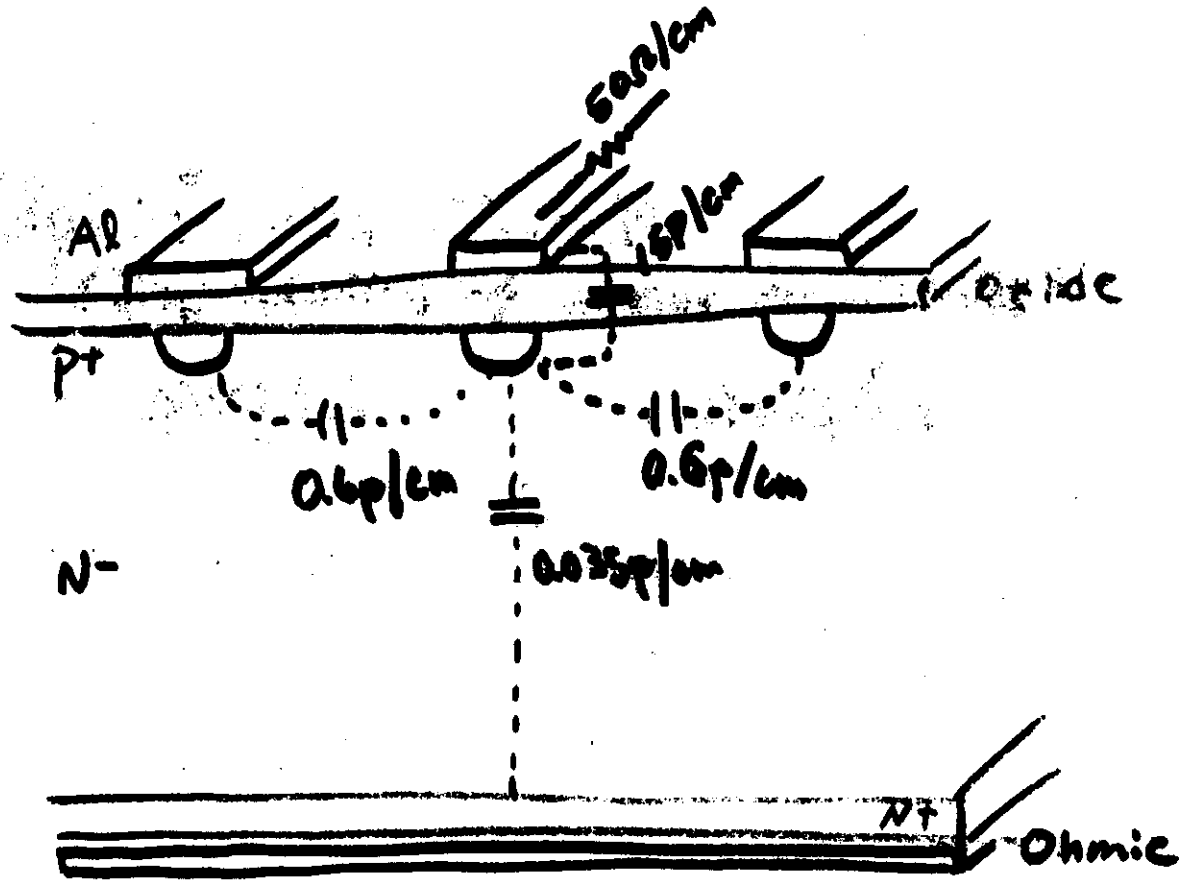
Metal strip resistance
(transmission-line effect)

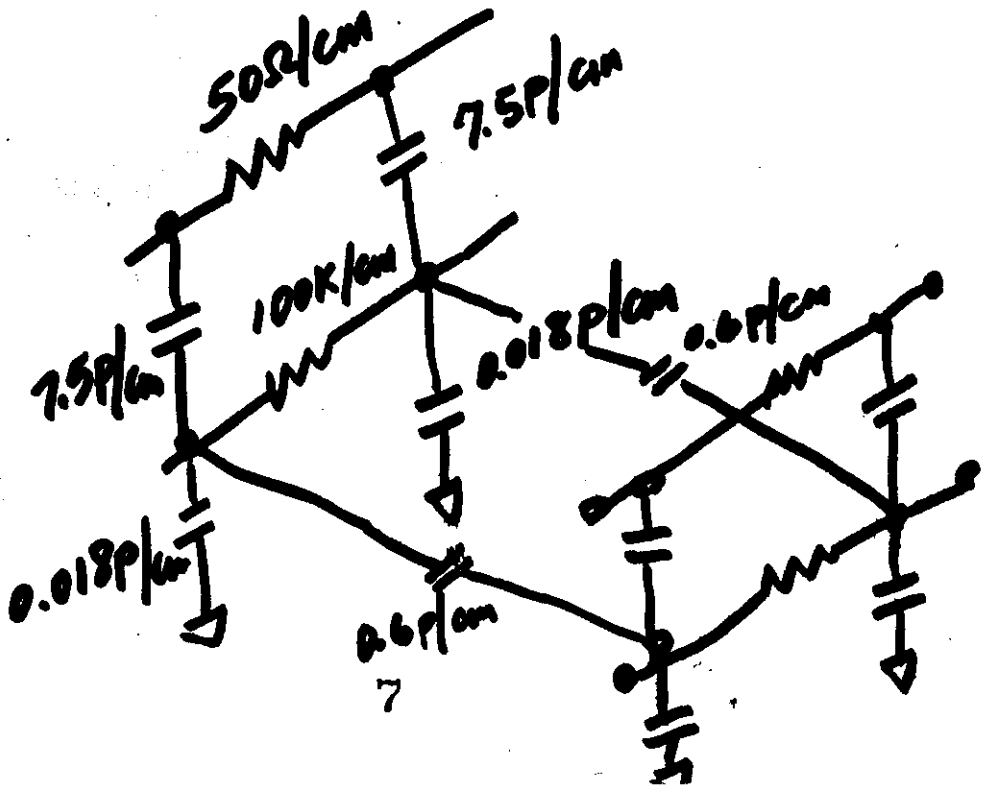
Charge-coupling

Realistic charge waveform

Time-walk

Pseudo Zero-crossing detection


50Ω/cm
Al
16P/cm
Oxide
P+
0.6p/cm
0.6p/cm
N-
0.035p/cm
N+
Ohmic


50Ω/cm
7.5P/cm
100K/cm
7.5P/cm
0.018P/cm
0.6P/cm
0.018P/cm
0.6P/cm

"Equiv." Noise Charege (e^- RMS)*
(Degradation of signal amplitude)

	50Ω/cm	20Ω/cm
12cm	2184	1864
18cm	3378	2761

* Far-end injection

✓ $0.8\mu^T \times 10\mu^W \rightarrow 80\Omega/cm$

Custom Bipolar Integrated Circuit Designs for the Front-End Electronics of the Silicon Tracker Subsystem for SSC-GEM Detector

Sangkoo F. Hahn and Maureen M. Cafferty
Los Alamos National Laboratory, Los Alamos, NM 87545

Abstract

Extremely high radiation background (up to 5 MRad over a 10 year lifetime), a large number of channels (3.2 M), high speed, low noise requirements (1250 electrons RMS), and low power consumption (1 mW/channel), present a formidable challenge for front-end electronics of the Silicon Tracker subsystem for the SSC-GEM (Gamma, Electron, Muon) Detector. Simulation results from the bipolar designs for an analog integrated circuit to process charge inputs from silicon strip detectors are presented using AT&T and Harris transistor models.

I. Introduction

The decision was made earlier that a bipolar IC technology was to be used for the processing of the charge signals from the Si-strip detectors to meet the noise, speed and power requirements. The main function of the bipolar IC is to make an unambiguous logic decision of either hit or no-hit per every beam-crossing (with a period of 16 ns) for every channel based on the amount of charge collected from the strip detectors. Due to the low occupancy of less than 1%, the dead-time of the circuit operation between events can be as much as 150 ns. The design features and the major simulation results are described.

II. Design Features

The preamp uses the familiar cascode configuration with an input transistor geometry of three times the area of the minimum geometry transistors to reduce the noise from the base spread resistance. The feedback resistor and capacitor set the shaping time of 30 ns. The feedback resistor is made as large as possible for minimum noise contribution while remaining small enough to maintain reasonably constant bias conditions, which are sensitive to transistor gain changes, over the lifetime of the system.

The intermediate amplifier is a minimum component stage which is very sensitive to the bias level at the base of Q22. The resistors, R5 and R6 are adjusted for maximum possible gain without pushing Q22 into saturation. This maximizes the signal to noise ratio from this stage (Figure 1).

The shaper/baseline restorer stage has a closed loop gain of about eight, for the signal, with a signal swing of about 40 mV for a 6000 electron input charge. The baseline restoration circuit causes some noise degradation but has a crucial role of stabilizing the DC bias level of the input node to the comparator. Without the restoration, the drift of the DC level would present a serious control problem to the circuit operation (Figure 2). The comparator design is straightforward with a differential-pair input stage followed by current-mirror amplifiers for current output (Figure 3).

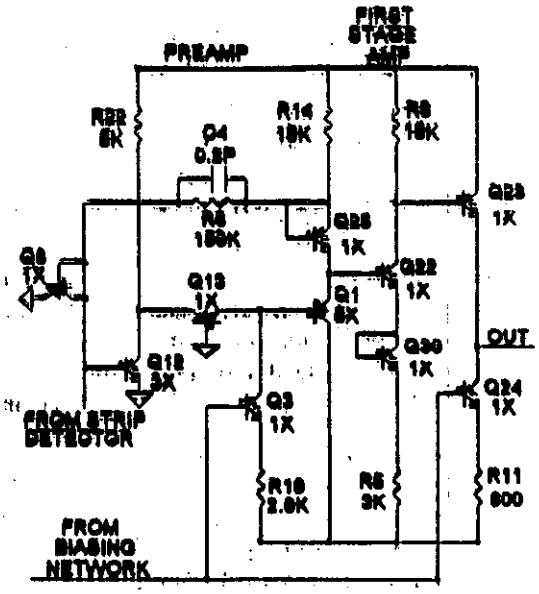


Fig. 1 Preamp & Intermediate-stage amplifier

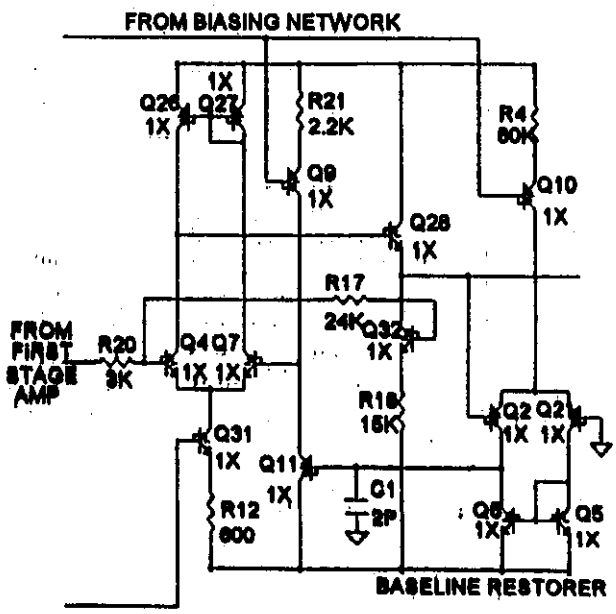


Fig. 2 Shaper\Amplifier

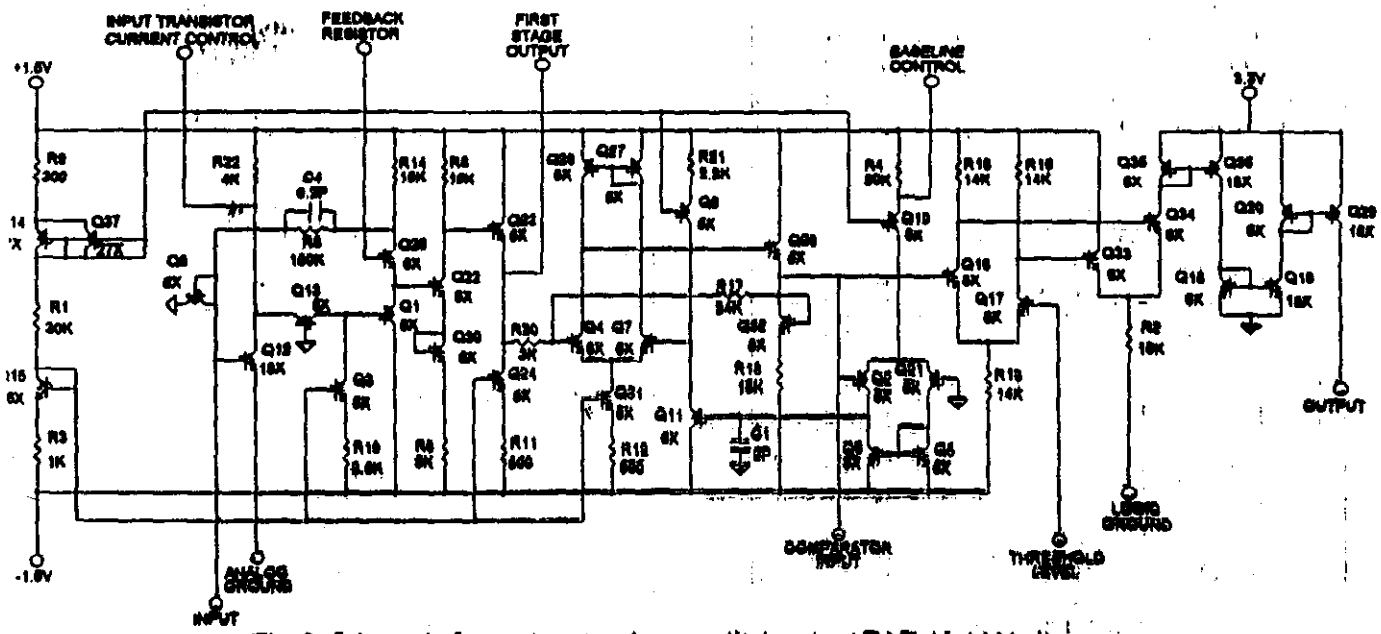


Fig. 3 Schematic for semi-custom layout utilizing the AT&T ALA110 tile array

III. Simulation Results

A. AT&T Tile Array ALA110

Simulations were performed using models from the AT&T CBIC-V process. A design based on the ALA110 tile array models will be submitted to AT&T for semi-custom fabrication, and the chip will be tested when available. The schematic and the pinouts are shown in Figure 3. The tile array is for small-scale applications and contains minimum area geometry transistors of 32.5 x 47.5 μm which are too large for the final design. The final design will be based on smaller geometry transistors.

Simulation results using MicroSim's PSPICE were obtained for charge inputs from 6000 electrons to 48000 electrons. The current source simulating the waveform out of a 300 μm thick PIN diode [1] is shown in Figure 4.

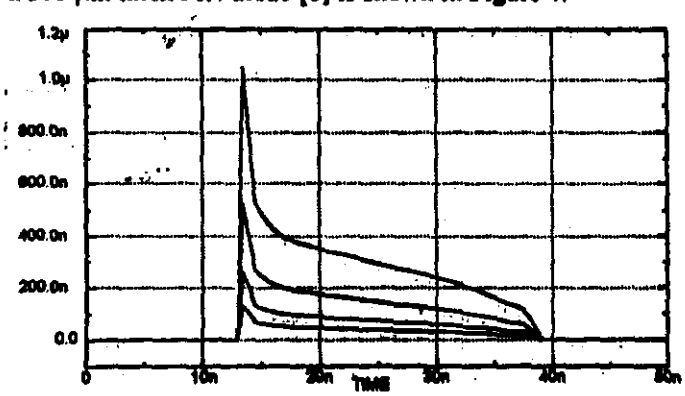


Figure 4

Simulations were run for strip lengths of 6 cm, 12 cm, and 18 cm with nominal transistor current gains for beginning of life and low current gains for assumed end of life performances. The strip detector was simulated using lumped elements with three strips and three amplifiers in parallel as shown in Figure 5 [2] to reflect coupling effects between adjacent channels.

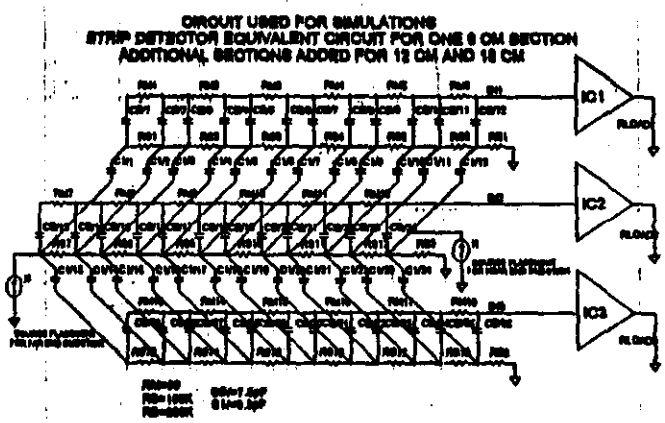


Figure 5

Simulation results between using AT&T subcircuit models for the resistors and capacitors and using ideal resistors and capacitors were virtually identical, but the noise performance was about 8% worse for the subcircuit resistors and capacitors. The simulation times for three amplifiers utilizing all subcircuit models were much longer than practical, therefore, ideal resistors and capacitors were used in all subsequent results.

Typical signals at the input of the comparator for 12 cm strip length, near end injection are shown in Figure 6 while the comparator outputs are shown in Figure 7. Note that the time-walk is measured at the falling edge of the comparator output waveform to take advantage of the pseudo zero-crossing time pick-off effect.

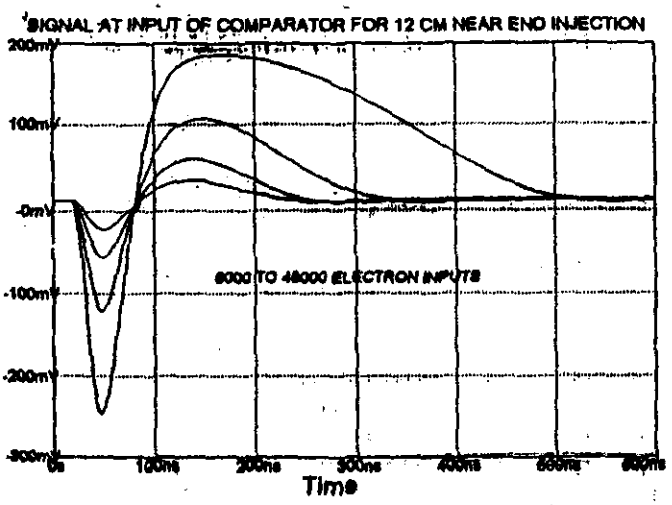


Figure 6

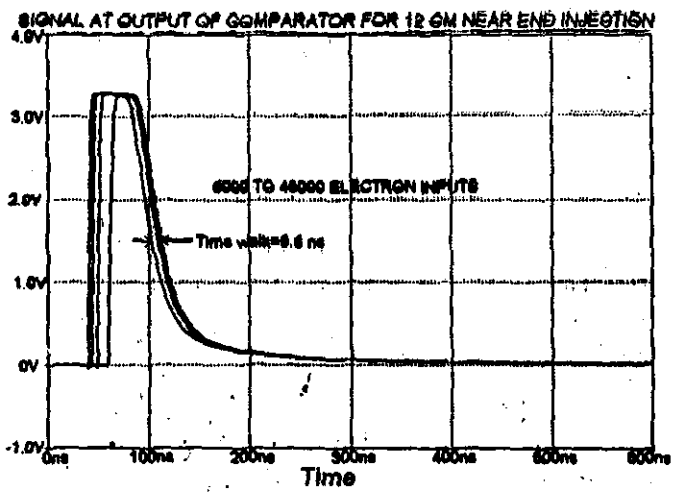


Figure 7

The simulation results are summed up in Table 1 for beginning of lifetime and end of lifetime. Small signal amplitude, time walk, and noise results are shown for 6 cm, 12 cm, and 18 cm detector strip lengths. The amplitude was measured for the 6000 electron input. Time walk was measured for 6000 to 48000 electron inputs with a comparator threshold level set to 60% of the small signal swing for each detector strip length. The noise was calculated at the input to the comparator.

B. Harris UHF

Simulations were also performed using models for Harris UHF small geometry transistors for 12 cm and 18 cm detector strip lengths.

The noise for the 12 cm far-end was 2540 electrons and 2210 electrons for the near-end. The time walk was 13.7 ns for the far-end and 10.2 ns for the near-end with the threshold level equal to 5000 electrons (no 6000 electron trigger).

The noise for the 18 cm far-end was 3550 electrons and 2710 electrons for the near-end. The time walk was 9.1 ns for the far-end (no 6000 or 12000 electron trigger) and 9.0 ns (no 6000 electron trigger) with the threshold level equal to 6250 electrons.

BEGINNING OF LIFETIME

(transistor current gain approx. 110, baseline=13.7 mV)

	FAR END INJECTION				
	AMPLITUDE (mV)	TIME WALK (ns)	THRESHOLD LEVEL (mV)	INTEGRATED NOISE (mV)	NOISE (electrons RMS)
6 CM	[illegible]	7.3	-6.4	7.8	1216
12 CM	31.6	12.5	-8.9	11.8	2184
18 CM	25.4	21.0	-6.6	14.8	3378
	NEAR END INJECTION				
	AMPLITUDE (mV)	TIME WALK (ns)	THRESHOLD LEVEL (mV)	INTEGRATED NOISE (mV)	NOISE (electrons RMS)
6 CM	[illegible]	[illegible]	-6.4	7.8	1212
12 CM	34.3	[illegible]	-8.9	11.8	2012
18 CM	31.6	11.8	-6.6	14.8	[illegible]

END OF LIFETIME

(transistor current gain approx. 45, baseline=23.8 mV)

	FAR END INJECTION				
	AMPLITUDE (mV)	TIME WALK (ns)	THRESHOLD LEVEL (mV)	INTEGRATED NOISE (mV)	NOISE (electrons RMS)
6 CM	[illegible]	7.3	11.8	6.4	1357
12 CM	22.4	11.3	14.2	8.3	2223
18 CM	18.2	19.5	15.4	9.8	3231
	NEAR END INJECTION				
	AMPLITUDE (mV)	TIME WALK (ns)	THRESHOLD LEVEL (mV)	INTEGRATED NOISE (mV)	NOISE (electrons RMS)
6 CM	26.4	7.1	11.6	6.4	1352
12 CM	24.1	9.8	14.2	8.3	2086
18 CM	22.0	11.4	15.4	9.8	2873

Table 1

IV. CONCLUSION

A preliminary design for the front-end electronics for the Silicon Tracker subsystem for the SSC-GEM (Gamma, Electron, Muon) Detector has been simulated and will be submitted to AT&T for semi-custom fabrication.

The results show excellent beginning-of-life performance and acceptable end-of life performance (10 year lifetime, 5 MRad total dose) for required time walk (<16 ns), with the given power (1 mW) for a 12 cm detector strip length, but clearly degraded performance at 18 cm lengths.

V. REFERENCES

[1] W.C. Sailor, H.-J. Ziock, W.W. Kinnison, K. Holzcheiter, "A Model for the Performance of Silicon Microstrip Detectors", *Nuclear Instruments and Methods in Physics Research*, A303 (1991) pp. 285-297

[2] Issy Kipnis "Analog Front-End Electronics for the SDC Silicon Tracker", Workshop on Front-End Electronics for Silicon Detectors at Future High Luminosity Colliders, Yellowstone National Park, Wyoming, 17 September 1992

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Presentation by:

Jim Musser

Jim Musser

IPC Status

amp: Design review @ Harris Mid Dec. Report by Paul.

SCA: Design review Nov 20/Dec 2 Droop problem resolved.

FADC: HA-900P samples obtained by U.M. will characterize over dose.

[redacted]

READ - WRITE ADDRESS GENERATOR

- FF register based status array

  Indicates write protection of an address for readout

  Two status bits read out per event clock

  Status bits control skip logic to pass over protected write locations

- Parallel adders

  Generate skip addresses

  Status bits select proper adder output for next address

  Write address latched for external analog memory and internally for reading out next status bits

  Read address is delayed by the trigger calculation time and is latched upon receipt of a trigger signal

  Read addresses are pushed into FIFOs for eventual readout

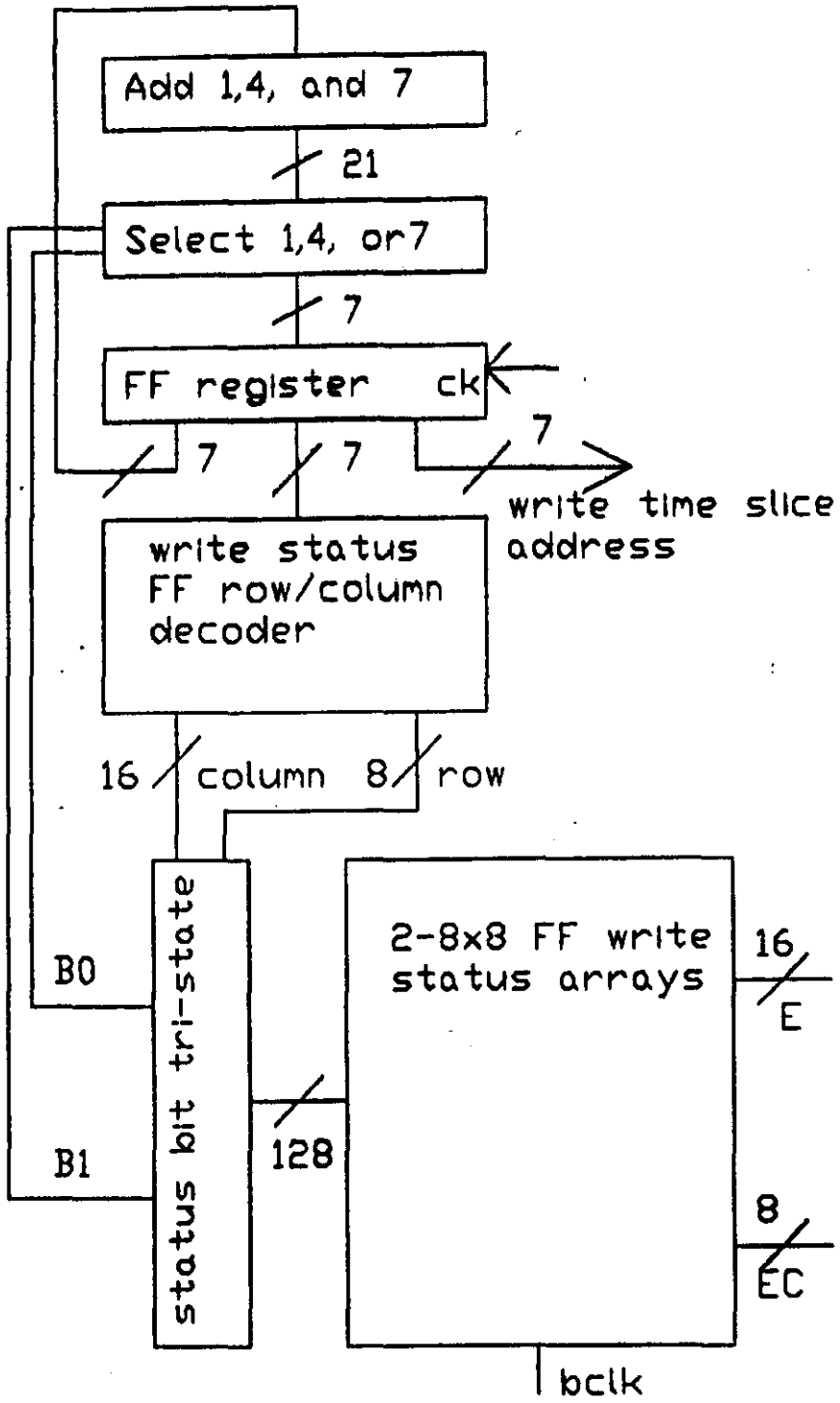
- Status of Read - Write generator

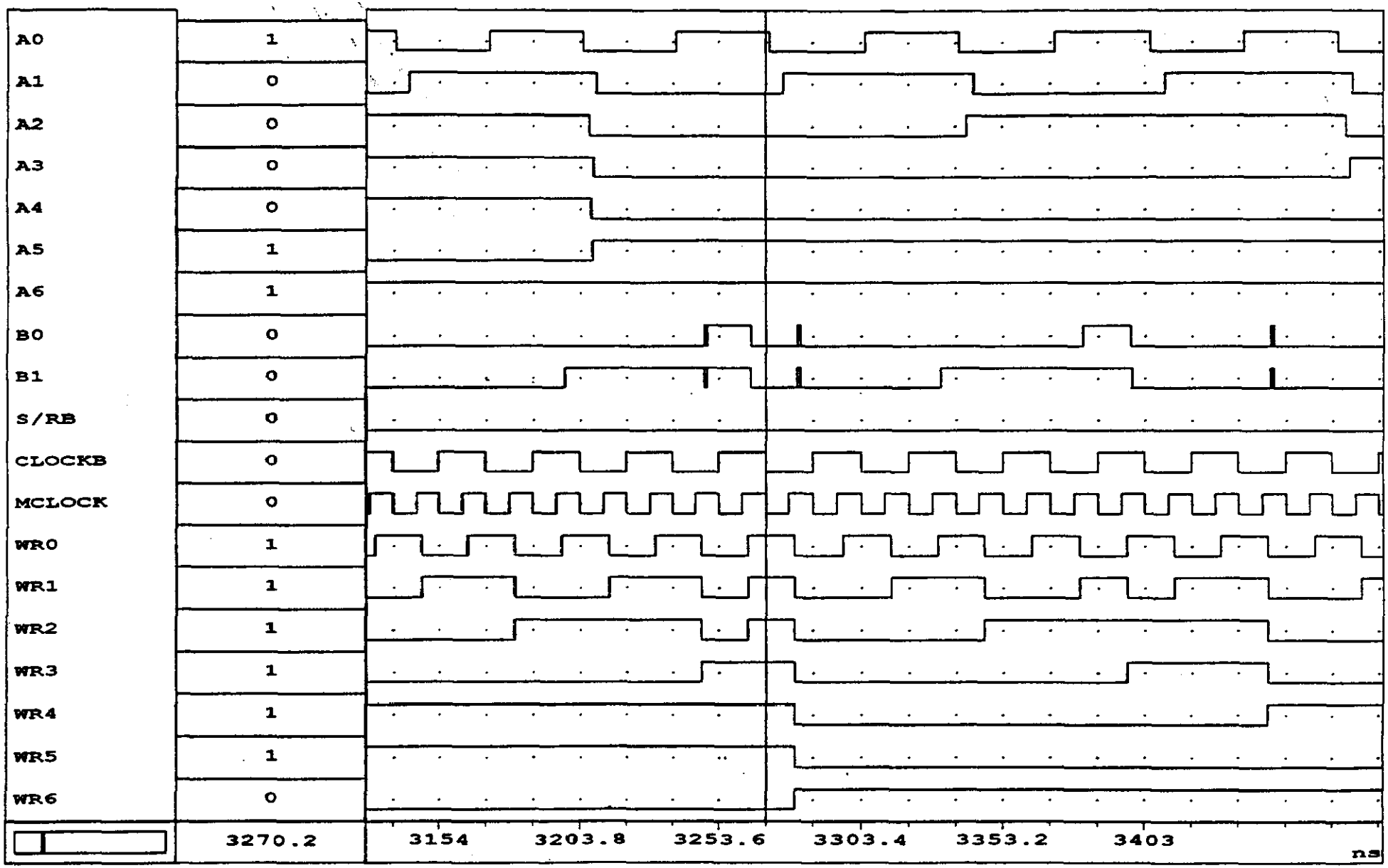
  Schematic capture completed

  Functional unit delay timing completed and passed

  Optimized routing in Xilinx IC in progress to meet system level speed

  Scheduled for completion by November 92


Add 1,4, and 7
21
Select 1,4, or7
7
FF register
ck
7
7
7
write time slice address
write status FF row/column decoder
16
column
8
row
B0
B1
status bit tri-state
128
2-8x8 FF write status arrays
16
E
8
EC
bclk


A0 1
A1 0
A2 0
A3 0
A4 0
A5 1
A6 1
B0 0
B1 0
S/RB 0
CLOCKB 0
MCLOCK 0
WR0 1
WR1 1
WR2 1
WR3 1
WR4 1
WR5 1
WR6 0
3270.2
3154
3203.8
3253.6
3303.4
3353.2
3403
ns

READOUT CONTROLLER IC

- Three functional blocks

  Read - Write address generators

  Timing and control

  Data readout

- Prototype technology

  Xilinx field programmable gate array - Static Ram based structure

  Three chip solution - Two Xilinx 3195-3 ICs & One SRAM

  Xilinx 3195 : 50 - 80 Mhz system level speed

  Greater than 9,000 nominal gates per 3195 IC

- End product technology

  LSI Logic LRH20K radiation hardened series gate array

  Guaranteed total dose specification 3E6 rad (si)

  Silicon - gate 1.0 micron (0.7 micron effective) 2 - layer metal HCMOS

Timing & Control/Data Readout

- Timing & Control

  Flip - Flop synchronous state machine

  Synchronous with the event clock

  Generates all sub-clocks and control signals

- Data readout

  FIFO data buffered from the output of eight Flash A-D converters

  SRAM stored thresholds are magnitude compared with FIFO buffered data for zero suppression

  Non-suppressed data are pushed into a FIFO for data frame packing

  Non-suppressed data, read address, bunch crossing ID, and frame sync word are packed into serial data frames

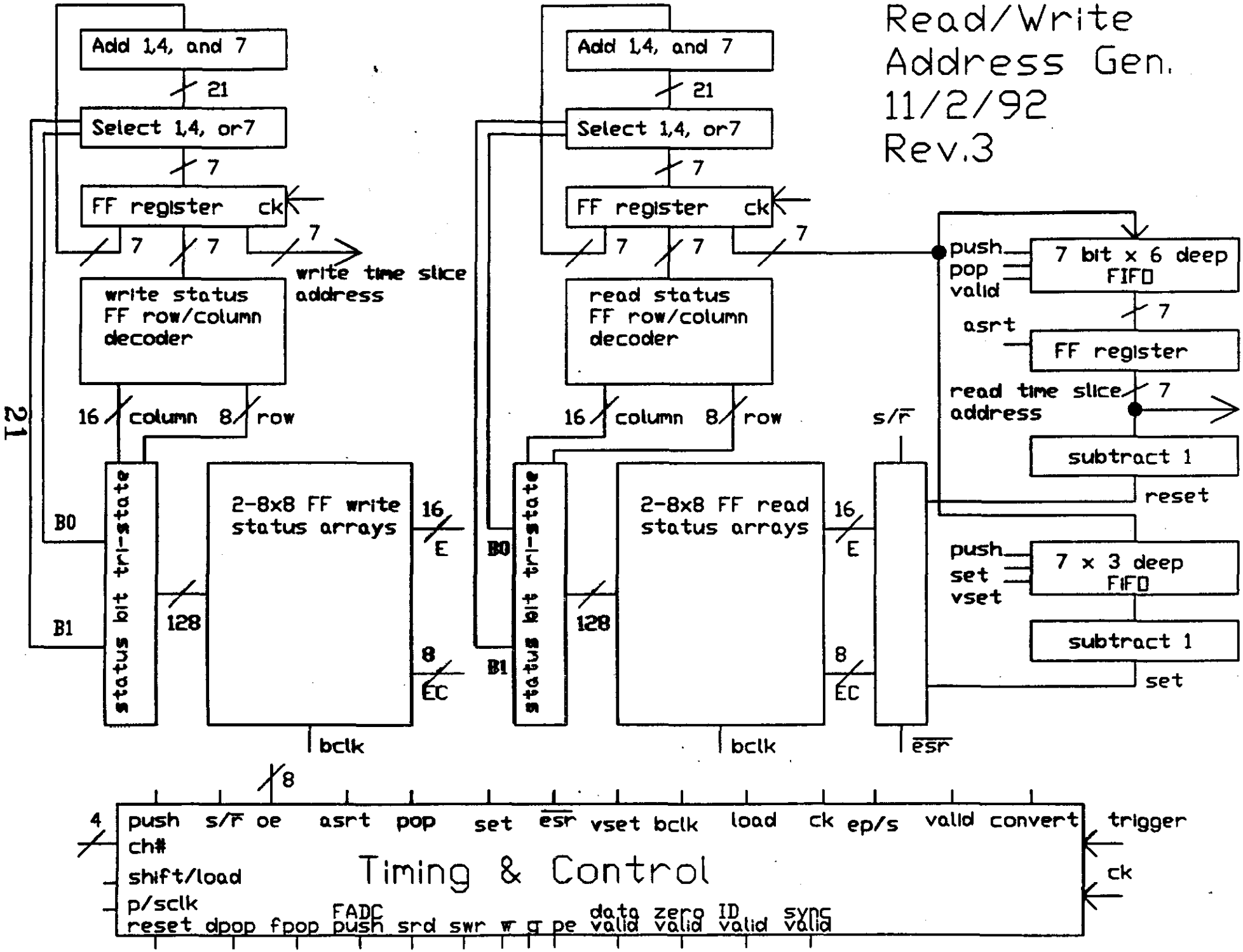
  Data transmission is synchronous, frame synched communication over fiber optic link

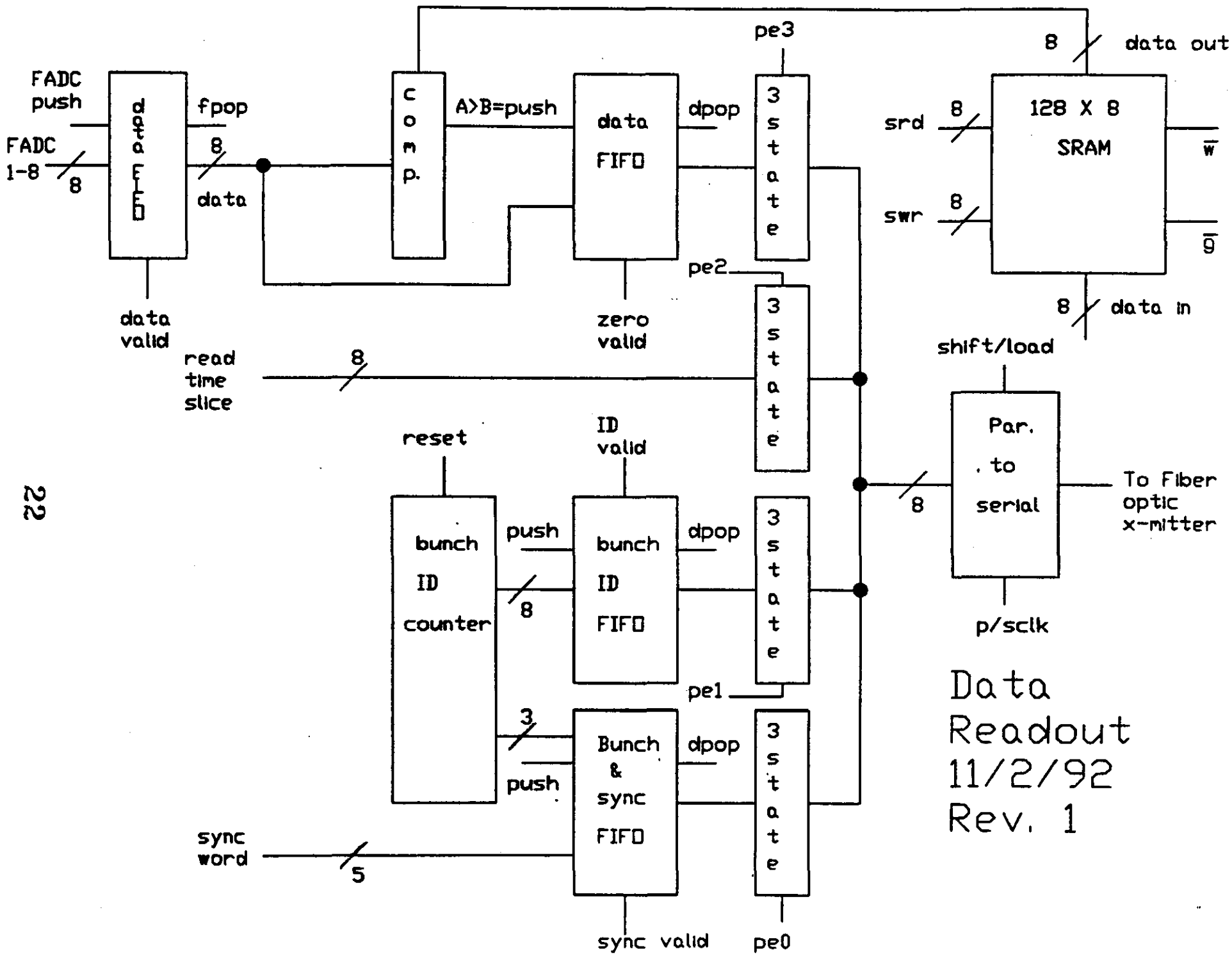
- Status of Timing & Control/Data readout

  Block diagram completed

  Schematic capture in progress

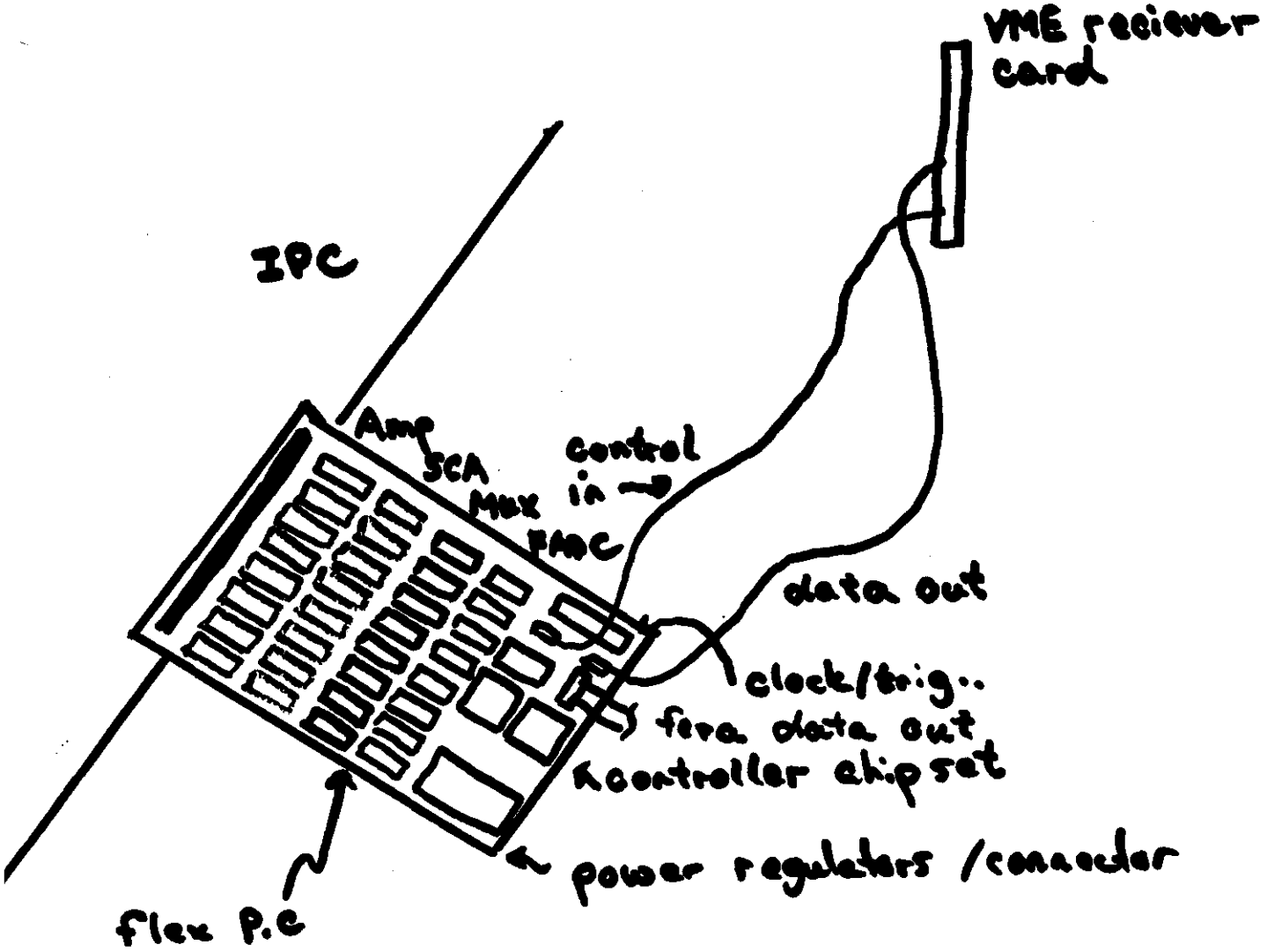
  Scheduled for completion by February 93


Read/Write
Address Gen.
11/2/92
Rev.3
Add 1,4, and 7
21
Select 1,4, or7
7
FF register ck
7
7
7
write time slice address
write status FF row/column decoder
16 column
8 row
B0
B1
status bit tri-state
128
2-8x8 FF write status arrays
16 E
8 EC
bclk
Add 1,4, and 7
21
Select 1,4, or7
7
FF register ck
7
7
7
read status FF row/column decoder
16 column
8 row
B0
B1
status bit tri-state
128
2-8x8 FF read status arrays
16 E
8 EC
bclk
s/r̄
esr̄
push
pop
valid
7 bit x 6 deep FIFO
7
asrt
FF register
read time slice address
7
subtract 1
reset
push
set
vset
7 x 3 deep FIFO
subtract 1
set
8
4
push s/r̄ oe asrt pop set esr̄ vset bclk load ck ep/s valid convert
trigger
ck
ch#
shift/load
p/sclk
reset dpop fpop FADC push srd swr w̄ g̅ pe data valid zero valid ID valid sync valid
Timing & Control


FADC push
FADC 1-8
8
data FIFO
fpop
8
data
data valid
comp.
A>B=push
data FIFO
dpop
zero valid
pe3
3 state
pe2
3 state
pe1
3 state
pe0
3 state
8
data out
srd
8
swr
8
128 X 8 SRAM
$\overline{w}$
$\overline{g}$
8
data in
read time slice
8
reset
bunch ID counter
push
8
3
push
ID valid
bunch ID FIFO
dpop
Bunch & sync FIFO
dpop
sync word
5
sync valid
shift/load
Par. to serial
8
p/sclk
To Fiber optic x-mitter
Data Readout 11/2/92 Rev. 1

Prototype R/O system

Goal: ready for beam tests in late 93



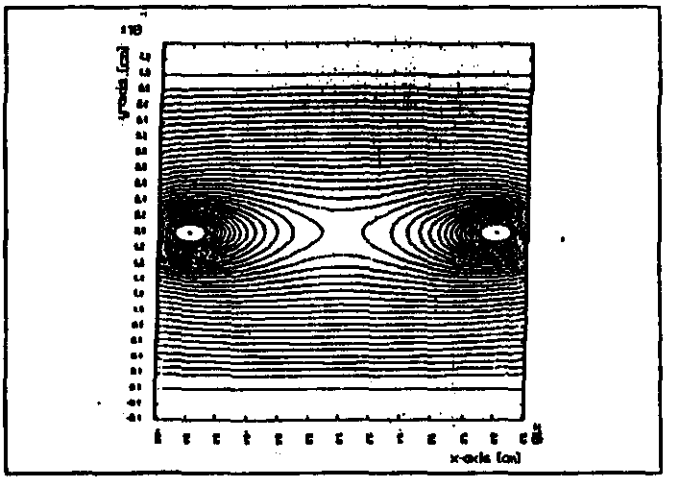
64 ch. card

IPC Front End Simulation

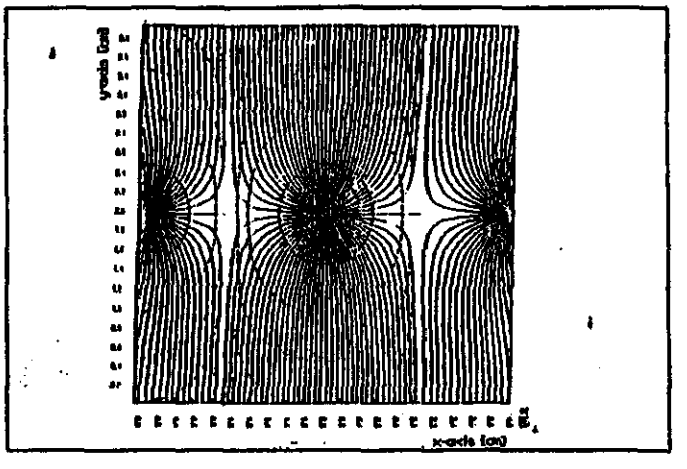
- Use GARFIELD to simulate IPC

  4 mm chamber thickness
  2 mm wire spacing
  20 micron wire diameter
  50-50 CF_4 CO_2
  2700 V operating voltage

E Field vs Position



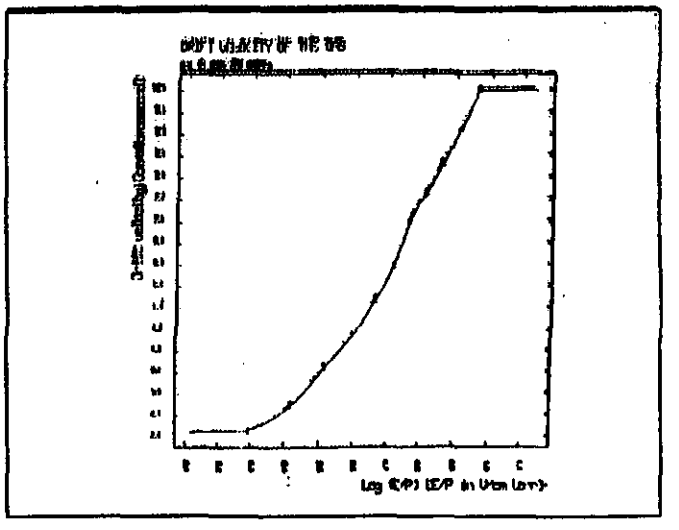
Drift Time Contours



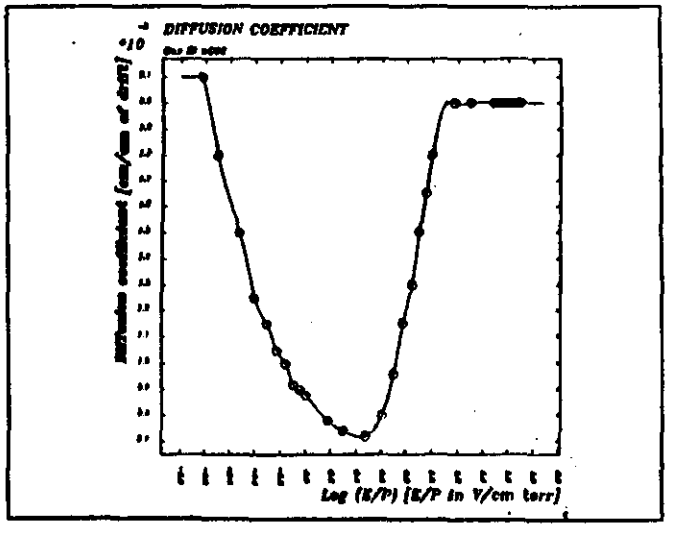
IPC Front End Simulation

- Drift Velocity vs E-Field based on IU measurements
- Diffusion - based on pure CO_2 , CF_4

Drift Velocity vs E

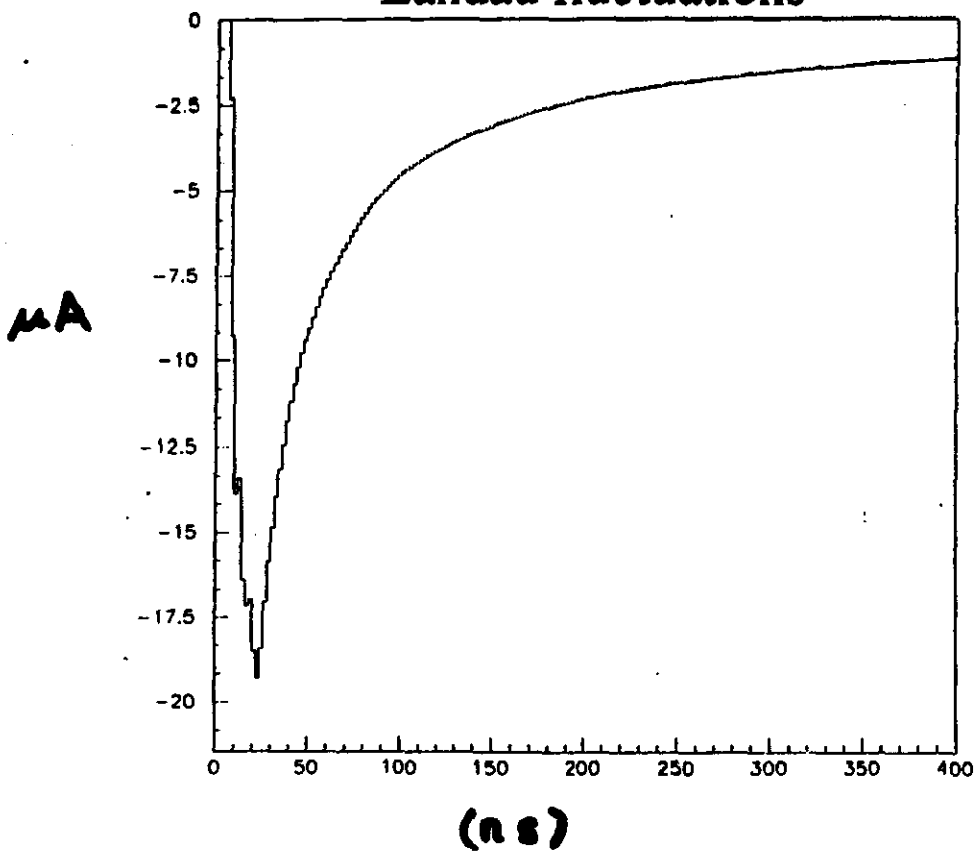


Diffusion vs E



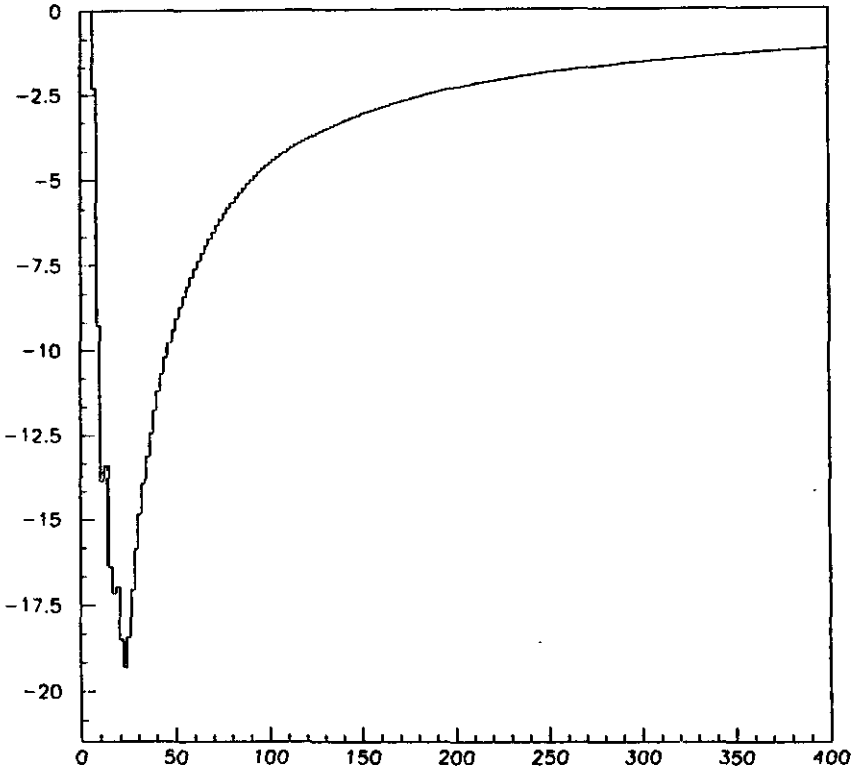
IPC Front End Simulation

- Simulate signals in IPC
  includes random trajectories
  diffusion
  Landau fluctuations



IPC Front End Simulation

- Simulate signals in IPC
  includes random trajectories
  diffusion
  Landau fluctuations



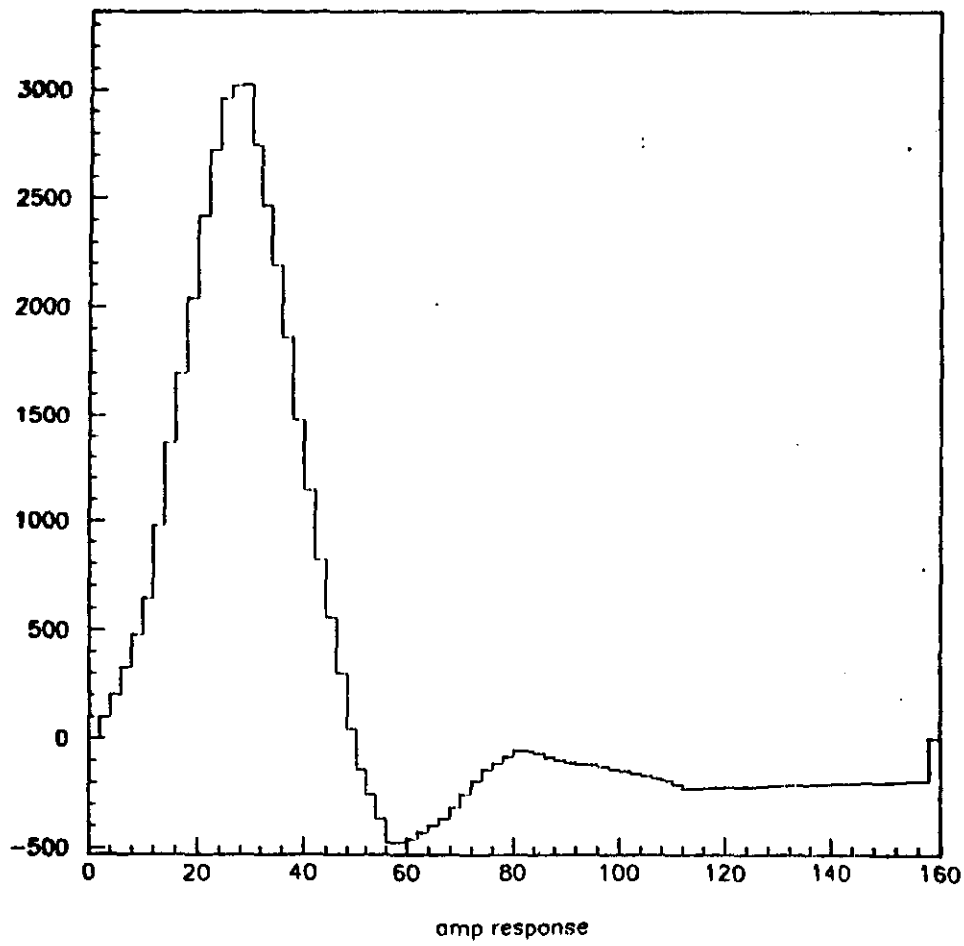
IPC Front End Simulation

- Apply transfer function from preamp/shaper

  Based on measured response of prototype amps. Pole Zero has been added to eliminate ion tail.

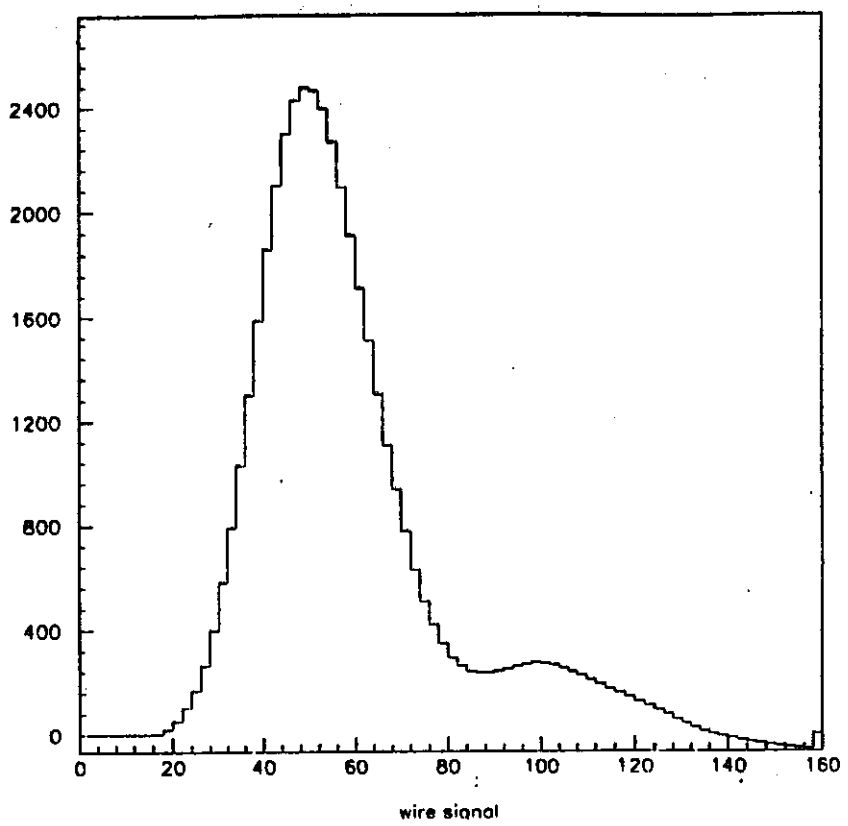
Amp. Impulse
Response Function

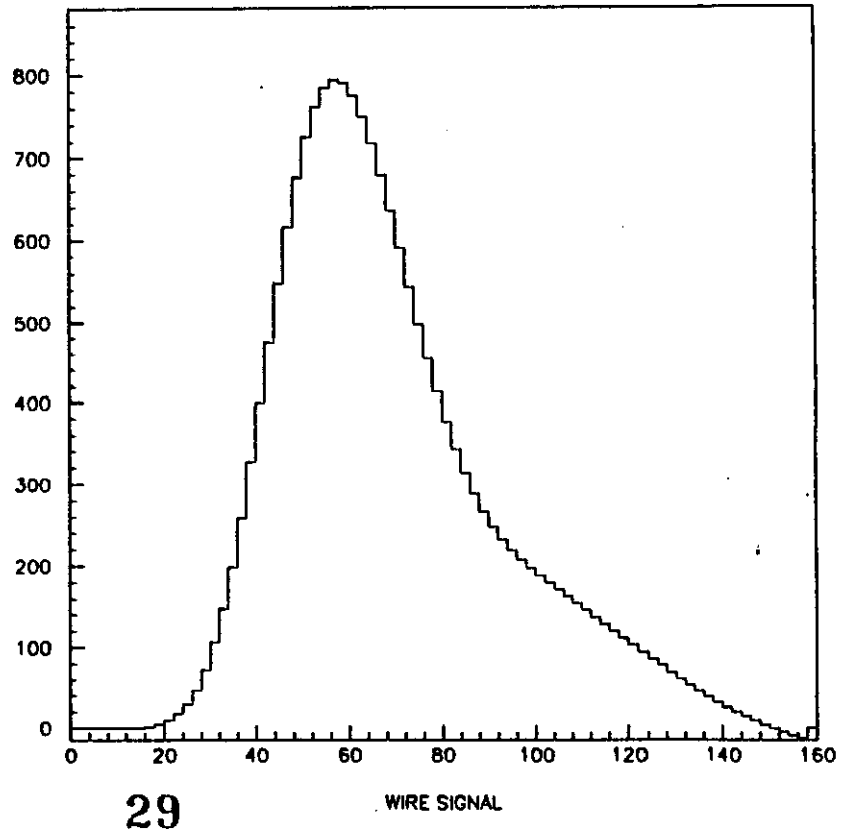
1 pC input



IPC Front End Simulation

Output pulses

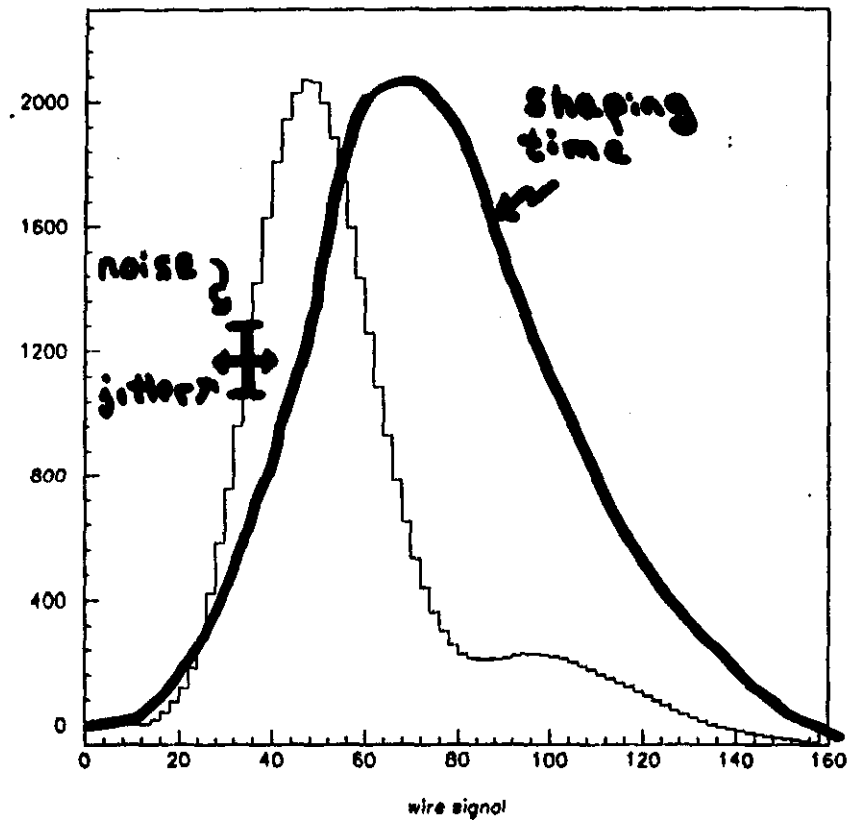




IPC Front End Simulation

- Choose position on pad at random
- Use position to make three pad signals according to known induced signal distribution.
- Sample three pad signals at 60 Mhz.
- apply 3 types of 'smearing' to samples

noise - added to sample using normal distribution
time jitter on sampling points
shaping time errors

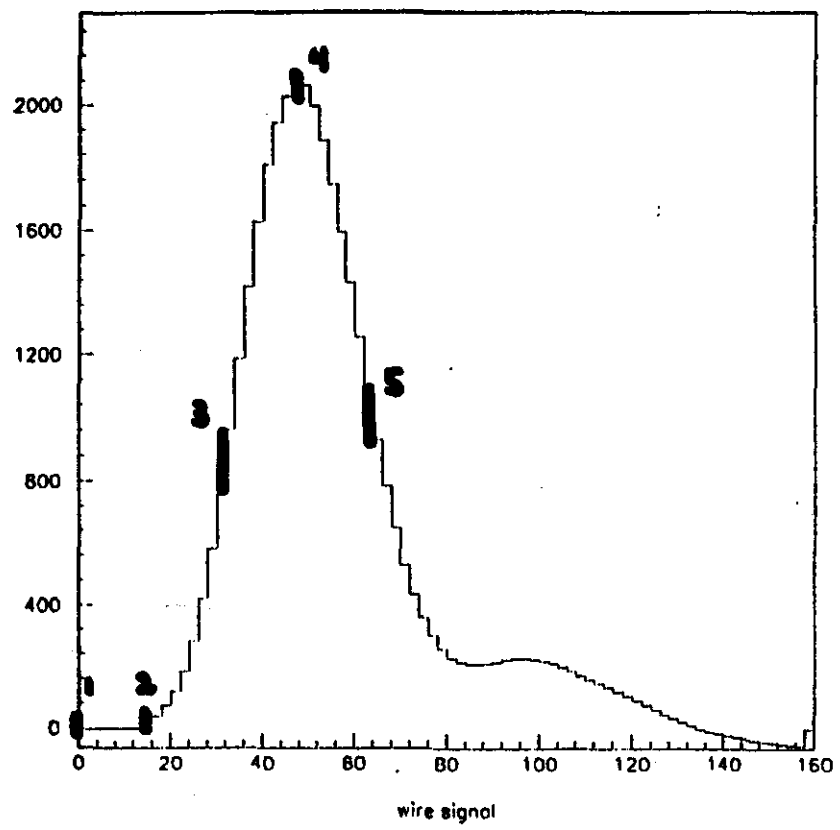


IPC Front End Simulation

- Electronics Noise

Look at three samples - (3rd, 4th, and 5th)

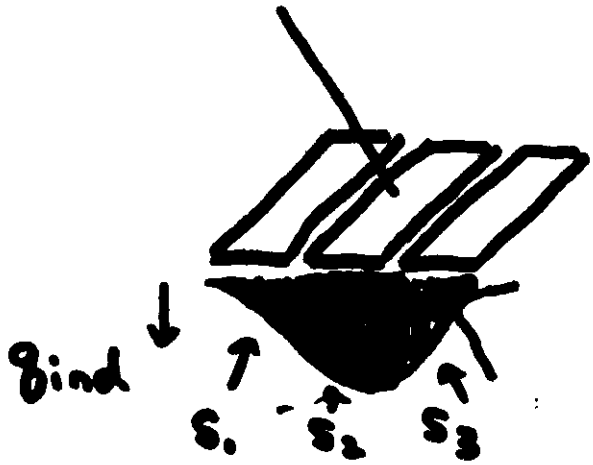
Approx Sample Loc.



Position Determination

2 methods:
- fit to known induced signal dist.
- weighted mean

fit



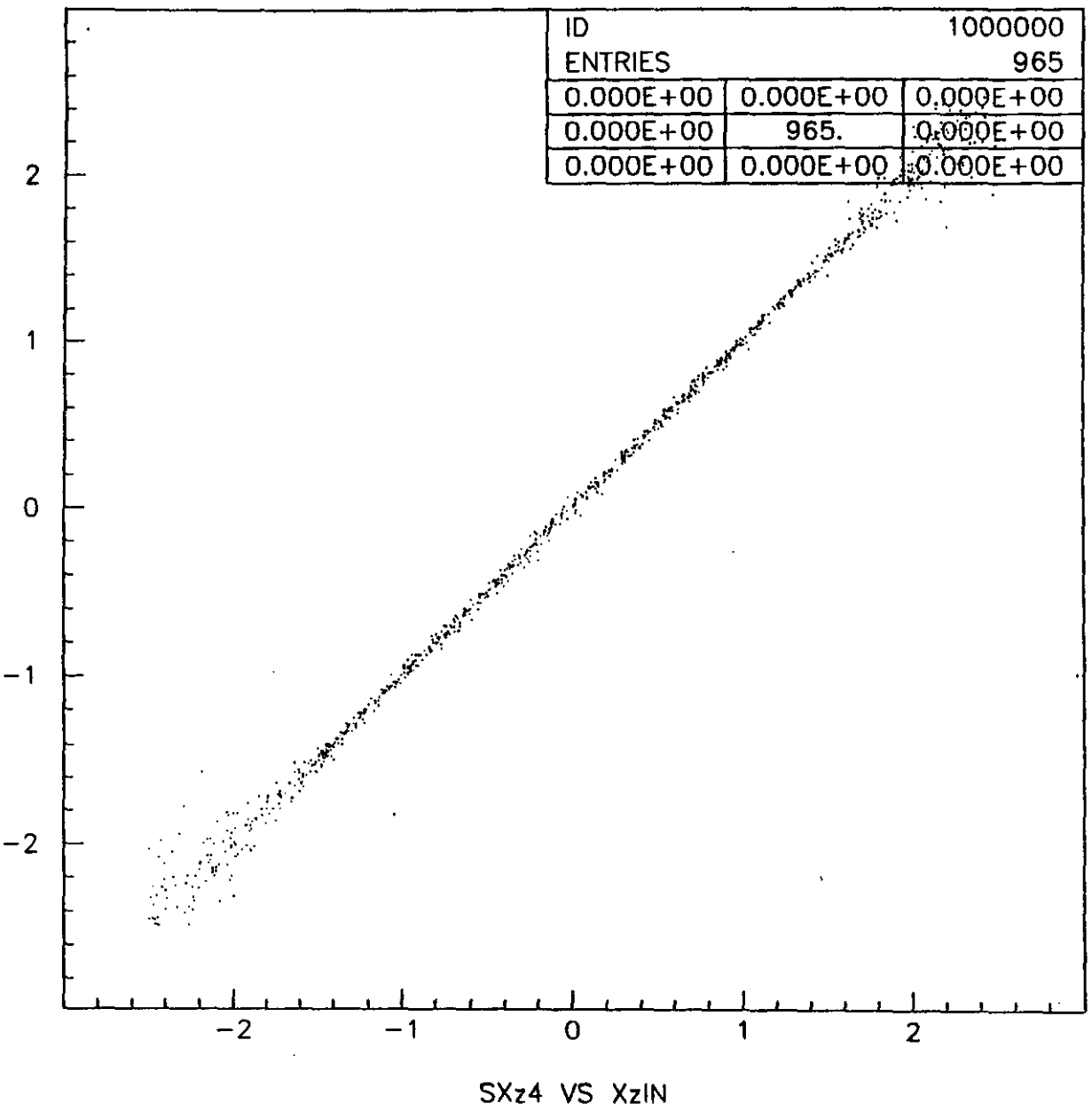
fit measured S_1, S_2, S_3 to known induced charge dist. to get X.

mean

$$X = \frac{-2.5\,mm \cdot S_1 + 2.5\,mm \cdot S_3}{S_1 + S_2 + S_3}$$

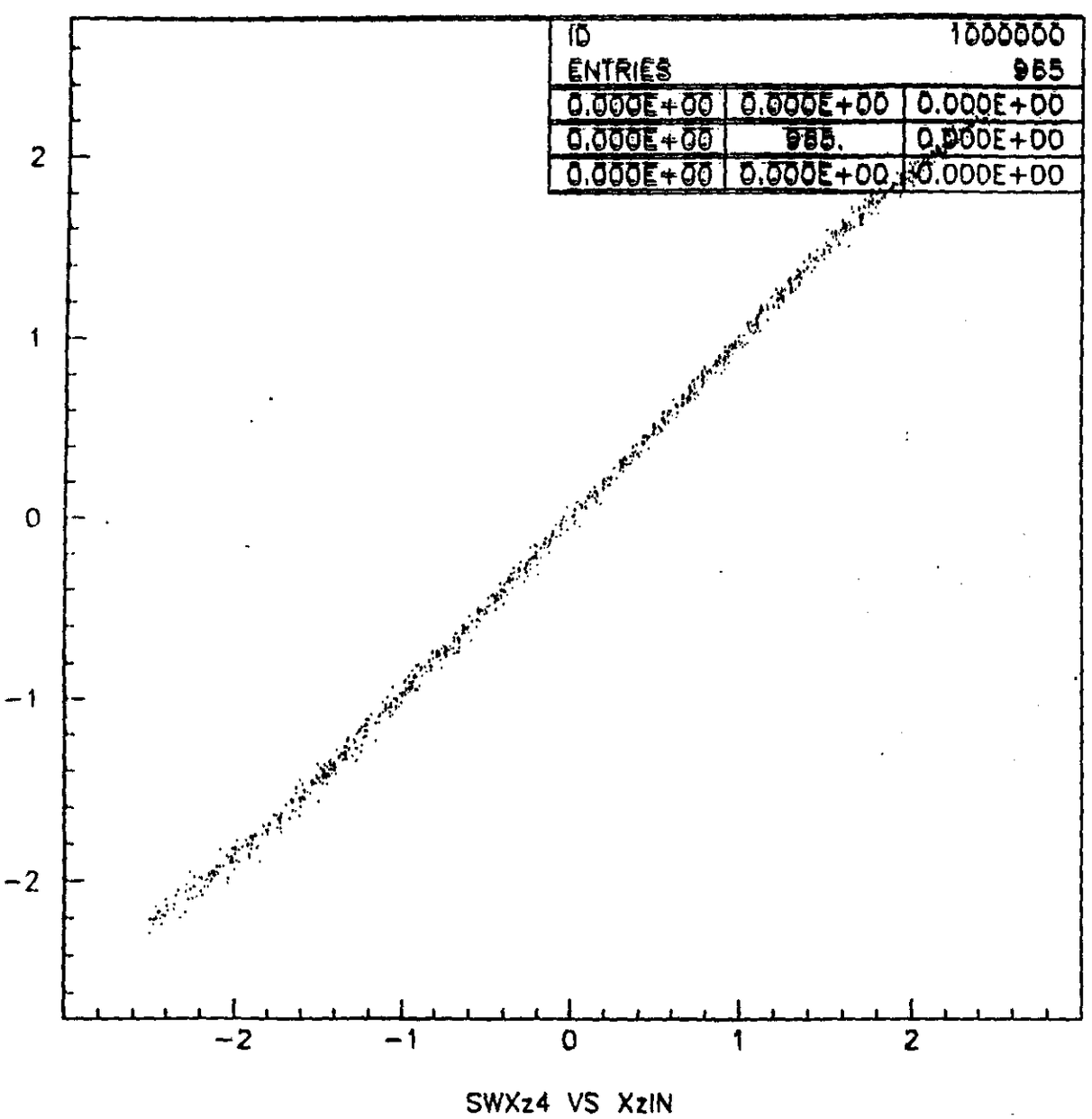
IPC Front End Simulation

4 th sample
x (fit) vs x(actual)



IPC Front End Simulation

4 th sample
x(mean) vs x(actual)

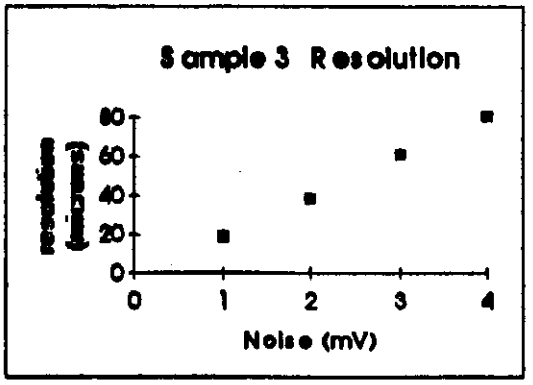


IPC Front End Simulation

- resolution vs noise level

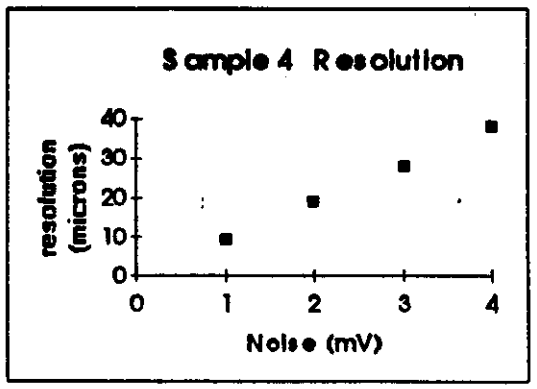
3 rd sample

$\langle S_1 + S_2 + S_3 \rangle = 180\,mV$



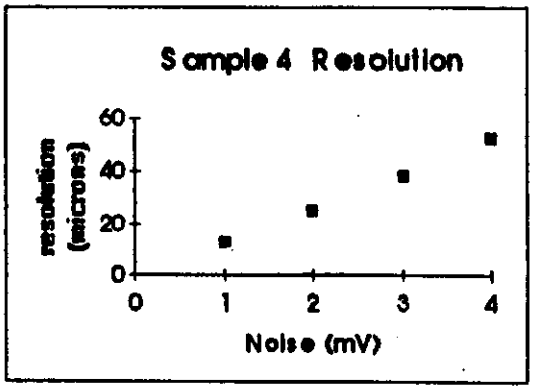
4 th sample

$\langle S_1 + S_2 + S_3 \rangle = 400\,mV$



5 th sample

$\langle S_1 + S_2 + S_3 \rangle = 300\,mV$

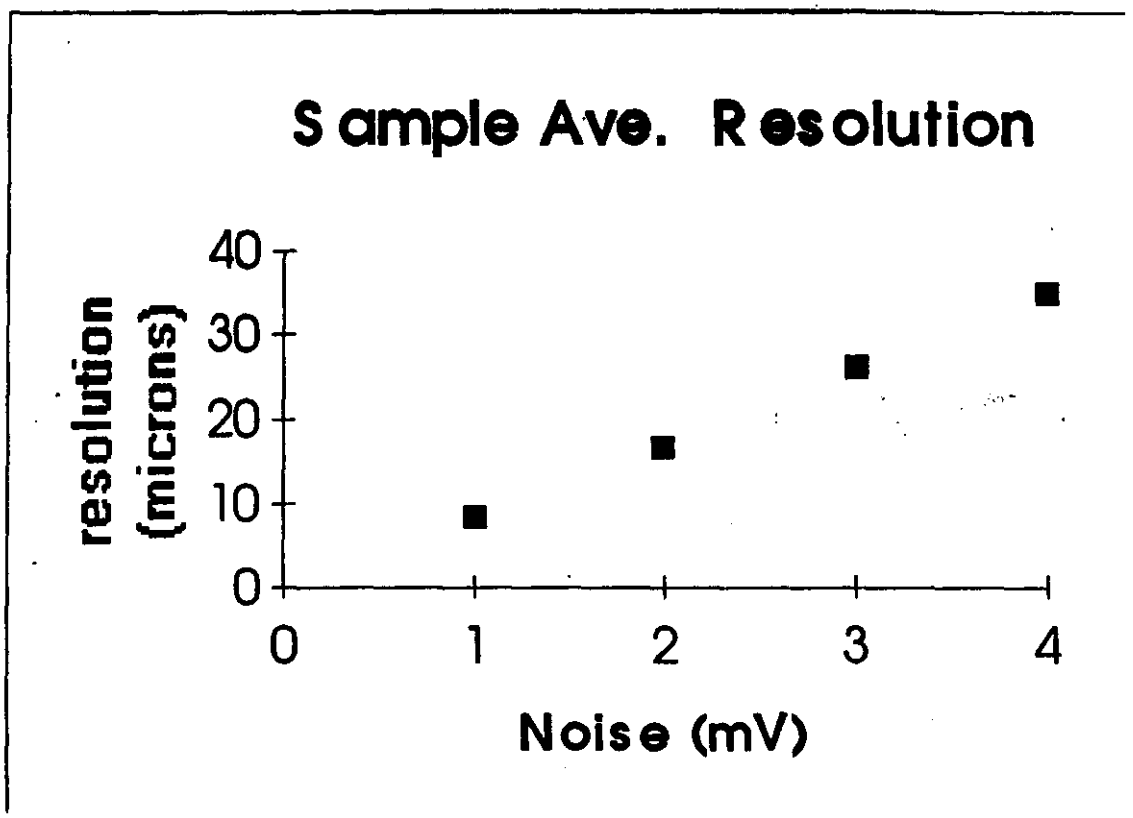


$$\frac{\sigma_x}{25\,mm} \hat{=} \sqrt{3}\,\frac{\sigma_S}{S}$$

IPC Front End Simulation

- Noise vs Resolution

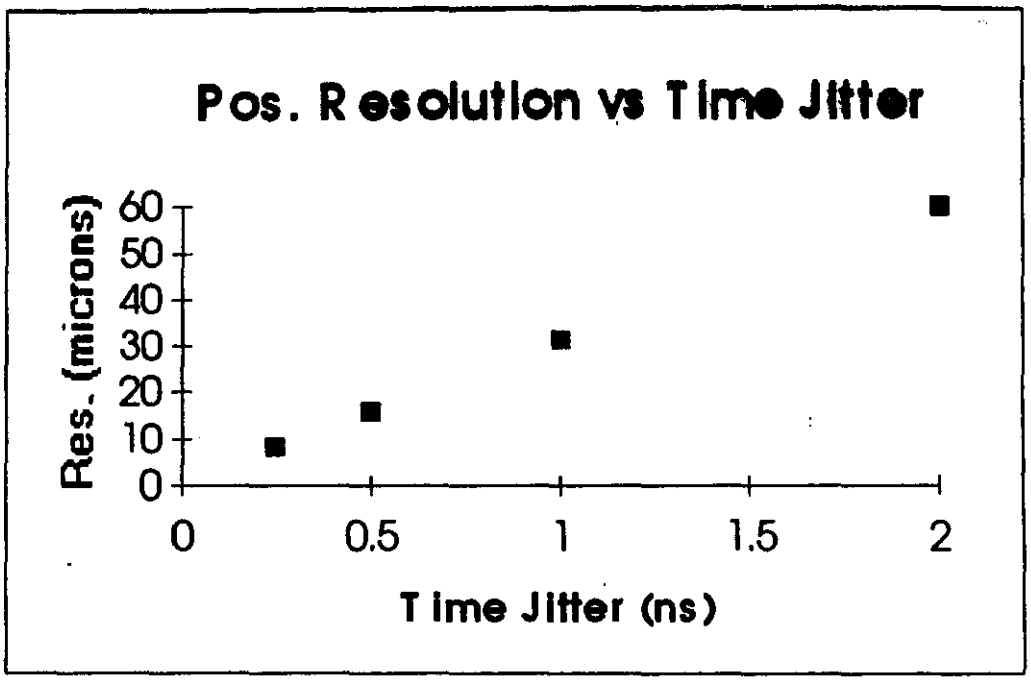
Average 3/4/5



IPC Front End Simulation

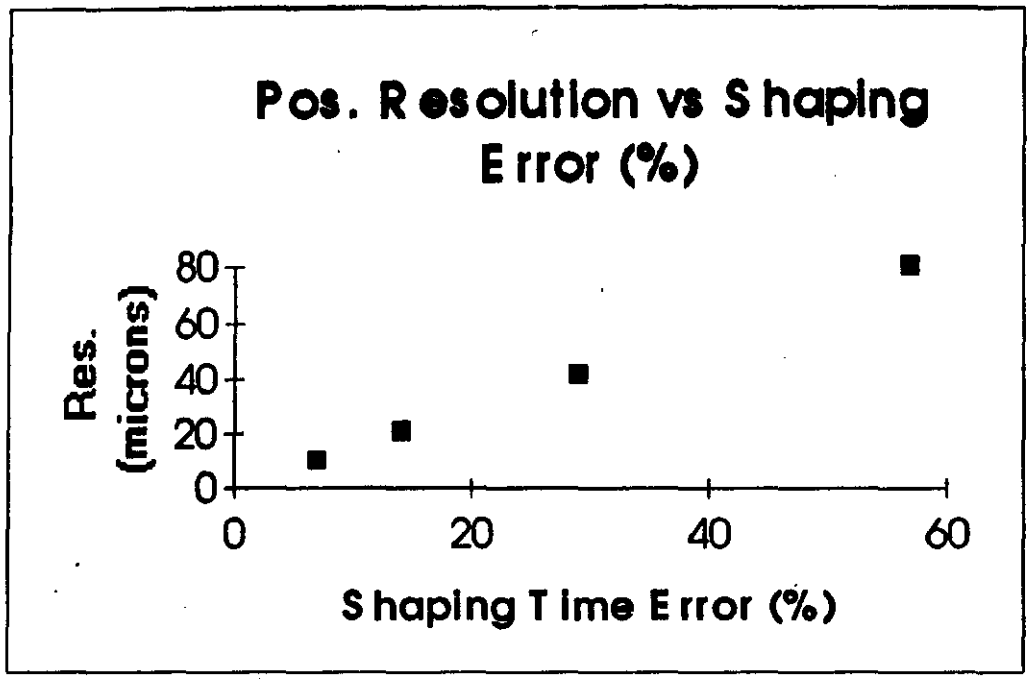
- Resolution vs Time Jitter

Average 3/4/5
No electronics noise



IPC Front End Simulation

- resolution vs shaping time errors
  No electronics noise
  No time jitter

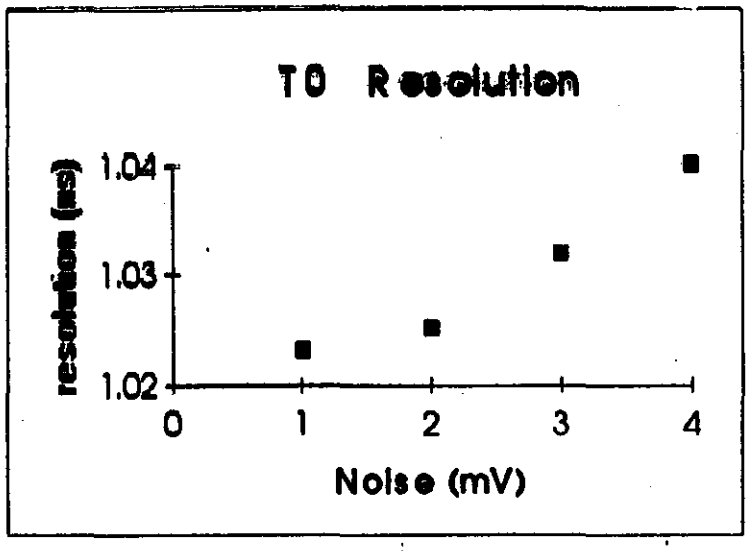


Sample 3/4/5 average

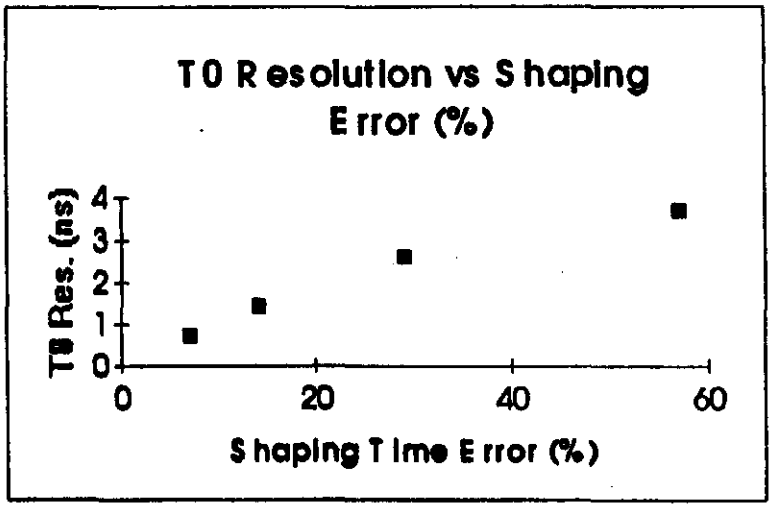
IPC Front End Simulation

- T0 resolution
  T0= (s1+16*s2+32*s3)/(s1+s2+s3)

T0 res. vs noise

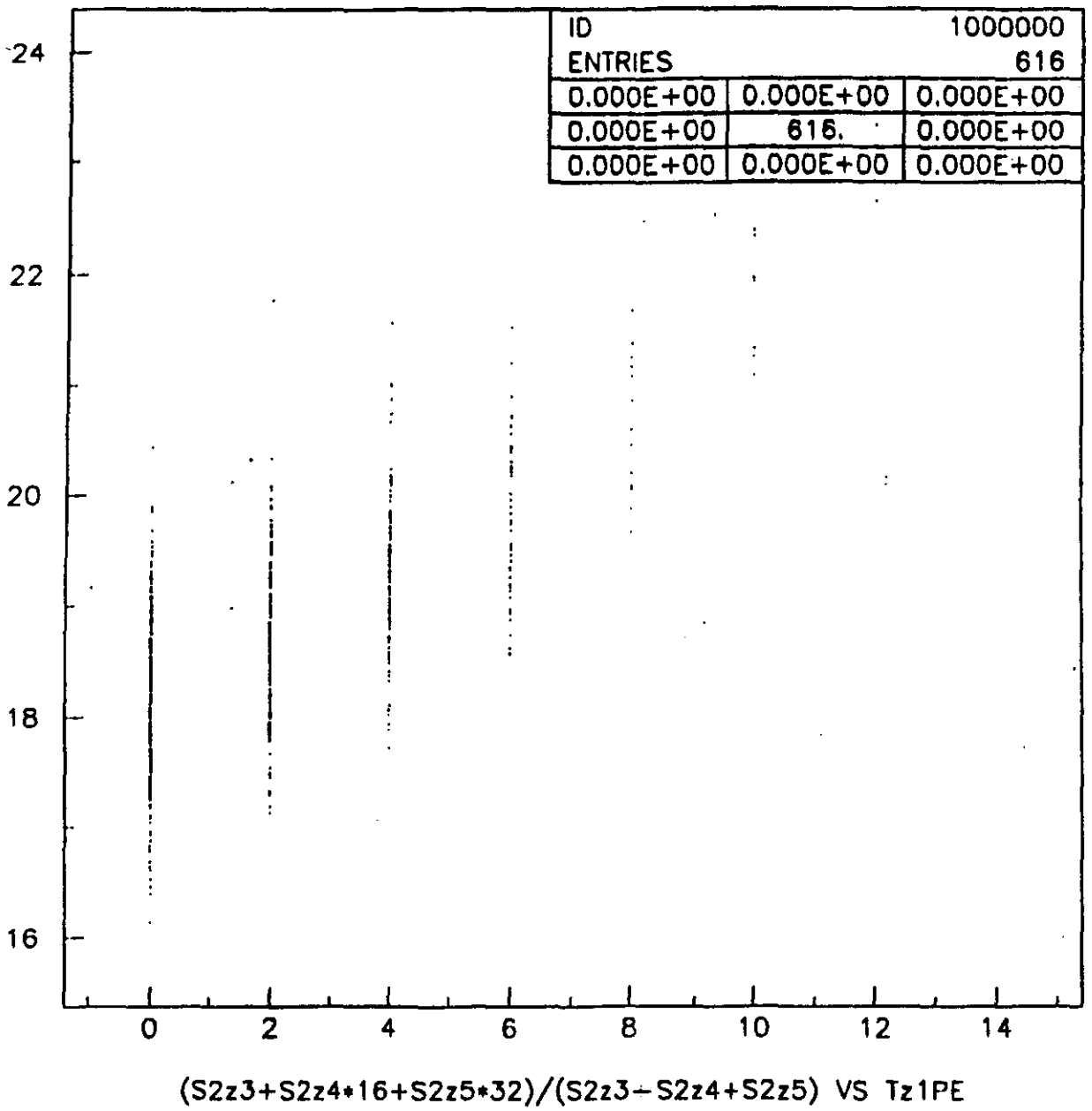


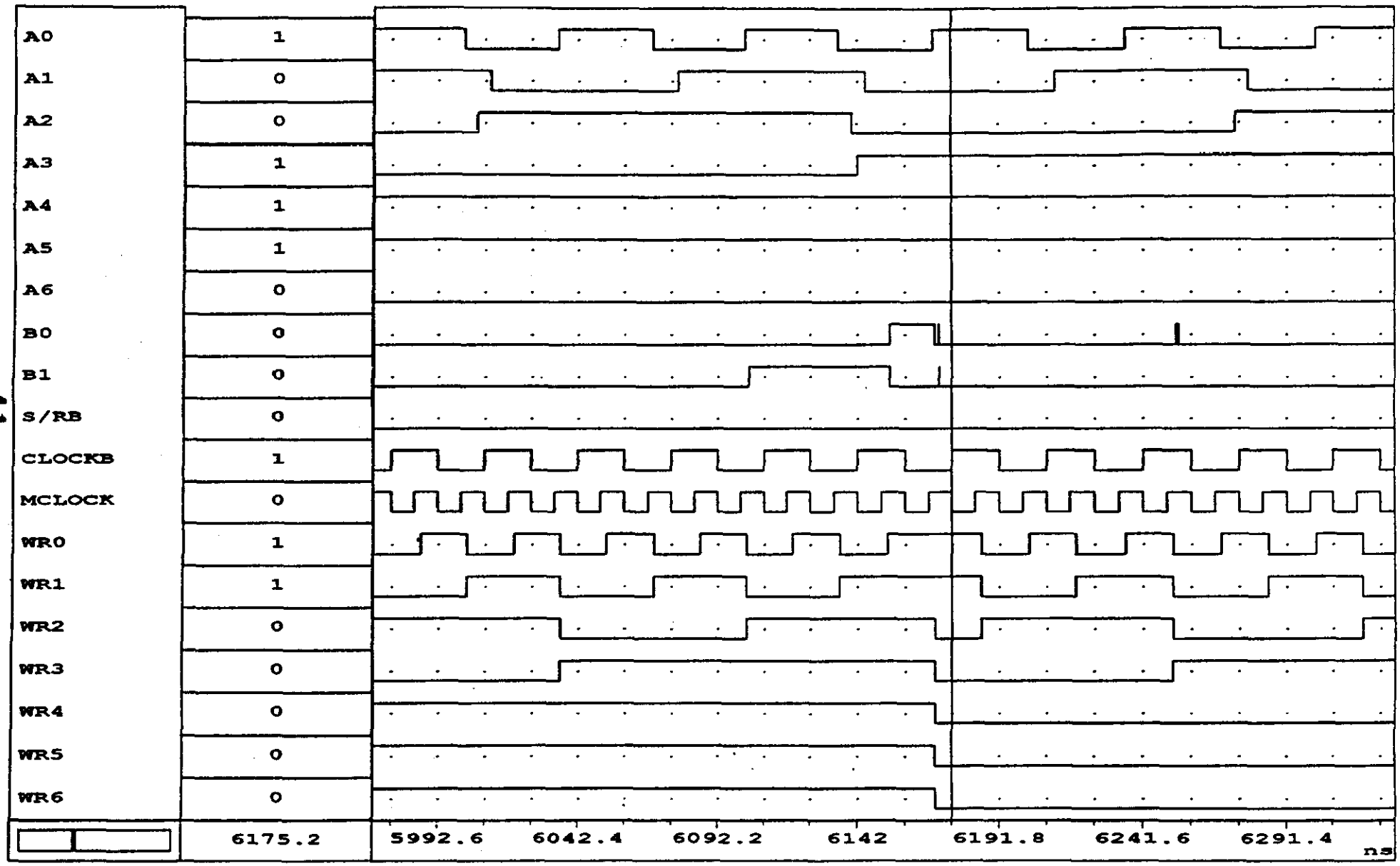
T0 res. vs shaping time error



IPC Front End Simulation

- T0 vs time of first electron at wire

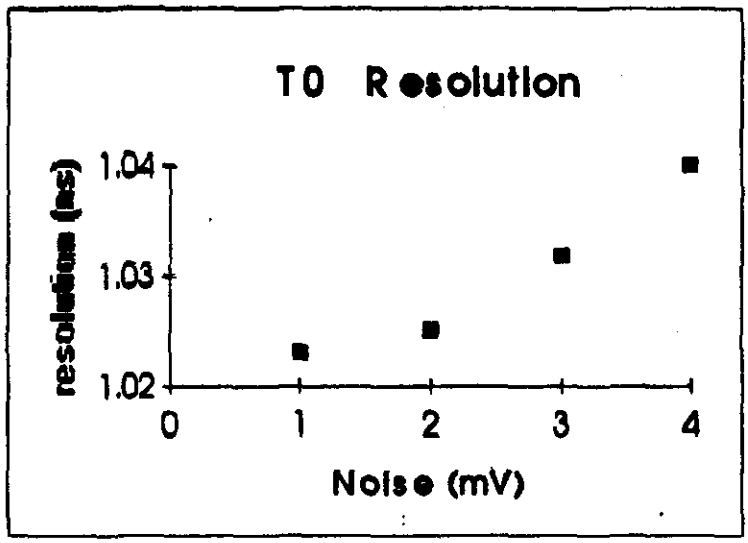



A0 1
A1 0
A2 0
A3 1
A4 1
A5 1
A6 0
B0 0
B1 0
S/RB 0
CLOCKB 1
MCLOCK 0
WR0 1
WR1 1
WR2 0
WR3 0
WR4 0
WR5 0
WR6 0
6175.2
5992.6
6042.4
6092.2
6142
6191.8
6241.6
6291.4
ns

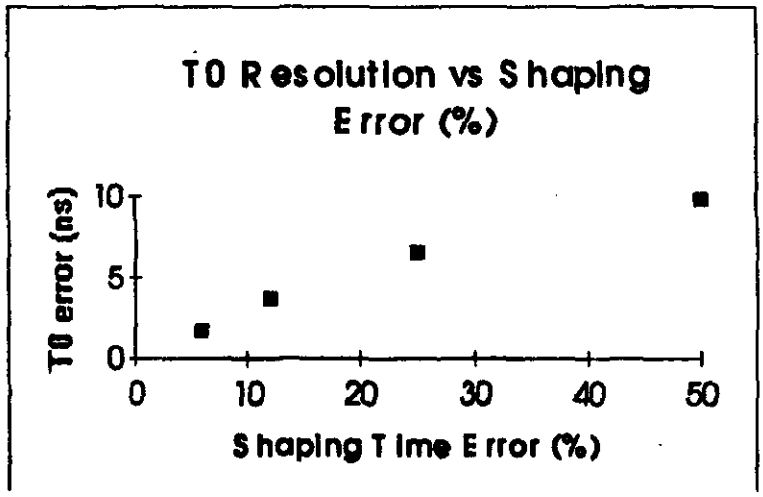
IPC Front End Simulation

- T0 resolution
  T0= (s1+16*s2+32*s3)/(s1+s2+s3)

T0 res. vs noise

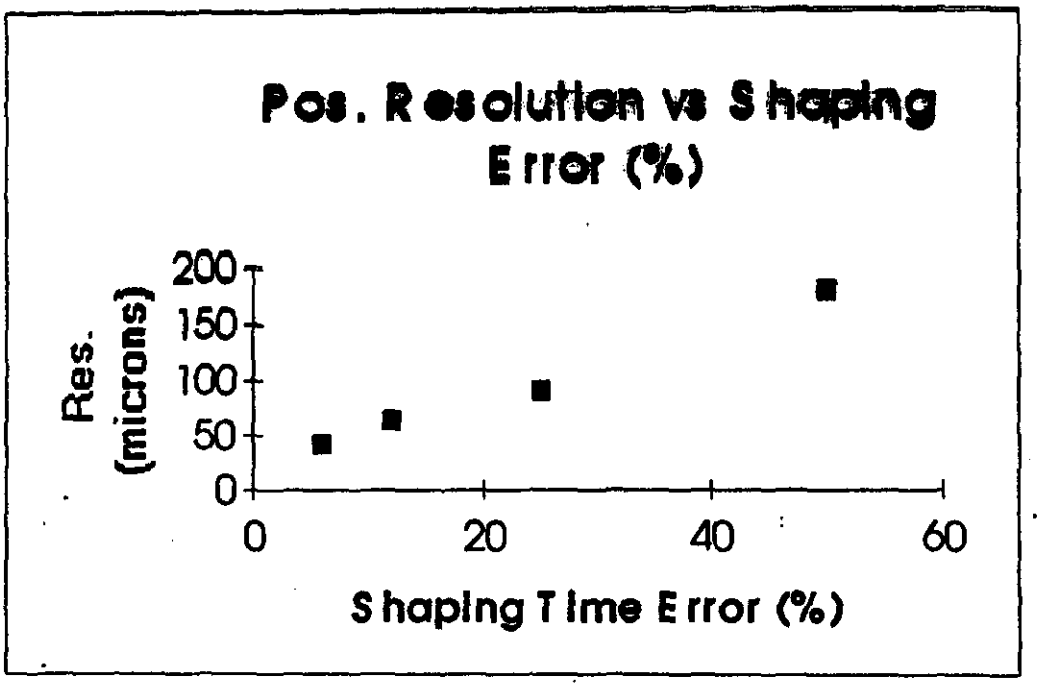


T0 res. vs shaping time error



IPC Front End Simulation

- resolution vs shaping time errors
  No electronics noise
  No time jitter



Sample 3/4/5 average

gem γeμ

Presentation by:

Eric Prebys

Update on Zero Suppression and Dynamic Range Studies for the GEM Liquid Argon Calorimeter

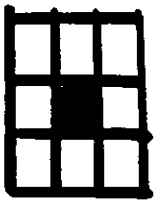
Eric Prebys, Princeton University

November 4, 1992

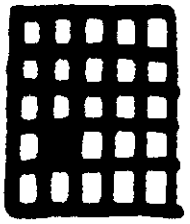
Zero Suppression Schemes

- *Scheme 1*- The simplest zero-suppression. Read out only those channels which are above a certain threshold. For this sort of suppression, the thresholds must be kept fairly low to reduce the losses in the low energy tails.

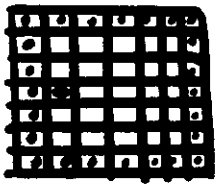
- *Scheme 2*- In this scheme, if a given channel is above threshold, all neighboring channels (front and back) are read out. Perhaps difficult to implement in practice, particularly at the boundaries between readout modules.



- *Scheme 3*- This is a fairly simple scheme. If any channel is above a given threshold, all the channels in its 5×5 readout module are read out, front and back.



- *Scheme 4*- This is somewhat like the last scheme, except that in addition to the readout cell containing the above-threshold channel, the bordering rows from the adjacent cells are read out.



Effectiveness of Zero Suppression

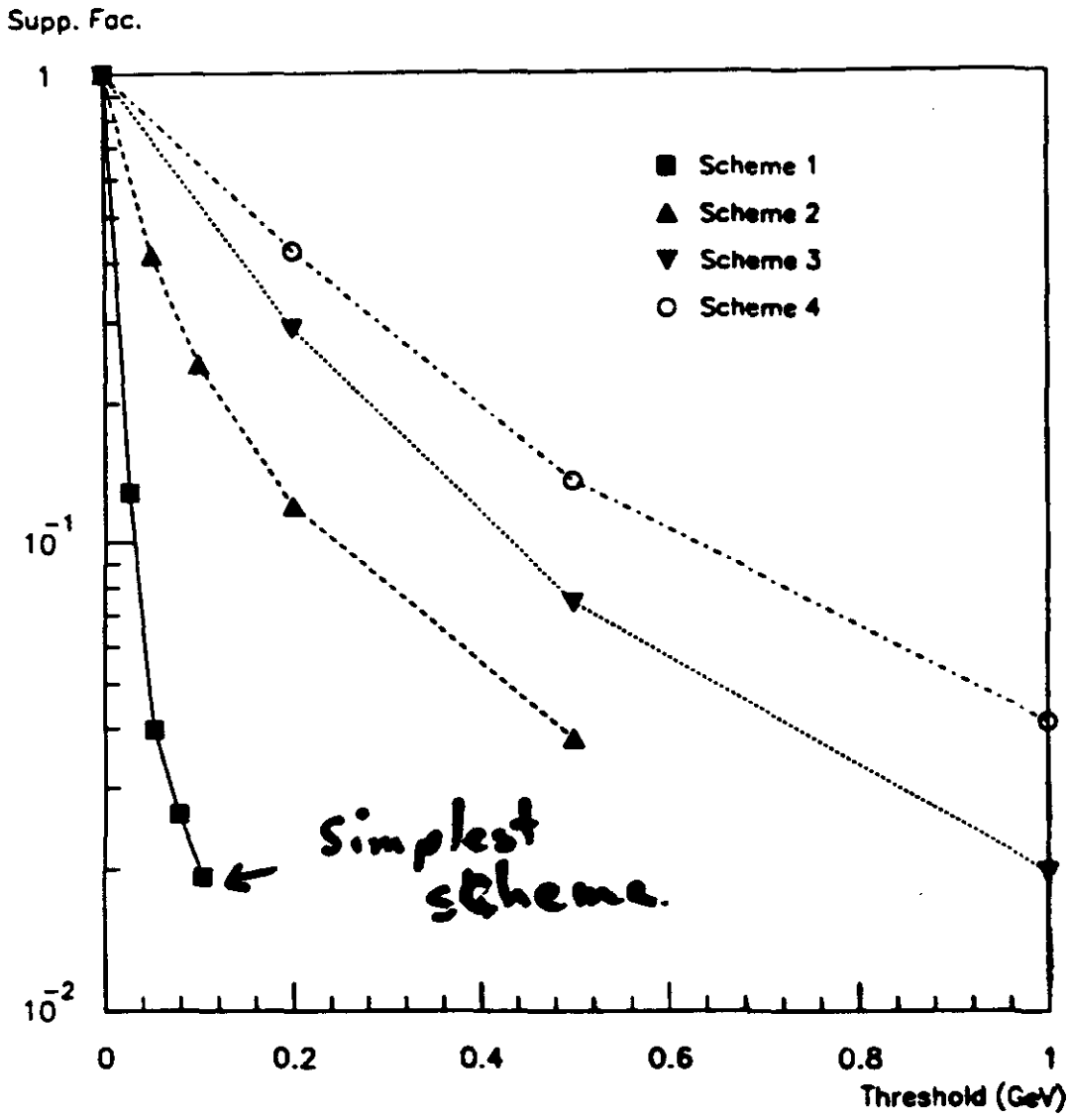


Figure 1: Zero suppression factor vs. zero suppression threshold for the various schemes discussed.

Effect on Resolution

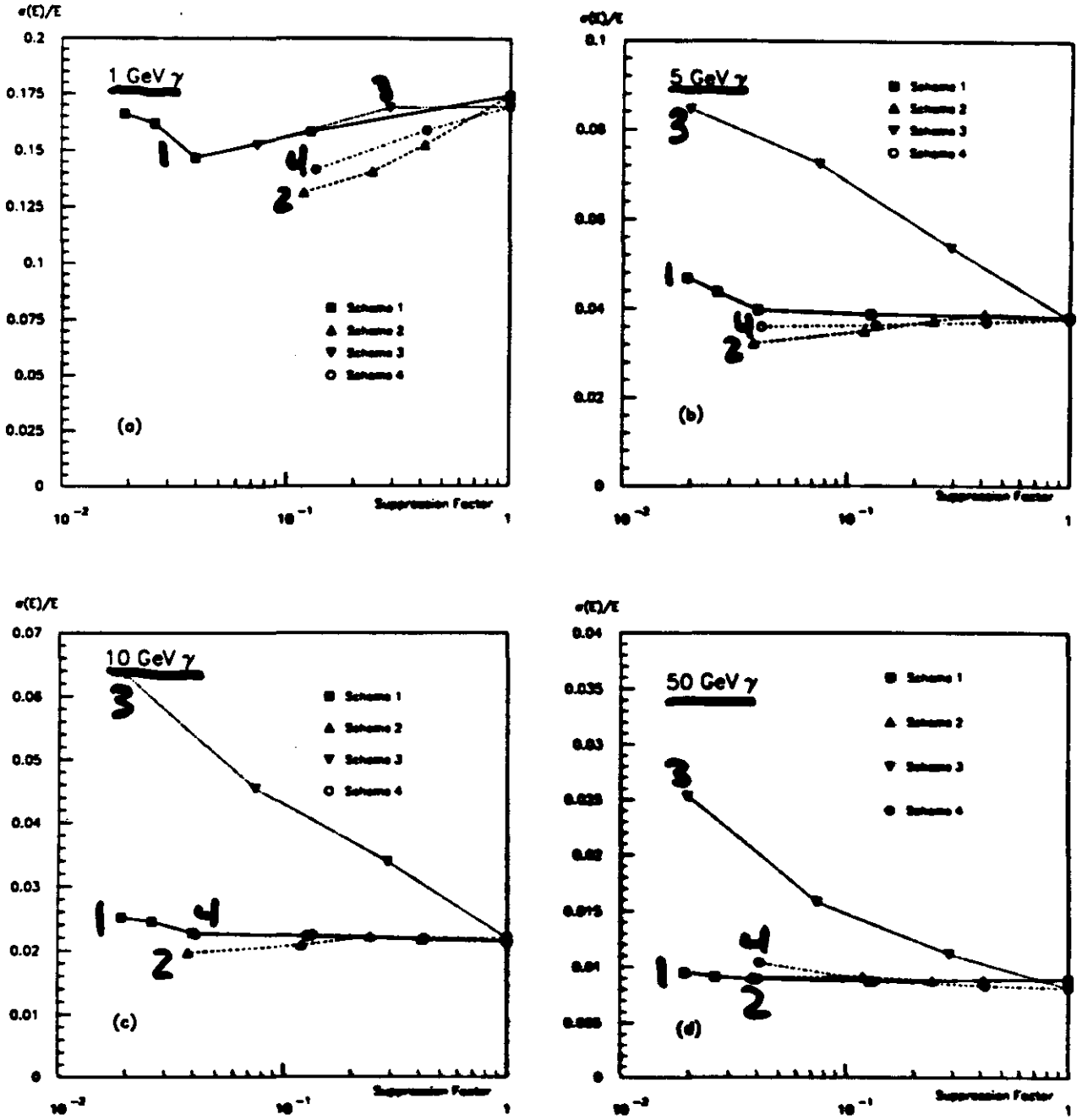


Figure 3: Energy resolution vs. zero suppression factor for various suppression schemes with (a) 1 GeV; (b) 5 GeV; (c) 10 GeV; and (d) 50 GeV photons.

Effect on Missing E_T

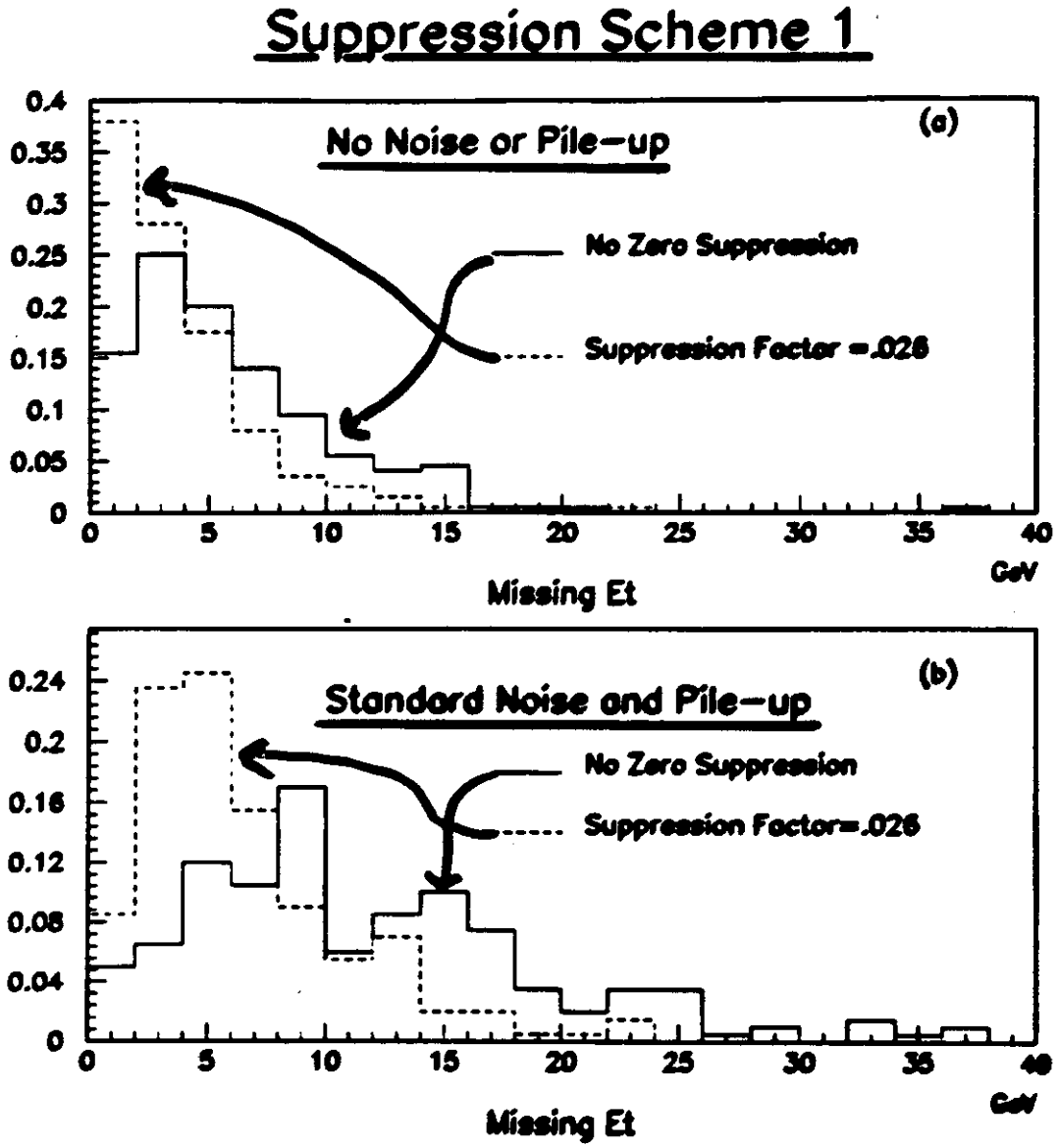


Figure 6: Effect of zero suppression on the total missing E_T spectrum (a) without and (b) with thermal and pileup noise simulated. The effects of scheme 1 zero suppression are shown by the superimposed histograms.

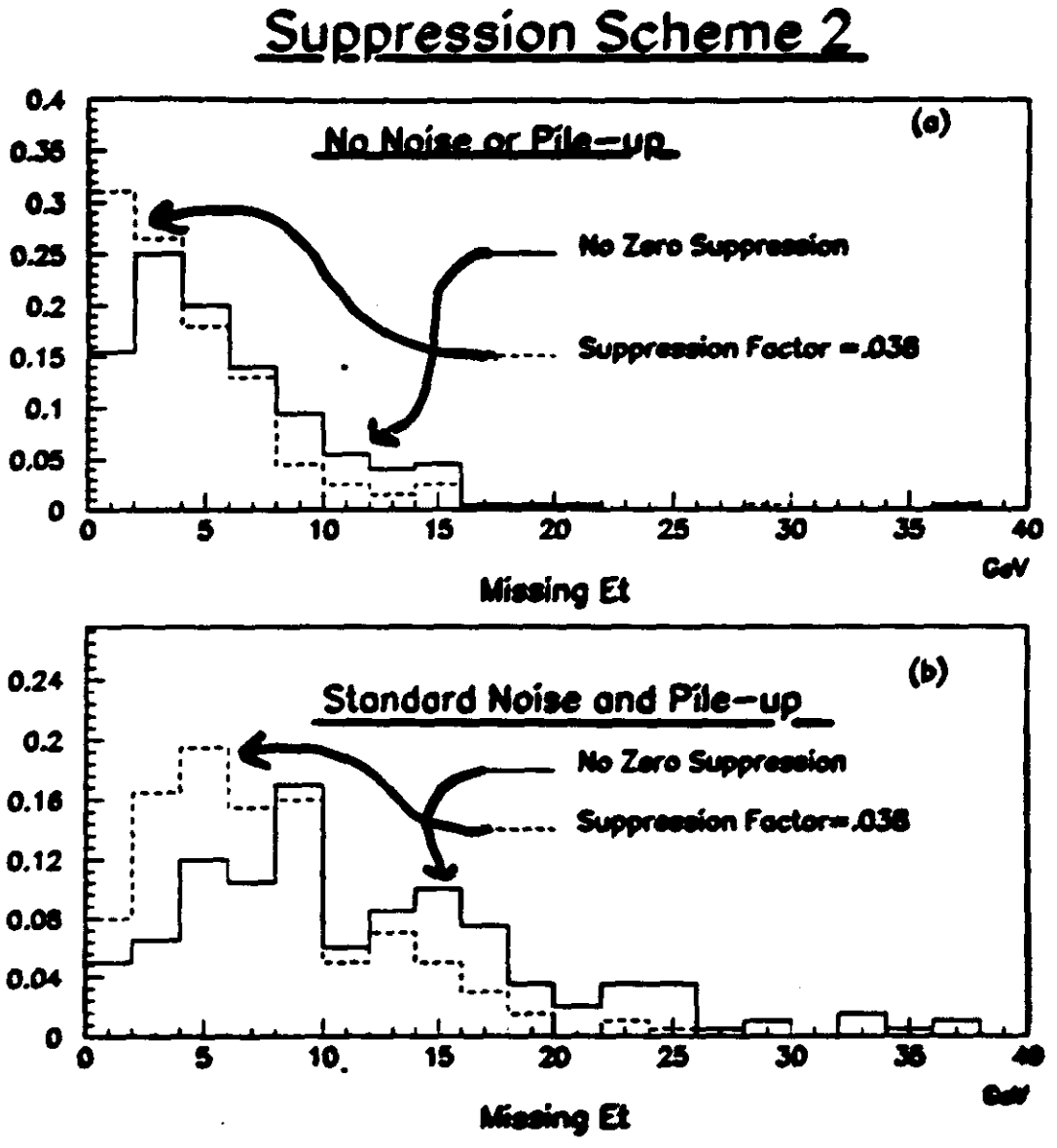


Figure 7: Effect of zero suppression on the total missing E_T spectrum (a) without and (b) with thermal and pileup noise simulated. The effects of scheme 2 zero suppression are shown by the superimposed histograms.

Zero Suppression Conclusions

Based on these studies, it is clear that one can achieve a reduction factor of greater than 10 with several zero suppression schemes without greatly sacrificing resolution or linearity. It also appears that the missing E_T resolution is not drastically compromised. Of the schemes studied, it appears that the most attractive is the most basic - namely the scheme in which one simply reads out channels satisfying a certain threshold. This scheme allows one to achieve reduction factors of up to 50 without greatly impacting the quality of the data. At lower reduction factors, the simple scheme shows similar or superior behavior to the other schemes.

Dynamic Range Studies

- Goal: To determine the dynamic range needed by both the electromagnetic and the hadronic calorimeters

- Low End of Dynamic Range: Total thermal and pileup noise $/\sqrt{2}$[1]
  - $\approx$ 25 MeV for the Electromagnetic Calorimeter
  - $\approx$ 140 MeV for the Hadronic Calorimeter

[1] To take into account the longitudinal segmentation.

High End of Dynamic Range for EM Calorimeter

Use decays of the form

$$Z' \rightarrow e^+e^-$$

Choose

$$M(Z') = 12 \text{ TeV}$$

because, assuming "standard" couplings, this gives 10 events in one year at $10^{34}\text{s}^{-1}\text{cm}^{-2}$ luminosity.

Maximum Tower Energy for EM

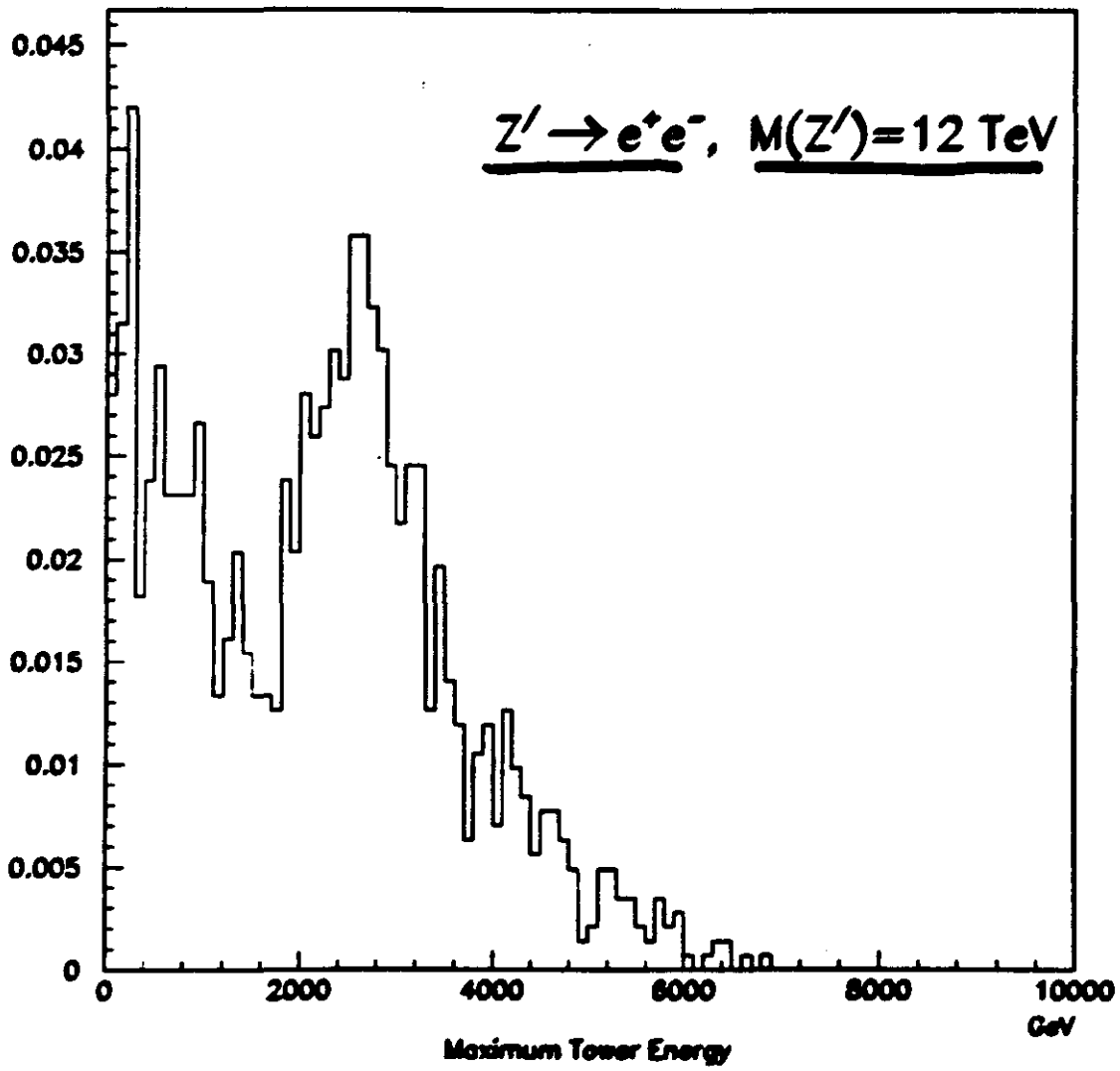


Figure 4: Highest energy in any electromagnetic tower for massive $Z' \rightarrow e^+e^-$ decays.

High End of Dynamic Range for Hadronic Calorimeter

Use high-p_T two jet events

Choose

$$p_T > 8 \text{ TeV}$$

because the standard model predicts roughly 100 events in this range in one year at $10^{34}\text{s}^{-1}\text{cm}^{-2}$ luminosity $\rightarrow$ enough to detect discrepancies (eg. compositeness).

Maximum Tower Energy for HC

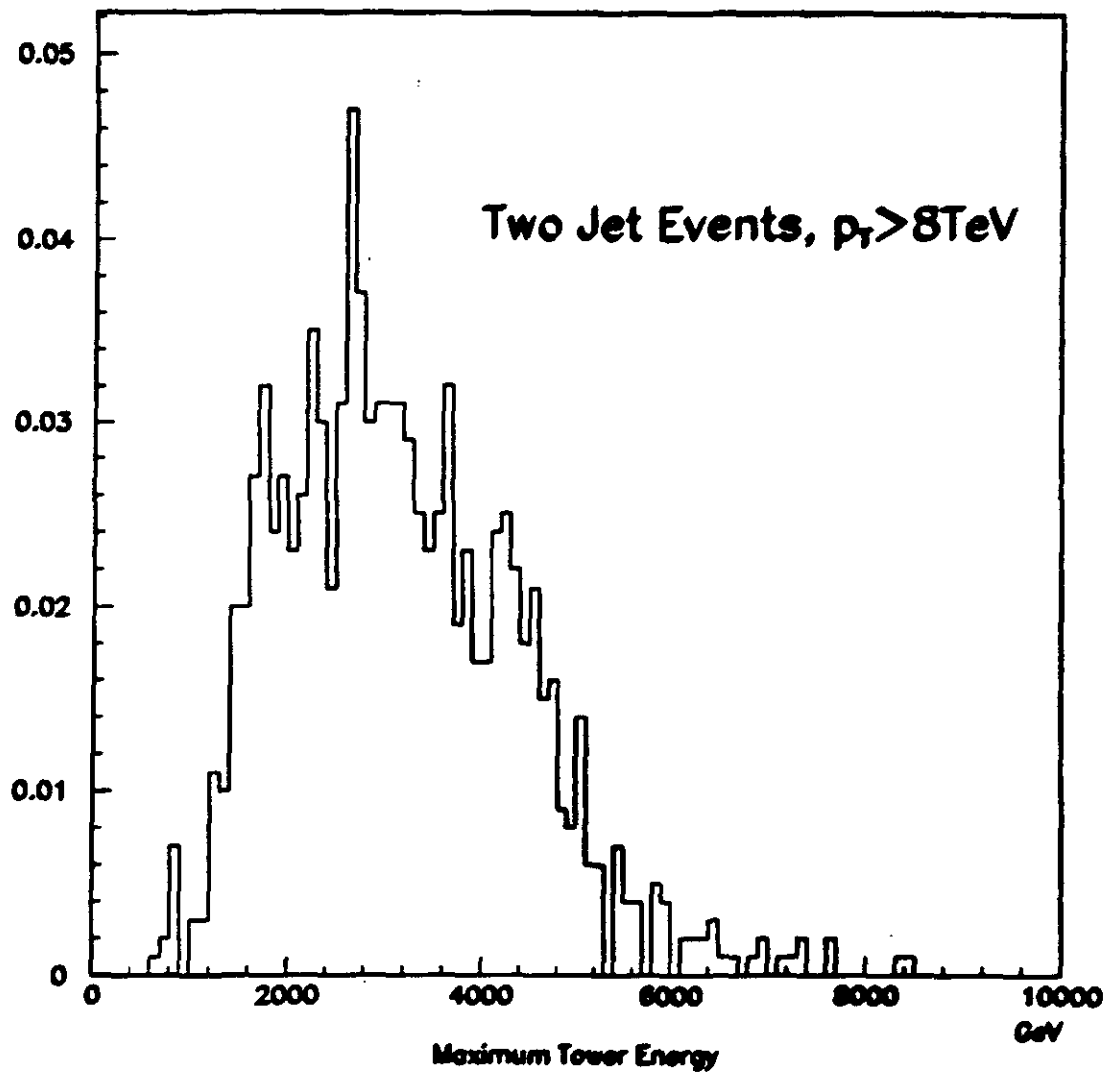


Figure 5: Highest energy in any hadronic tower for high-p_T two jet events.

Summary of Dynamic Range Studies

Electromagnetic Calorimeter

$$\textbf{range} = \frac{6000}{.025} \times \frac{6}{5} \approx 288000 \approx \underline{\textbf{18bits}}$$

negative undershoot

Hadronic Calorimeter

$$\textbf{range} = \frac{6000}{.140} \times \frac{6}{5} \approx 51400 \approx \underline{\textbf{16bits}}$$

Implementation of 18-bit Dynamic Range

- ***Nonlinear Preamps?***
  - Easy to build, but
  - Might be tricky to build and calibrate to desired accuracy.
- ***Triple Range 12-bit ADC?***
  - Probably available technology,
  - Allows 9 bit overlap, but
  - Might be tricky to build.
- ***Dual Range 13-bit ADC?***
  - Only two ranges needed, but
  - Only 8 bit resolution at overlap.
  - Might not exist.
- ***Some Combination of the Above?***

Implications for $H \to \gamma\gamma$

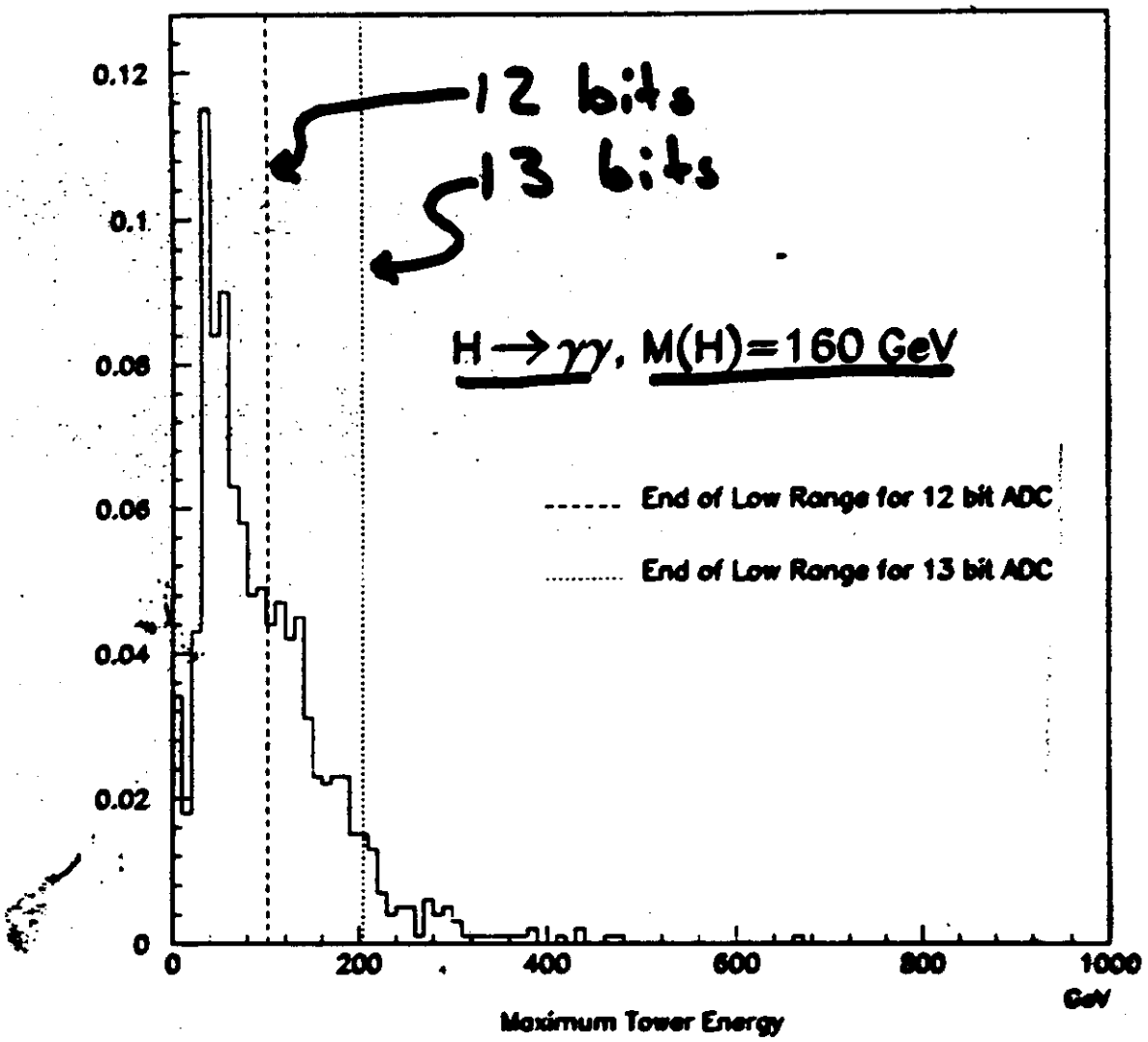


Figure 6: Highest energy in any electromagnetic tower for $H \to \gamma\gamma$ decays.

gem

γeμ

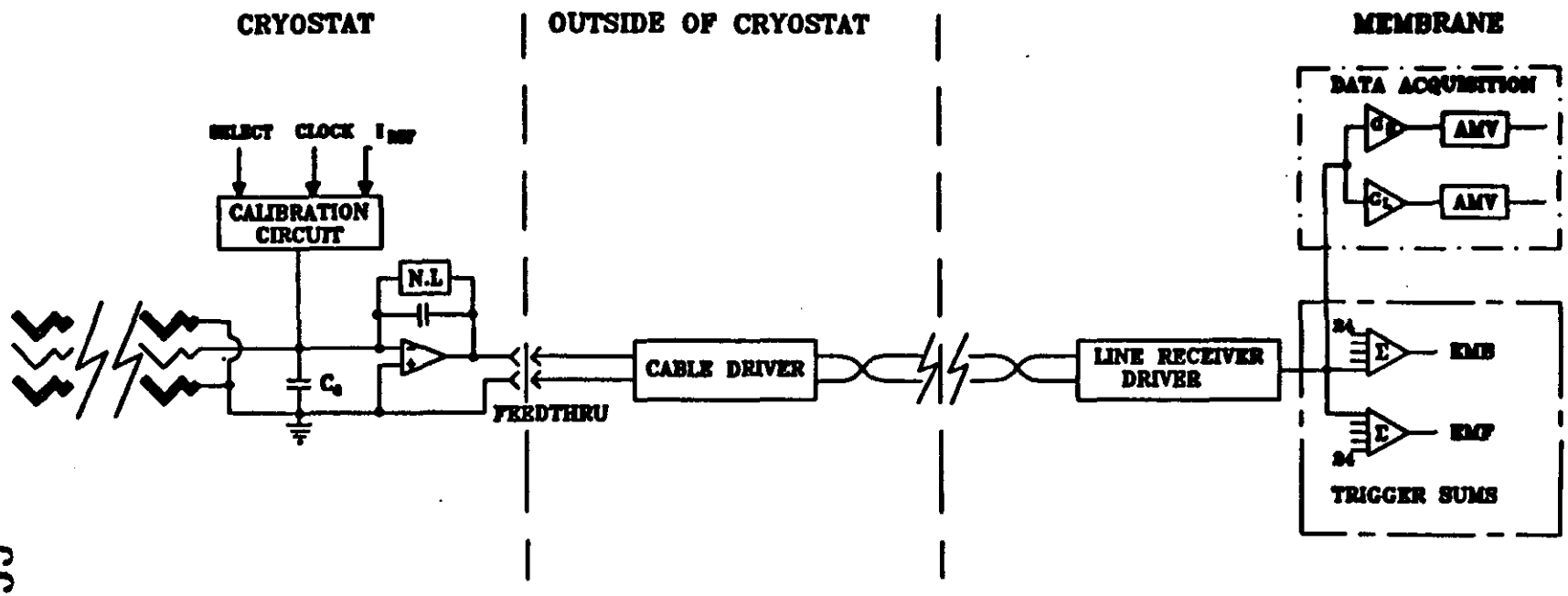
Presentation by:

Sergio Rescia

Sergio Rescia
Instrumentation Division
Brookhaven National Laboratory

LKr/LAr CALORIMETER FRONT-END ELECTRONICS

GEM COLLABORATION MEETING
BNL, 5 Nov. 1992


CRYOSTAT
OUTSIDE OF CRYOSTAT
MEMBRANE
SELECT
CLOCK
I_{REF}
CALIBRATION CIRCUIT
N.L
C_d
FEEDTHRU
CABLE DRIVER
LINE RECEIVER DRIVER
DATA ACQUISITION
AMV
AMV
24
Σ
EMB
24
Σ
EMF
TRIGGER SUMS

AIM:

Design of a charge sensitive preamplifier for Liquid Argon preamplifier for cryogenic ionization chamber calorimeters (Liquid Argon, Krypton) at hadron collider experiments (SSC, LHC).

ENVIRONMENT
(10 years of operation)

T=90 K

Neutron Flux: 10^{14} N/cm^2

Dose: 30 Mrad

SPECIFICATIONS

Low Noise (trigger sums)

C_D=100 pF-1 nF

t_p=15-50 ns

High g_m, g_m/C_{iss}, g_m/I_{DSS}

$C_D/10<C_{iss}<C_D/2$

W=10^4 μm (1 cm)

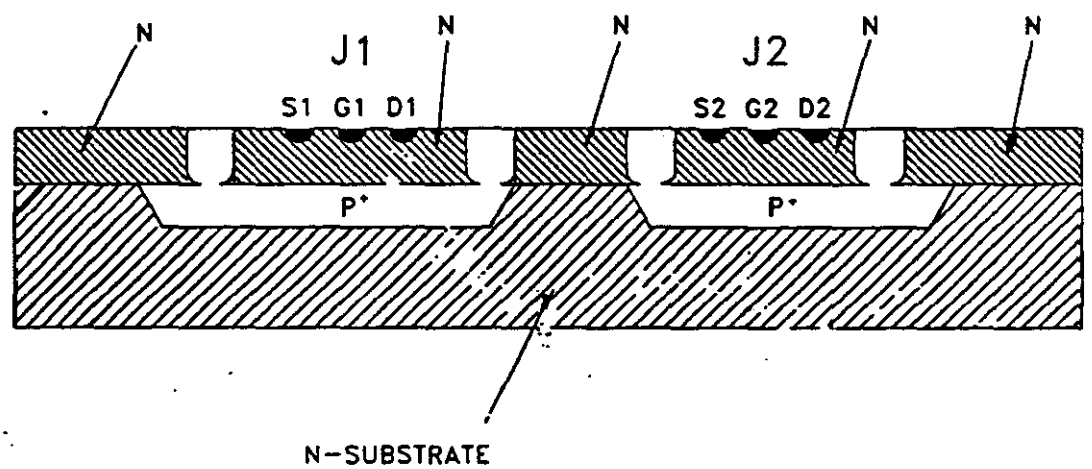
TECHNOLOGY

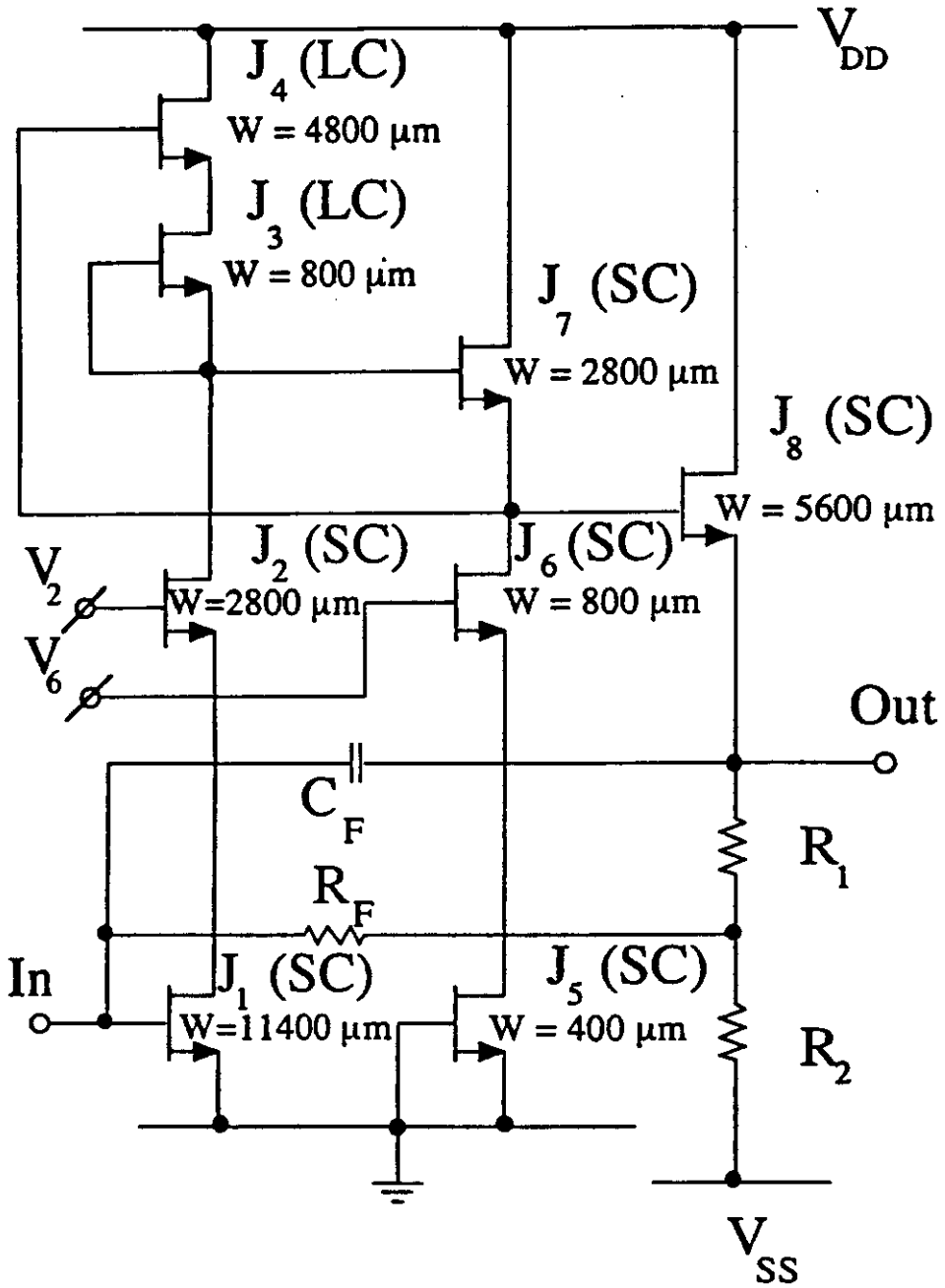
Epitaxial channel JFETs meet all these requirements and are manufactured with a mature, well proven technology. Hybrid preamplifiers using discrete JFETs have been built and successfully operated up to three years.
To achieve monolithic integration interdevice isolation must be obtained *while preserving the characteristic of discrete JFETs.*

BURIED LAYER TECHNOLOGY

To achieve interdevice insulation a junction-insulated technology based on a diffused P^+-type buried layer which acts as a back gate has been developed. It uses an epi channel and diffused gate, source and drain to achieve an optimum noise performance.

- ρ_{subs}=0.5 Ωcm
- ρ_{buried}=0.002 Ωcm
- ρ_{epi}=0.5-2 Ω cm
- t_{epi}=4-7 μm
- isolation ring doping: >10^{18} cm^{-3} at the surface to prevent surface inversion




V_{DD}
J_4 (LC)
W = 4800 µm
J_3 (LC)
W = 800 µm
J_7 (SC)
W = 2800 µm
J_8 (SC)
W = 5600 µm
V_2
V_6
J_2 (SC)
W=2800 µm
J_6 (SC)
W = 800 µm
Out
C_F
R_F
R_1
In
J_1 (SC)
W=11400 µm
J_5 (SC)
W = 400 µm
R_2
V_{SS}

P	FEATURES	I_d[mA]	$g_m\left[\frac{mA}{V}\right]$	$SW_e\left[\frac{nV}{\sqrt{Hz}}\right]$	$SW_t\left[\frac{nV}{\sqrt{Hz}}\right]$	$\frac{SW_e}{SW_t}$	GBW [MHz]
1	TEST PADS ADDED (ceramic carrier)	9.2	48.3	0.57	0.49	1.16	200
2	TEST PADS ADDED (ceramic carrier)	1.9	22	0.76	0.72	1.05	112
3	TEST PADS ADDED (ceramic carrier)	2	23	0.75	0.70	1.07	127
4	NO TEST PADS (TO-78)	3	26	0.73	0.68	1.07	194
5	TEST PADS ADDED (ceramic carrier)	4	32	0.66	0.60	1.10	136
6	NO TEST PADS (TO-78)	5	31	0.68	0.61	1.11	200

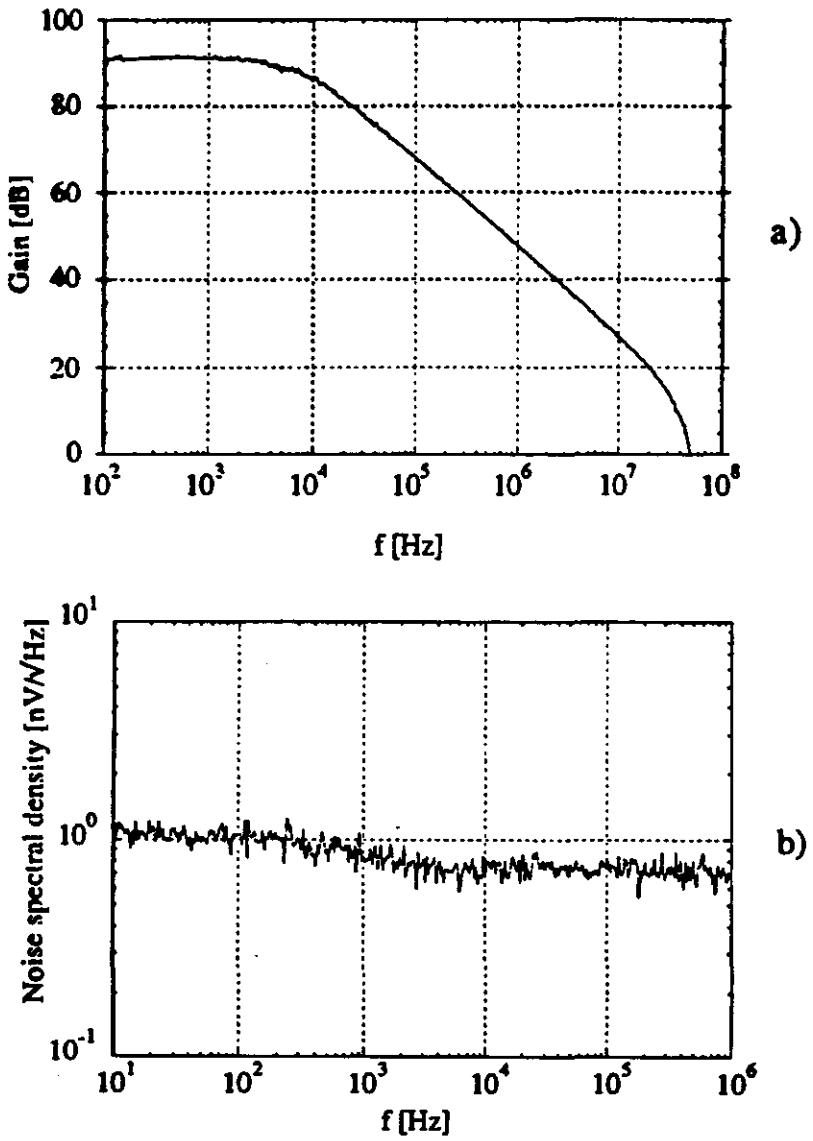
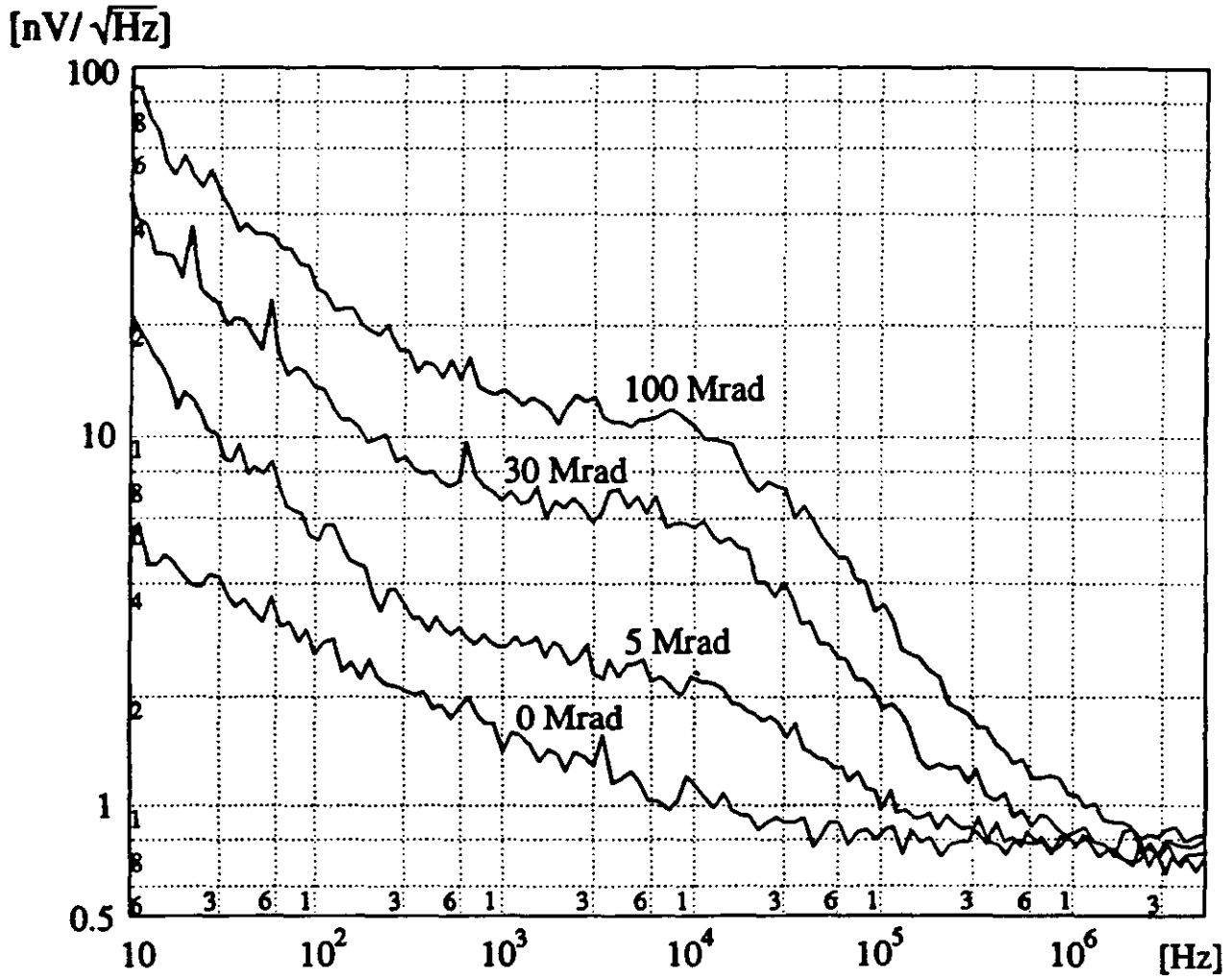


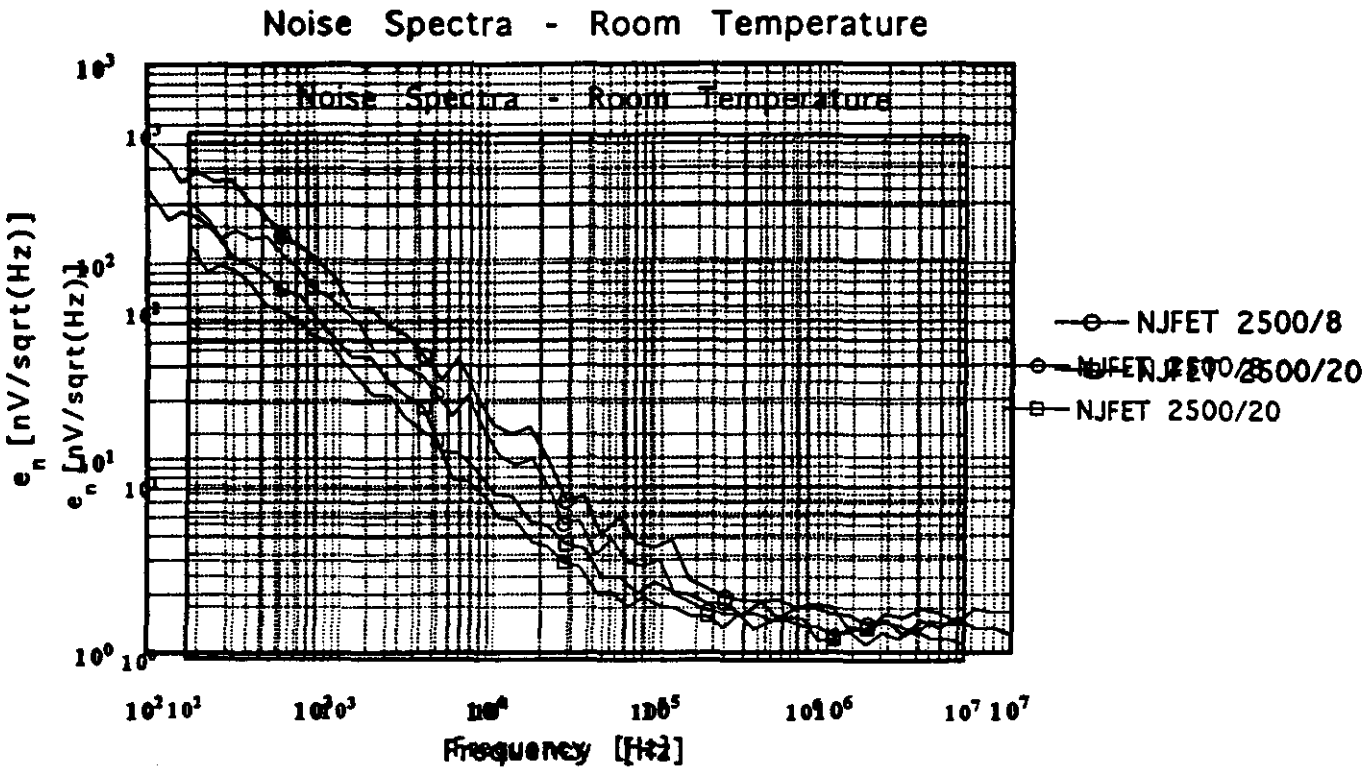
Fig. 2 - Characteristics of the preamplifier labelled 4 in Table I.
(a) Open-loop gain-frequency dependence.
(b) Spectral density of the noise voltage referred to the preamplifier input as a function of frequency.

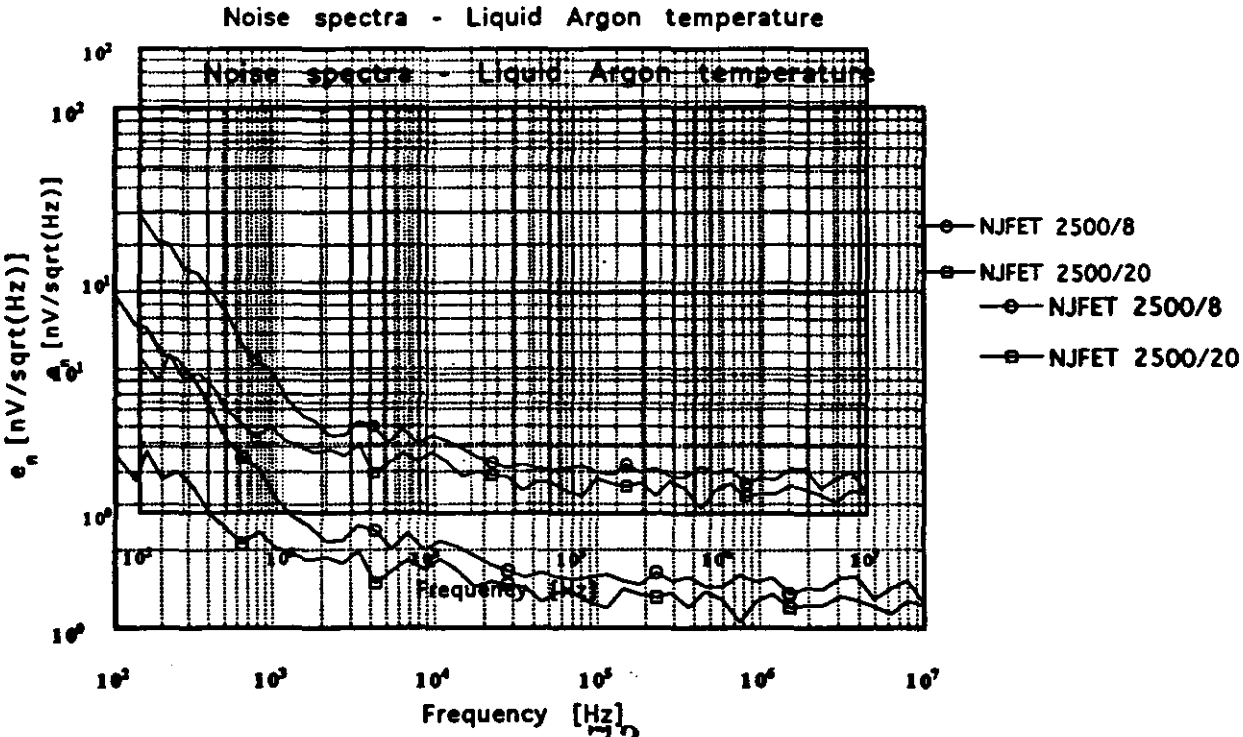
JFET RADIATION EFFECTS
(^{60}Co)

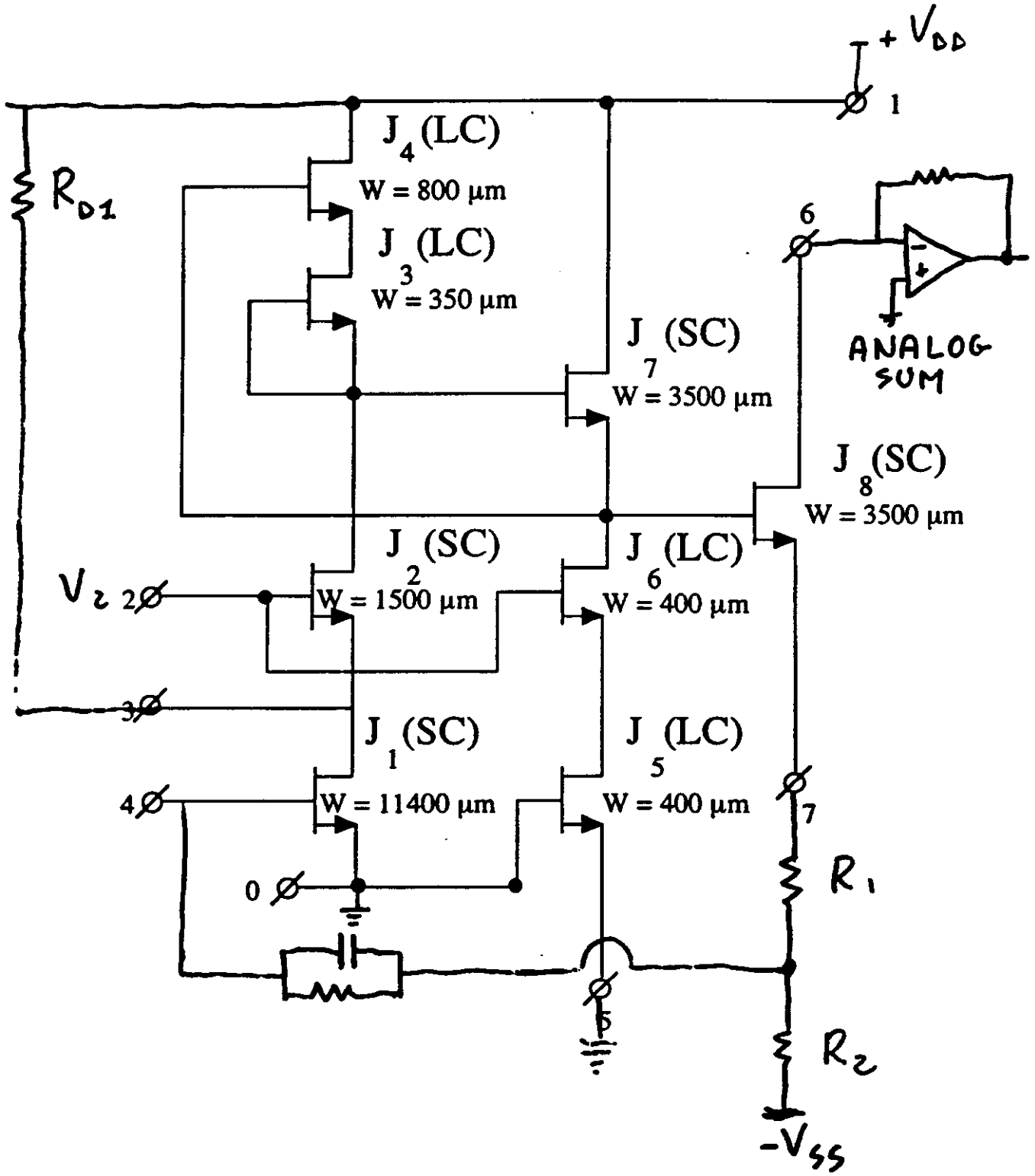
NOISE SPECTRUM

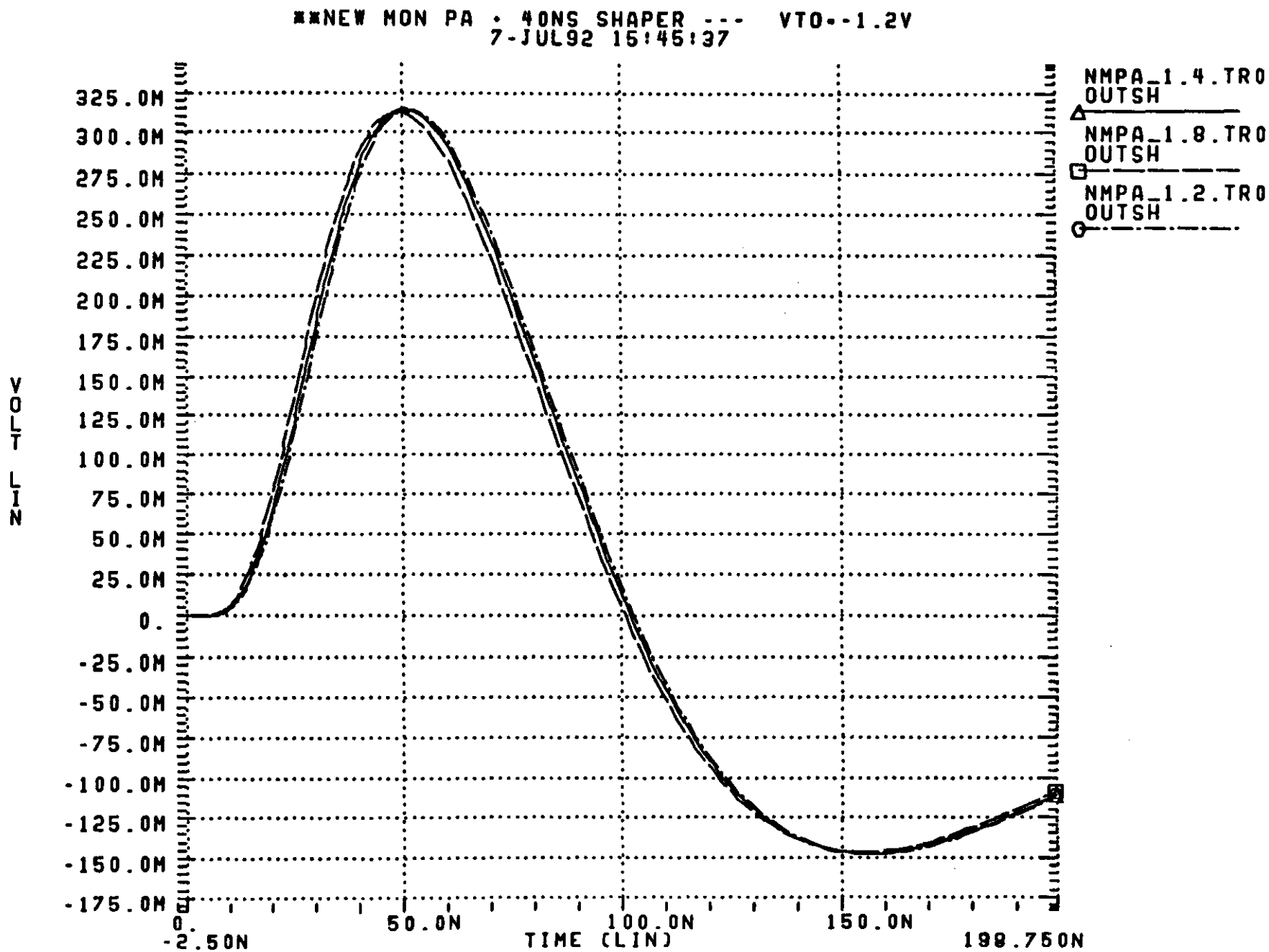


SHORT CHANNEL JFETs : NOISE






+ V_{DD}
1
R_{D1}
J_4 (LC)
W = 800 µm
J_3 (LC)
W = 350 µm
6
ANALOG SUM
J_7 (SC)
W = 3500 µm
J_8 (SC)
W = 3500 µm
V_2 2
J_2 (SC)
W = 1500 µm
J_6 (LC)
W = 400 µm
3
J_1 (SC)
W = 11400 µm
J_5 (LC)
W = 400 µm
4
7
0
R_1
5
R_2
$-V_{SS}$


**NEW MON PA . 40NS SHAPER --- VTO--1.2V
7-JUL92 15:45:37
NMPA_1.4.TRO
OUTSH
NMPA_1.8.TRO
OUTSH
NMPA_1.2.TRO
OUTSH
VOLT LIN
325.0M
300.0M
275.0M
250.0M
225.0M
200.0M
175.0M
150.0M
125.0M
100.0M
75.0M
50.0M
25.0M
0.
-25.0M
-50.0M
-75.0M
-100.0M
-125.0M
-150.0M
-175.0M
0.
-2.50N
50.0N
100.0N
150.0N
198.750N
TIME (LIN)

SUMMARY

A monolithic charge sensitive preamplifier has been realized featuring:

- GBW=200 MHz
- P_{diss}=100 mW
- Dynamic Range=+2 V
- Integral non-linearity=0.2%
- en=0.7 nV/√Hz
- No degradation after 100 Mrad (t_p=40 ns, T=90 K)

Future Improvements:

- Study of neutron resistance
- Realization of monolithic resistors (Si-Cr)
- Development of a short channel version
- Non-linear response for expanded dynamic range

Acknowledments:

Larry A. Rehn, INTERFET Co.

gem

γeμ

Presentation by:

H. Takai

Precision Timing with Liquid Ionization Calorimeters

O. Benary[9], S. Cannon[5], W. Cleland[7], I. Ferguson[2], C. Finley[5], A. Gordeev[6], H. Gordon[3], E. Kistenev[3], P. Kroon[3], M. Leltchouk[5], D. Lissauer[3], H. Ma[3], D. Makowiecki[3], A. Maslennikov[4], S. McCorkle[3], D. Onoprienko[6], A. Onuchin[4], Y. Oren[9], V. Panin[4], J. Parsons[5], J. Rabel[7], V. Radeka[3], L. Rogers[3], D. Rahm[3], S. Rescia[3], J. Rutherfoord[2], M. Seman[5], M. Smith[3], J. Sondericker III[3], R. Steiner[1], D. Stephani[3], E. Stern[7], I. Stumer[3], H. Takai[3], H. Themann[8], Y. Tikhonov[4]

1. Adelphi University, Garden City, NY 11530
2. University of Arizona, Tucson, AZ 85721
3. Brookhaven National Laboratory, Upton, NY 11973
4. Budker Institute for Nuclear Physics, Novosibirsk, Russia
5. Columbia University, New York, NY 15633
6. Oak Ridge National Laboratory, Oak Ridge, TN 37831
7. University of Pittsburgh, Pittsburgh, PA 15260
8. SUNY at Stony Brook, Stony Brook, NY 11794
9. Tel-Aviv University, Tel-Aviv, Israel

Precision Timing with Liquid Ionization Calorimeters.

- Good timing from Calorimeters:

  ⟶ unique assignment of an event to a particular beam crossing. (bunch spacing ~15 ns)

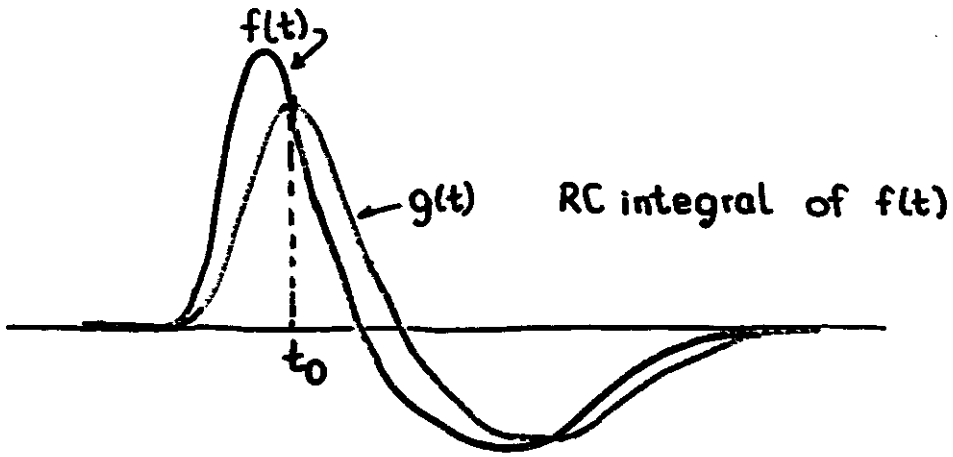
- Conventional Wisdom:

  "Scintillators are fast; PMT have sharp signal"
  therefore: "GOOD TIMING"

- HOWEVER:

  Liquid ionization Calorimeters have:
  - very uniform waveform
  - very low fluctuations (3×10^6 e^-/GeV)
  - good timing is possible !

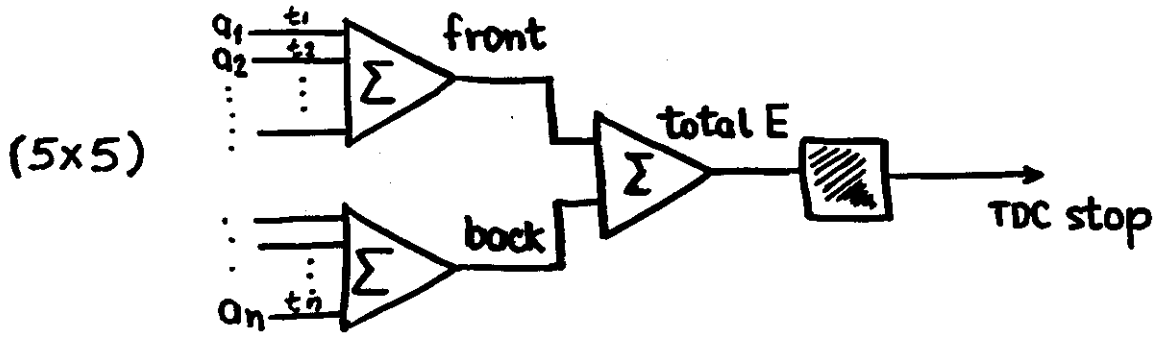
Principle of Operation (Turko & Smith)



☞ t_0, when $f(t) = g(t)$ is independent of amplitude.

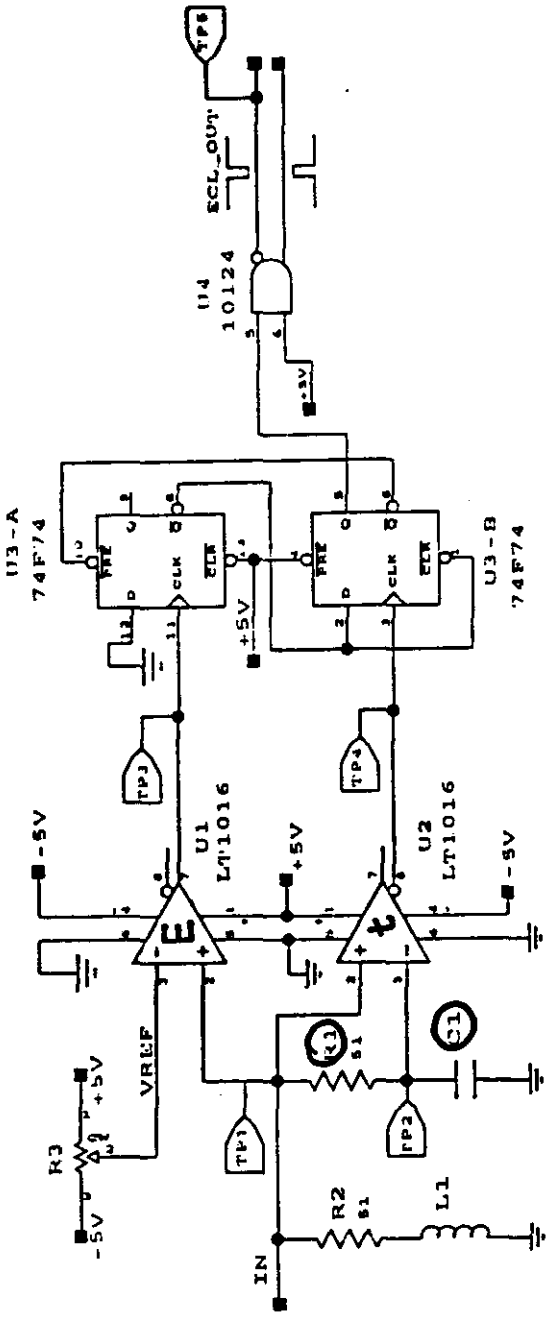
Test Setup:

- Accordion geometry Liquid Krypton Calorimeter
- P_{beam} = 5, 10, 15, 20 GeV

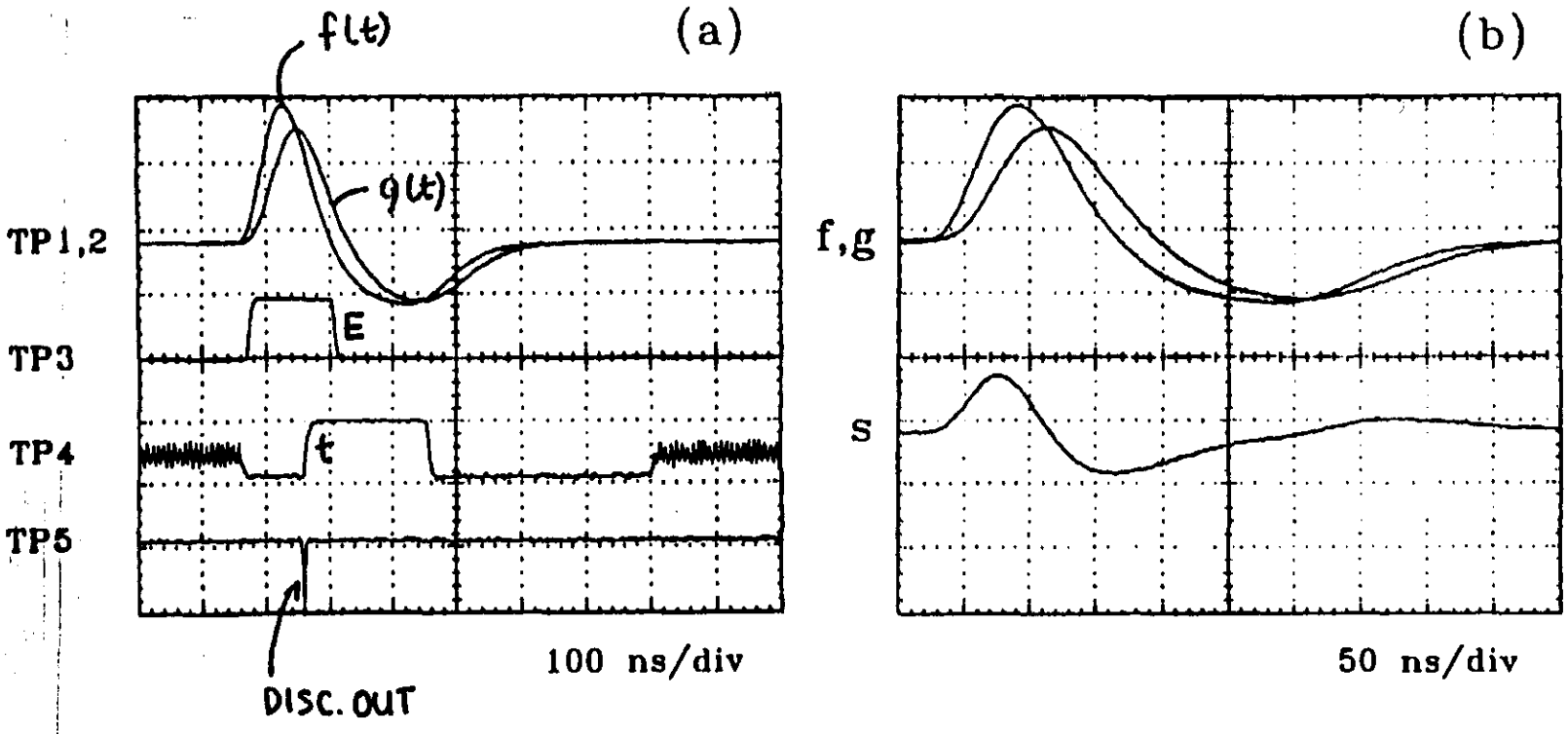


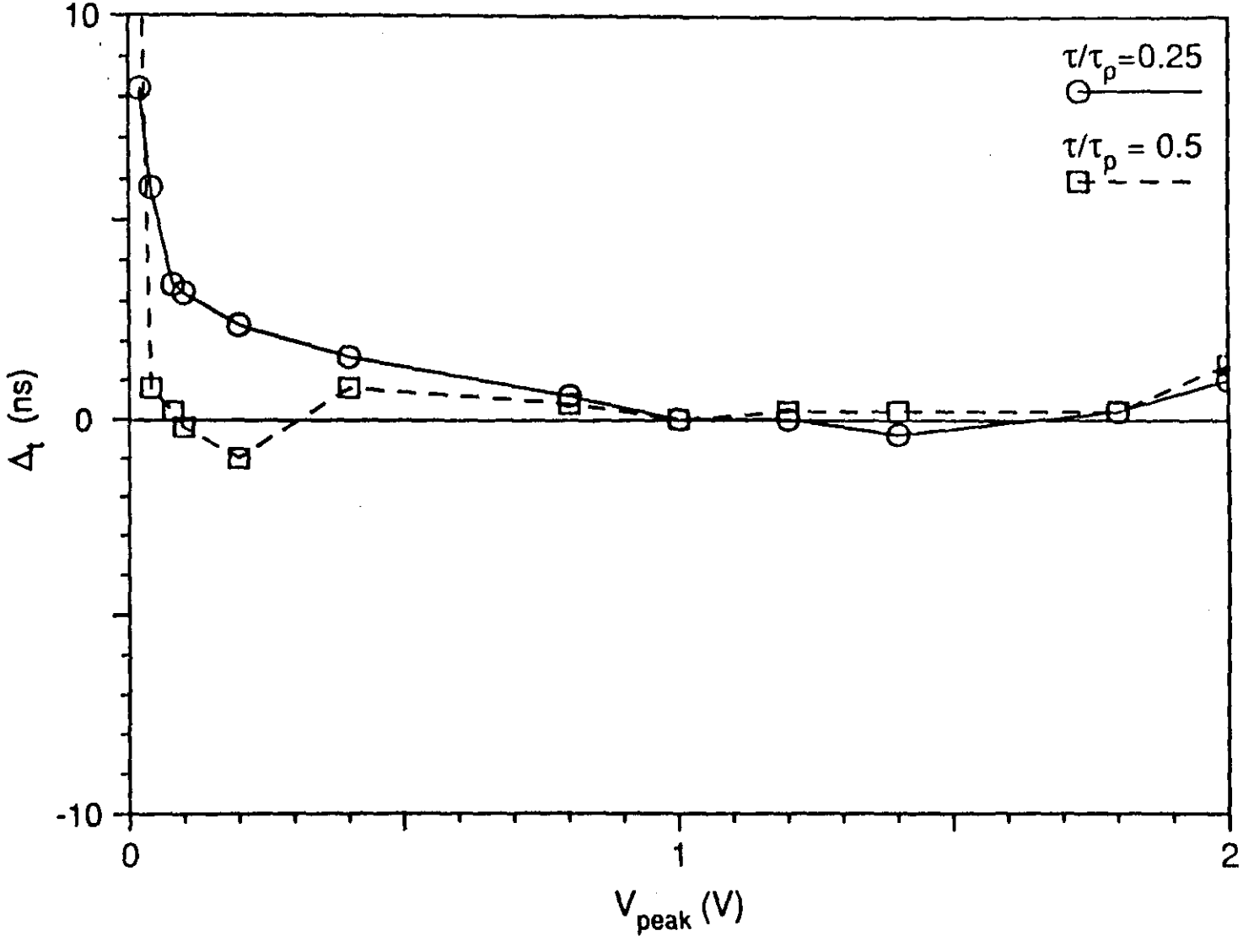
- Total Energy → $F(t) = \sum a_i f(t - t_i)$

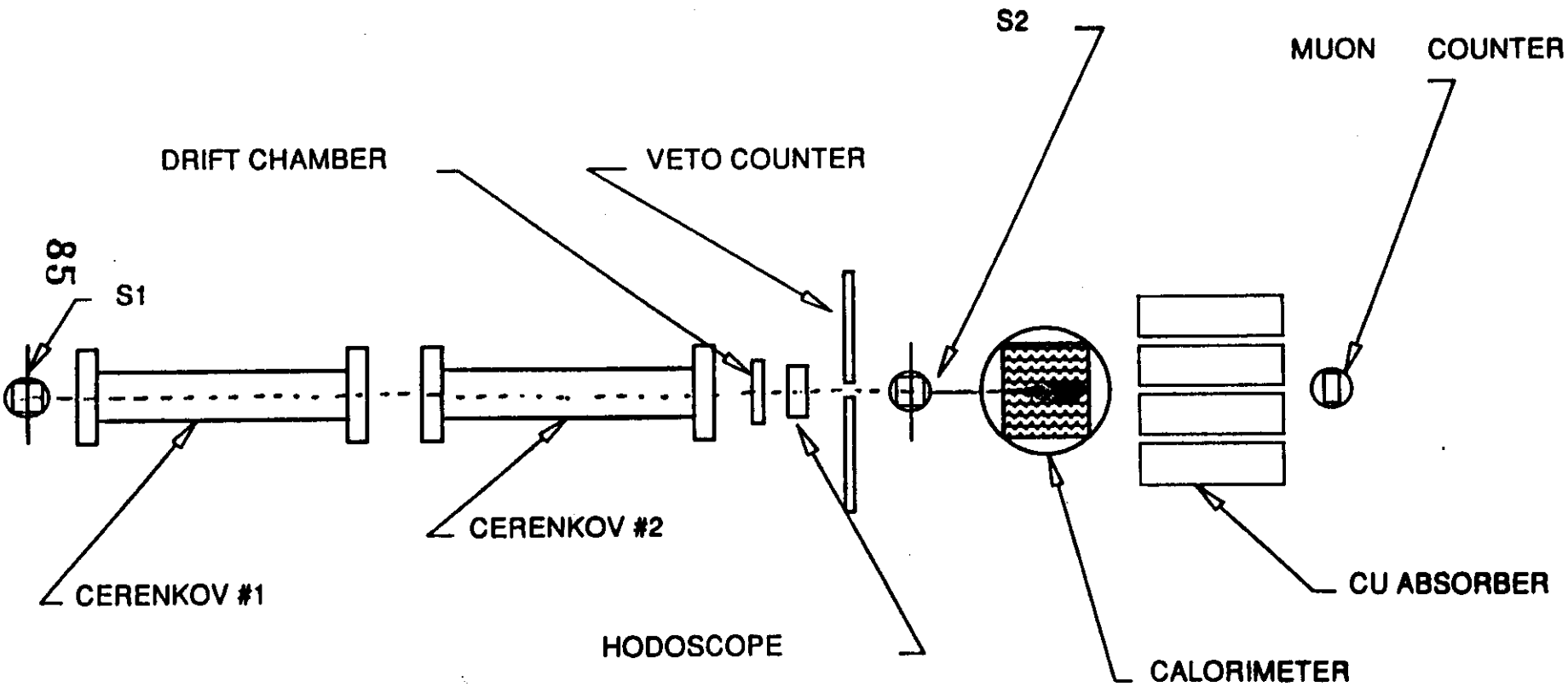
t_i, channel time offset.



U4
10124
ECL_OUT
U3-A
74F74
U3-B
74F74
U1
LT1016
U2
LT1016
-5V
+5V
VREF
R3
R2
L1
IN


(a)
f(t)
g(t)
TP1,2
TP3
E
TP4
t
TP5
DISC. OUT
100 ns/div
(b)
f,g
s
50 ns/div


10
0
-10
0
1
2
Δ_t (ns)
V_{peak} (V)
τ/τ_p=0.25
τ/τ_p = 0.5



S_1, S_2 timed by CFDs

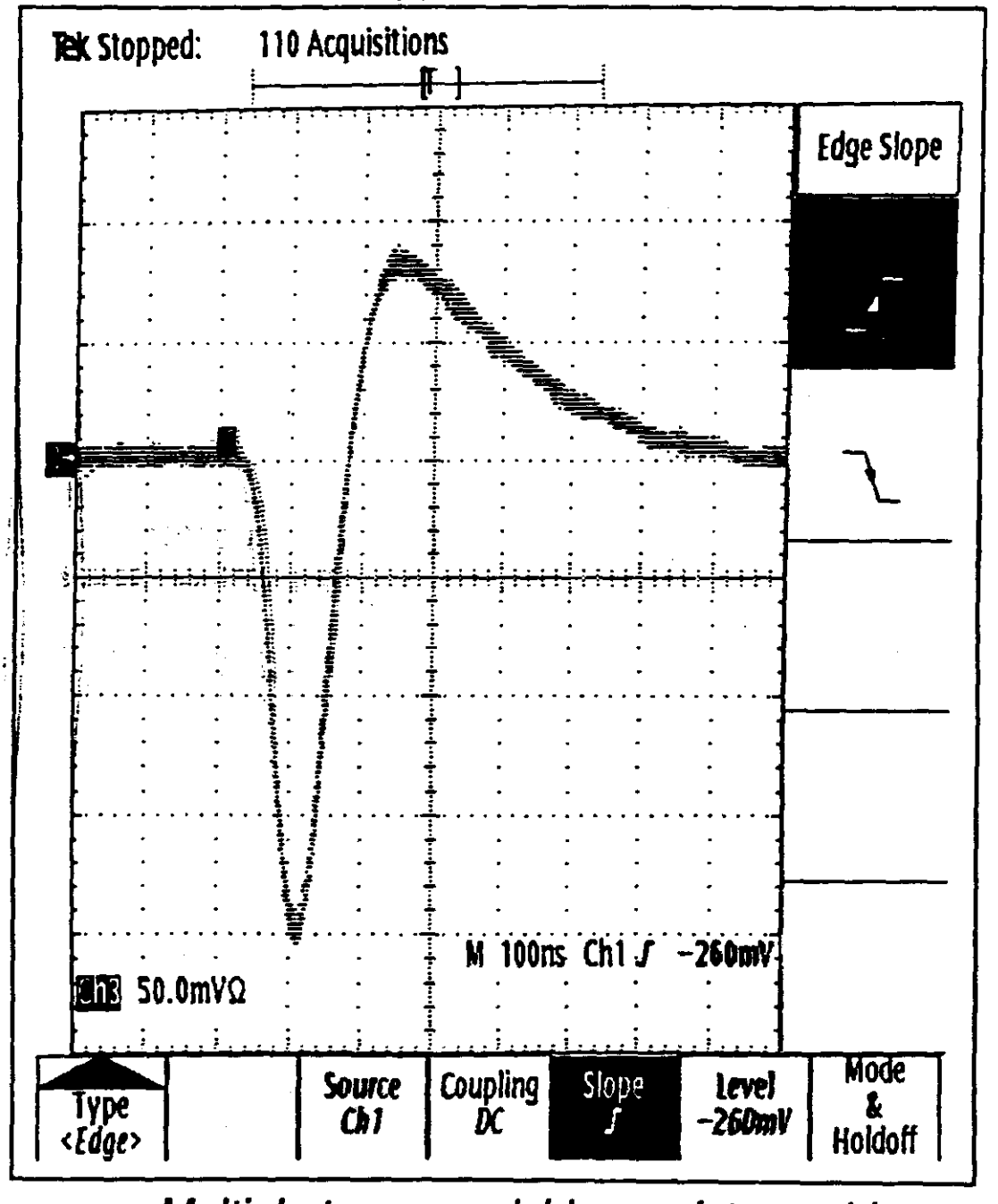
$S_2 \Rightarrow$ Start Counter

On-line Pulse Shape

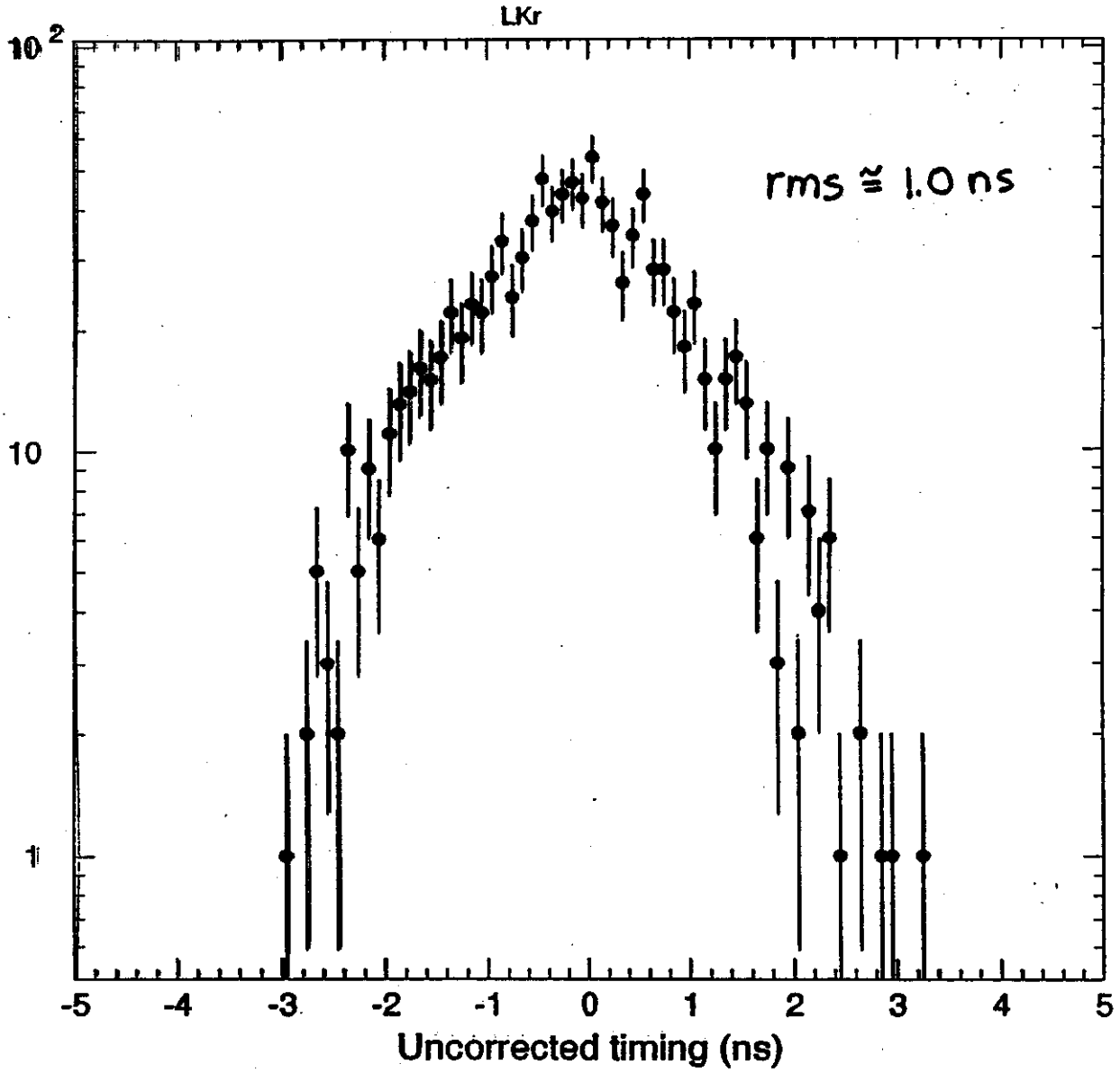
LKr, 2mm stack, 1.5kV

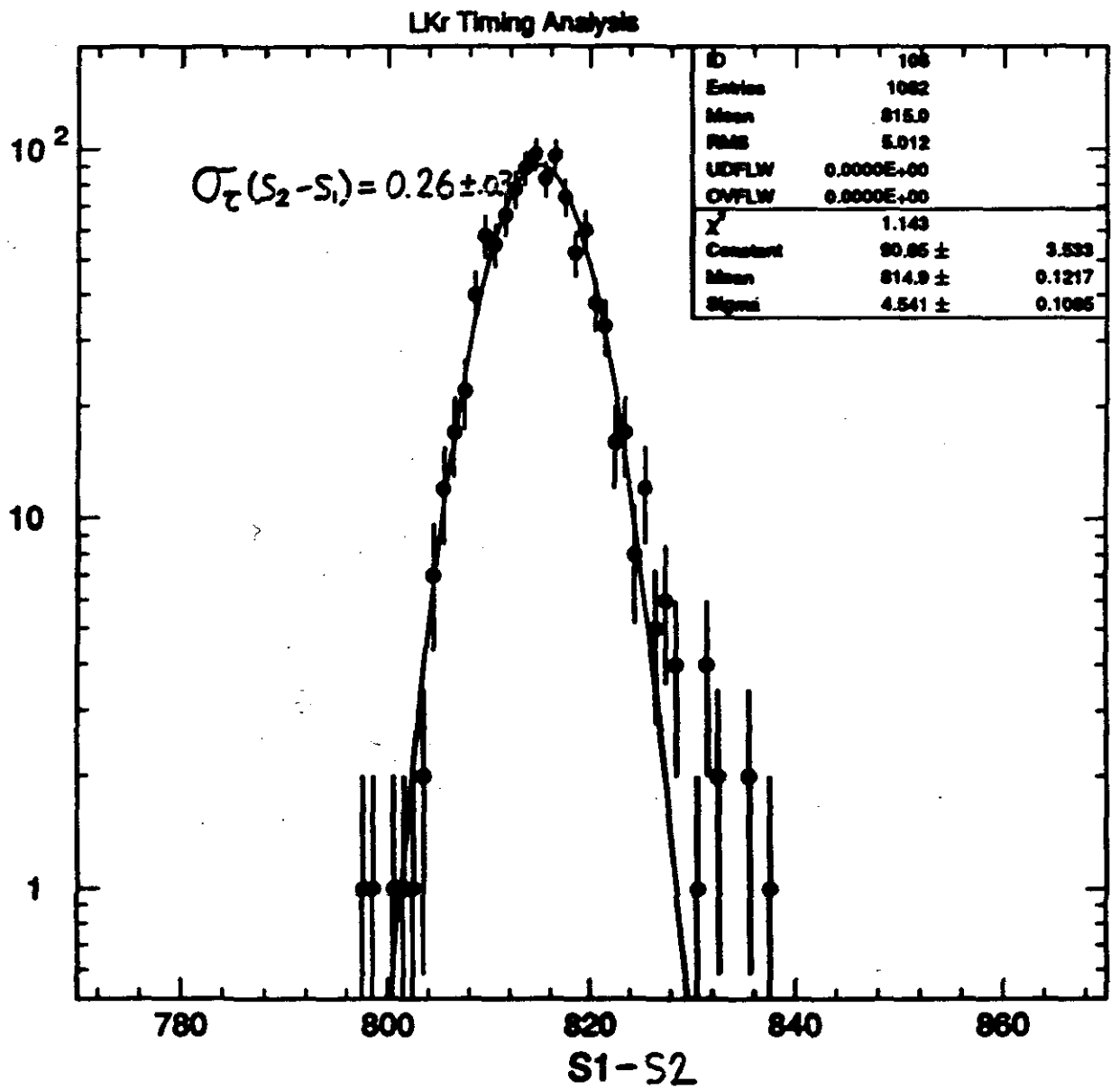
Beam Momentum = 20 GeV

Sum of approx. 150 channels



Multiple trace - variable persistence ! !


LKr
rms ≅ 1.0 ns
10^2
10
1
-5
-4
-3
-2
-1
0
1
2
3
4
5
Uncorrected timing (ns)


LKr Timing Analysis
ID 105
Entries 1082
Mean 815.0
RMS 5.012
UDFLW 0.0000E+00
OVFLW 0.0000E+00
χ² 1.143
Constant 90.85 ± 3.533
Mean 814.9 ± 0.1217
Sigma 4.541 ± 0.1085
$\sigma_\tau(S_2-S_1) = 0.26 \pm .03$
10²
10
1
780
800
820
840
860
S1-S2

"The Correction"

- it can be shown that for $F(t) = \sum a_i f(t - t_i)$ a timing shift $\delta = \frac{\sum a_i t_i}{\sum a_i}$ will be introduced.

- Therefore t_i can be found offline by minimizing

$$\sum_{j=1}^{\text{events}} \epsilon_j^2 = \sum (t_j^0 - \sum \alpha_{ij} t_i)^2$$

t_j^0 measured time for event j

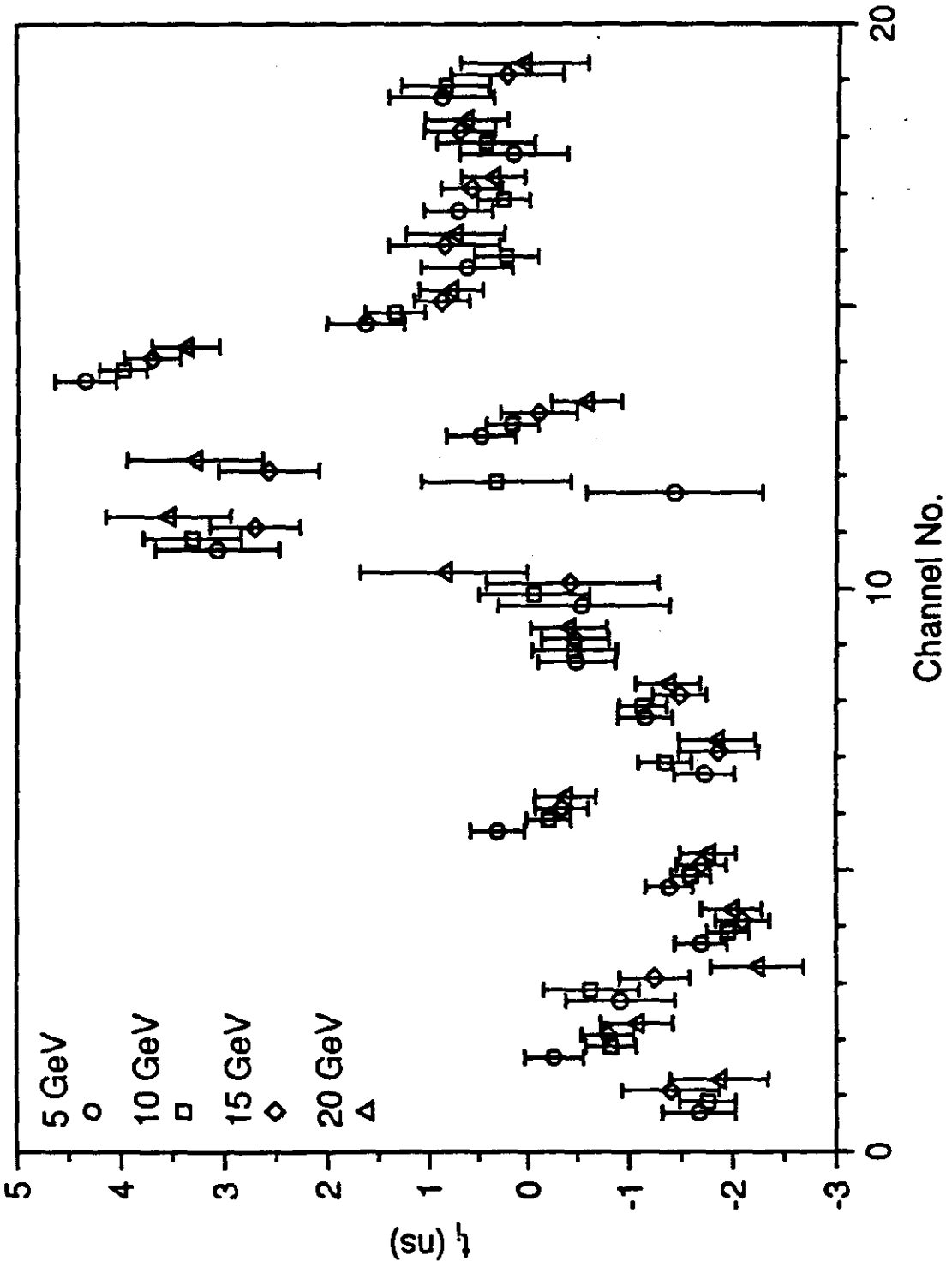
$\alpha_i = \frac{a_i}{\sum a_i}$, normalized p.h.

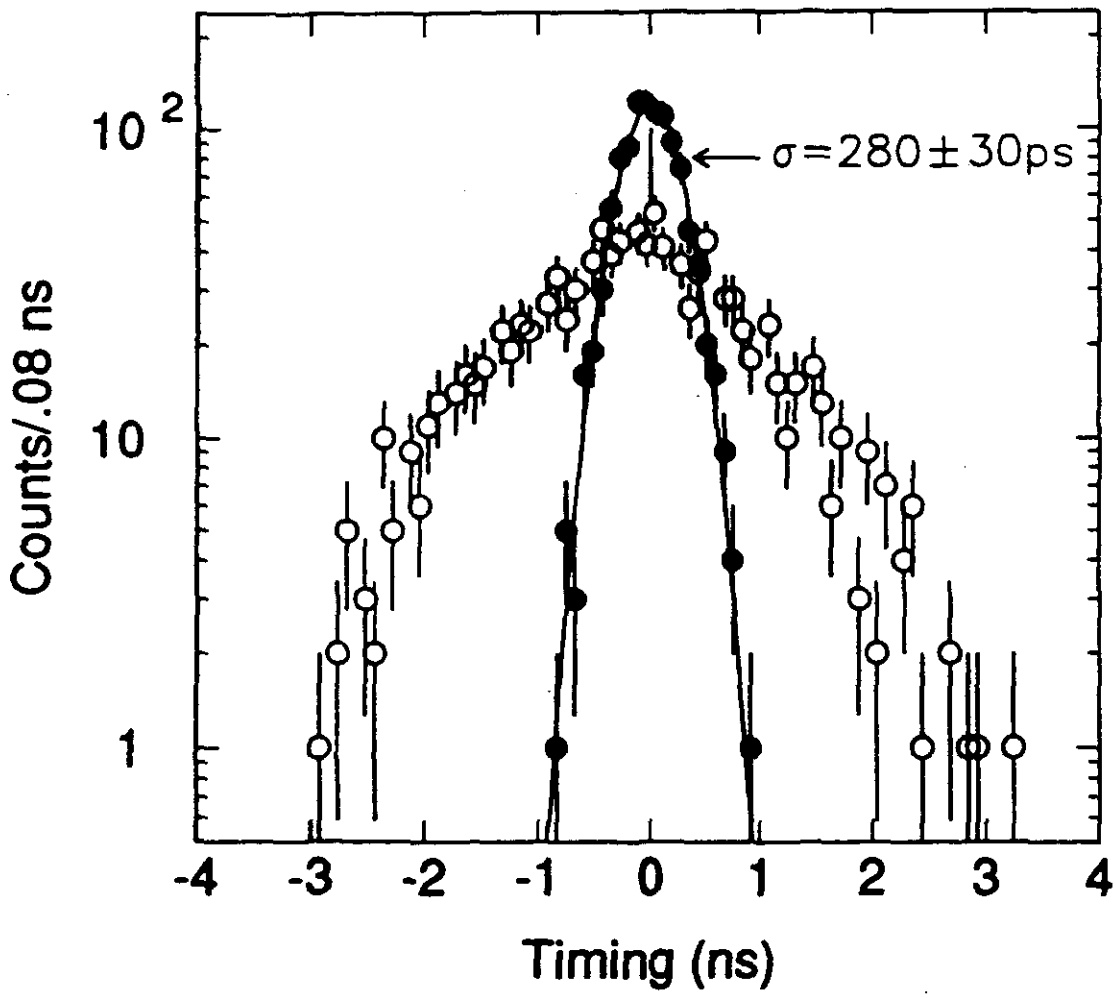
- This leads to:

$$\mathbb{A} - \mathbb{R}\mathbb{t} = 0$$

$$\mathbb{A} = \sum_{j=1} t_j^0 \alpha_{kj} \quad \text{and} \quad \mathbb{R}_{ki} = \sum_{j=1} (\alpha_{kj} \alpha_{ij})$$

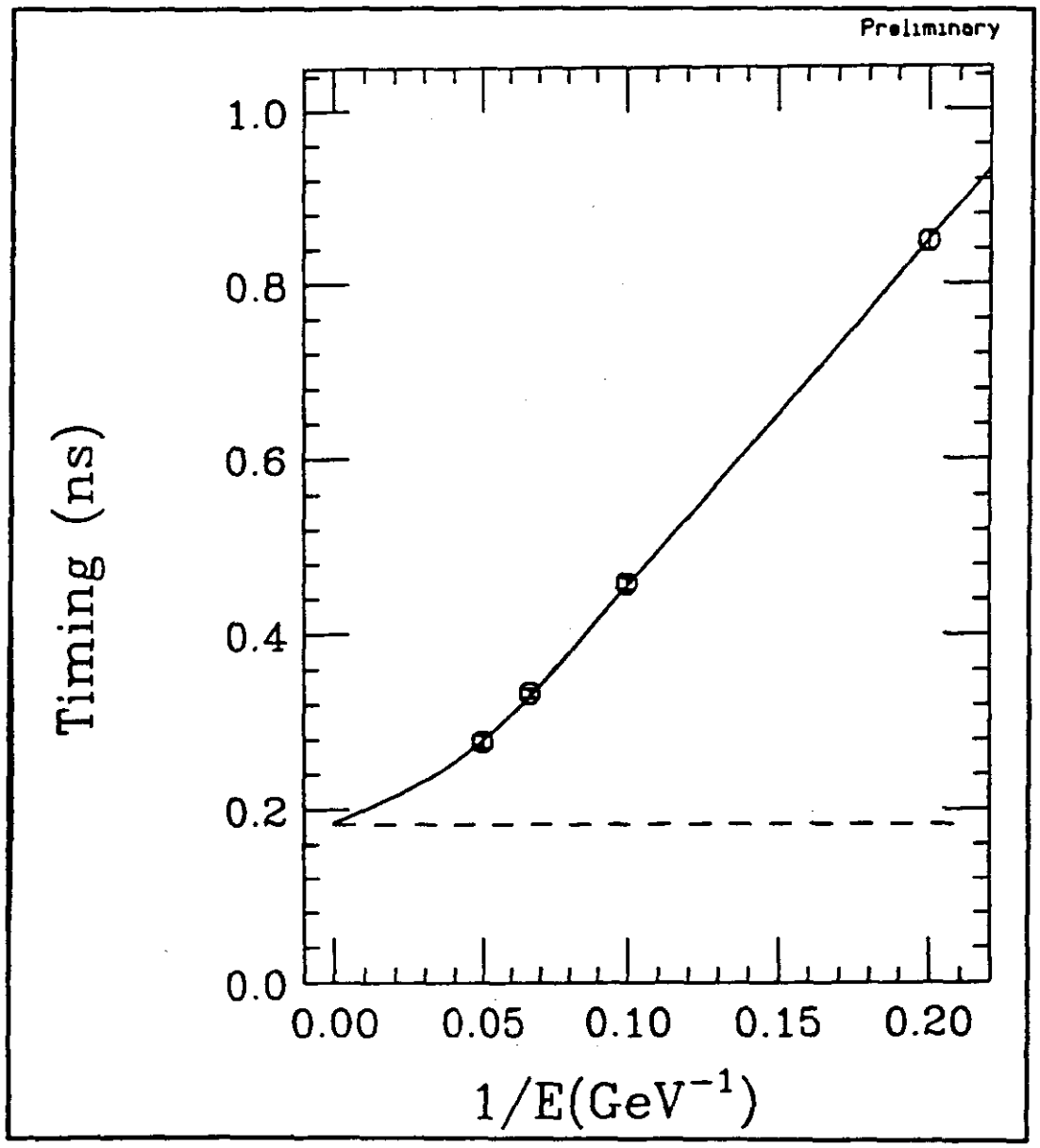
- apply this to all runs, limiting calorimeter to 3x3 tower geometry.


5 GeV
10 GeV
15 GeV
20 GeV
t (ns)
Channel No.
5
4
3
2
1
0
-1
-2
-3
0
10
20


σ=280±30ps
Counts/.08 ns
Timing (ns)
10 2
10
1
-4
-3
-2
-1
0
1
2
3
4

Timing

Energy Dependence



$$\delta t = (0.183 \pm .020)\ ns \oplus (4.16 \pm 0.06)\ GeV \cdot ns/E$$

$$\frac{\sigma_\tau(t_2 - t_1)}{\sqrt{2}} = (0.19 \pm 0.02) \qquad \sigma_\tau = \frac{\sigma_E}{E} \cdot \frac{1}{\frac{d}{dt}(g(t) - f(t))\Big|_{t=t_0}} = 4.5$$

Conclusions

- Liquid Ionization Calorimeters have excellent timing properties.
- Energy dependence is calculable
- the inherent timing resolution of one tower $\longrightarrow$ $0.8 \frac{\text{GeV.ns}}{E}$

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γeμ

Presentation by:

Paul O'Connor

Paul O'Connor

Muon Front End

Electronics Meeting

Front End ICs for Readout of Cathode Pad/Strip Chambers

P. O'Connor, BNL Instrumentation Division

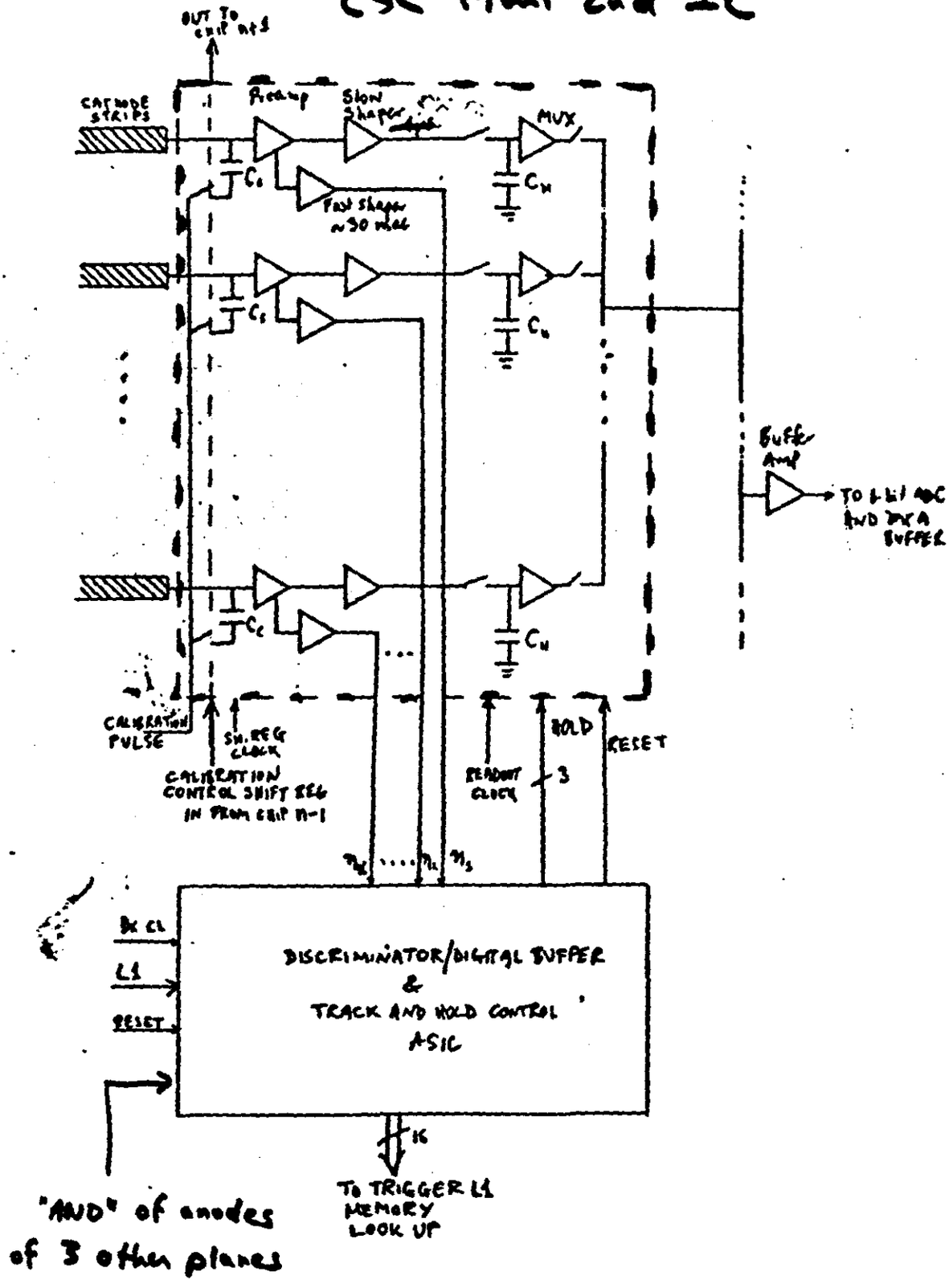
OUTLINE

- Performance Specifications
- Readout Function Blocks
- Circuit Design and Technology Choices
- BNL Test Chips & Results
- Plans for Future Work

Specifications: IPC Central Tracker

- Pad Capacitance: 10-50 pF
- Most probable Q_{strip}: ~30 fC
- Max. occupancy time: (2 - 4) x 16 nsec
- Desired position interpolation accuracy: 1% of pad pitch
- Desired time tagging: within 10 nsec from time of avalanche

CSC Front End IC



Specifications: CSC Front End IC

Strip Capacitance: 8-120 pF

Most probable Q_{strip}: ~30 fC

Hit rate per strip: ~ 100 Hz (tracks), 50 Hz - 50 kHz (neutrons)

Desired position interpolation accuracy: 1% of strip pitch

Desired time tagging: within 10 nsec from time of avalanche

Noise

For $\sigma_x / x = .01$, need $\sigma_Q/Q = .006$

$\sigma_Q = (.006)\ (30\ fC) = 0.17\ fC = 1100\ e^-$

For 1000 e^-, $C_D = 40$ pF, $C_{FET} + C_{stray} = 15$ pF, $t_m = 25$ ns ($CR\text{-}RC^4$)

$e_n < 0.46\ nV/\sqrt{Hz}$

($R_{eq} < 15\ \Omega$)

Input device $g_m > 52$ ms (FET), 39 mS (BJT)

$I_C > 1.0$ mA (BJT) ... but need to consider parallel noise of ~ 10 uA I_B

Id x W/L > 27A (I) for MOSFET in strong inversion

PLUS

30% - 50% from preamp other devices

noise of Rg, Rsub

2nd stage noise

CSC:

$C_D = 120$ pF

$t_m = 500$ ns

$\rightarrow e_n < 0.87\ nV/\sqrt{Hz}$ (48 Ω)

$g_m = 35$ mS (FET)

$I_d \cdot W/L = 12$ A

Noise

For $\sigma_x / x = .01$, need $\sigma_Q/Q = .006$

$\sigma_Q = (.006)\ (30\ fC) = 0.17\ fC = 1100\ e^-$

For 1000 e^-, $C_D = 40$ pF, $C_{FET} + C_{stray} = 15$ pF, $t_m = 25$ ns ($CR\text{-}RC^4$)

$\boxed{e_n < 0.46\ nV/\sqrt{Hz}}$

($R_{eq} < 15\ \Omega$)

Input device $g_m > 52$ ms (FET), 39 mS (BJT)

$I_C > 1.0$ mA (BJT) ... but need to consider parallel noise of ~ 10 uA I_B

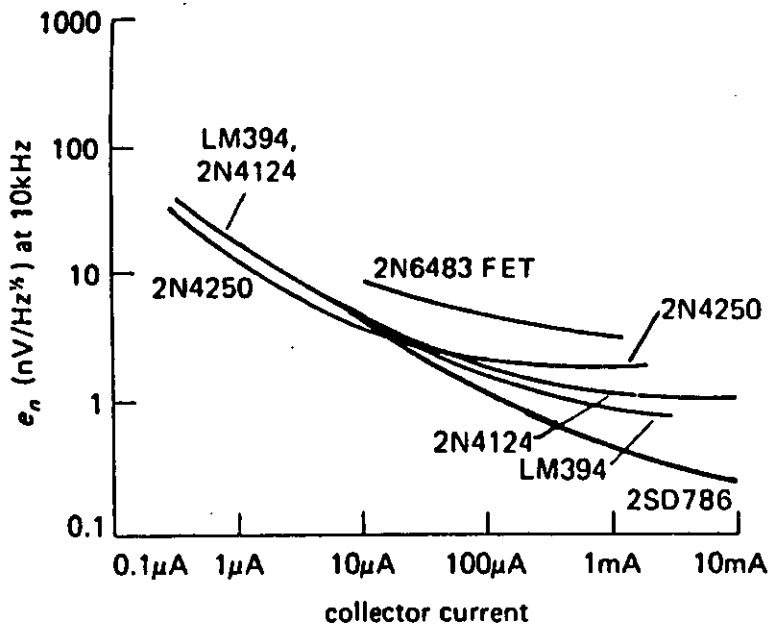
Id x W/L > 27A (!) for MOSFET in strong inversion

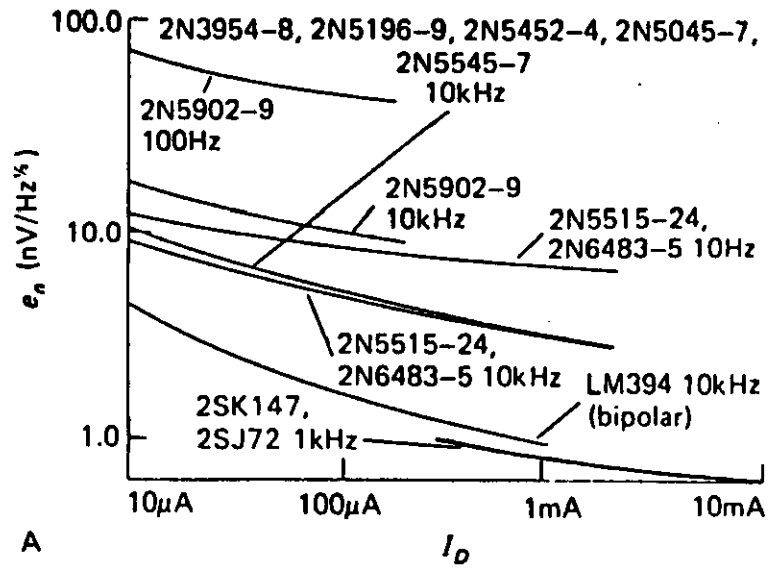
PLUS

30% - 50% from preamp other devices

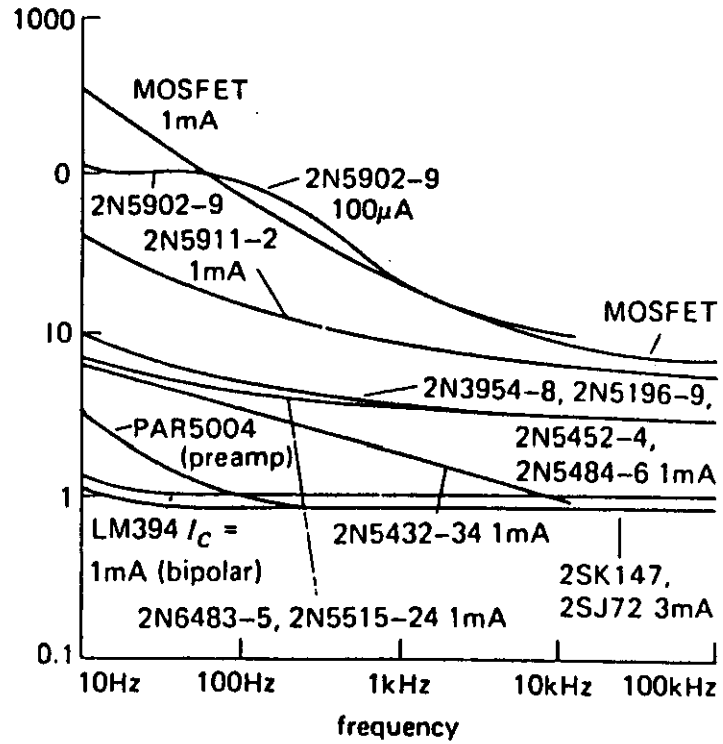
noise of Rg, Rsub

2nd stage noise


1000
100
10
1
0.1
e_n (nV/Hz$^{1/2}$) at 10kHz
LM394,
2N4124
2N4250
2N6483 FET
2N4250
2N4124
LM394
2SD786
0.1μA
1μA
10μA
100μA
1mA
10mA
collector current


100.0
10.0
1.0
e_n (nV/Hz$^{1/2}$)
2N3954–8, 2N5196–9, 2N5452–4, 2N5045–7,
2N5545–7
10kHz
2N5902–9
100Hz
2N5902–9
10kHz
2N5515–24,
2N6483–5 10Hz
2N5515–24,
2N6483–5 10kHz
LM394 10kHz
(bipolar)
2SK147,
2SJ72 1kHz
10μA
100μA
1mA
10mA
I_D

A


1000
0
10
1
0.1
MOSFET
1mA
2N5902–9
100μA
2N5902–9
2N5911–2
1mA
MOSFET
2N3954–8, 2N5196–9,
PAR5004
(preamp)
2N5452–4,
2N5484–6 1mA
LM394 I_C =
1mA (bipolar)
2N5432–34 1mA
2SK147,
2SJ72 3mA
2N6483–5, 2N5515–24 1mA
10Hz
100Hz
1kHz
10kHz
100kHz
frequency

Charge Sensitive Preamp - Input Device Technology Choice

Equivalent input noise charge:

$$ENC^2 = a_1 \frac{C_T^2 e_n^2}{\tau_m} + a_2 i_n^2 \tau_m \qquad \text{(EQ 1)}$$

for BJT,

$$e_n^2 = 4kT\left(\frac{1}{2g_m} + R_{bb'}\right) \qquad \text{(EQ 2)}$$

$$i_n^2 = 2qI_B + 4kT\left(\frac{1}{R_F} + \frac{1}{R_{bias}}\right) \qquad \text{(EQ 3)}$$

for MOS,

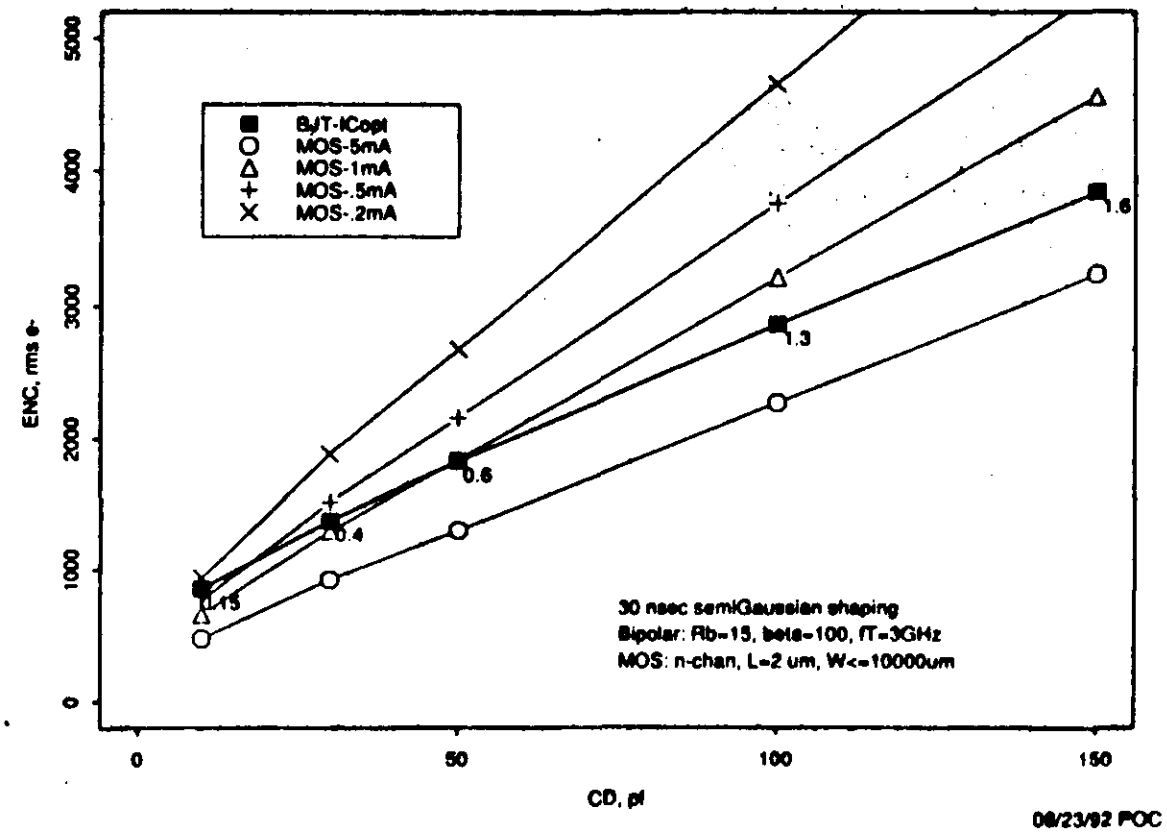
$$e_n^2 = 4kT\left(\frac{2\Gamma}{3g_m} + R_g\right) + a_3 \tau_m \frac{K_f}{C_{ox}^2 WL} \qquad \text{(EQ 4)}$$

$$i_n = 4kT\left(\frac{1}{R_f}\right) \qquad \text{(EQ 5)}$$

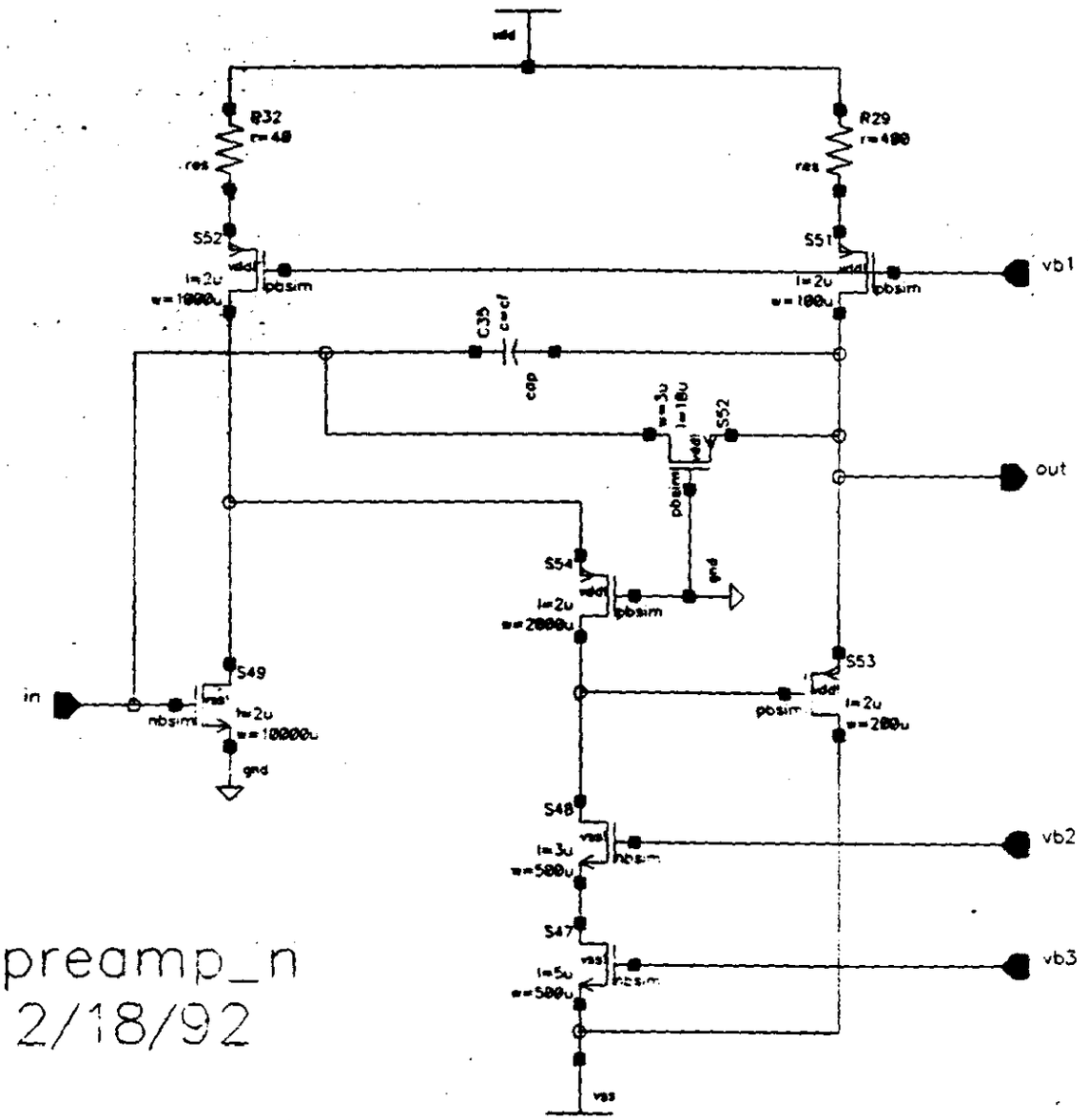
Conclusions (short τ_m):

For BJT, achievable ENC is limited by $R_{bb'}$, β, and f_T. For MOS in strong inversion, ENC is constrained by power and area allocated to the input device. In practice secondary effects like excess noise sources, ease of integration, and accuracy of modeling large input device must be carefully considered.

Comparison of BJT and MOS noise



IPC Front End Electronics



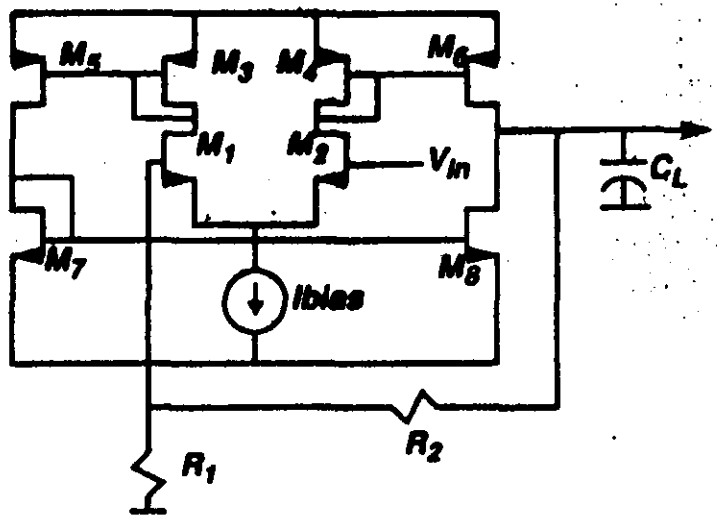
preamp_n
2/18/92

PO'C 2/28/92
test
1/1

Shaper Design

- Noise (power and area tradeoff)
- Peaking time control
- Dynamic range
- DC and AC stability

CMOS Lowpass Section for Semigaussian Shaper



$\tau_0 \approx 2g_{m3}/C_i \sim (\text{ibias})^{1/2}$

$$Q^2 \approx \frac{C_i}{g_{m3}}\frac{\beta_5}{\beta_3}\frac{g_{m1}R_1}{(R_1+R_2)C_L} = \sqrt{\frac{\beta_1}{\beta_3}}\frac{\beta_5}{\beta_3}\frac{C_i}{C_L}\frac{R_1}{(R_1+R_2)} \rightarrow$$

- peaking time depends only on (ibias)
- shape of pulse is determined by component ratios, independent of (ibias).

1991-2 Prototyping Activity

- **9 MOSIS Tiny Chips submitted**
- **All 2um CMOS / BICMOS process (Orbit Semi.)**
- **Investigated:**

10000/2 NMOS, PMOS test transistors

Preamps:

Charge sensitive folded cascode (NMOS, PMOS input device)

45 kOhm transimpedance (NMOS, bipolar npn input device)

Shapers:

20, 40 -100, 500 -1000 nsec unipolar CR-$(RC)^4$

Output Drivers: source followers

Preamp-shaper, preamp-shaper-track/hold with output drivers

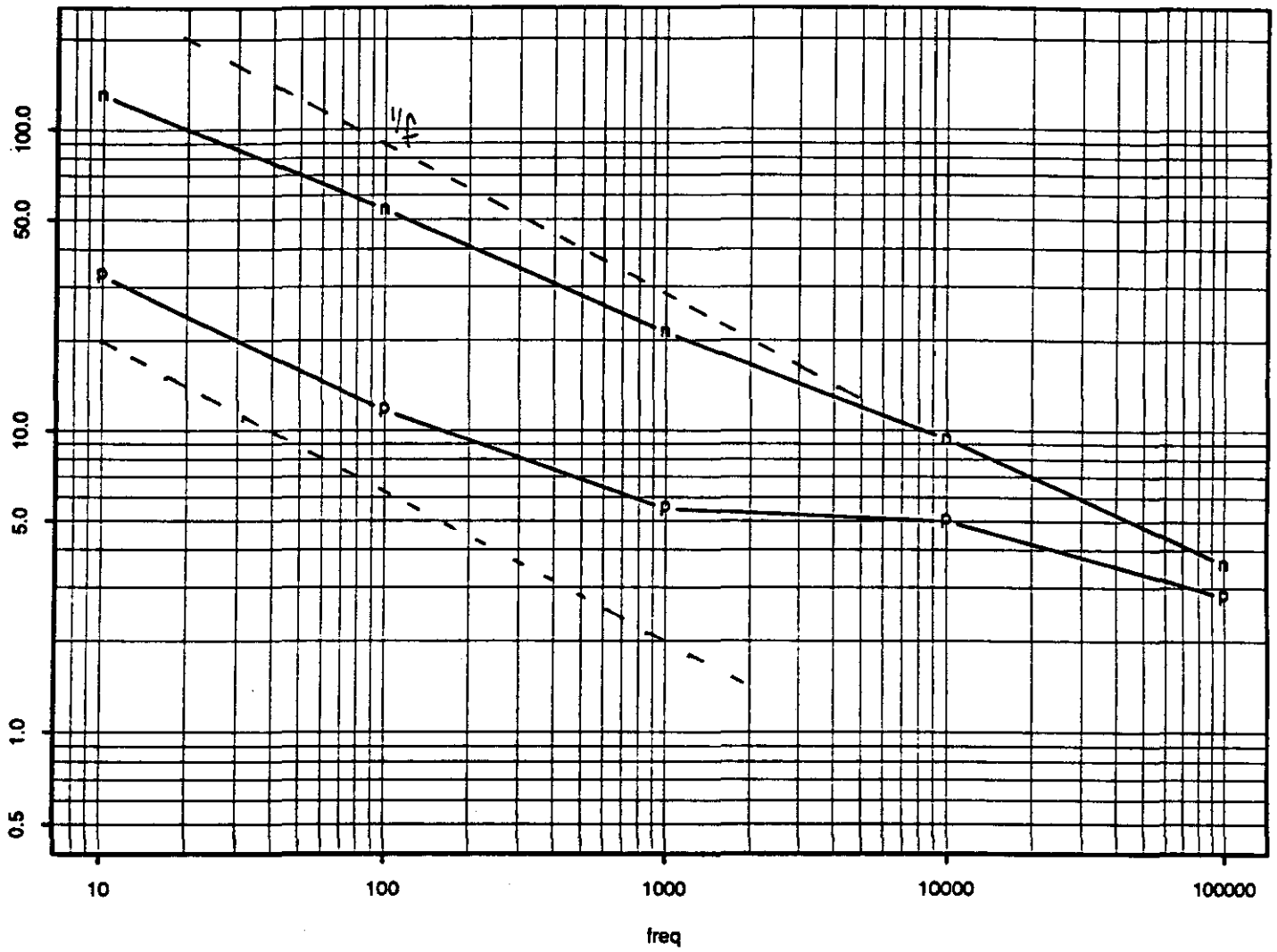
- RAD-HARD run (HARRIS AVLSIRA 1.2 μm) to start 1/93

Tests

- **Components**
  - R, C, MOS, BJT
    - I-V
    - noise vs. frequency, bias
    - ESD
    - radiation
- **Circuits**
  - Noise vs. tm, Cd, bias
  - Linearity, dynamic range
  - Peak time
  - frequency response
  - Loading effects
  - Crosstalk

10/30/92

IC5 MOSFET Noise vs. Frequency -- Id ~ 4mA



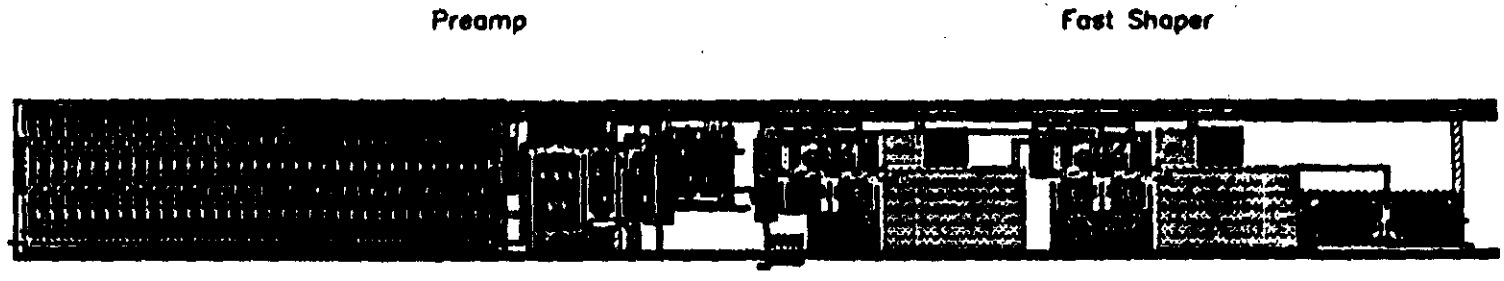
$g_m \sim 24mS$

$K_f \sim 5.1 \times 10^{-24}$ J nmo

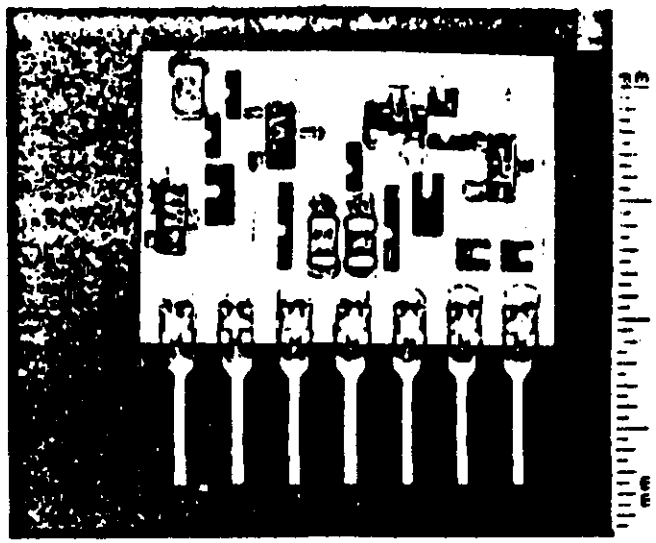
3.2×10^{-25} J pmo

8-channel 25 nsec preamp/shaper

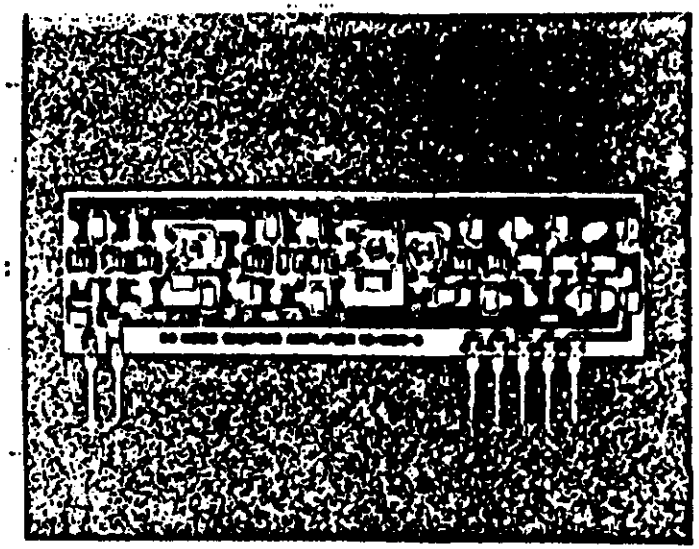
- Layout of one channel



Front End Section



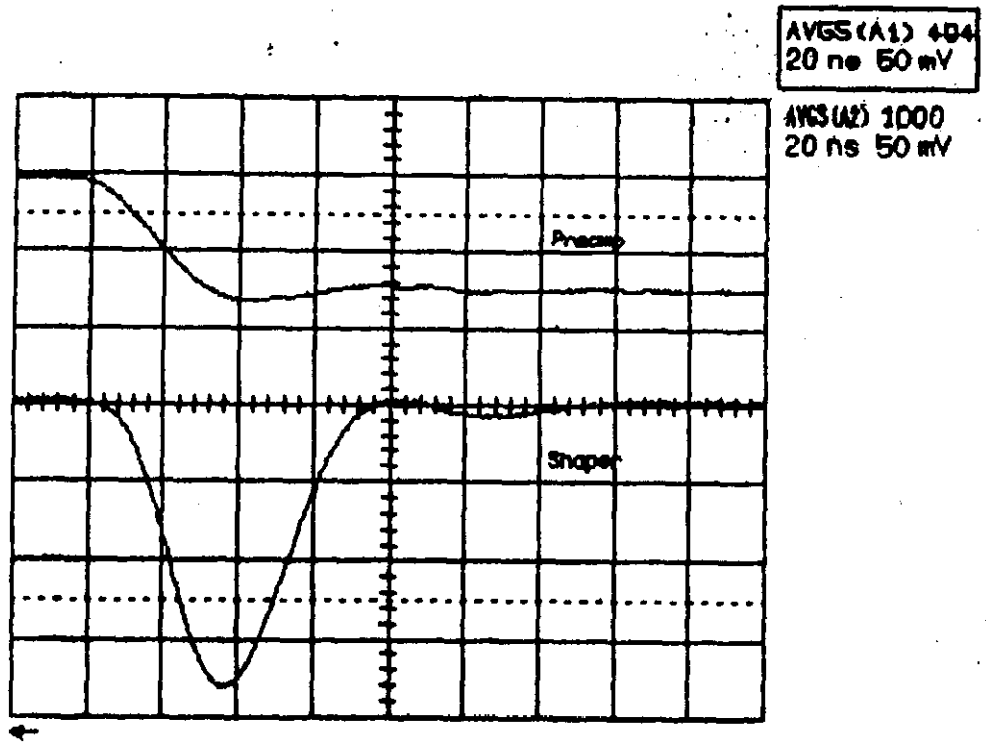
Hybrid Preamp
12.5 x 19 mm

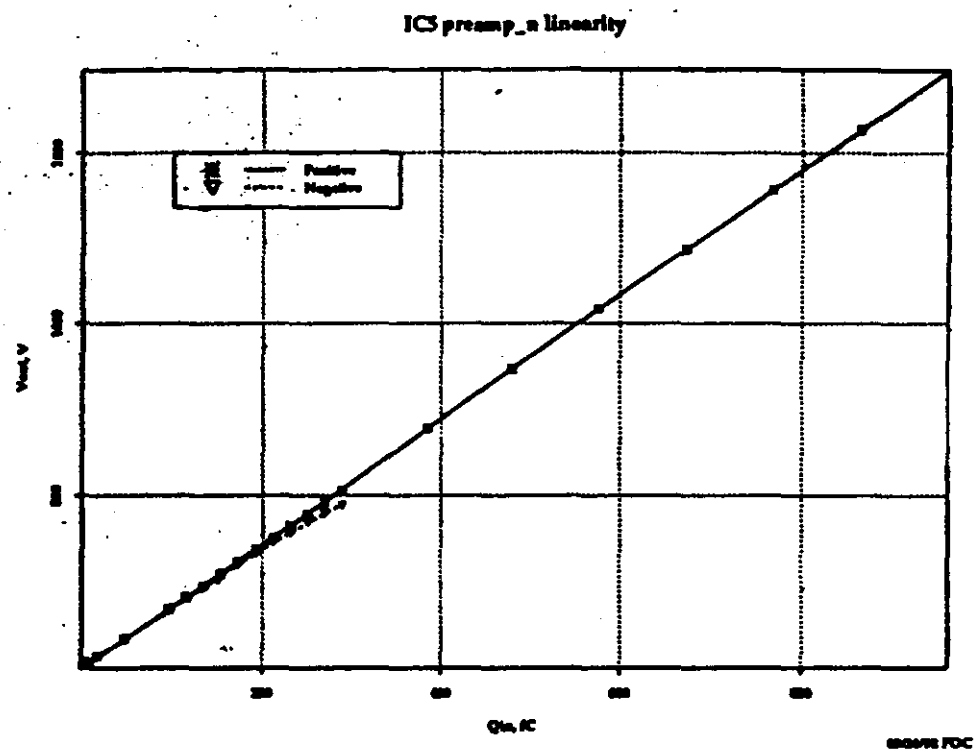


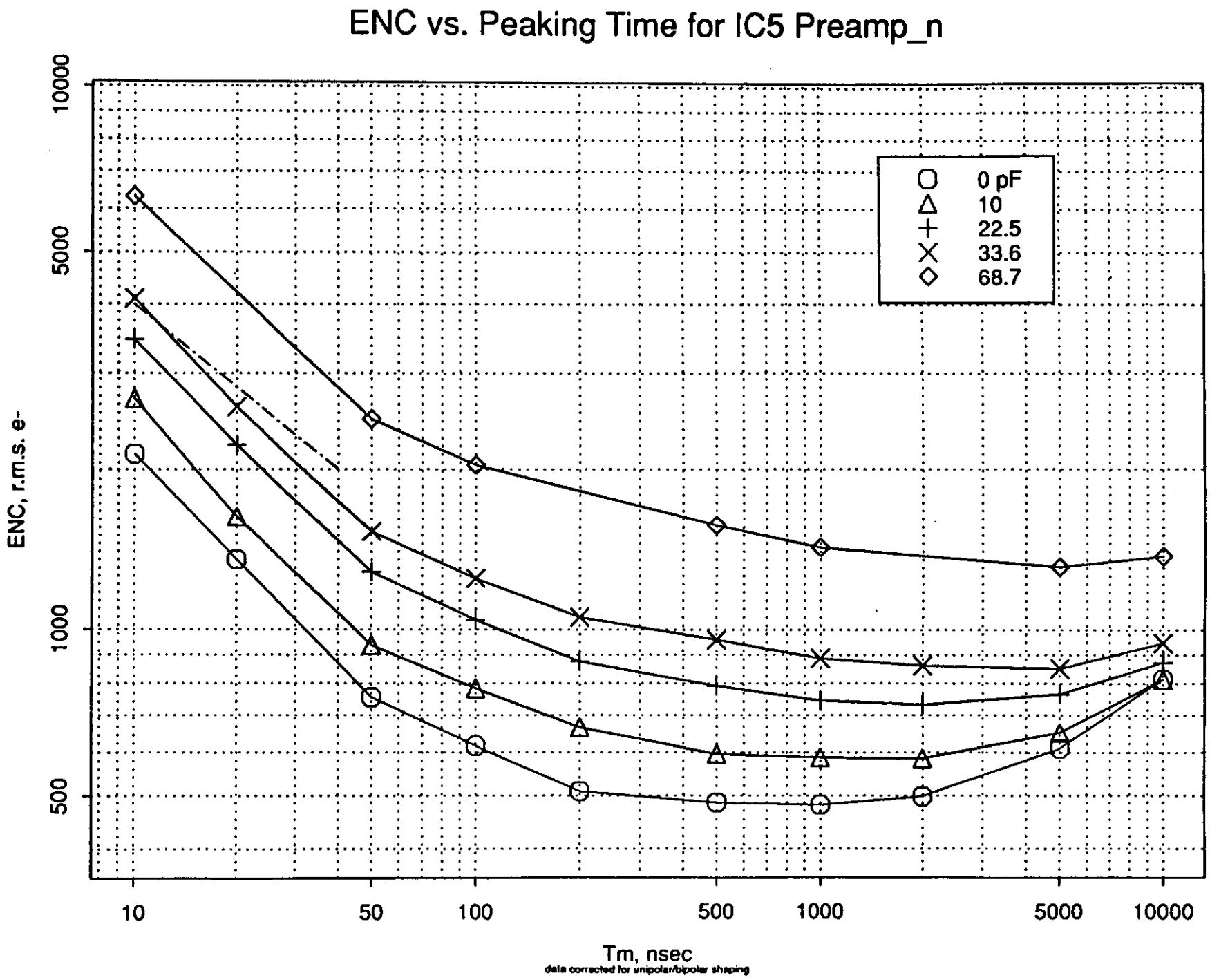
Hybrid Shaper
19 x 5.9 mm

Results of Preamp/Shaper Test Chips Designed at BNL

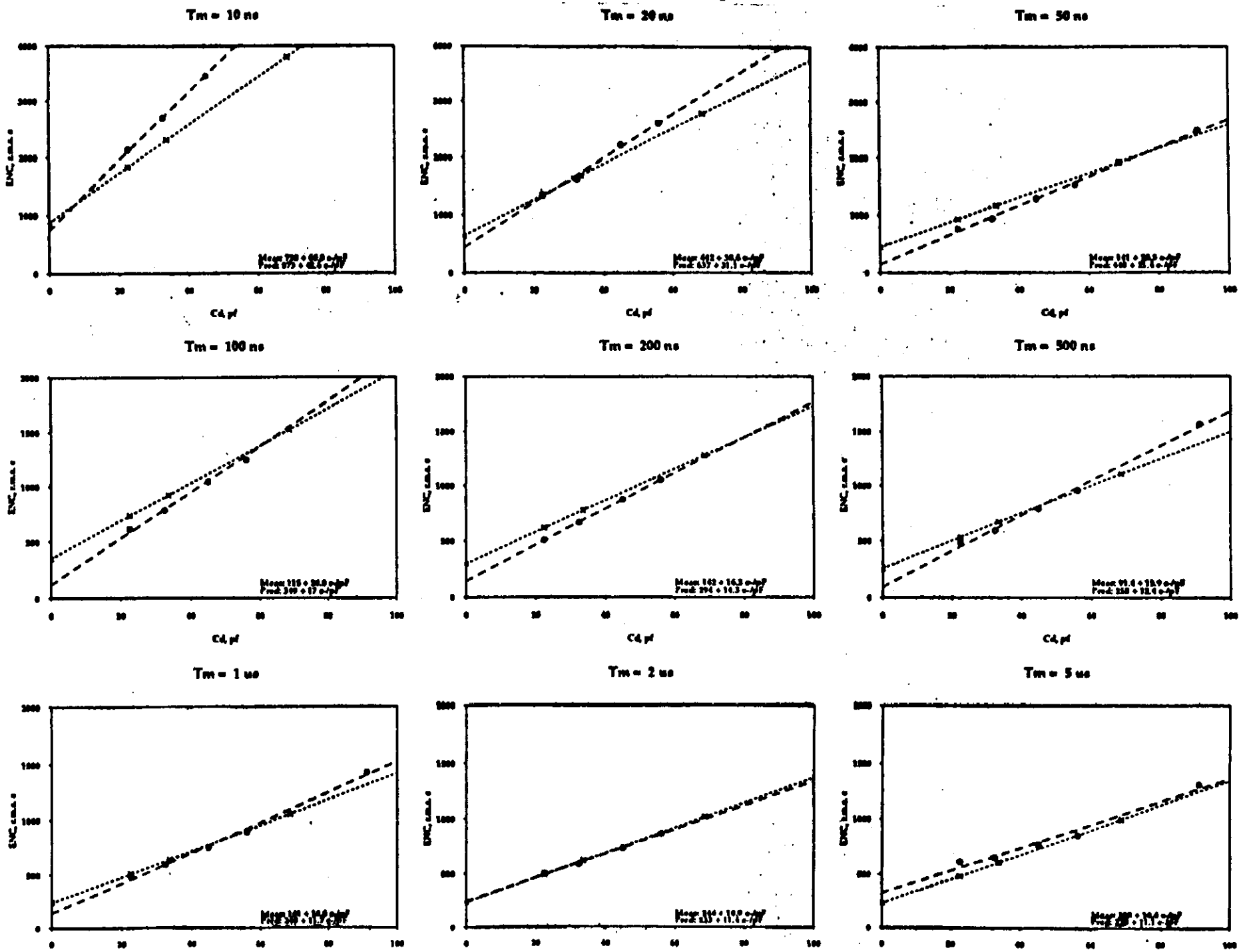
8 channel preamp/shaper




ICS preamp_a linearity
Positive
Negative
Vout, V
Qin, fC

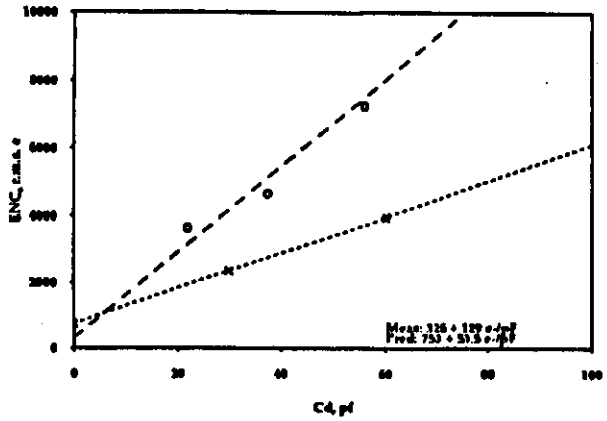

ENC vs. Peaking Time for IC5 Preamp_n
ENC, r.m.s. e-
10000
5000
1000
500
10
50
100
500
1000
5000
10000
Tm, nsec
data corrected for unipolar/bipolar shaping
0 pF
10
22.5
33.6
68.7

ENC vs. Cd for IC5 Preamp_n

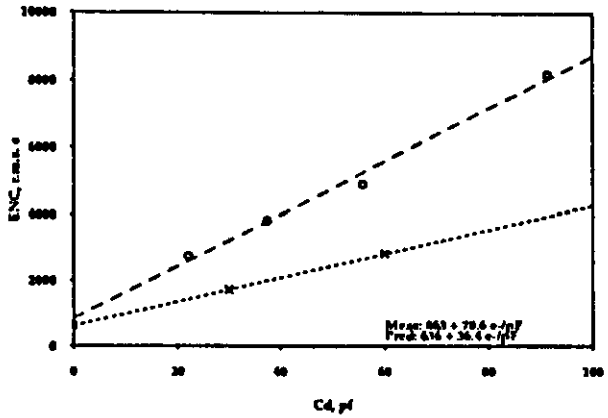


ENC vs. Cd for IC5 Preamp_p

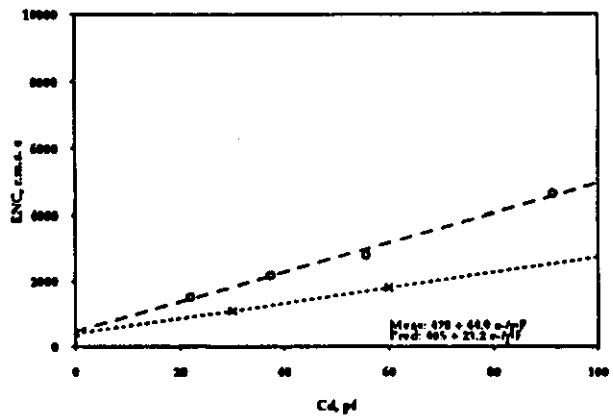
Tm = 10 ns



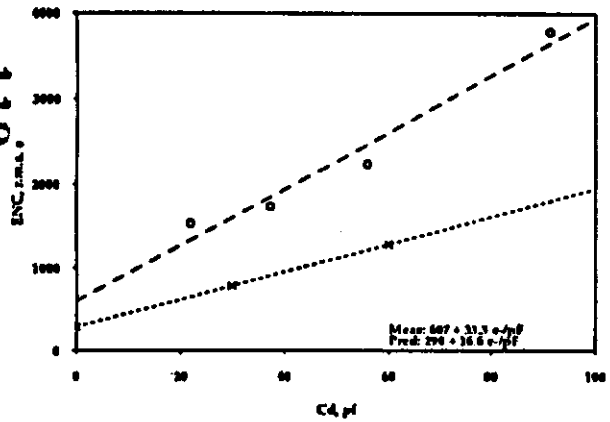
Tm = 20 ns



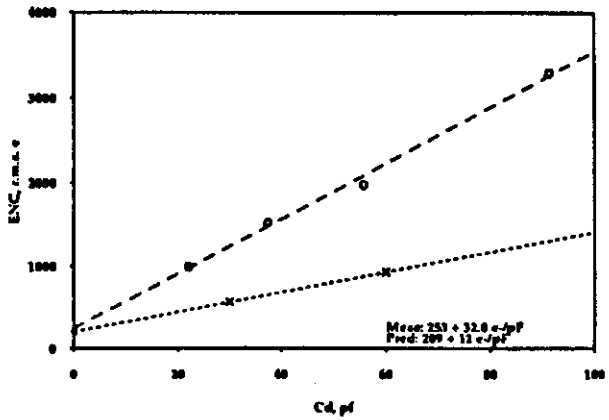
Tm = 50 ns



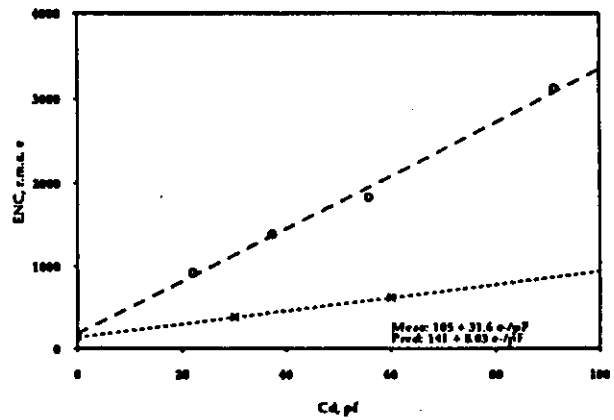
Tm = 100 ns



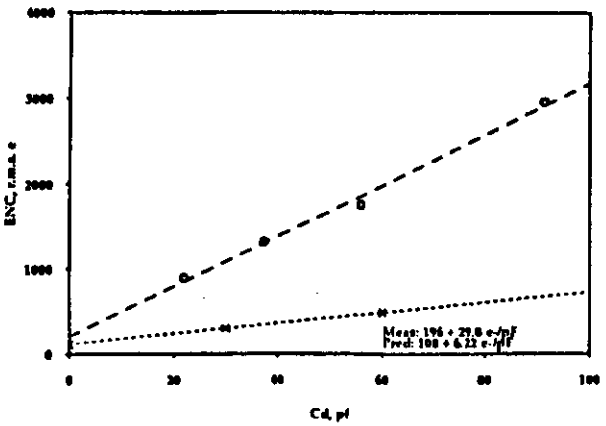
Tm = 200 ns



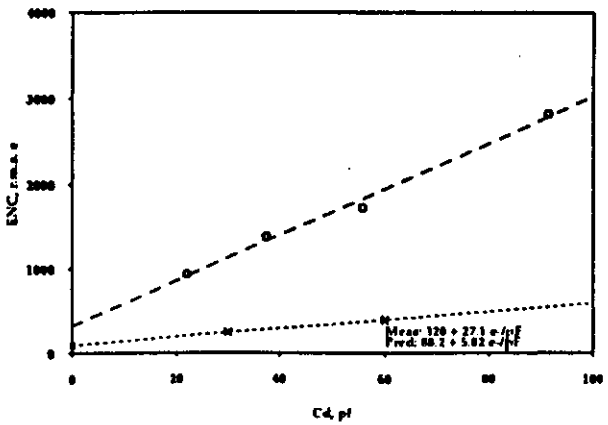
Tm = 500 ns



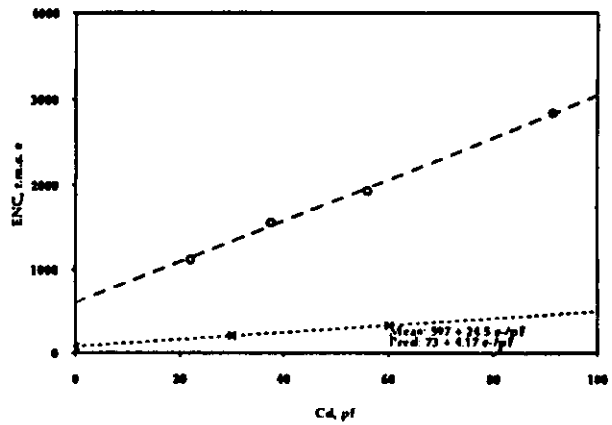
Tm = 1 us

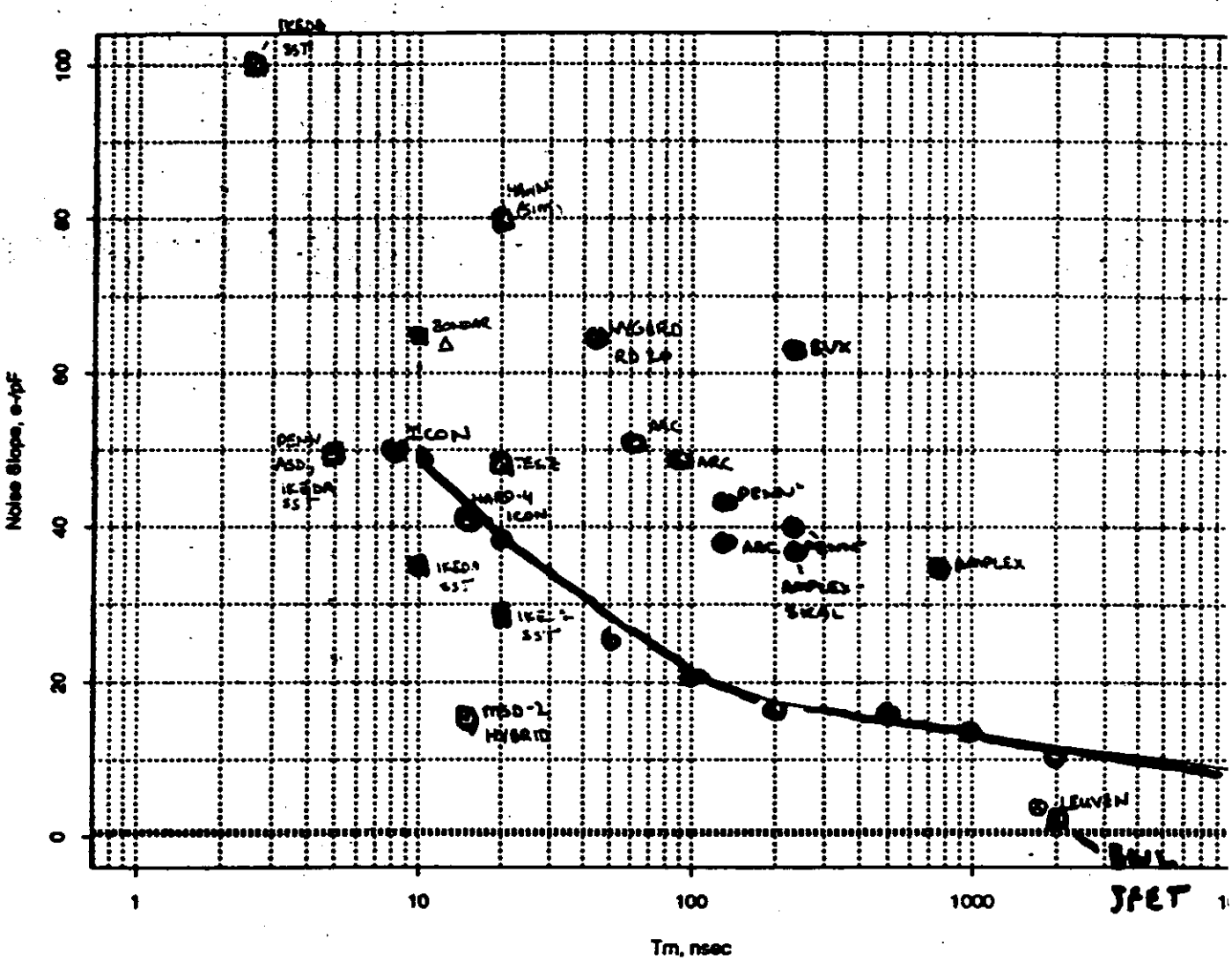


Tm = 2 us



Tm = 5 us

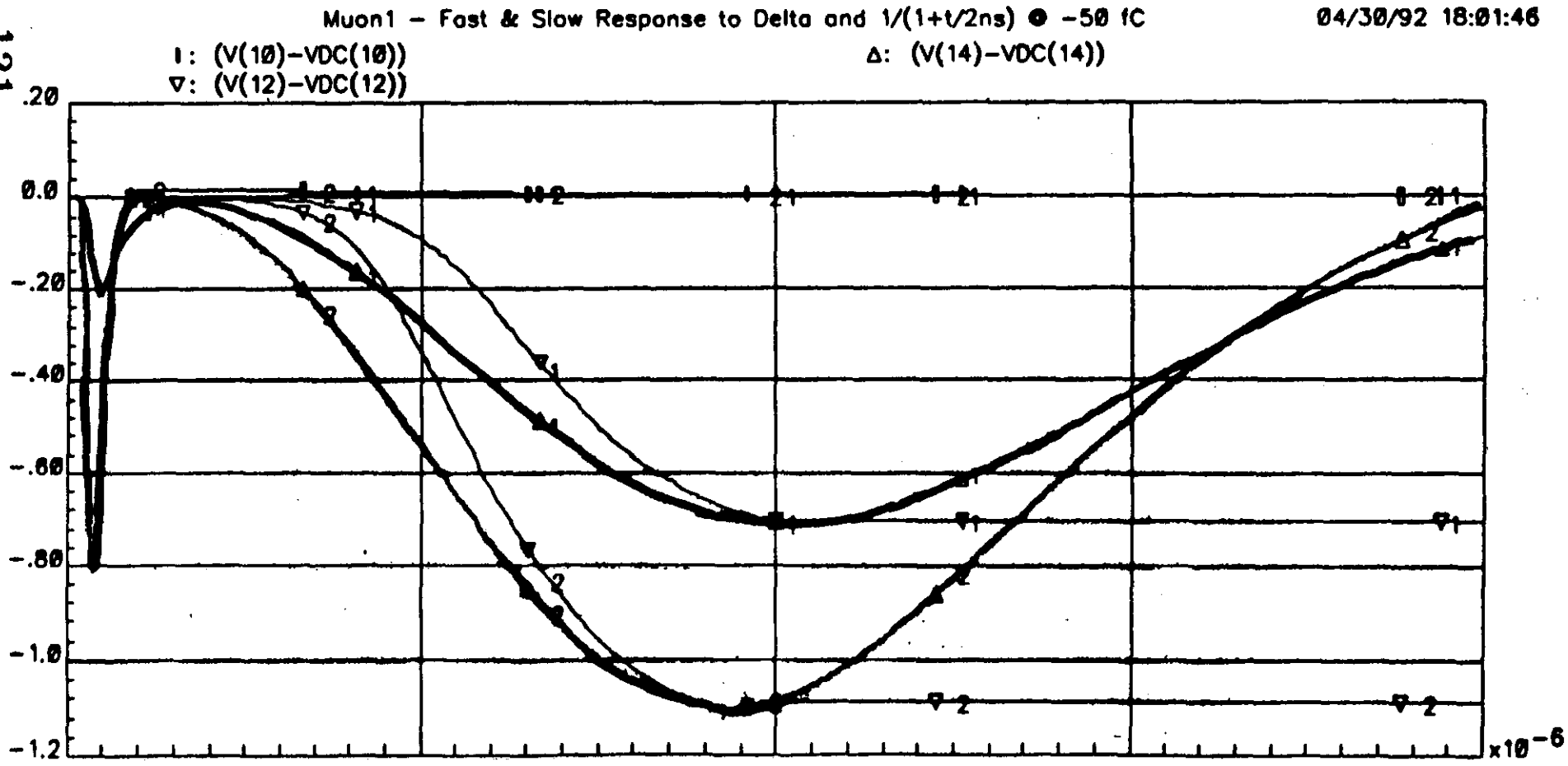


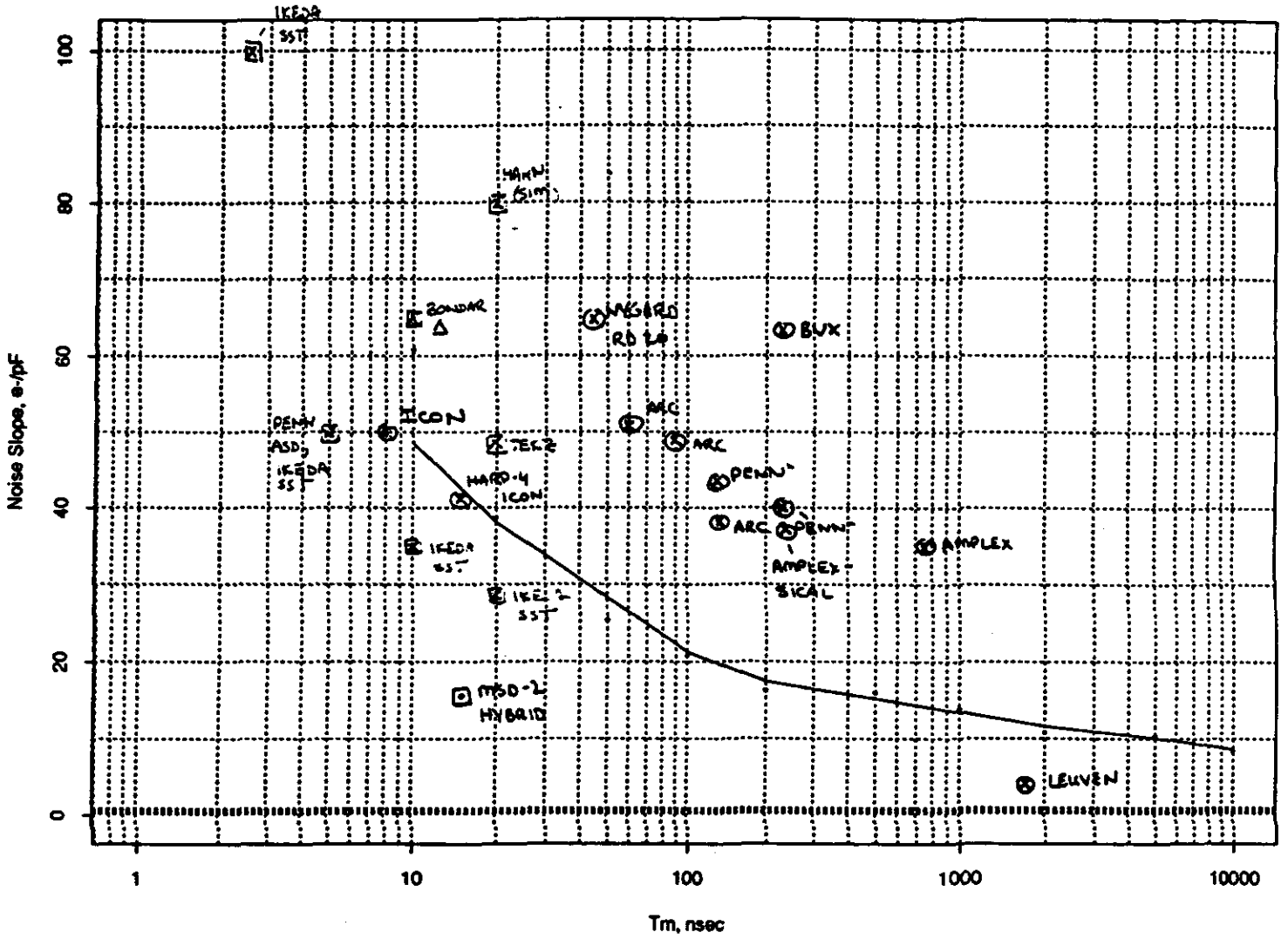


Hybrid

Bipolar IC

CMOS IC

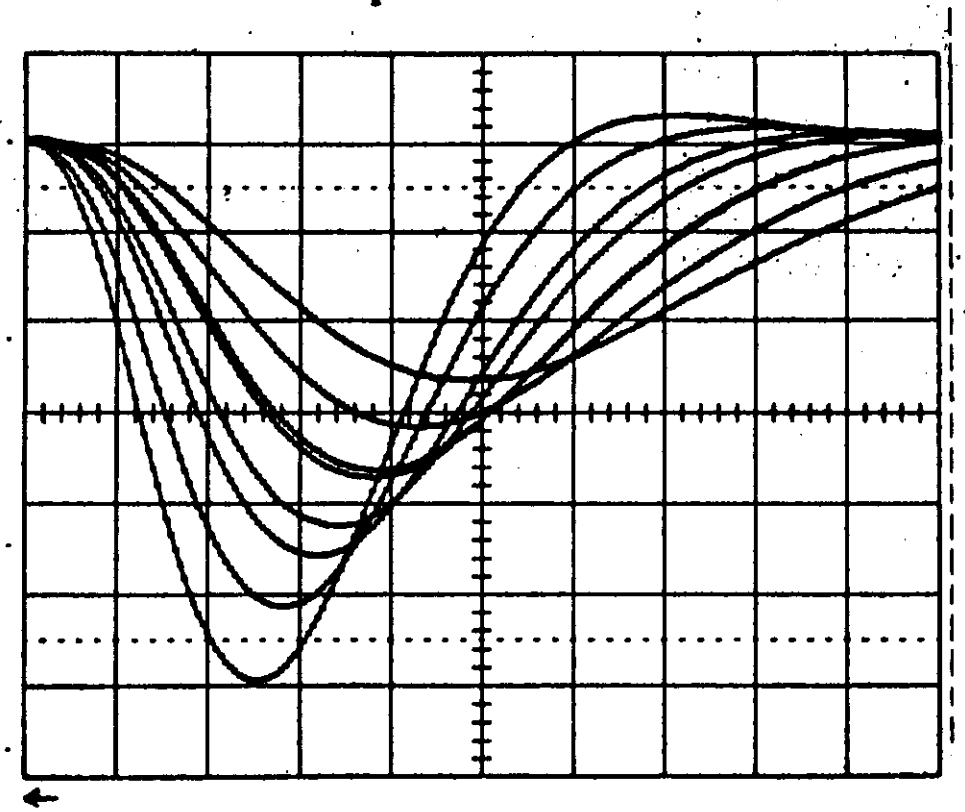

Muon1 – Fast & Slow Response to Delta and 1/(1+t/2ns) @ -50 fC
04/30/92 18:01:46
I: (V(10)-VDC(10))
▽: (V(12)-VDC(12))
Δ: (V(14)-VDC(14))
.20
0.0
-.20
-.40
-.60
-.80
-1.0
-1.2
x10^-6



Noise Slope, e-/pF
Tm, nsec
0
20
40
60
80
100
1
10
100
1000
10000
IKEDA SST
HAHN (SIM)
BONDAR
WEGARD RD 20
BUX
ICON
PENN ASD, IKEDA SST
TEKZ
ARC
ARC
PENN
HARP-4 ICON
ARC
PENN
AMPLEX
AMPLEX-SICAL
IKEDA SST
IKE 2 SST
MSD-2 HYBRID
LEUVEN

Results of Preamp/Shaper Test Chips Designed at BNL

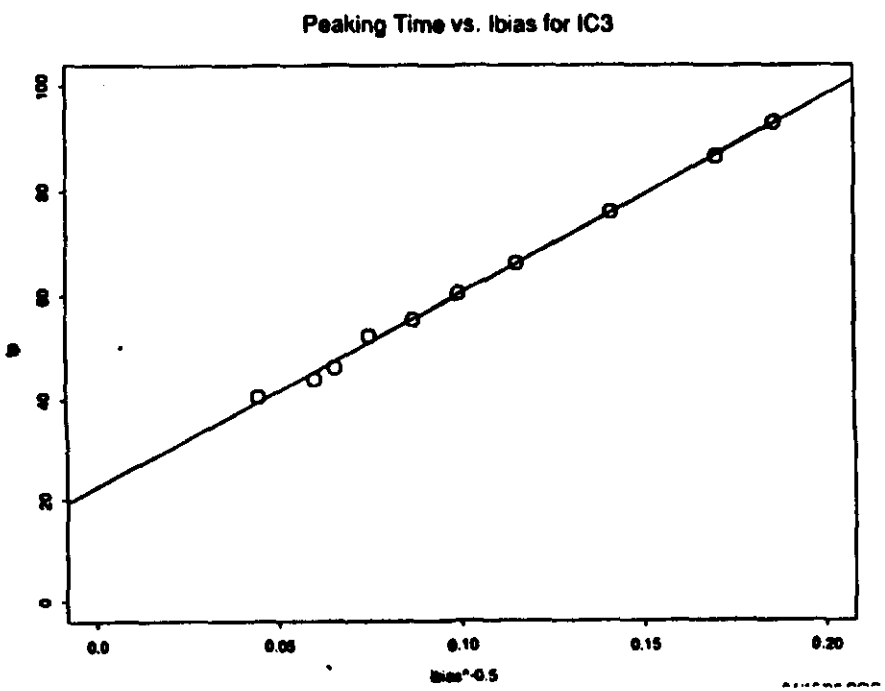
70 nsec variable CMOS shaper

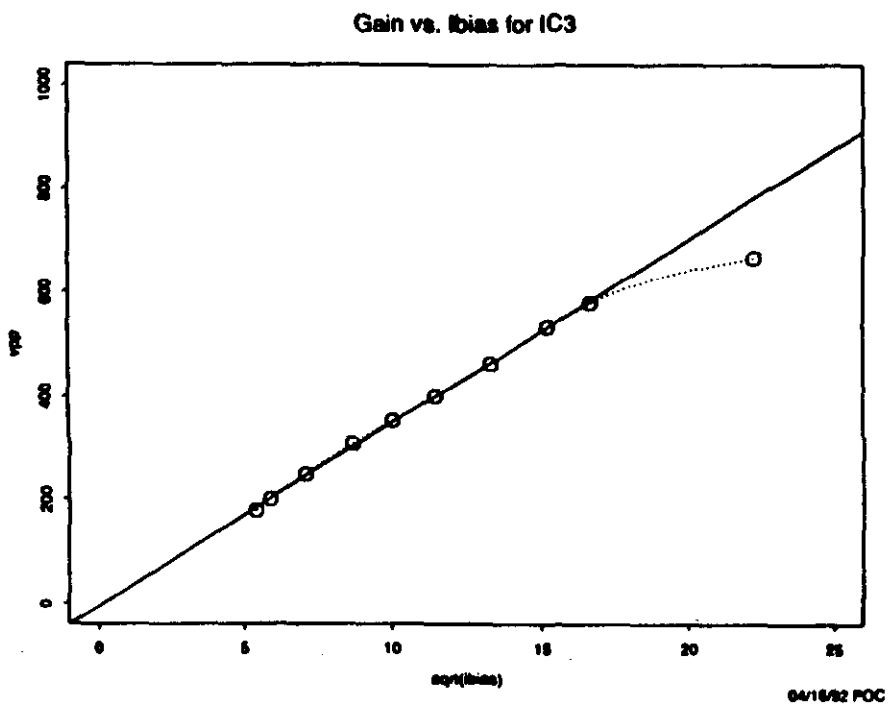


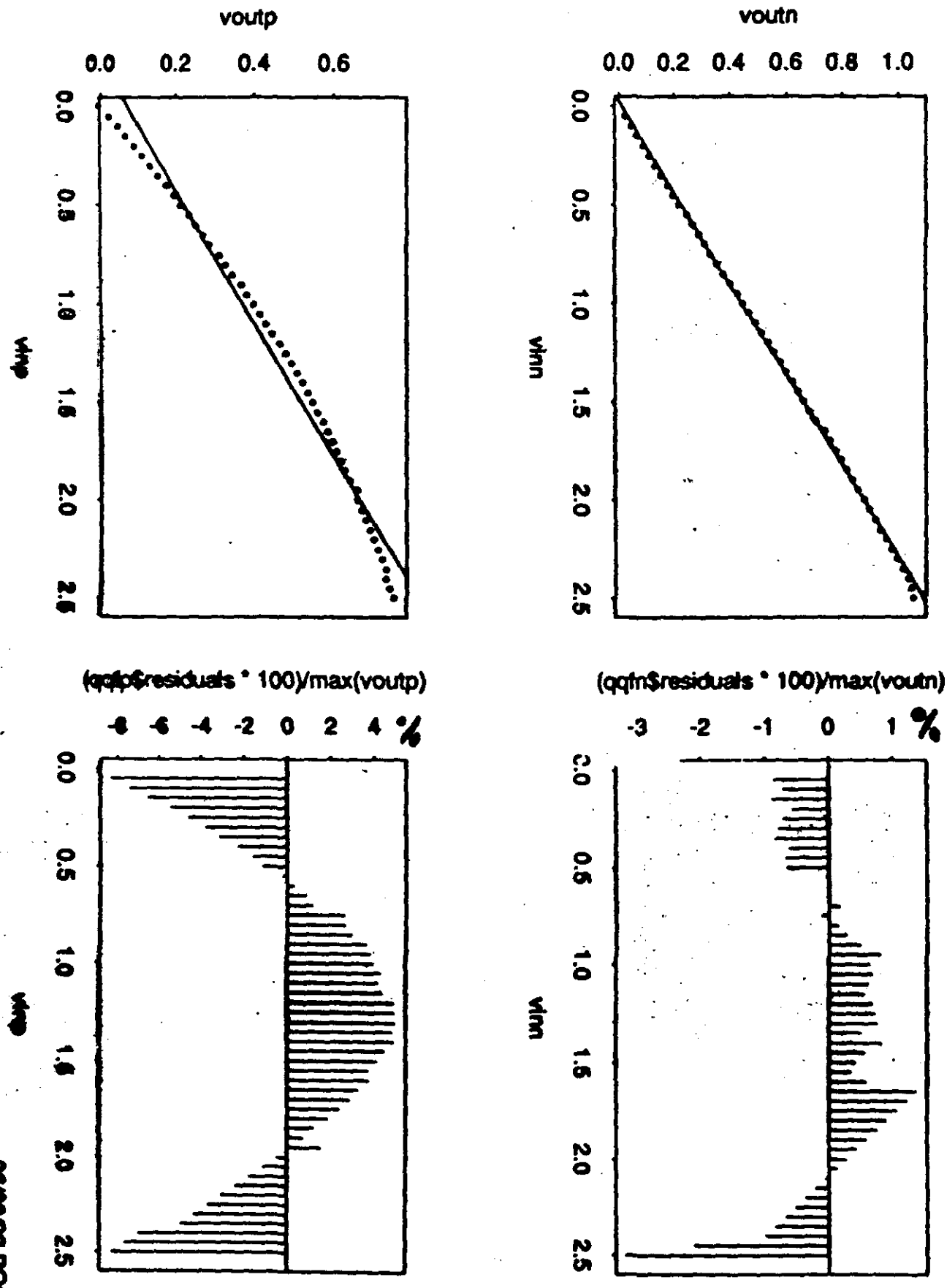
Horizontal: 20 nsec/div

Vertical: 50 mV/div

Results of Preamp/Shaper Test Chips Designed at BNL






voutp
0.0 0.2 0.4 0.6
vinp
0.0 0.5 1.0 1.5 2.0 2.5
voutn
0.0 0.2 0.4 0.6 0.8 1.0
vinn
0.0 0.5 1.0 1.5 2.0 2.5
(qqfp$residuals * 100)/max(voutp)
-6 -6 -4 -2 0 2 4 %
vinp
0.0 0.5 1.0 1.5 2.0 2.5
(qqfn$residuals * 100)/max(voutn)
-3 -2 -1 0 1 %
vinn
0.0 0.5 1.0 1.5 2.0 2.5

gem

γeμ

Presentation by:

D. Crosetto

CROSETTO

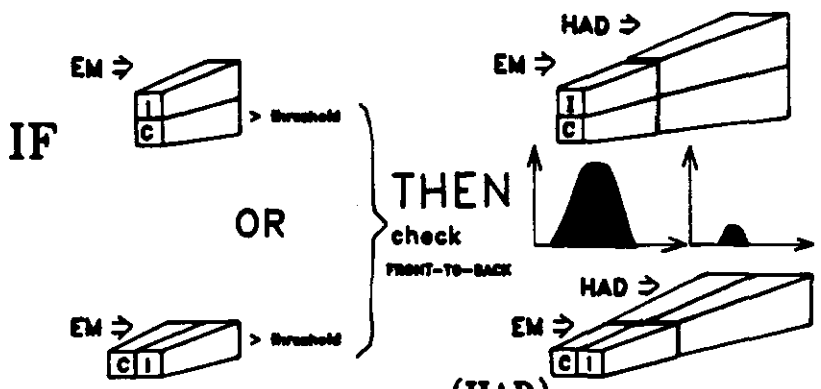
Algorithms examples

Local maximum

I	I	I
I	C	I
I	I	I

$C > I_i$ for $i = 1, \ldots, 8$.

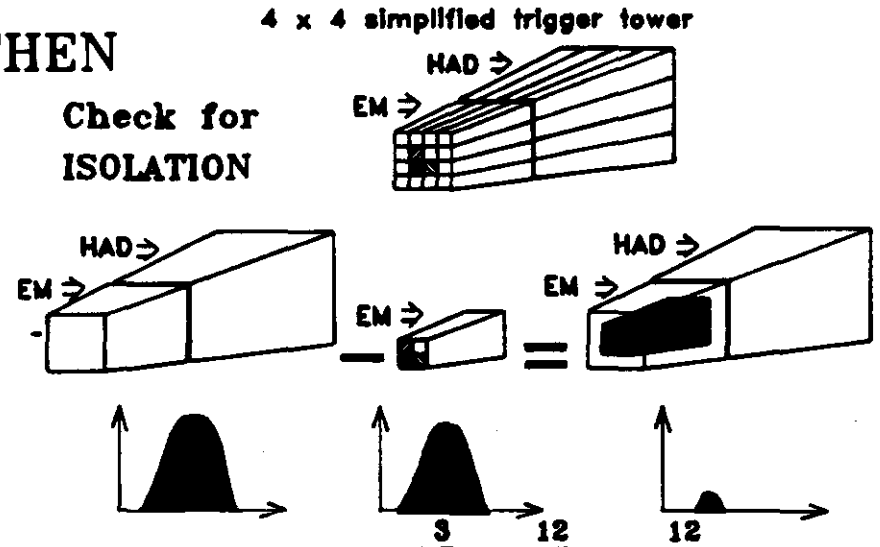
Threshold $< \sum_{i=1}^{8} I_i + C$.



Threshold $< C_{em} + I_{em}$; $\frac{(HAD)}{(EM)} <$ Threshold

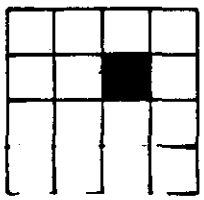
THEN

Check for ISOLATION



Threshold $< C_E + \sum_{i=1}^{3} I_{E_i} + \sum_{i=1}^{12} O_{E_i} + \sum_{i=1}^{12} O_{EM_i}$

Jet finding



Threshold $< \sum_{i=1}^{16} E_{EM_i} + \sum_{i=1}^{16} E_{E_i}$

15 steps

31 steps

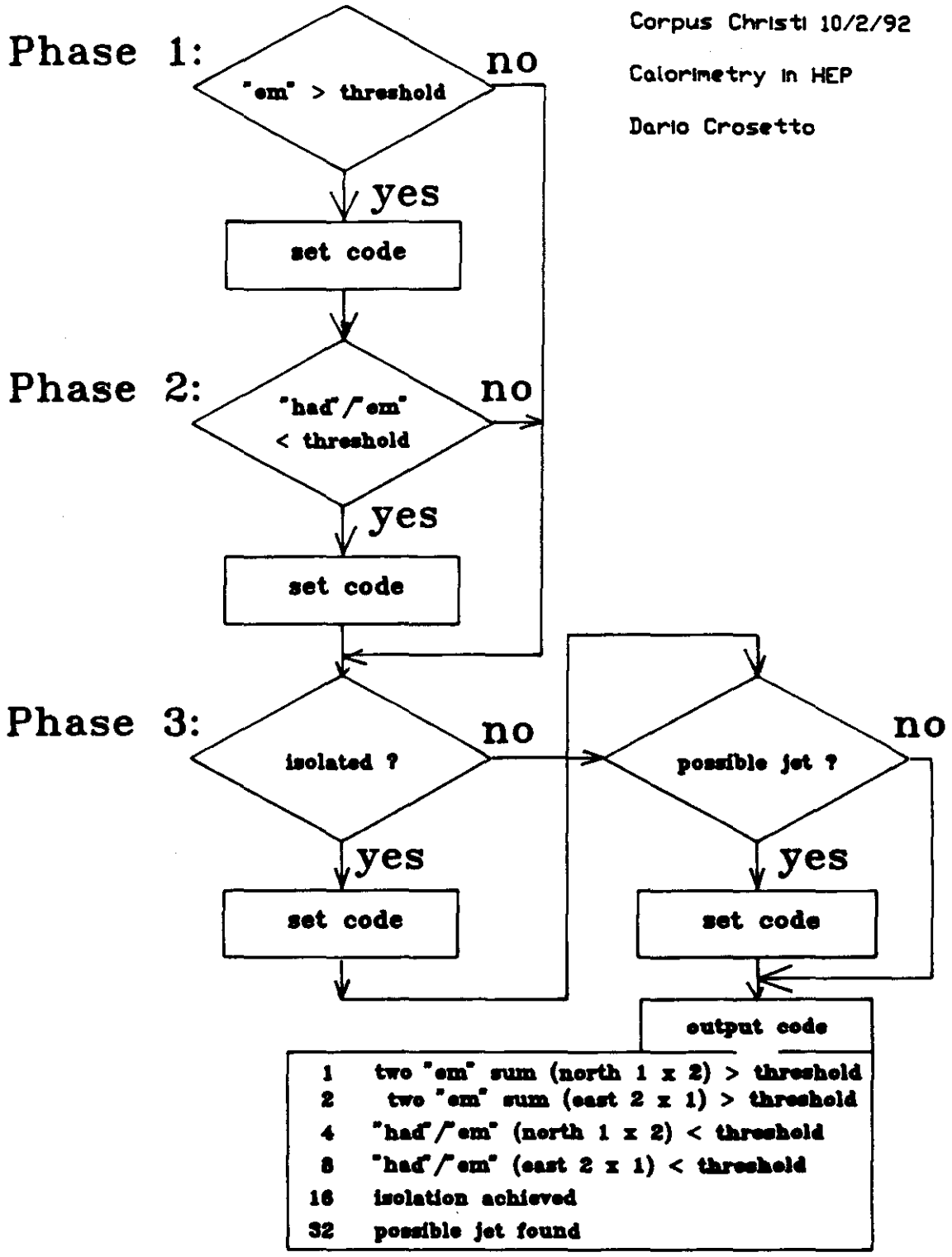
Any algorithm type and length

Algorithm flow-chart

Corpus Christi 10/2/92

Calorimetry in HEP

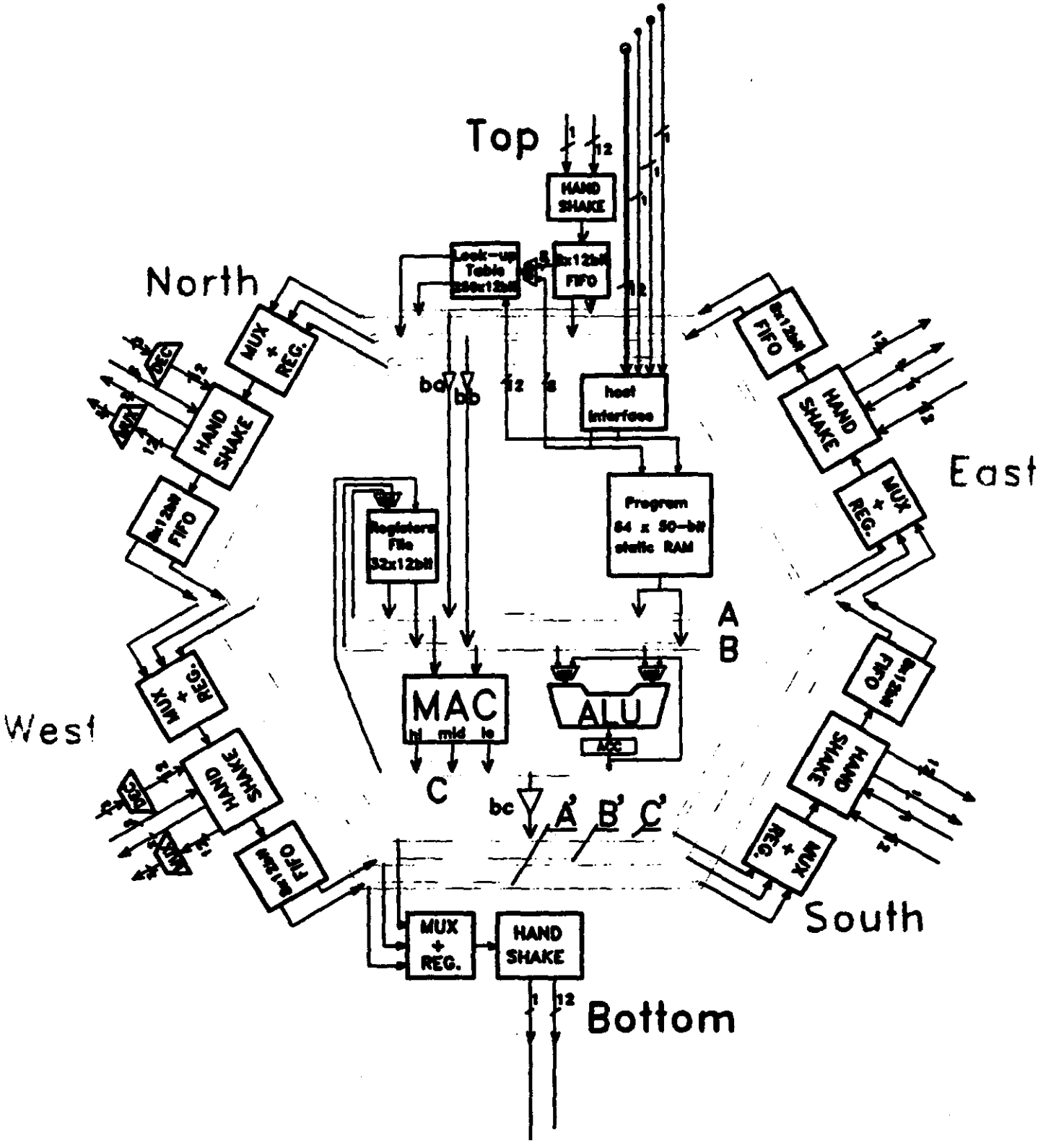
Dario Crosetto



e.g. A "FEP" may return a code = 37 (1+4+32) stating:

- a possible electron was found,
- but it was not isolated from the sorrounding energy,
- and that cell may be part of a 4 x 4 jet.

3D-Flow Cell Architecture



Dario Crosetto

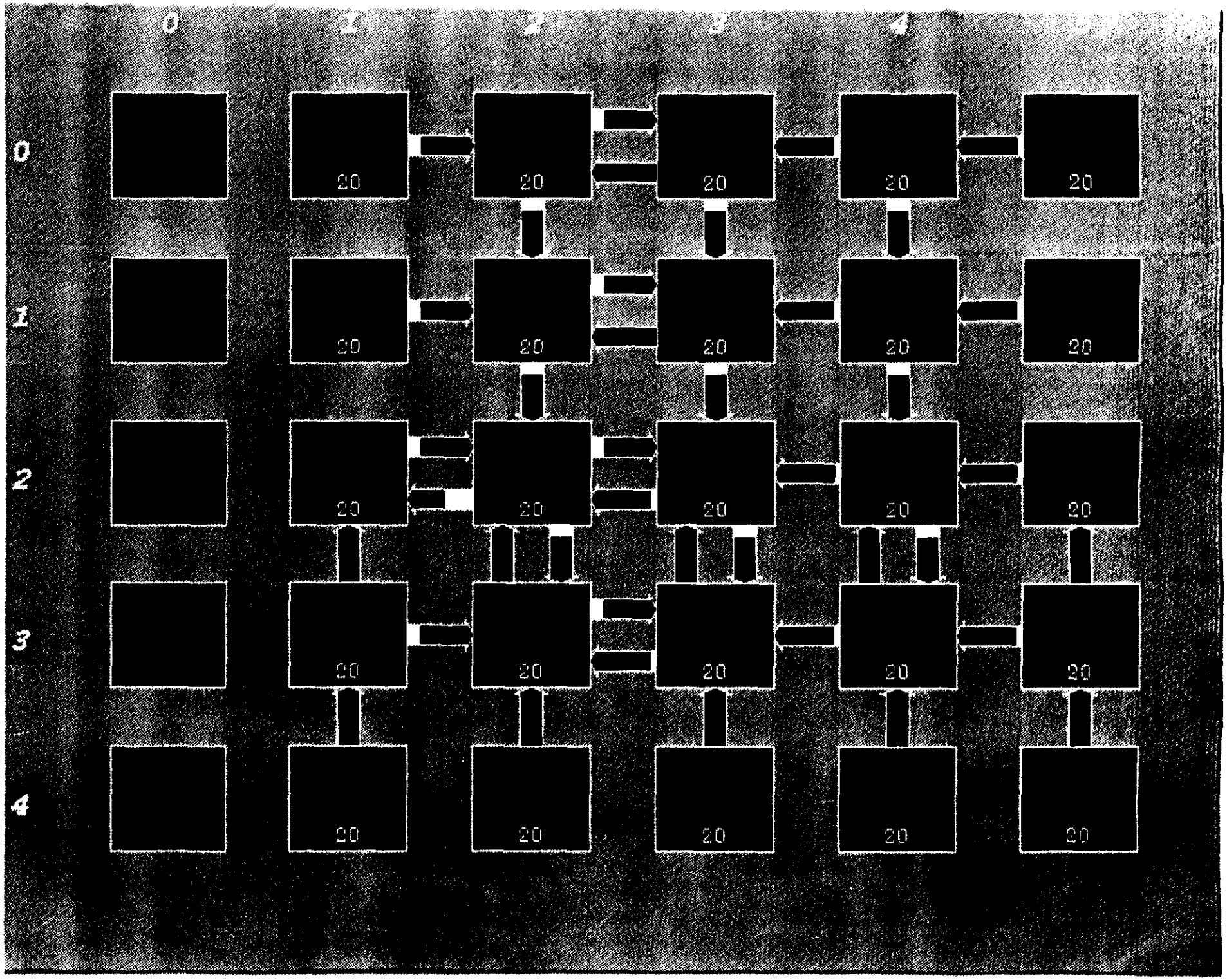
September 24, 1992

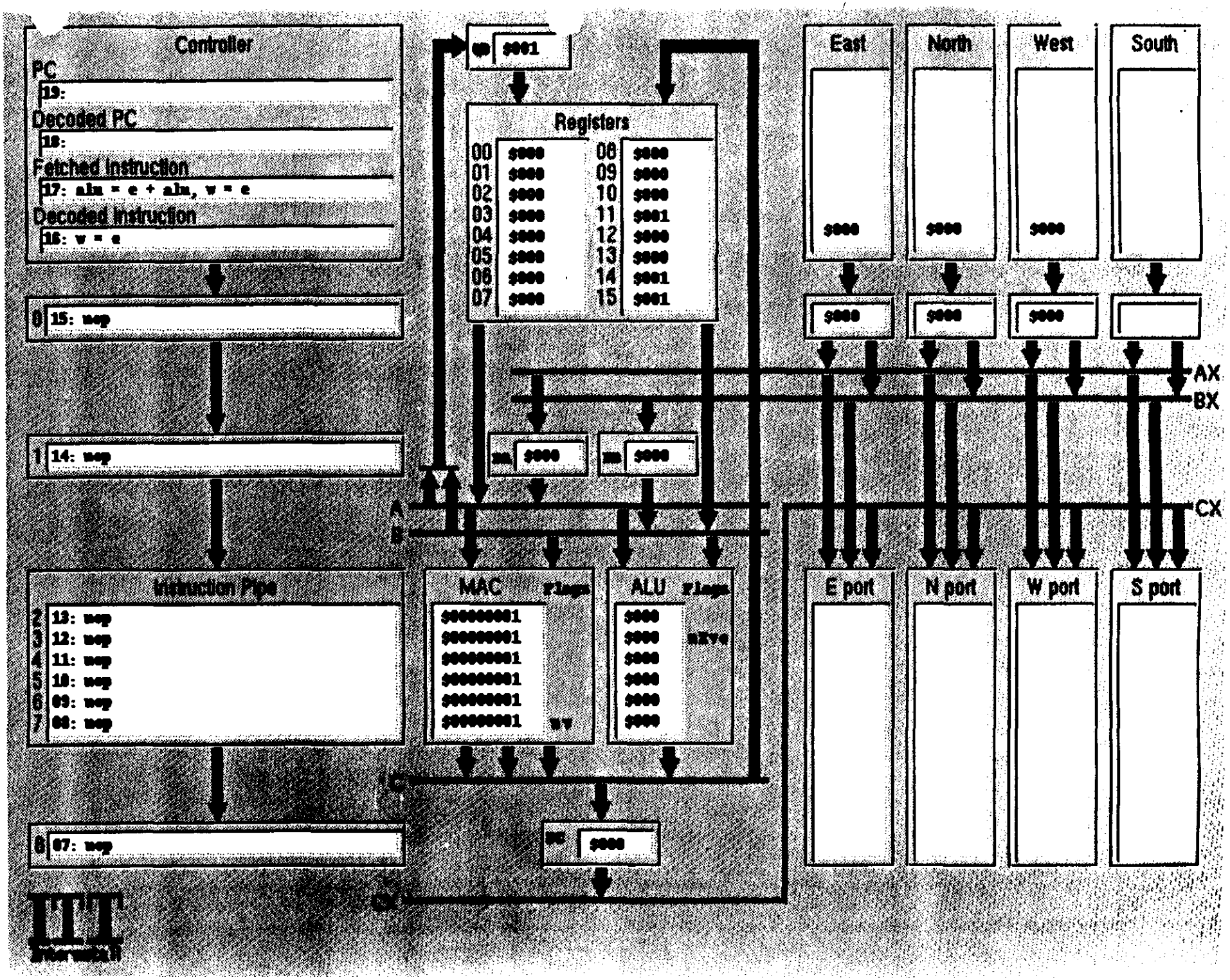
EP assembler code of the four pipelined stages of the 15 steps algorithm

xec. tep	common code to all stages		Different code for different stages				Comments	line code
			Stage 4	Stage 3	Stage 2	Stage 1		
	.cell 0,1,2							
0	loop:	r1=s=w=t*r14	(4a)	(3a)	(2a)	(1a)	; receive "em" value from calorimeter	1
1		r2=s=w=t*r15	(4b)	(3b)	(2b)	(1b)	; receive "had" value from calorimeter	2
2		r7=r1+n,	b=t (1c)				; north 1 x 2 "em" sum	3
3		r8=r2+n,	b=t (1d)				; north 1 x 2 "had" sum	4
4		r9=r1+e,		b=t (4a)	b=t (3a)	b=t (2a)	; east 2 x 1 "em" sum	5
5		r10=r2+e,		b=t (4b)	b=t (3b)	b=t (2b)	; east 2 x 1 "had" sum	6
6		alu=r7-r6,	b=t (2c)	b=t (1c)			; compare 1 x 2 "em" sum to Threshold	7
7		bpl north,	b=t (2d)	b=t (1d)				8
8		alu=r9-r6,			b=t (4a)	b=t (3a)	; compare 2 x 1 "em" sum to Threshold	9
9		bpl east,			b=t (4b)	b=t (3b)		10
10		bra nosend1	b=t (3c)	b=t (2c)	b=t (1c)			11
8	north:	acc=r7*r6,			b=t (4a)	b=t (3a)	; "em" * Threshold (1 x 2)	12
9		acc=acc-r8,			b=t (4b)	b=t (3b)	; "em" * Threshold - "had"	13
10		bmpl sendn,	b=t (3c)	b=t (2c)	b=t (1c)			14
11		bra nosend2,	b=t (3d)	b=t (2d)	b=t (1d)			15
10	east:	acc=r9*r6,	b=t (3c)	b=t (2c)	b=t (1c)		; "em" * Threshold (2 x 1)	16
11		acc=acc-r10,	b=t (3d)	b=t (2d)	b=t (1d)		; "em" * Threshold - "had"	17
12		bmpl sende,				b=t (4a)		18
13		bra nosend3,				b=t (4b)		19
11	sendn:	nop,	b=t (3d)	b=t (2d)	b=t (1d)			20
12		nop,				b=t (4a)		21
13		nop,				b=t (4b)		22
14		b=012	(4c)	(3c)	(2c)	(1c)	; send out tower id	23
15		b=r7, bra loop	(4d)	(3d)	(2d)	(1d)	send out 1 x 2 "em" energy	24
13	sende:	nop,				b=t (4b)	; send out tower id	25
14		b=012	(4c)	(3c)	(2c)	(1c)		26
15		b=r9, bra loop	(4d)	(3d)	(2d)	(1d)	; send out 2 x 1 "em" energy	27
11	nosend1:	nop,	b=t (3d)	b=t (2d)	b=t (1d)			28
12	nosend2:	nop,				b=t (4a)		29
13		nop,				b=t (4b)		30
14	nosend3:	b=0	(4c)	(3c)	(2c)	(1c)	; send out null value	31
15		b=0, bra loop	(4d)	(3d)	(2d)	(1d)	; send out null value	32
	.end							

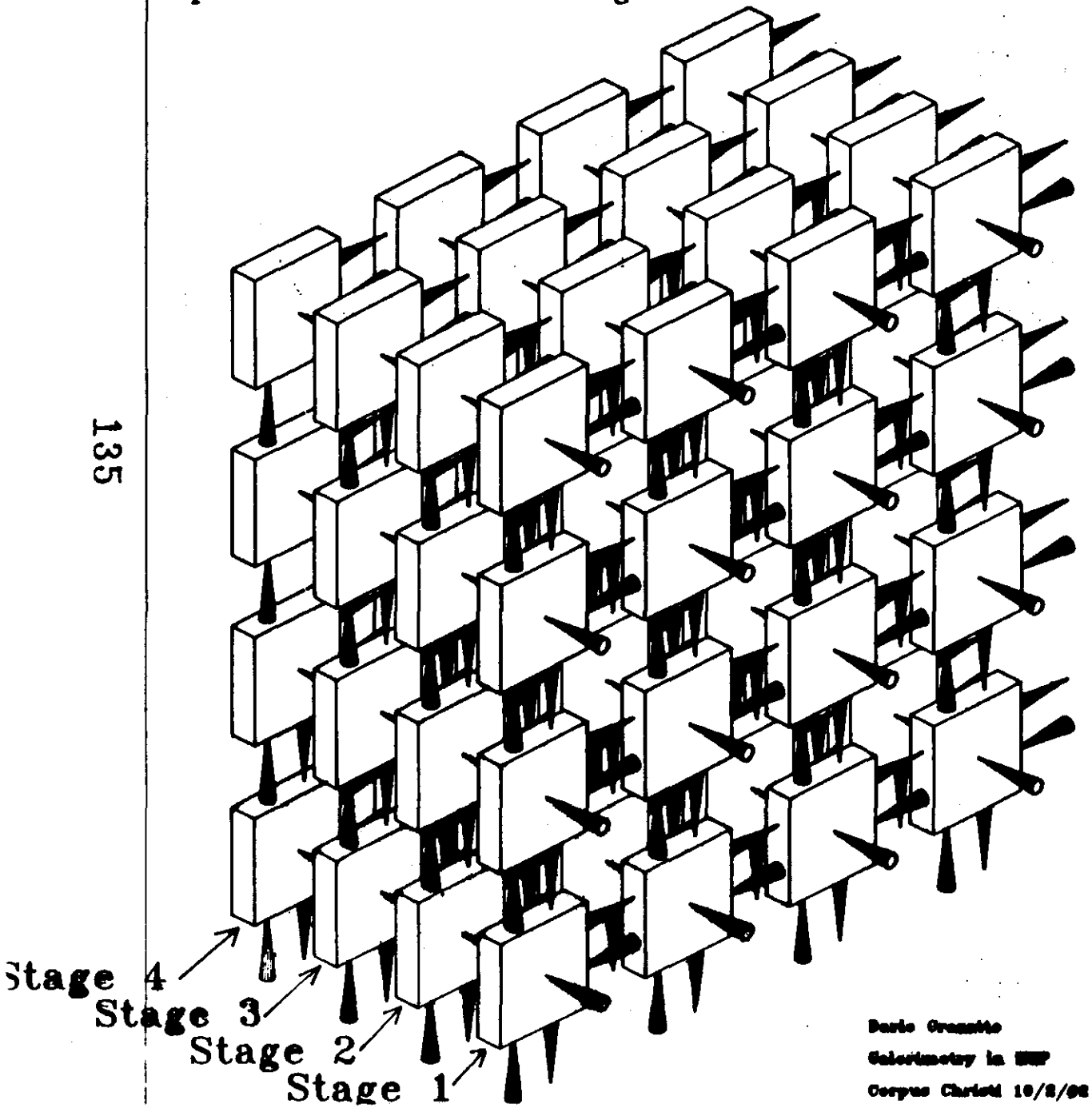
a = inputted "em" value c = outputted tower id

b = inputted "had" value; d = outputted "em" sum (either 1 x 2 or 2 x 1)


0
1
2
3
4
0
1
2
3
4
20

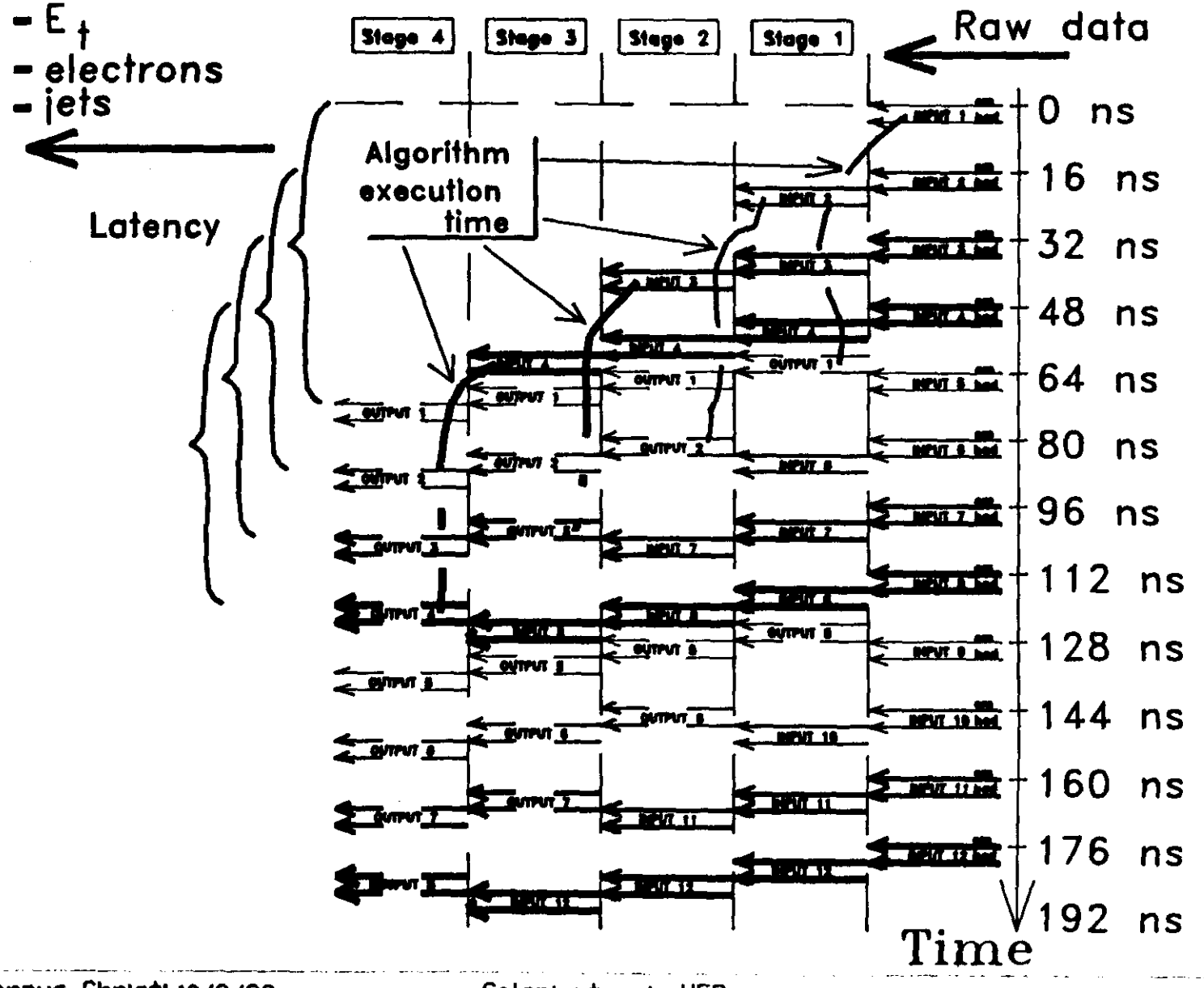

Controller
PC
19:
Decoded PC
18:
Fetched Instruction
17: alu = e + alu, w = e
Decoded Instruction
16: w = e
0 15: nop
1 14: nop
Instruction Pipe
2 13: nop
3 12: nop
4 11: nop
5 10: nop
6 09: nop
7 08: nop
8 07: nop
$001
Registers
00 $000
01 $000
02 $000
03 $000
04 $000
05 $000
06 $000
07 $000
08 $000
09 $000
10 $000
11 $001
12 $000
13 $000
14 $001
15 $001
$000
$000
A
B
MAC
Flags
$00000001
$00000001
$00000001
$00000001
$00000001
$00000001
ALU
Flags
$000
$000
$000
$000
$000
$000
C
$000
East
North
West
South
$000
$000
$000
$000
$000
$000
AX
BX
CX
E port
N port
W port
S port
ITT

Pipelined Parallel Processing Architecture



Dario Grazzotto
Calorimetry in [illegible]
Corpus Christi 10/2/92

Timing Diagram of Four FEP Stages of a Pipelined Programmable Level 1 Trigger



Question asked at this point:

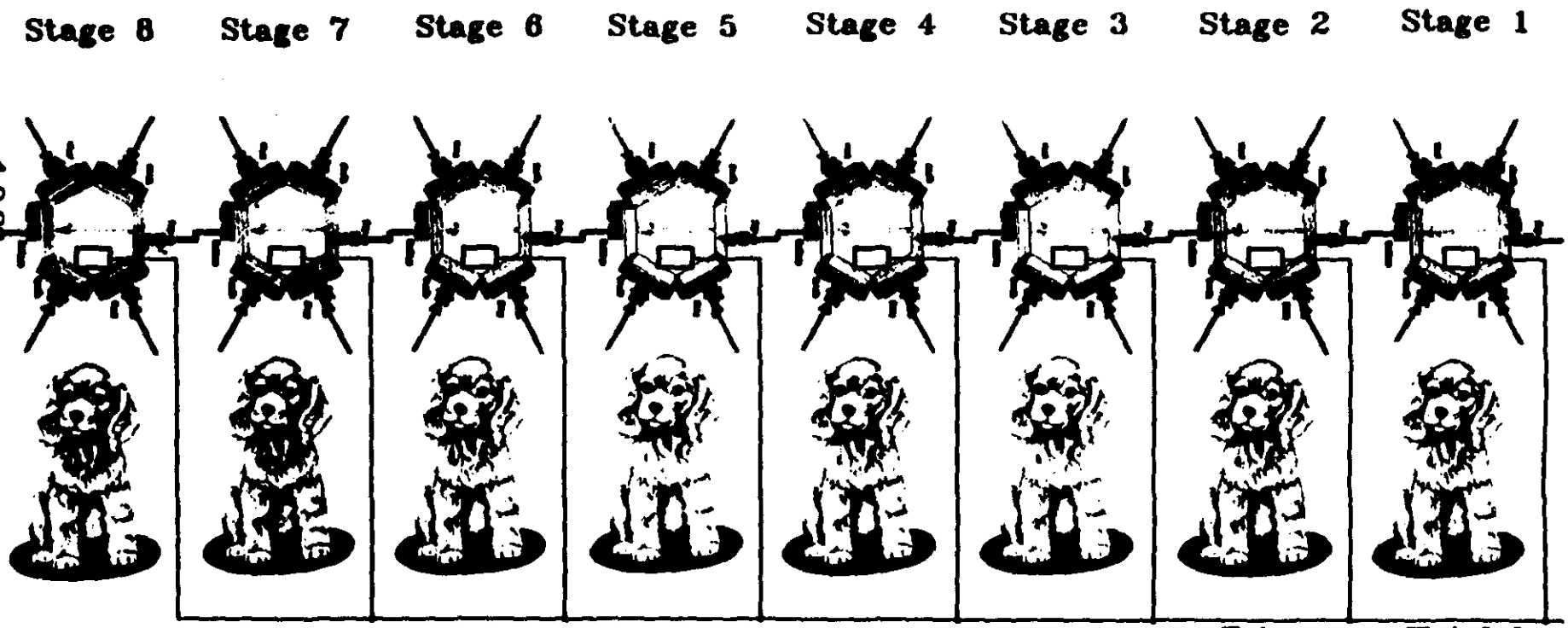
- how can you control the data-flow interruption in a thousand processor array ???

Answer:

- watchdog circuitty at each 3D-Flow processor

One Channel of the "3D-Flow"

Pipelined Parallel Processing Architecture



Trigger = Watchdog

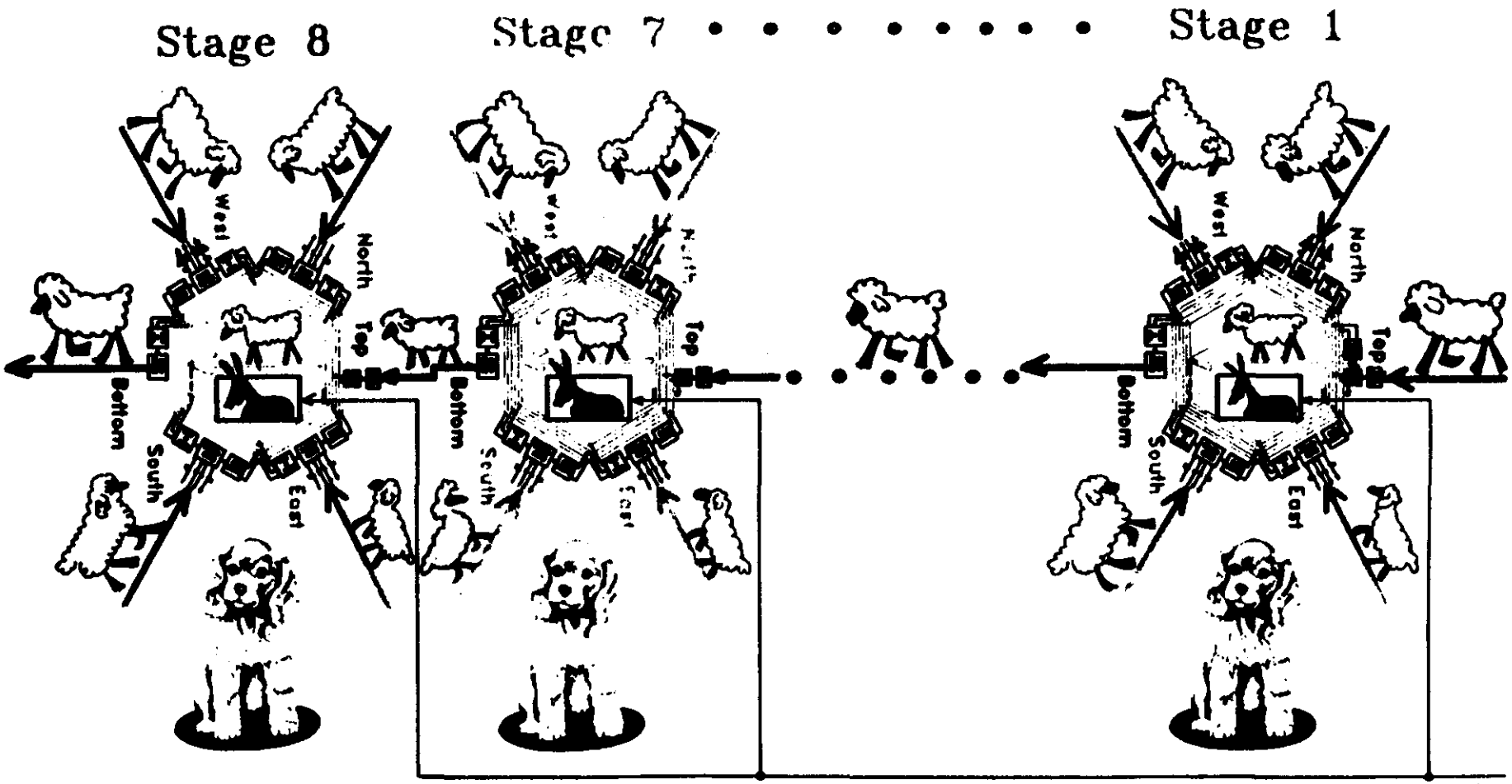
Watchdog Data-Flow Control

SSCL 10/23/1992

Dario Crosetto

One Channel of the "3D-Flow"

Pipelined Parallel Processing Architecture



Trigger = Watchdog

Watchdog Data-Flow Control

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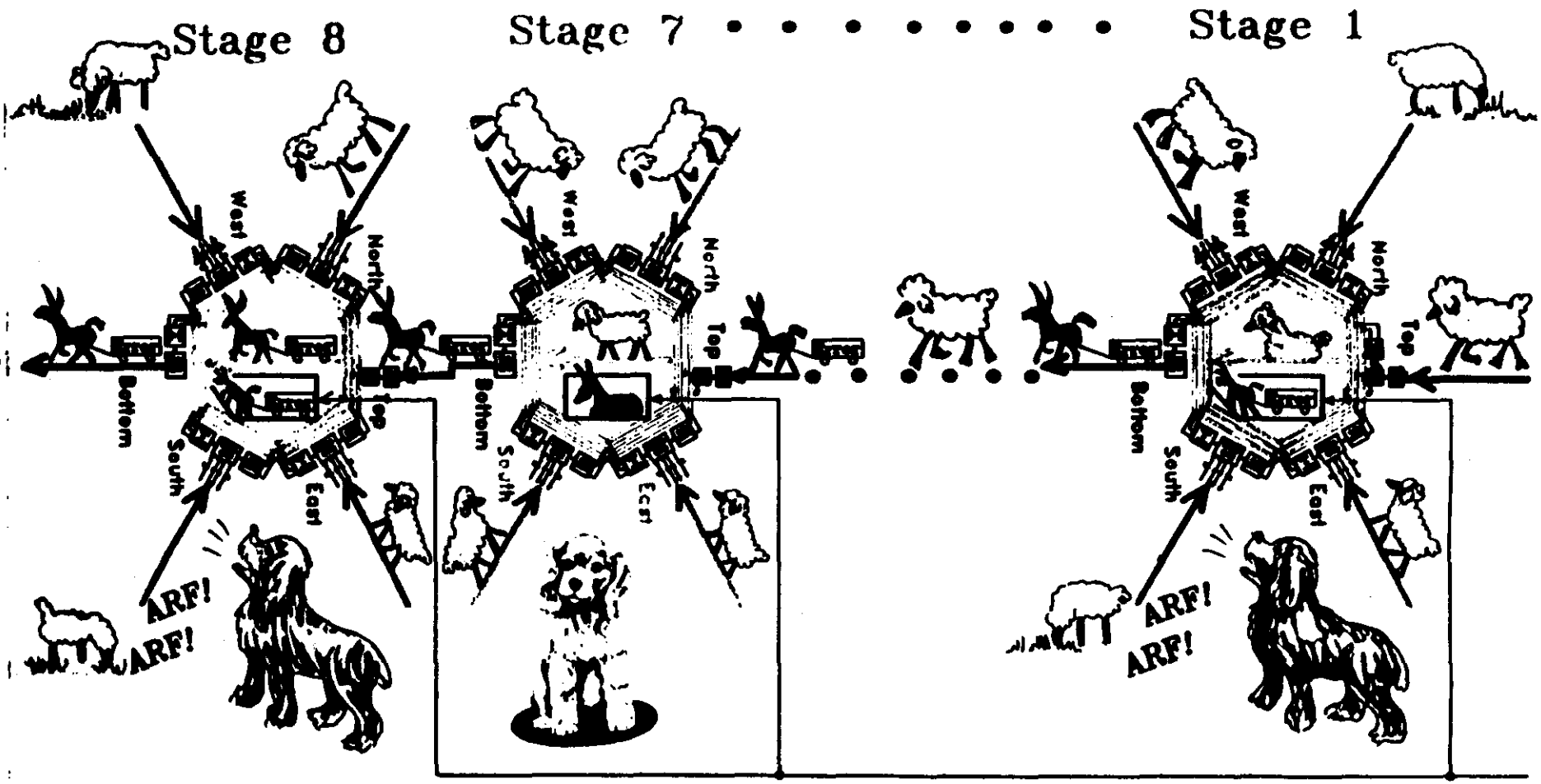
One Channel of the "3D-Flow"

Pipelined Parallel Processing Architecture



Trigger = Watchdog

Watchdog Data-Flow Control

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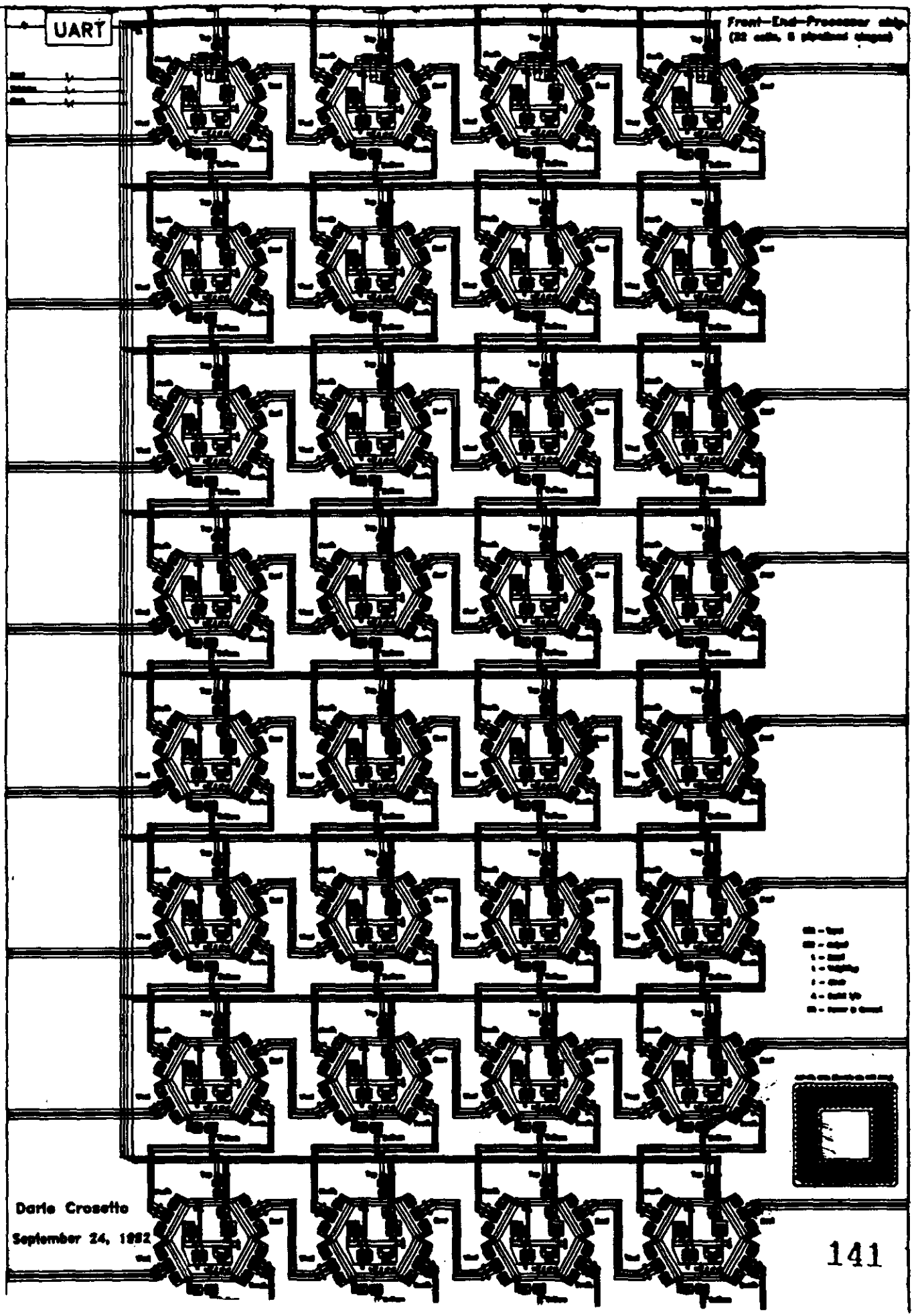
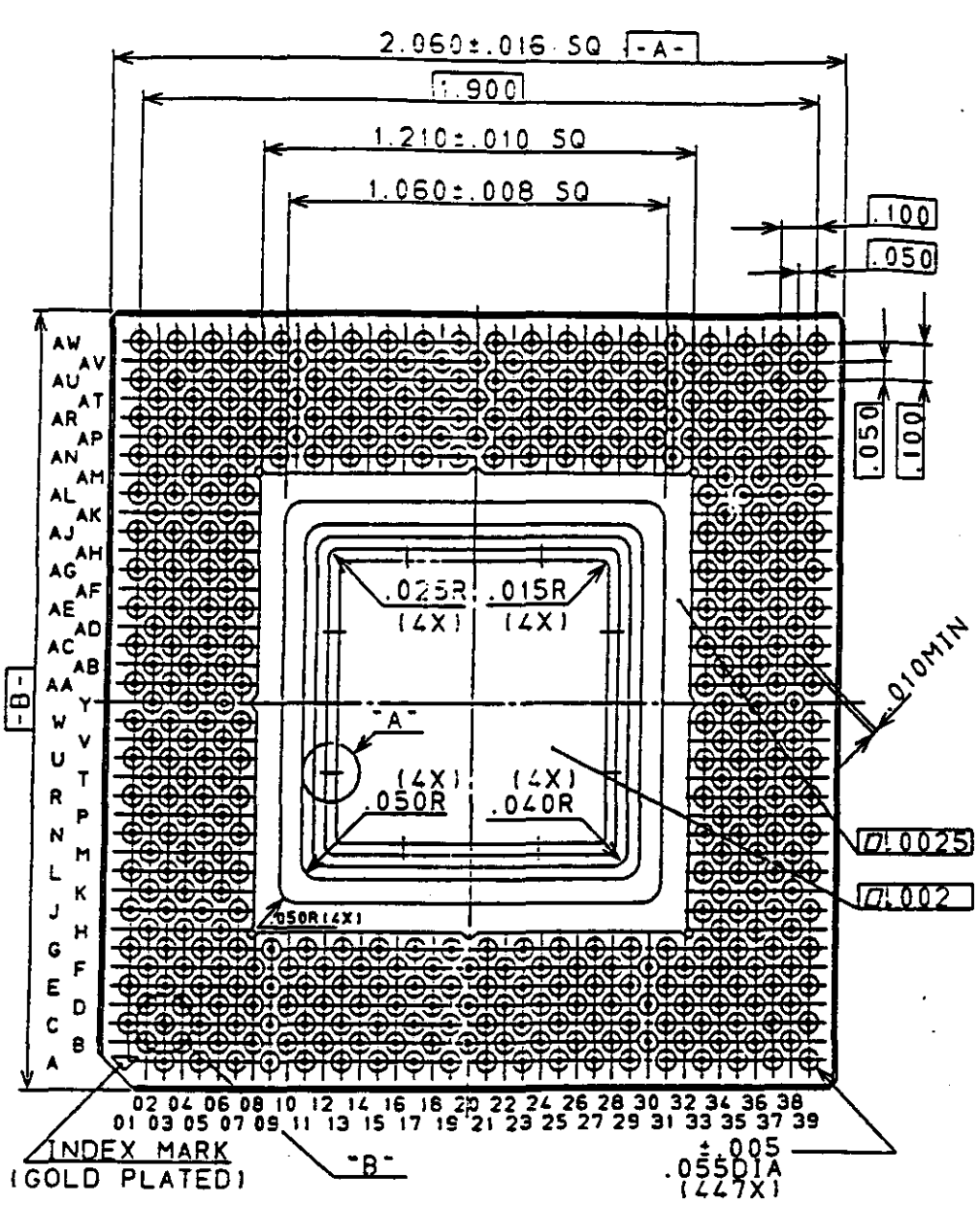
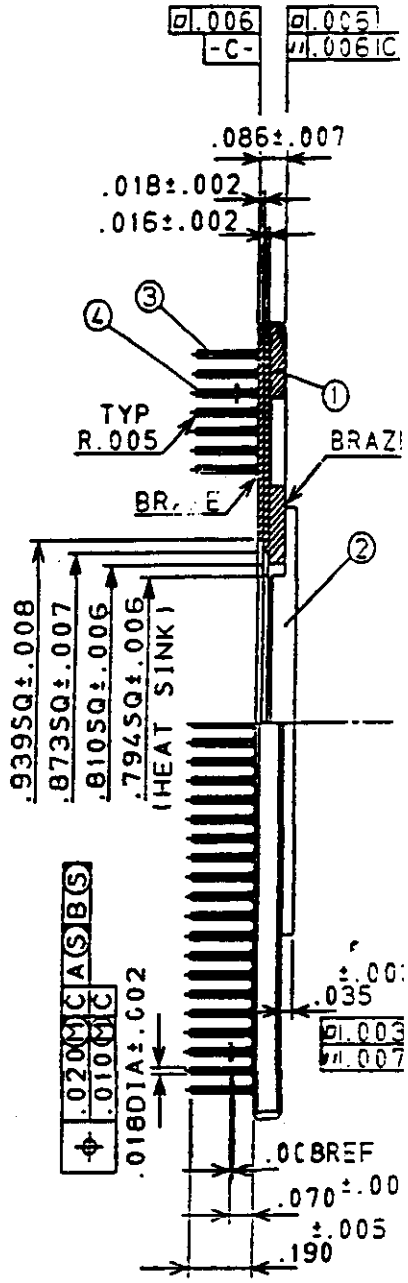
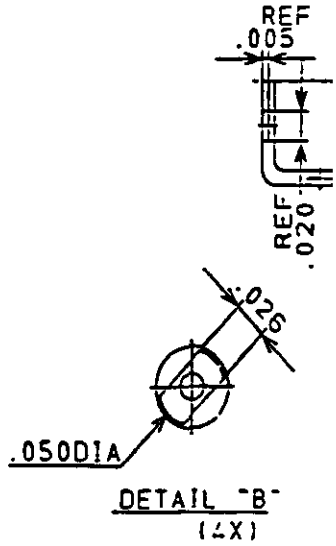

UART
Front-End-Processor chip
Dario Crosetto
September 24, 1982

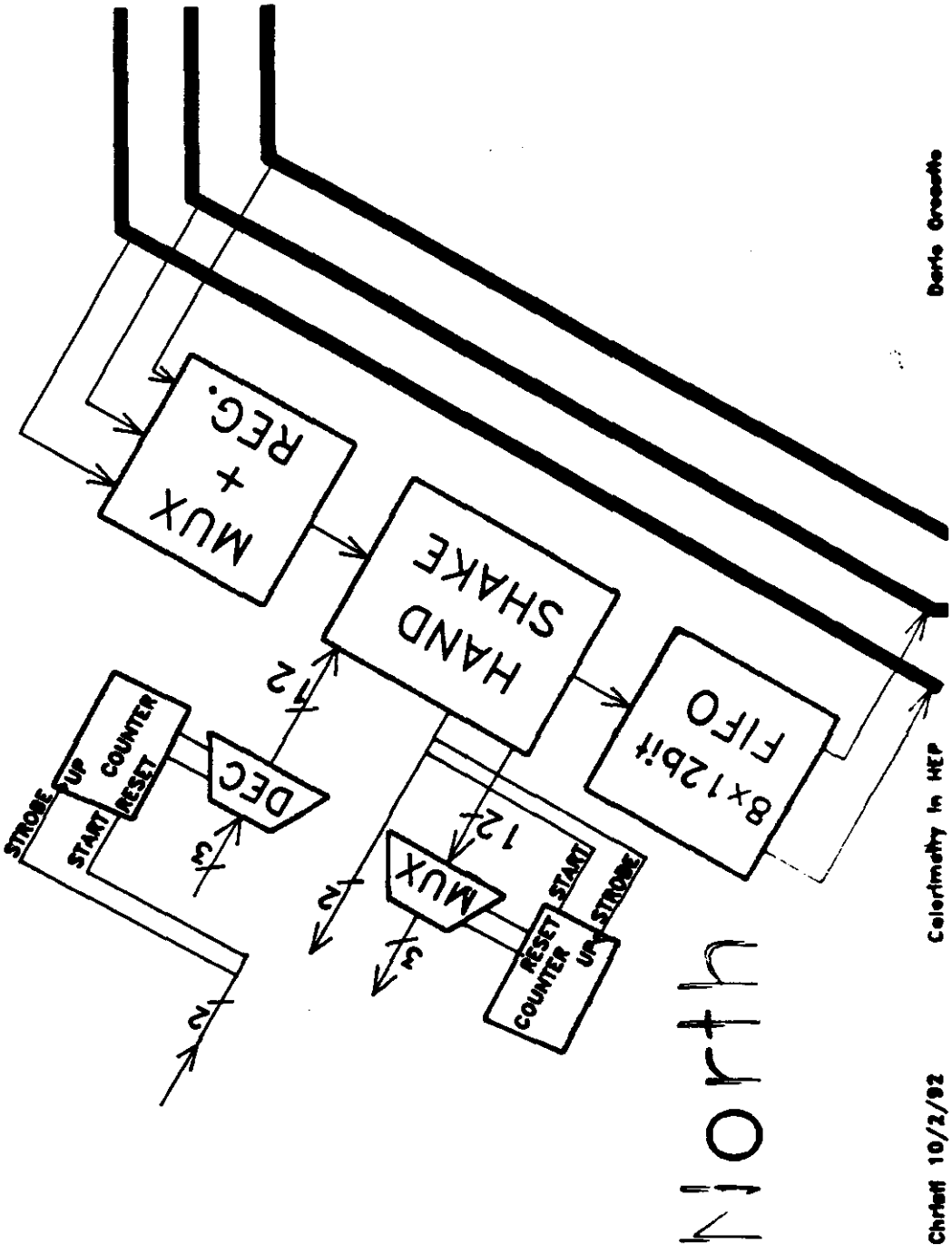




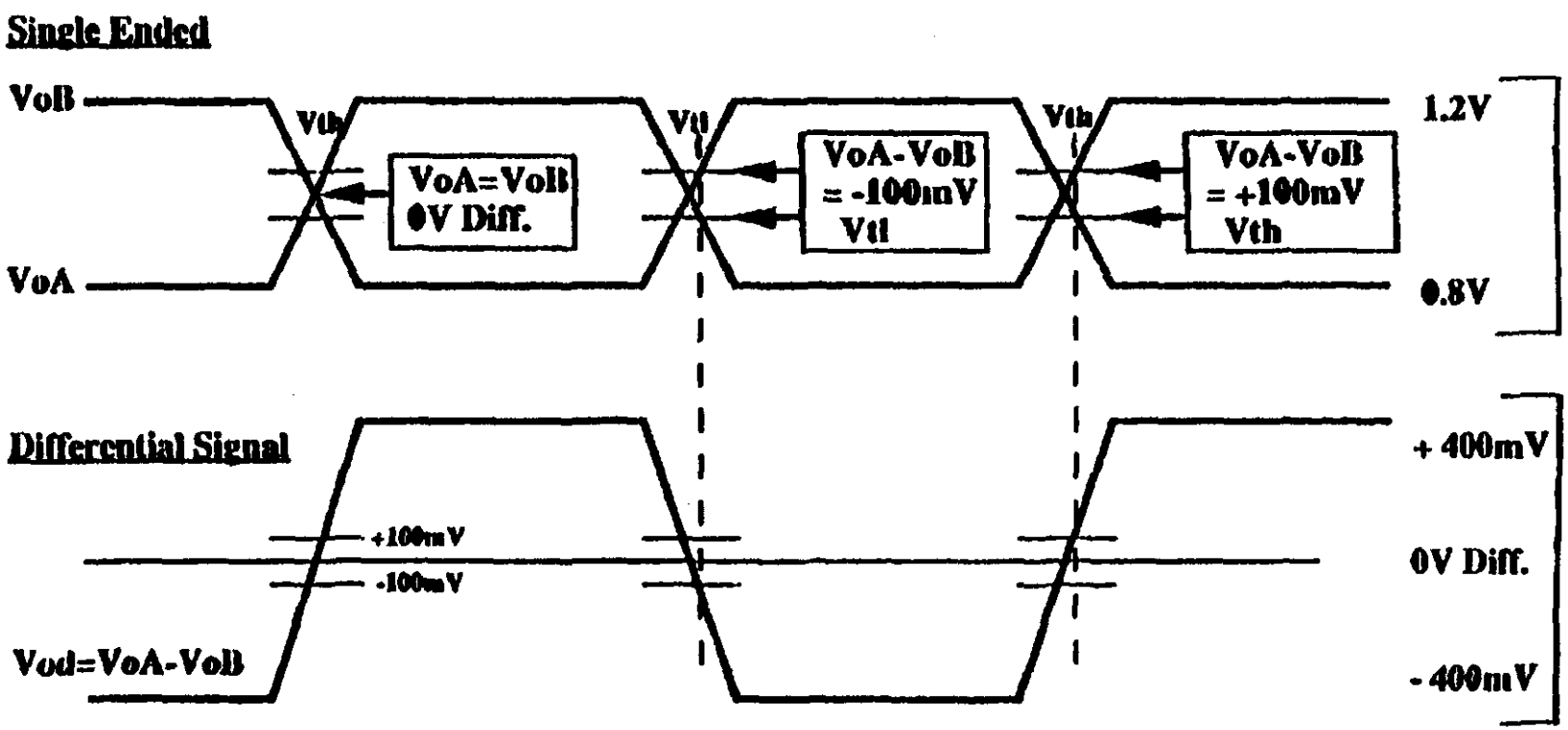


NOTES:

1. GOLD PLATE 60μ~225μ INCHES OVER 50μ~350μ INCHES MIN NICKEL.
2. HEAT SINK TO BE ELECTRICALLY ISOLATED FROM ALL PINS
3. SEAL RING TO BE ELECTRICALLY CONNECTED TO VSS.
4. MATERIALS SHALL CONFORM TO LSI SPEC JB00-000002-00 LATEST REVISION AT TIME OF PURCHANSE.
5. ALL VIAS TO BE SOLID SUCH THAT VOIDING IN VIA WILL NOT REDUCE THE VIA CROSS SECTION BY GREATER THAN 20 % VIA DIAMETER. (0/76 VIA 3 LTPD)
6. T-BAR STAND OFFS TO POINT TOWARDS CAVITY CENTER.
7. LEAD RESISTANCE: SIGNAL---1Ω MAX.
8. REFERENCE VENDOR NTK: (PKA4F4-685ZA.


MUX
+
REG.
HAND
SHAKE
8x12bit
FIFO
DEC
MUX
STROBE
UP
COUNTER
START
RESET
12
3
2
12
2
3
RESET
COUNTER
UP
START
STROBE
North
Corpus Christi 10/2/92
Calorimetry in HEP
Dario Grosso

Differential Waveform



- Small signal swing eases rapid switching speeds
- Differential signals provide noise immunity

OCT-22-1992 09:51 FROM ASIP DESIGN SC BLD E NO 9214106 P.04

TABLE 1. Estimated number of Gates required for a 60 MHz 3D-Flow chip assembly (32 cells)

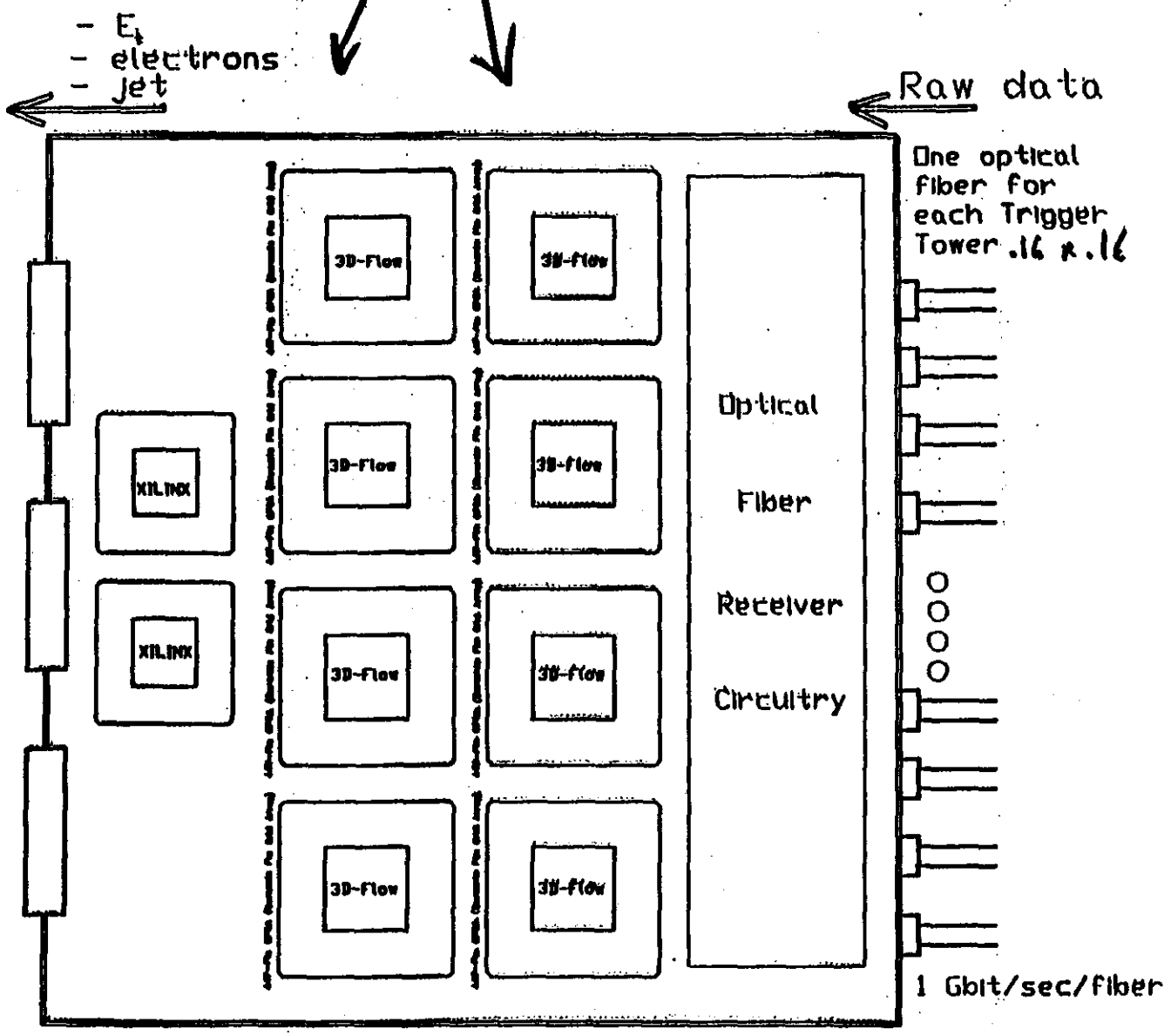
Unit	Logic Function	Functions/ Chip	Gates/3D-Flow cell	Gates/ Unit	3D-Flow with 32 cells/chip. Gates/Chip
3D-Flow core	Register File	32	3,072	11,422	98,304
	ALU 20-bit	32	900		28,800
	Program RAM	32	6,400 G. equiv.		204,800
	Prog. RAM control	32	250		8,000
	Internal Host Interf.	32	800		25,600
Additional core	MAC 27-bit	32	4,500	4,500	144,000
Interface to Calorimeter	Look-up Table (256x12-bit)	4	6,144 G. equiv.	6,144	24,576
Host Interface	UART	1	1,000		1,000
Output	MUX Out	24	250x4	1,182	6,000
	Direct Out	136	182x1		24,752
FIFOs	Top 8x12-bit	32	192 G. equiv (x1)	752	6,144
	Control Top	32	80		2,560
	NEWS 2x12-bit	128	120x4		15,360
	Control+MUX	24	200x4		4,800
3D-Flow w/o CAL interf. w/o MAC			13,356		
3D-Flow w/ CAL interf. w/o MAC			19,500		450,696
3D-Flow w/ CAL interf. w/ MAC			24,000		594,696

Table 1:

Processing Element Cell and chip description	Technology	CPU Clock frequency in MHz	I/O Speed in MHz	Load on Output (pF)	Number of gates estimated for each CPU	Total number of gates estimated	Power (watt)	Packaging (pins)	Design Cost-Delivery $x1K-weeks	Layout Cost-Delivery $x1K-weeks	Fabrication Cost-Delivery $x1K-weeks	Test Cost-Delivery $x1K-weeks	Total Cost-weeks (10 chips tested and delivered) $x1K-weeks	Cost per chip for 5,000 unit prod. Die-die+pack ($)
FEP w/o MAC w/o SCAN	xxxx_.xu xxCMOS	120	240 480	10 10	xx,xxx	xxx,xxx	x.x y.y	447 CPGA	xxx-aa yyy-bb	xxx-aa yyy-bb	xxx-aa yyy-bb	xxx-aa yyy-bb	xxx-aa yyy-bb	xxx-aaa yyy-bbb
FEP w/o MAC w/ SCAN		120	240 480	10 10				447 CPGA						
FEP w/ MAC w/o SCAN		120	240 480	10 10				447 CPGA						
FEP w/ MAC w/ SCAN		120	240 480	10 10				447 CPGA						
FEP w/o MAC w/o SCAN		60	120 240	10 10				447 CPGA						
FEP w/o MAC w/ SCAN		60	120 240	10 10				447 CPGA						
FEP w/ MAC w/o SCAN		60	120 240	10 10				447 CPGA						
FEP w/ MAC w/		60	120 240	10 10				447 CPGA						

GEM Programmable Level 1 Trigger = 180 boards

One Board of the Programmable Level 1 Trigger with 3D-Flow Pipelined Array



SSCL 10/23/1992

Dario Crosetto

- Trigger Algorithms

- Algorithms Simulation
  on a programmable processor-array

- Design of System and Chip
  ARCHITECTURE

- Feasibility Study

- Checked with Industries

?

Build a prototype CHIP

R&D cost: from 189 K to 279 K $

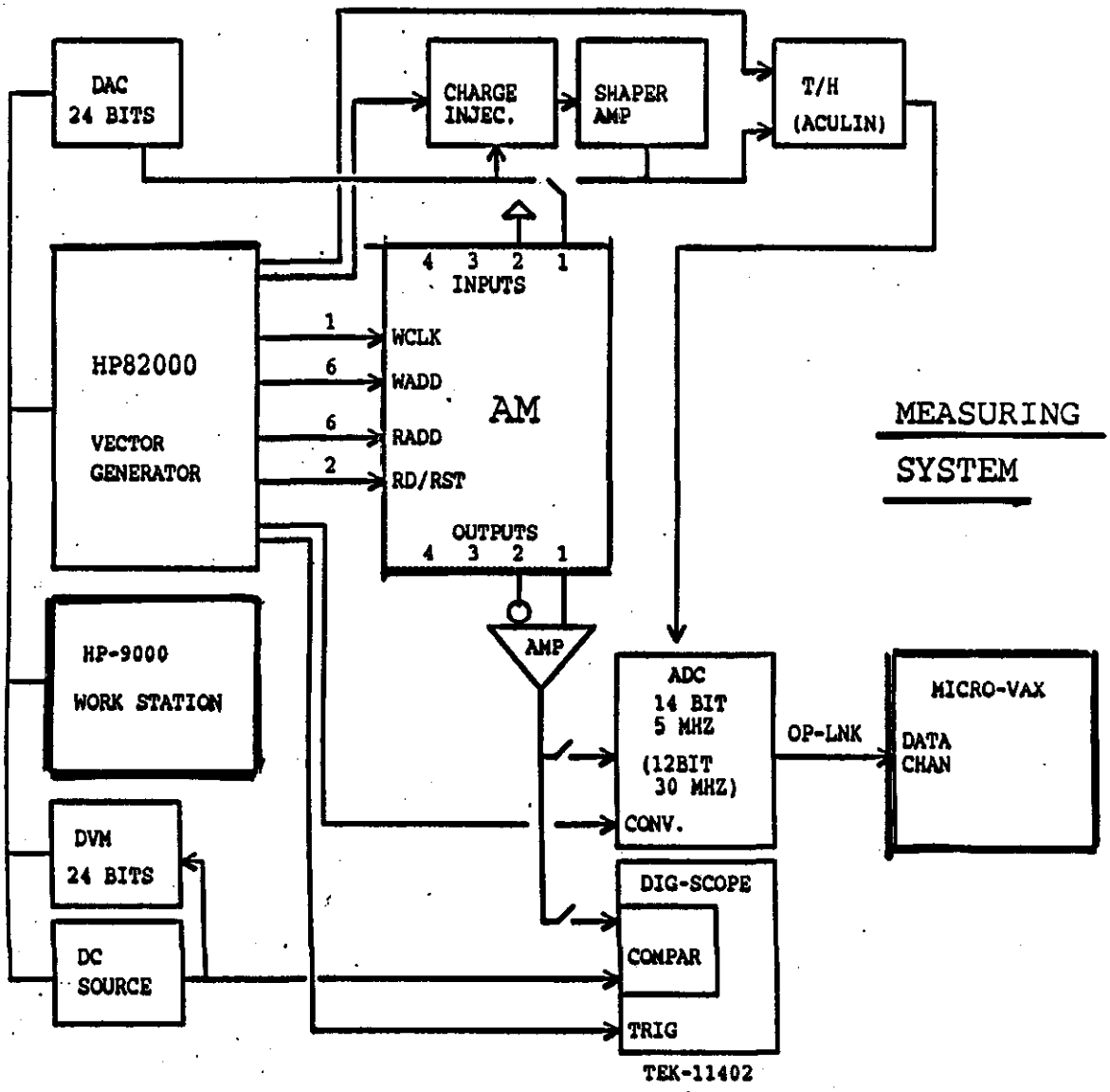
gem

γeμ

Presentation by:

W. Sippach

AM-TEST


DAC
24 BITS
CHARGE
INJEC.
SHAPER
AMP
T/H
(ACULIN)
HP82000
VECTOR
GENERATOR
4 3 2 1
INPUTS
1
6
6
2
WCLK
WADD
RADD
RD/RST
AM
OUTPUTS
4 3 2 1
MEASURING
SYSTEM
HP-9000
WORK STATION
AMP
ADC
14 BIT
5 MHZ
(12BIT
30 MHZ)
CONV.
OP-LNK
MICRO-VAX
DATA
CHAN
DVM
24 BITS
DIG-SCOPE
COMPAR
TRIG
DC
SOURCE
TEK-11402

PRELIMINARY RESULTS ON A NEVIS ANALOG MEMORY

GOAL: DEVELOP AN AM FOR HI PRECISION CALORIMETRY FOR GEM AT SSC.

8 DIFFERENTIAL , 200 CELL CHANNELS.
60 MHZ SAMPLING , SIMULTANEOUS READ-WRITE FOR PIPELINING.
5 MHZ MUX READOUT TO ADC'S.
0.1% CALIBRATION , TWO 12BIT RANGES FOR 16 TO 17 BIT DYN. RANGE.

TEST CHIPS: (ORBIT 1.2U DMDP N WELL PROCESS)

1 8 CELL 4 CHANNEL , INDEPENDENT R-W , NO DECODING - FINISHED

2 48 CELL 4 CHANNEL , INDEPENDENT R-W , FULL DECODING - FINISHED

3 SAME AS 2 WITH OUTPUT MUX AND BUFFER OUTPUT TO ADC - DESIGNED

4 SAME AS 2 WITH PUSHPULL W-ADDRESS LOGIC TO STUDY NOISE.

PRELIMINARY RESULTS FOR 4 CH 48 CELL CHIP: (12 FORSIGHT TINY CHIPS)

1	DC LINEARITY (MAX.DEV. ST LINE)	0.1 %
2	DYNAMIC RANGE	> 3 VOLTS
3	TOTAL PEDESTAL NOISE	< 1 MV.
4	PATTERN NOISE DEPENDENCE: DC INPUT VOLTAGE	INVARIENT
	WRITE FREQUENCY	"
	ADDRESS PERMUTATION	?
5	CHANNEL CROSS-TALK -	MOSTLY THRU PACK.
6	INDUCED NOISE FROM READ TO WRITE PROCESS	< 1 MV
7	" " " WRITE " READ "	> 1 MV OF BINARY NOISE
8	DROOP	< 1MV / 10 MSEC.
9	AC LINEARITY	FUNCTION OF DV/DT
10	6 V. POWER VDDA	15 MW
	5 V. " VDDD AT 60 MHZ	11 MW

11 ALL CHIPS WERE FUNCTIONAL , AND NONE HAVE BEEN DAMAGED DURING TEST.

SOME CONCLUSIONS :

1 BINARY EDGE CHANGES ARE INDUCED THROUGH INPUT PAD TO SUBSTRATE CAPACITANCE ,AND NOISE IS ADDED BETWEEN THE SUBSTRATE AND EXT. GND.

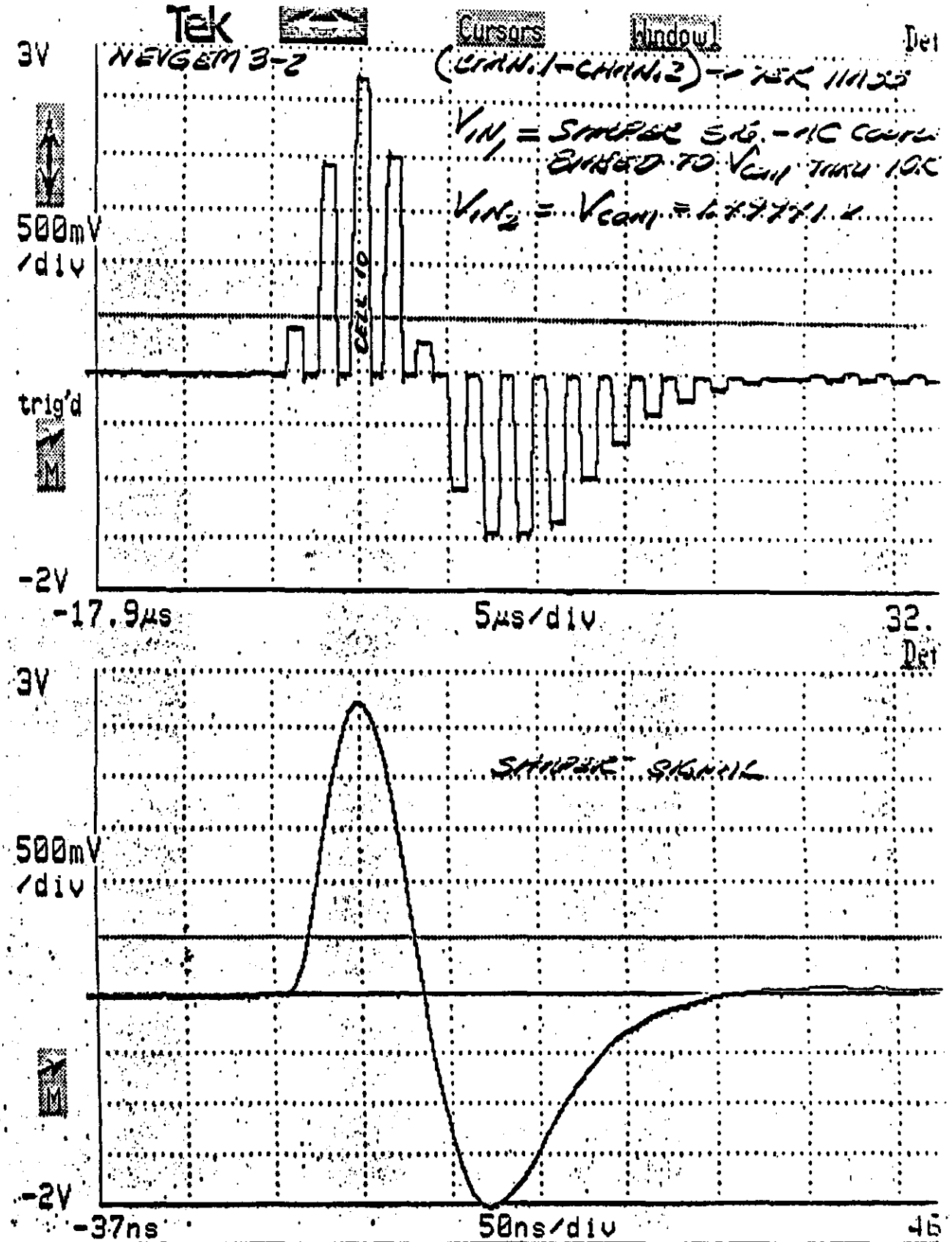
OUR DIFFERENTIAL READOUT REJECTS COMMON MODE NOISE , BUT HAS TROUBLE WITH VERY FAST EDGES.

2 AC LINEARITY IS LIMITED BY THE WRITE SW RES. DEPENDENCE ON SIGNAL VOLTAGE TIMES DV/DT.

3 WE SEE SYSTEMATIC EFFECTS FROM SEQUENCE PERTURBATIONS. THESE STUDIES REPRESENT OUR MAIN TEST EFFORT.

11402 DIGITIZING OSCILLOSCOPE
date: 9-OCT-92 time: 7:01:39

(exp:3.7,dig:3.91,dsy:3.3
Instrument ID# B010270



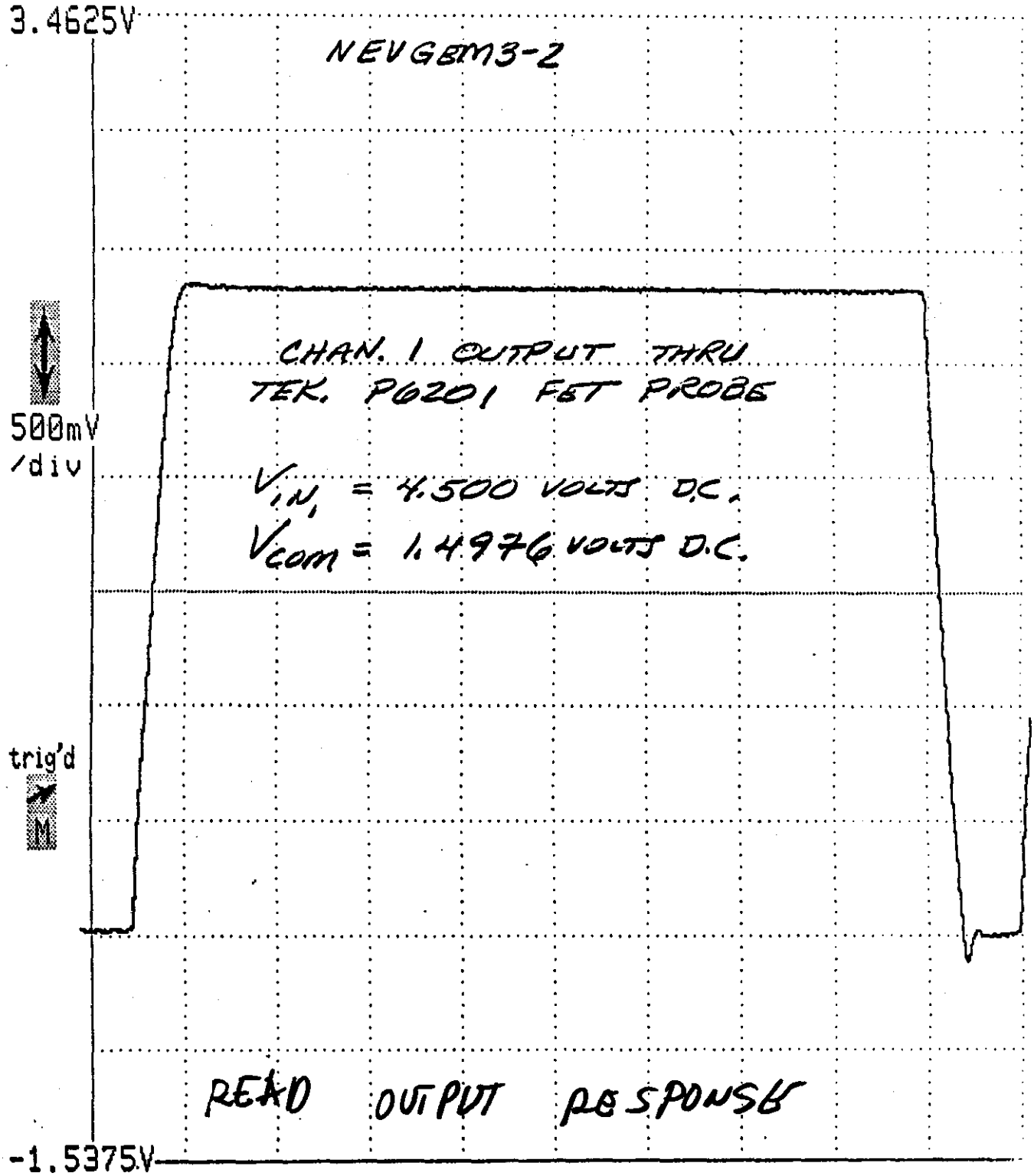
Vertical Desc	Horizontal Desc	Acquire Desc	Upper Graticule	Main Size
Avg(R1)	Main	Avg# >32	Linear	5µs/div
Fast	@ 1024 pts			Main Pos
				-10.5µs

60 MHz SAMPLING OF SHAPER

11402 DIGITIZING OSCILLOSCOPE {exp:3.7,dig:3.91,dsy:3.3}
date: 2-NOV-92 time: 11:23:31 Instrument ID# B010270

Tek

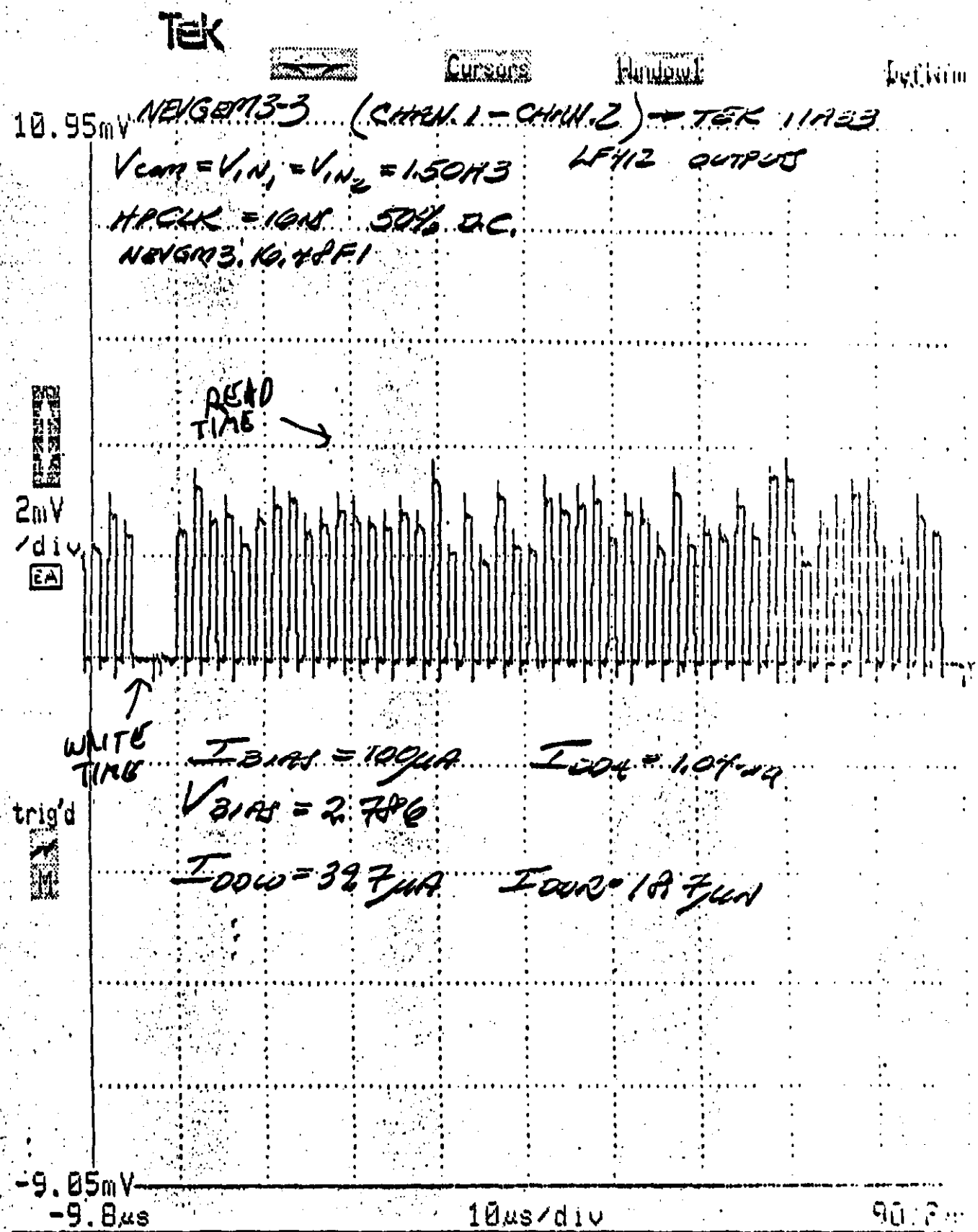
Cursors Window1 DefWfm



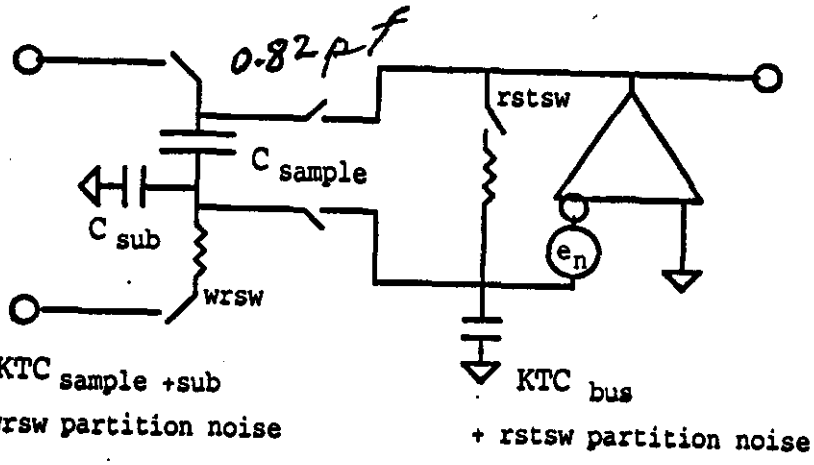
Vertical Desc	Horizontal Desc	Acquire Desc	Graticules	Main Size
				200ns/div
Avg(R1)	Main	Avg# >32	Linear	Main Pos
Fast	@ 1024 pts			-200ns

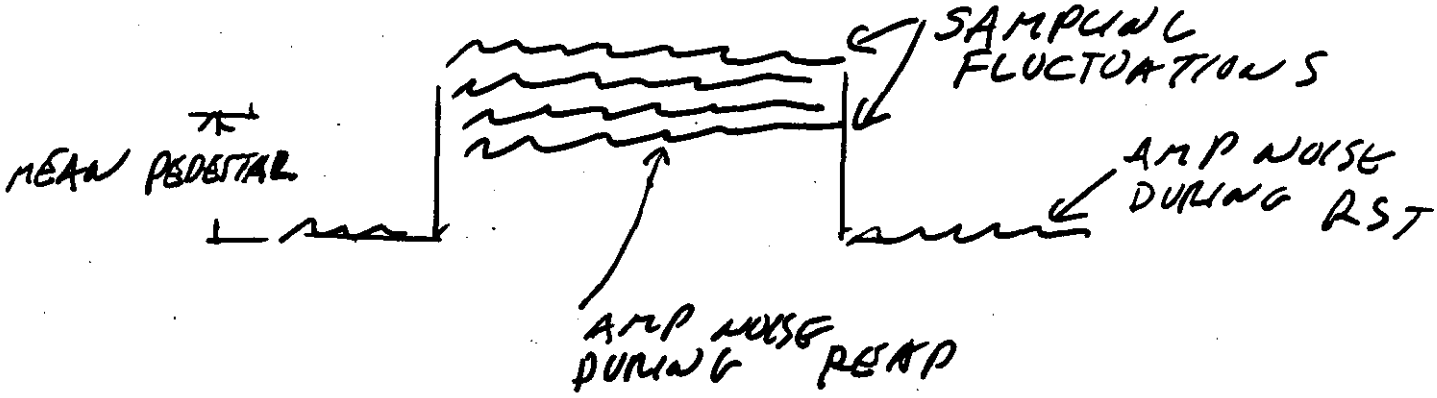
11402 DIGITIZING OSCILLOSCOPE
date: 8-OCT-92 time: 9:49:32

[exp:3.7,dig:3.91,dsy:3.3]
Instrument ID# B010270



TYP. PEDESTALS

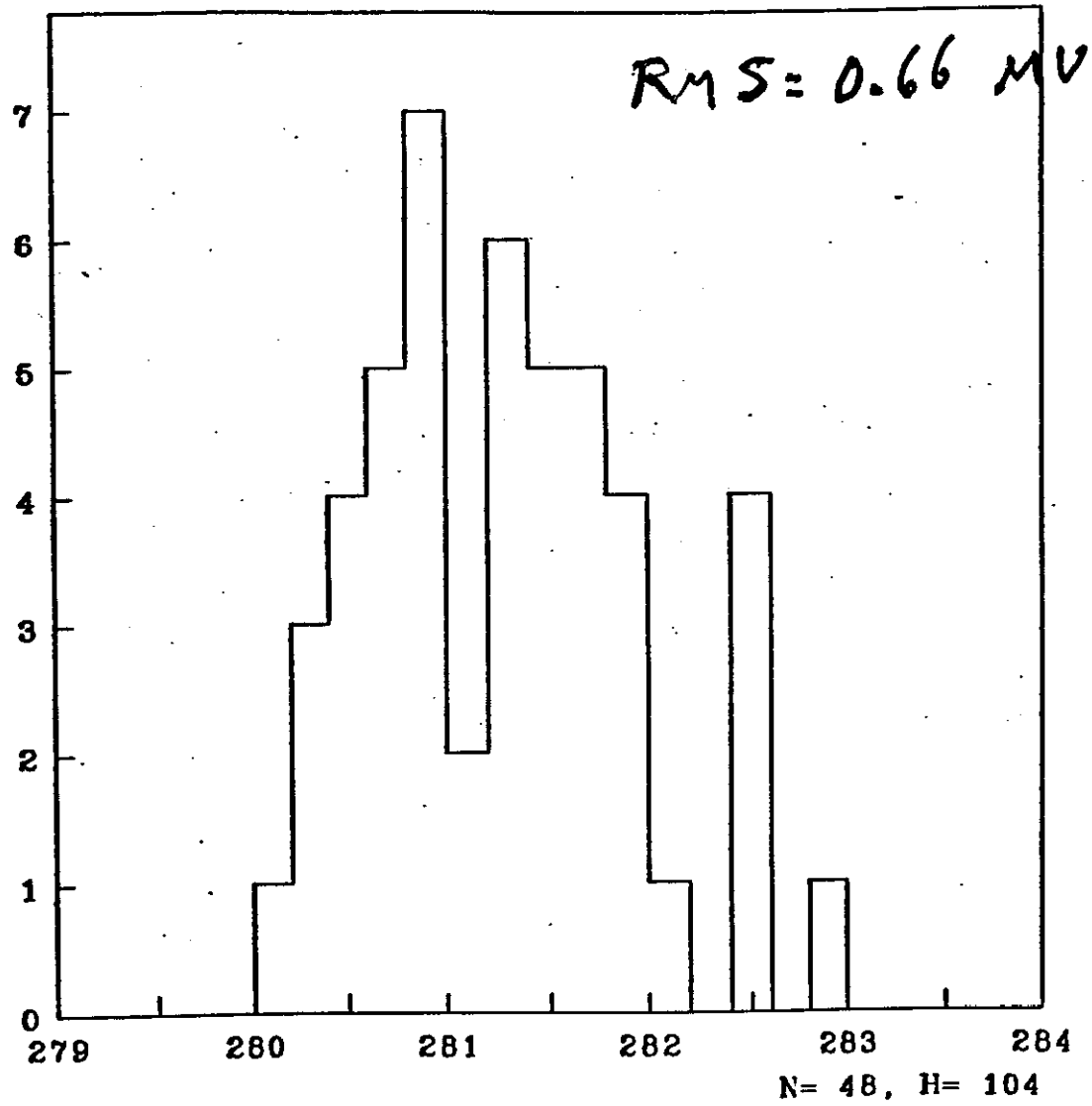




NOISE AT OUTPUT OF DIFFERENTIAL PIPELINE:

SAMPLING NOISE (AVG. CELL)	0.28 MV RMS
PEDESTAL DISTRIBUTION 48 CELLS	0.66 MV RMS
"MEASURING SYSTEM" NOISE WITH 12 BIT ADC	0.096 MV RMS

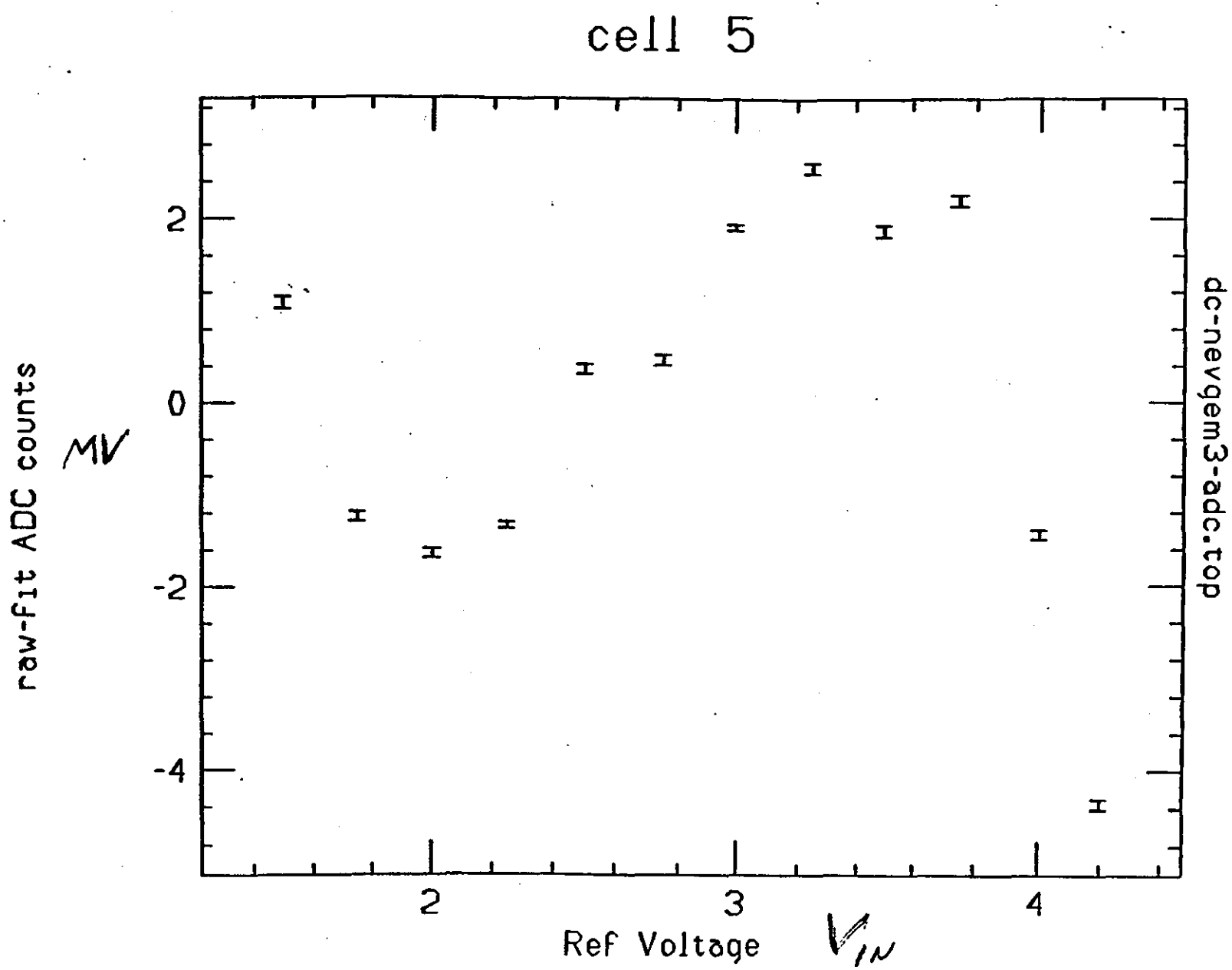
1992-11-03 12:51:04.10



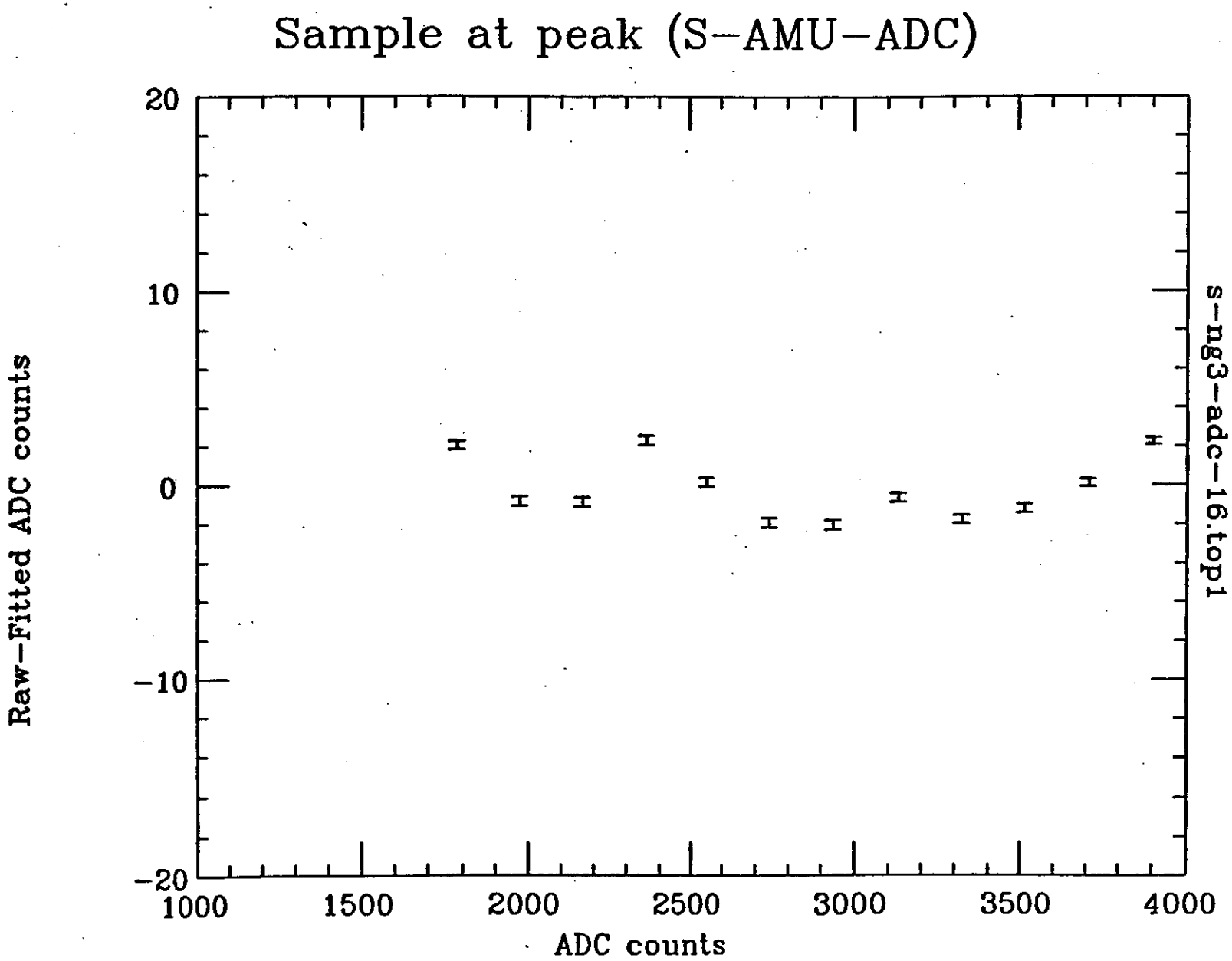
Pedestal Distribution (in MV)

VCOM-NEVGEM3-X5-ADC48

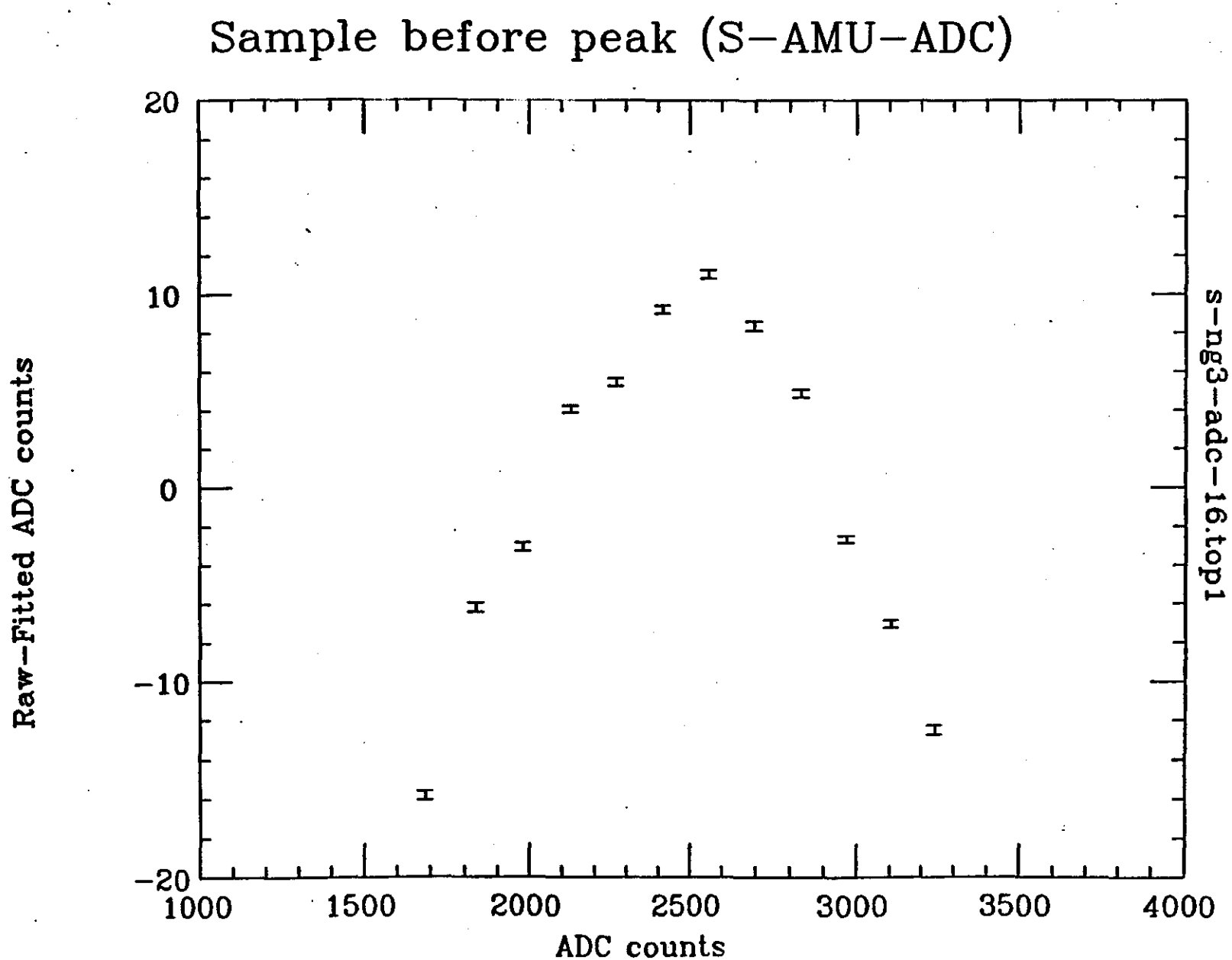
PEDESTALS



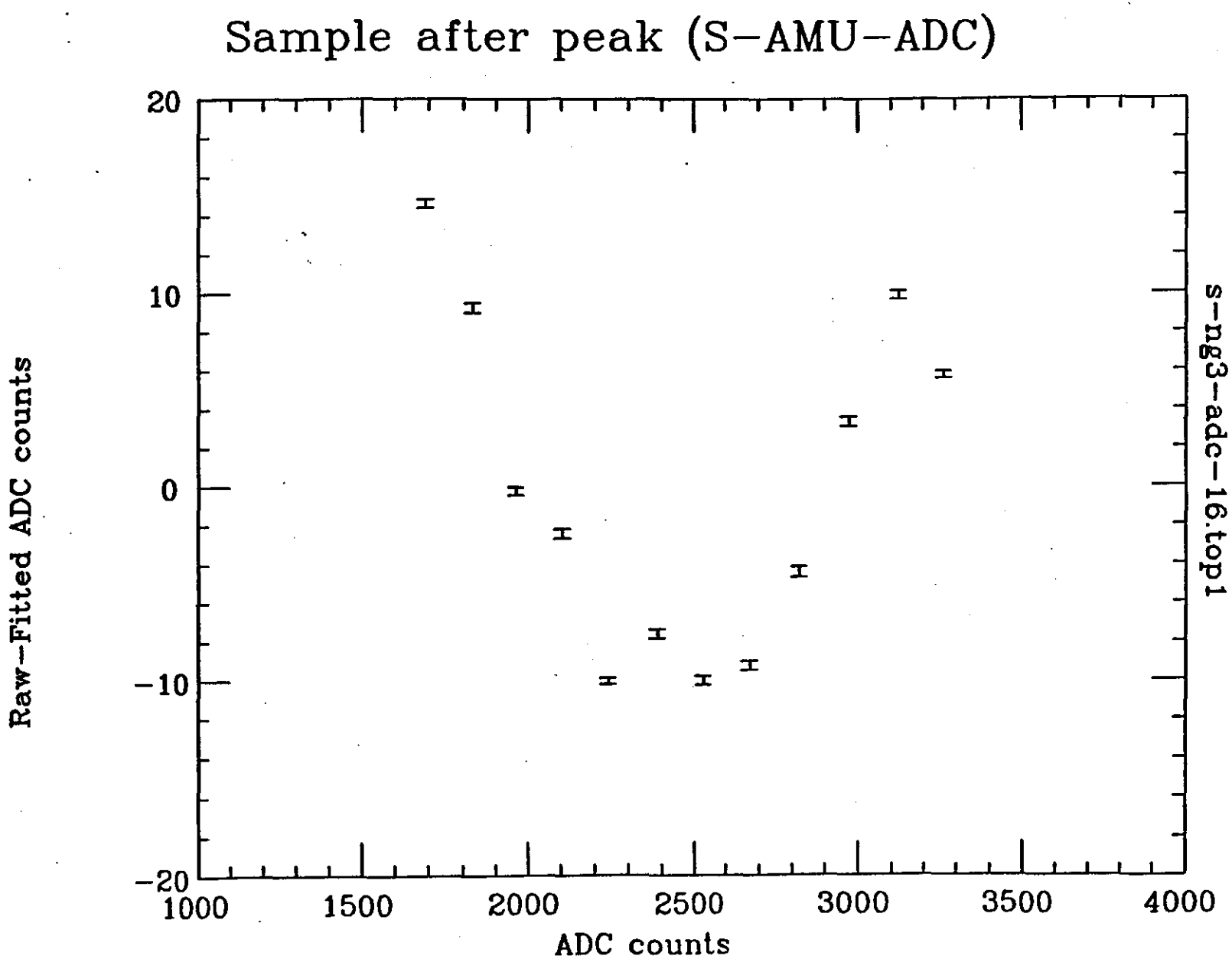
DC LINEARITY



LINEARITY FOR PEAK SAMPLE OF 40ns SHAPER



LINEARITY OF SAMPLE 16.6 ns BEFOR PEAK



LINEARITY OF SAMPLE 16.6 μS AFTER PEAK

COMPARISON OF AM AND HI SPEED ADC SOLUTIONS

ADVANTAGES OF AM SOLUTION:

1. REDUCES ADC SPEED FROM 60 MHZ TO 5 OR 10 MHZ.
2. ALLOWS MUX OF ADC FOR 8 CHANNELS.
3. ALL SAMPLES CAN BE CHOSEN FROM THE SAME GAIN SCALE.
4. LOWEST COST SOLUTION.
5. LOW POWER.
6. ACCESSABLE TECHNOLOGY - CMOS.

ADVANTAGES OF HI SPEED ADC SOLUTION:

1. NO ADDRESS SEQUENCE PERMUTATION NOISE AS WITH THE AM.
2. NO CELL NUMBER RELATED CALIBERATION CONSTANTS AS WITH THE AM.
3. POTENTIALLY BETTER LINEARITY FOR SAMPLES WITH LARGE dv/dt.
4. NO CELL NUMBER DEPENDENCE OF SAMPLING TIME AS WITH THE AM.
5. NO LIMIT IMPOSED ON LEVEL1 LATENCY.
6. NO LIMIT IMPOSED ON LEVEL1 RATE.
7. NO LIMIT IMPOSED ON TIME WINDOW.
8. PROVIDES DIGITAL INFORMATION FOR LEVEL1.

COMPARISON OF AM AND HI SPEED ADC SOLUTIONS

DISADVANTAGES OF AM SOLUTION:

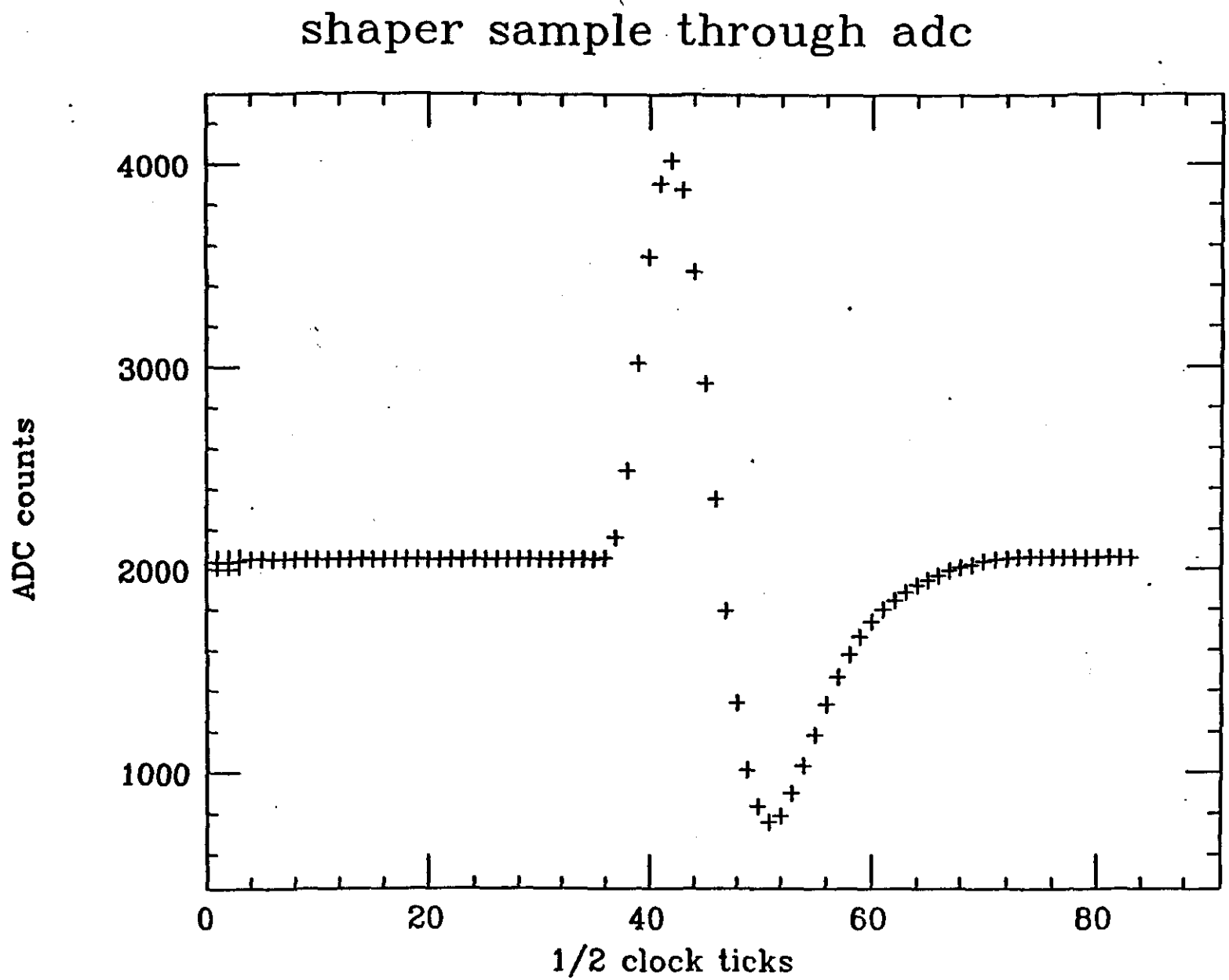
1. SIMULTANEOUS READ AND WRITE REQUIRES ADDRESS SWAPPING.
2. REQUIRES A LARGE NUMBER OF CALIBRATION CONSTANTS:

   CORRECTIONS FOR EACH OF 200 CELLS.
   CORRECTIONS FOR NON-LINEARITIES.

3. ADDRESS SEQUENCE PERMUTATIONS PRODUCE SYSTEMATIC NOISE THAT CANNNOT BE REMOVED BY CALIBRATION.
4. LEVEL1 LATENCY IS LIMITED TO A FEW MICROSECONDS.
5. LEVEL1 RATE IS LIMITED BY THE ADC TIME.
6. THE TIME WINDOW IS LIMITED TO ABOUT 5 SAMPLES.
7. INFORMATION FOR LEVEL1 MUST BE PROCESSED SEPARATELY.

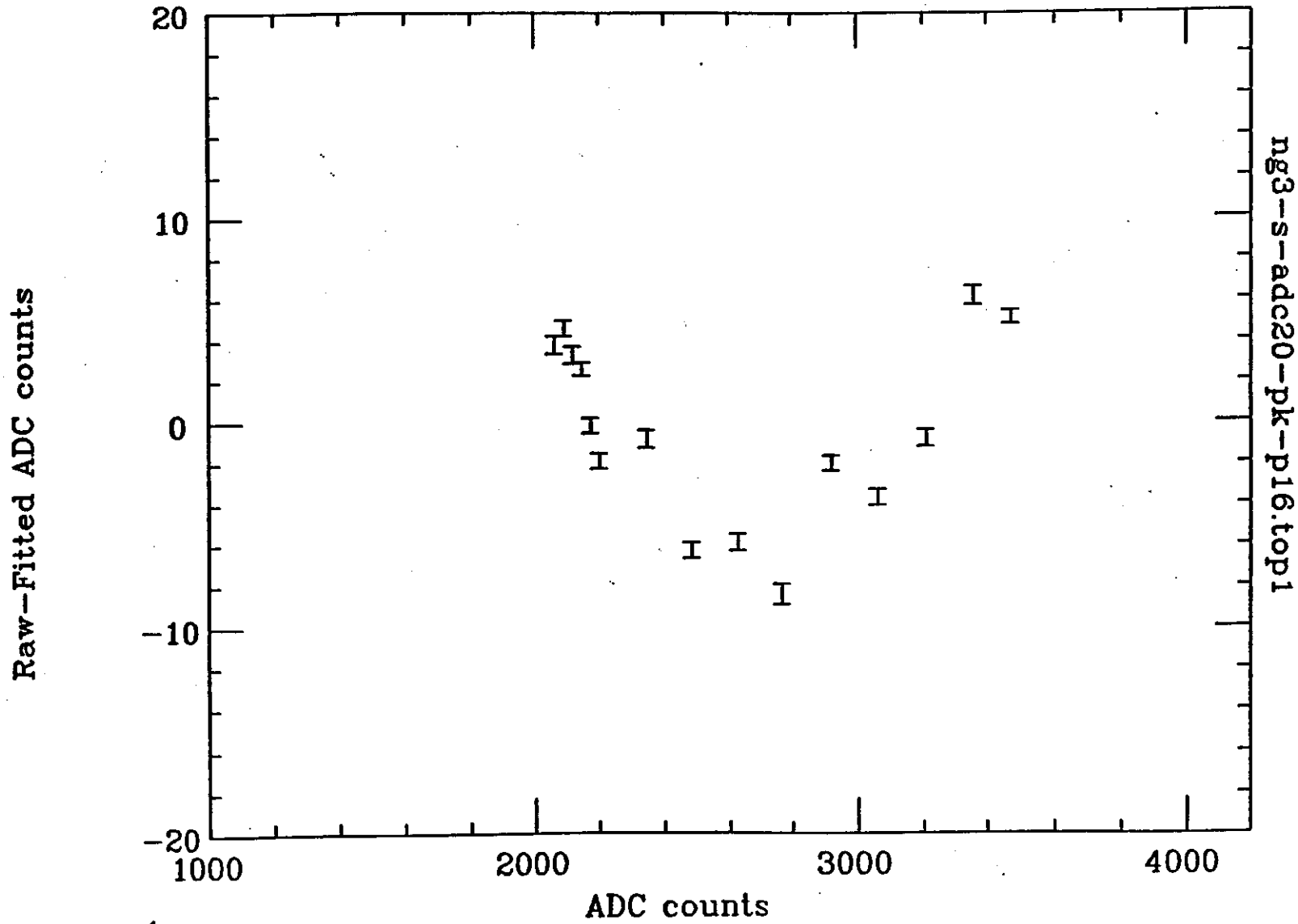
DISADVANTAGES OF HI SPEED ADC SOLUTION:

1. REQUIRES 60 MHZ 10 TO 12 BIT ADC.
2. REQUIRES DYNAMIC RANGE SPLITTING.
3. NO SHARING OF INPUTS WITH THE ADC.
4. HIGHER COST.
5. HIGHER POWER.
6. DEPENDS ON LESS ACCESSIBLE TECHNOLOGY (BIPOLAR OR BICMOS).

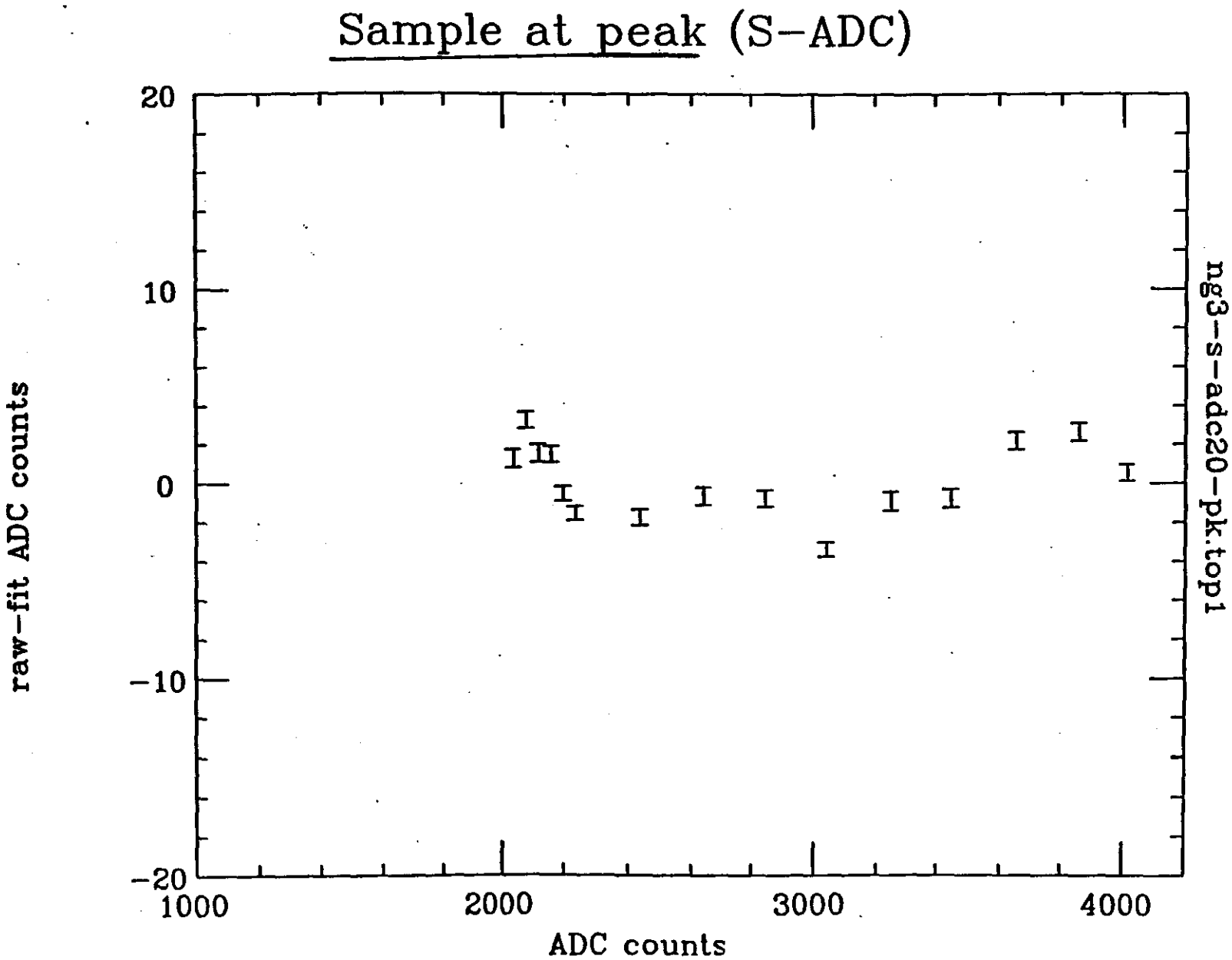


RESPONSE OF SPT 30MHZ, 12BIT ADC TO 40 ns SHAPER

Sample after peak (S-ADC) 84 16.6 nS

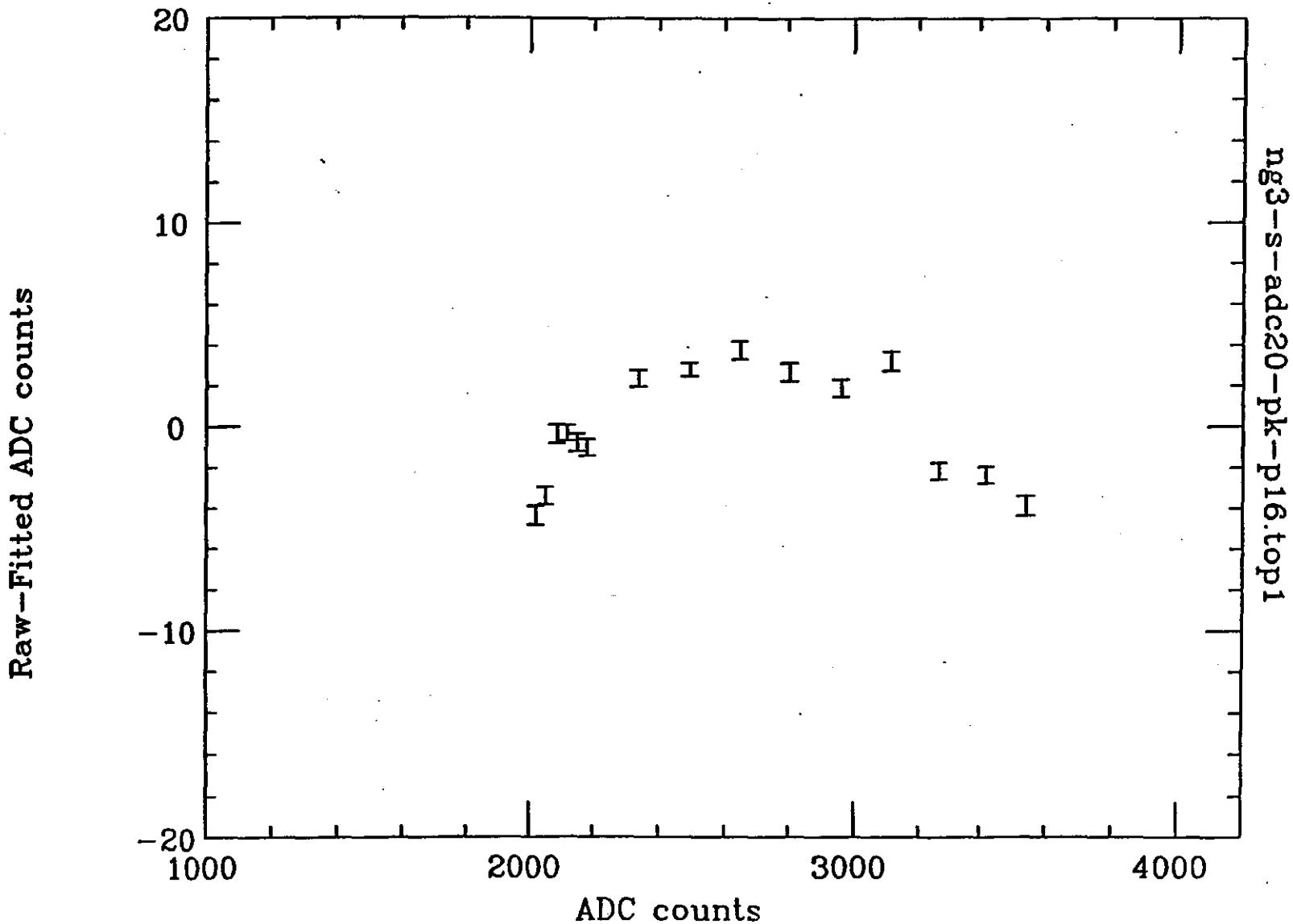


LINEARITY OF SPT 30MHZ ADC WITH 4ns SHAPER



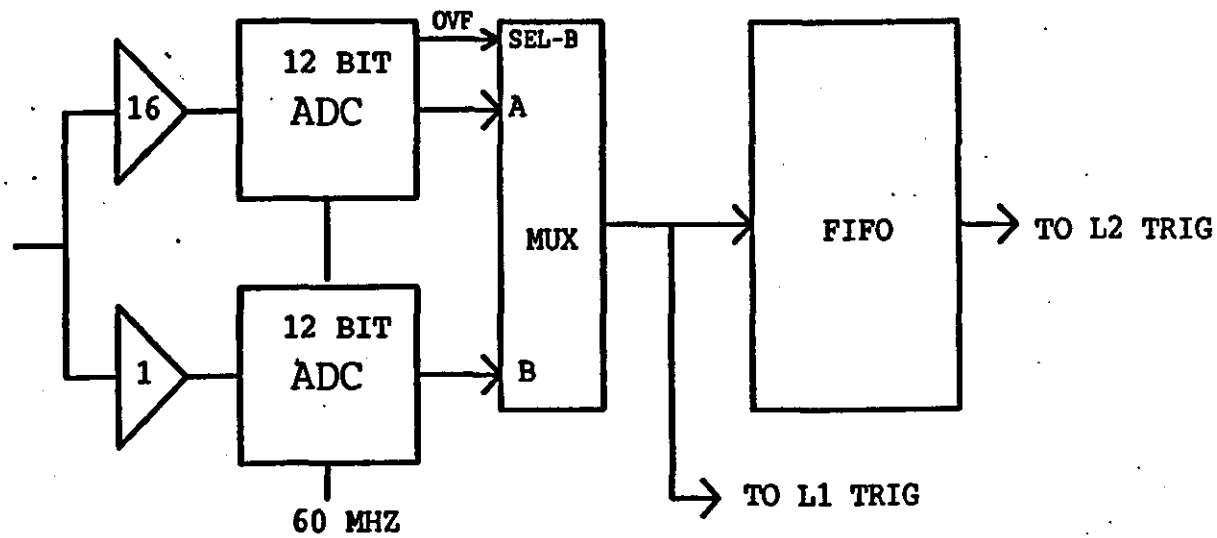
LINEARITY OF SPT 30MHZ ADC WITH 40NS SHAPER

Sample before peak (S-ADC) BY 16.6 μS



LINEARITY OF SPT 30MHZ ADC WITH 40μS SHAPER

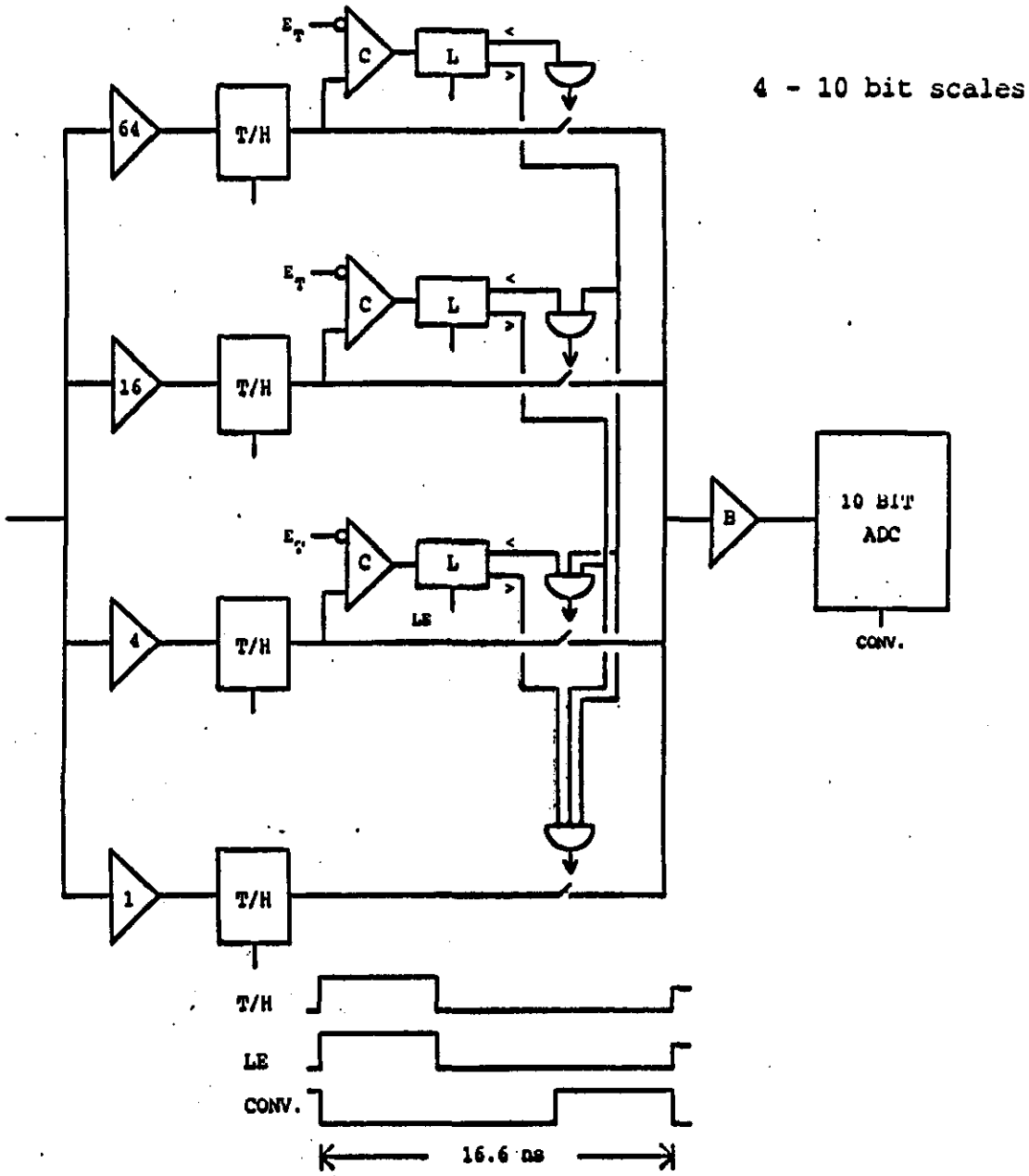
ADC1



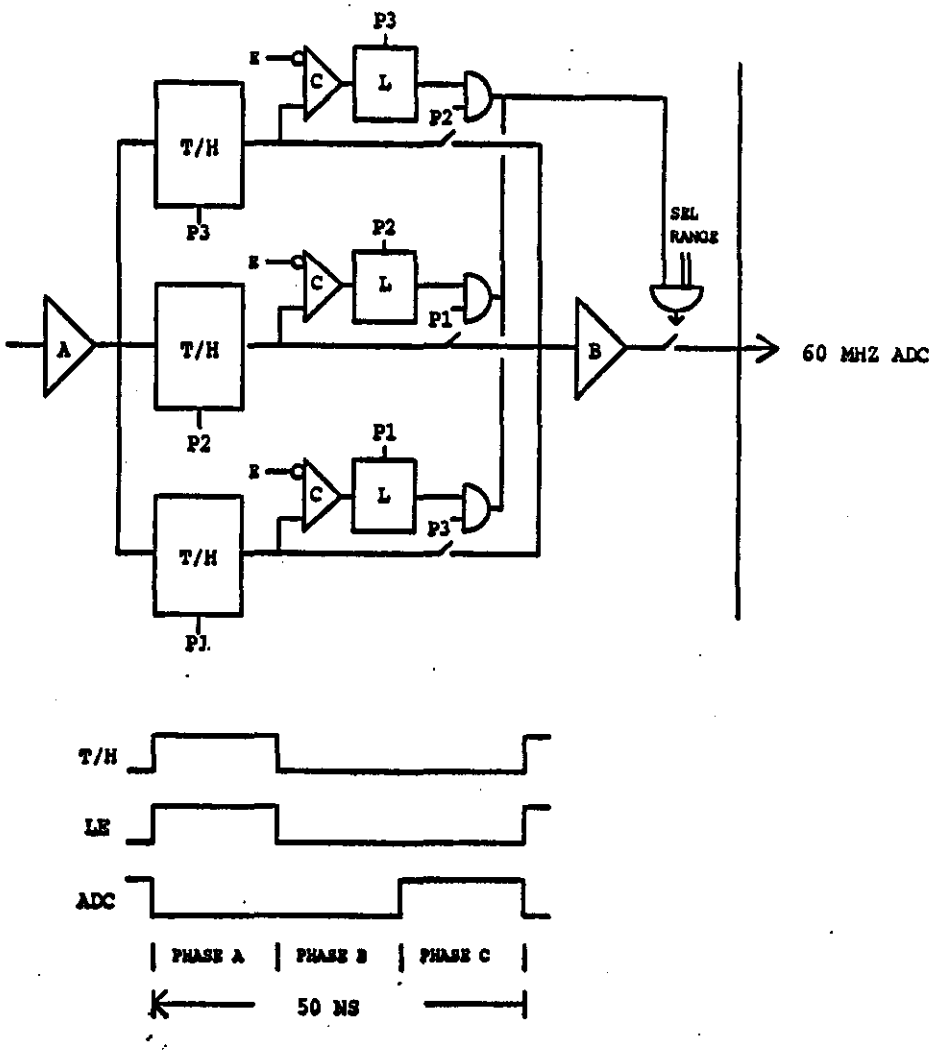
60 MHZ ADC

CLASSIC SOLUTION
TO DIRECT ENCODING

ADC3



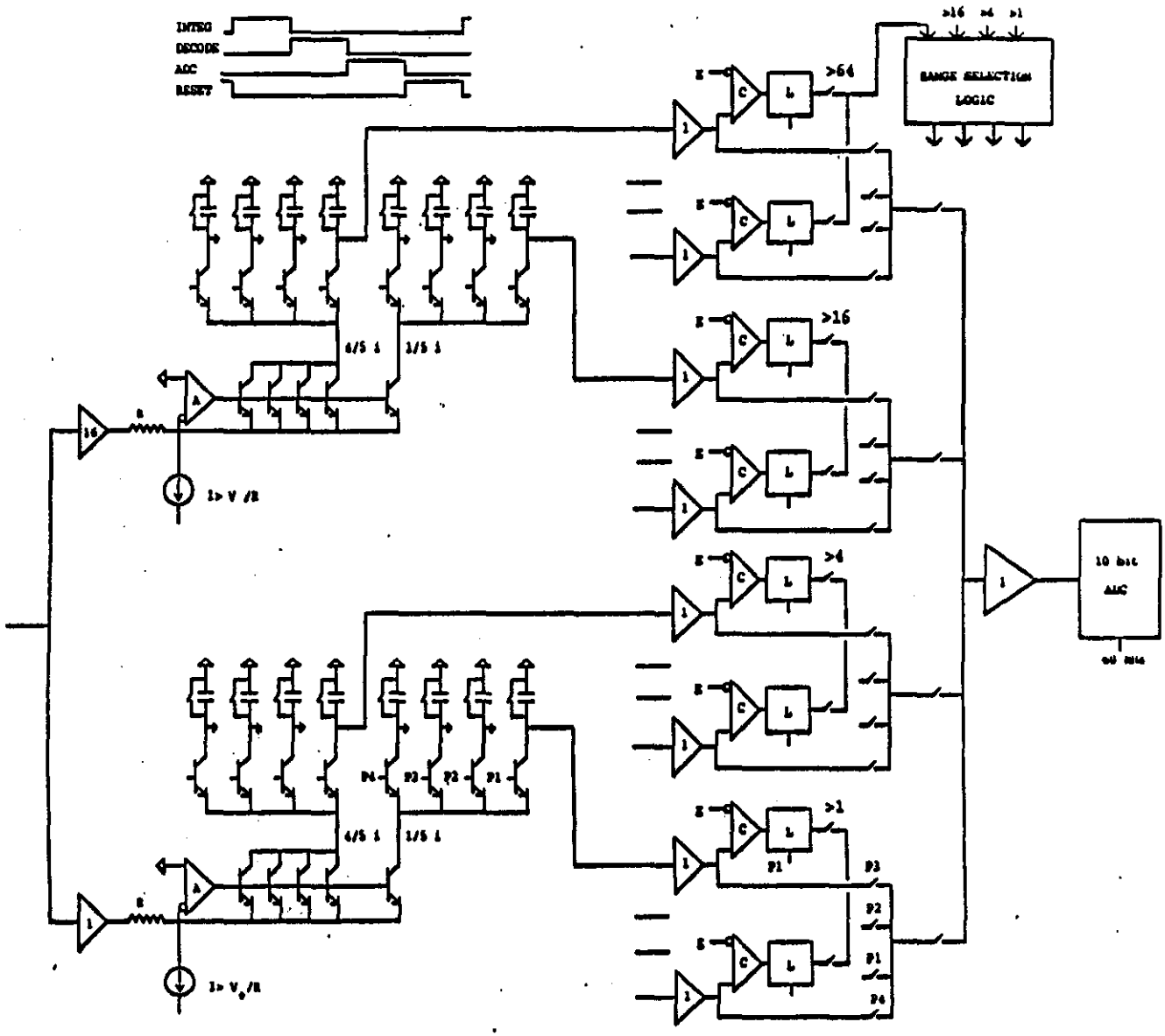
MUX RANGE SPLITTING
TO REDUCE NO. OF ADC'S AND NO BITS



THREE 16.6 ns PHASES TO INCREASE T/H AND RANGE DECISION TIME

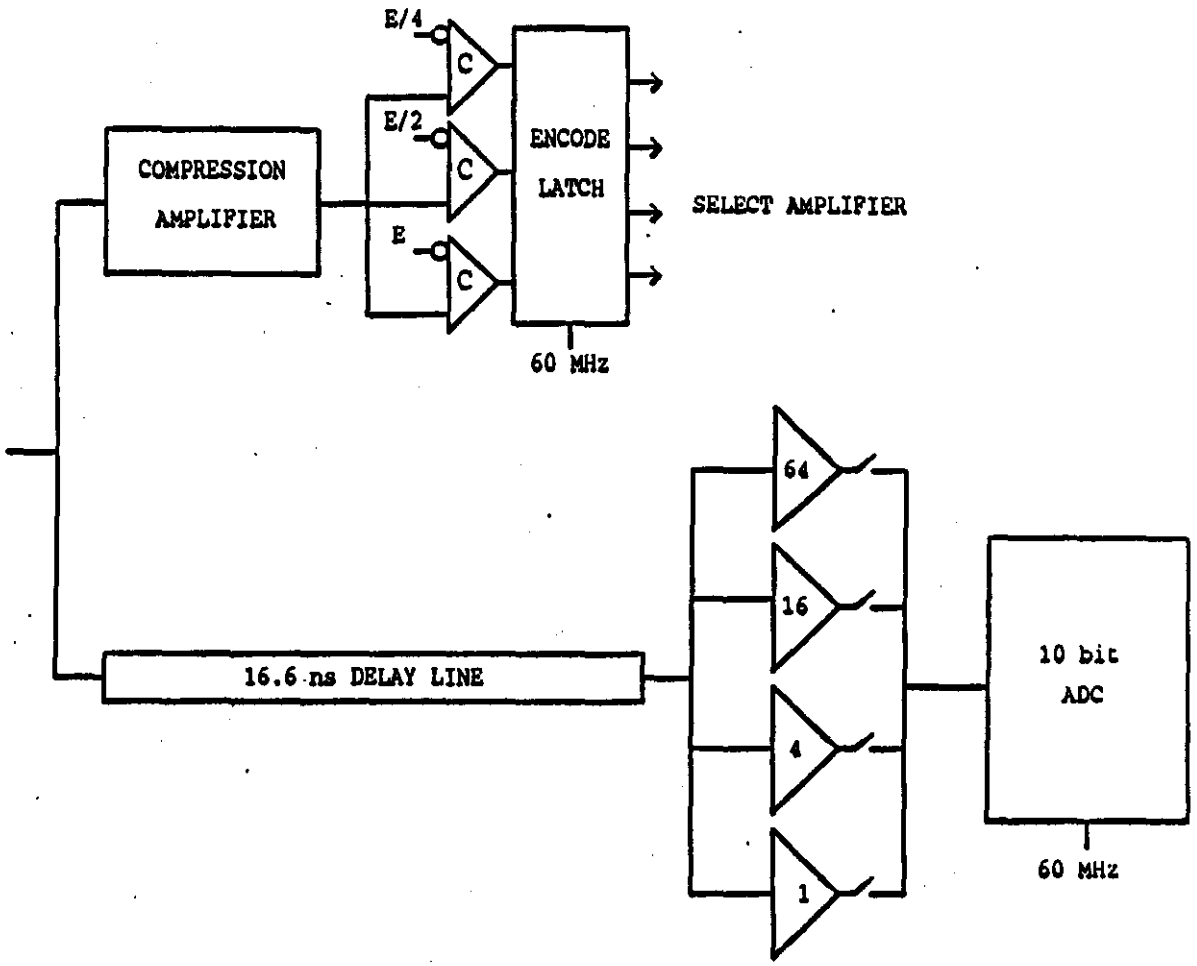
MULTIPLE PHASES TO PROVIDE MORE SET UP TIME FOR THE META-STABLE LATCH STATES AND ALSO MORE, TRACKING TIME FOR THE T/H'S.

CURRENTSPLITTER BASED ON FERMILAB SCHEME



INTEGRATION OF SIGNAL DURING SAMPLING INTERVAL VS VOLTAGE SAMPLING, TO SIMPLIFY HARDWARE.

BASED ON FERMILAB SCHEME.



PIPELINED RANGE SELECTION

SUMMARY

AMU DEVELOPMENT:

1. OUR FIRST GOAL IS TO FULLY UNDERSTAND THE SYSTEMATIC ERRORS RELATED TO ADDRESS SEQUENCE , ADDRESS SETUP TIME , AND COUPLING BETWEEN READ AND WRITE PROCESSES.

2. THIS REQUIRES BUILDING ADDITIONAL TEST CHIPS TO SEPERATE SUBSTRATE NOISE INDUCED BY CURRENTS THROUGH THE PACKAGE LEADS , AND NOISE INDUCED BY ON CHIP SWITCHING.

3. WE ARE CURRENTLY DEVELOPING AN OUTPUT BUFFER AMP TO EASE THE PROBLEM OF INTERFACING TO THE EXTERNAL ADC.

4. WHEN THESE ISSUES ARE RESOLVED WE WILL BUILD THE FULL SIZE , 8 DIFFERENTIAL , 200 CELL PROTOTYPE CHIP THRU ORBIT FORESIGHT.

DIRECT DIGITIZATION AT 60 MHz:

1. WE ASSUME FOR NOW THAT INDUSTRY CAN SUPPLY 10 BIT 60 MHz ADC'S WITH AFFORDABLE COST AND POWER REQ.

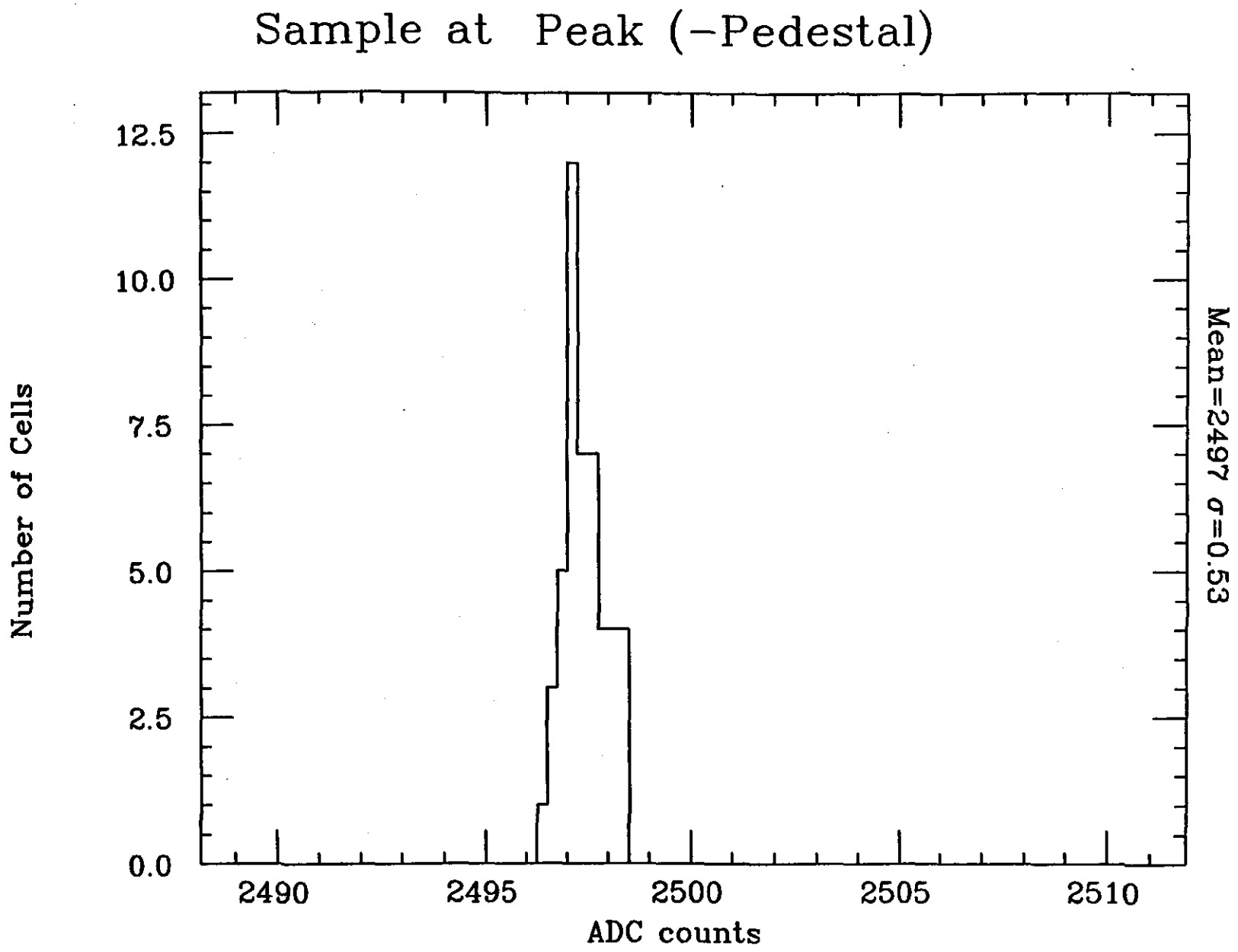
2. WE WILL DEVELOP A RANGE SPLITTER AS AN ALTERNATIVE TO THE AM , BASED ON AN ACCESSABLE (TO US) TECHNOLOGY.

3. WE ARE PURCHASING DESIGN TOOLS FROM TEKTRONIX FOR THEIR CUSTOM PROCESS.

4. THE ORBIT 2 BICMOS PROCESS (USED AS A DEVELOPMENT TOOL BY FERMILAB FOR THEIR DIGITAL P.M.) IS AVAILABLE TO US THRU FORESIGHT.

TEST MODULE DEVELOPMENT:

WE WILL BUILD A MULTI-CHANNEL AMU - ADC TEST MODULE BY THE END OF '93 TO TEST THE SYSTEM FEATURES.THIS WILL INCLUDE CONTROL , DIGITAL BUFFERING , AND OUTPUT LINK.


Sample at Peak (−Pedestal)
Number of Cells
12.5
10.0
7.5
5.0
2.5
0.0
2490
2495
2500
2505
2510
ADC counts
Mean=2497 σ=0.53

gem

γeμ

Presentation by:

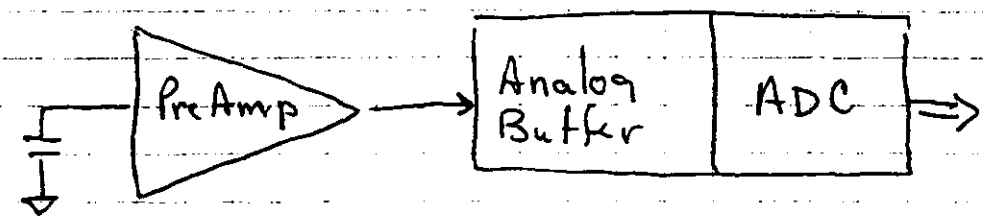
R. L. Wixted

CSC READOUT

REQUIREMENTS & OPTIONS

R. L. Wixted
Princeton Univ.
5 NOV 1992

CSC Readout Schematic



- Analog Buffer Requirements
- ADC Options

CSC Requirements Summary

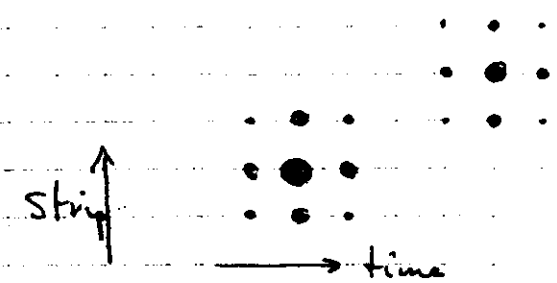
Average Neutron Rate

$$\bar{n} = \bar{F}_n A \epsilon_n = (2\times10^5)(.5\times200)(3\times10^{-4}) = 6000 \text{ neutrons/sec}$$

Probability of Interference

$$P_{total} = m\sum_{n=1}^{\infty}\frac{(\bar{n}\tau)^n}{n!}\exp(-\bar{n}\tau) \simeq m\bar{n}\tau_s = (21)(6000)(10^{-7})$$

$$= 0.013$$



Estimation Accuracy

$$\left(\frac{\sigma_x}{x}\right)^2 = (2+3s^2)\left(\frac{\sigma_q}{Q}\right)^2 \leq 2.75\left(\frac{\sigma_q}{Q}\right)^2$$

$$\text{Spatial SNR} \geq \sqrt{2.75}\left(\frac{5}{.05}\right) = 166$$

$$\text{temporal SNR} \geq \sqrt{2.75}\left(\frac{8}{.1}\right) = 133$$

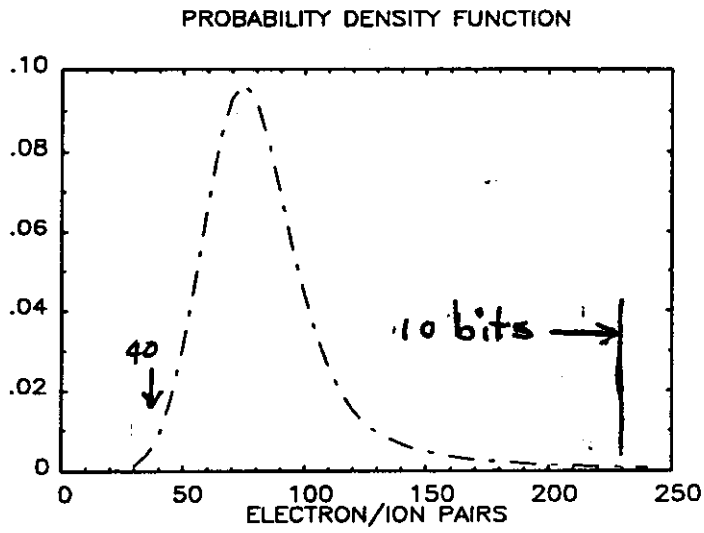
Signal Amplitude Range

Min = 40 Max = 230 Ion pairs

Dynamic Range

$$\text{Full scale SNR} = 166\left(\frac{230}{40}\right) = 954 \quad (10 \text{ bits})$$

CSC Readout Amplitude Density Function



after Marlow

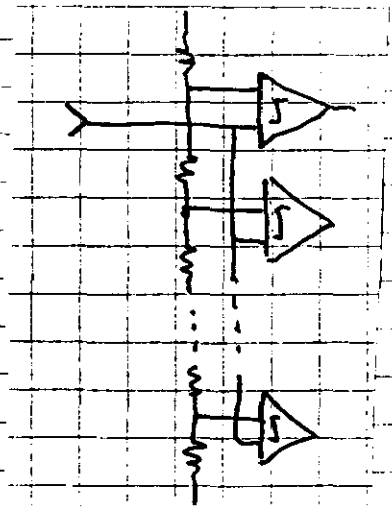
SCA Requirements

Sample Period (8 crossings)	128 nsec
Buffer Length	36 samples
- Pending Level 1	16
- Pending ADC*	20
Readout rate	500 Ks/s
Dynamic range	10 bits
Channels/chip	Lots

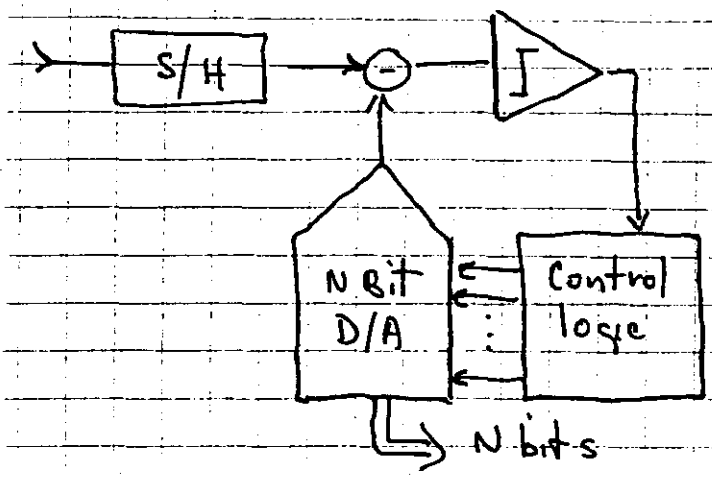
* 4 sample sets, 5 samples/set (.99999 coverage)

Assorted ADC Concepts

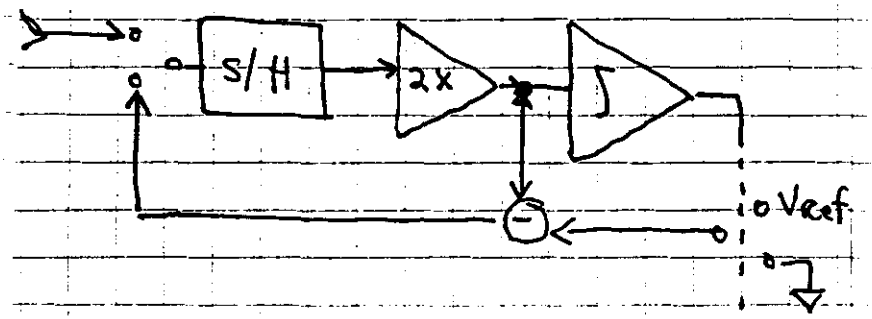
Flash



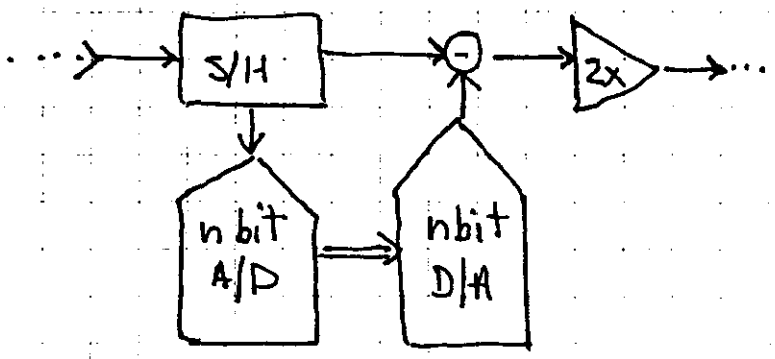
Successive Approx



Algorithmic

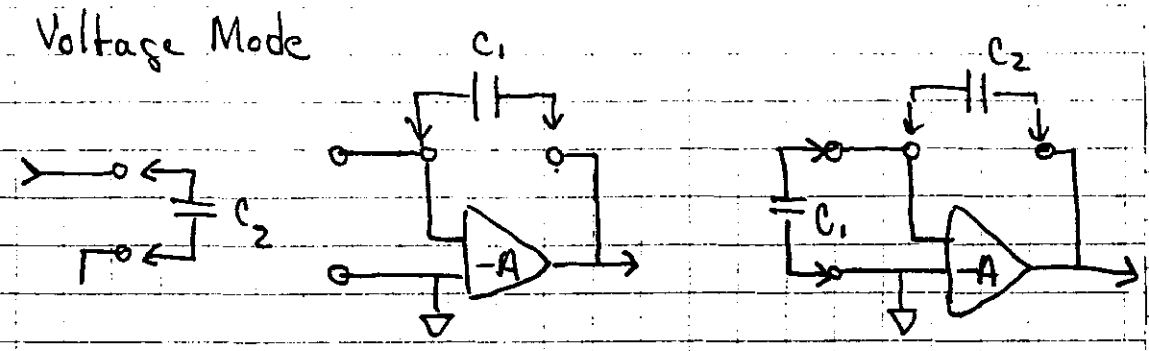


Pipelined

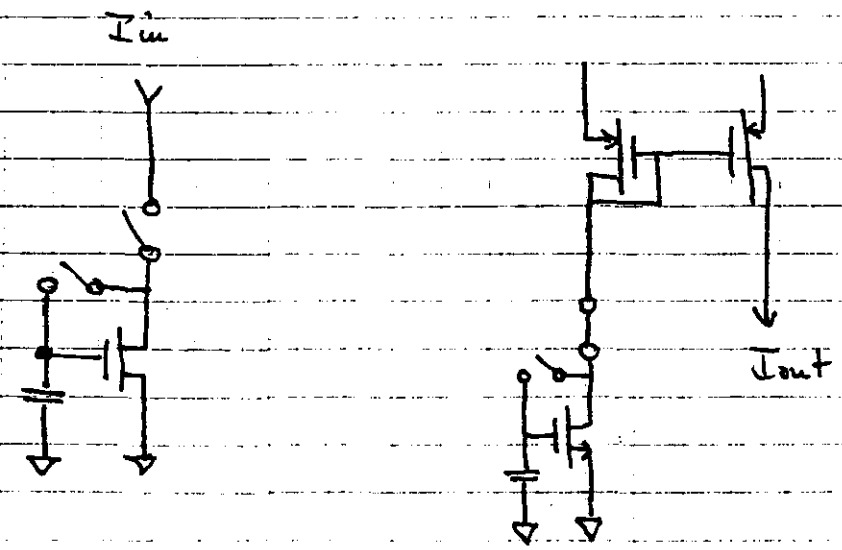


Analog Storage Modes

Voltage Mode



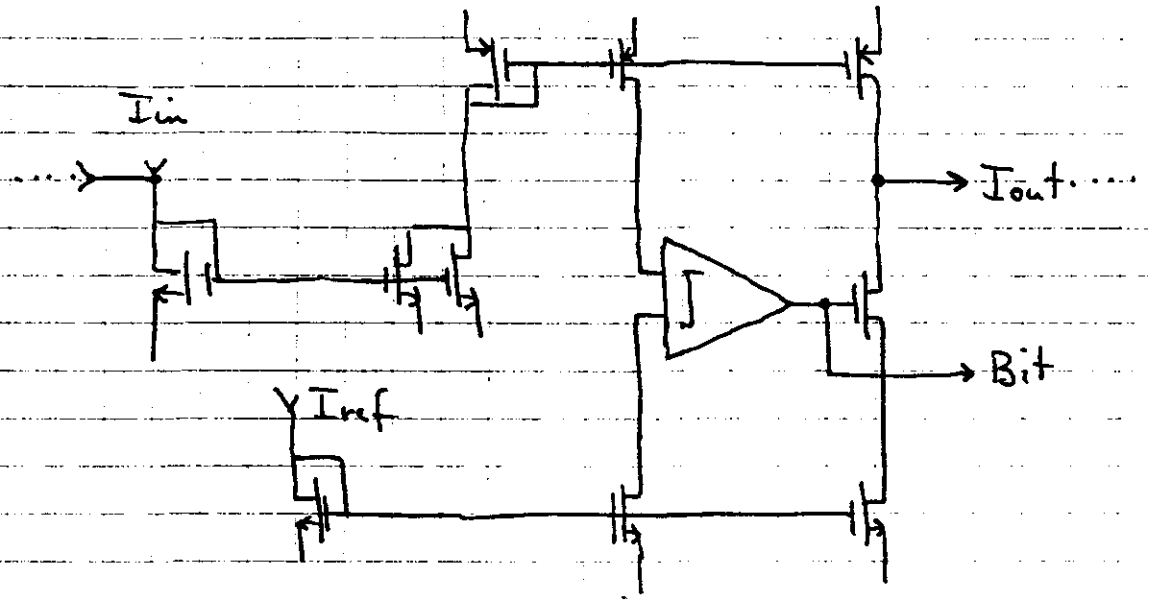
Current Mode



Storage Cell

Readout

Pipelined Current Mode Cell



gem

γeμ

Presentation by:

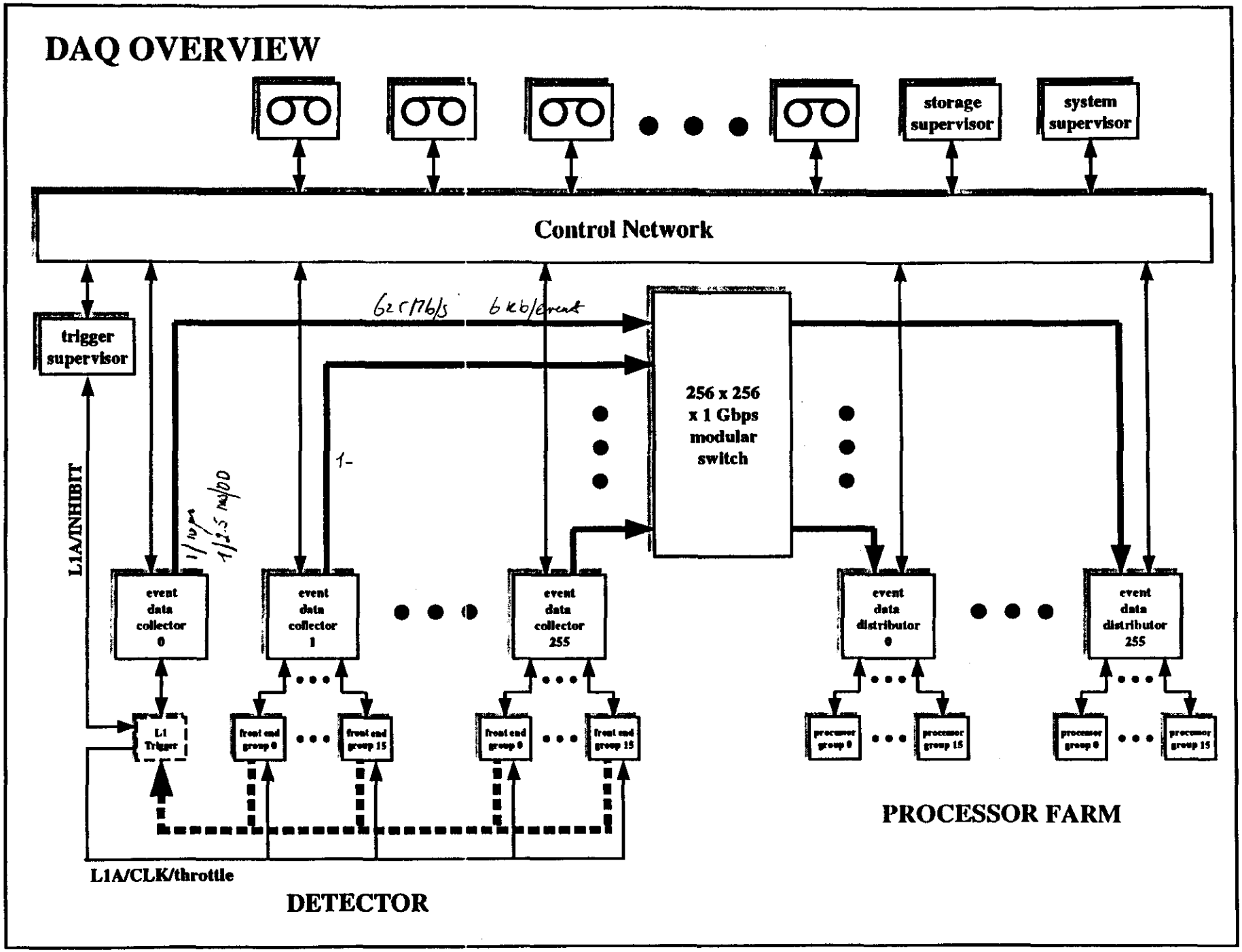
J. Dorenbosch

SUB-SYSTEM DATA RATES

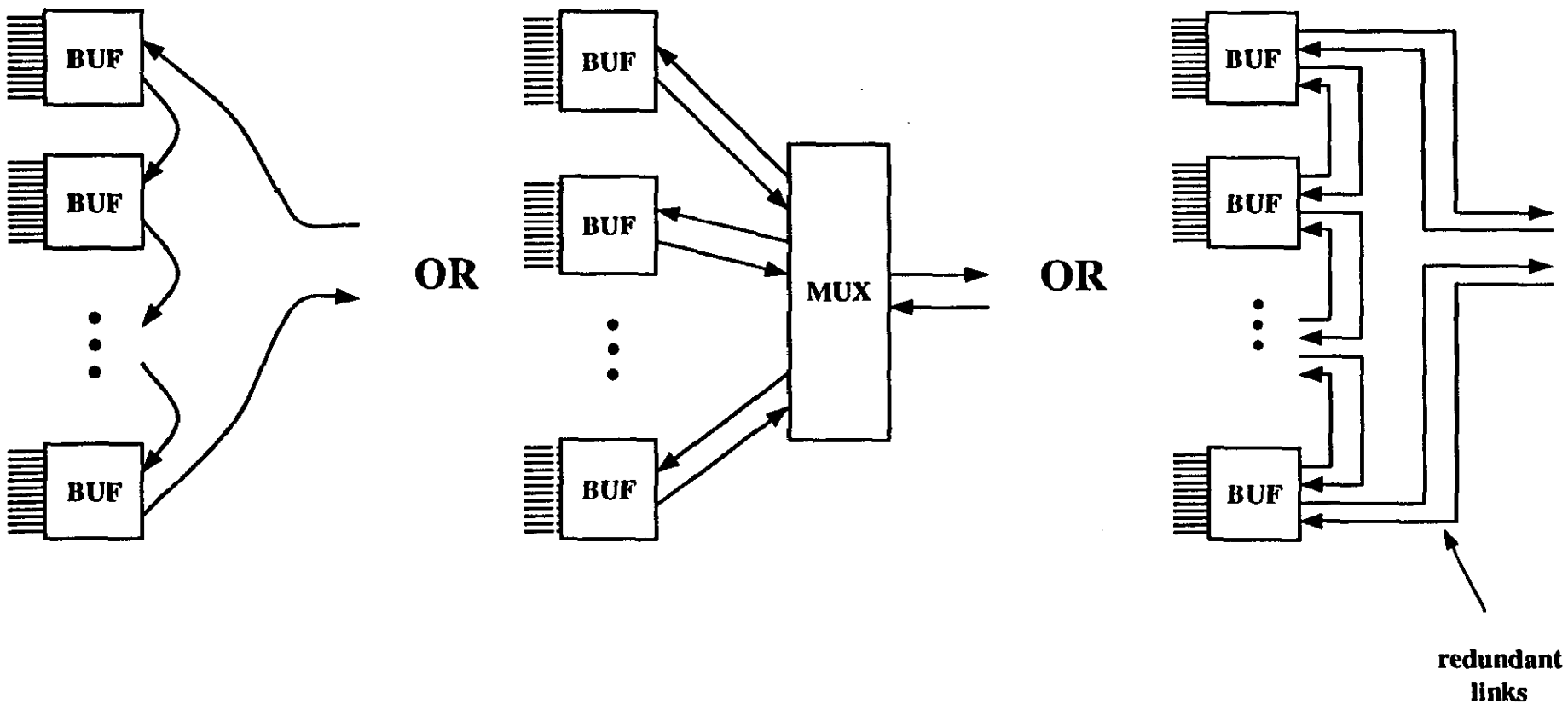
SUB-SYSTEM	CHANNELS	EVENT SIZE	DATA RATE @100 KHz TRIGGER RATE
CALORIMETER	82 K	50 KB	5 GB/s = ~~67~~ EDC
IPC	446 K	80 KB	8 GB/s 108
SILICON	3230 K	20 KB	2 GB/s 29
MUON	518 K	40 KB	4 GB/s 54
TOTAL	4276 K	190 KB	19 GB/s 256

19 GB ≈ 150 Gb ≈ 256 1 Gb fibers
≈ 2,560 100 Mb fibers

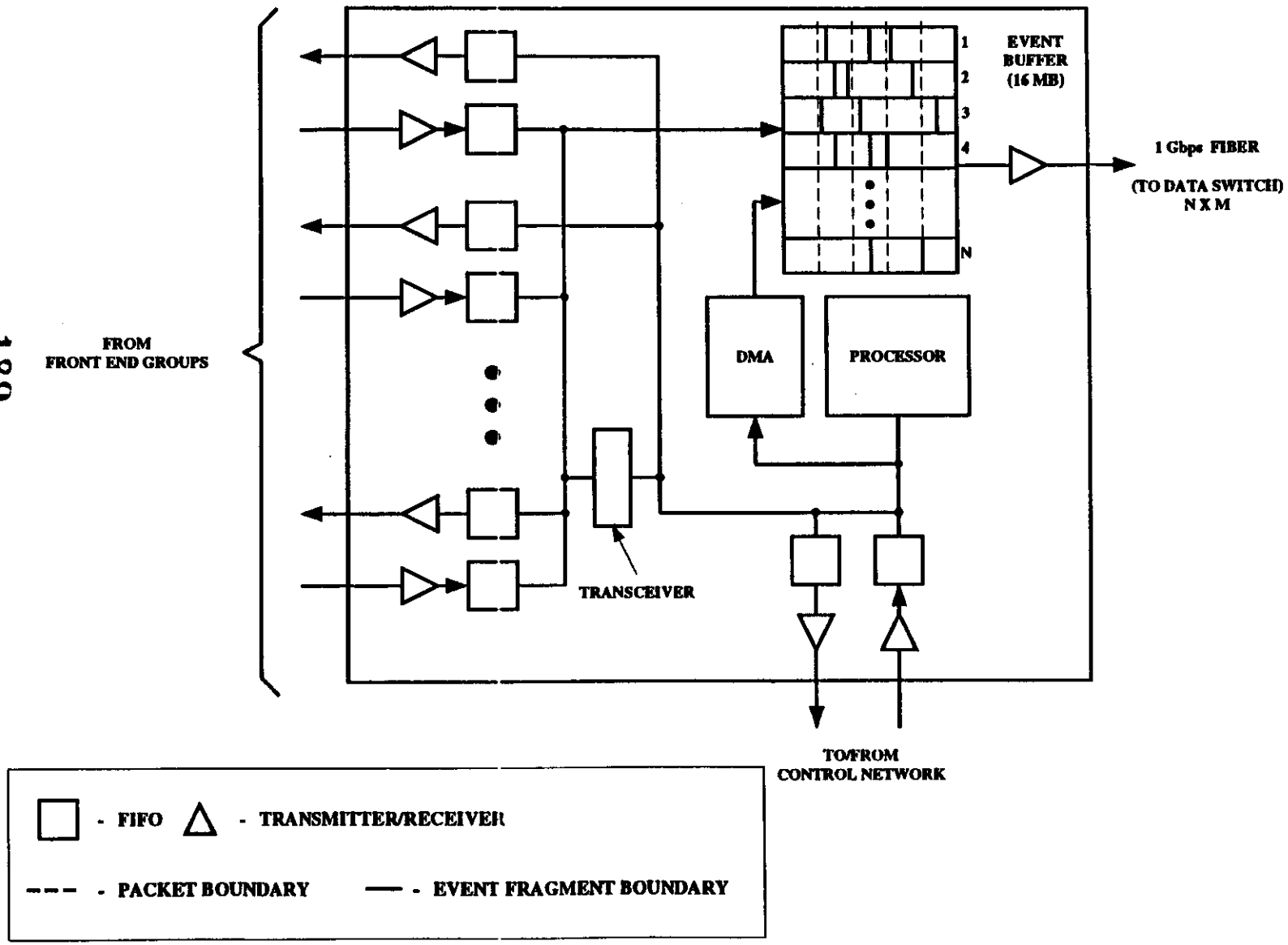
1 EDC = 19 GB / 74 kB/s


DAQ OVERVIEW
storage supervisor
system supervisor
Control Network
trigger supervisor
L1A/INHIBIT
256 x 256 x 1 Gbps modular switch
event data collector 0
event data collector 1
event data collector 255
event data distributor 0
event data distributor 255
L1 Trigger
front end group 0
front end group 15
processor group 0
processor group 15
L1A/CLK/throttle
DETECTOR
PROCESSOR FARM

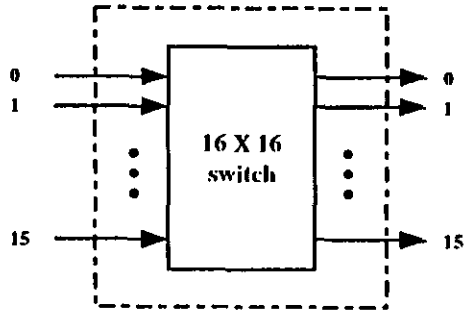
FRONT END GROUP

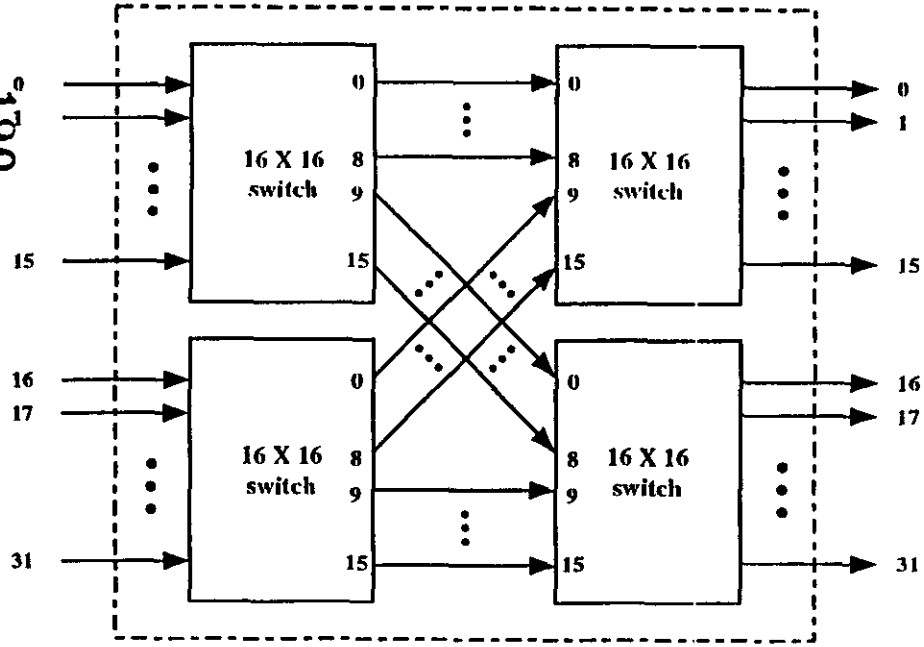


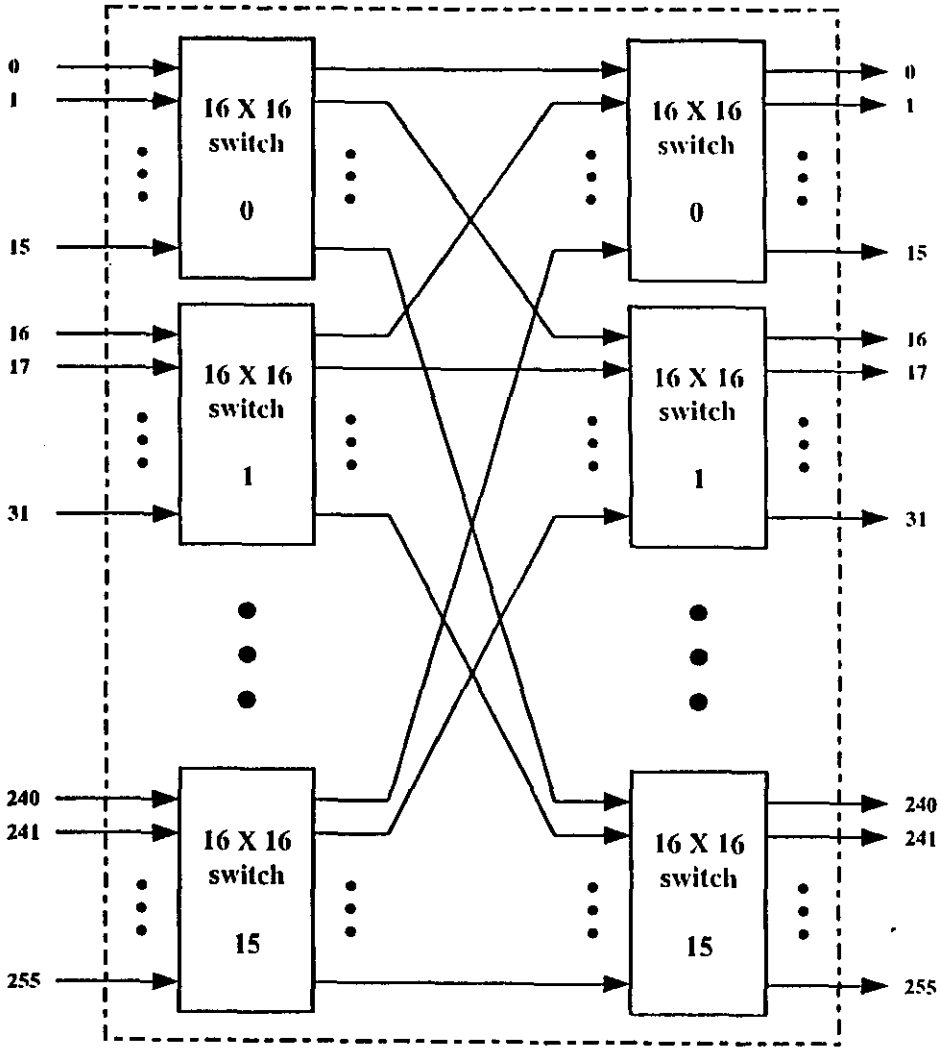
EVENT DATA COLLECTOR



MODULAR SWITCH DESIGN

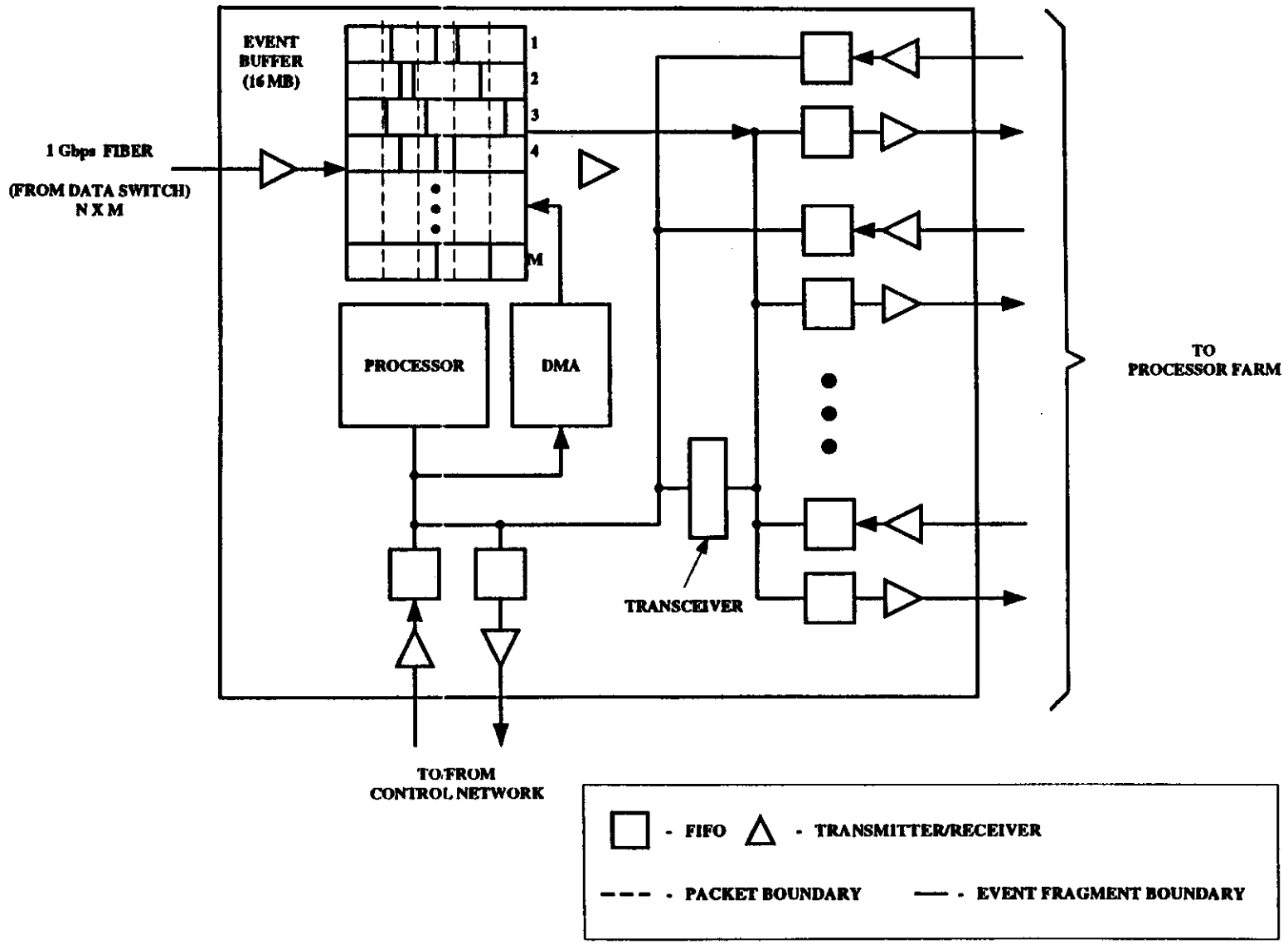




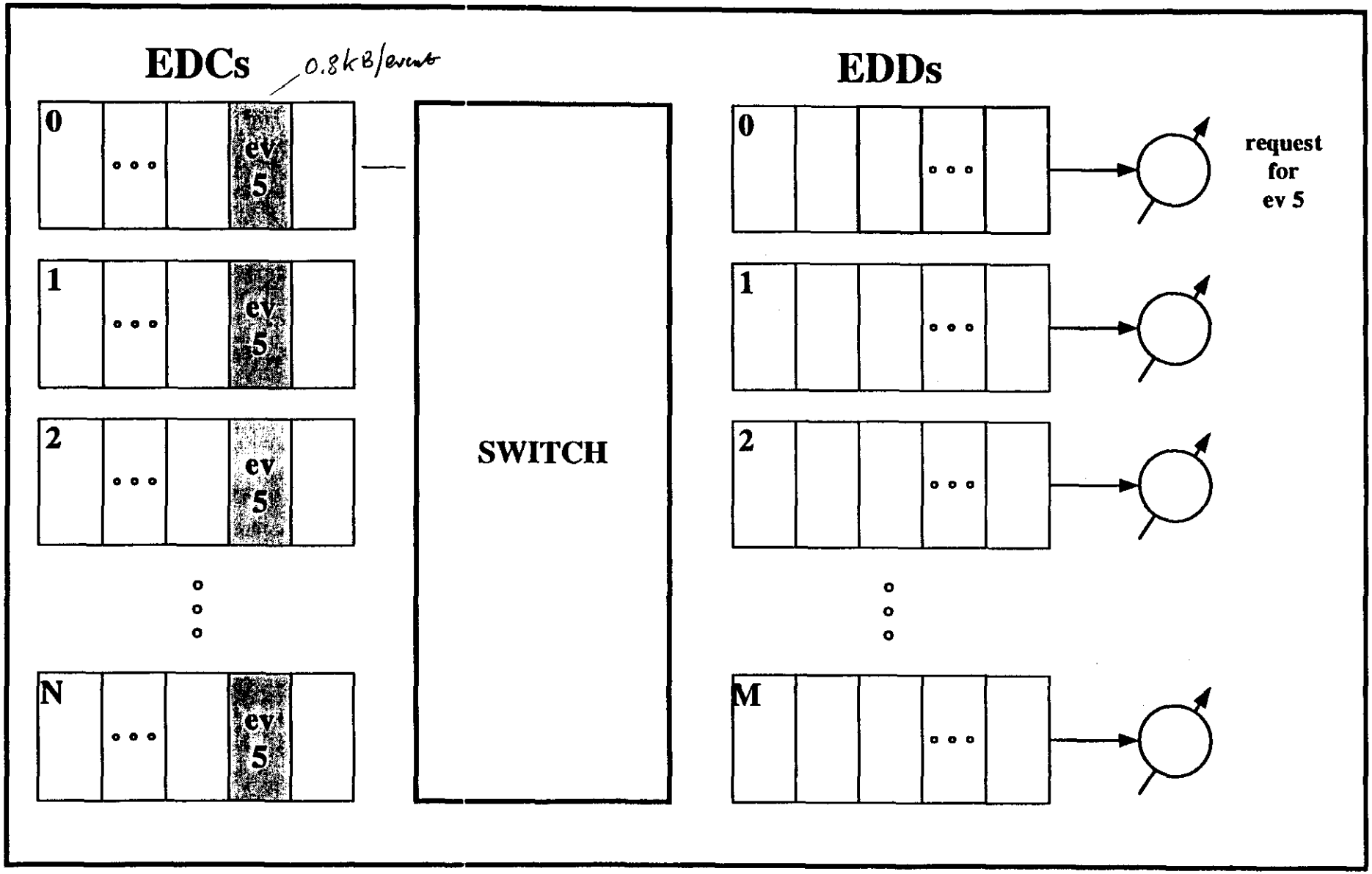


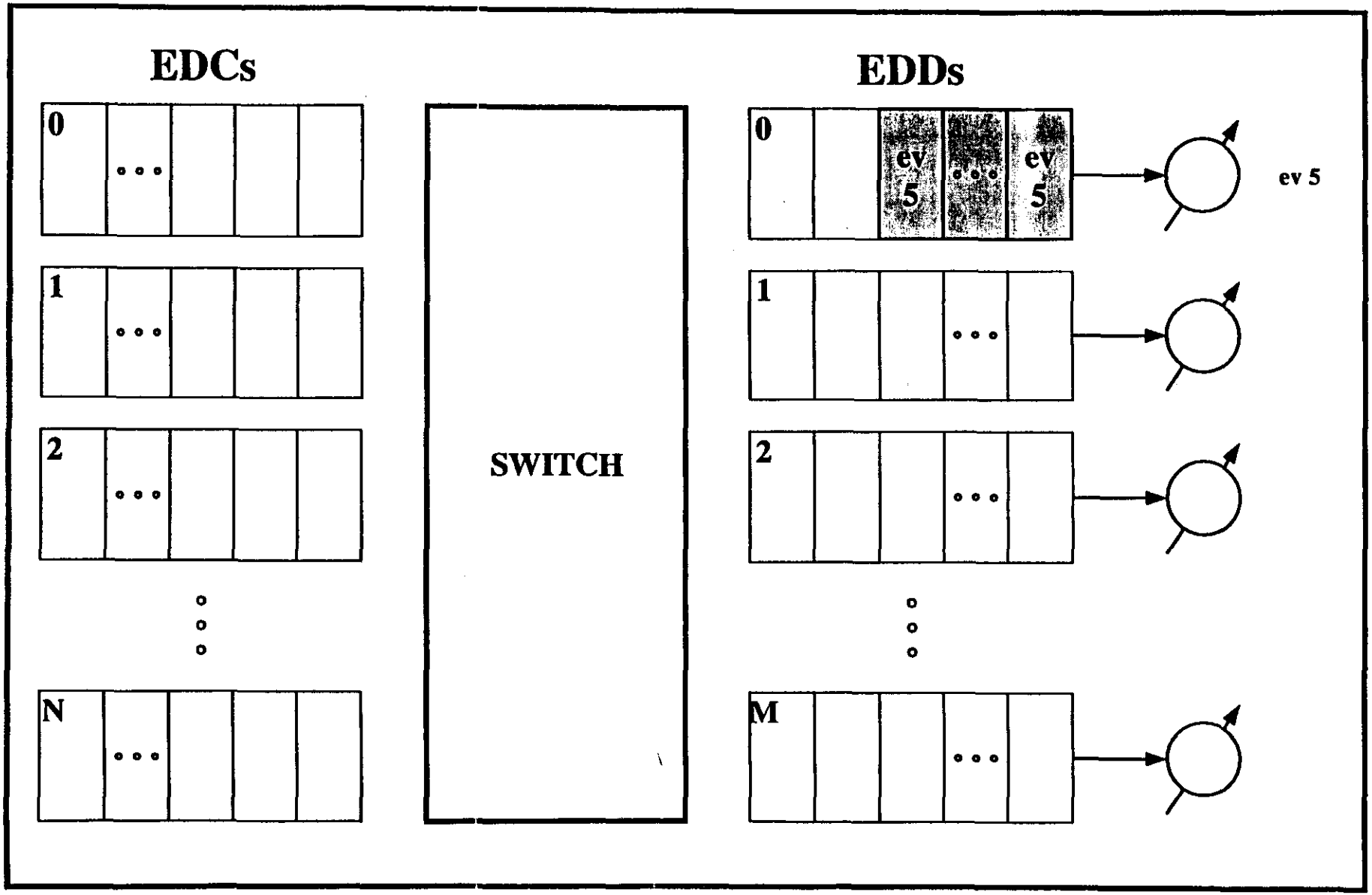
TIME DIVISION MULTIPLEXED SWITCH
(256 CHANNELS @ 1 Gbps)
IMPLEMENTING 65,536
VIRTUAL CHANNELS @ 4 Mbps

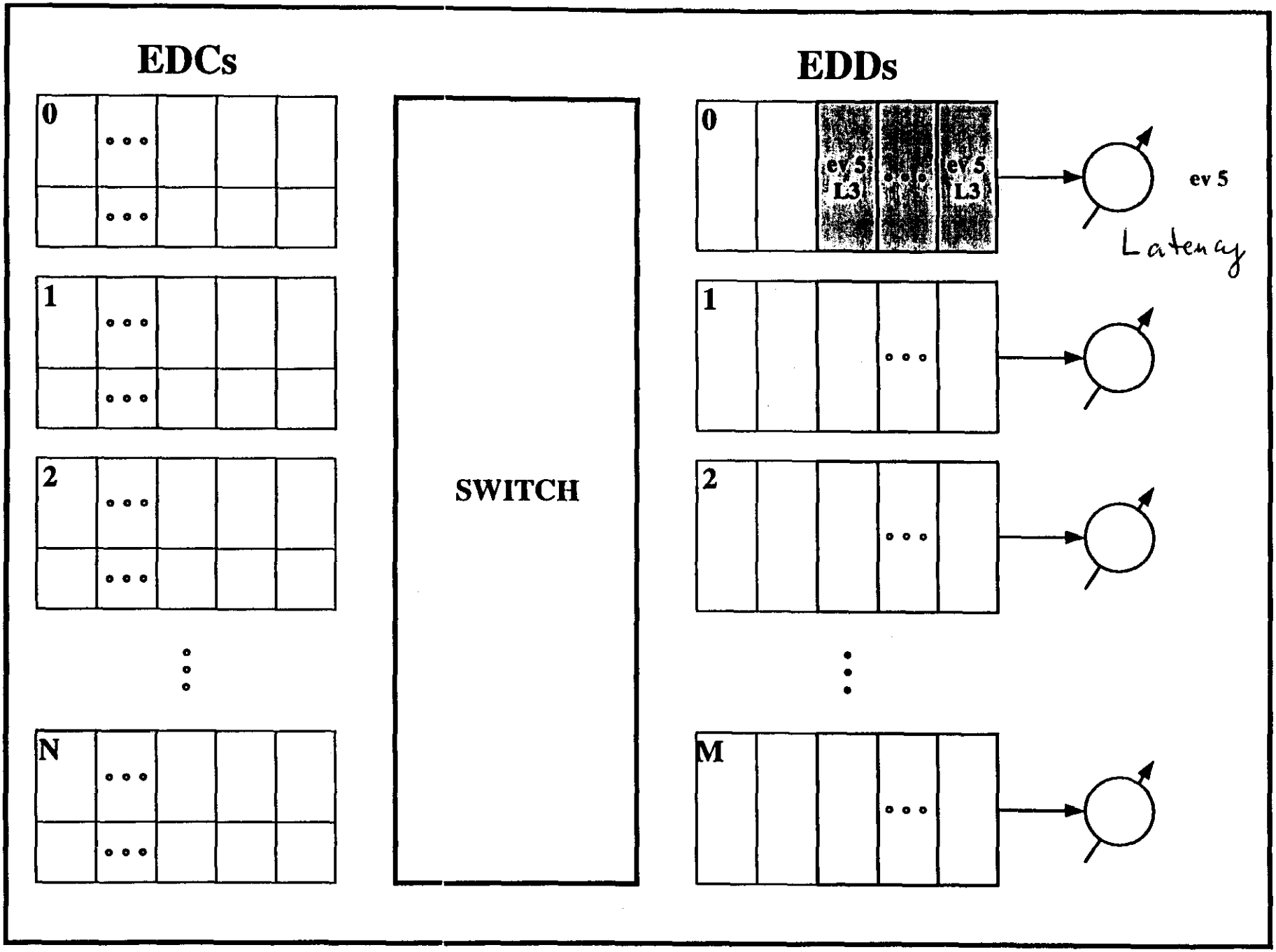
EVENT DATA DISTRIBUTOR

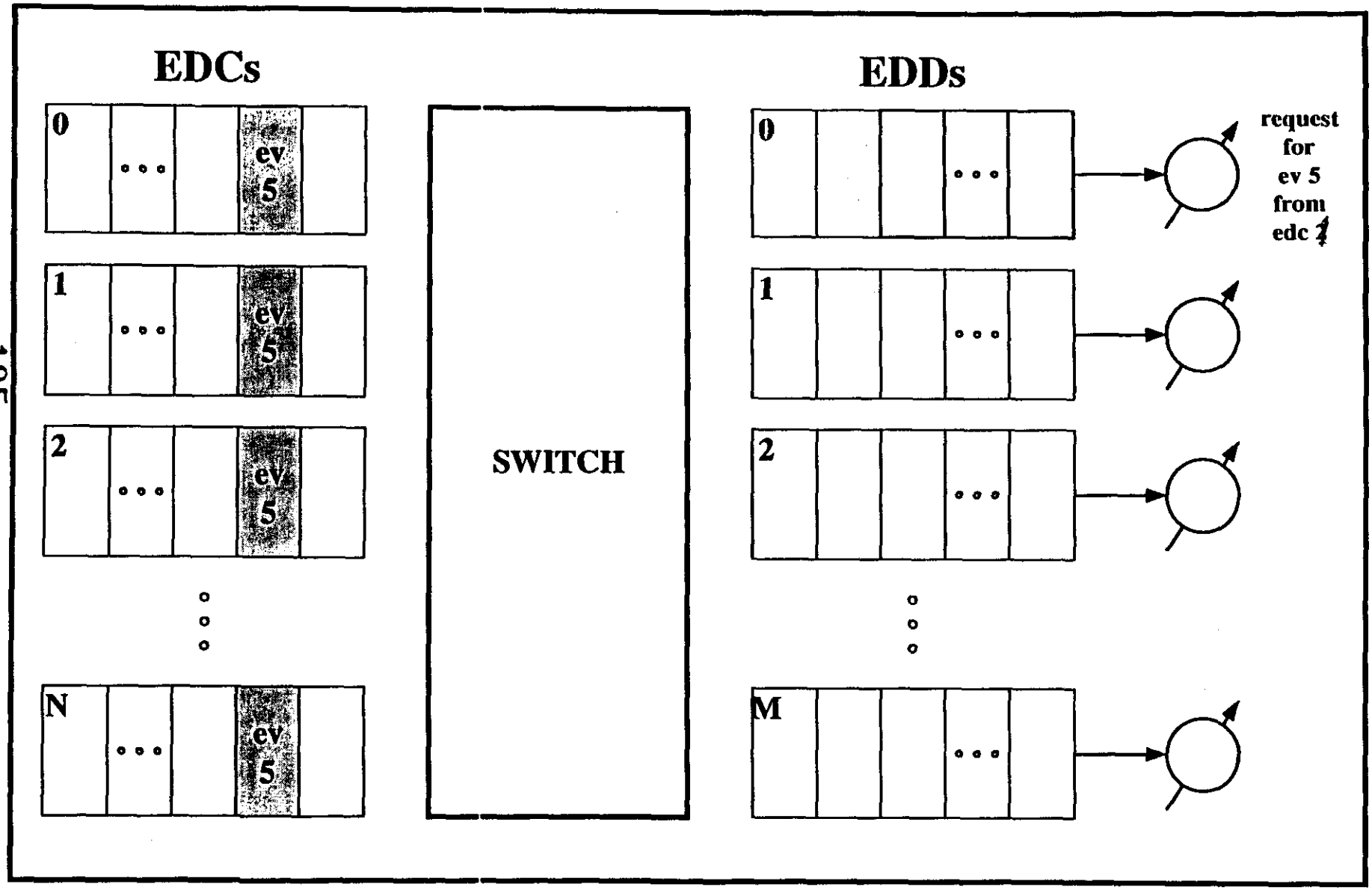


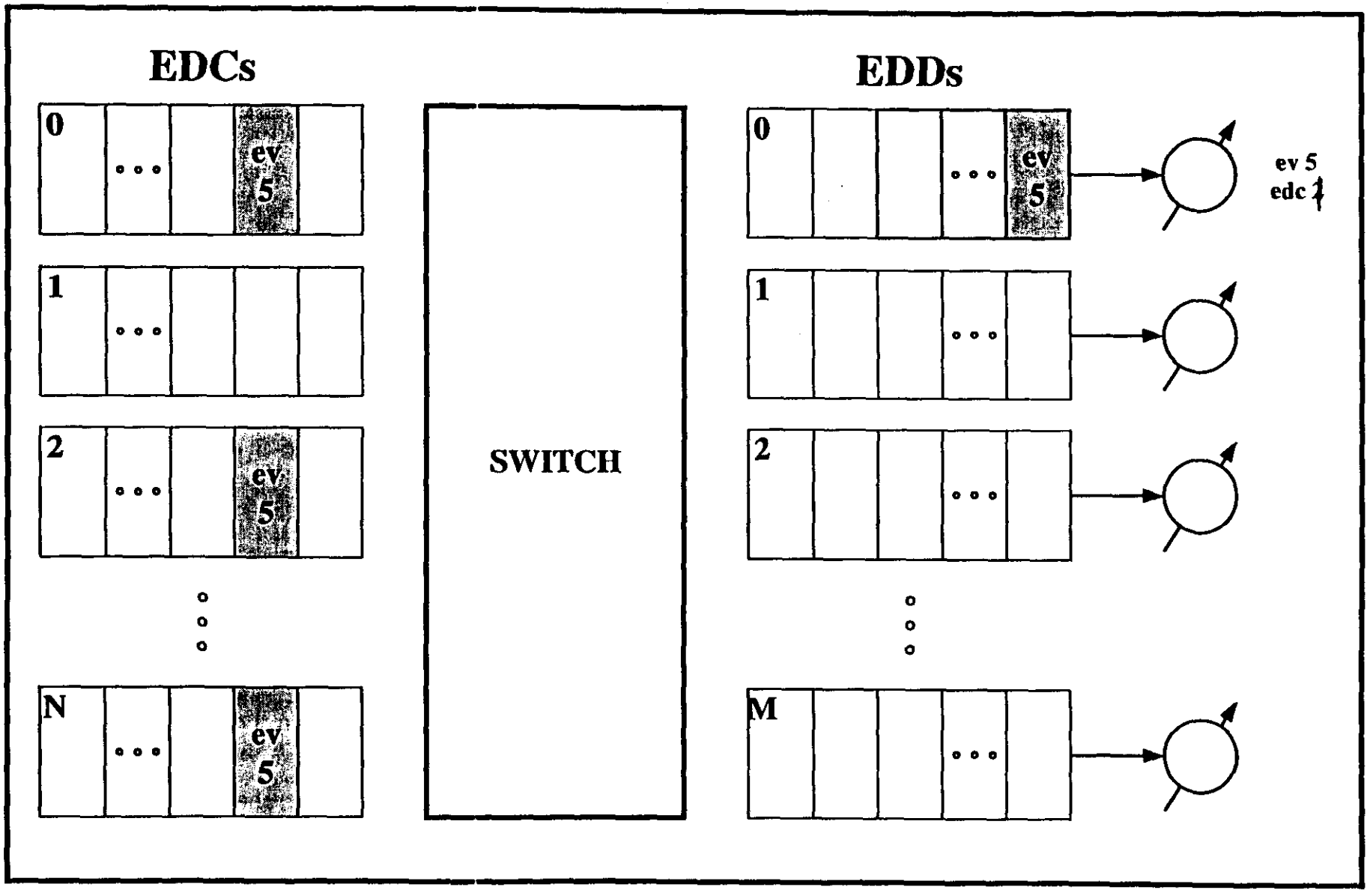
10^5 events packages/s, ≈ 1kB/event

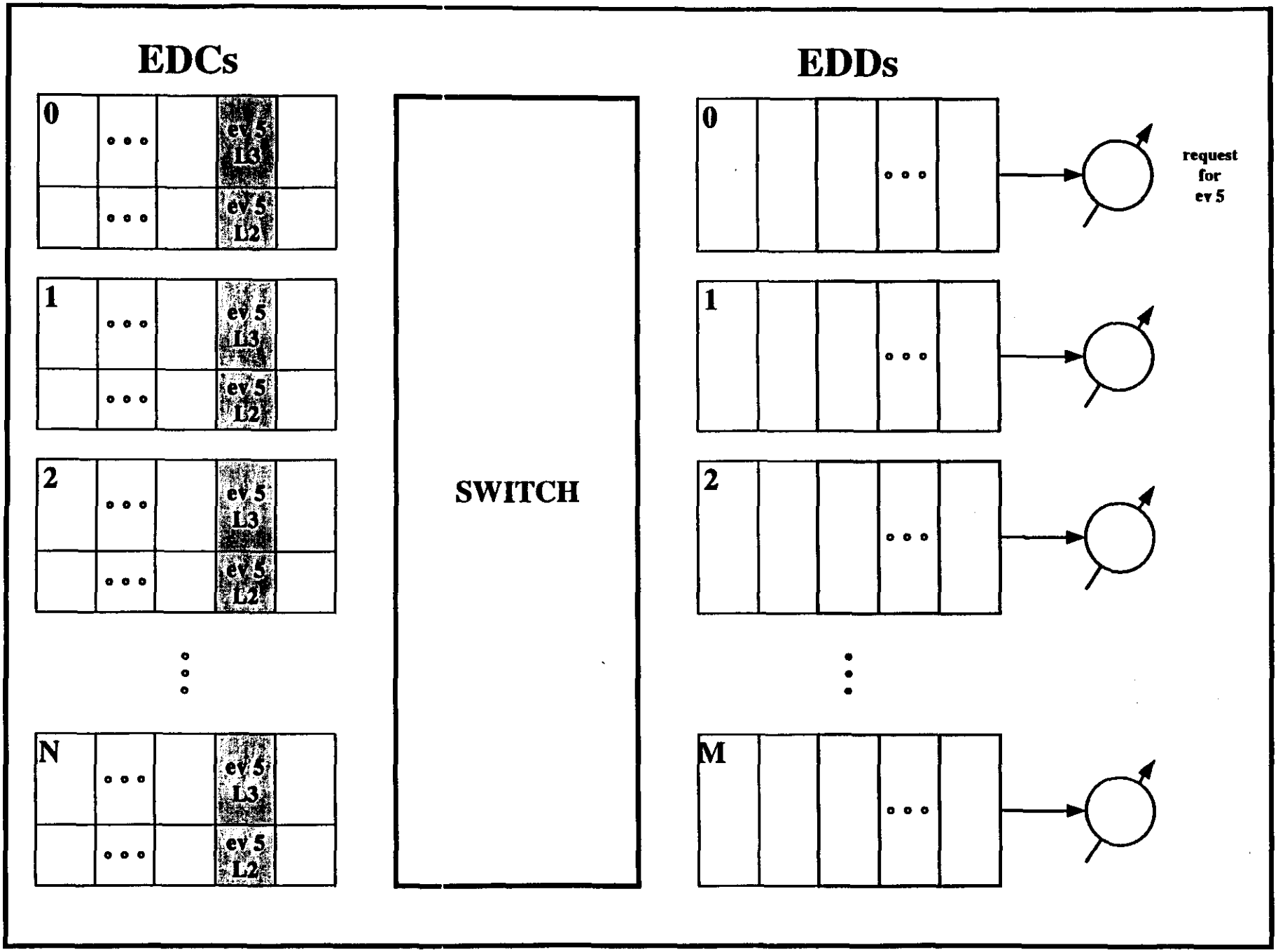


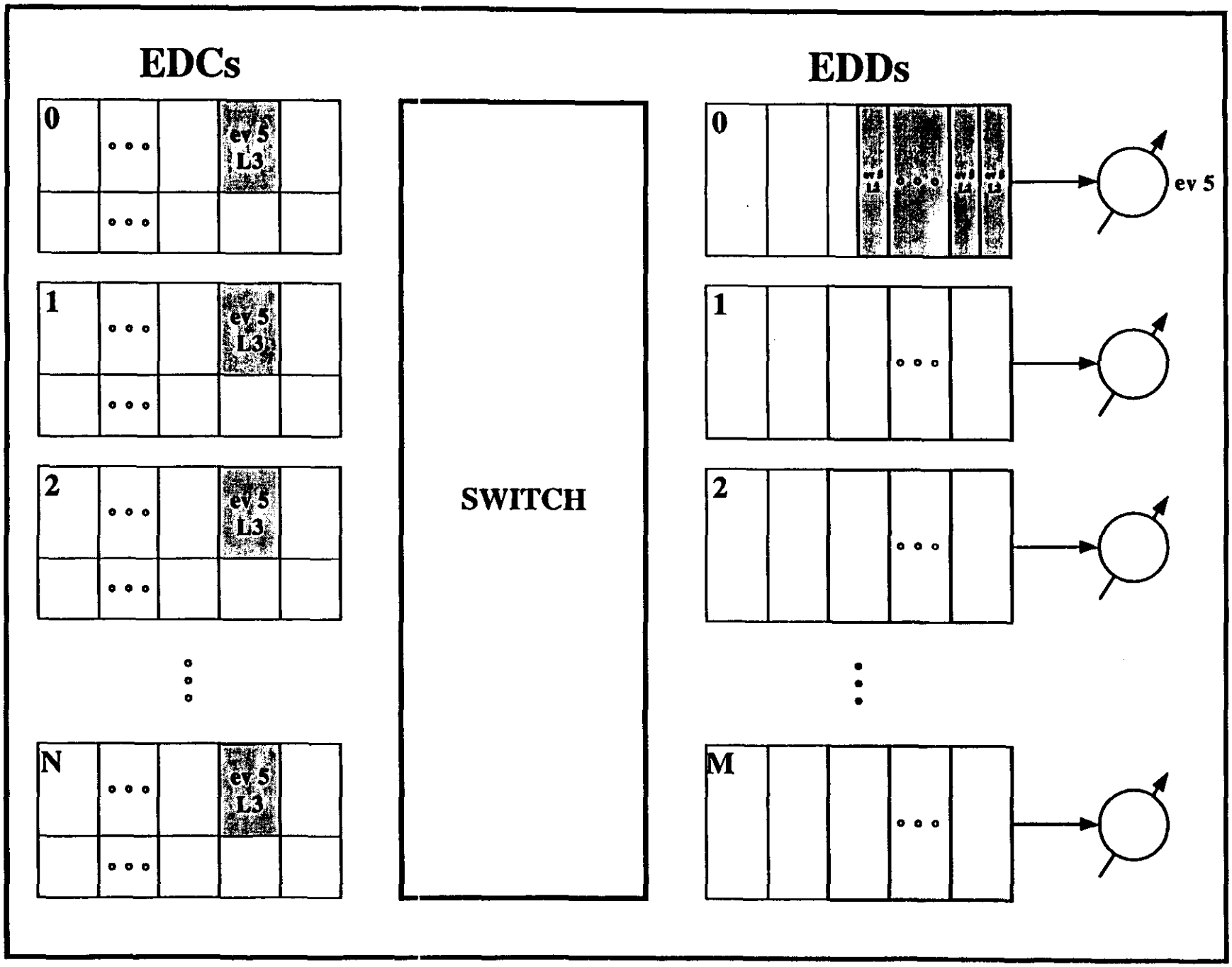

EDCs
0
1
2
N
SWITCH
EDDs
0
ev 5
ev 5
1
2
M
ev 5

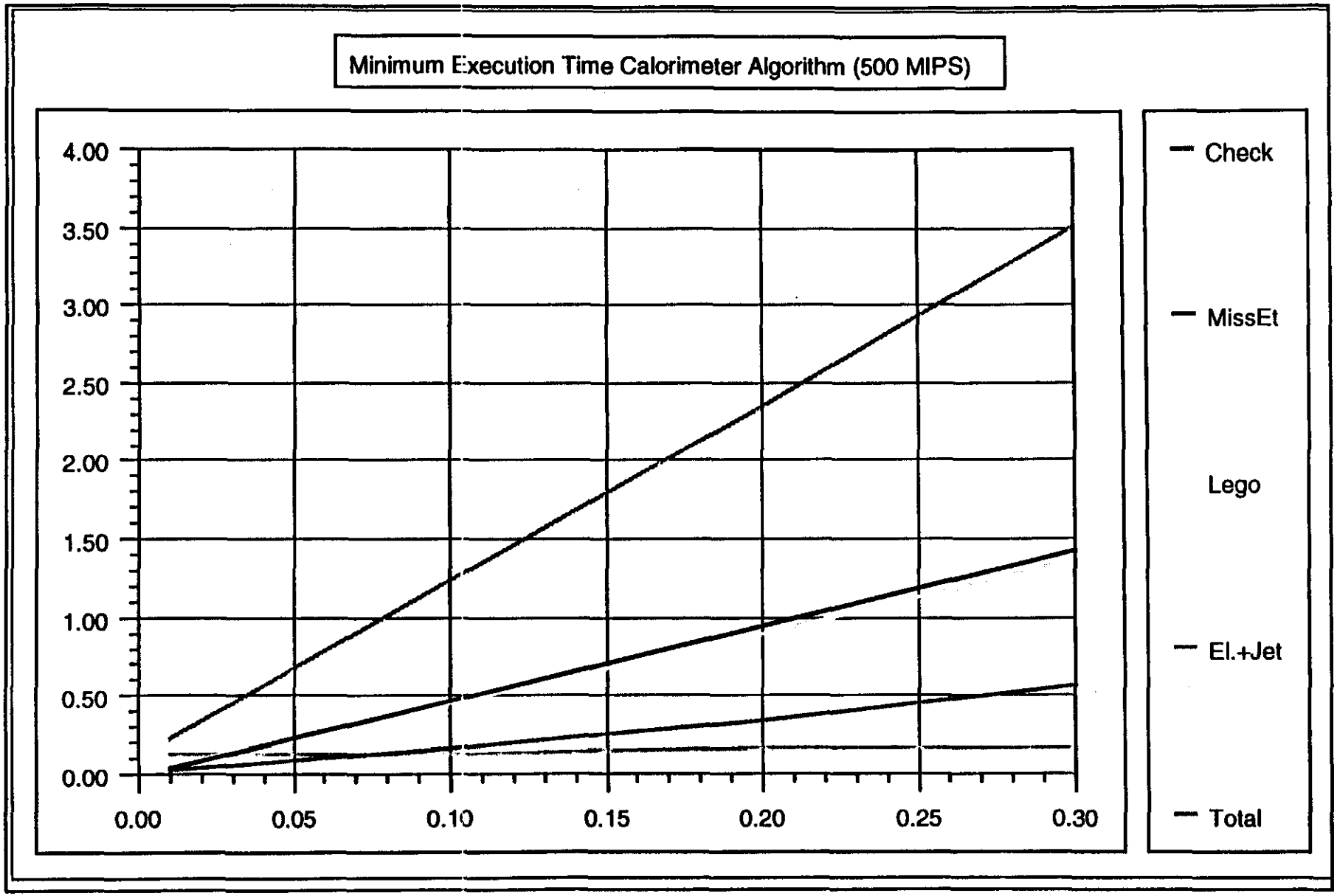

EDCs
EDDs
0
1
2
N
SWITCH
0
1
2
M
ev 5
L3
ev 5
L3
ev 5
Latency ≈ 30 m


EDCs
0
ev 5
1
ev 5
2
ev 5
N
ev 5
SWITCH
EDDs
0
1
2
M
request for ev 5 from edc 2

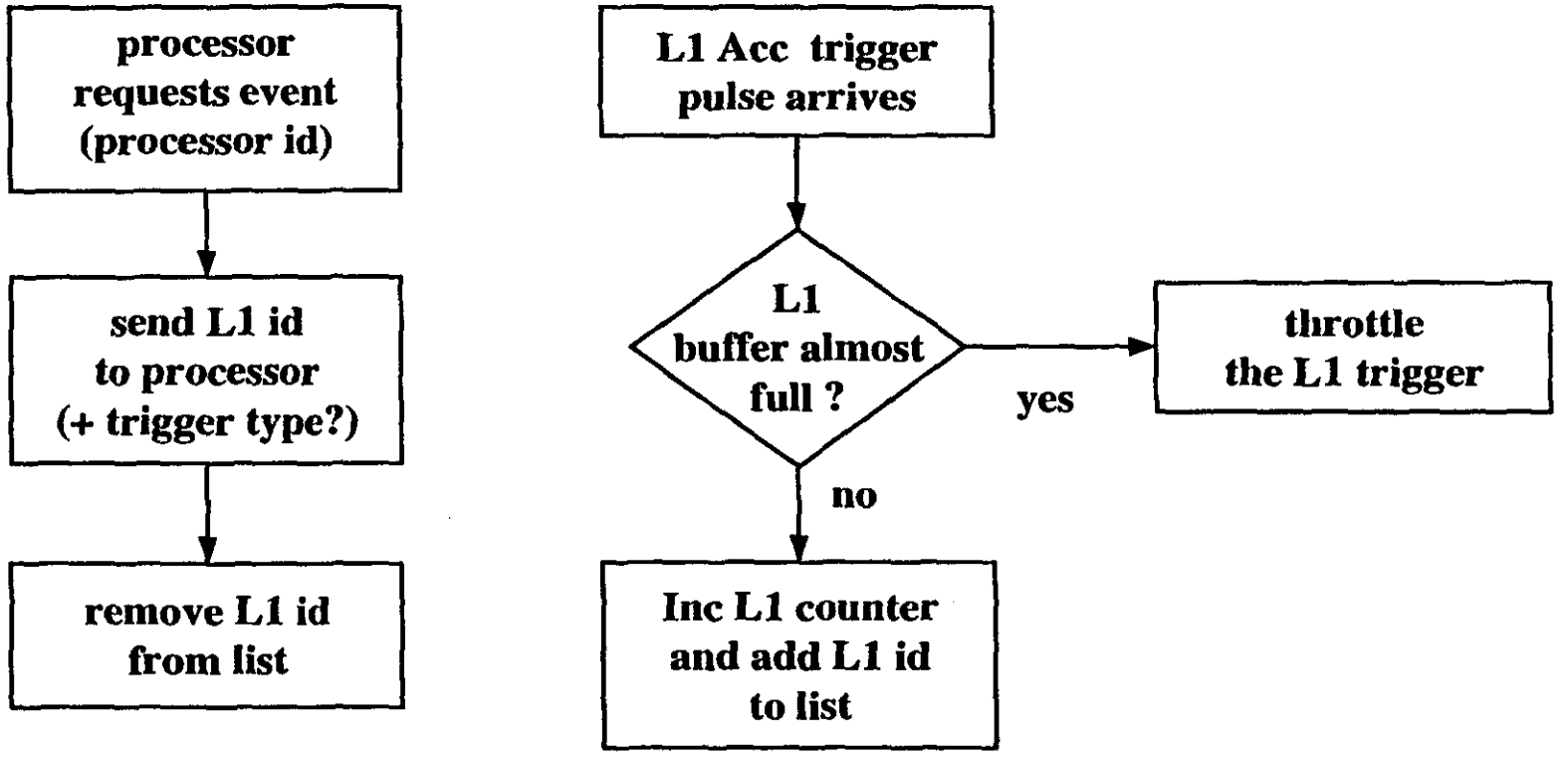

EDCs
0
ev 5
1
2
ev 5
N
ev 5
SWITCH
EDDs
0
ev 5
1
2
M
ev 5
edc 1


EDCs
EDDs
0
1
2
N
ev 5
L3
ev 5
L2
SWITCH
M
request
for
ev 5


EDCs
0
ev 5
L3
1
ev 5
L3
2
ev 5
L3
N
ev 5
L3
SWITCH
EDDs
0
1
2
M
ev 5

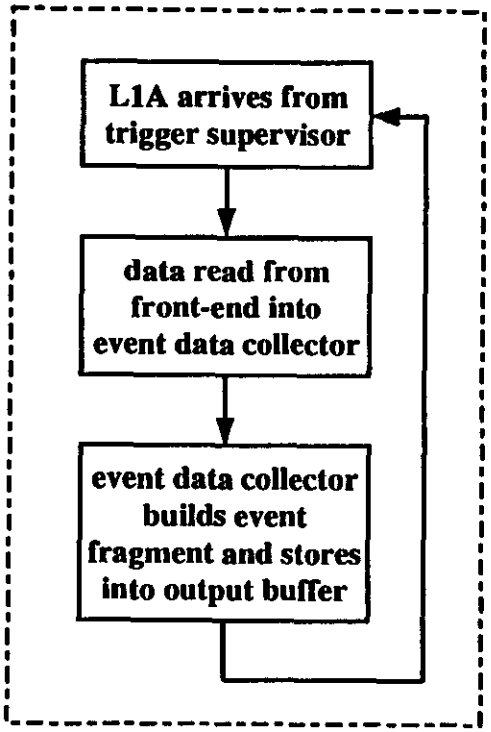

Minimum Execution Time Calorimeter Algorithm (500 MIPS)
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0.00
0.05
0.10
0.15
0.20
0.25
0.30
Check
MissEt
Lego
El.+Jet
Total

TRIGGER SUPERVISOR

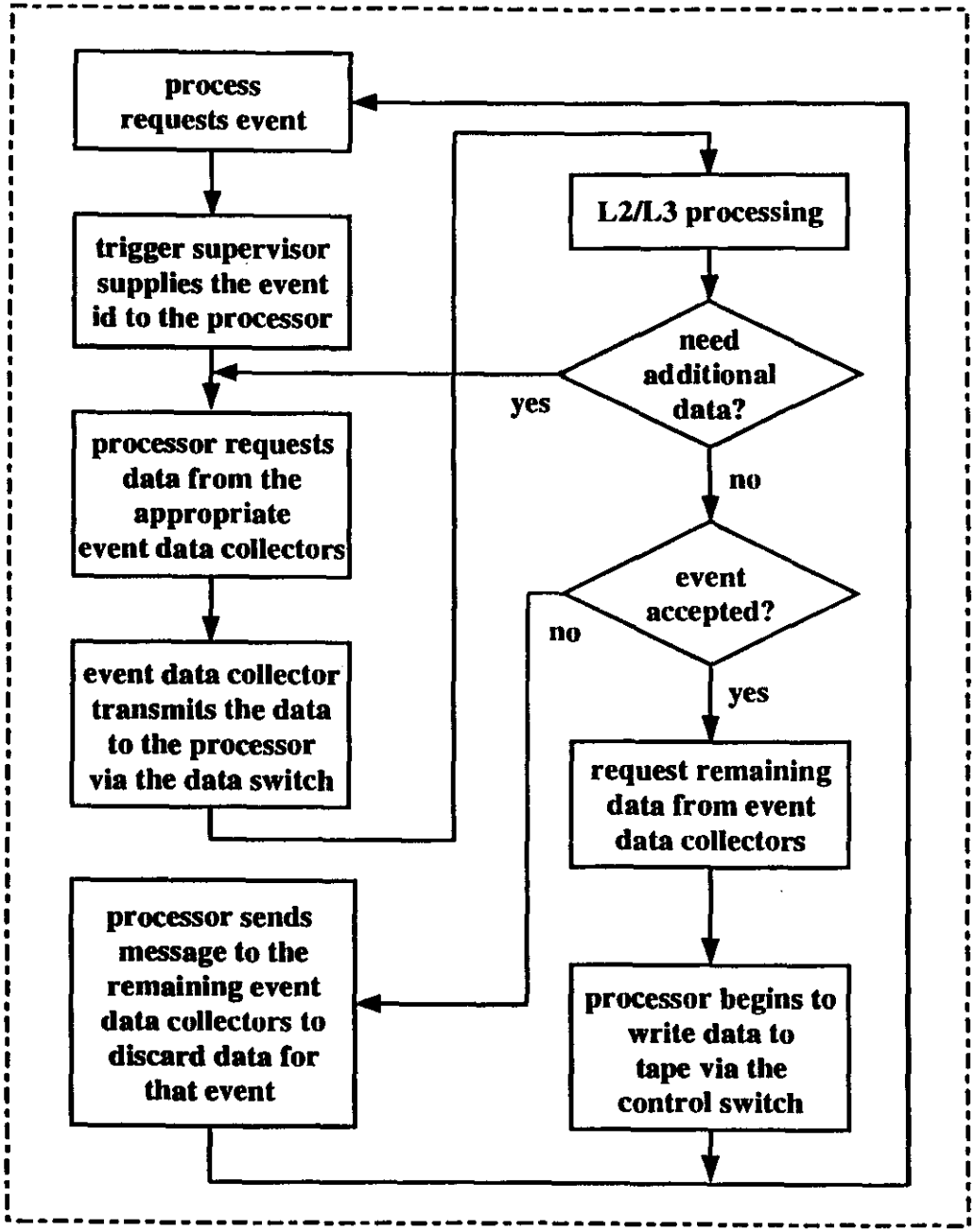


200

DATAFLOW OUTLINE



EVENT DATA COLLECTOR



L2 PROCESS

gem

γeμ

Presentation by:

K. Freeman

Operation of Transformers in Magnetic Fields

K. Freeman

SETUP + MEASUREMENTS

- Solenoid fringe field 200 gauss (C/E Shaft Lev. 0) to ~ 3 k gauss (FFS) – tend toward saturation.

- Measured transformer response in cyclotron magnet fringe field:
  - Primary voltages 120, 60, 30 volts RMS
  - Upright, sideways, flat orientations
  - $B_{EXTERNAL}$ 5 gauss ⟶ 3 k gauss
  - Secondary winding not loaded.

CONCLUSIONS (EARLY RESULTS)

- At constant primary voltage, exciting current increases with $B_{EXTERNAL}$ until full saturation
  - ⟹ Primary inductance drops
  - ⟹ Inductors behave differently with Solenoid energized – test vs. experiment.
  - ⟹ Secondary inductance should also drop.

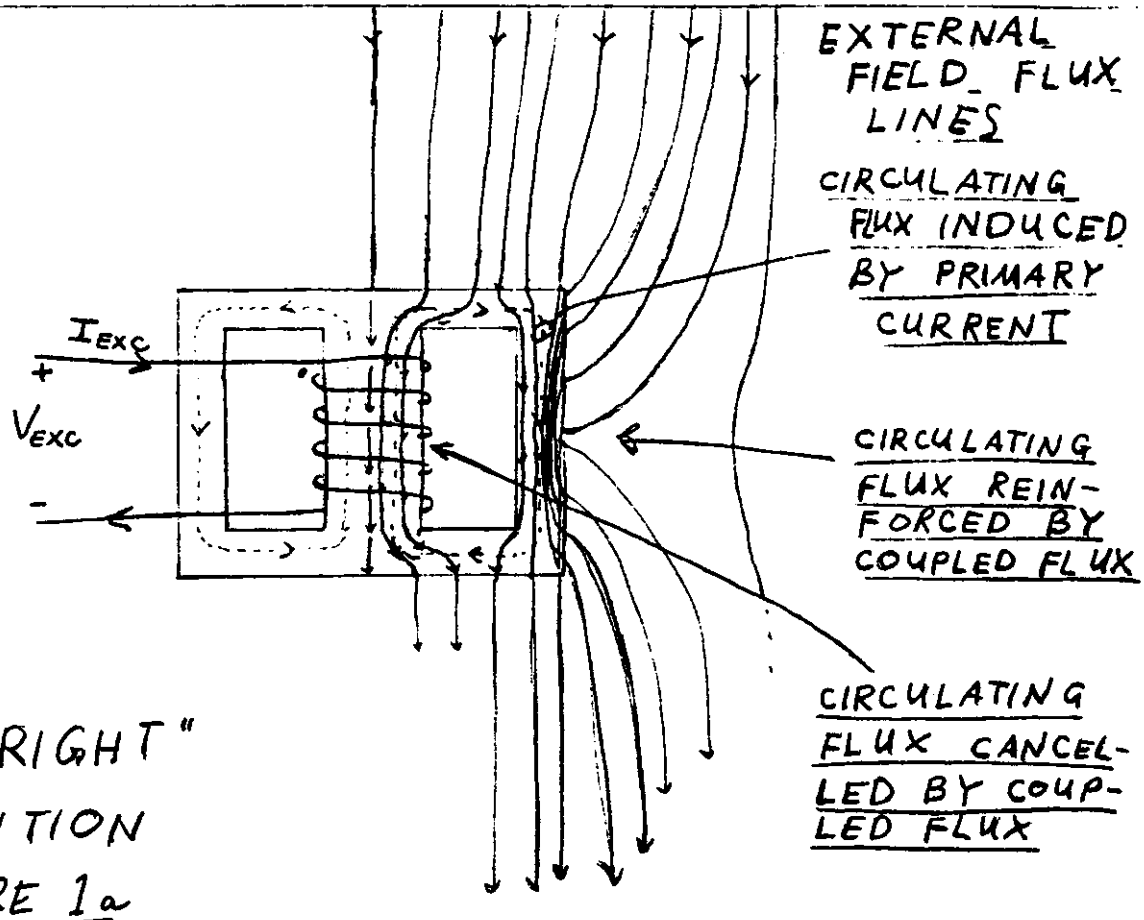
  MUTUAL INDUCTANCE ? ? ?
- Below ~ 400 gauss, little response to B_{EXT}
  ⟹ C/E Shaft Level 0 unaffected.
- Orientation strongly influences tolerance:
  - Flat was best – largest area, fluxes ⊥
  - Upright next – larger area than sideways
  - Sideways worst – half of conduction area.

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

FUTURE WORK – REFINEMENT + EXPANSION

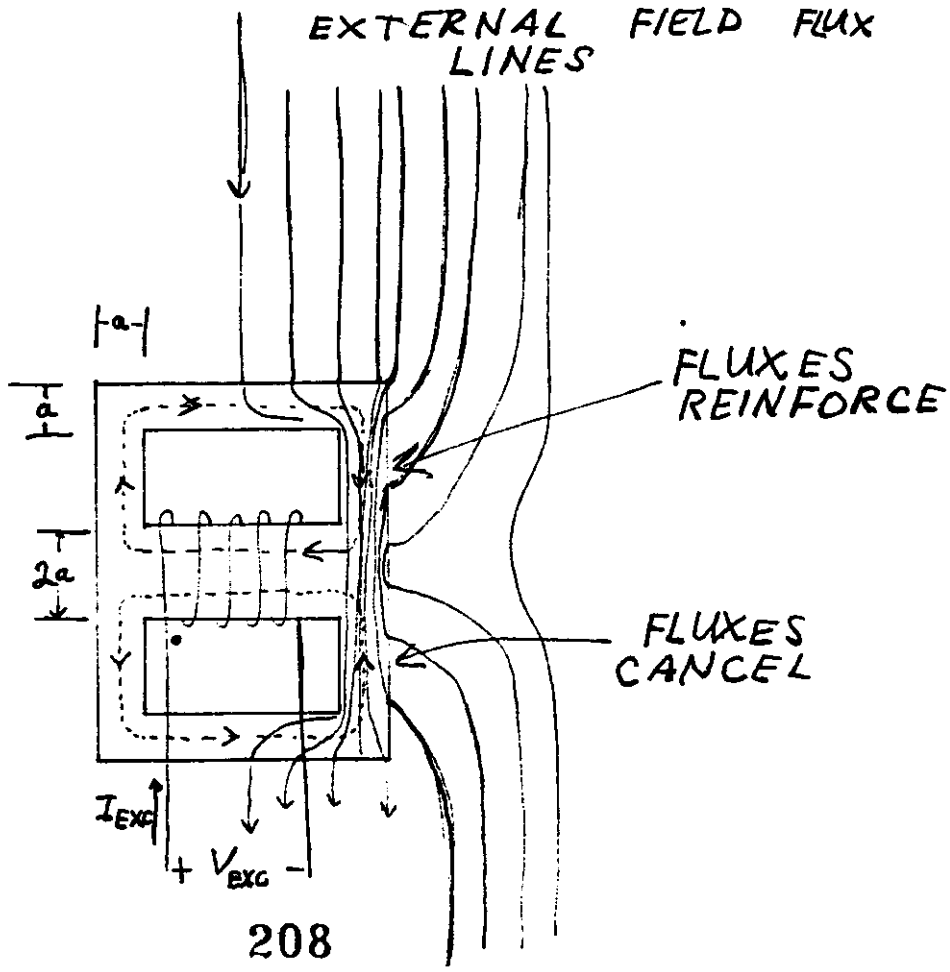
- Larger transformers – scaling issue
- Loaded secondaries – mutual inductance effect
- Reduce series resistance – maintain voltage
- More points, more detail
- Add true RMS measurement
- Improve mounting – stability, alignment, length
- Observe harmonic variation with spectrum analyzer
- Characterize voltage saturation with no external field.

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD



"UPRIGHT" POSITION

FIGURE 1a



"SIDEWAYS" POSITION

FIGURE 1b

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

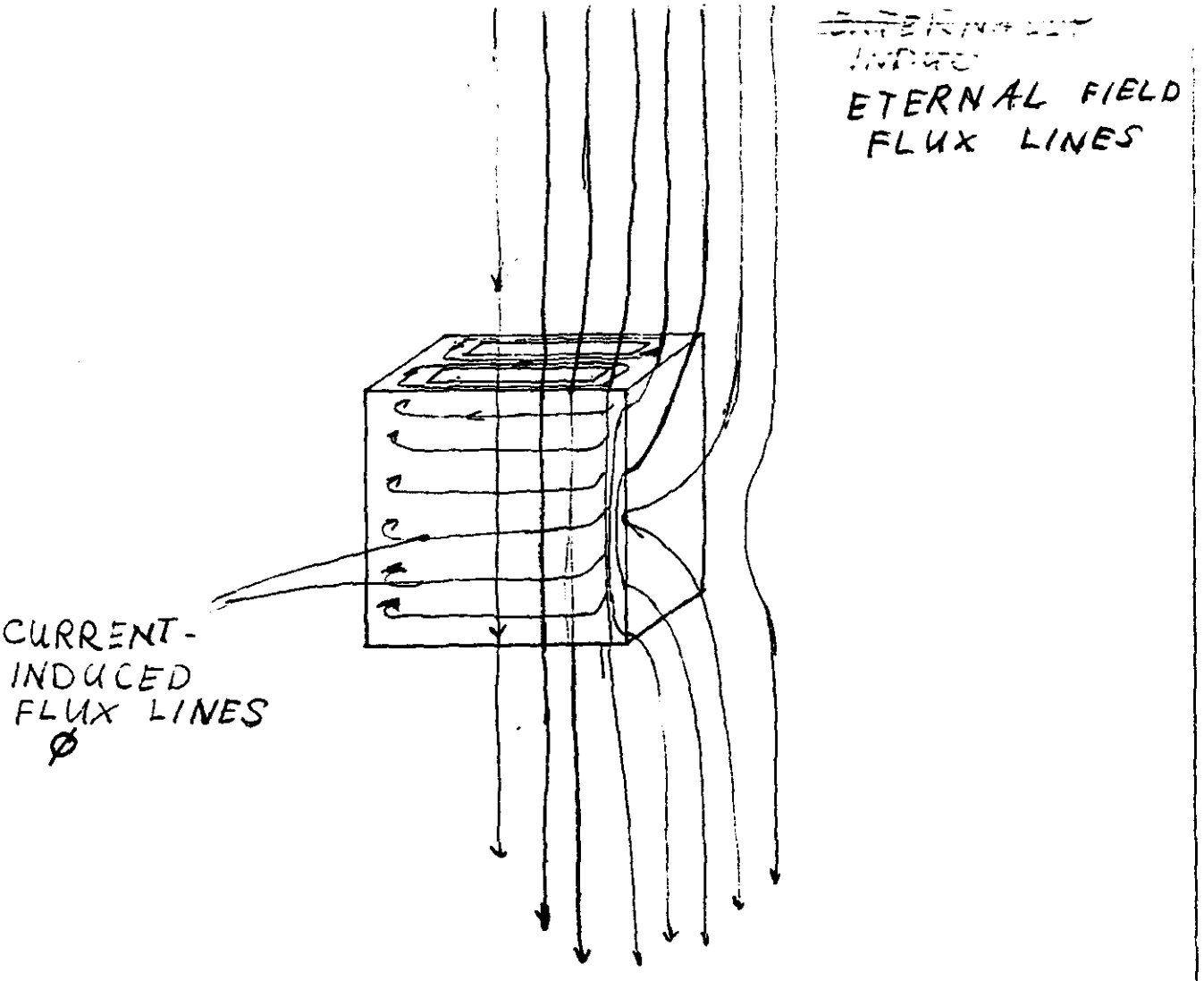
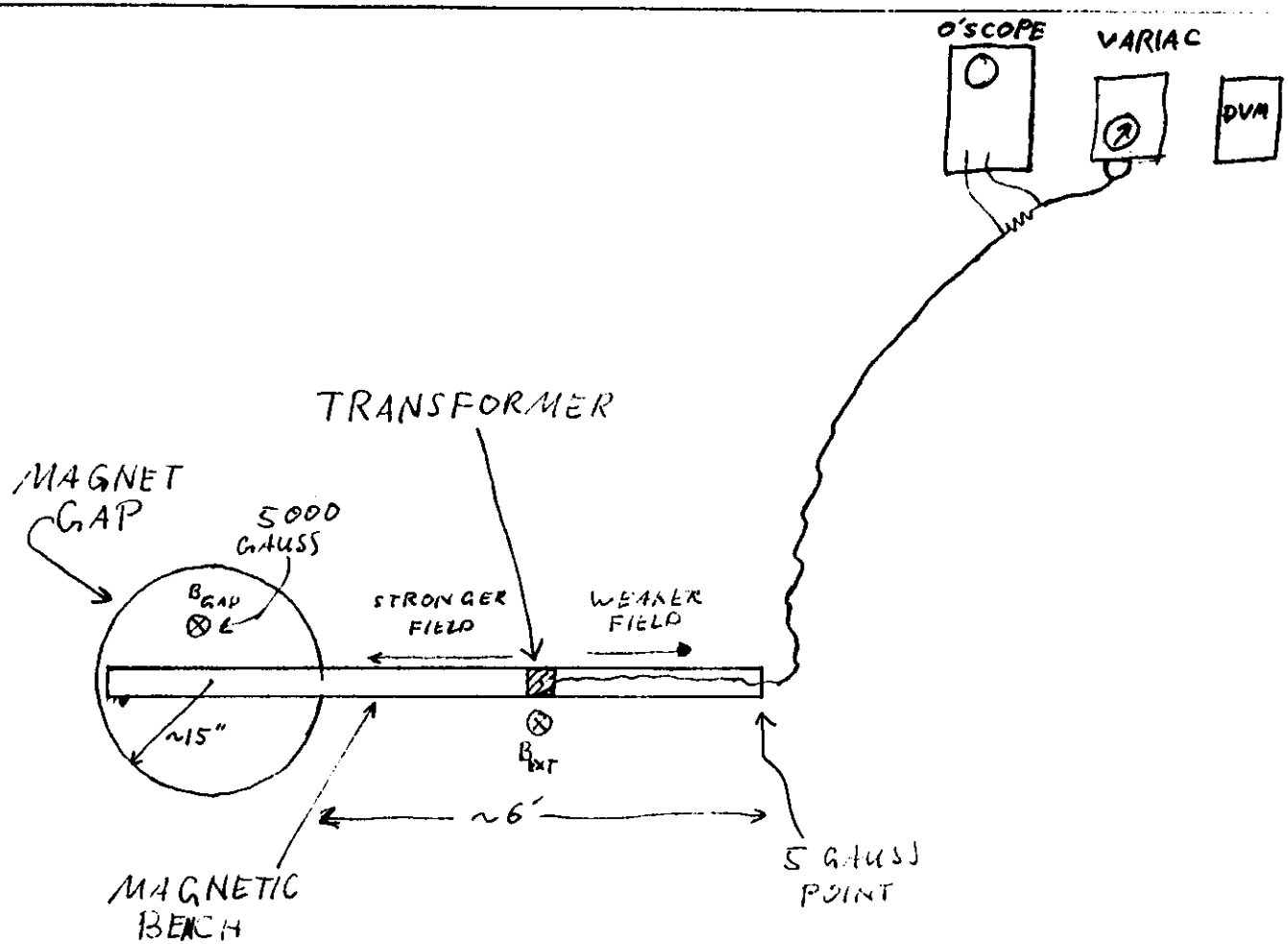


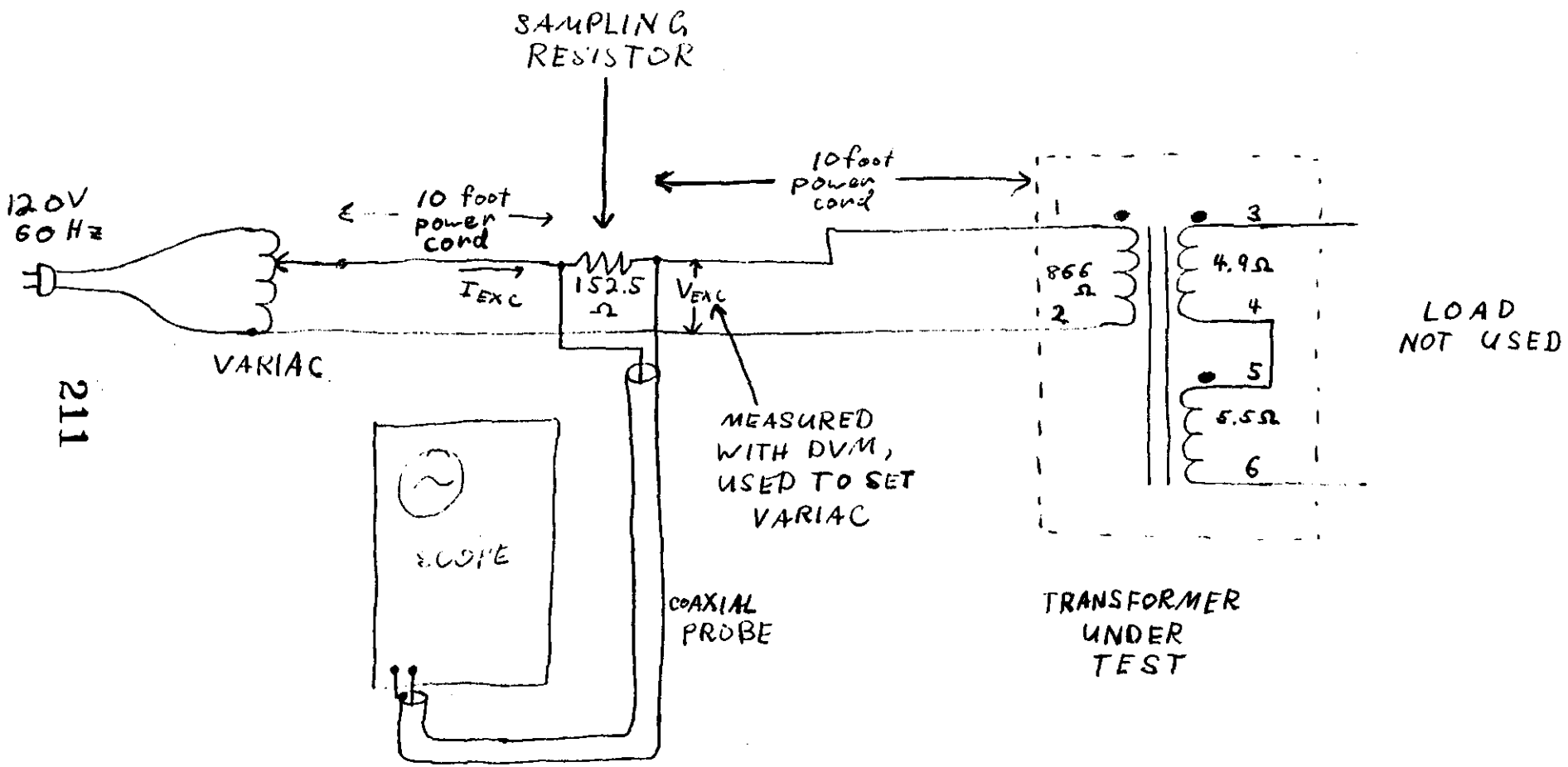
FIGURE 1c "FLAT" ORIENTATION

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD



AMPAD 22-141 50 SHEETS 22-142 100 SHEETS 22-144 200 SHEETS

AMPAD 22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS



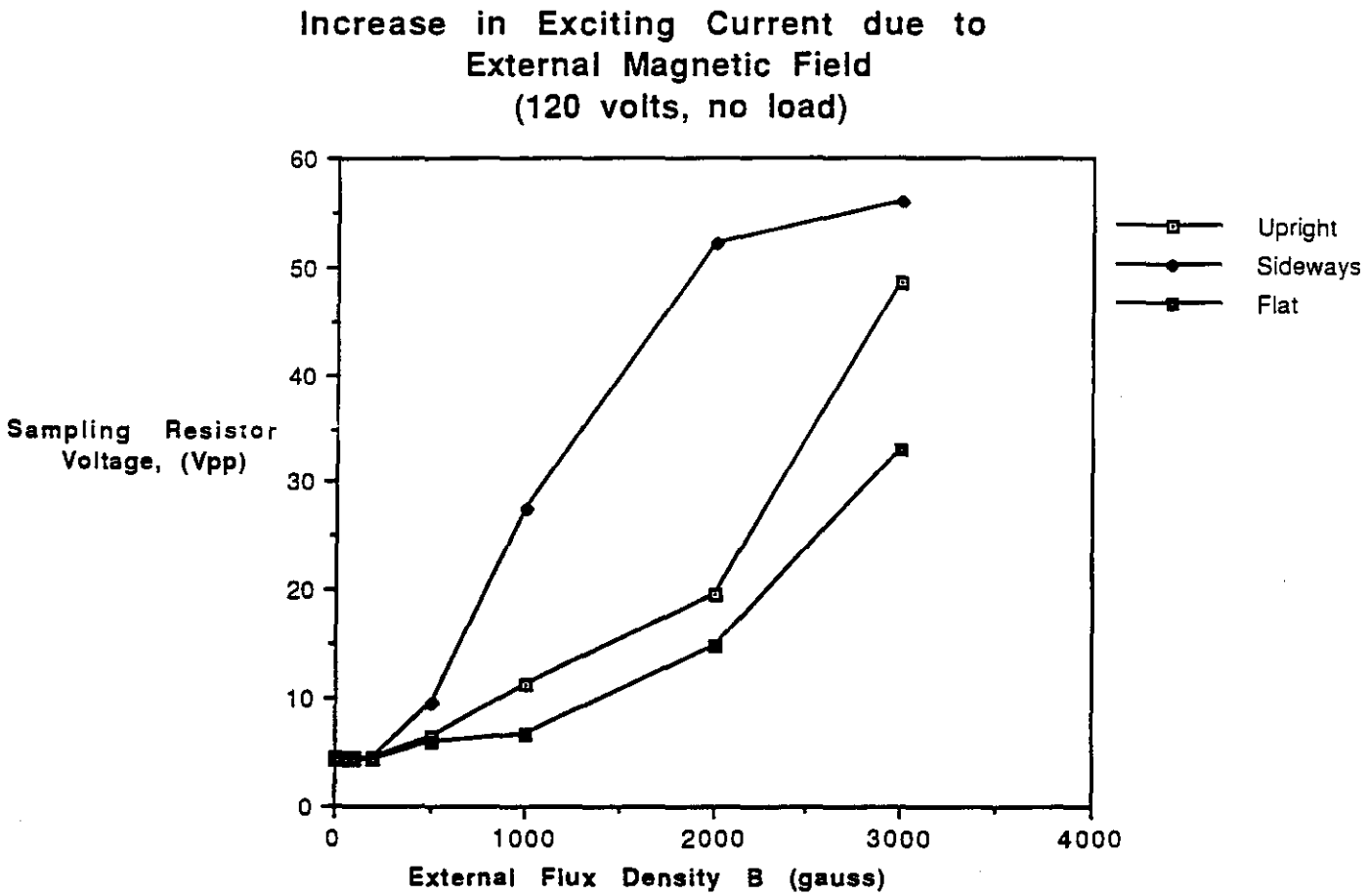

Increase in Exciting Current due to
External Magnetic Field
(120 volts, no load)
Sampling Resistor
Voltage, (Vpp)
60
50
40
30
20
10
0
0
1000
2000
3000
4000
External Flux Density B (gauss)
Upright
Sideways
Flat

FIGURE 4

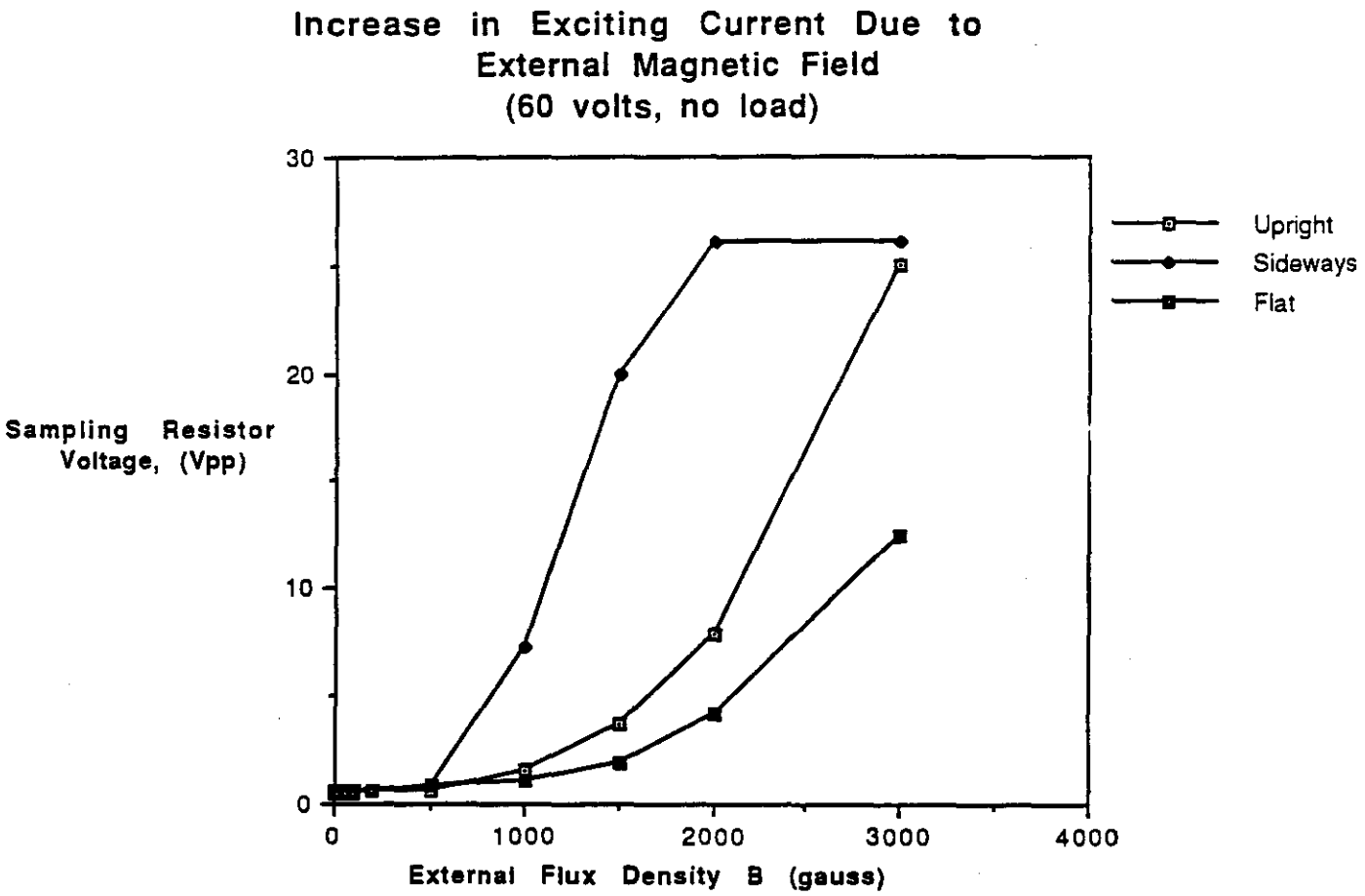

Increase in Exciting Current Due to
External Magnetic Field
(60 volts, no load)
Sampling Resistor
Voltage, (Vpp)
30
20
10
0
0
1000
2000
3000
4000
External Flux Density B (gauss)
Upright
Sideways
Flat

FIGURE 5

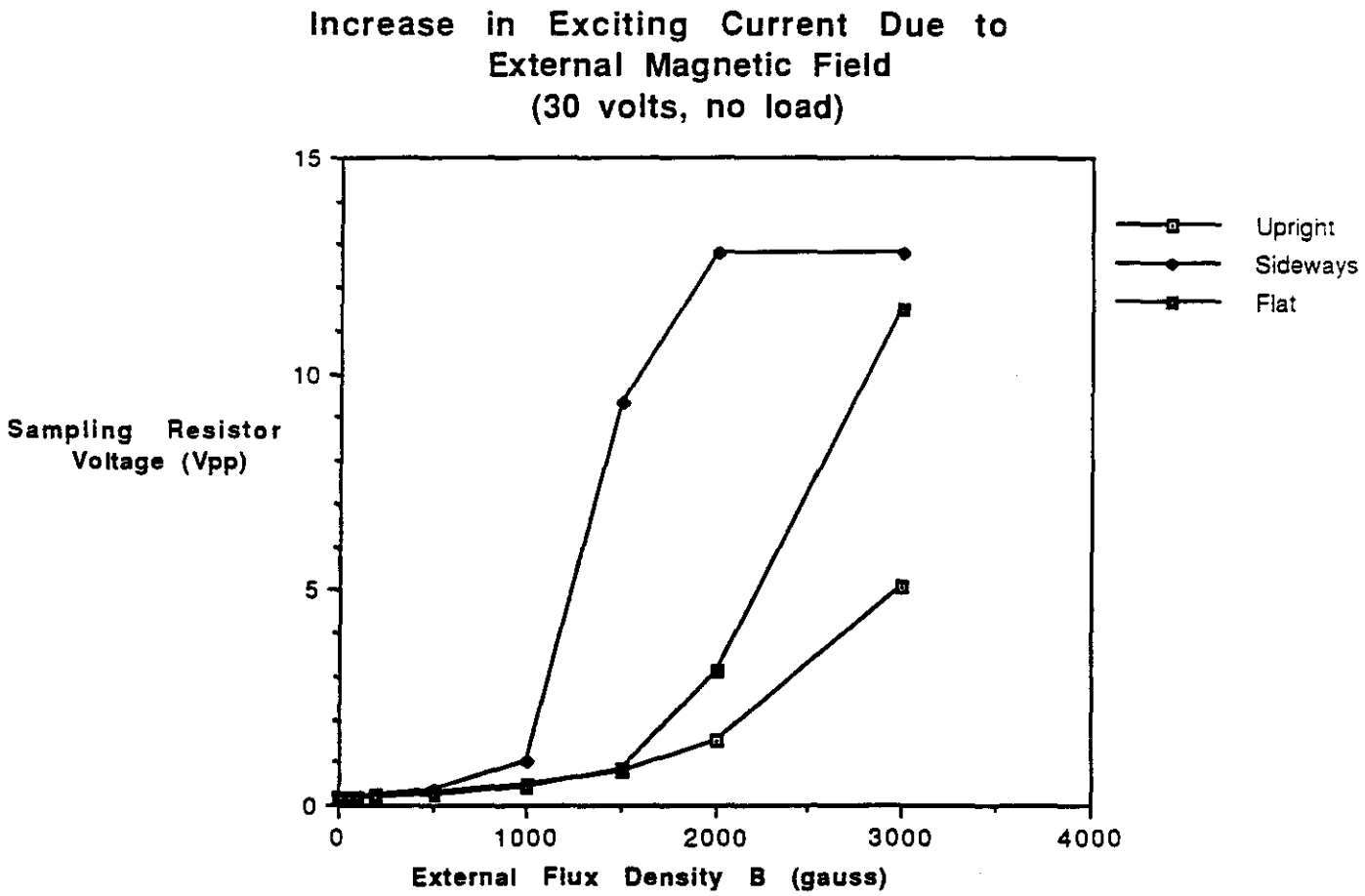

Increase in Exciting Current Due to
External Magnetic Field
(30 volts, no load)
Sampling Resistor
Voltage (Vpp)
15
10
5
0
0
1000
2000
3000
4000
External Flux Density B (gauss)
Upright
Sideways
Flat

FIGURE 6

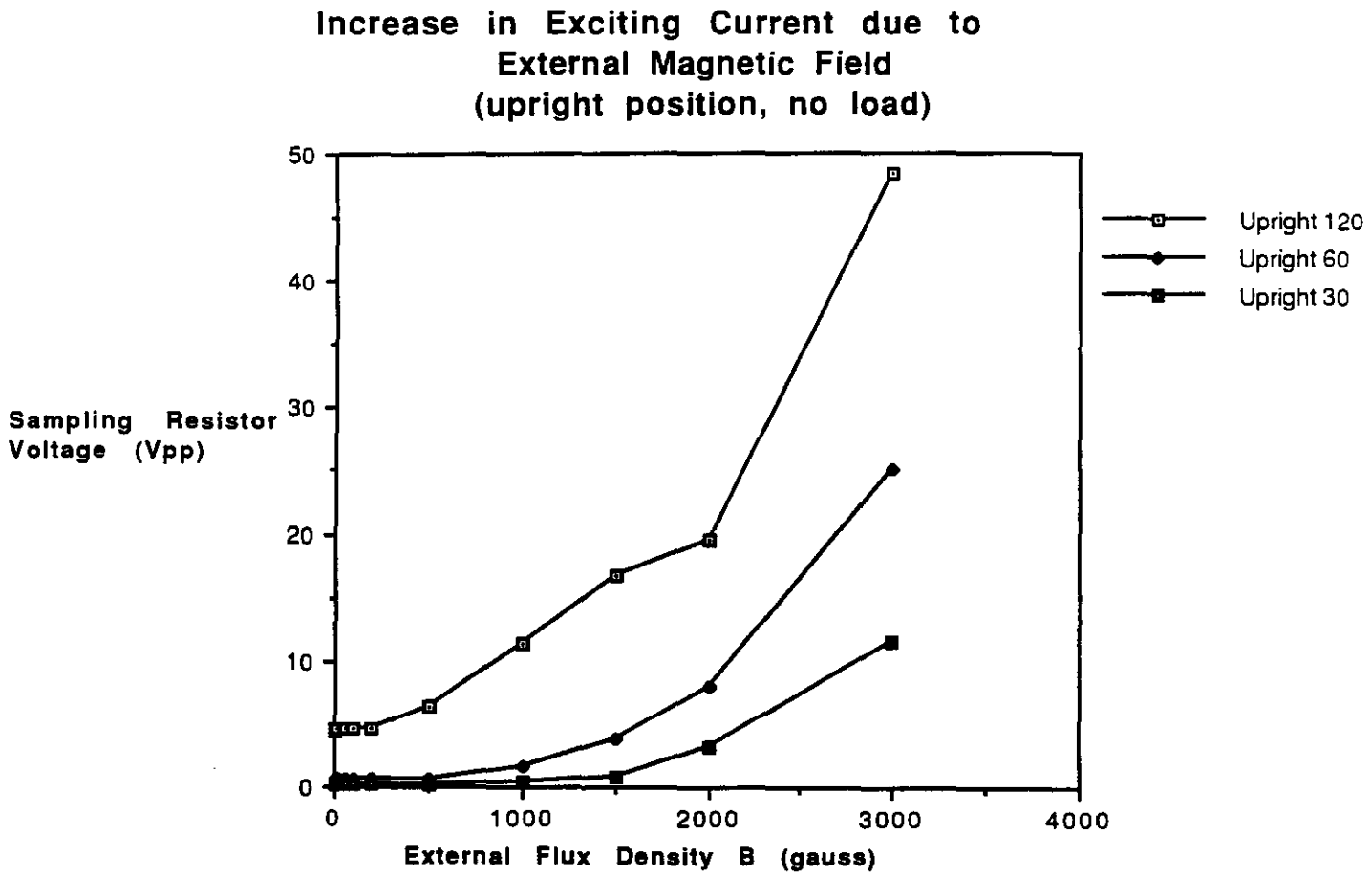

Increase in Exciting Current due to
External Magnetic Field
(upright position, no load)
Sampling Resistor
Voltage (Vpp)
50
40
30
20
10
0
0
1000
2000
3000
4000
External Flux Density B (gauss)
Upright 120
Upright 60
Upright 30

FIGURE 7

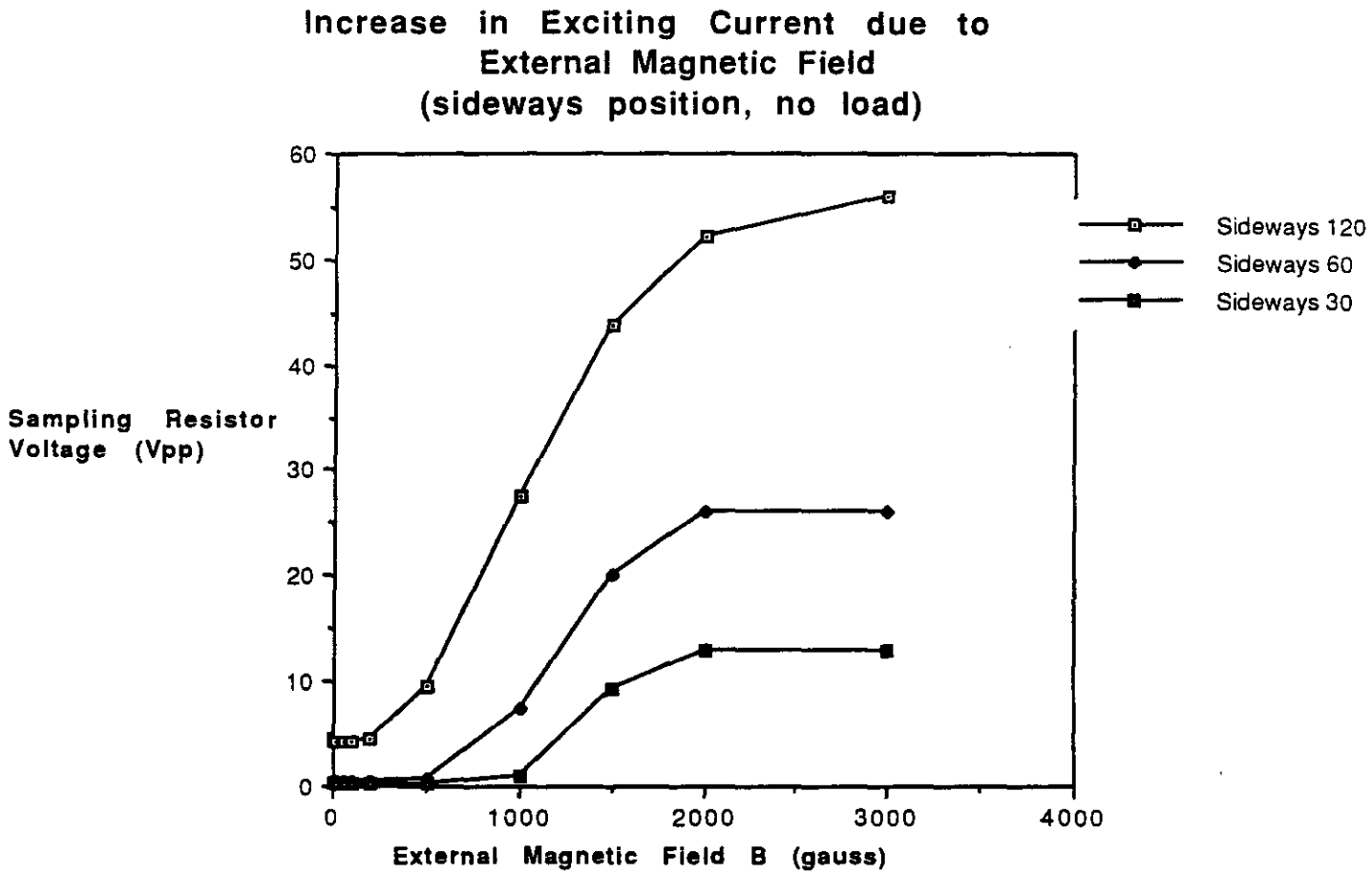

Increase in Exciting Current due to
External Magnetic Field
(sideways position, no load)
Sampling Resistor
Voltage (Vpp)
60
50
40
30
20
10
0
0
1000
2000
3000
4000
External Magnetic Field B (gauss)
Sideways 120
Sideways 60
Sideways 30

FIGURE 8

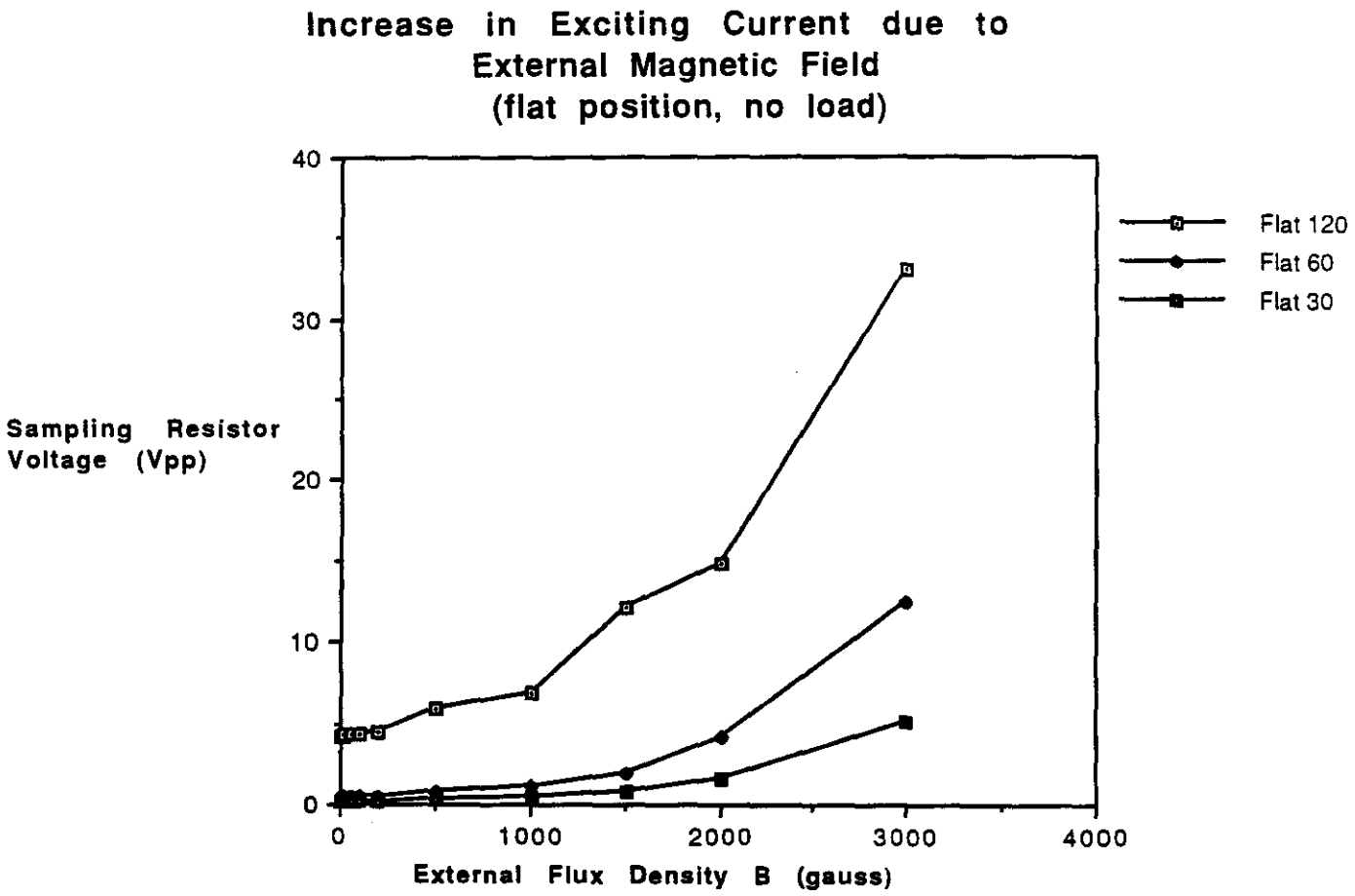
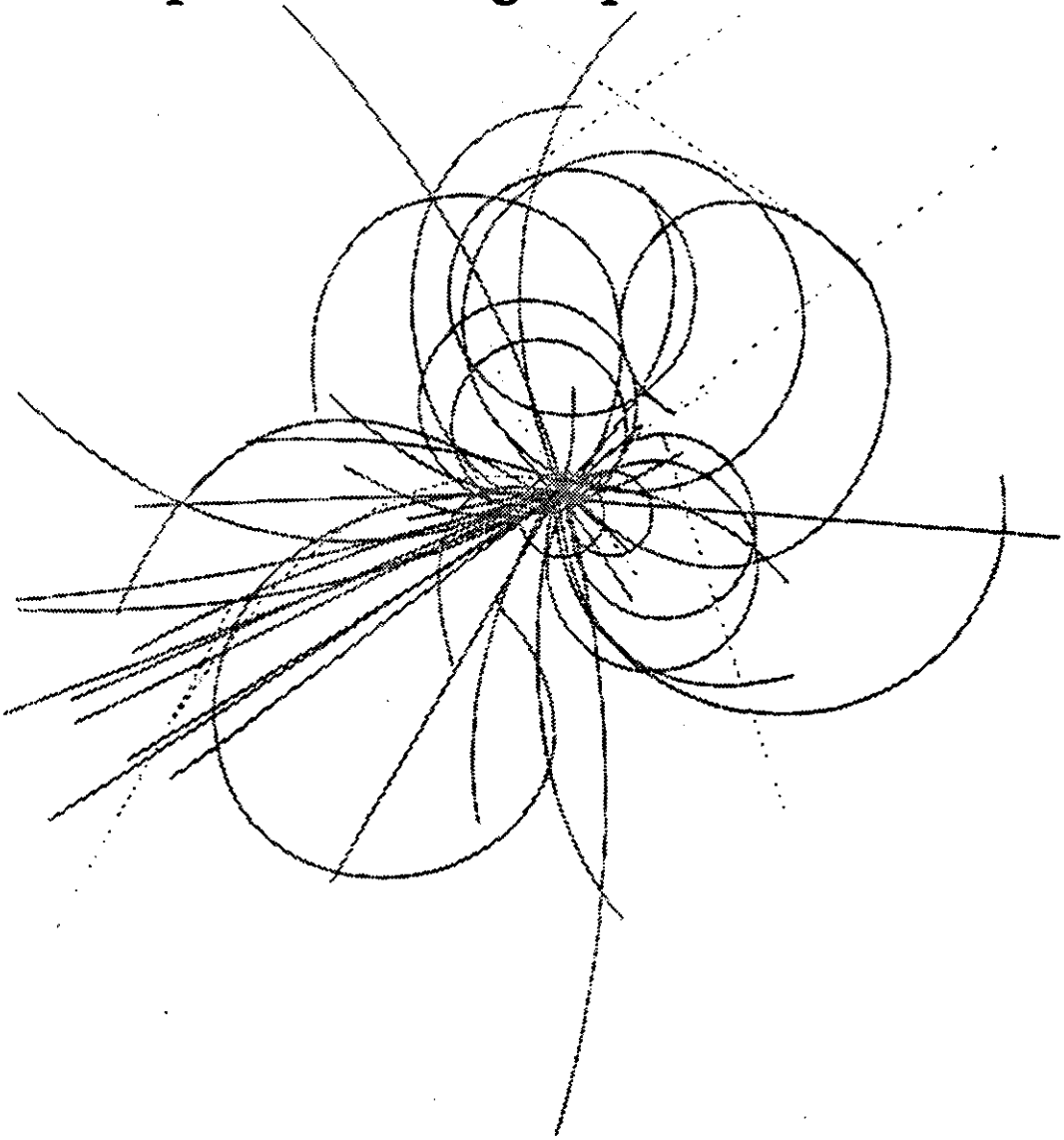

Increase in Exciting Current due to
External Magnetic Field
(flat position, no load)
Sampling Resistor
Voltage (Vpp)
40
30
20
10
0
0
1000
2000
3000
4000
External Flux Density B (gauss)
Flat 120
Flat 60
Flat 30

FIGURE 9

SSCL-Preprint-164

SSCL-Preprint-164

Superconducting Super Collider Laboratory



3D-Flow Processor for a Calorimeter Programmable Level-1 Trigger

D. Crosetto

October 1992

SSCL-Preprint-164

3D-Flow Processor for a Calorimeter Programmable Level-1 Trigger*

Dario Crosetto

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Dallas, TX 75237

October 1992

*Presented at the 1992 Nuclear Science Symposium (NSS), Medical Imaging Conference (MIC), Oct. 25–31, 1992, Orlando, Florida.

†Operated by the Universities Research Association, Inc., for the U.S. Department of Energy under Contract No. DE-AC35-89ER40486.

3D–Flow Processor for a Calorimeter Programmable Level-1 Trigger

D. Crosetto
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Abstract

The types of detectors and the physics involved in present experiments are reaching a level of cost and complexity so great that it is preferable to implement a programmable trigger solution at all levels rather than a system realized with cabled logic. Experience demonstrates that fine tuning on the trigger is often achieved only after running an experiment and analyzing the first data acquired. A Level-1 trigger is required to identify objects (particles such as electron, jets, etc.) with programmable algorithms at 60 million frames-per-second. These requirements have led to the design of a special "3D-Flow" processor that, together with a special pipelined parallel-processing architecture, allows a sustained data rate of 60 million frames-per-second. The 3D-Flow is a data-flow processor that can be used in one-, two-, or three-dimension array for high-speed signal-processing applications such as identifying objects in a matrix in a programmable form. Feasibility studies demonstrate that with present technology a 3D-Flow chip consuming 8 W, and accommodating 32 processors at 60 MHz can be built today, and that the same chip can be built one year from now at a 120-MHz clock rate.

I. Introduction

The Superconducting Super Collider (SSC) is being built to study high-energy physics. Every 16 ns, proton beams will collide and the particles produced by the collision must be identified and studied. Many detectors will be used to detect and identify the particles. The calorimeter is one of the sub-detectors used at the SSC. Two proton beams will collide in the center of the calorimeter, sending particles to the calorimeter towers in the barrel and end caps. The amount of energy released in the collision is detected and then transferred through channels to digital processors, where the identification of particles is begun in Level-1 triggering. The triggering mechanism must be able to rapidly reduce the amount of data by discarding unimportant data. The calorimeter will provide Level-1 trigger information regarding electrons, photons, jets, and missing E_t (such as neutrinos).[1] The starting point is the off-line algorithms that require milliseconds (ms) for execution. The challenge is to find a given "system architecture," "processor architecture," and its "instruction set" that provide the best and most suitable (to the component) conversion of the off-line trigger algorithms to a fast and simple "real-time" algorithm that will still have high particle-identifying efficiency.[2,3]

II. Physic Requirements

With a programmable solution, it is possible to use the same electronic (commonality) chain for several experiments. For this reason, and because all physicists do not accept a specific type of trigger algorithm, a programmable solution is highly desirable. As an example of programmability, many trigger algorithms have been implemented. Among these are finding a local maximum, calculating cluster and transverse energy, comparing cluster and partial sums to different threshold, determining whether an electromagnetic cluster is isolated from nearby energy deposition, and determining whether a 4×4 matrix is a possible jet. There are many conditions to test when making the Level-1 decision. As an example of a programmable system, a few methods that will verify these conditions will be implemented using the 3D-Flow parallel-processing system array. Figure 1 shows how to check some of these conditions.

In order to distinguish electrons and photons, the "em" trigger tower energy must be greater than a threshold, the "had" to "em" ratio must be very small, and if isolation is to be achieved in Level 1, the surrounding towers must contain only small amounts of energy. For jet identification, the sum of a tower matrix must be tested against a threshold. To distinguish neutrinos, the E_τ sum must be compared with a threshold (see Figure 1). An isolated electron should be recognized by a large amount of energy deposited in a small area (about 1 tower wide) while a jet's energy should be spread out covering a large matrix of calorimeter towers. Figure 2 show the flow-chart of the algorithm that executes two "em" sum + front-to-back + isolation + jet finding.

*Operated by the Universities Research Association, Inc., for the U.S. Department of Energy under Contract No. DE–AC35–89ER40486.

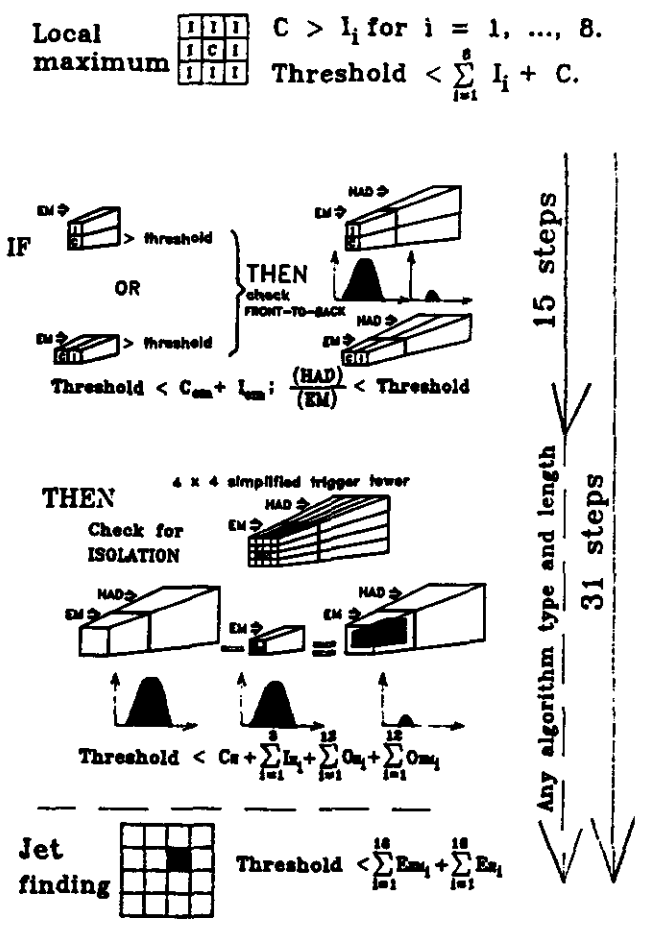

FIGURE 1. Trigger algorithms examples.

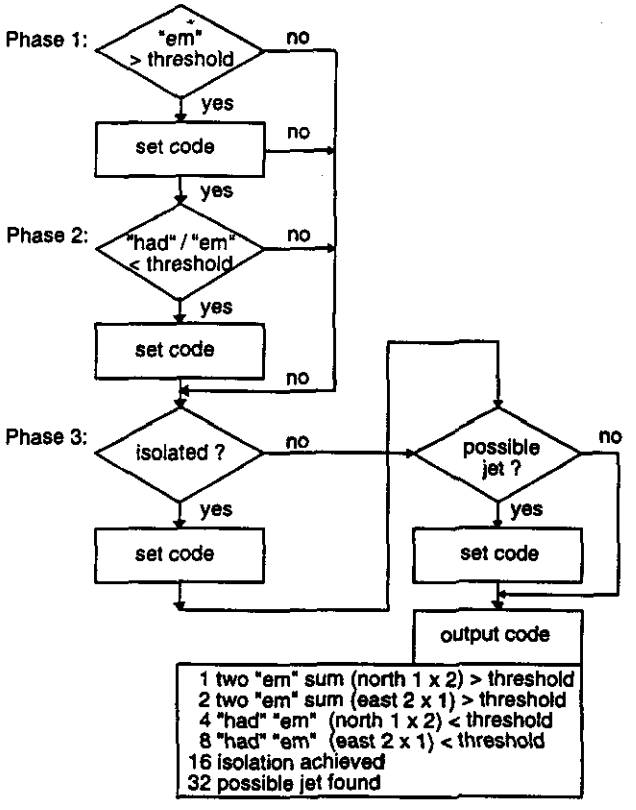

FIGURE 2. Algorithms flow-chart. For example, a 3D-Flow may return a code 37 (1+4+32) stating that a possible electron was found, but it was not isolated from the surrounding energy, and that cell may be part of a 4 × 4 jet.

III. 3D-Flow Processor Architecture

The architecture of the 3D-Flow processor is shown in Figure 3. The 3D-Flow operates on a data-driven principle. Program execution is controlled by the presence of the data at the five ports (North, East, West, South, and Top) according to the instructions being executed. A clock running at a frequency of 60 (or 120) MHz synchronizes the operation of the cells.[4]

IV. 3D-Flow Pipelined Parallel-Processing Architecture

Figure 4 shows the 3D-Flow processor in a pipelined parallel-processing architecture.[5] The program execution at stage 1 must not only route the new incoming data from the calorimeter to the next stage in the pipeline staging (stage 2), but must also execute its trigger algorithm. A graphical representation of the input and output results and the data flow in the pipelined architecture are shown in the timing diagram of Figure 5.

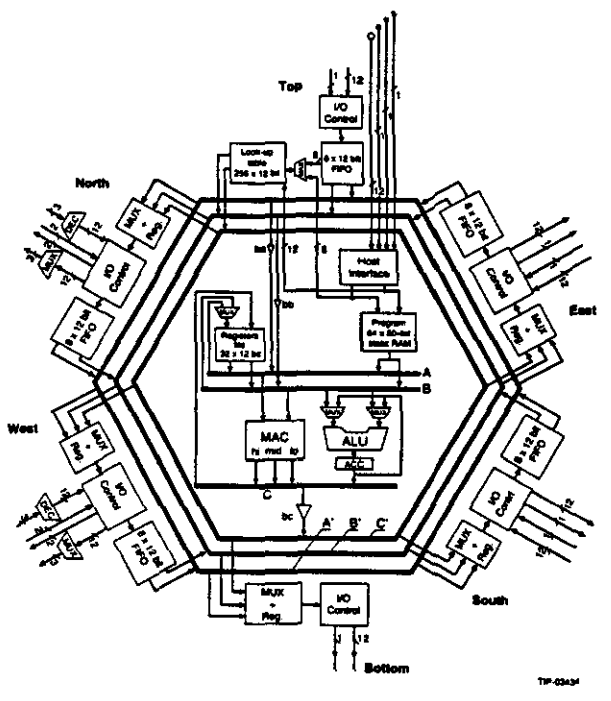

FIGURE 3. 3D-Flow cell architecture.

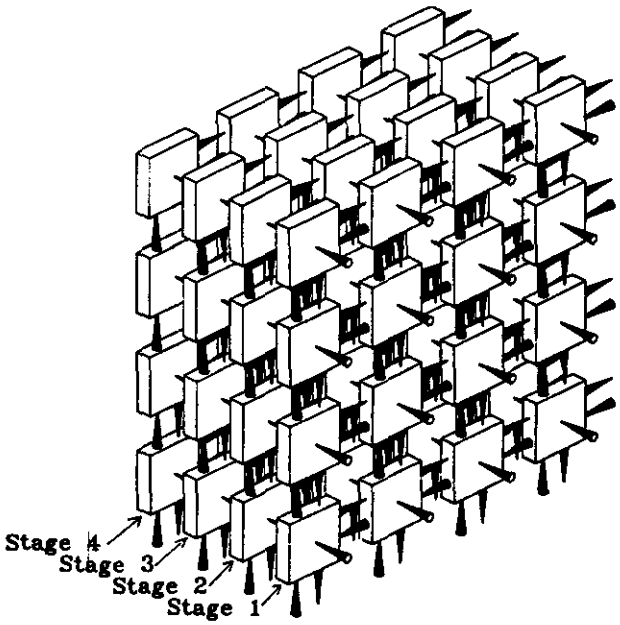

FIGURE 4. General scheme of the pipelined parallel-processing architecture using the 3D-Flow.

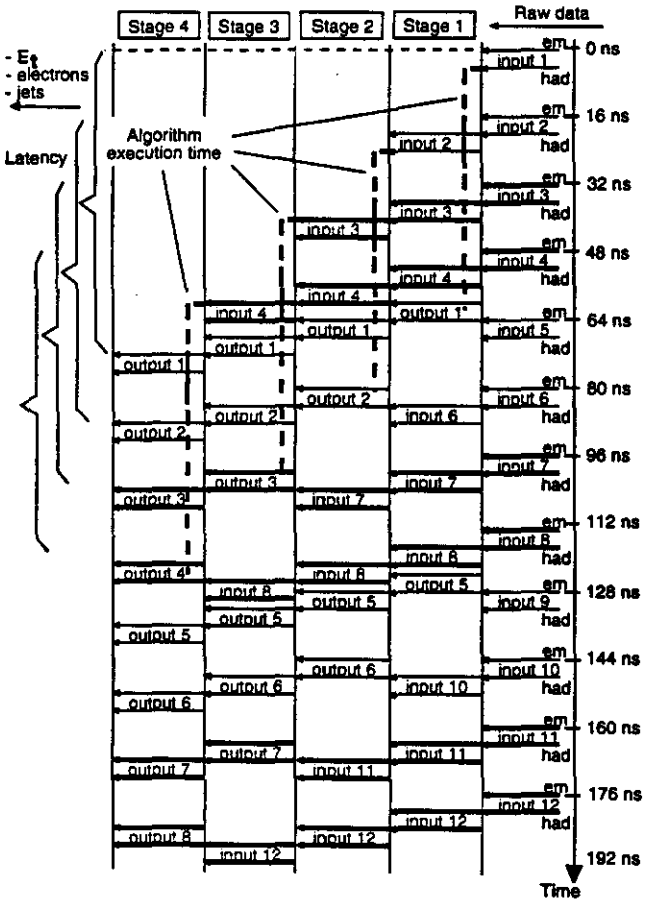

FIGURE 5. Timing diagram of four stages of pipelined programmable Level-1 trigger.

V. 3D-Flow Chip Assembly And Board Assembly

Preferably the assembly of the chip should be in a good thermoconducting package with good power and ground distribution, such as the 447 Ceramic Pin Grid Array with 96 pins of Vcc and Gnd. Feasibility studies demonstrate that with present technology a 3D-Flow chip consuming 8 W, and accommodating 32 processors at 60 MHz can be built today, and that the same chip can be built one year from now at a 120-MHz clock rate. Figure 6 shows an assembly of 8 × 3D-Flow chips on a single board, thus making it possible to analyze calorimeter channels relative to a 0.4 × 0.4.

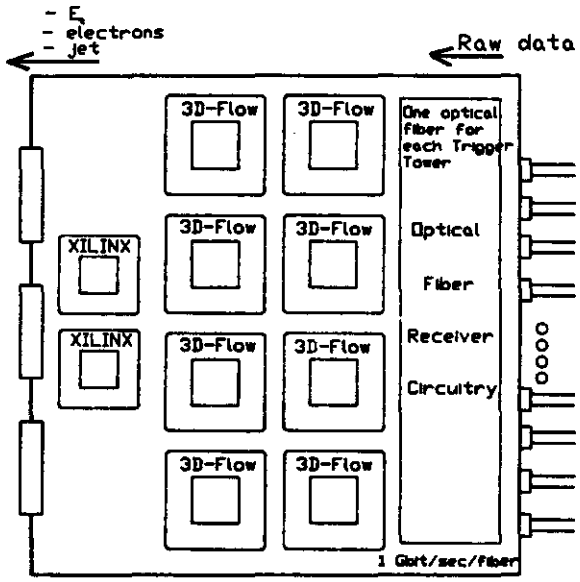

FIGURE 6. Board of the programmable Level-1 trigger with 3D-Flow array.

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