GEM TN-92-87

Central Tracker Meeting - SSCL

April 2, 1992

Abstract:

Transparencies of the presentations at the April 2, 1992 meeting at the SSCL. Included are capacitance calculations and measurements for the IPC pads, status reports for Silicon Tracker, IPC electronics, simulations, and integration. A short discussion of test beam possibilities at SLAC is also included.

04/08/92-KM

Central Tracker Meeting

1. Software & Physics Studies — S. McKee
2. Silicon Tracker optimization — D. Lee, R. Barber
3. Pad layout optimization — B. Yu
4. Pad chamber parameters & Electronics issues — J. Musser
5. Test Beam possibilities at SLAC — J. Venuti
6. Integration Issues — K. Morgan

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Presentation By:

Shawn McKee

Central Tracking Simulations Meeting

April 3, 1992

AGENDA

Parameterization Code: CTFAST1

1) Current Status: Working code is in place on PDSF
CTMAT needs to be upgraded to include
a) Vertex along beam axis
b) Charged particles differences
CTMEAS needs to be upgraded to include
a) Vertex along beam axis

2) Additional requests: The physics/simulations people have requested some additional capabilities from CTFAST1:

1.) Efficiency to construct a complete track (including effects of luminosity, topology).

2.) Efficiency to find a track stub in front of a calorimeter cell.

3.) Multi-track resolution, particularly as it relates to \tau identification.

3) Work division for FAST1

GEANT MC Code:

1) Current status: Initial mass distribution version within days of appearing on PDSF

2) Division of work/Interests

We need work on the following:

a) Track finding/pattern recognition
(Los Alamos, Taiwan)

b) Lepto-quark physics
(Yale)

c) Coding of realistic detector responses (IPCs)
(IU, Michigan, Yale)

d) Vertex tagging/B and Tau physics
(Albany)

e) Higgs to Gamma Gamma (misidentified electrons)
(?) Los Alamos

Gluino Pairs
f) Charge sign determination physics (W+ scat.)
(SSCL-Jenny Thomas? Yale)

g) FAST1 upkeep with GEANT MC code
(Michigan?)

h) Others?
Calibrations using data? Frequency of calibrations?
Material in tracker - is there a physics process which can act as our "canary"?

3) Timeline/Deadlines? Should we be setting specific dates for completion of various studies?

4) Code management and coding standards

We need to discuss how the code management and revision control will function. Also, a discussion of minimal code requirements is needed for ease of transfer of code between systems.

Weekly updates/reports: We need to discuss how to funnel information about ongoing work back to a single source for distribution. The physics group has requested weekly reports. Each institution needs a contact person to be responsible for collecting info about their CT effort.

Other subjects? Assignment of responsible persons for each physics working group.

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Presentation By:

Dave Lee

Dave Lee

Work in Progress

1 Pattern Recognition

a. Improve Pattern Recognition

b. Correct Covariance Error Matrix for Fit

2 Update Silicon Geometry

3 Include Complete Coordinate Inefficiencies

a Dead Time

b Dead Strip

c Electronic Noise

d Dead Spaces

IPC Geometry

a Implement IU Geometry into Geant

b Ship to SSC for Shawn to Debug and Distribute

Questions

Who is responsible for completing Pad Software?

BROOKS

LOS ALAMOS SIMULATION STATUS

Silicon Geomtry

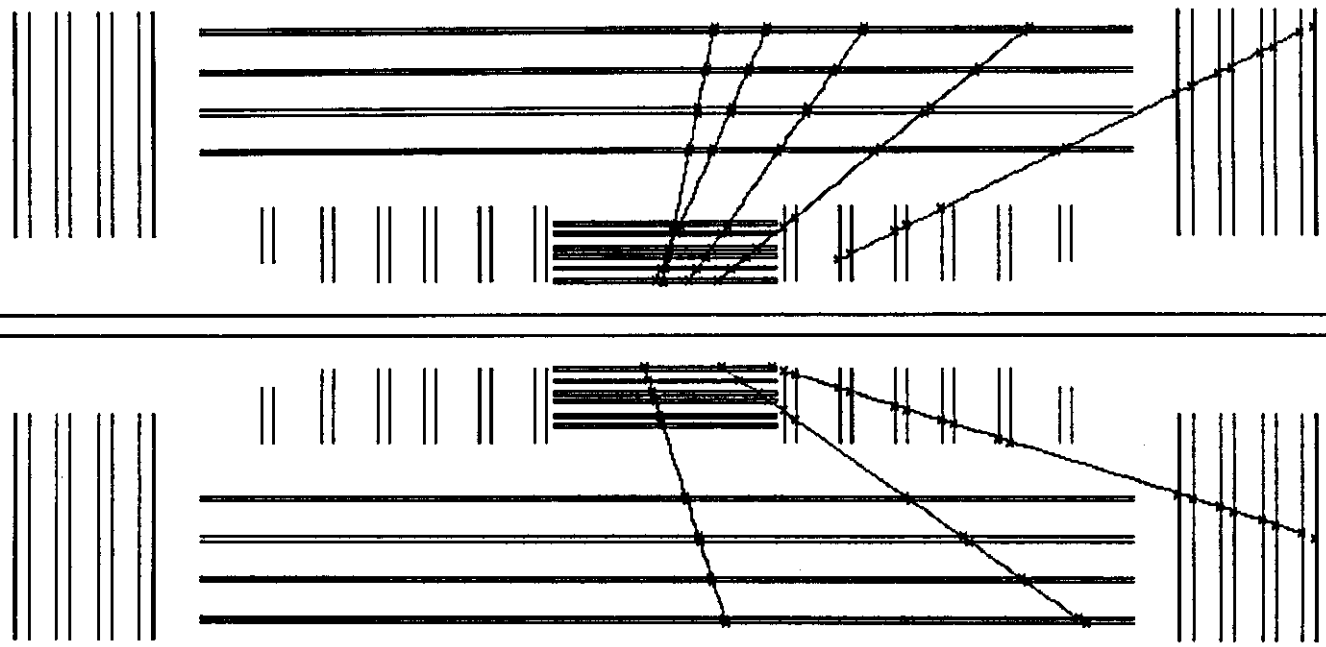
1. Silicon Baseline Geometry Installed
2. Correct 2mm overlap
3. Support Structure (Barrel)
   a. Mechanical is up-to-date
   b. Electronics - still to be done (now- +30% of Si)
4. Pattern Recognition
   a. fit track in Silicon
   b. fit track in Pads
   c. join both

Fast Parameterization

1. provided tables for
   a. deltap/p vs. eta and p
   b. deltap/p (vertex constraint) vs. eta and p
   c. impact parameter vs. eta and p

BROOKS 4/1/92 DML

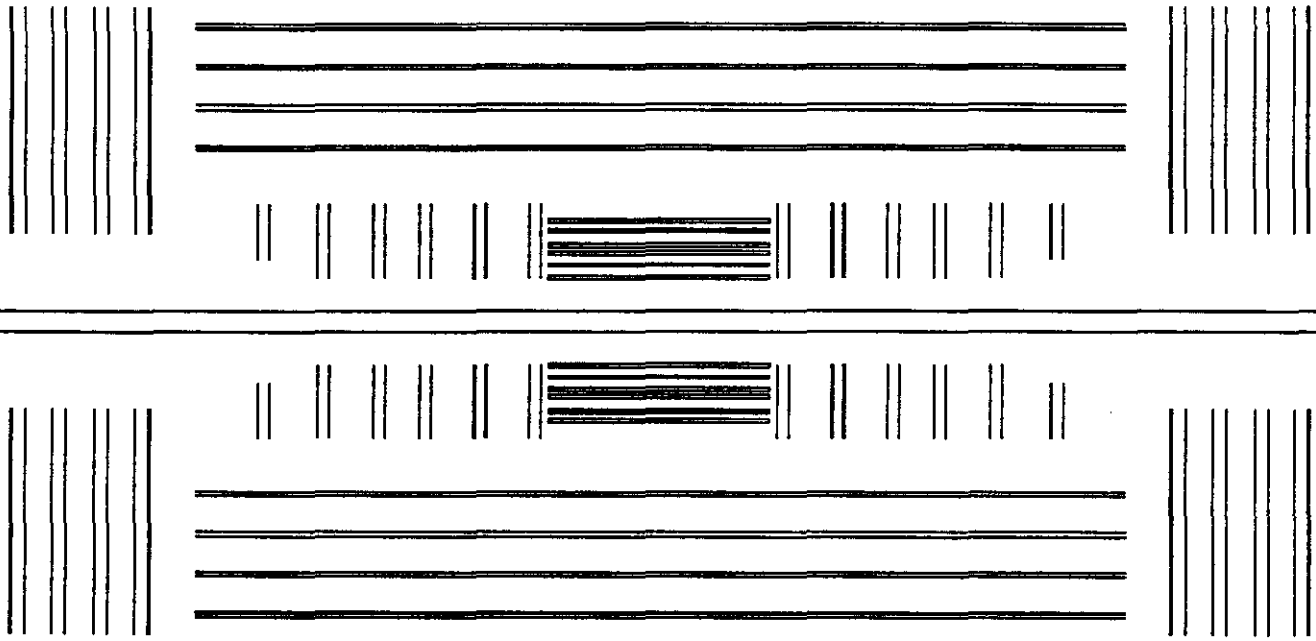
LSDT RUN NR 1
EVENT NR 0 1/ 4/92



BROOKS

Los Alamos

LSDT RUN NR 1 EVENT NR 0 1/ 4/92



BROOKS

Los Alamos

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Presentation By:

Ron Barber

See further

Mechanical Engineering Priorities

Preparation for the Cost Review

- Develop drawings with enough detail to get vendor estimates
- Accurately refine the designs
- Develop documentation to substantiate the cost estimates
- Follow up later with analysis to technically substantiate the design

Develop a plan to begin Si Wafer production by FY 94 or earlier

- Develop R&D and fabrication plans with vendors
- Advance Si Wafer and Ladder details
  Design, Assembly, Testing
- Develop prototypes - evaluate assembly processes } Not funded, but critical to meeting the schedule!!
- Testing of prototypes

Revised: 4/1/92

Preparation for the ~~April 14th~~ May 7th Cost Review

	Tasks	Individuals	Completion
1.	Facility Requirements Input (GEFUR)	Morgan	3/
	Mechanical Requirements	Barber/Emmet	
	Electronic Requirements	Cooke/Musser	
2.	Silicon Tracker Baseline Parameters	Barber	
	IPC Tracker Baseline Parameters	Emmet	
	Central Tracker Cabling & Utility Req.	ALL/Barber	
3.	Cost Estimate (Drawings Specs. and Cost documentation)		
	Silicon Tracker Design		
	Mechanical Design	Barber	
	Si Detectors/Subassemblies	Barber	
	Tooling	Barber/Michaud	
	Gas Enclosure	Barber/Thompson	
	Poly Shield	Johnson	
	Kinematic Mounts	Barber	
	Cooling Rings/Support Cyl.	Thompson	
	Space Frame	Thompson	
	Cooling System	Woloshun/Van Anne	
	Alignment Systems	Hanlon	
	Electronics Design		
	Analog/Digital/Hybrid	Hahn	
	Optical Driver & readout	Hahn	
	Data Acquisition System	Cooke	
	Power Distribution	Cooke	
	Silicon Tracker Assembly	Barber/Hahn/Mills	
	Beam Tube Design	Barber	
	Getter Pump Design	Chapman	
	IPC Tracker Design		
	Mechanical Design	Emmet	
	Module Assembly	Emmet	
	Truss Core/Stability	Thompson	
	Cathodes/Leads	Emmet/Michigan	
	Anode Wire	Emmet	
	Gas Enclosure	Emmet	
	Module Interface	Emmet/Thompson	
	Space Frame	Thompson	
	Cooling System	Woloshun	
	Gas Supply System	Woloshum	

	Electronics Design		Musser	
	Front End Electronics			
	LED/Readout system			
	Power Supply/Distribution			
	Packaging/Cooling Interface		Musser/Woloshun	
	IPC Assembly		Emmet	
	SSCL Si/IPC Tracker Assembly		Barber/Morgan	
	SSCL Calibration and Testing			
	SSCL Installation and hookup			
	Proj Management		Baltay	
5.	Meetings Eng 2C	Integration Tracker	SSCL	3/25
			SSCL	4/2
		Integration Tracker	SSCL	4/27-28 4/30
7.	Publication of cost book		R.Barber H. Pretty	5/1
8.	Cost presentation		All	5/7 ??

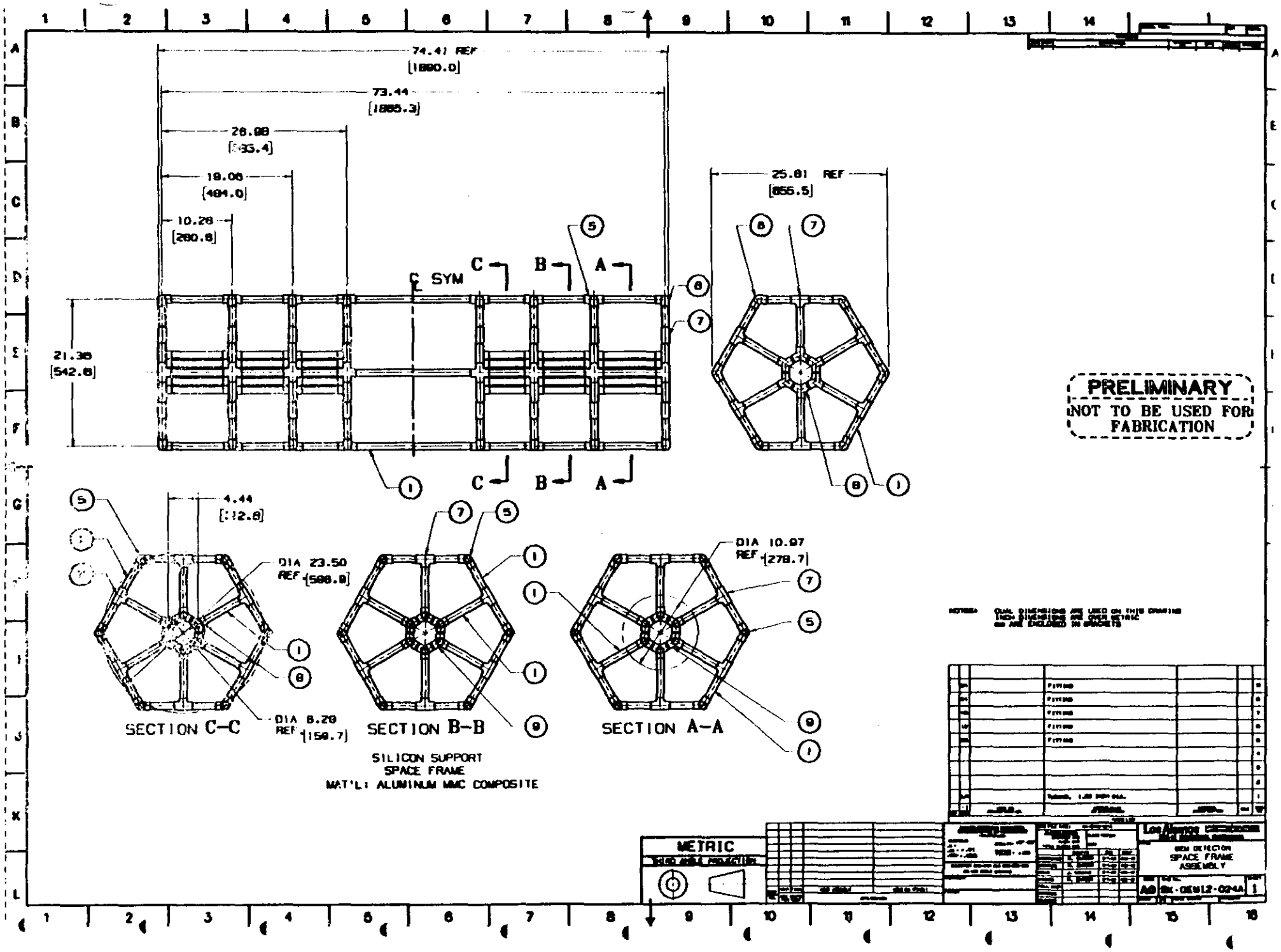
CENTRAL TRACKER SYSTEM COST ESTIMATE

WBS No.	Title	Engineering & Design			M & S	Inspection Q/A			Proc/Fab	Installation/ Assembly					Totals				
		Labor	Rate	Total	Materials	Labor	Rate	Total	Material	Labor	Rate	Subtotal	Material	Total	Labor	Material	Subtotal	Contin.	Total K$
5.2.2.3.5	Central Tracker Subsystem																		
5.1	Silicon Tracker	22	100	2200	440	8	91	724	7087	19	74	1403	460	1863	4447	7957	12404	4102	16507
5.1.1	Mechanical Struc. & Cooling	18.2	104	1896	364	4.5	90	406	3165	12.5	73	911	330	1241	3213	3859	7072	2460	9532
5.1.1.1	Central Region SubAssemblies	3.5	109	380	70	0.8	85	68	720	2.9	69	199	90	289	647	880	1527	501	2028
5.1.1.1.1	Cen. Reg. Cooling Rings	1.2	97	116	24	0.3	80	24	472	0.5	96	48	35	83	188	538	726	290	1016
5.1.1.1.2	Kinematic Mounts	0.5	96	48	10	0.1	80	8	81	0.2	80	16	10	26	72	101	173	43	216
5.1.1.1.3	Assembly Tooling	1.3	123	160	26	0.2	80	16	120	0.5	83	41	25	66	217	171	388	85	474
5.1.1.1.4	Assembly	0.5	112	56	10	0.2	100	20	40	1.7	55	94	20	114	170	70	240	82	322
5.1.1.2	Forward Region Subassemblies	2.5	99	248	50	0.9	93	84	552	2.6	69	180	75	255	512	677	1189	406	1595
5.1.1.2.1	Fwd. Reg. Cooling Rings	1	96	96	20	0.5	96	48	380	0.4	90	36	35	71	180	438	618	247	865
5.1.1.2.2	Kinematic Mounts	0.5	96	48	10	0.1	80	8	109	0.2	80	16	10	26	72	129	201	50	251
5.1.1.2.3	Assembly Tooling	0.5	96	48	10	0.1	80	8	40	0.3	80	24	10	34	80	60	140	31	171
5.1.1.2.4	Assembly	0.5	112	56	10	0.2	100	20	20	1.7	61	104	20	124	180	50	230	78	308
5.1.1.3	Central Region Support Cylinders	1.3	108	136	26	0.3	93	28	127	0.4	75	30	10	40	194	163	357	101	458
5.1.1.3.1	Composite Cylinders	0.8	105	84	16	0.2	100	20	95	0.2	70	14	5	19	118	116	234	70	304
5.1.1.3.2	Kinematic Mounts	0.5	104	52	10	0.1	80	8	32	0.2	80	16	5	21	76	47	123	31	154
5.1.1.4	Space Frame	1	100	100	20	0.3	80	24	400	0.8	81	65	10	75	189	430	619	248	867
5.1.1.5	Gas Enclosure	3.4	100	368	68	0.6	87	52	504	0.8	71	57	40	97	477	612	1089	378	1467
5.1.1.5.1	Outer Enclosure	2	110	220	40	0.4	90	36	344	0.4	75	30	15	45	286	399	685	233	918
5.1.1.5.2	Inner Enclosure	0.8	110	88	16	0.1	80	8	96	0.2	68	14	10	24	110	124	234	84	318
5.1.1.5.3	End Enclosures	0.6	100	60	12	0.1	80	8	62	0.2	68	14	15	29	82	89	171	61	232
5.1.1.6	Detector Supports	1.1	98	108	22	0.2	80	16	102	0.5	76	38	15	53	162	139	301	106	407
5.1.1.6.1	End Supports	0.6	100	60	12	0.1	80	8	85	0.1	80	8	5	13	76	102	178	75	253
5.1.1.6.2	Kinematic Mounts	0.5	96	48	10	0.1	80	8	17	0.4	75	30	10	40	86	37	123	31	154
5.1.1.7	Cooling System	1.9	103	196	38	0.3	93	28	350	2.1	74	156	50	206	380	438	818	218	1033
5.1.1.8	Alignment System and Instrument	3.4	104	352	68	1	98	98	380	1.9	78	149	20	169	599	468	1067	483	1550
5.1.1.8.1	Shell Assy Optical System	1.3	108	140	26	0.3	93	28	130	0.7	86	60	10	70	228	166	394	225	619
5.1.1.8.2	Internal Optical System	1.5	101	152	30	0.3	100	30	155	0.8	78	62	5	67	244	190	434	191	625
5.1.1.8.3	Assy and Installation Alignment Sy	0.6	100	60	12	0.4	100	40	95	0.4	68	27	5	32	127	112	239	67	306
5.1.1.9	Shipping	0.1	80	8	2	0.1	80	8	30	0.5	74	37	20	57	53	52	105	22	127
5.1.2	Silicon Detector	3.3	110	364	66	2	84	168	3606	4.4	85	372	110	482	904	3782	4686	1406	6092
	Vacuum Beam Tube								74						0	0	0	0	0
	Polyethylene								31						0	78	78	23	98
	SSCL Assembly														0	31	31	9	40
															0	0	0	0	0
															0	0	0	0	0
5.1.5	Detector Calibration and Testing	0.5	120	60	10	1.5	100	150	100	2	60	120	20	140	330	210	540	205	745

Note: Move SSCL Assembly to 5.4

−.4M$

+.6M$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SECTION C–C
SECTION B–B
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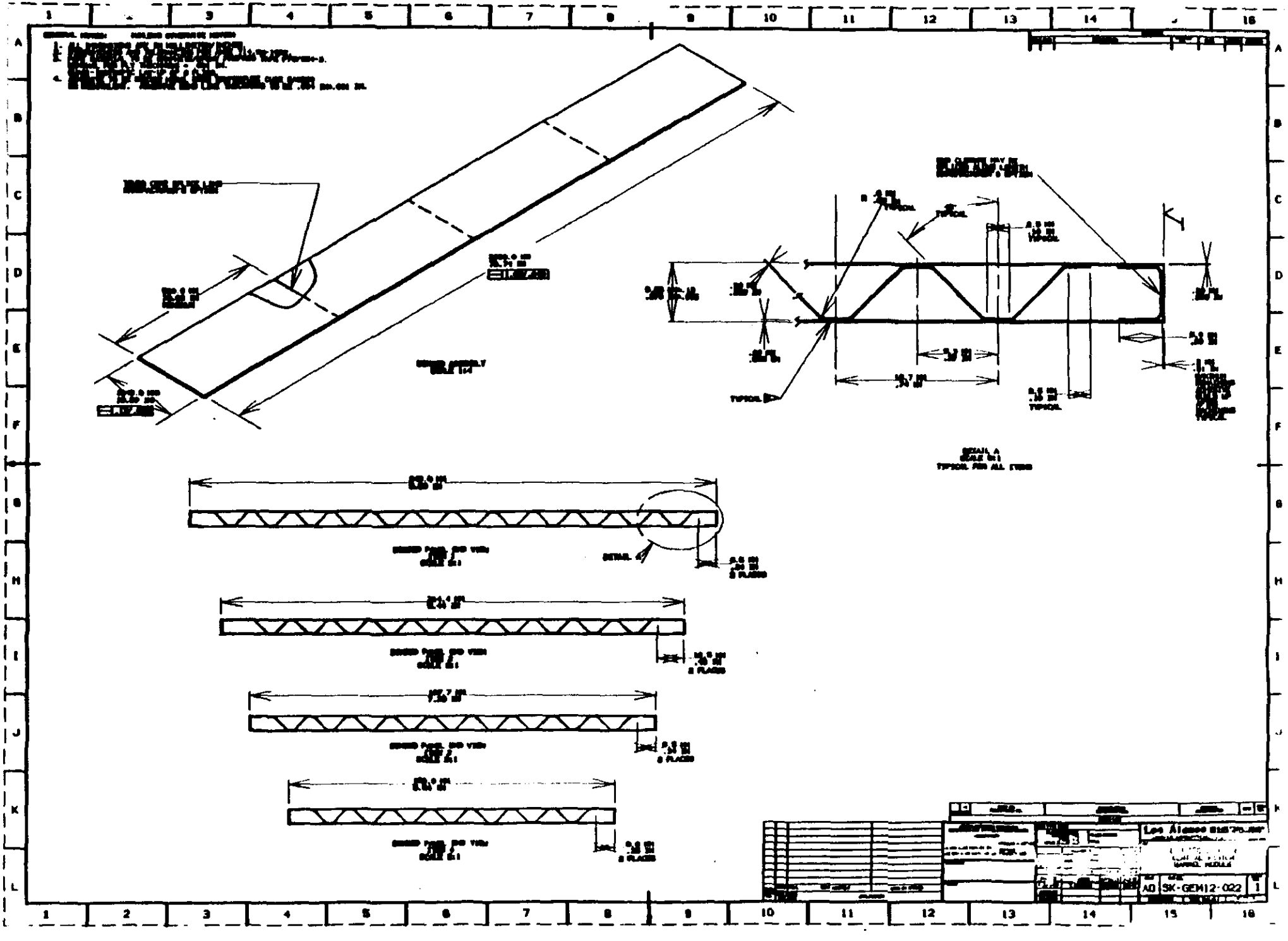
SILICON SUPPORT
SPACE FRAME
MAT'L: ALUMINUM MMC COMPOSITE
PRELIMINARY
NOT TO BE USED FOR
FABRICATION
METRIC
THIRD ANGLE PROJECTION
Los Alamos
SPACE FRAME
ASSEMBLY
A0
1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TYPICAL
TYPICAL
TYPICAL
DETAIL A
SCALE 1:1
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DETAIL
2 PLACES
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2 PLACES
Los Alamos
A0
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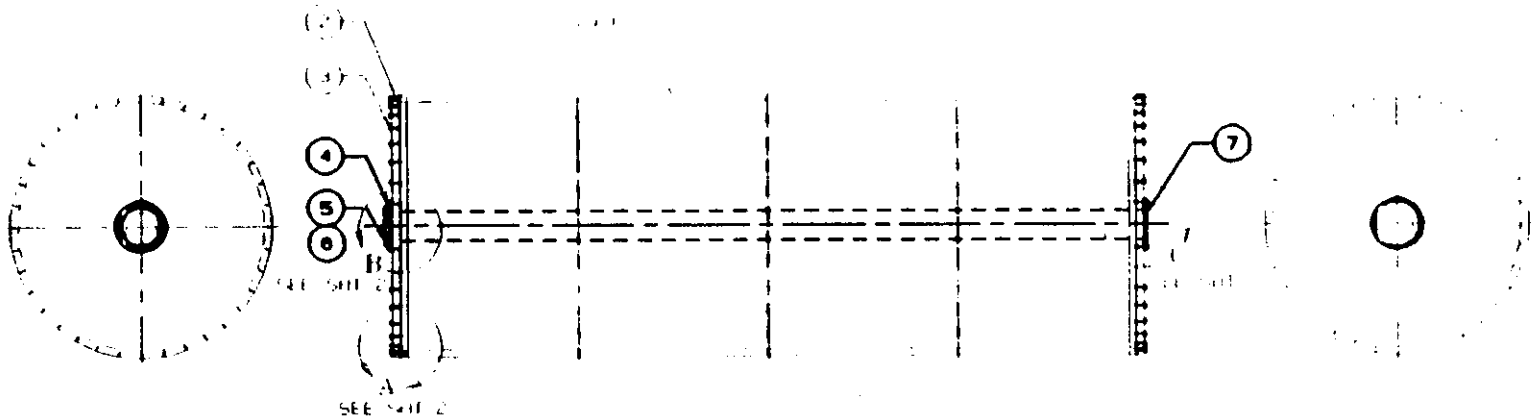

MATERIAL OPTIONS:
1. GRAPHITE EPOXY (P75/954-3)
   QUASI ISOTROPIC LAYUP (0°/±45°/90°)
2. HEXCELL HFTG-327-3/16-4.0
   GRAPHITE/POLYEMIDE HONEYCOMB

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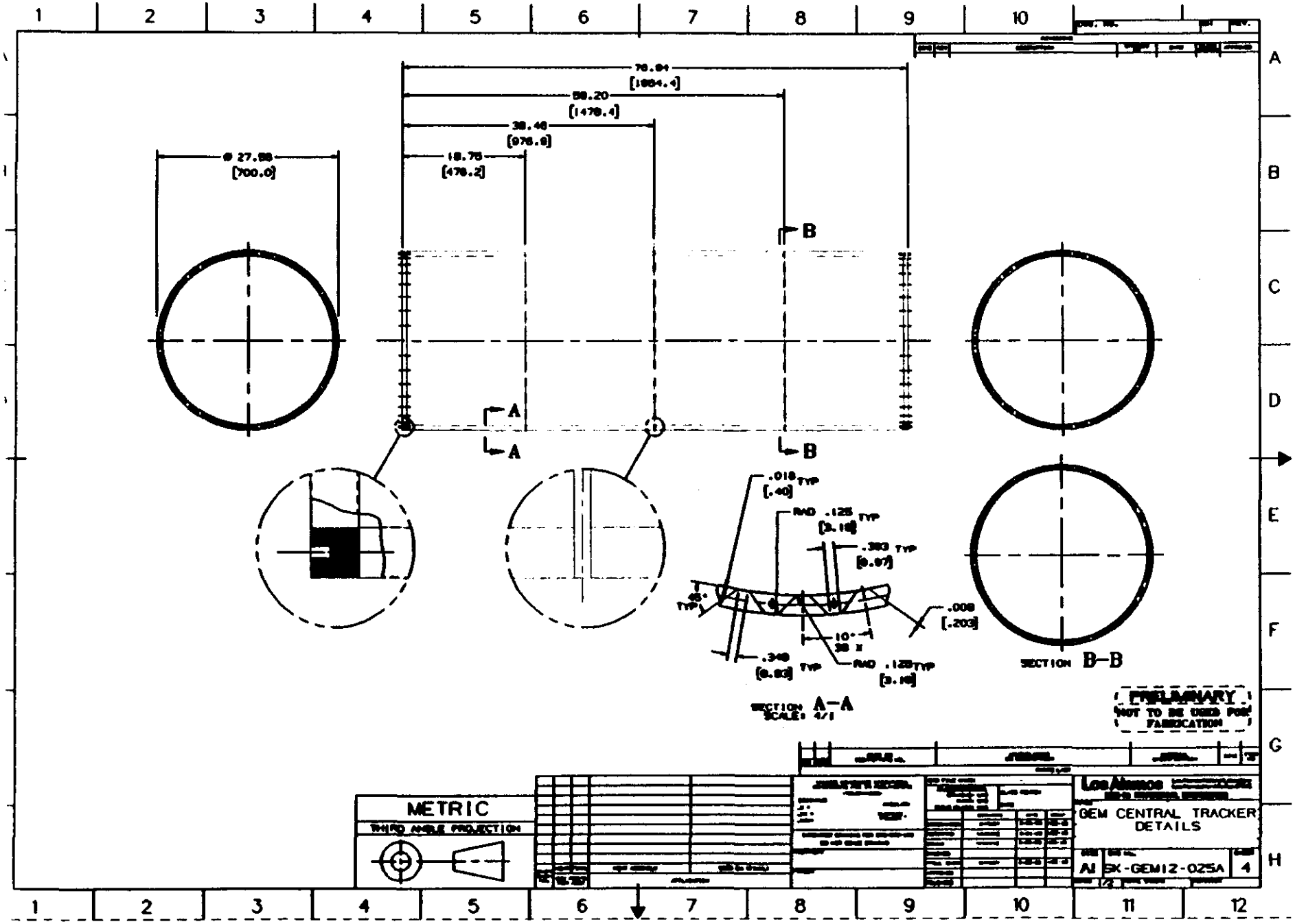
METRIC
THIRD ANGLE PROJECTION

Los Alamos

GEM CENTRAL TRACKER
GAS ENCLOSURE

A1 SX-GEM12-025A 1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38 X
.348
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RAD .125 TYP
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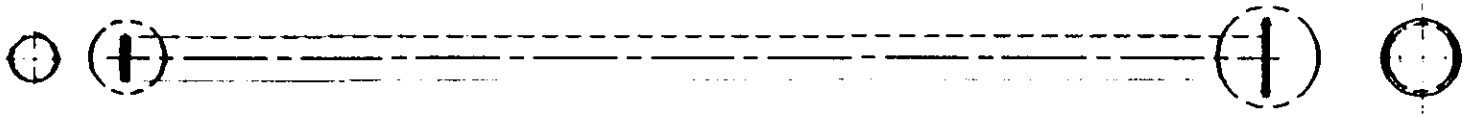
SCALE: 4/1
SECTION B–B
PRELIMINARY
NOT TO BE USED FOR FABRICATION
METRIC
THIRD ANGLE PROJECTION
Los Alamos
GEM CENTRAL TRACKER DETAILS
A1
SK-GEM12-025A
4



Inner Be enclosure
.5 - 1 mm thick

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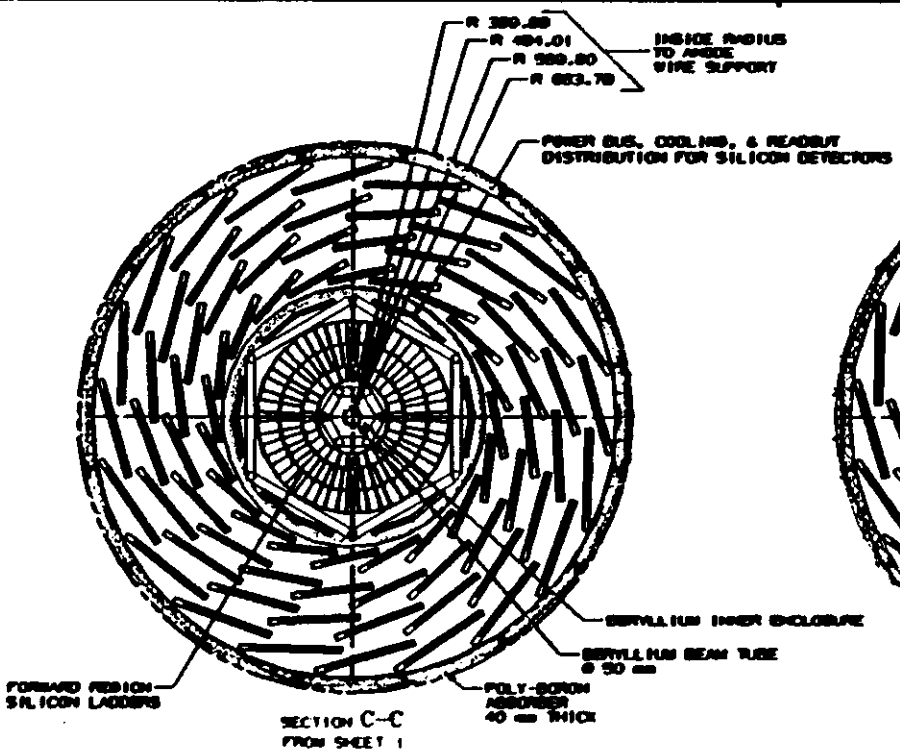
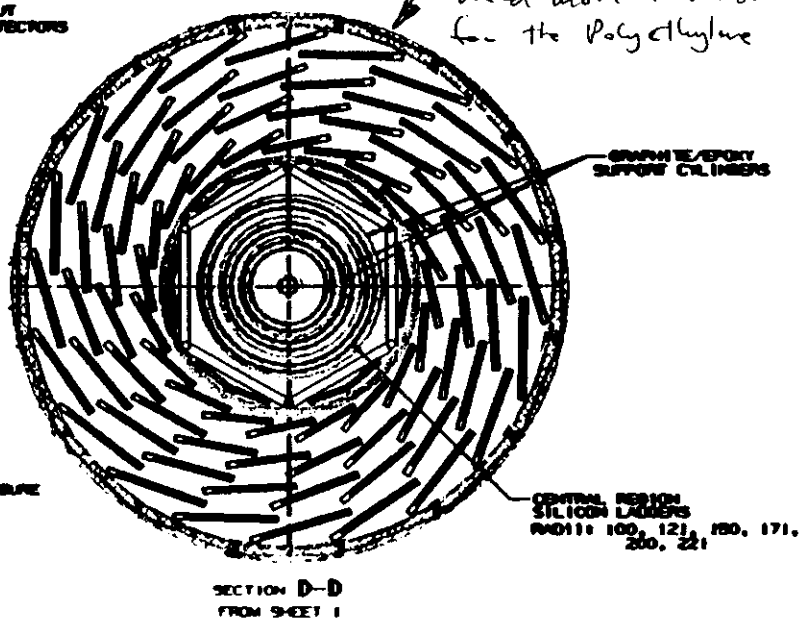


Note: We may need more Radial clearance for the Polyethylene



METRIC

THIRD ANGLE PROJECTION

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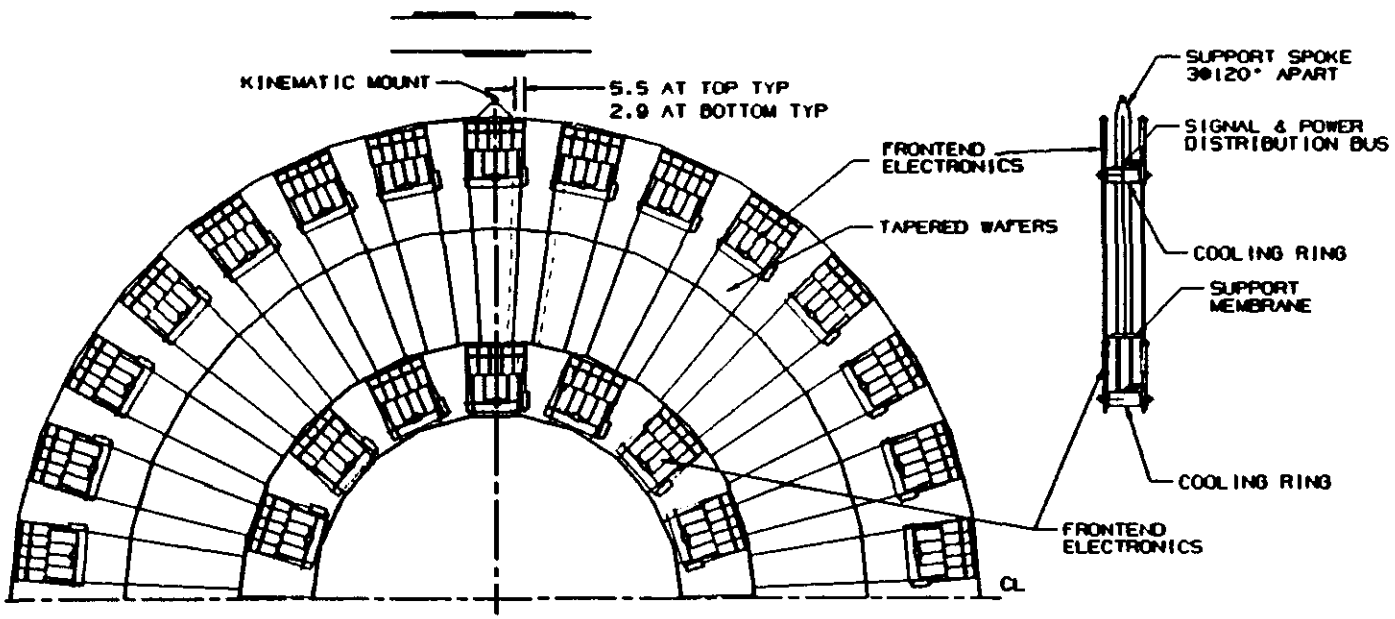
GEM CENTRAL TRACKER WORKING LAYOUT

A1 SK-GEM12-009C 3

GEM SILICON TRACKER

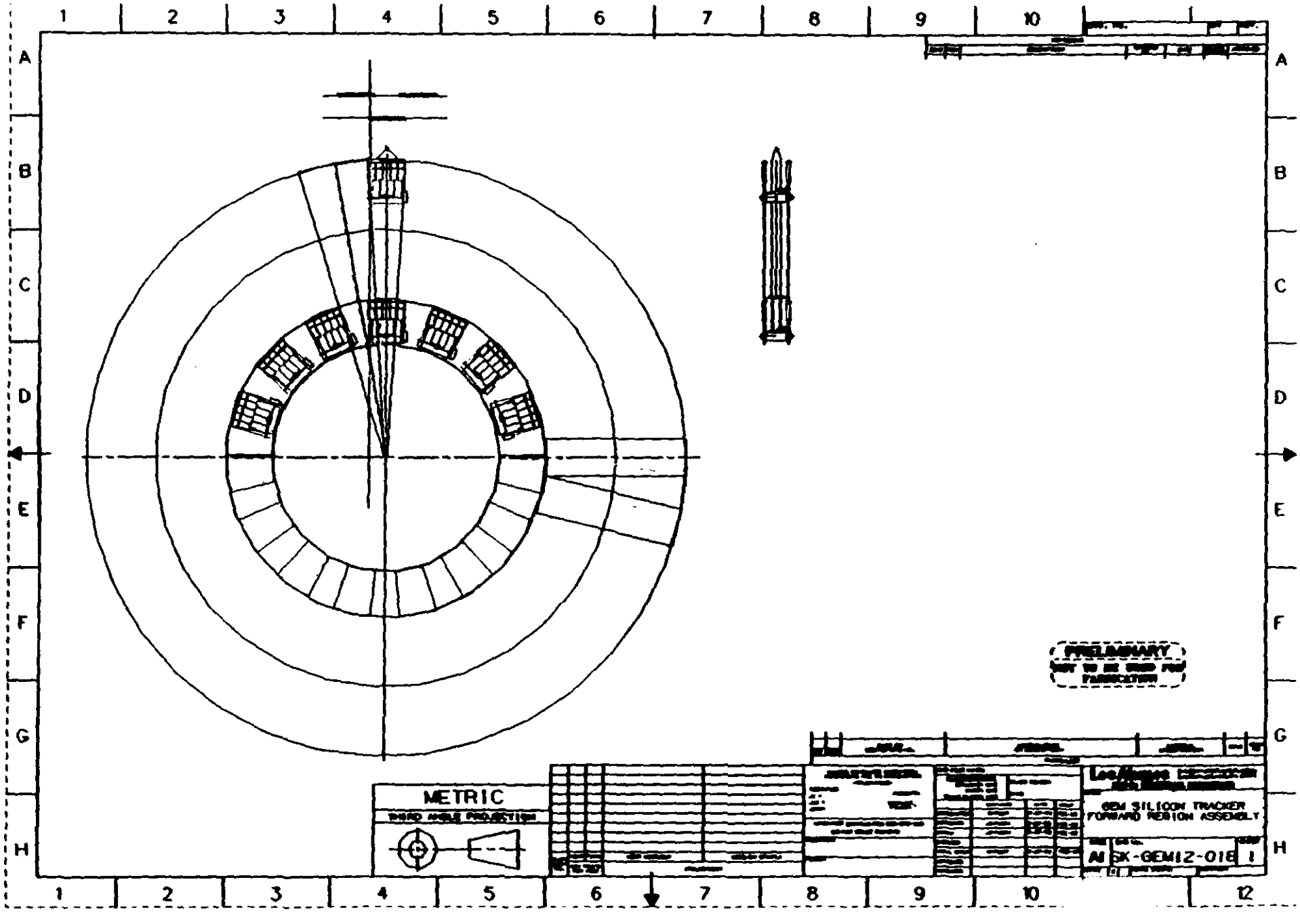
FORWARD REGION SUBASSEMBLY



ALL DIMENSIONS ARE IN mm

LOS ALAMOS

MEE-12
MECHANICAL AND ELECTRONIC ENGINEERING DIVISION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THIRD ANGLE PROJECTION
GEM SILICON TRACKER
FORWARD REGION ASSEMBLY
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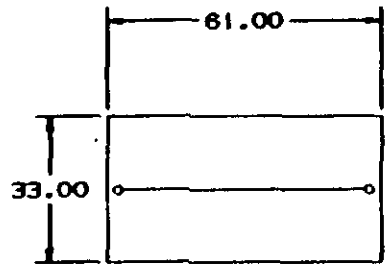
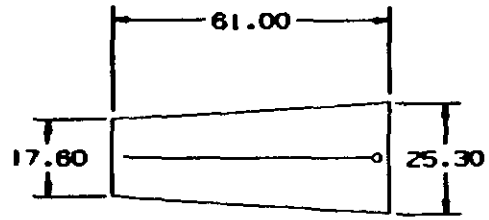
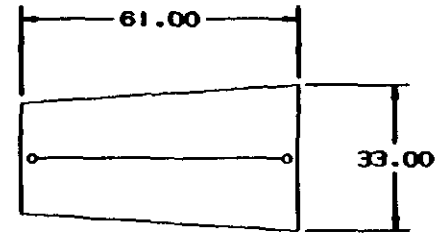


PAD BOTH ENDS

(1) QUANTITY:1614 EACH FOR X LAYER
QUANTITY:1614 EACH FOR STEREO LAYER
TOTAL OF 3228 WAFERS

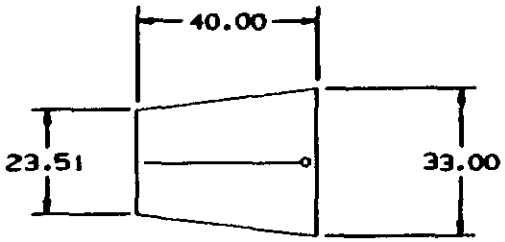


PAD ONE END



PAD BOTH ENDS

(2) QUANTITY:1266 EACH FOR X LAYER
QUANTITY:1266 EACH FOR STEREO LAYER
TOTAL OF 5064 WAFERS



PAD ONE END

(3) QUANTITY:456 EACH FOR X LAYER
QUANTITY:456 EACH FOR STEREO LAYER
TOTAL OF 912 WAFERS

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NOTES:

1. FOR WAFER SPECIFICATIONS REFER TO WAFER DRAWING SK-GEMI2-001 & SK-GEMI2-002

METRIC
THIRD ANGLE PROJECTION

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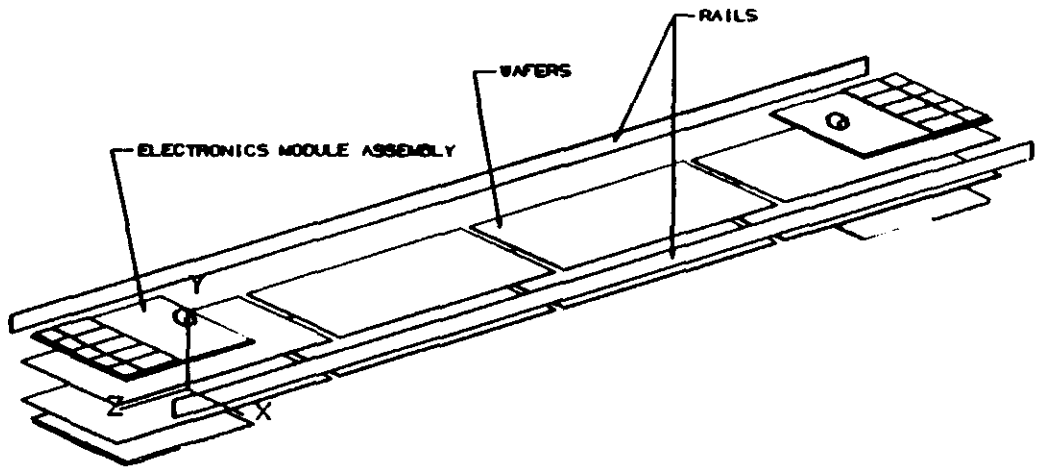
SILICON WAFER GEOMETRIES

A1 SK-GEMI2-007A 1



PRELIMINARY
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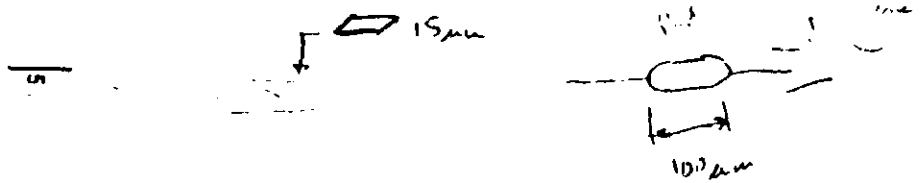
METRIC
THIRD ANGLE PROJECTION

Los Alamos

GEM SILICON TRACKER
EXPLODED LADDER ASSY

A1 SK-GEM12-026 1

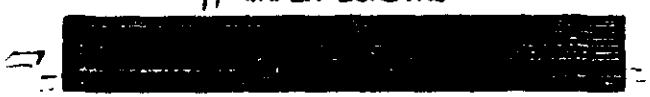


1. 50μm gaps for Adhesive
2. Adhesive:
3. Adhesive excess: flush on the backside
   Excess allowed on the top side
4. Strip Strengthens profile: 8μm for each 12 cm ladder; 20μm overall 24cm ladder
5. Flatness profile 15μm
6. Inspection tests:

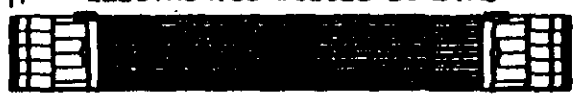
1. 150μm Adhesive thickness
2. Adhesive:
3. Bond area
4. Pad to Pad profile 20μm

1. 640 wafer to wafer (2 times)
   640 wafer to Elec. MCM (2 times)
2. Wire type
3. Percentage of wire breaks ___

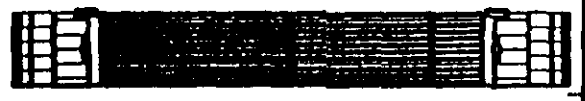
WAFER BONDING



ELECTRONICS MODULE BONDING



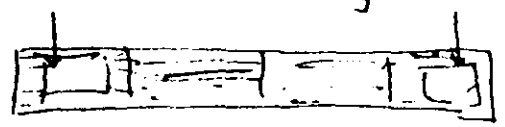
WIRE BONDING



BACK TO BACK BONDING

RAIL BONDING

Final Testing



1. Serfes & Geoff Mills

PRELIMINARY
NOT TO BE USED FOR FABRICATION

1. Strip to Strip Tolerance
2. 50μm adhesive gap
   Adhesive type:
   Conductivity:
   Bond area
3. Flatness profile 10μm

1. 4mm high x 200μm wide rib
2. Bond thickness & fillet radius
   Adhesive type:
   Conductivity:
3. Rail positioning.

METRIC
THIRD ANGLE PROJECTION

Los Alamos
GEM CENTRAL TRACKER
LADDER ASSY STEPS

A1 SK-GEM12-026 2

gem

γeμ

Presentation By:

Geoffrey Mills

Silicon Electronics Developements

- **Non-Disclosure agreements Completed with:**

  Orbit Semiconductor: Received Design Rules
  UTMC

- **Non-Disclosure agreements in Progress with:**

  Motorola :
  - Multi-Chip Module Technology
  - MOSAIC Transistor Design
    - (14Ghz @200μA)

- **Front-End Electronics Block Diagram: First Attempt**

  Need additional custom chip for:
  - Inerface/Control
  - Line Driver/Receiver
  - Housekeeping(Stateof-Health):
    - Amplifier, A/D

  Cable Cost Estimates with Lenthor, PentaFlex

- **IC Cost estimates:**

  Yield plays an important role: $Y = \frac{1}{(1+dA)}$

  where :
  - d=# defects/area(d <100/in^2 for Harris UHF)
  - A=area

  for zero defects:
  - Y~ 0.2 for Harris UHF, A=6.4x6.4mm^2

  Need to optimize allowed channel failure rate, number of channels per wafer, and die size.

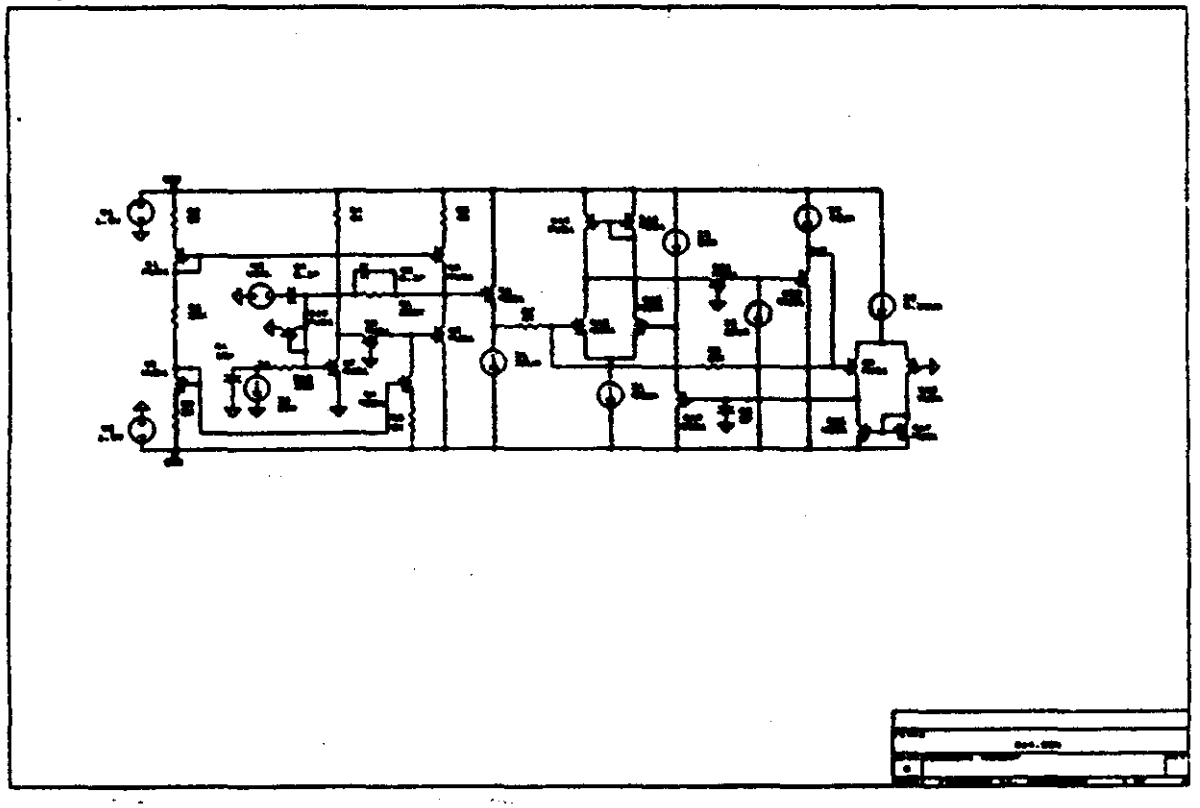
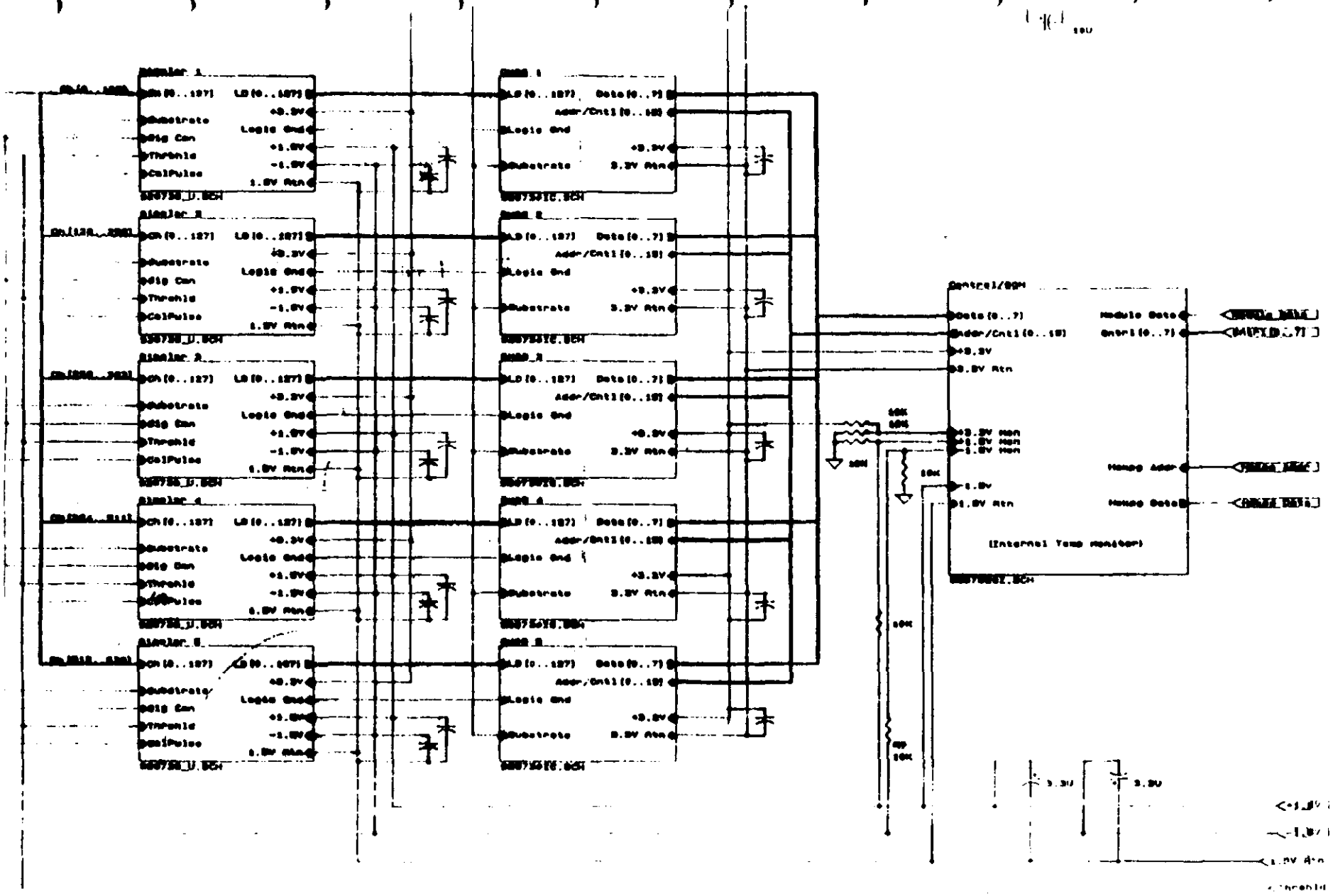
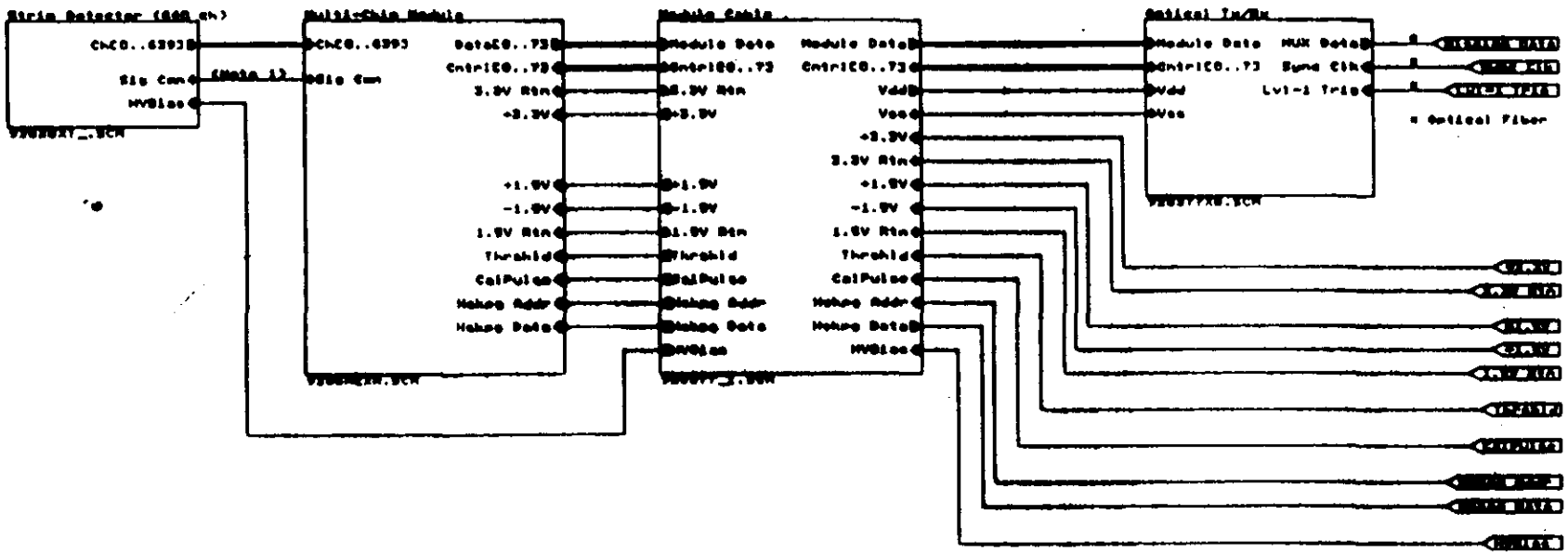


Figure 1a. Preamp/Shaper Schematic Used for SPICE Simulation


Control/SGM
Module Data
Hexag Addr
Hexag Data
(Internal Temp Monitor)
Substrate
Dig Cmn
Threhld
CalPulse
Logic Gnd
Addr/Cntl
3.3V Rtn
10K
3.3U



Los Alamos National Laboratory

Title

Si-Tracker Front-End, Electrical

gem

γeμ

Presentation By:

John Venuti

APRIL 2, 1992

TRACKER MEETING

John Venuti

TEST BEAMS AT S.L.A.C.

HISTORY:

* PAUL MOCKETT CONTACTED D. LEITH – 3/2/92
  1st INTEREST in SLAC T.B.'s

* JIM BRAU / J.V. CONTACTED ROGER Gearhart AND LOU KELLER ABOUT THE POSSIBILITIES OF USING SLAC TEST BEAM – 3/18/92
  ROGER + LOU WOULD LIKE TO GET T.B.'s BACK in OPERATIONS — NEED MONEY

* J.V. CONTACTED DAVID LEITH (3/31)
  VERY RECEPTIVE TO RESTORING BEAM LINE AND MAKING IT AVAILABLE TO "OUTSIDE" PHYSICS COMMUNITY – BUT – CANNOT MAKE DECISION UNTIL WITHERELL REPORTS TO D.E.

BEAM LINE-19 AT SLAC

* Will take ~ 1 year to commission; e^+ only

  COST: ~ \$250K - 400K

* $E_{max} \gtrsim 25$ GeV; 10 - 20 pps

  $$\frac{\Delta p}{p} = 0.2\%$$

* To run parasitic w/ End Station A experiment (E-142 Pol. e^-'s on pol. He^3 tgt)

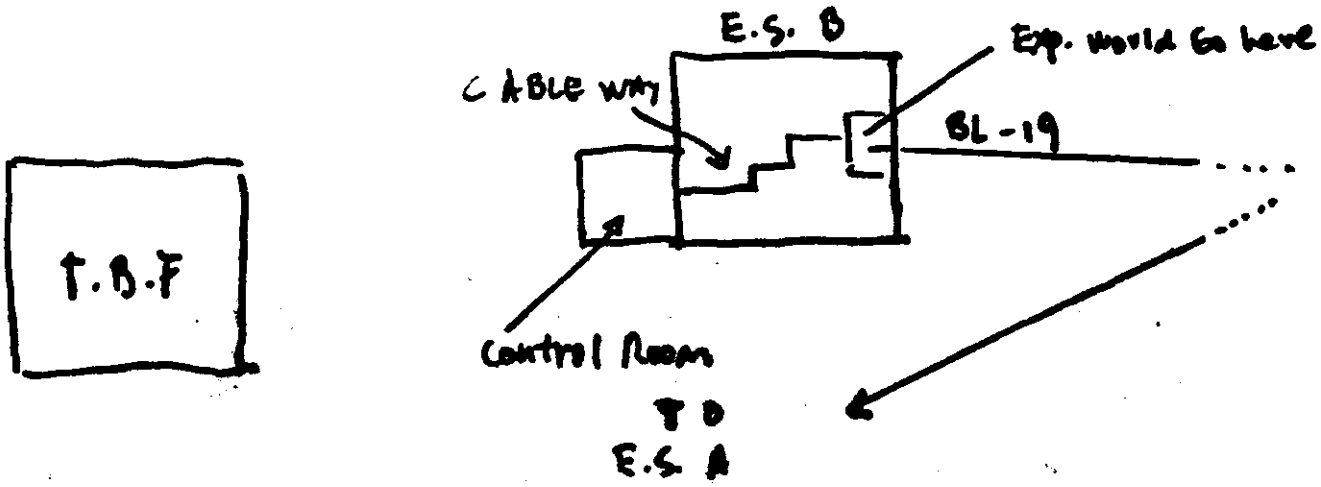
* Run time: ~ 3 mos./year

IF SLAC STARTED NOW (or before July '92)

- 3/92 - 3/93 to commission
- SLD to run 1/93 → ? (8/93)
- 1st opportunity to get test beam:

  ~ Fall of '93

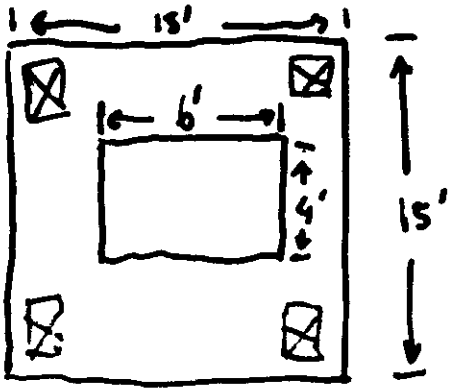
PHYSICAL LAYOUT



* AMPLE SPACE TO SET UP EXPERIMENT
* CABLE WAY IN PLACE WHICH LEADS TO CONTROL ROOM
* ACCESS TO VM/VMS ?? — DAQ?

IN TEST BEAM FACILITY (TBF)

* THERE IS A 1.3 or 1.6 T DIPOLE
* ROGER CLAIMS $\vec{B}$-FIELD IS VERTICLE!
  - JV: THINKS $\vec{B}$-FIELD IS HORIZONTAL
    COIL WINDINGS INDICATE $\rightarrow \vec{B}$
* COST TO MOVE TO E.S. B ~ $ 100K



IF WE ARE INTERESTED . . . .

* MOCKETT et. al. NOT INTERESTED AT THIS BUT . . .

* IF WE ARE INTERESTED, SHOULD SUBMIT PROPOSAL TO SLAC (ROGER Gearhart's suggestion),

* IF WE DO DECIDE TO WRITE A PROPOSAL PAUL MOCKETT WOULD like to be part of it!

gem

γeμ

Presentation By:

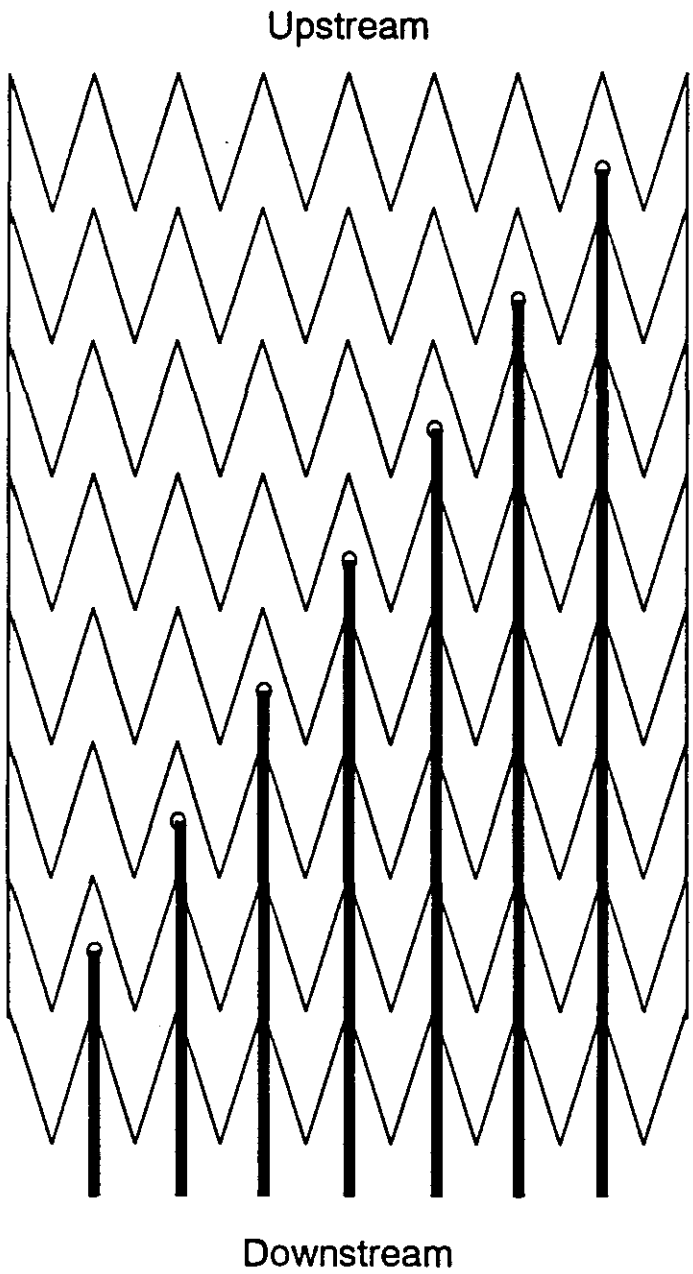
Bo Yu

Bo Yu

IPC

Pad shape, area, capacitance

readout spacing

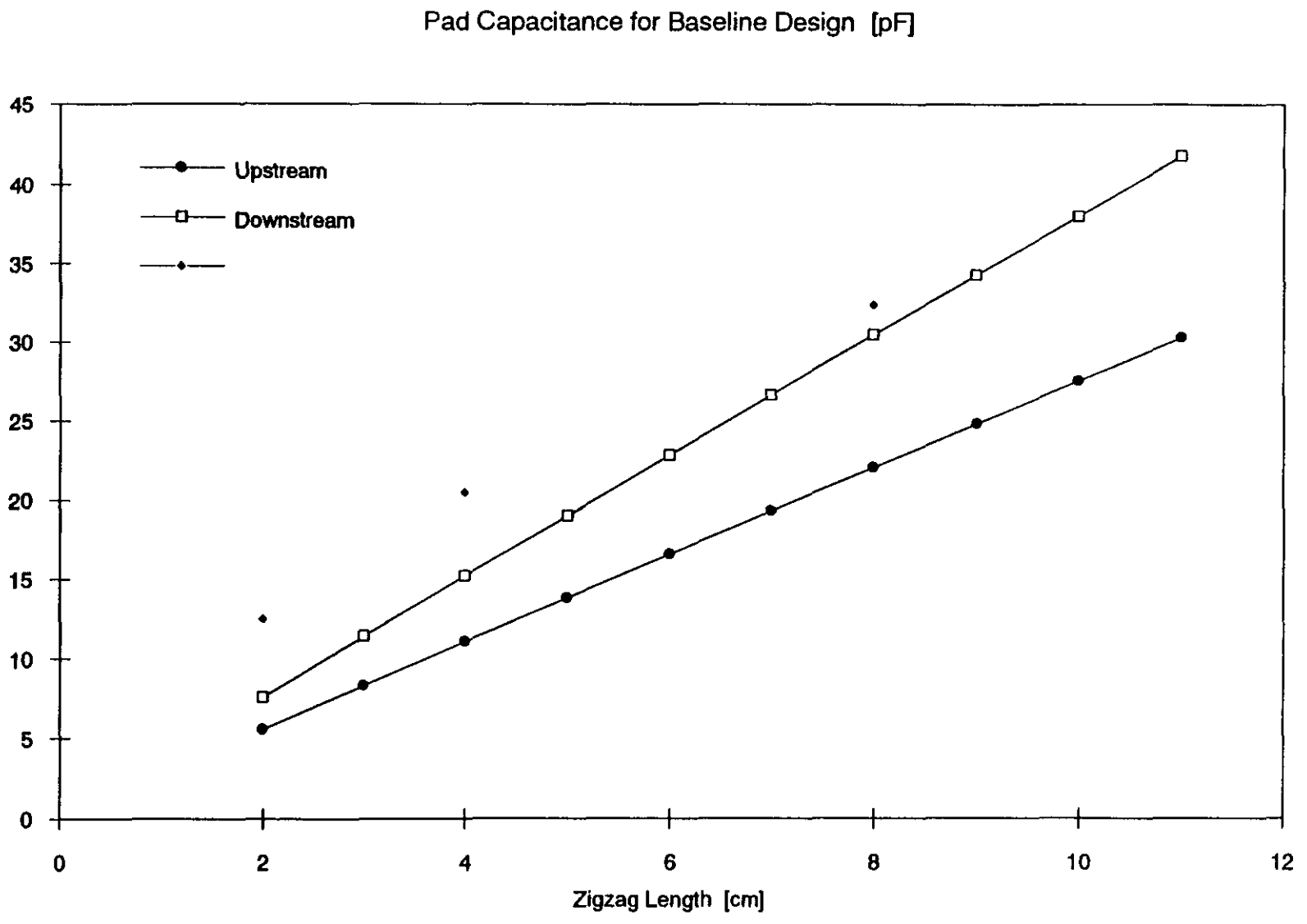

Upstream
Downstream

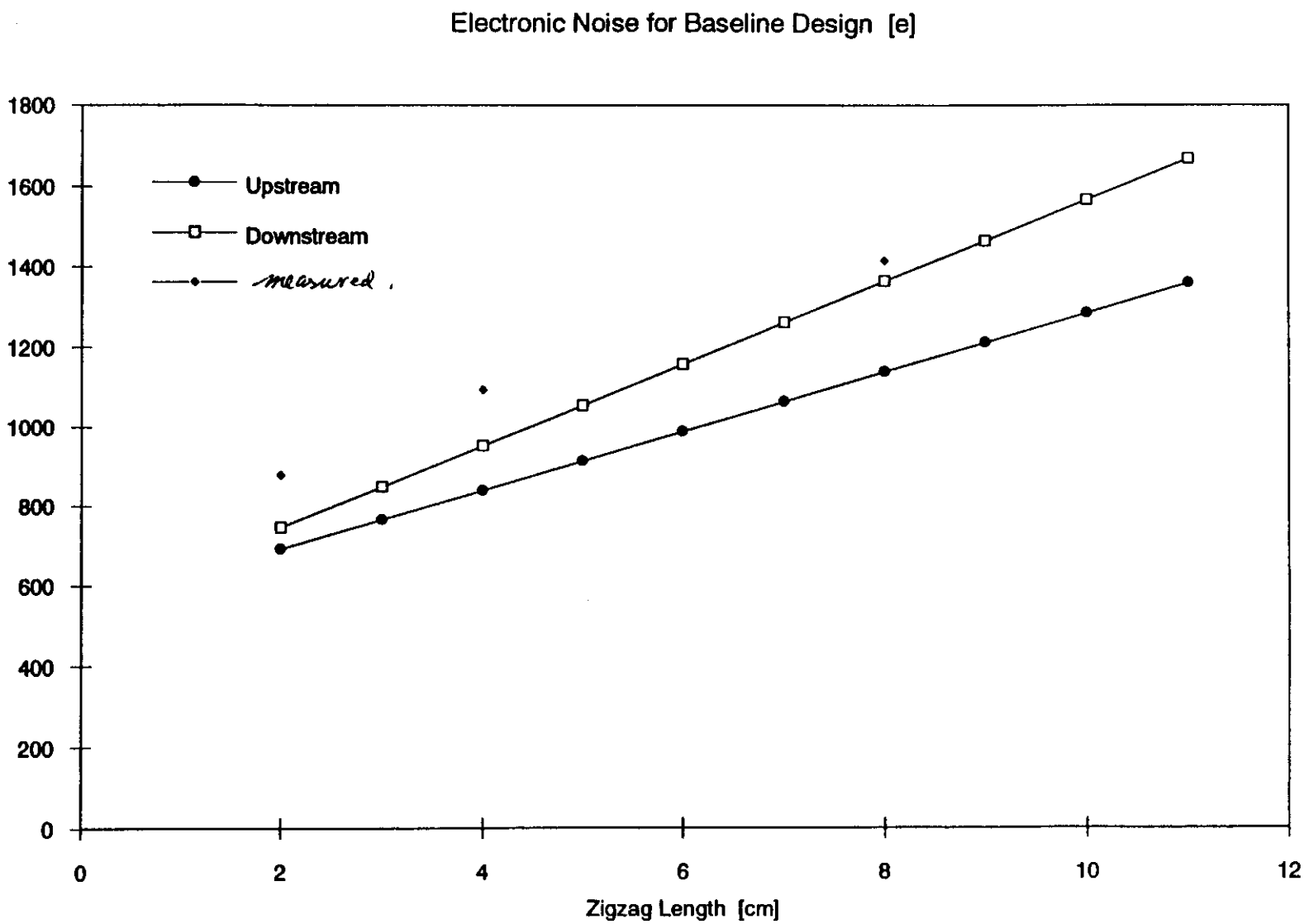
$$\sigma_Q = \frac{dENC}{dC_T} \cdot C_T$$

$$\frac{dENC}{dC_T} = 0.00433 \text{ fC / pF} = 27 \text{ e / pF}$$

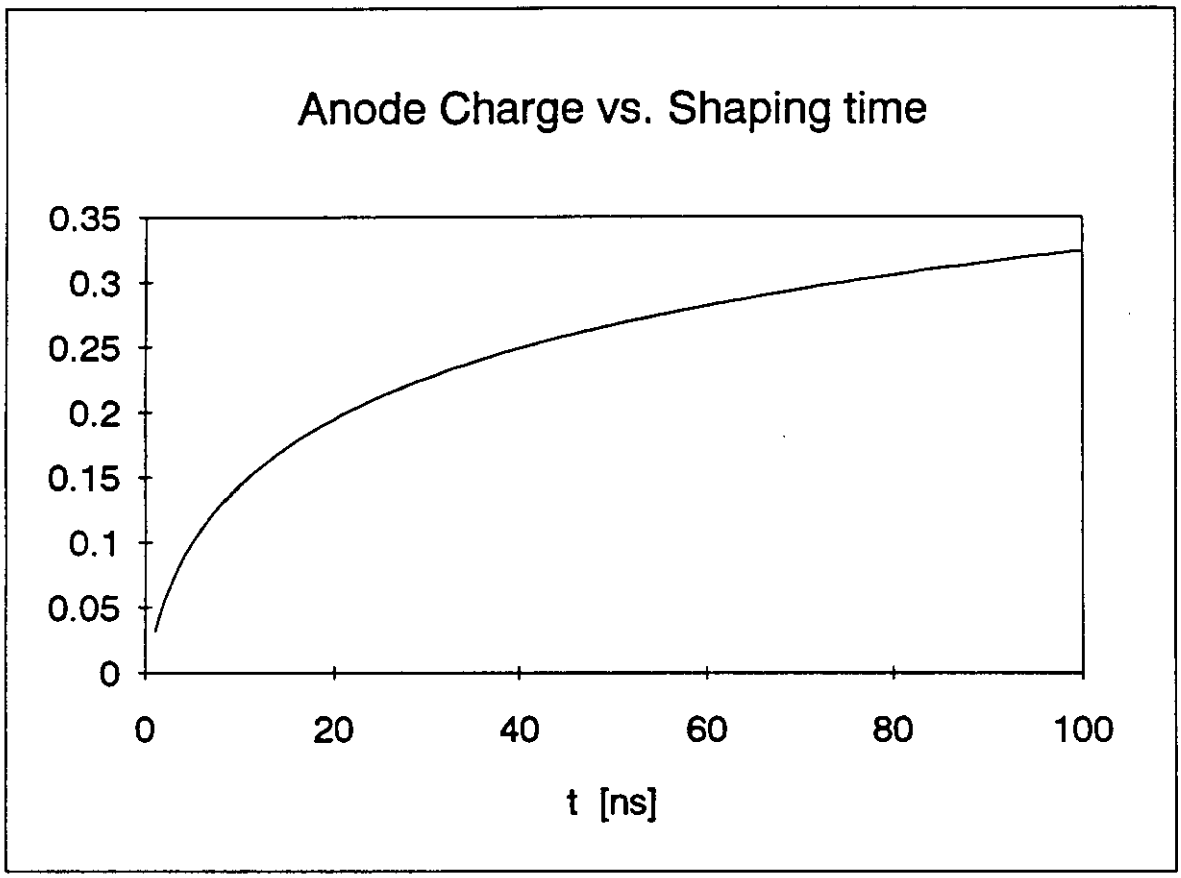
$$C_{\mathrm{T}} = C_{\mathrm{det}} + C_{\mathrm{in}} + C_{\mathrm{F}} + C_{\mathrm{parasitic}} \approx C_{\mathrm{det}} + 20 \text{ pF}$$

$$C_{\mathrm{det}} = 0.2 \cdot l_{\mathrm{edge}} + 7.6 \cdot \mathrm{Area} + 0.7 \cdot l_{\mathrm{readout}}$$

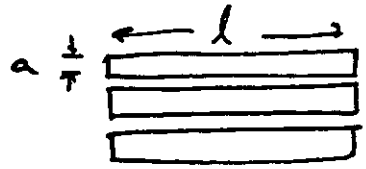

Pad Capacitance for Baseline Design [pF]
Upstream
Downstream
45
40
35
30
25
20
15
10
5
0
0
2
4
6
8
10
12
Zigzag Length [cm]


Electronic Noise for Baseline Design [e]
1800
1600
1400
1200
1000
800
600
400
200
0
Upstream
Downstream
measured
0
2
4
6
8
10
12
Zigzag Length [cm]

ra=	0.002	
rc=	0.7366	=a/2/pi*EXP(pi*h/a)
t0=	2.2222	=ra/(2 mu Ea)
mu=	1	
Ea=	450000	
a=	0.2	
h=	0.2	



Optimized design with rectangular pads.



$.85 < \text{Area} < 5.5\ cm^2$

now a = variable $< .5\,cm$

$\text{Area} = a \cdot l =$ ~~constant~~ fixed to keep $\Delta\eta \cdot \Delta\phi$ constant

$\Rightarrow l = A/a$

<u>Capacitance</u>

Upstream pads.

Pad edge capacitance is now a weak function of a

a	C pF/cm edge
.2	.66
.3	.69
.4	.71
.5	.72

Readout line capacitance is same as before (16 pF)

$$\Rightarrow \boxed{C_{pad} = \left(.66 - .72\,\frac{pF}{cm}\right) \cdot \frac{A}{a} + 16}$$ increases as a decreases

Downstream pads

Use same area coefficient as before: $7.5\,pF/cm^2$

$$\Rightarrow \boxed{C'_{pad} = 7.6\,pF/cm^2 \cdot A}$$ independent of a

(fig. 2)

Pad Capacitance vs. Readout Spacing :

rectangular pads, fixed area, vary width

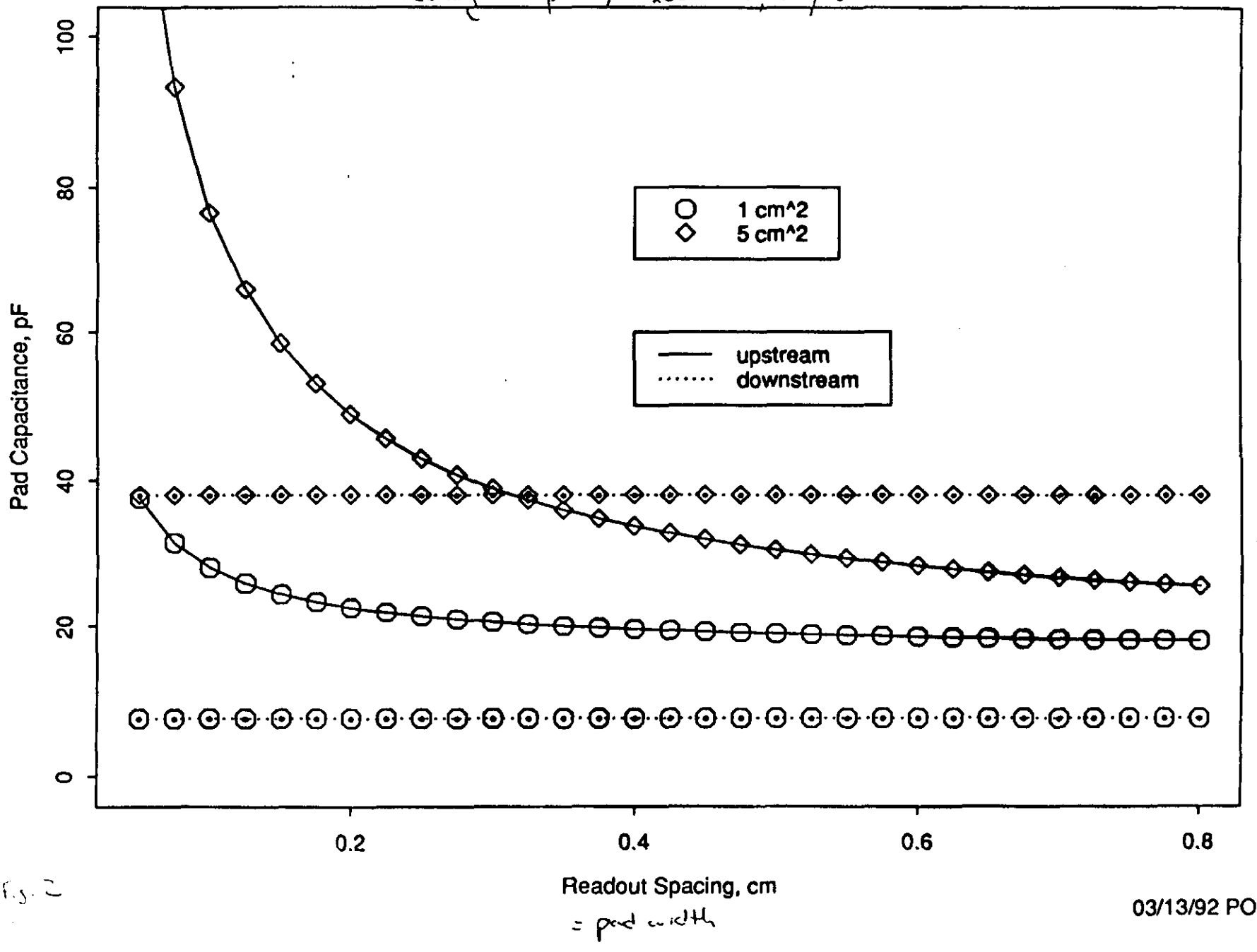


Fig. 2

03/13/92 POC

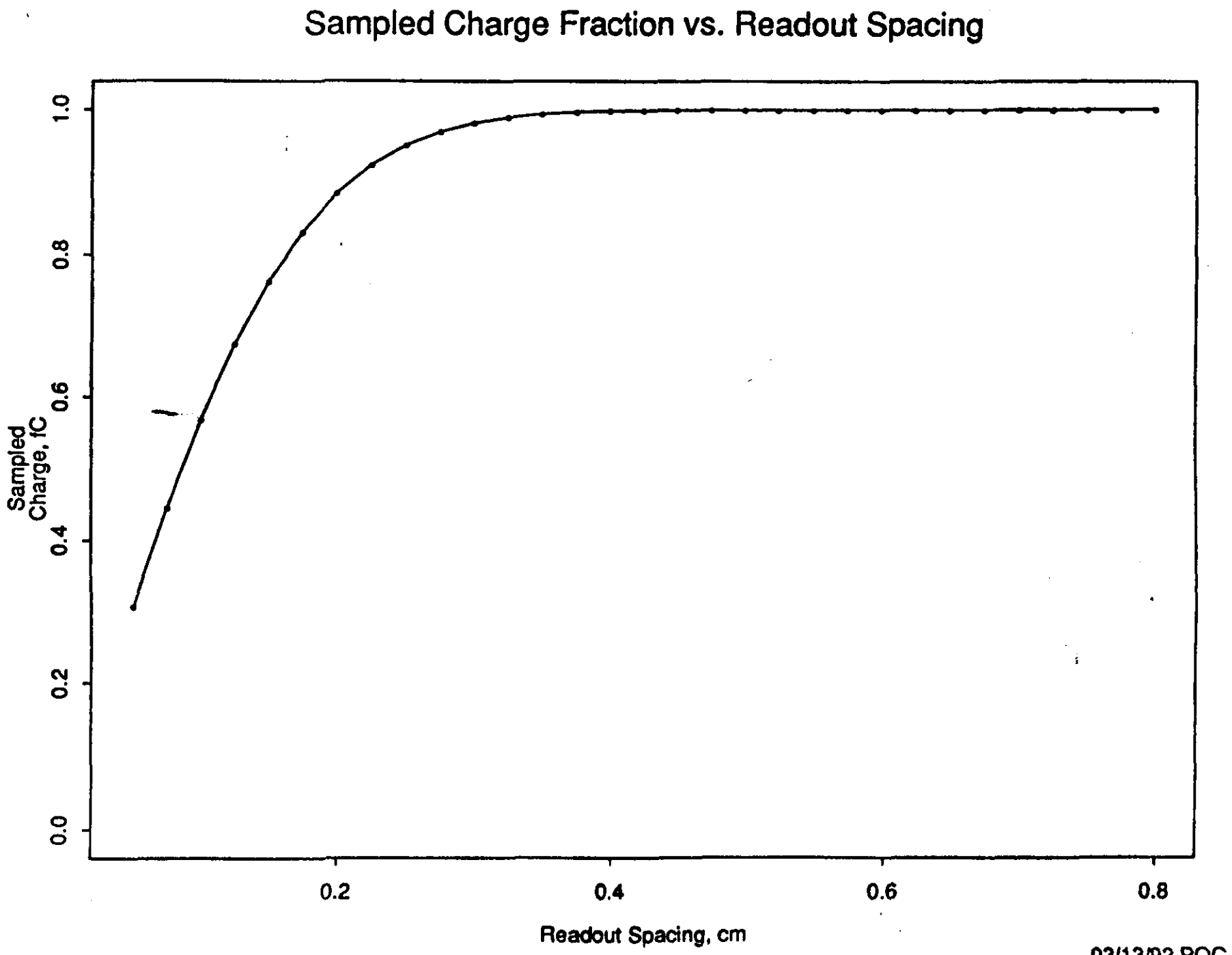
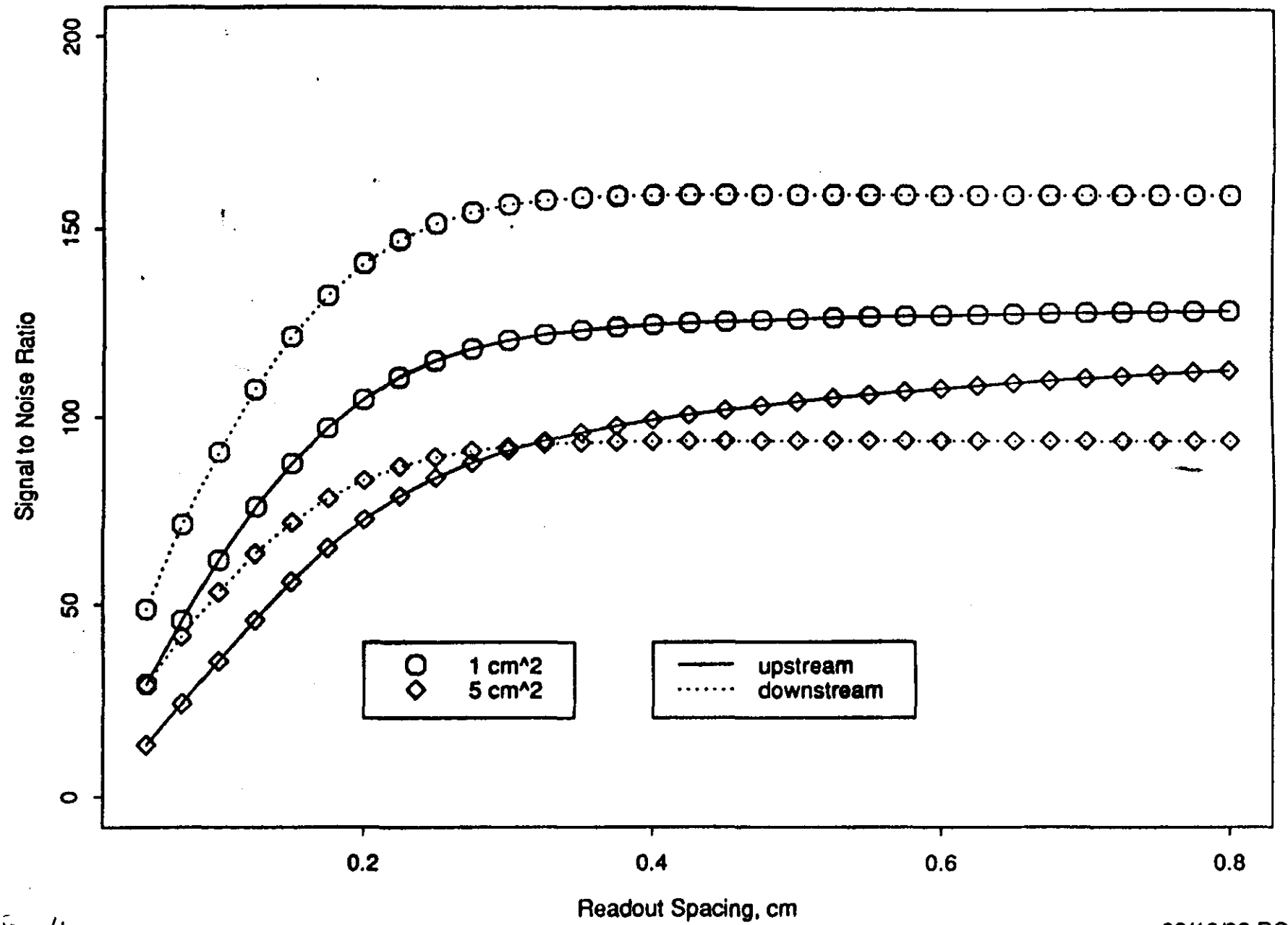

Sampled Charge Fraction vs. Readout Spacing
Sampled Charge, fC
0.0
0.2
0.4
0.6
0.8
1.0
0.2
0.4
0.6
0.8
Readout Spacing, cm
03/13/92 POC

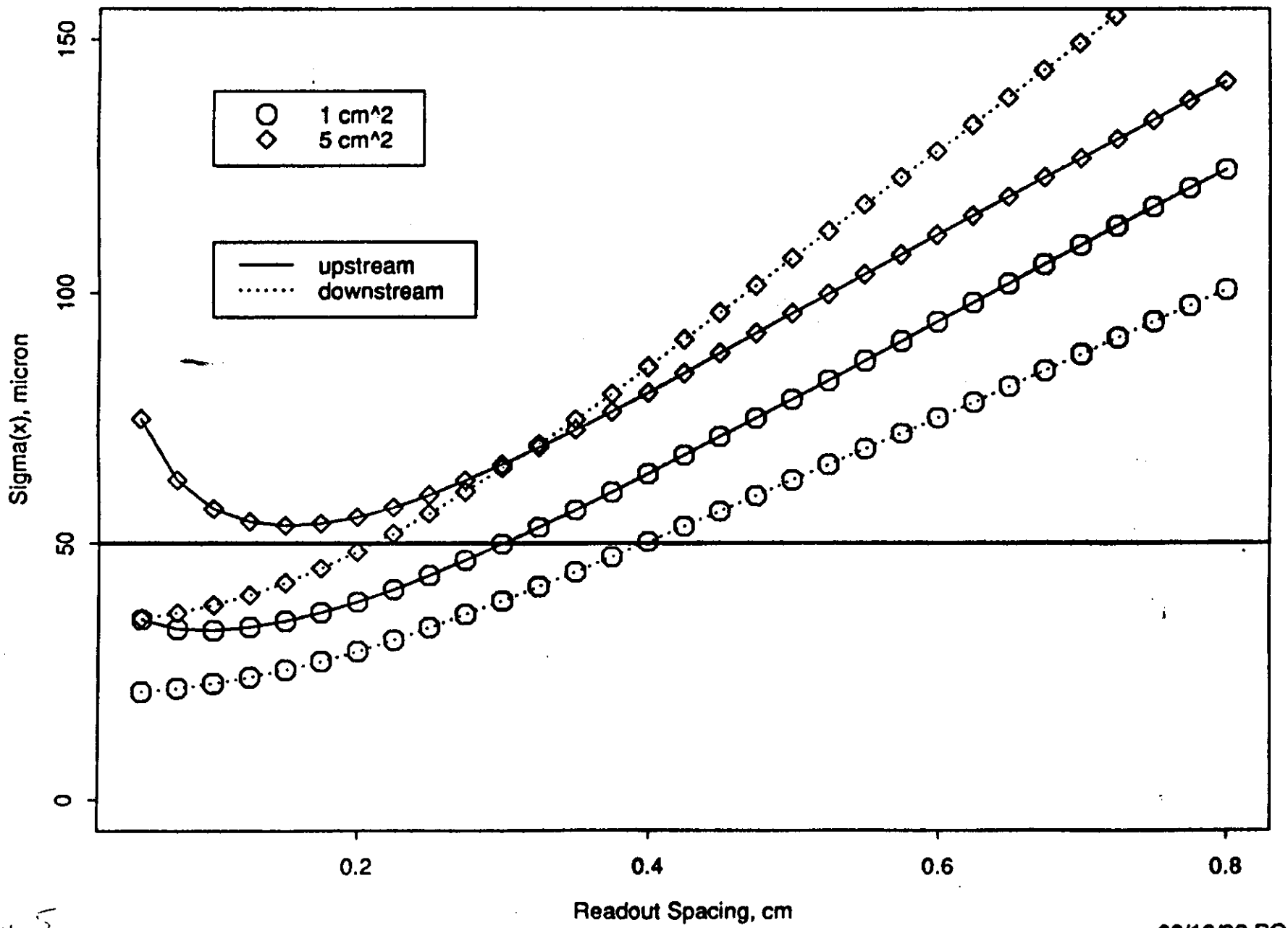
fig. 3

Signal-to-Noise vs. Readout Spacing



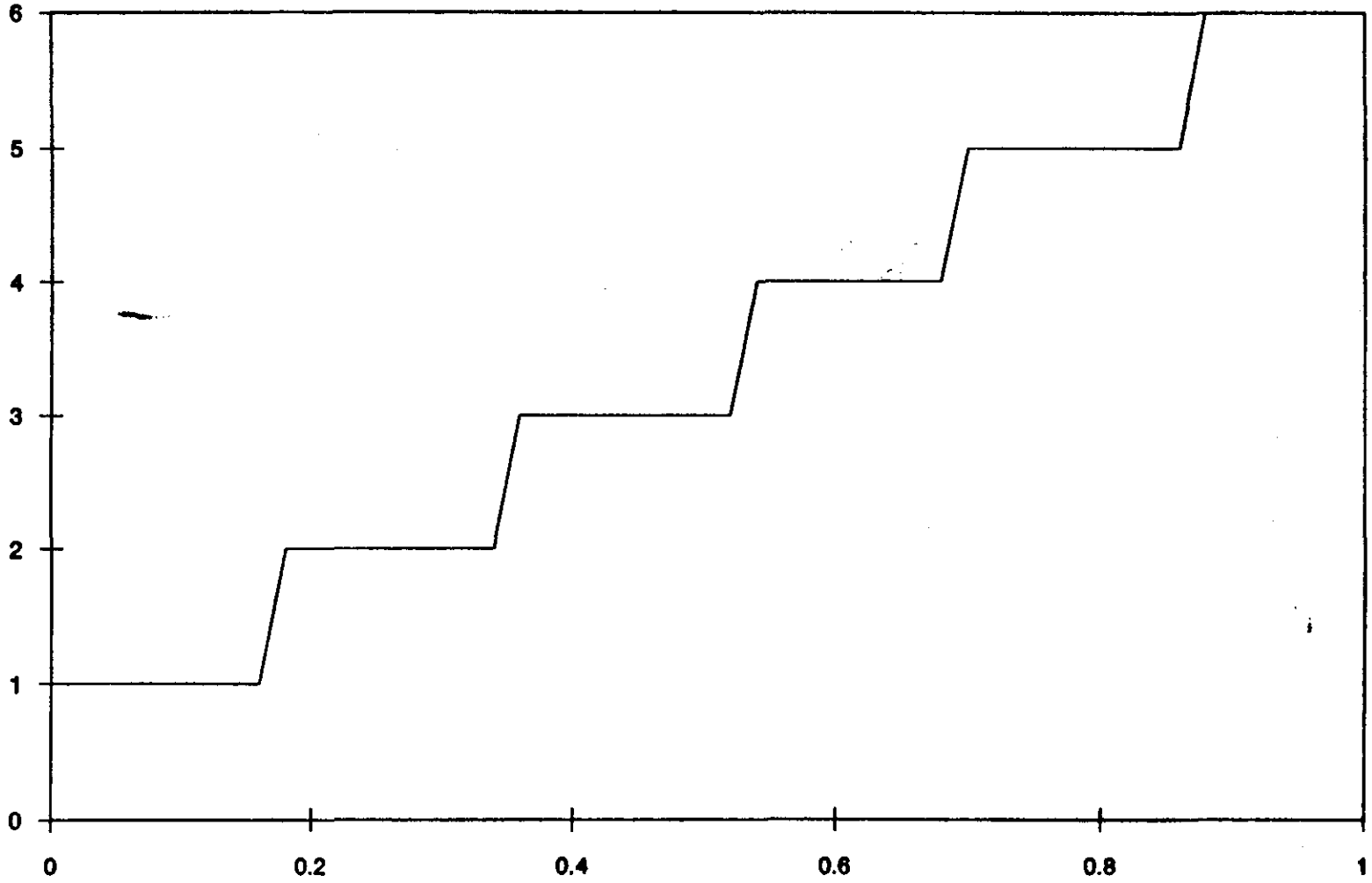
03/13/92 POC

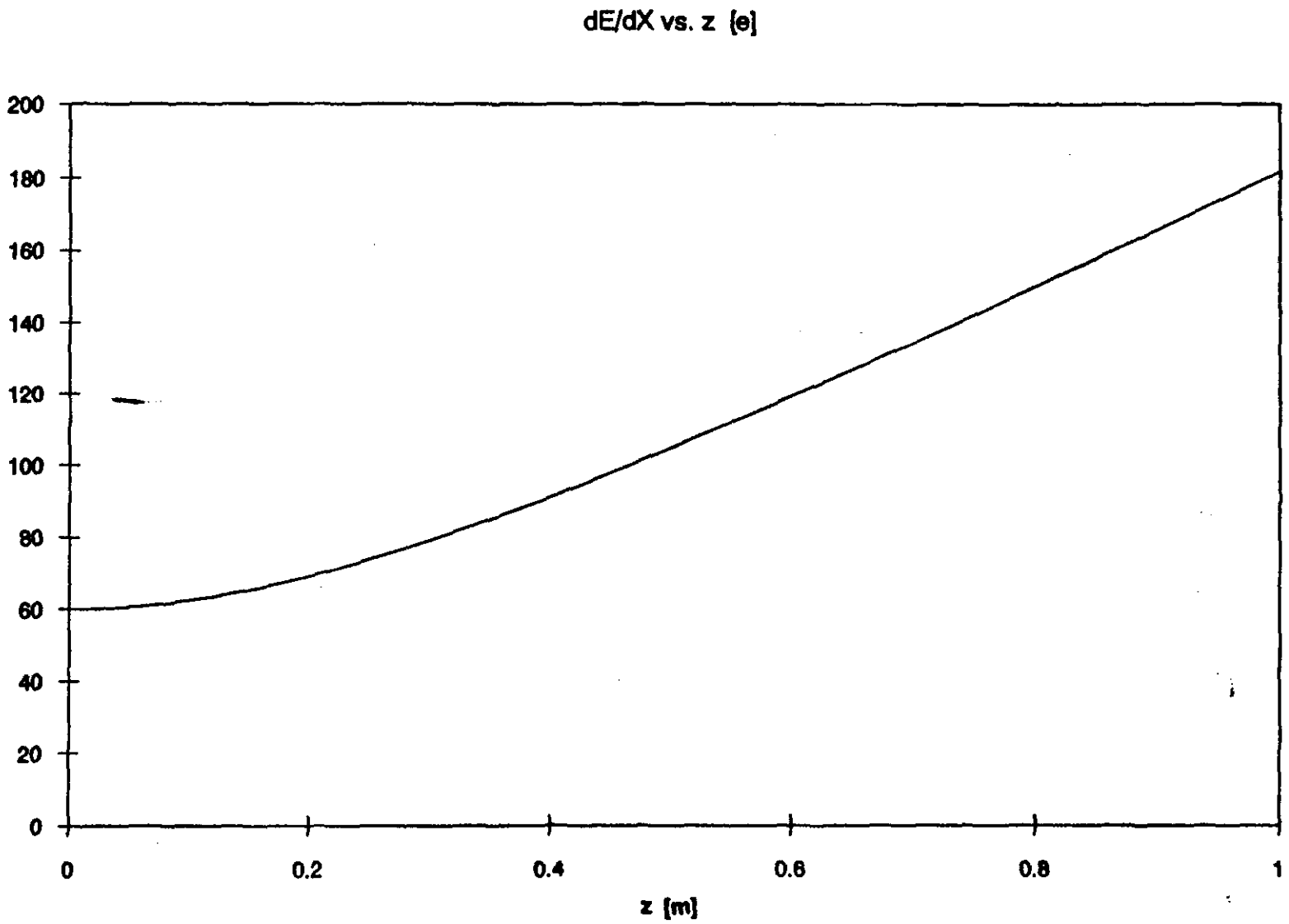
Resolution vs. Readout Spacing

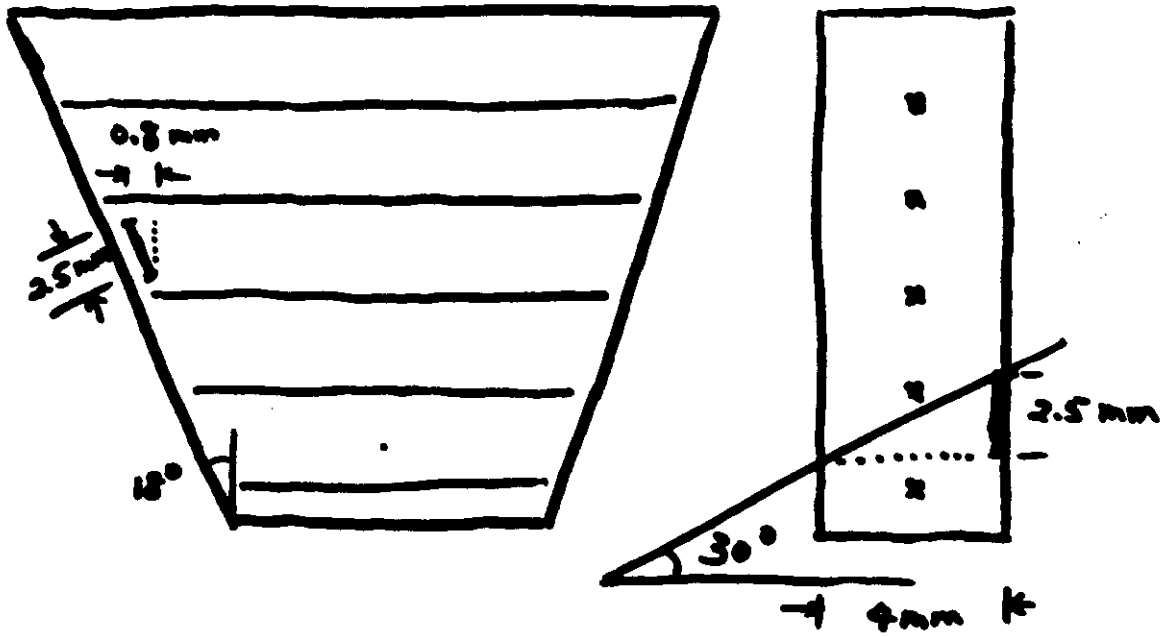


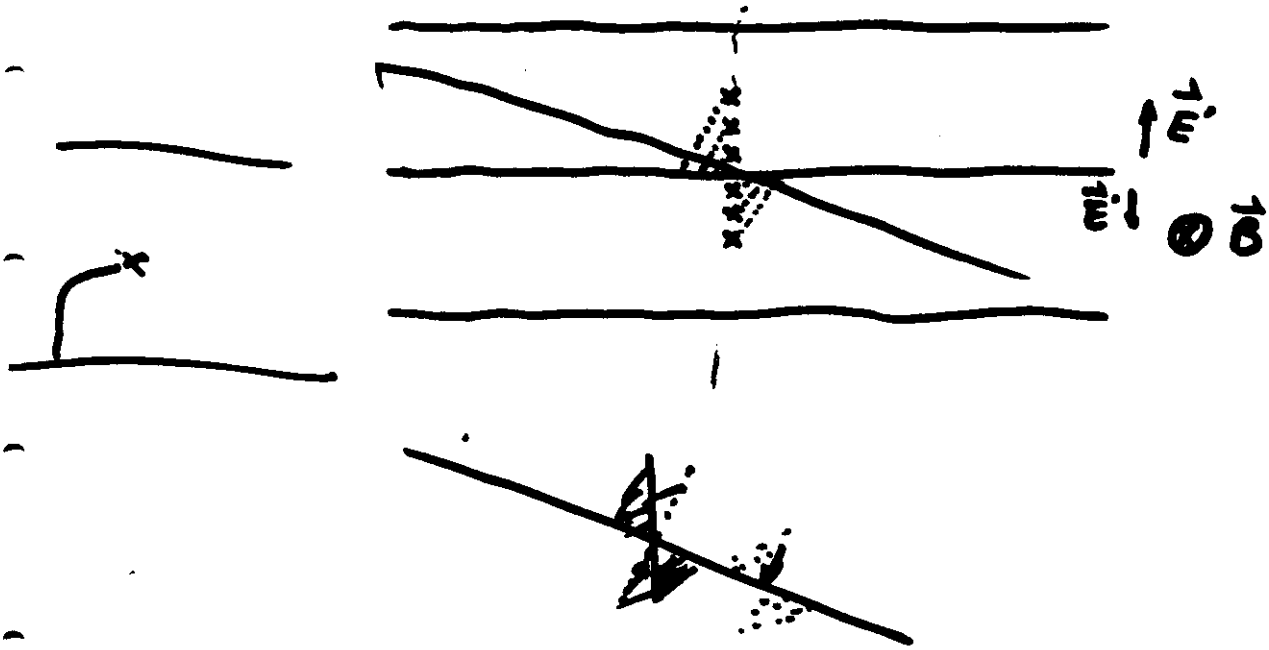
03/13/92 POC

Number of Cells Hit vs. Z




dE/dX vs. z [e]
200
180
160
140
120
100
80
60
40
20
0
0
0.2
0.4
0.6
0.8
1
z [m]


0.8 mm
2.5 mm
18°
2.5 mm
30°
4mm


$\vec{E}'$
$\vec{E}'$
$\otimes \vec{B}$

gem

γeμ

Presentation By:

Jim Musser

Jim Musser

Rectangular Pad Resolution

$C \doteq 0.65\ pf/cm \cdot \ell + 12pf$

$$\Rightarrow \sigma_x = \frac{2 \cdot a}{30fC \cdot f(a)} \left[0.07fC + 0.00433 \left(2.065 \frac{A}{a} + 12 \right) \right]$$

A = area = $0.97\ cm^2 - 5.5cm^2$
a = pad width

f(a) = fraction of charge collected by 3 pads

$\doteq 0.9$ @ $a = 2mm$

@ $a = 2mm$

& $\sigma_x^{min} \cong 20\ \mu m$

$\sigma_x^{max} \cong 41\ \mu m$

Chevron Pad Resolution

Chevron Lengths – 1.7cm → 11cm

for 0.5cm wide, perimeter = 10.2 · length

min cap: (0.3 pf/cm)(1.7 cm)(10.2) + 12 = $\boxed{17\,pf}$

max cap: (0.3 pf/cm)(11 cm)(10.2) + 12 = $\boxed{46\,pf}$

not included: effect of other conductor lines.

$$\left(\frac{2\sigma_q}{q}\right)_{min}(0.5\,mm) = 48\,\mu m$$

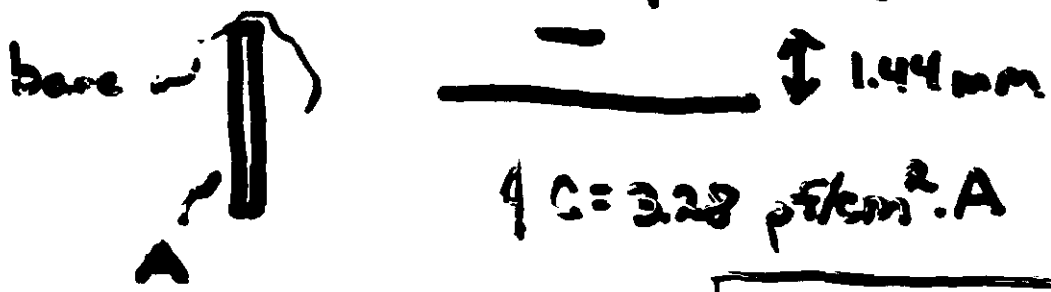
$$\left(\frac{2\sigma_q}{q}\right)_{max}(0.5\,mm) = 90\,\mu m$$

$q = 30\,fC$

N.G. chevron cap too large!

Cap. Meas. (cont)

2.5 mm wide strip over ground plane



$C = 3.28\ pf/cm^2 \cdot A$

@ 3.5 mm thick $\boxed{C = 9.4\ pf/cm^2 \cdot A}$

assume 0.5 mm wide trace, 25 cm long

$\boxed{C \cong 12\ pf}$

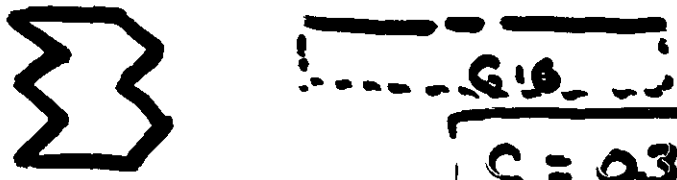
2.5 mm wide strip - surrounded by cathode ~~pat~~ plane, ground plane beneath

$C \cong .65\ pf/cm$ (10 cm long panel)

Capacitance Measurements

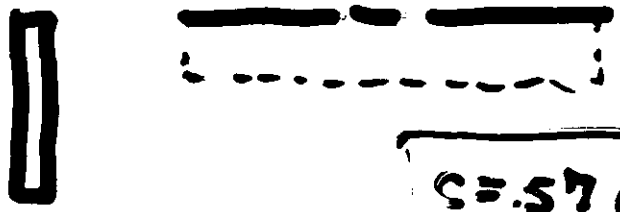
Use scribed mylar "pads" on G10 substrate in various configurations.

Chevron pad - 5mm wide on G10 substrate



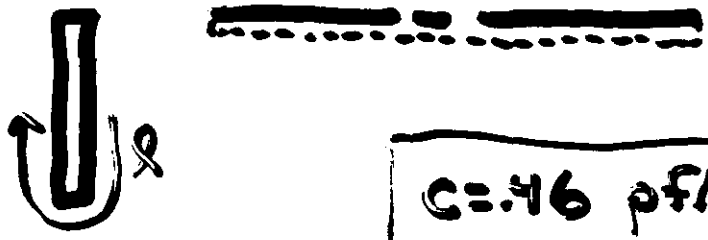
$C = 0.3\ pf/cm\text{-}chevron \cdot \ell$

Straight pad - 2.5mm wide on 1.4mm G10



$C = .57\ pf/cm \cdot \ell$

Straight pad - 2.5mm wide 0.5mm G10

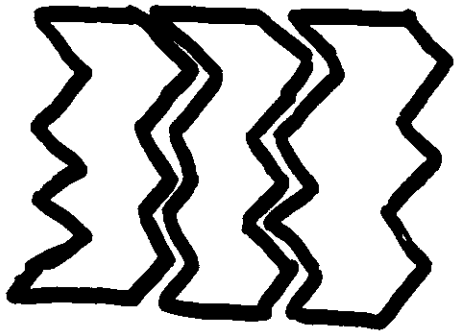


$C = .46\ pf/cm \cdot \ell$

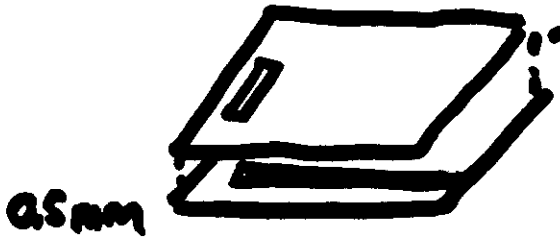
Detector Capacitance

3 contributions

1) Pad-Pad capacitance



2) readout line → other pads



3) pad - other readout lines

~ conducting plane

Pad Geometry Optimization

Position Resolution

$$\frac{\sigma_x}{x} \cong \frac{2\sigma_q}{q}$$

appropriate for centroid calc. Can do better using fit to $q(x)$

$$\boxed{\sigma_q = ENC_0 + \frac{dENC}{dC_T} C_T}$$

$ENC_0 = 0.07\ fC$ (430 e's)

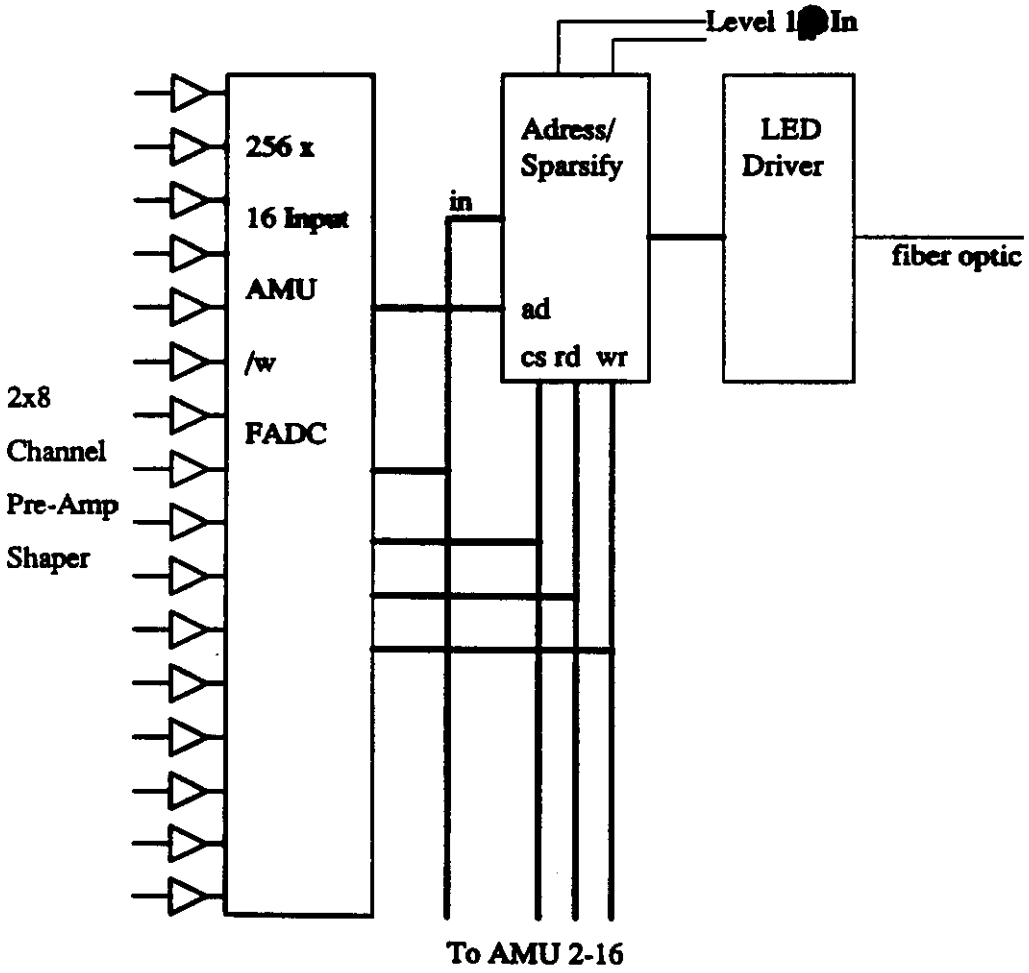
$\frac{dENC}{dC} = 0.00433\ fC/pf$ (27 e's/pf)

assumes $g_m = 44\ mS$
$\beta = 1.5$
$t_p = 30\ ns$

$C_T = C_{det} + 5pf$

IPC Electronics Baseline Design

On-Chamber Digitization Option



γεμ

Radiation Damage in CMOS

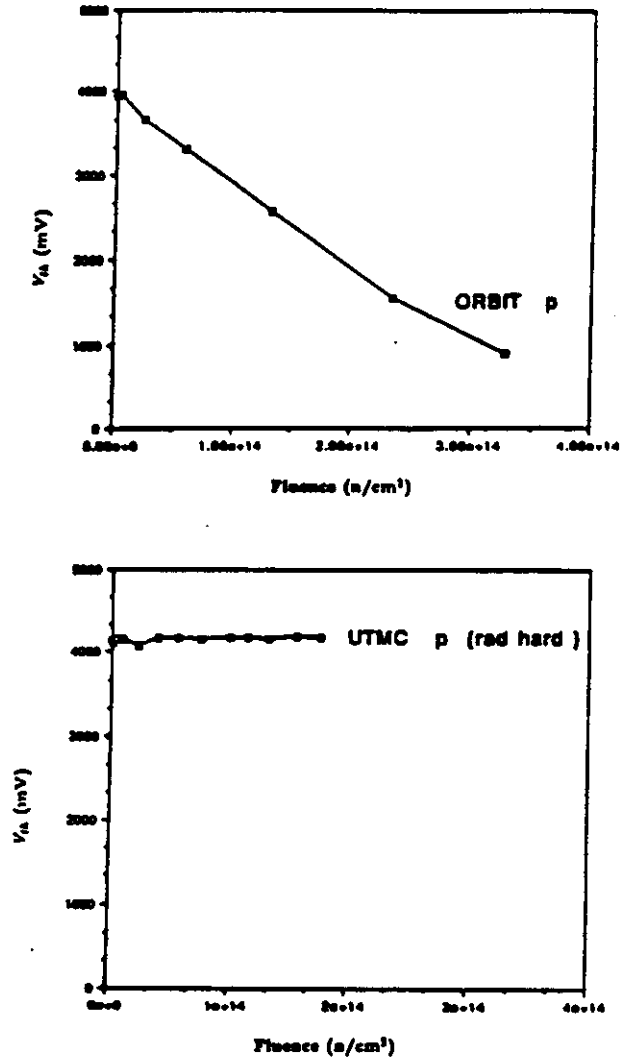


Fig. 1. a) Threshold voltage V_{th} *vs.* neutron fluence for the non-rad-hard *p* transistor #2 manufactured by ORBIT. b) Threshold voltage V_{th} *vs.* neutron fluence for the rad hard *p* transistor #7 manufactured by UTMC.

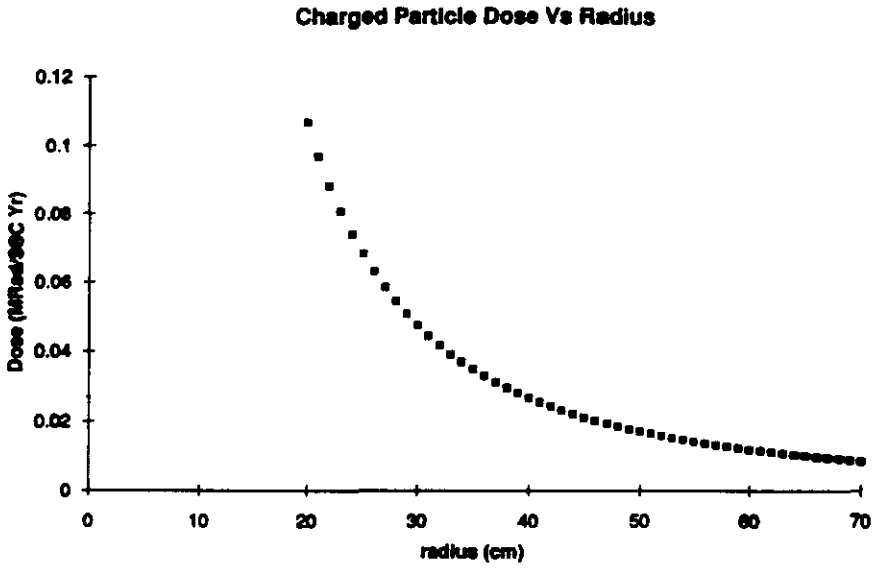
Neutrons: bulk damage doesn't effect CMOS

typical rating > 10^{14} cm^{-2}

IPC Electronics

Radiation Tolerance

C.T. Prog. Rpt. ⇒



closest electronics @ 40cm

Dose = 0.025 Mrad/SSC-yr

1 Mrad rate ⇒ 40 SSC yrs

Neutrons: ~ 2×10^{12} /cm²-SSC-yr E>100K

10^{14} N/cm² ⇒ 50 SSC yrs.

Ionizing Radiation in CMOS

trapped holes accumulate in oxide layer + interface. ⇒

Carrier transport mechanism

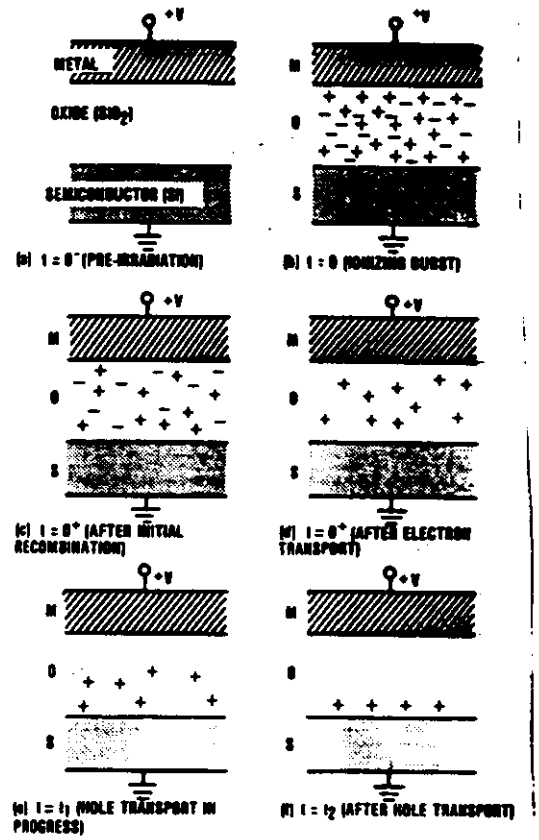


FIGURE 5. Illustration of recombination, transport, and trapping of carriers in SiO_2 films.

Causes thresh. voltage to drop with total exposure.

⟹

Total dose effects on P and N channel transistors

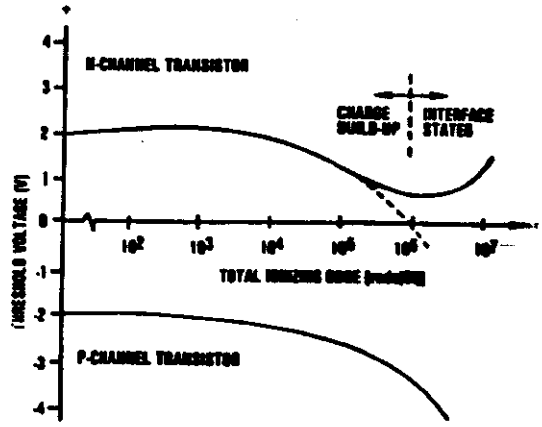


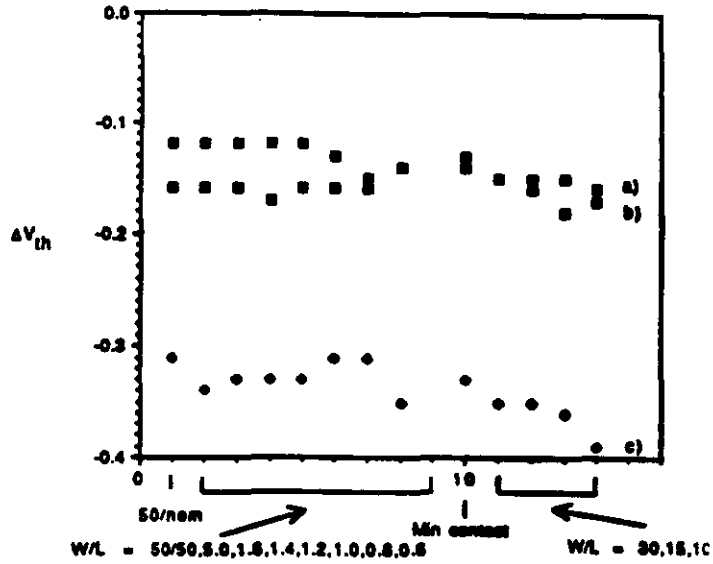
Illustration of the effect of positive charge building and interface state production on the threshold voltage in irradiated n- and p-channel MOS transistors.

FIGURE 7.

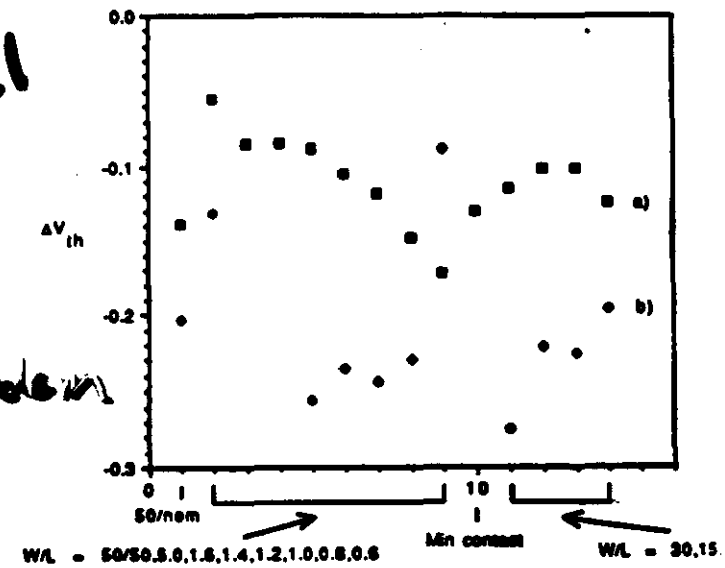
Other Effects: mobility decrease (>10^6 rad)
leakage current

Radiation Damage in CMOS

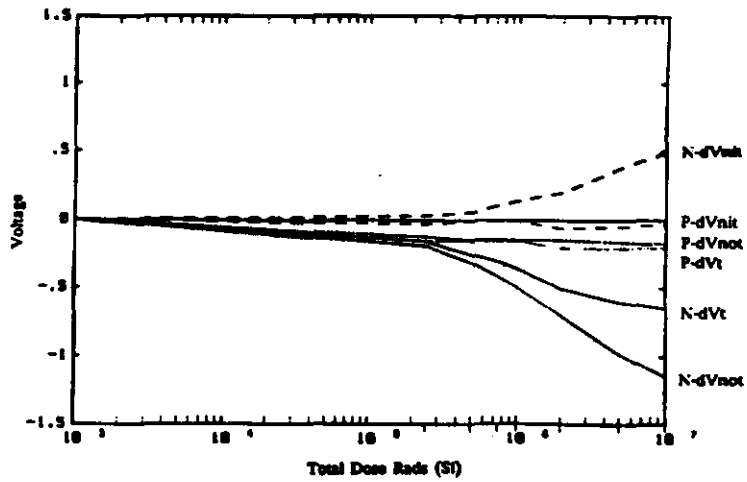
V_{th} shift ~0.2V



Sadrozinski et al
3 Mrad



P. O'Connor claims $\Delta V_{th} = 0.2$ V not a problem for amp.



UTMC
Int. Data

Readout Chip:

Contains:

State machine for driving readout sequence.

Static RAM buffer (256x8) for holding threshold values

Readout Buffer

Readout Encoding Logic

Cheapest Soln: fully custom VLSI chip.

Existing Soln: Implement on rad-hard gate arrays

(multiple vendors) - LSI Logic

UTMC

⋮

Switched-Cap Array

Now under development @ ORNL

Chuck Britton - Engineer in Charge

Looking into several Rad-Hard processes

UTMC UTD-R (1.5 μm)
UTE-R (1.2 μm)

However, no caps! To be useful, need cooperation of UTMC to develop analog capability.

Harris - AVLSIRA ← looks very good

TS054 digital Process

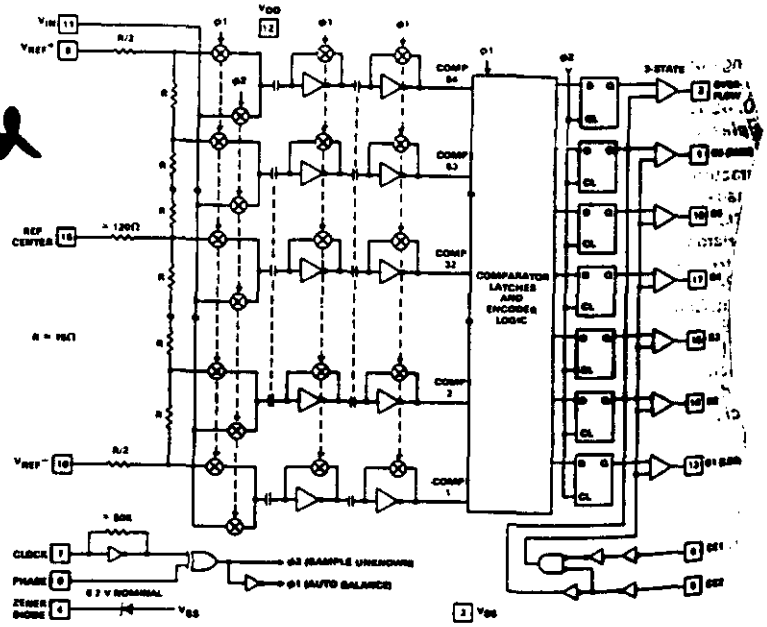
RH01 - implanted O_2 (SOI)

To proceed, need non-disclosure @ ORNL

UTMC - in hand
Harris - working on it (have at IU)

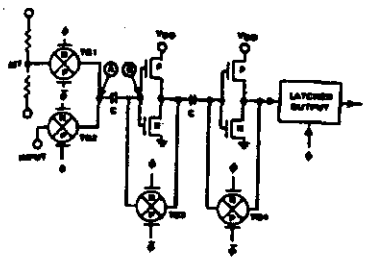
FADC - rad-hard design exists in SOS

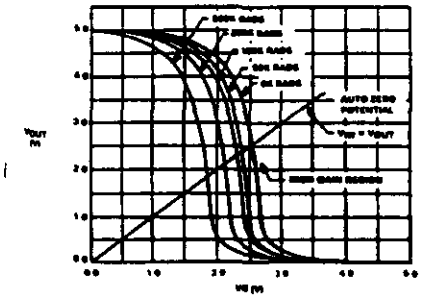
6-8 bit FADC - hard to 1 Mrad.



FADC's particularly sensitive to radiation damage due to ΔV_{th}

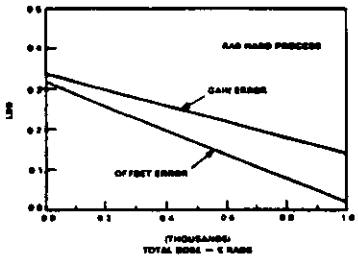
Soln: "Autozero"



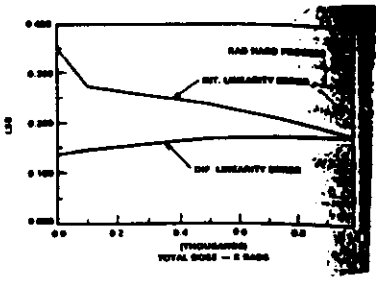


FADC (cont)

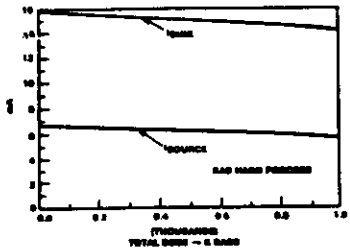
Diff. linearity →
<0.5 LSB



Int linearity →
<0.5 LSB



$\Delta I_s < 10\%$



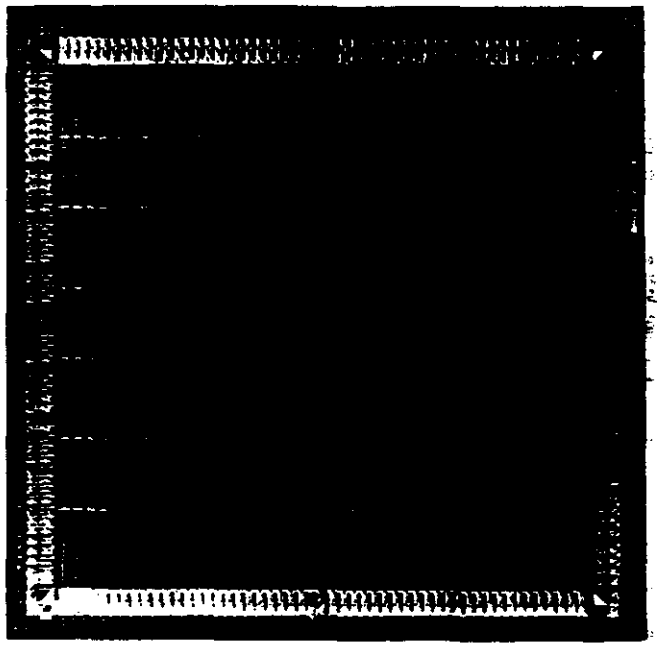
UTD-R Gate Array Family

UTMC ★★★ RAD SPEC

Features

- ☐ Total dose 1E6 rads(Si) to data sheet specification according to MIL-STD-883, Method 1019
- ☐ Total dose 1E7 rads(Si) functional
- ☐ Dose-rate upset > 1E9 rads(Si)/sec
- ☐ Dose-rate latchup > 2E11 rads(Si)/sec*
- ☐ Projected neutron fluence > 10E14 n/cm^2
- ☐ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B
- ☐ Screening also available to MIL-M-38510/606-608 (JAN)
- ☐ 1.5μ CMOS, epitaxial, double-level-metal technology
- ☐ Gate delay: 750 picoseconds typical (2-input NAND w/2 loads)
- ☐ Patented continuous-column architecture
- ☐ Complexity
  - 3,400 to 11,000 usable gates
  - 116 to 212 pads
- ☐ I/O TTL and CMOS compatible
- ☐ All I/O individually programmable as driver, receiver, bidirect, three-state, open-drain
- ☐ Low power dissipation
- ☐ Extensive cell and macro libraries
- ☐ Design support through UTMC's Mentor Graphics® and Valid Workstation Toolkits on Apollo® and Sun® platforms and UTMC's in-house design system

* May be design dependent



UT212DR

Product Description

The UTD-R gate array family is designed to meet the needs of designers of high-reliability military and aerospace systems where high radiation tolerance is a must. Built using UTMC's proprietary radiation-hardened process, these devices meet the needs of tactical and strategic radiation-hardened systems.

UTMC has developed special low-temperature processing techniques to enhance total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability of our standard gate array products. For transient radiation hardness and latchup immunity, UTMC builds all its radiation-hardened products on epitaxial wafers using an advanced silicon gate CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, ensuring greater transient-upset resistance.

LSI LOGIC

RHASIC LRH20000 Radiation Hardened Series

Preliminary

Description

RHASIC is the LSI Logic family of radiation hardened application- specific integrated circuits. The LRH20000 RHASIC Series is a Channel Free™ gate array technology offering superior speed performance and high gate counts. The device is processed using 1.0 micron, 2-layer metal, epitaxial bulk silicon HCMOS technology. Densities from 14,000 to 170,000 equivalent gates are offered. Usable gate capacities from 5000 to 70,000 gates, and up to 348 signal I/Os can be implemented.

The speed and range of gate counts available in the LRH20000 Series make it ideally suited for achieving system-to-silicon integration. Sophisticated algorithms incorporated in LSI Logic's proprietary Concurrent Modular Design Environment™ (CMDE ®) development software allow a circuit designer's modular hierarchy to be utilized to its maximum potential. By performing an optimized functional placement of these building blocks, and then collapsing and compacting them to minimum size, substantial benefits are realized in both speed and silicon area utilization.

Output buffer drive strengths of 0.8, 1.6, 3.2, 4.8, 6.4 and 9.6 mA are available and determined by the user during the design phase. Also available is output slew rate control that allows dV/dt of each output to be tailored to individual load conditions.

Overview

- Guaranteed total dose specification 3E6 rad (Si)
- Upset resistant for dose rates up to 1E9 rad(Si)/sec
- Latch-up resistant to dose rate $\geq 1E^{12}$ rad(Si)/sec
- SEU 2E-10 errors/bit-day measured at room temperature on a latch type memory structure without cross-coupled resistors. Actual value will be design and layout dependent.
- No SEU latchup for 320MeV Au ions, LET=200MeV/mg/cm^2
- Silicon-gate 1.0 micron (0.7 micron effective), 2-layer metal HCMOS technology
- Up to 348 signal I/O capability
- Speed performance of 0.40nS through 2-input NAND gate, standard load =2
- Extensive macrocell, macrofunction and megafunction library elements (directly compatible with industry standard LCA10000 series)
- Seven array sizes from 5,000 to 50,000 usable gates (to 70,000 gates in early 1992)
- High reliability gate oxide isolation
- Fully supported by CMDE software for verification, simulation and layout
- Spice based library for pre- and post- radiation simulations
- Channel-Free architecture for maximum layout flexibility
- Configurable output drive up to 9.6 mA with slew rate control capability
- Inputs and outputs protected from over-voltage and electrical latchup
- TTL/CMOS I/O compatibility
- Efficient implementation of large logic blocks
- Advanced packaging available
- Can be processed to Level S Reliability requirements
- On board process monitor circuit included in all designs
- Radiation Hardness test data available through Mil/Aero Marketing under ITAR restrictions

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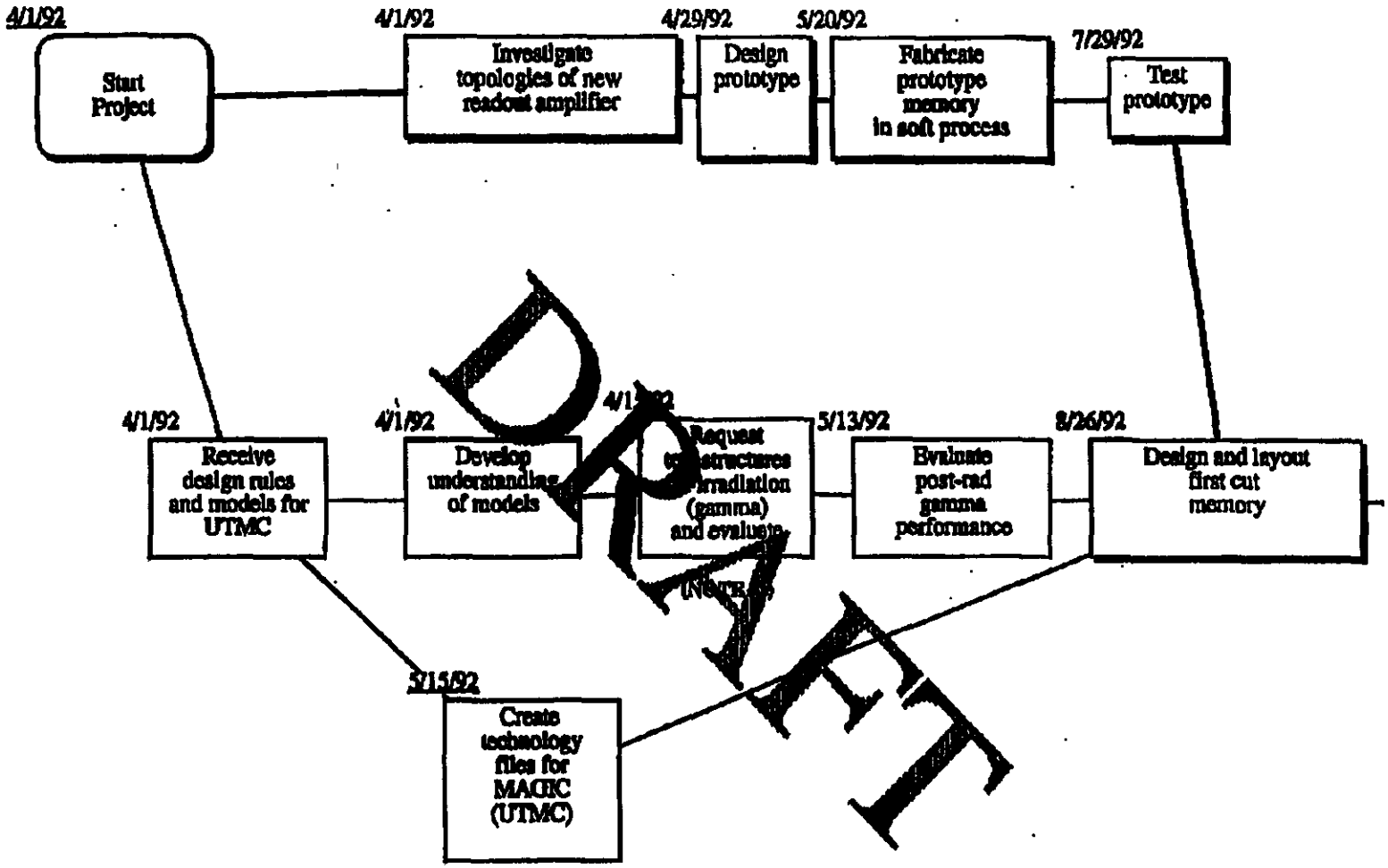
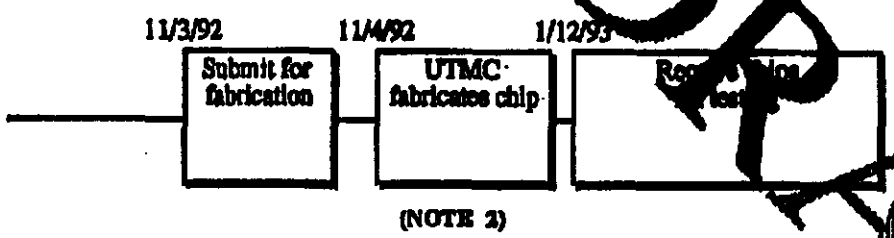


DRAFT

UTMC FABRICATION ALTERNATIVE

C. L. Britton, Jr.
A. L. Wintenberg
ORNL 3/31/92

NOTES:
1. Assumes test structures are readily available.
2. Assumes 10 week fabrication time.



DRAFT

UTMC FABRICATION ALTERNATIVE

C. L. Britton, Jr.
A. L. Wintenberg
ORNL 3/31/92

Pre-Amp / Shaper

Engineer in charge - Paul O'Connor (BNL)

Has design in hand for rad-soft 8ch pre-amp / shaper.

Rad-Hard:

many advantages to using same process as SCA. (share cost of fab runs, share work of gen. tech files...)

disadvantage - optimal noise figure for amp would probably be obtained in bipolar.

Now working on non-disclosure with Harris, UTMC.

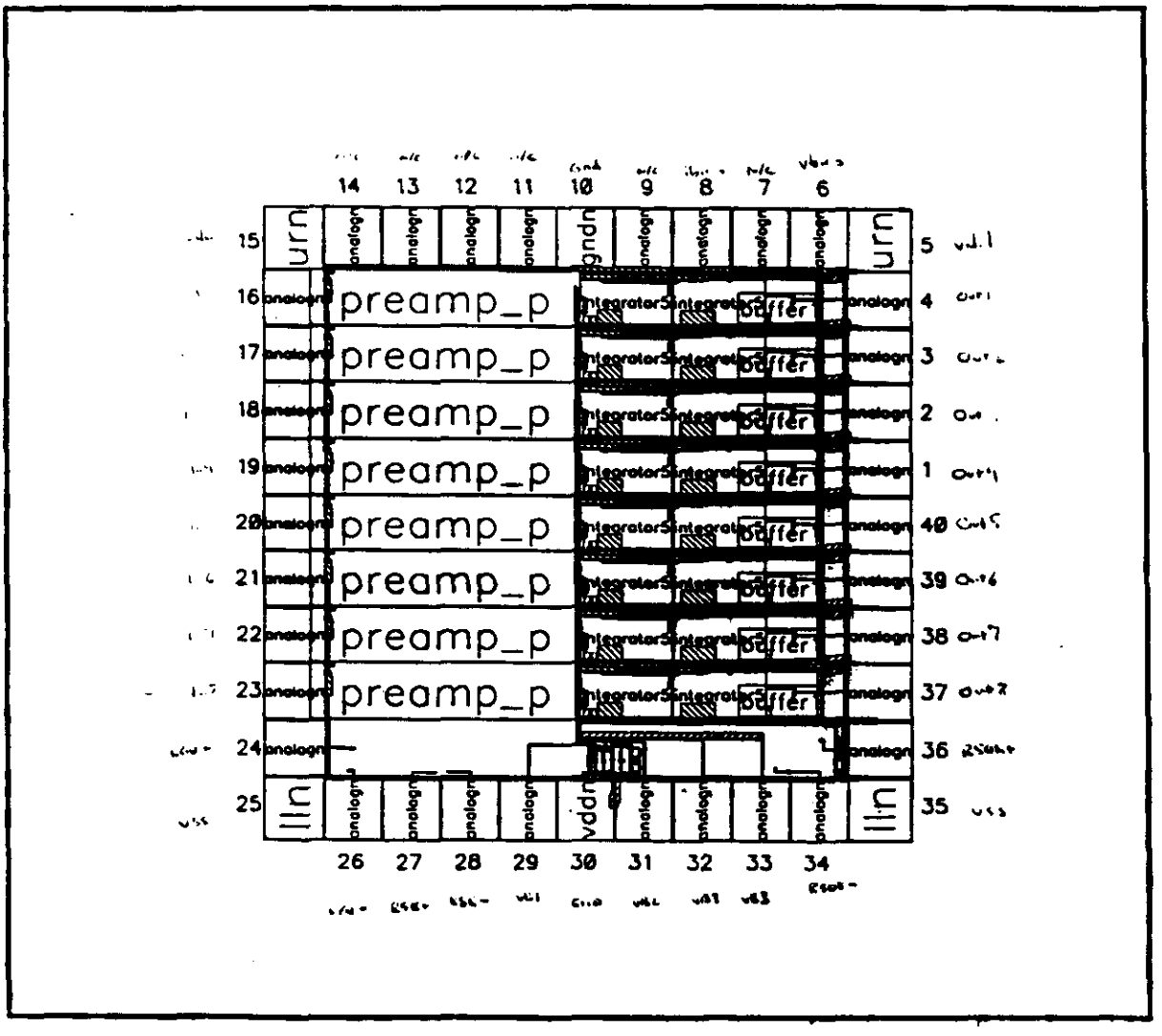
Will continue development of radsoft design through one more MOSIS run to tune design.

In parallel, will gear up in rad-hard process & modify design in time to share first rad-hard fab run w-th ORNL.

IPC Front End Electronics

Prototype Design

- Layout - preamp + shaper (8 channel Tiny Chip)



Confidential Agreement
Page 4

8. This Agreement shall be governed by and construed in accordance with the laws of the State of Florida.

9. This Agreement is subject to United States Export laws and regulations. Further, Recipient agrees to obtain all applicable government export licenses and to comply with all applicable laws and regulations, including but not limited to, the U.S. Export Administration Regulations and the International Traffic in Arms Regulations.

10. This Agreement supersedes all previous and contemporaneous communications, transactions and understandings, whether oral or written, and constitutes the sole and entire agreement pertaining to the subject matter hereof. No modification or addition to these terms shall be binding unless made in writing and signed by an authorized representative of both parties hereto.

Each party acknowledges its acceptance of this Agreement by the signature below of its authorized officer on duplicate counterparts of the Agreement, one of which fully executed counterparts is to be retained by each party.

COMPANY	HARRIS CORPORATION Semiconductor Sector Military and Aerospace Division
By: [signature]	By: [signature]
Printed Name: Melvin J. DeBecker	Printed Name: JOHN P. YANAS
Title: Director Technology Transfer	Title: (EAI) Contract Adm.
Date: March 27, 1992	Date: 3/27/92

gem

γeμ

Presentation By:

Chuck Bower

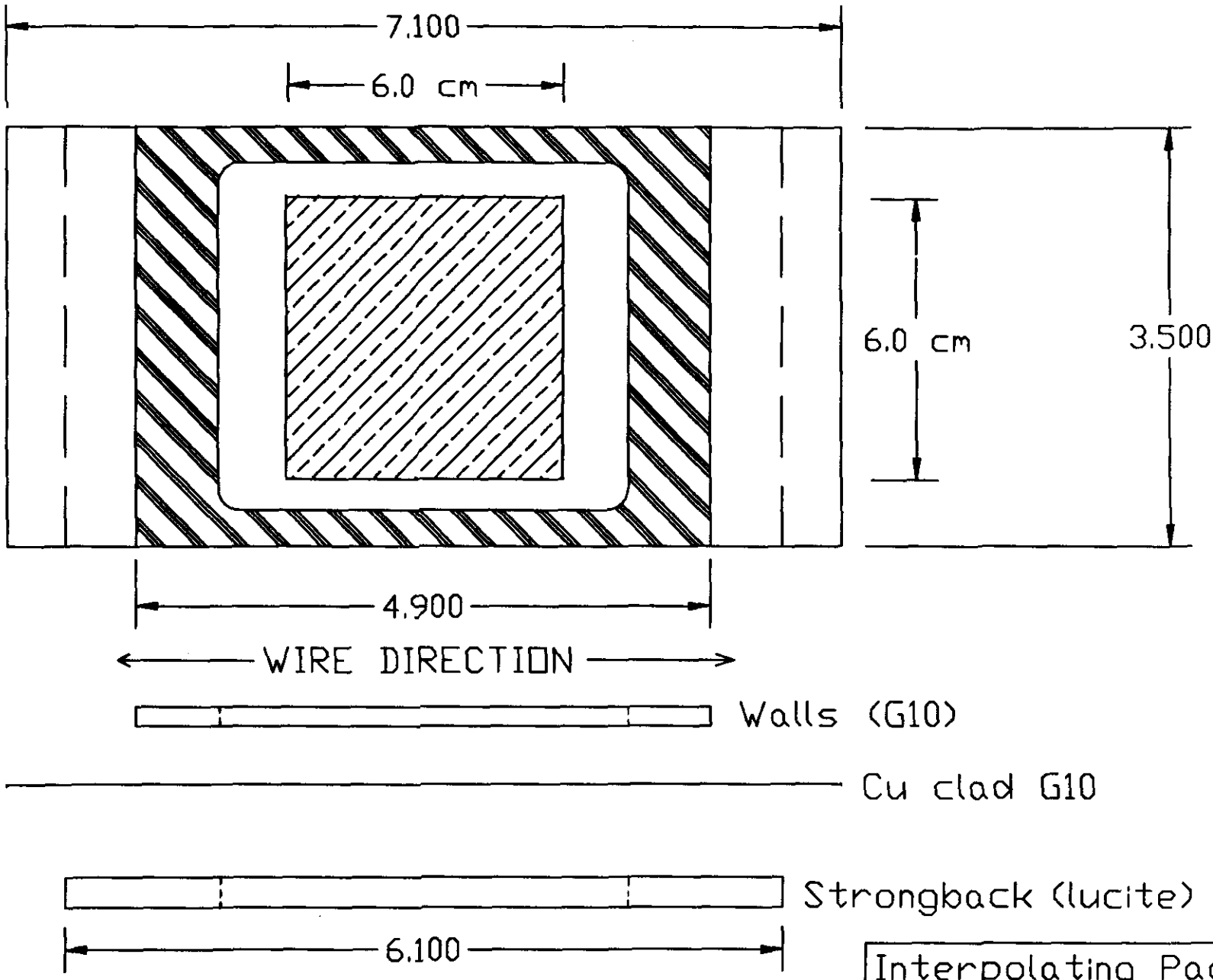
GEM Central Tracker

IPC Prototype

Chamber Design & Test Plan

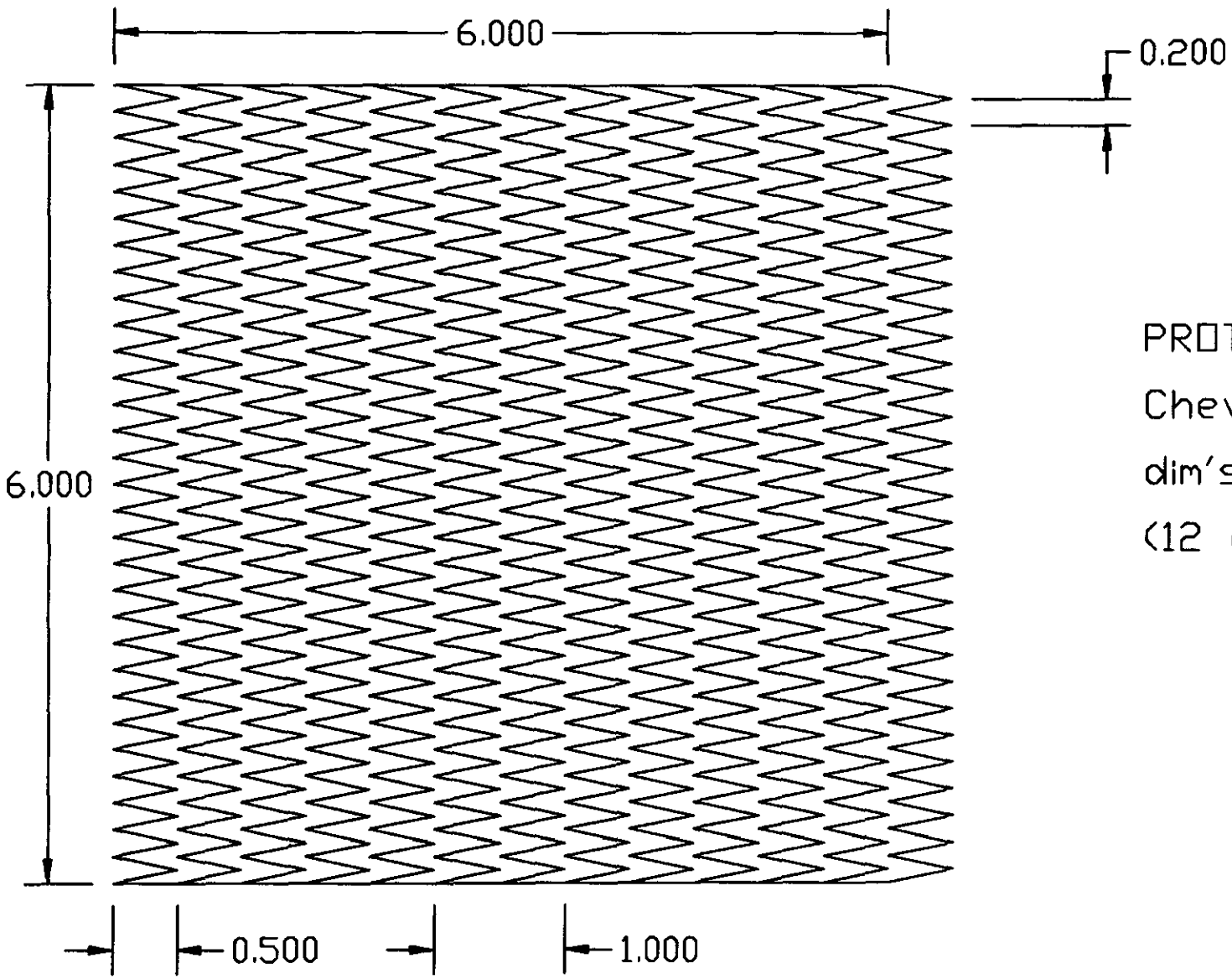
2 Apr 1992

Chuck Bower
Indiana Univ.



Interpolating Pad Chamber
GEM Prototype
Assembly Drawing
C. Bower 2/92

dim's in inches except as noted



PROTOTYPE

Chevron Cathode

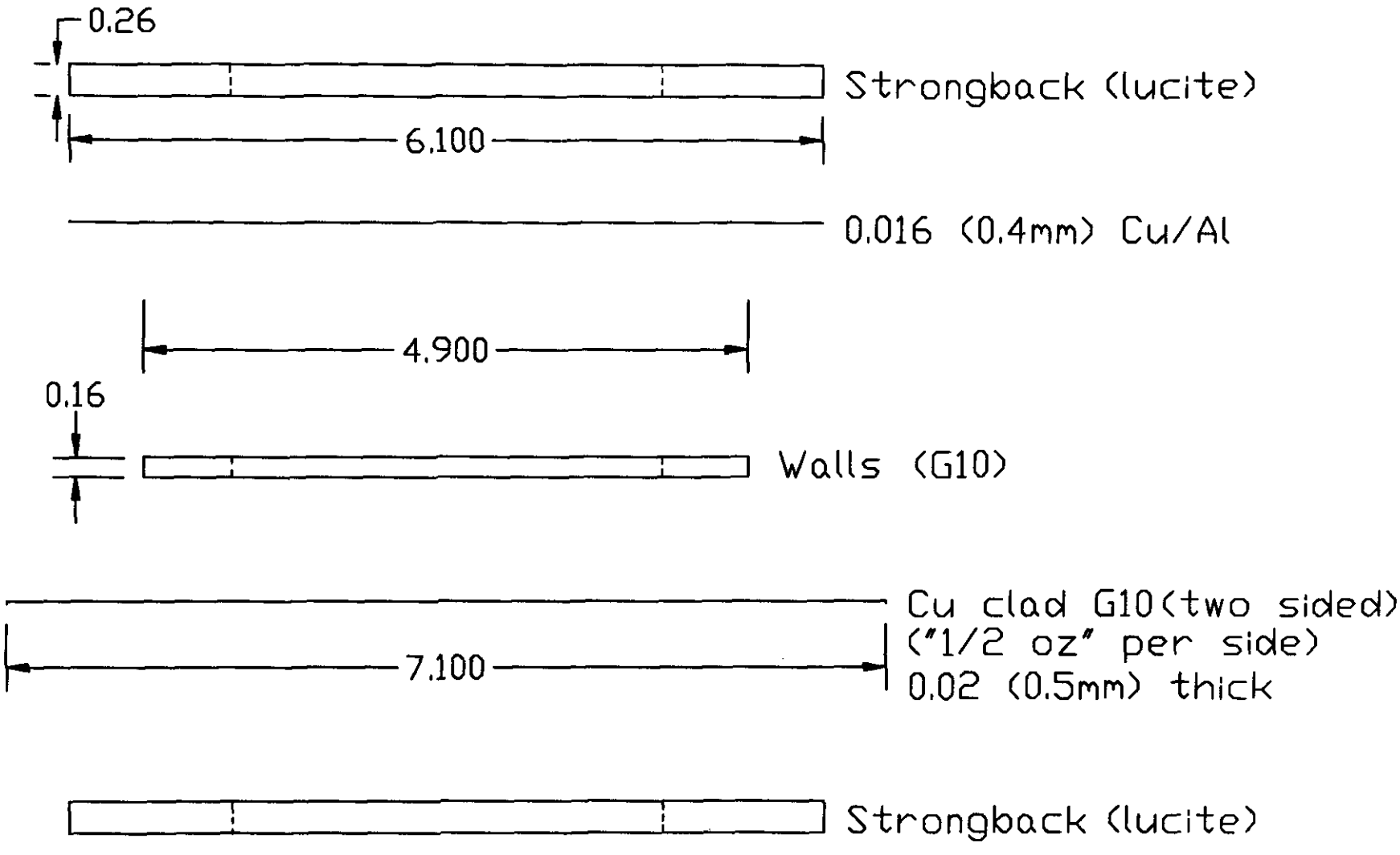
dim's in cm

(12 electrodes)

GEM CENTRAL TRACKER
INTERPOLATING PAD CHAMBER PROTOTYPE

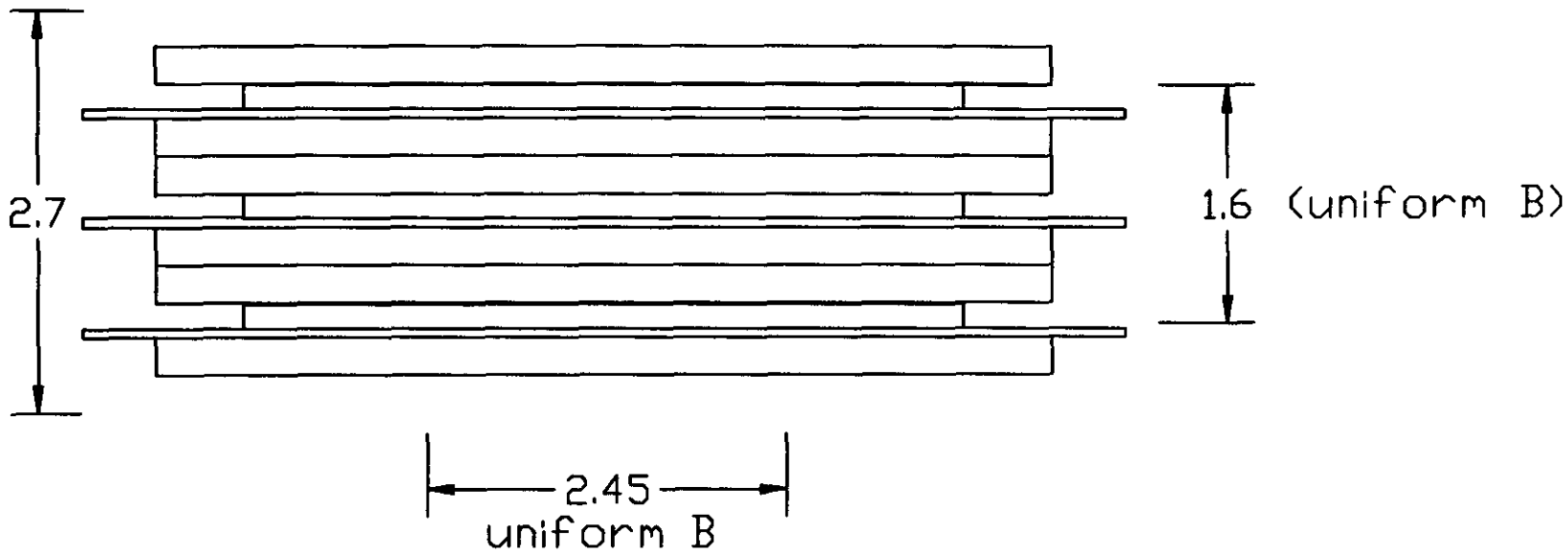
Specifications

Sensitive Area	60 mm X 60 mm
Chamber thickness	4 mm
Chamber volume	26 ml
Anode wire pitch	2 mm
Anode-Cathode distance	2 mm
Field wire-Anode distance	(NO field wires)
Anode wire	0.020 (0.040) mm Au/W
Top (non-readout) cathode	Cu plated Al
Bottom (readout) cathode	"1/2 oz" Cu/G10
Chamber walls	G10
Number of cathode channels	12 (24)
Chevron period	2 mm
Anode wire offset (WRT chevron peak)	0.5 mm
Single chevron area	5 mm X 60 (30) mm
Inter-chevron spacing	0.075 mm
Chamber gas	CF_4-CO_2 @ 1 atm (% mixture TBD)



dim's in inches except as noted

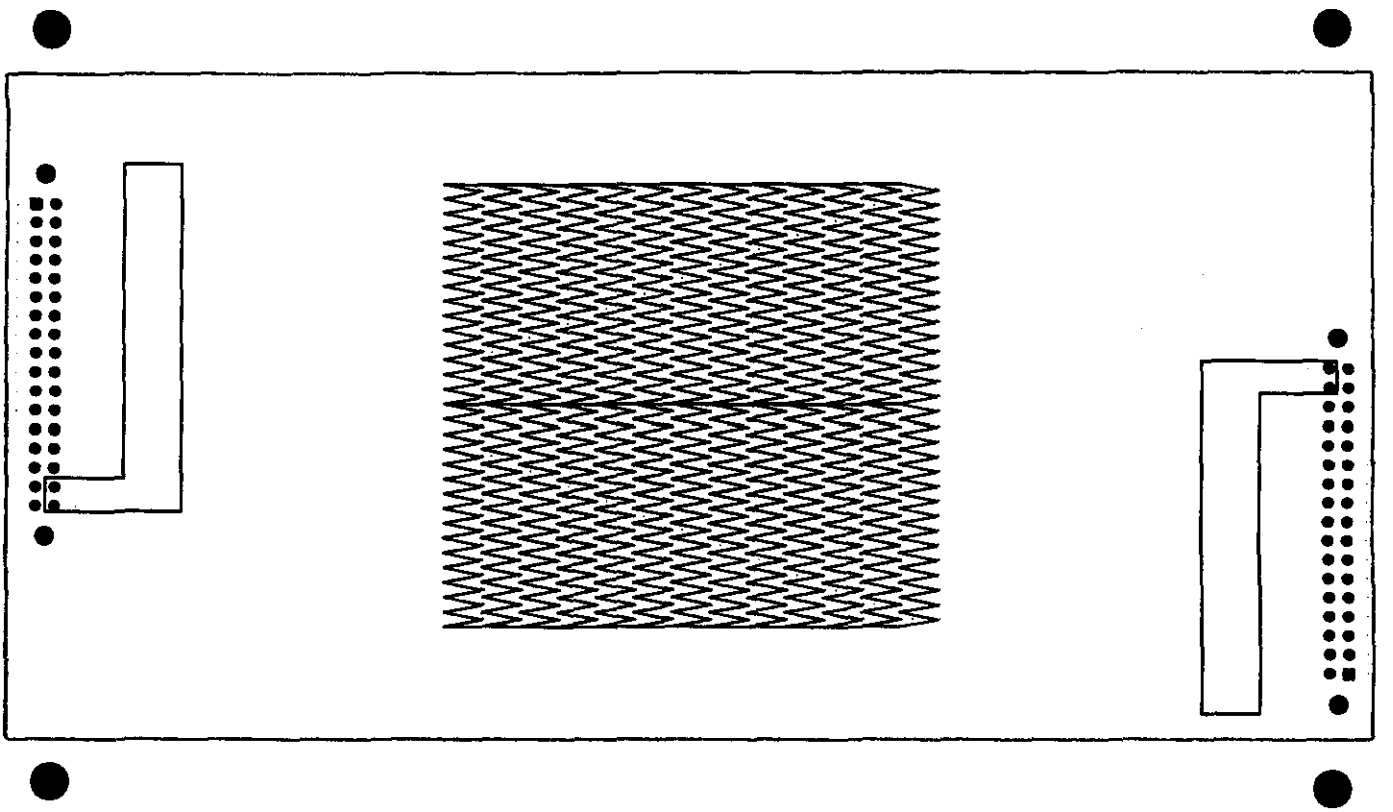
Interpolating Pad Chamber
GEM Prototype
Assembly Drawing
C. Bower 2/92



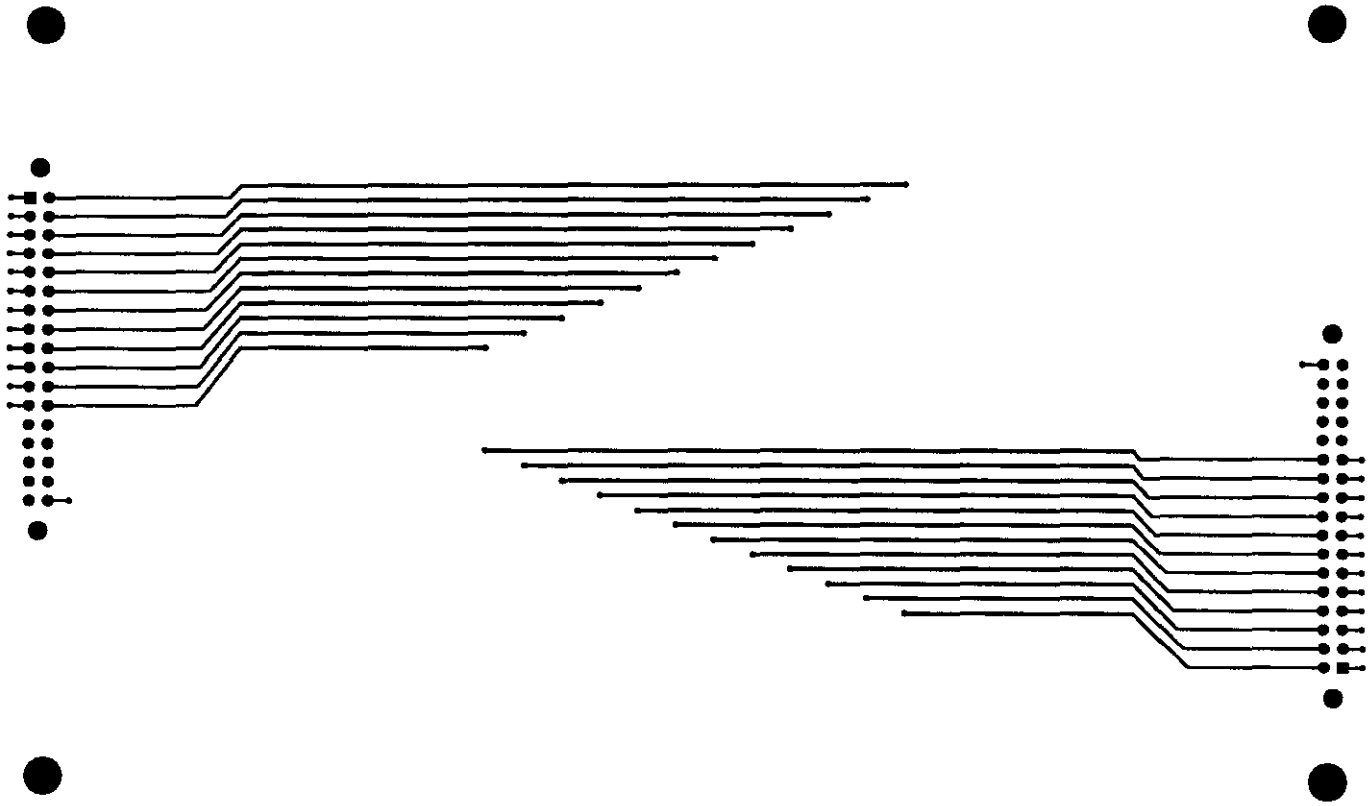
Interpolating Pad Chamber
GEM Prototype
Assembly Drawing
C. Bower 2/92

dimensions in inches

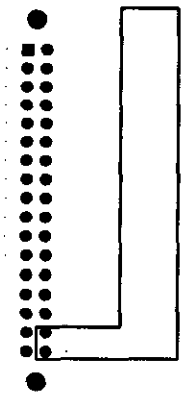
pad2.job - Wed Apr 01 12:04:42 1992

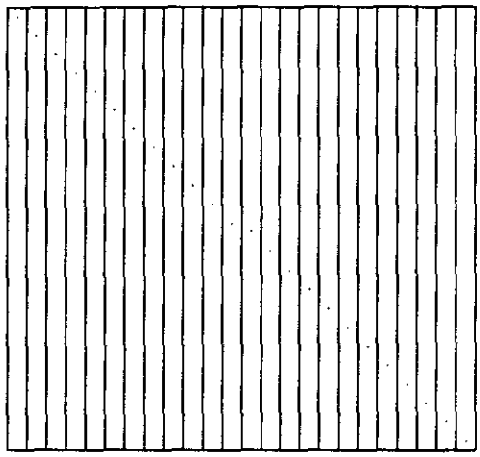


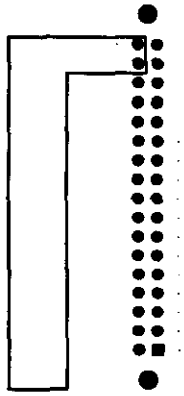
pad2.job - Wed Apr 01 12:04:48 1992



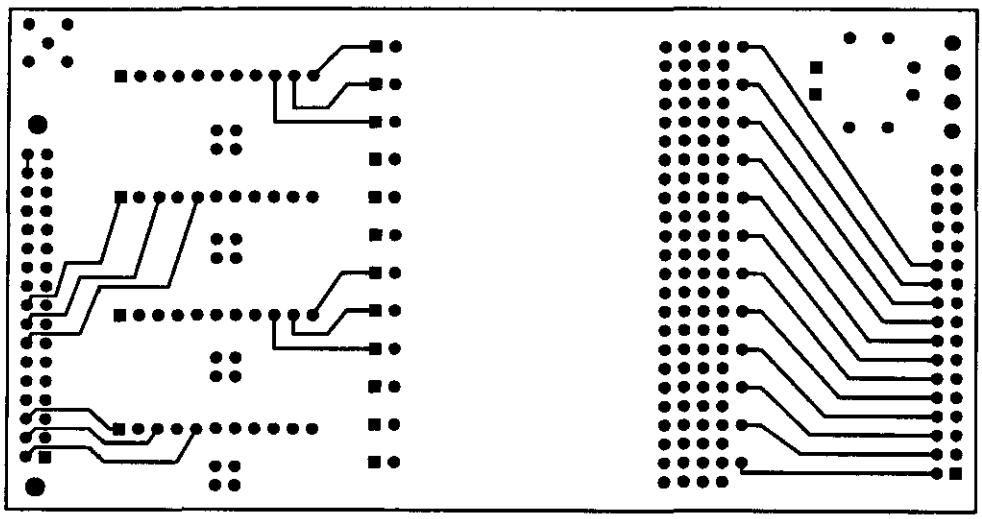
pad1.job - Wed Apr 01 12:02:58 1992

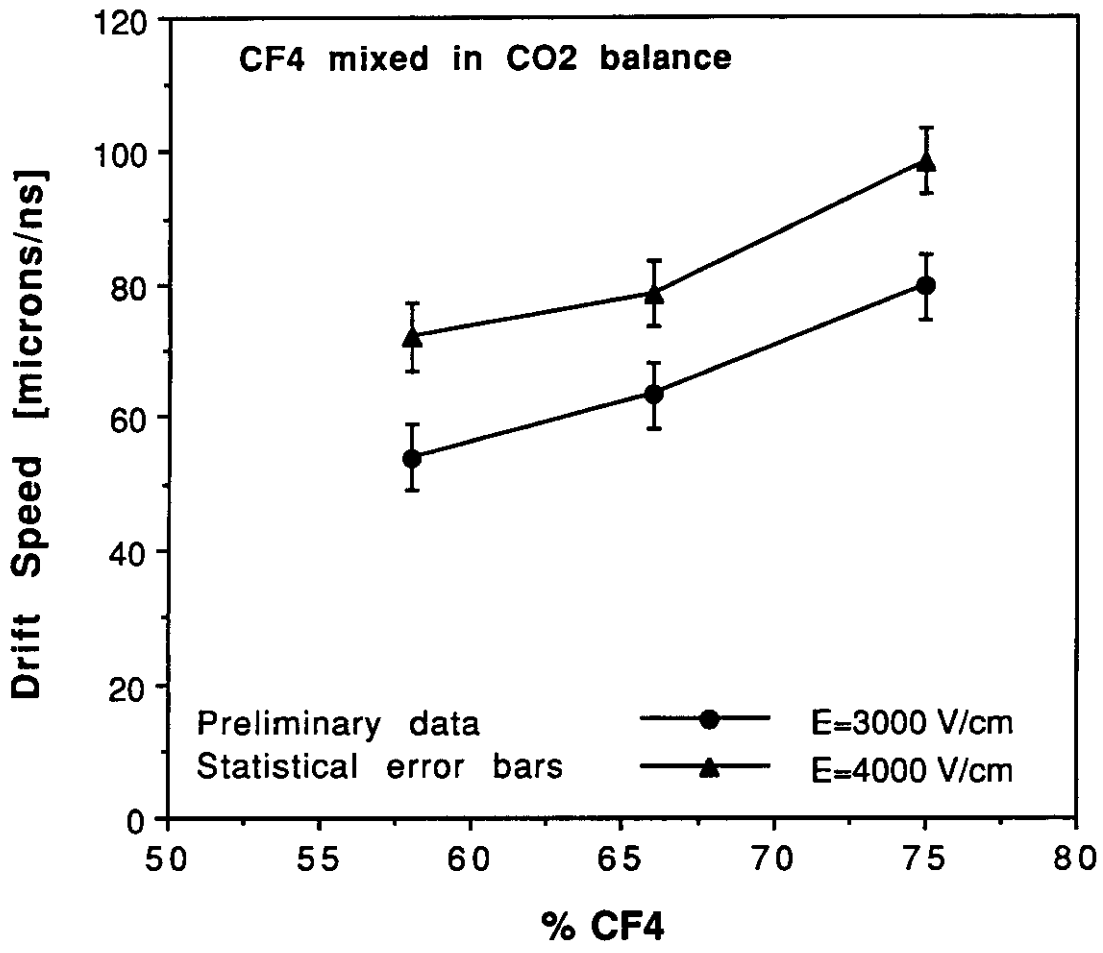


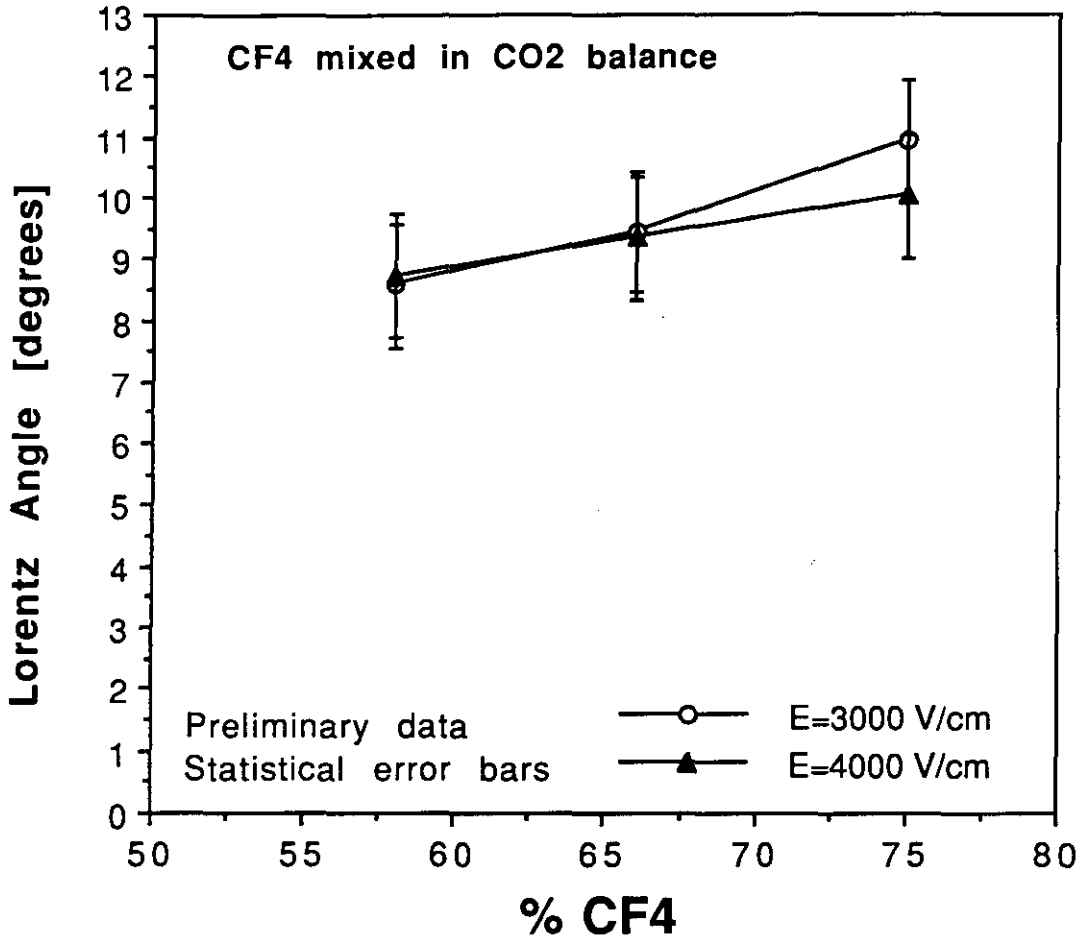


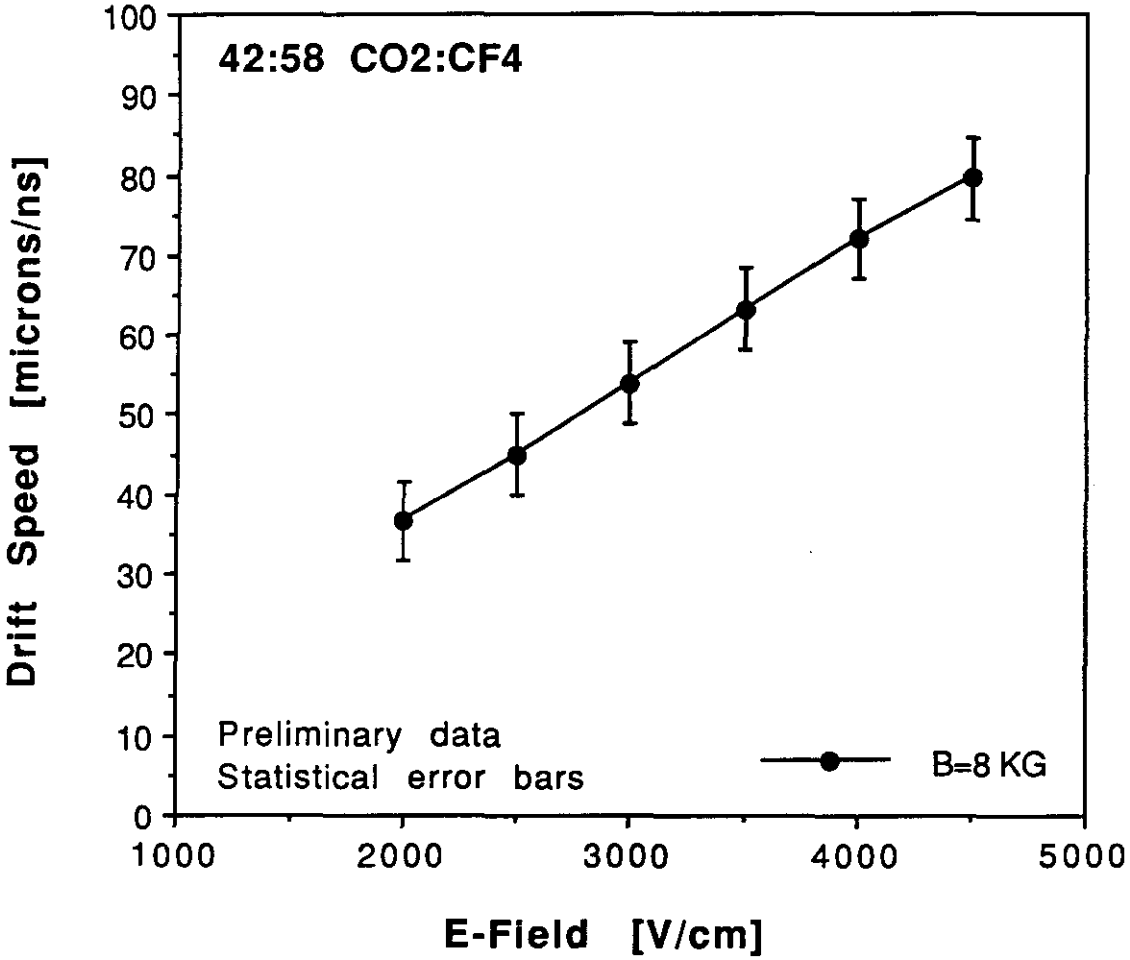


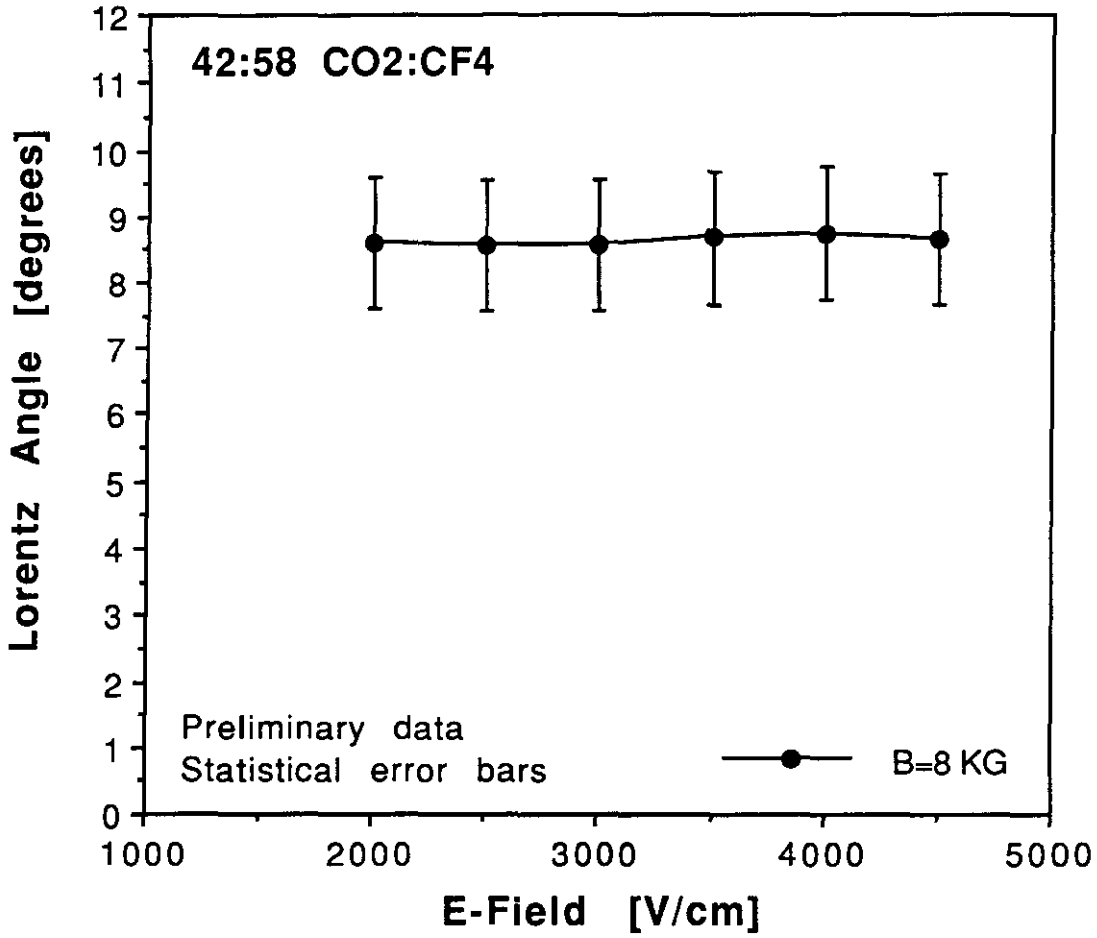
rdout.job - Wed Apr 01 12:59:02 1992




CF4 mixed in CO2 balance
Drift Speed [microns/ns]
% CF4
Preliminary data
Statistical error bars
E=3000 V/cm
E=4000 V/cm
0
20
40
60
80
100
120
50
55
60
65
70
75
80


CF4 mixed in CO2 balance
Lorentz Angle [degrees]
% CF4
Preliminary data
Statistical error bars
E=3000 V/cm
E=4000 V/cm
0
1
2
3
4
5
6
7
8
9
10
11
12
13
50
55
60
65
70
75
80


42:58 CO2:CF4
Drift Speed [microns/ns]
E-Field [V/cm]
Preliminary data
Statistical error bars
B=8 KG
0
10
20
30
40
50
60
70
80
90
100
1000
2000
3000
4000
5000


42:58 CO2:CF4
Lorentz Angle [degrees]
E-Field [V/cm]
Preliminary data
Statistical error bars
B=8 KG
0
1
2
3
4
5
6
7
8
9
10
11
12
1000
2000
3000
4000
5000

Components & Properties to be Investigated

A Pulse height & width; charge distribution, etc.

B Single track position resolution vs.:

1) position (DFNL)
2) incident angle
3) $\vec{B}$ field (0.8T)
4) event rate
5) fast shaping times

C Drift times

D 2 Track Resolution

IPC Prototype TEST MATRIX

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CHAMBER DESIGN																
12X Chev	X	X			X	X	X	X	X	X	X	X	X			
24X Chev			X													
Straight pads				X												
20 μm anode	X	X	X	X	X	X	X	X	X		X	X	X			
40 μm anode										X						
FILL GAS																
P10	X															
CF_4-CO_2		X	X	X	X	X	X	X	X	X	X	X	X			
ELECTRONICS																
slow	X	X	X	X		X										
fast					X		X	X	X	X	X	X	X			
MAGNET (0.8T)								X	X	X						
SOURCE																
X-Rays	X	X	X	X	X											
Cosmic Rays						X	X	X	X	X						
slow p											X					
fast ?												X	X			
NUMBER OF CHAMBERS	1	1	1	1	1	1	1	1	3	3	1	1	3			
PROPERTIES INVESTIGATED (see prev. page for codes)	A	A	B1	B1	A	A	A	A	B1	A	A	A	B1			
	B1	B1			B1	C	B5	C	B2	B1	B4		B4			
					B5				B3	B2			D			
										C						

Components & Properties to be Investigated

A Pulse height & width; charge distribution, etc.

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1) position (DFNL)
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C Drift times

D 2 Track Resolution

gem

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Test Beams

at

S.L.A.C

APRIL 2, 1992

TRACKER MEETING

TEST BEAMS
AT
S.L.A.C.

HISTORY:

* PAUL MOCKETT CONTACTED D. LEITH – 3/2/92
  1st INTEREST in SLAC T.B.'s

* JIM BRAU / J.V. CONTACTED ROGER Gearhart AND LOU KELLER ABOUT THE POSSIBILITIES OF USING SLAC TEST BEAM – 3/18/92
  ROGER + LOU WOULD LIKE TO GET T.B.'s BACK in OPERATIONS — <u>NEED MONEY</u>

* J.V. CONTACTED DAVID LEITH (3/31)
  VERY RECEPTIVE TO RESTORING BEAM LINE AND MAKING IT AVAILABLE TO "OUTSIDE" PHYSICS COMMUNITY – BUT – CANNOT MAKE DECISION UNTIL WITHERELL REPORTS TO DoE.

BEAM LINE-19 AT SLAC

* Will take ~ 1 year to commission; e^+ only

  COST: ~ \$250K - 400K

* $E_{max} \approx 25$ GeV; 10 - 20 pps

  $\frac{\Delta p}{p} = 0.2\%$

* To run parasitic w/ End Station A experiment (E-142 Pol. e^-'s on pol. He^3 target)

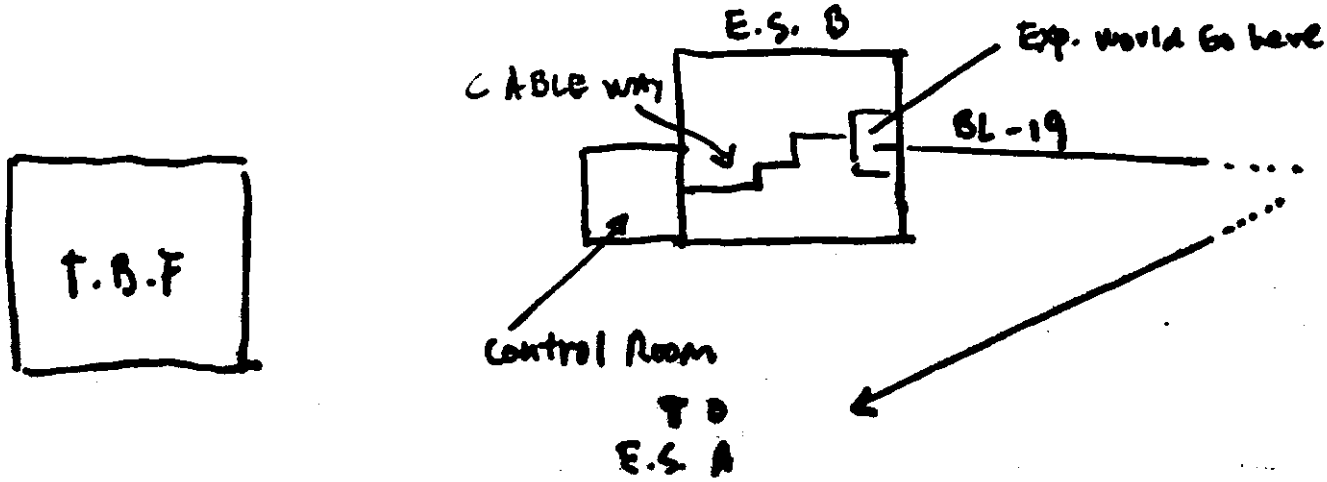
* Run time: ~ 3 mos./year

If SLAC started now (or before July '92)

- 3/92 - 3/93 to commission
- SLD to run 1/93 → ? (8/93)
- 1st opportunity to get test beam:

  ~ Fall of '93

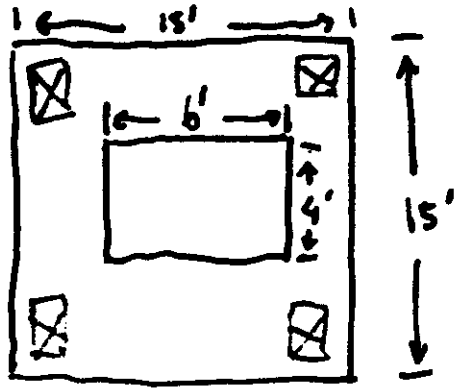
PHYSICAL LAYOUT



* AMPLE SPACE TO SET UP EXPERIMENT
* CABLE WAY IN PLACE WHICH LEADS TO CONTROL ROOM
* ACCESS TO VH/VMS ?? — DAQ?

IN TEST BEAM FACILITY (TBF)

* THERE IS A 1.3 or 1.6 T DIPOLE
* ROGER CLAIMS $\vec{B}$-FIELD IS VERTICLE!
  - JV: THINKS $\vec{B}$-FIELD IS HORIZONTAL
    coil windings indicate $\rightarrow \vec{B}$
* COST TO MOVE TO E.S. B ~ $ 100K



IF WE ARE INTERESTED . . . .

* MOCKETT et. al. NOT INTERESTED AT THIS BUT . . .

* IF WE ARE INTERESTED, SHOULD SUBMIT PROPOSAL TO SLAC (ROGER Gearhart's suggestion),

* IF WE DO DECIDE TO WRITE A PROPOSAL PAUL MOCKETT WOULD like to be part of it!