GEM TN-92-83

GEM Trigger/DAQ Group Meeting

March 8 & 10, 1992

Abstract:

Attenders and transparencies of the GEM Trigger/DAQ Group Meeting held on March 8 and 10, 1992, at the Collaboration Meetings in Tuscon

Tucson Trigger Meeting

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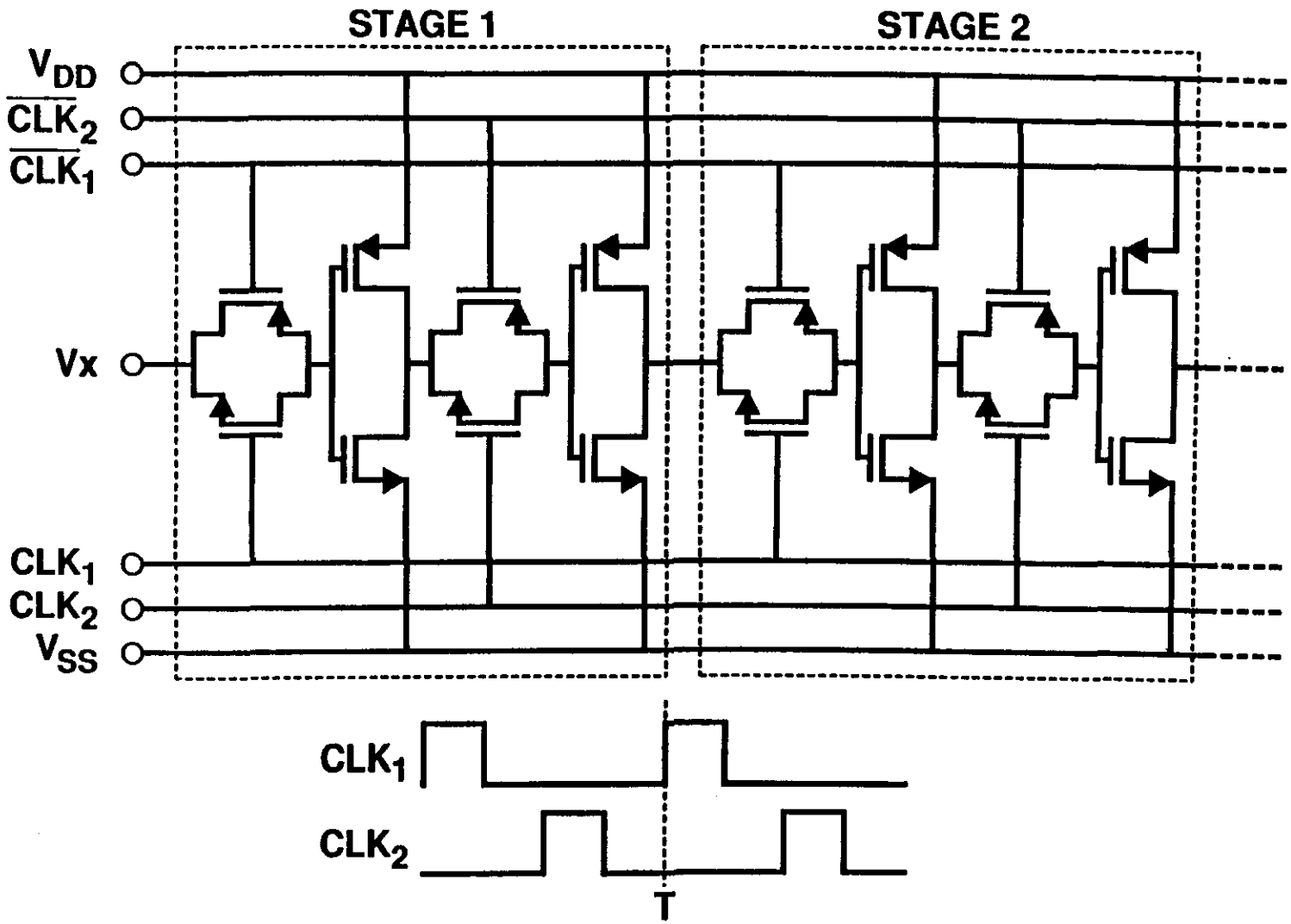
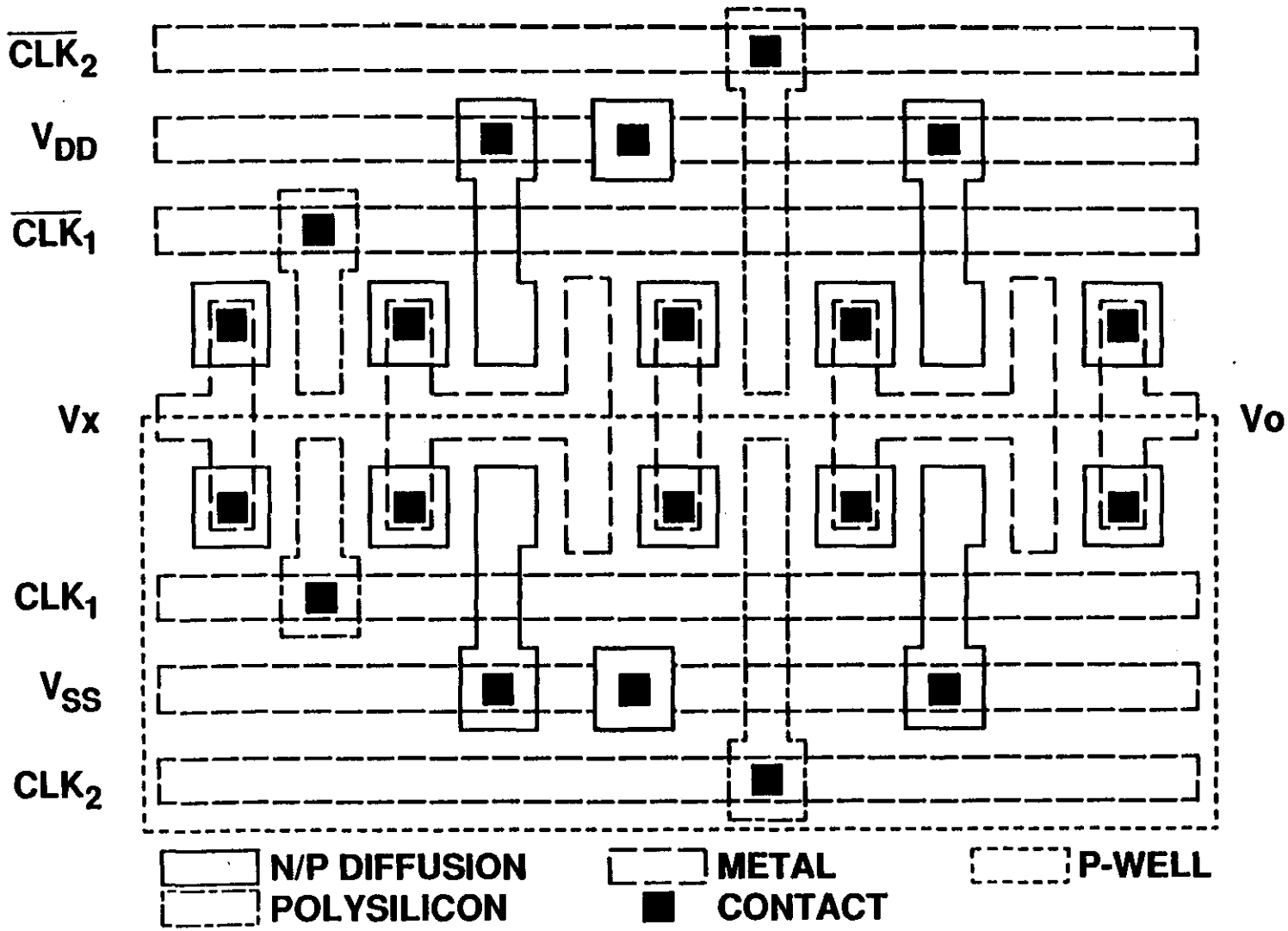
Presentation By:

Brad Cooke

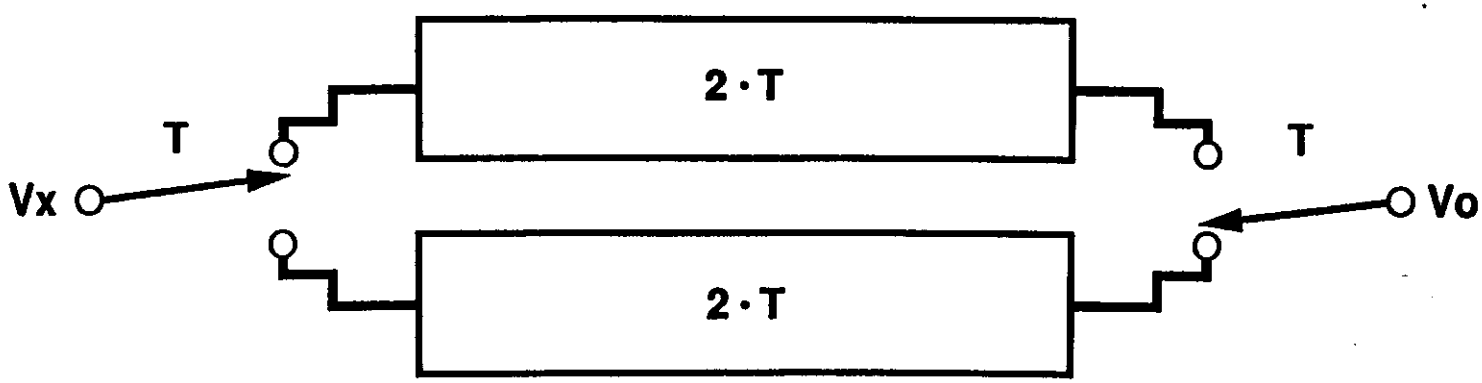
N-STAGE CMOS DYNAMIC SHIFT REGISTER



SINGLE-STAGE CMOS DYNAMIC SHIFT REGISTER CELL



ALLEVIATE BANDWIDTH CONGESTION WITH INPUT CHOPPING



SUPERCONDUCTING SUPER COLLIDER DATA COMPRESSION AND DRIVER/MODULATOR ARCHITECTURE

by
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Abstract

We present a prototype architecture that provides chip-level data compression and high-speed optical drive capabilities for rad-hard Superconducting Super Collider data acquisition applications. The data compression is accomplished through a pipelined edge-detection and clustering algorithm, while the driver/modulator uses high-throughput data-management techniques, including variable register lengths, bus queuing, and time-division-multiplexing for fast optical-data transmission. An architecture of this sort can provide efficient transmission of a very large numbers of events.

I. INTRODUCTION

The generic architecture of an inner-detector system is shown in Figure 1. The basic detector unit considered here is a silicon PIN-diode strip detector consisting of 500 to 1000 strips. A particle traversing a wafer will activate a

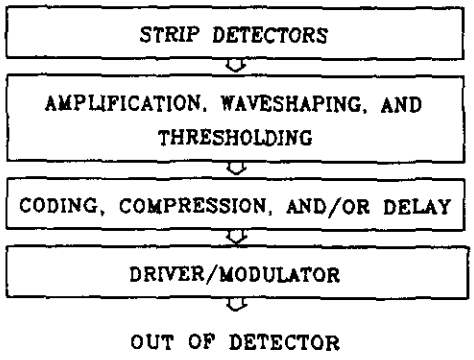


Figure 1. SSC Inner-Detector Architecture.

cluster of strips. The amplified strip signals provide the information on the position of a particle(s) in one dimension. The data acquisition task is to extract the locations of the activated strips and transmit this information to an external data-processing unit that can integrate information of many strip detectors.

Our paper will focus on a pipelined data compression and the driver/modulator architecture of the inner-detector system. Detailed information concerning the application of the data compression and driver/modulator in our prompt/delayed-channel pipelined encoder architecture can be found in [1].

II. DATA COMPRESSION ALGORITHM

The data compression is accomplished by transmitting cluster information instead of information about individual strips. The algorithm proceeds as follows: The raw data are first edge-detected, reducing the clusters to a series of edges. Then, using a pipelined architecture, the relative offsets of the edge boundaries are found. The resulting compressed data vector is then composed of the number of edges, the offsets of each edge from the previous edge, and, if desired, the total number of hits.

An illustration of the algorithm follows. Figure 2 shows a 16 bit (strip) detector with three "clusters" and a binary

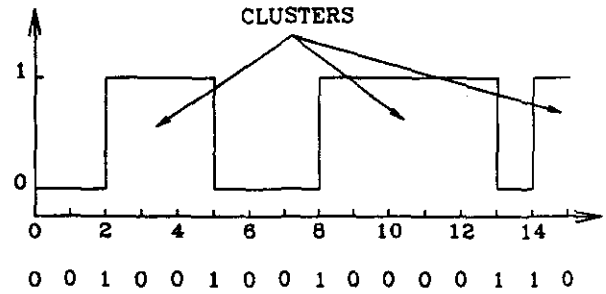


Figure 2. 16-Bit Detector With Three Clusters.

data vector representing the cluster edges. As the data vector is "passed through" the pipelined encoding algorithm, the edges are detected and the edge offsets counted. The decimal encoding of the three clusters in terms of pipeline stage, edge count, and accumulated offset reduce to the following:

Stage	# Edges	Offset
0	0	0
1	0	1
2	1	2/0
3	1	2/1
4	1	2/2
5	2	2/3/0
6	2	3/2/1
7	2	2/3/2
8	3	2/3/3/0
9	3	2/3/3/1
10	3	2/3/3/2
11	3	2/3/3/3
12	3	2/3/3/4
13	4	2/3/3/5/0
14	5	2/3/3/5/1/0
15	5	2/3/3/5/1/1.

Note that the "/" denotes an edge boundary and that it also needs to be encoded. The equivalent binary representation of the data vector in Figure 2 is

Stage	Accumulator	# Edges	Data Vector
0	[Offset] 0 [Edge] 0	0	0010010010000110
1	1 0	0	010010010000110
2	10 01	1	10010010000110
3	101 010	1	0010010000110
4	1010 0100	1	010010000110
5	1011 0101	10	10010000110
6	10111 01010	10	0010000110
7	101110 010100	10	010000110
8	101111 010101	11	10000110
9	1011111 0101010	11	0000110
10	10111110 01010100	11	000110
11	10111111 01010100	11	00110
12	101111100 010101000	11	0110
13	101111101 010101001	100	110
14	1011111011 0101010011	101	10
15	10111110111 01010100110,	101	0

where the input data vector is in the right hand column and the accumulated edge boundary and offset are on the left. The edge location and offset are now represented by two separate binary vectors. Note that a single vector element can be processed per pipeline stage allowing the algorithm to be implemented with a 60-MHz system clock (we are hard-pressed, as it is, to find a low-power, rad-hard CMOS process capable of 60-MHz operation, let alone a higher clock rate). Also, note that the compressed data is right (or left) justified.

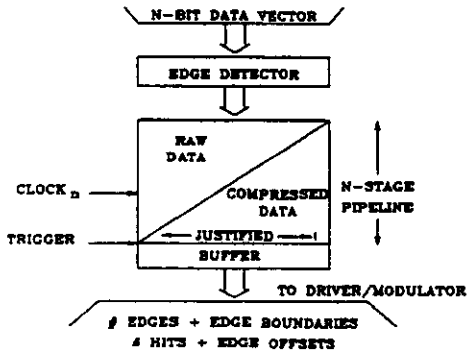


Figure 3. Compressor Architecture.

III. COMPRESSOR AND DRIVER/ MODULATOR ARCHITECTURE

A prototype compressor architecture is shown in Figure 3. The compressor would accept an N-bit data vector, edge detect, and it compresses the edge data utilizing the previously described compression algorithm. The edge detector and compressor can be implemented with relatively straight-forward digital logic and shift registers for the required pipelined architecture. The resulting two output vectors would then be composed of the number of edges + edge boundaries and the number of hits + edge offsets.

Typically, since N is on the order of 500-1000 bits and realistic chip Input/Outputs (I/O) are on the order of 100-200, input vector segmenting is required. A practical realization of a four-segment 4x128 (512-bit) compressor and driver/modulator architecture is shown in Figure 4. The chip

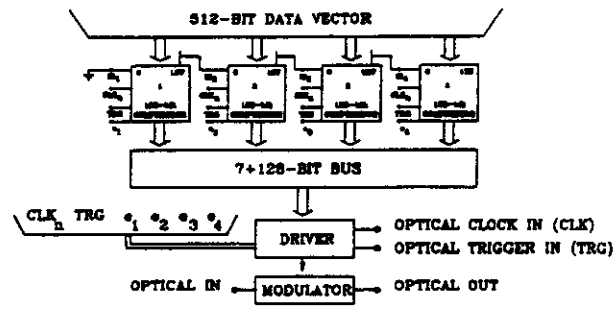


Figure 4. 4x128-Bit Compressor and Driver/Modulator.

set is composed of four 128-bit compressors. On arrival of the external trigger, the compressed data is multiplexed over a 7+128-bit data bus to the driver/modulator chip for optical transmission. While a segmented architecture allows the implementation of chips with reasonable I/O pin counts, data compression is degraded as will be discussed in Section IV. Figure 5 shows the corresponding driver/modulator architecture for the 4x128 compressor. The 4x(7+128)-bit vector segments are sequentially read and stored in the bus buffer registers. After the bus buffer acquires all four data segments, a fast block transfer of the segments is made to the time-division-multiplexing (TDM) buffer where each segment is then sequentially shifted into the TDM variable length drive register for optical transmission. The TDM variable length drive register provides a means of sending only non-zero compressed information (determined by the edge-count vector), preventing the transmission of redundant information. The 2:1 TDM modulator takes advantage of the equal lengths of edge boundary and offset vectors. Note that an optical clock and trigger are used to minimize time jitter.

IV. MONTE CARLO SIMULATION

The compression efficiency of the algorithm for single and multiple segmented compressors was evaluated with a simple a Monte Carlo simulation. The simulation observed the following steps:

(i) Random selection of the positions of clusters over the width of the detector wafer.

(ii) Random selection of the width of each cluster.

(iii) Calculate the encoded binary representation.

(iv) Repeat i-iii to determine the average compression ratio.

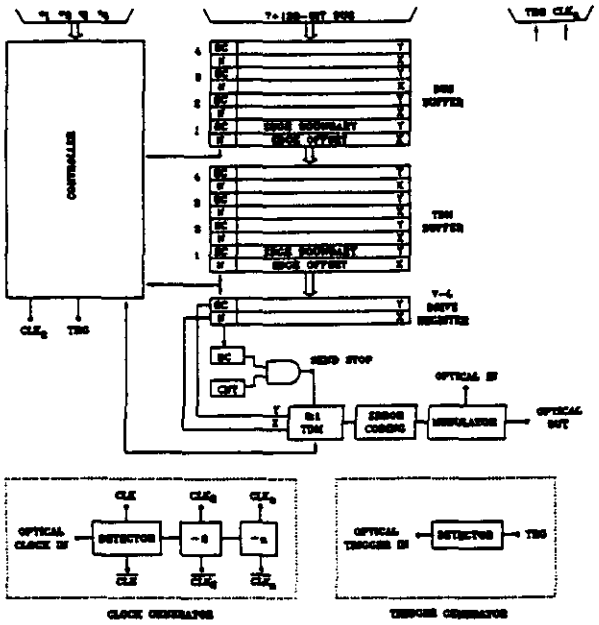


Figure 5. 128-Bit Driver/Modulator Architecture.

A uniform distribution is assumed for (i) and (ii). In addition, the clusters are composed of 1 to 7 hit strips and are allowed to overlap. The average compression ratio was defined as

$$\frac{\text{Total Number of Strips}}{\langle\text{Offset Vector + Boundary Vector}\rangle},$$

where <> indicates averaging over 25 samples. Figures 6 and 7 show the compression ratios for a single-segment and a 4-segment 512-bit compressor. The single-segment compressor yields a 15:1 compression for a single cluster and 6:1 for five clusters, while the 4-segment provides a 7.5:1 and 4.5:1 compression ratio for one and five clusters, respectively. The degraded efficiency is caused by the reduction in binary encoding efficiency with decreasing vector size and encoding clusters which overlap segment boundaries (such clusters require two or more binary numbers to encode). Hence, compression efficiency is penalized as the number of segments are increased and data vector lengths are reduced. Techniques to improve segmented compression by combining segments before transmission are under investigation. Note that the sum of the offsets in a segment will always add up to the segment size, thus providing an end-of-transmission sum-check.

V. CIRCUIT DESIGN CRITERIA

This section considers various design criteria associated with the practical implementation of the compressor and driver/modulator architecture.

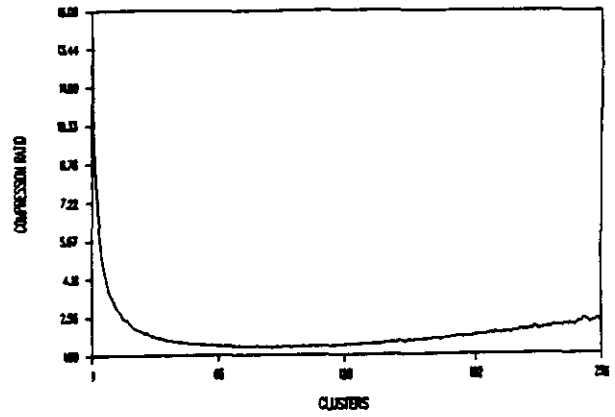


Figure 6. Compression Ratio for a Single-Segment, 512-Bit Vector.

A. Compressor Register Requirements

The minimum number of registers required to implement a 512-bit compressor architecture for 1 to 8 segments assuming a 60 MHz clock rate, 1-shift/cycle, and 1-add/cycle is as follows:

Segment Size	# Registers	Compression
512	393K	15:1
256	196K	10.5:1
128	98K	7.5:1
64	49K	5:1.

Note that the pipeline delay, compression efficiency, bandwidth (the product of segment size times 60-MHz clock rate), and number of registers (i.e. circuit density and power dissipation) can be traded off. Again, emphasis should be placed on the fact that segment size will be limited, by practical engineering considerations, to I/O pins counts of 100-200.

An estimate of the approximate power dissipation per register can now be obtained. Using the 4x128 compressor chip discussed in section III, there are 25K registers required per chip. If a total of 250 mW of power is allocated for the data compression of 512 bits, then each chip is limited to approximately 63 mW, or leaving less than 2.5μW per register not including overhead chip circuitry. Note that the compressor architecture requires 50% more registers than does a simple delay line architecture.

B. Driver and Optical Modulator

The driver/modulator chip can be implemented with various technologies depending on cost, speed, power dissipation, and complexity. For our SSC applications, we are considering three combinations of driver-modulator topologies: Silicon-$LiNbO_3$, GaAs-$LiNbO_3$, and GaAs-GaAs. The silicon and GaAs drivers devices would be bipolar and MESFET respectively while the $LiNbO_3$ and GaAs modulators are both electrooptic waveguide devices [2].

A summary of the three driver/modulator technologies under consideration is as follows:

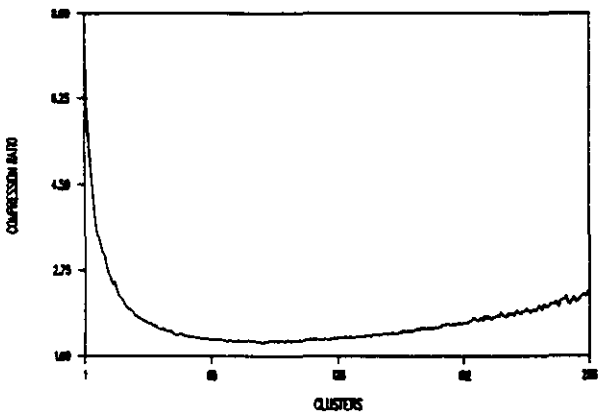


Figure 7. Compression Ratio for a Four-Segment, 512-Bit Vector.

Driver-Modulator	Speed	Technology
Silicon-$LiNbO_3$	Moderate	Mature
GaAs-$LiNbO_3$	Moderate+	New
GaAs-GaAs	Fast	Under Development.

The first two technologies are hybrid devices where the $LiNbO_3$ modulator is wire bonded to the silicon or GaAs substrate while the third integrates the driver and modulator on the same substrate, reducing parasitic losses and potentially reducing production costs. The best power-speed figure is realized with GaAs High-Electron-Mobility-Transistors (HEMT) [3]. However, it should be noted that HEMT processes are still primarily confined to laboratories and not readily commercially available. In addition, GaAs chips in general exhibit a lower thermal conductivity then its silicon counterpart.

Our preliminary design goal is the development of a silicon-$LiNbO_3$ driver/modulator operating at 1-5 GHz with a power dissipation of 250-500mW (if this goal is unattainable we will then focus on an HEMT driver). The optical modulator prototype is a Mach-Zehnder interferometer [2] adapted for a low drive digital voltage [4]. A LANL radiation exposure test of the $LiNbO_3$ Mach-Zehnder interferometer (total dose 10^{14} 647 MeV protons/cm^2) [5] along with the appropriate selection of optical fibers [6] indicate that good resistance to SSC level radiation exposure can be expected.

VI. CONCLUSION

We have presented a prototype architecture that provides chip-level data compression and high-speed optical drive capabilities for rad-hard Superconducting Super Collider data acquisition applications. We have discussed how data compression is accomplished through clustering and introduced a flexible high-speed driver/modulator for fast optical-data transmission. A practical 4x128 compressor architecture was introduced to illustrate the algorithm. We believe an architecture of this sort can provide efficient transmission of very large numbers of events.

VII. REFERENCES

[1] B. J. Cooke, K. S. Lackner, D. H. Sharp, and C. L. Winter, "Efficient Data Transmission From Silicon Wafer Strip Detectors," Nuclear Science Symposium, Santa Fe, NM, Nov. 5-9, 1991.

[2] R. C. Alferness, "Waveguide Electrooptic Modulators," IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-30, No. 8, August 1982.

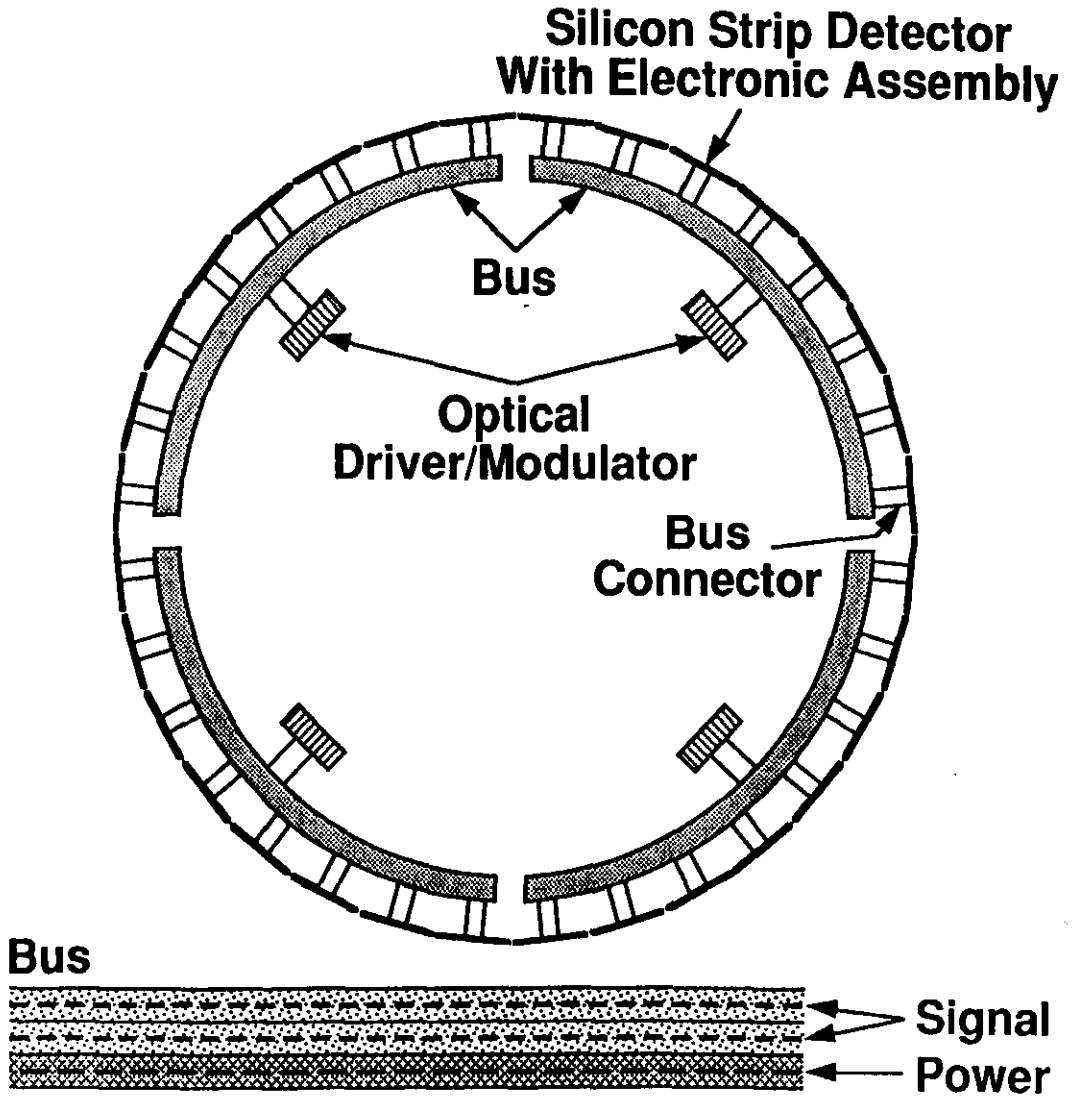
[3] M. Abe, T. Mimura, K. Nishiuchi, A. Shibatomi, M. Kobayashi, and T. Misugi, "Ultra-High-Speed HEMT Integrated Circuits," Semiconductors and Semimetals, Vol. 24, Academic Press, 1987, pp. 253-254.

[4] J. L. Jackel, and J. J. Johnson, "Nonsymmetric Mach-Zehnder Interferometers Used as Low-Drive-Voltage Modulators," Journal of Lightwave Technology, Vol. 6, No. 8, August 1988, pp. 1348-1351.

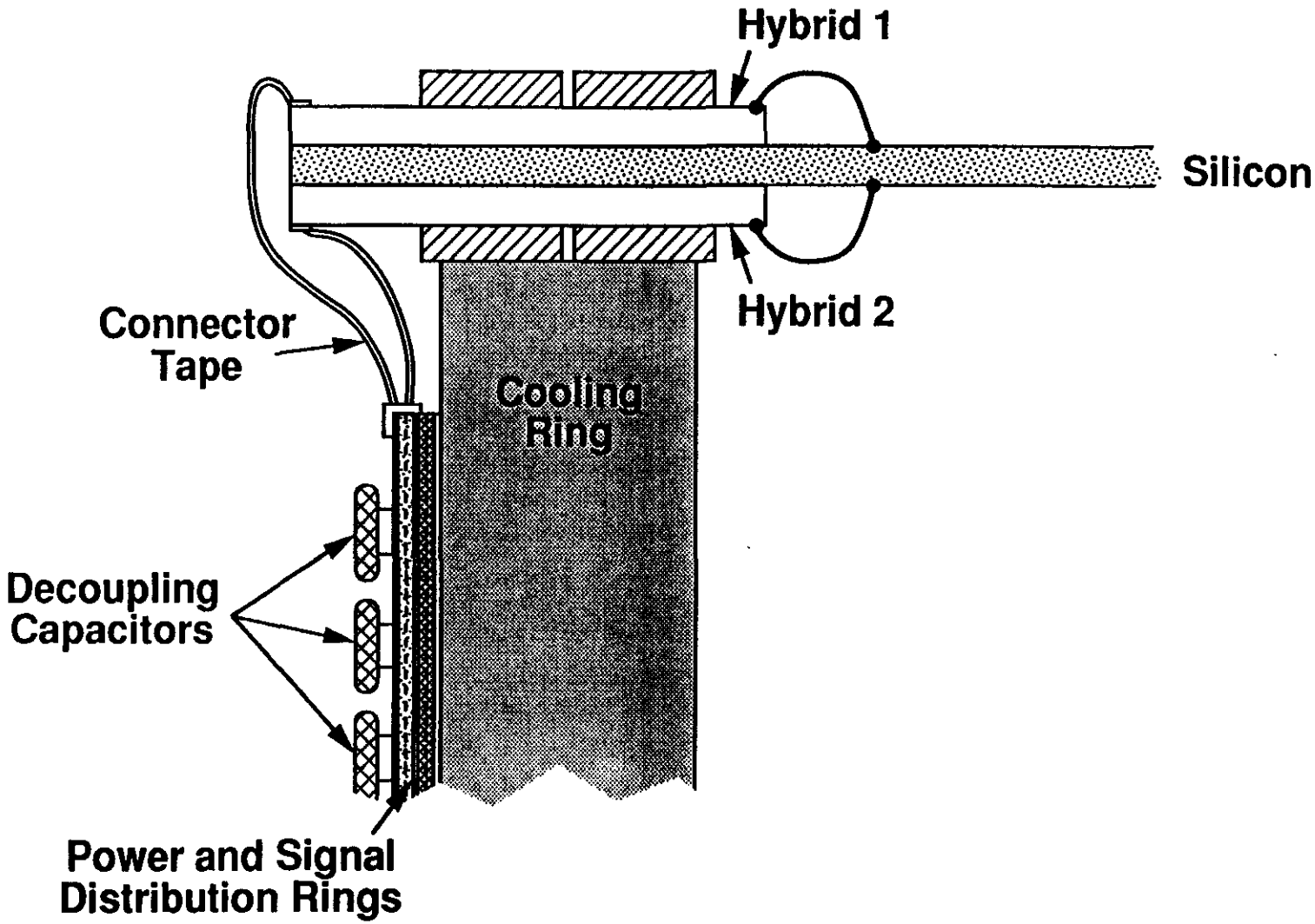
[5] Private Communication H. Ziock Los Alamos National Lab and M. Lowry Lawrence Livermore National Lab.

[6] B. D. Evans and G. H. Sigel, Jr., "Radiation Resistant Fiber Optic Materials and Waveguides," IEEE Transactions on Nuclear Science, Vol. NS-22, No. 6, December 1975, pp. 2462-2474.

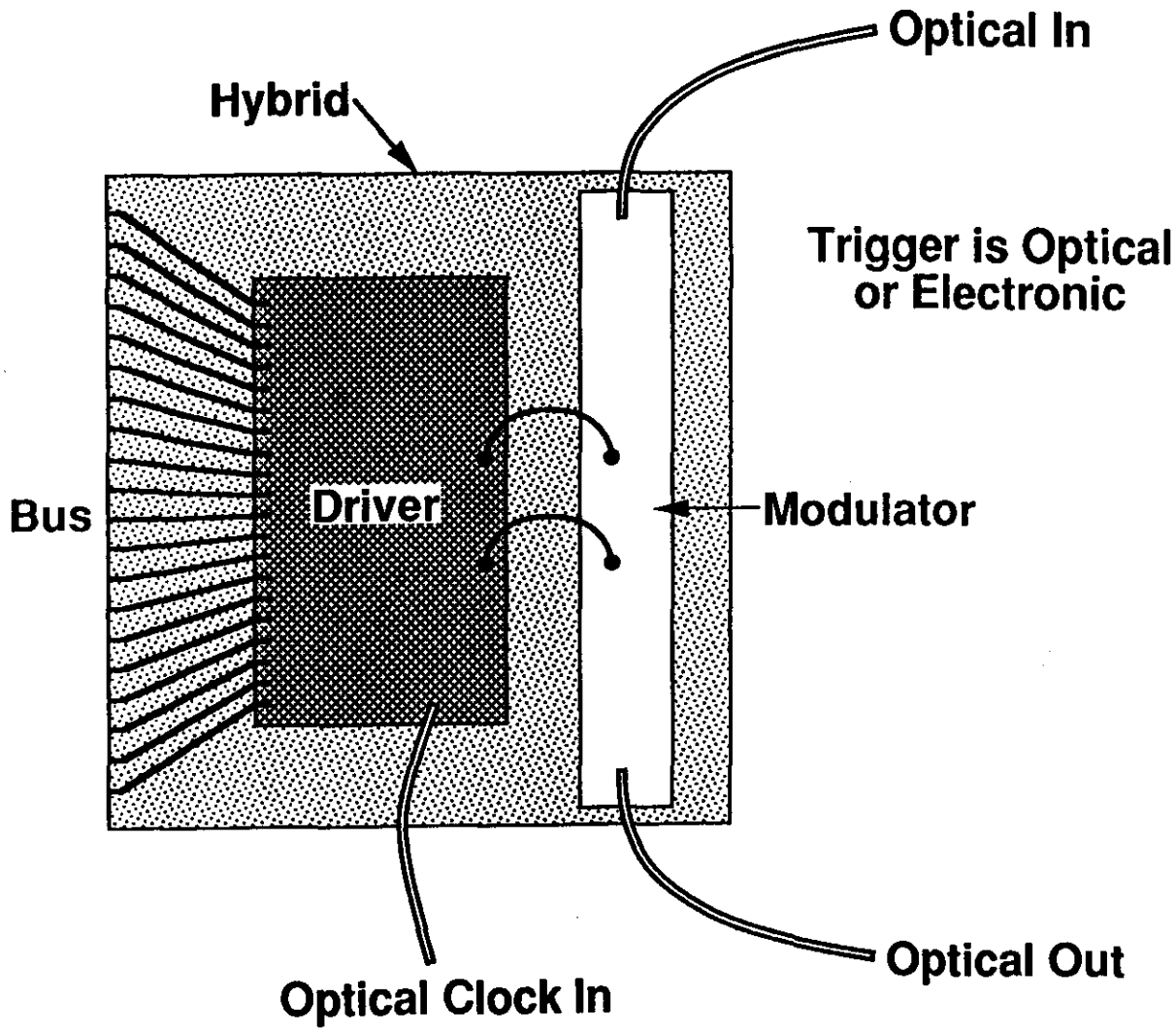
SILICON TRACKING SYSTEM WAFER SHELL



DOUBLE SIDED SILICON STRIP DETECTOR WITH ELECTRONIC ASSEMBLY



OPTICAL DRIVER/MODULATOR

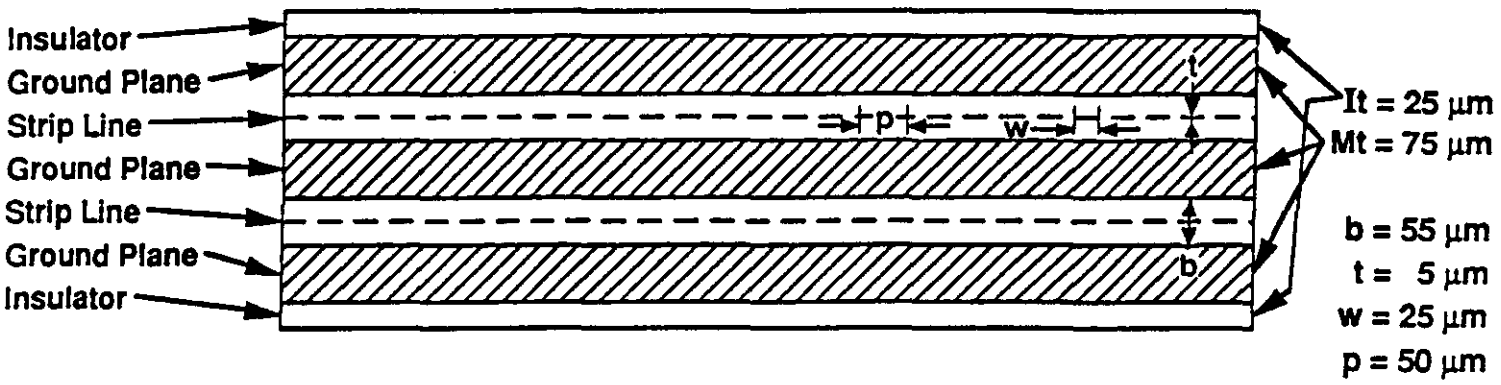


TECHNOLOGICAL ADVANTAGES OF HEMTs COMPARED WITH VARIOUS COMPETING HIGH-SPEED DEVICE APPROACHES

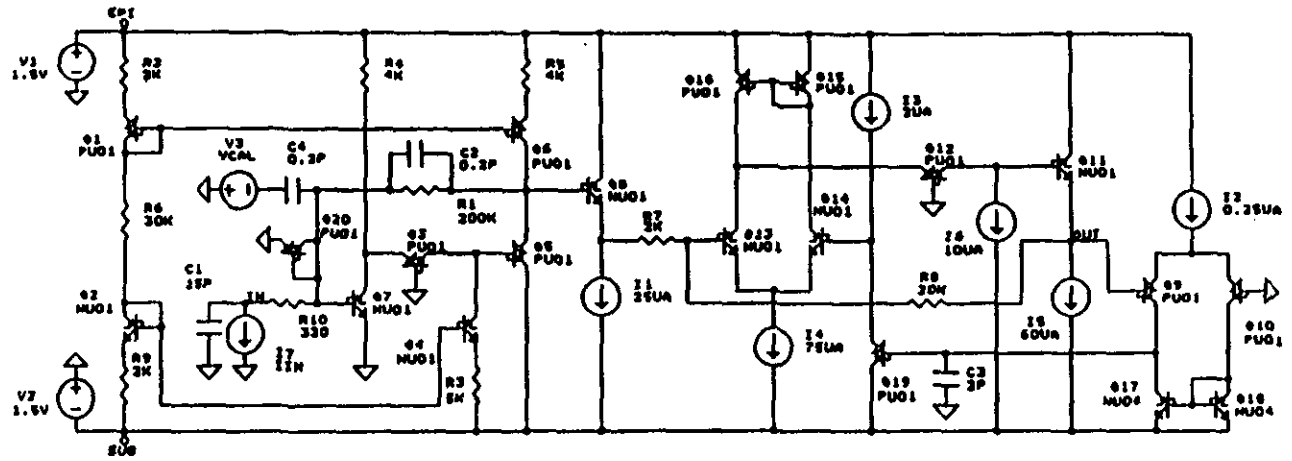
Device Approach	Performance		Uniformity and Controllability (σV_T/swing ratio)	Fabricability	Material Problems	Total Advantages
	Speed	Power				
HEMT L_G = 0.5 -1 μm	Excellent 10 ps Highly Geometry Contollable	Very Good 0.1 mW	Excellent 10-20 mV (2%)	Excellent Simple MBE and Dry Etching	Good Defect and Trap-Free epi High Throughput	Excellent
GaAs MESFET L_G = 0.5 -1 μm	Good 20 - 30 ps Poor Geometry Controllable	Good 1 mW	Good 60 mV (10%)	Excellent Simple	Good Defect-Free Ingot	Good
GaAs/AlGaAs HBT	Excellent 10-30 ps	Good 1 mW	Excellent (<1%)	Complex New Process Required	Good Defect and Trap-Free epi High Throughput	Unknown
Si MOSFET	Very Poor 80 ps	Very Good 0.1 mW	Excellent (1%)	Complex	Excellent	Difficult To High Speeds
Si Bipolar	Good 30 - 60 ps	Poor 1 -10 mW	Excellent (<1%)	Complex	Excellent	Difficult To Large Scale

M. Abe et al, Semiconductor and Semimetals, Vol. 24

SILICON TRACKING SYSTEM
2-LAYER HYBRID



Material	Zo (ohm)	Attenuation (dB/cm) @ 100 MHz	Thermal Resistance (C/W/cm^2)	Radiation Length (%)
Kapton	47	3.4	1.03	0.31
AlN	30	5.3	0.017	0.44
BeO	34	4.7	0.017	0.36
Alumina	29	5.6	0.061	0.47
SiC	14	11.7	0.017	0.44



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Date	February 10, 1992	Sheet 1 of 1

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Presentation By:

Dan Marlow

Muon Trigger Comparison

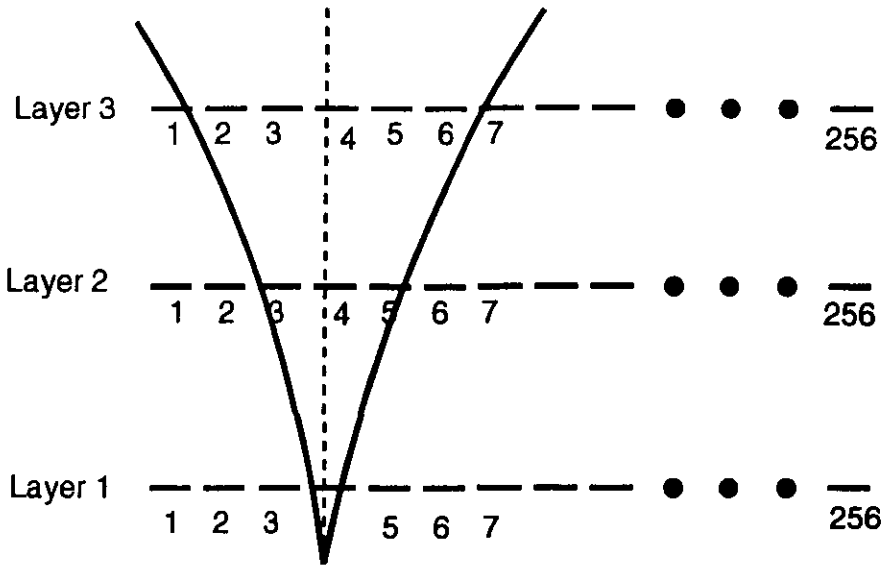
Pipelined Muon Logic

- Advantages
  - — Conceptually Simple
  - — Robust: Immune to extra hits
  - — $\sim$ Zero deadtime
- Disadvantages
  - — Cable intensive (not so bad for barrel RPC's, but getting up there for endcap CSC's)
  - — (probably) requires custom IC development

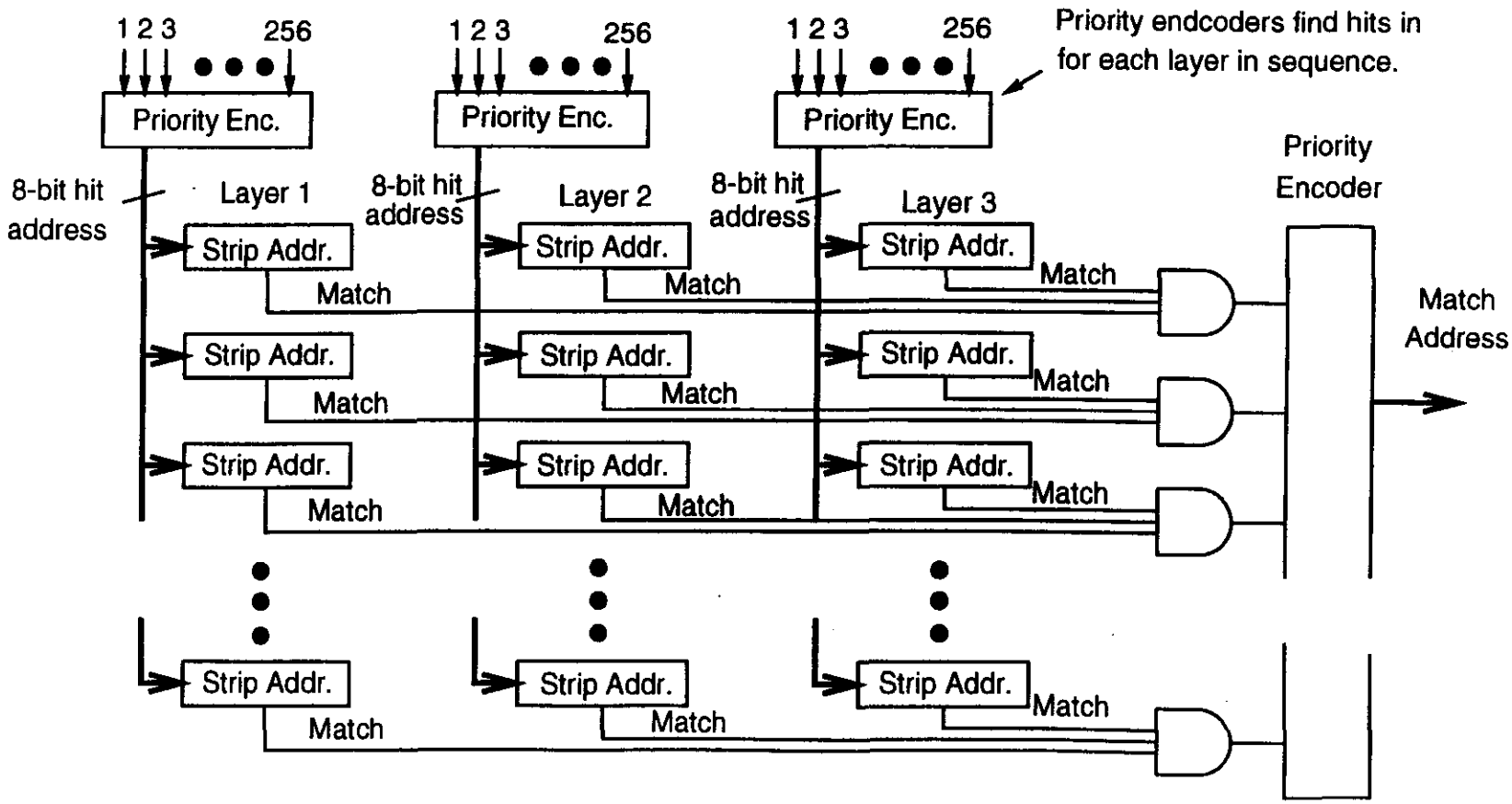
Associative (Content Addressable) Memory Logic

- Advantages
  - — Greatly reduces cable plant
  - — Robust: Immune to extra hits and inefficiency
- Disadvantages
  - — Cannot obviously be pipelined
  - — Requires custom IC development

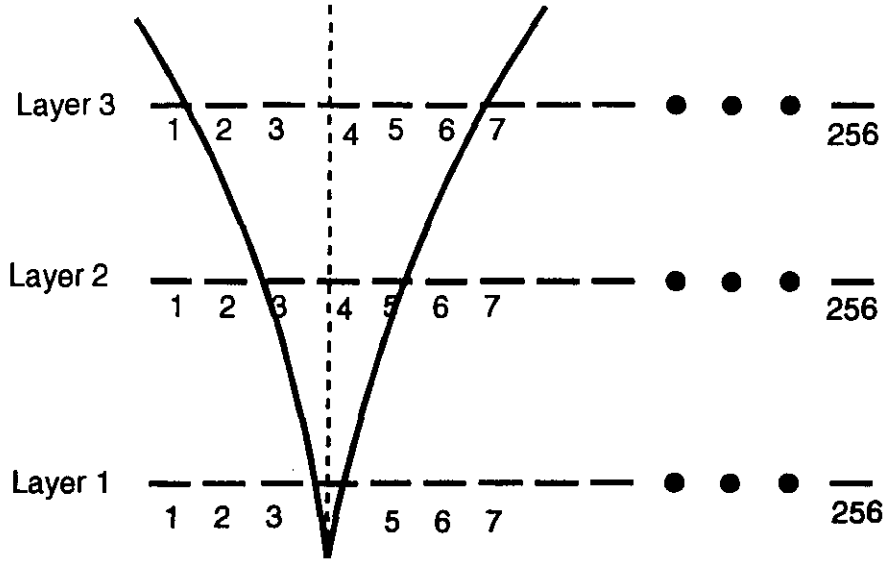
Question: Can we get the best of both worlds—i.e. a pipelined scheme with a light cable plant?

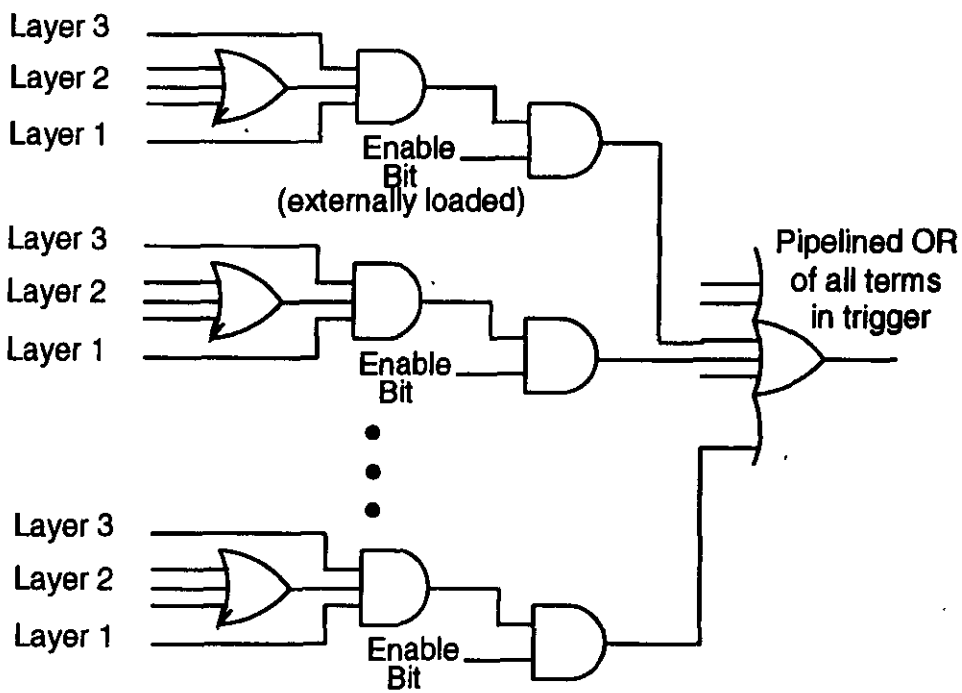


Content Addressable Memory Logic for Muon Trigger



Pipelined Muon Logic





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Presentation By:

Mark Lowry

An Update on the LLNL Electro-optics Effort in Support of the GEM Detector

Kent McCammon, Electronics Engineer
Mark Lowry, NTES Photonics Project Leader
L-Division
Phone: 510/423-2924; email:Mlowry@LLNL.Gov

Lawrence Livermore National Laboratory

presented to

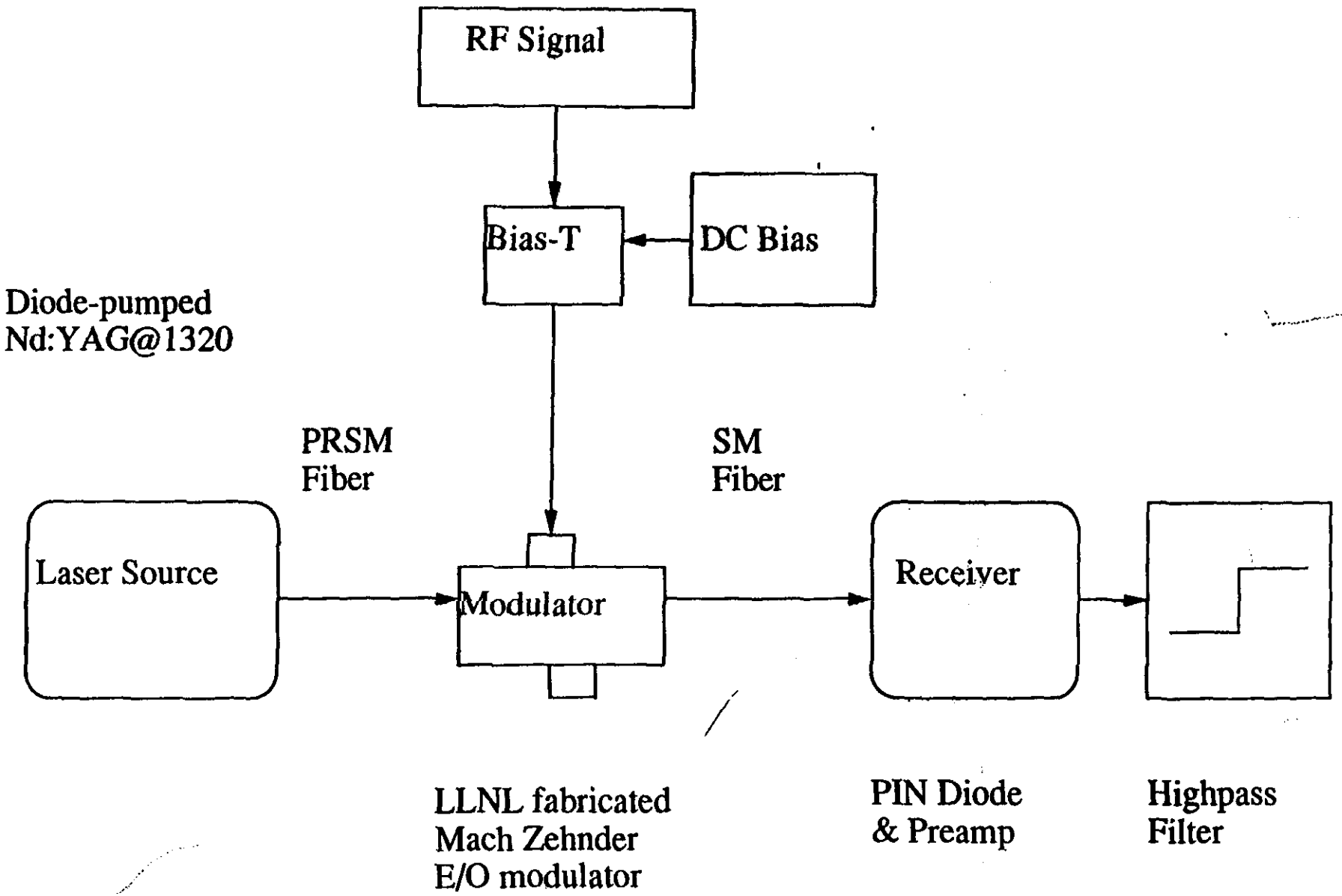
GEM collaboration
Detector Electronics Group
3/8/92
Tucson, AZ

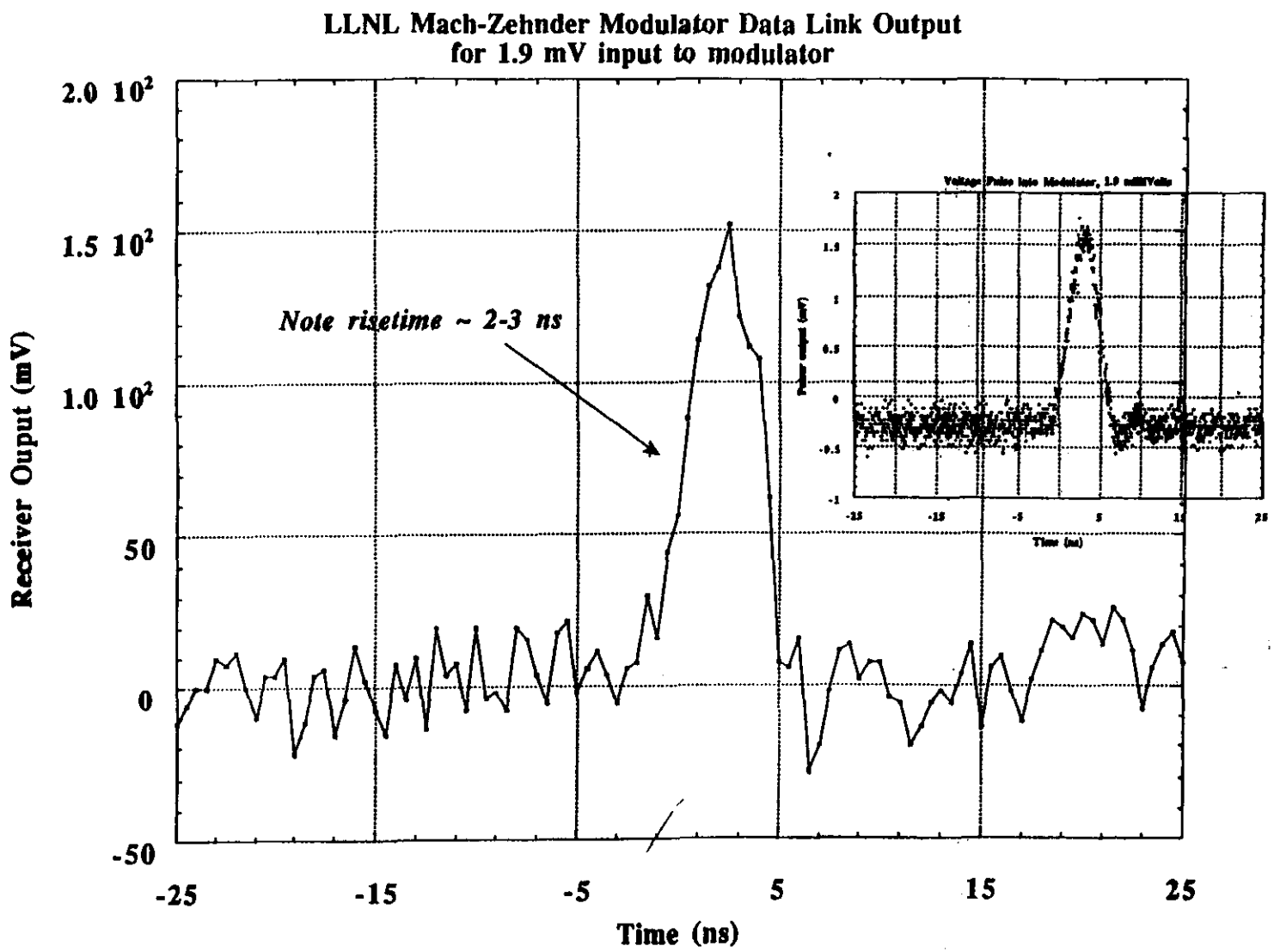
Outline for LLNL E/O update

- Our latest direct charge-readout data link results using the MIT drift tube (now better fidelity than the conventional)
  - link output scope data
    - s/n, voltage and charge sensitivity
    - system bandwidth and signal risetime
    - implications for muon chamber timing data, from drift tube data
  - Pulse-height spectrum from Fe^{55}

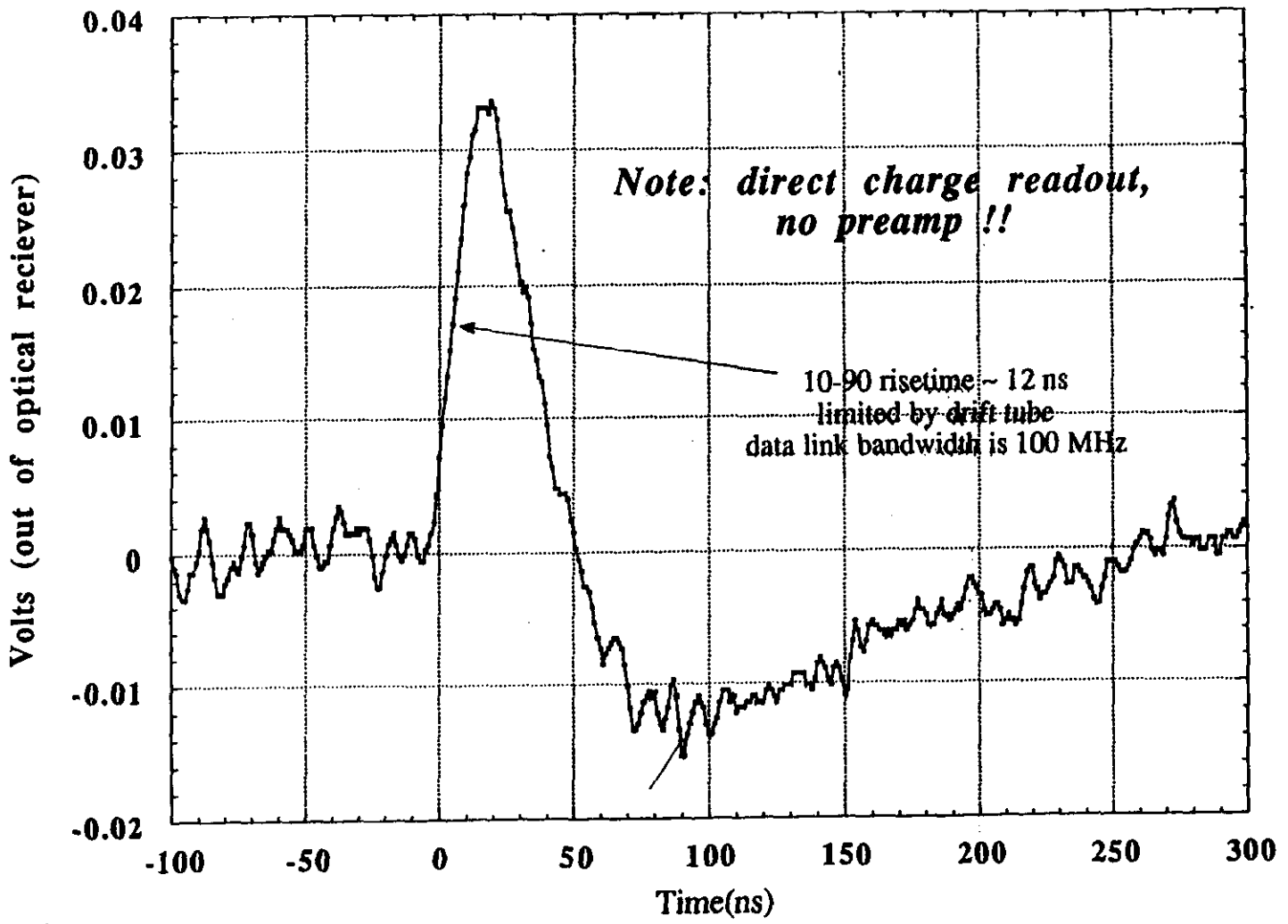
- Update on IOCC's flip-chip multi-channel modulator packaging work (R. Becker, et.al.)

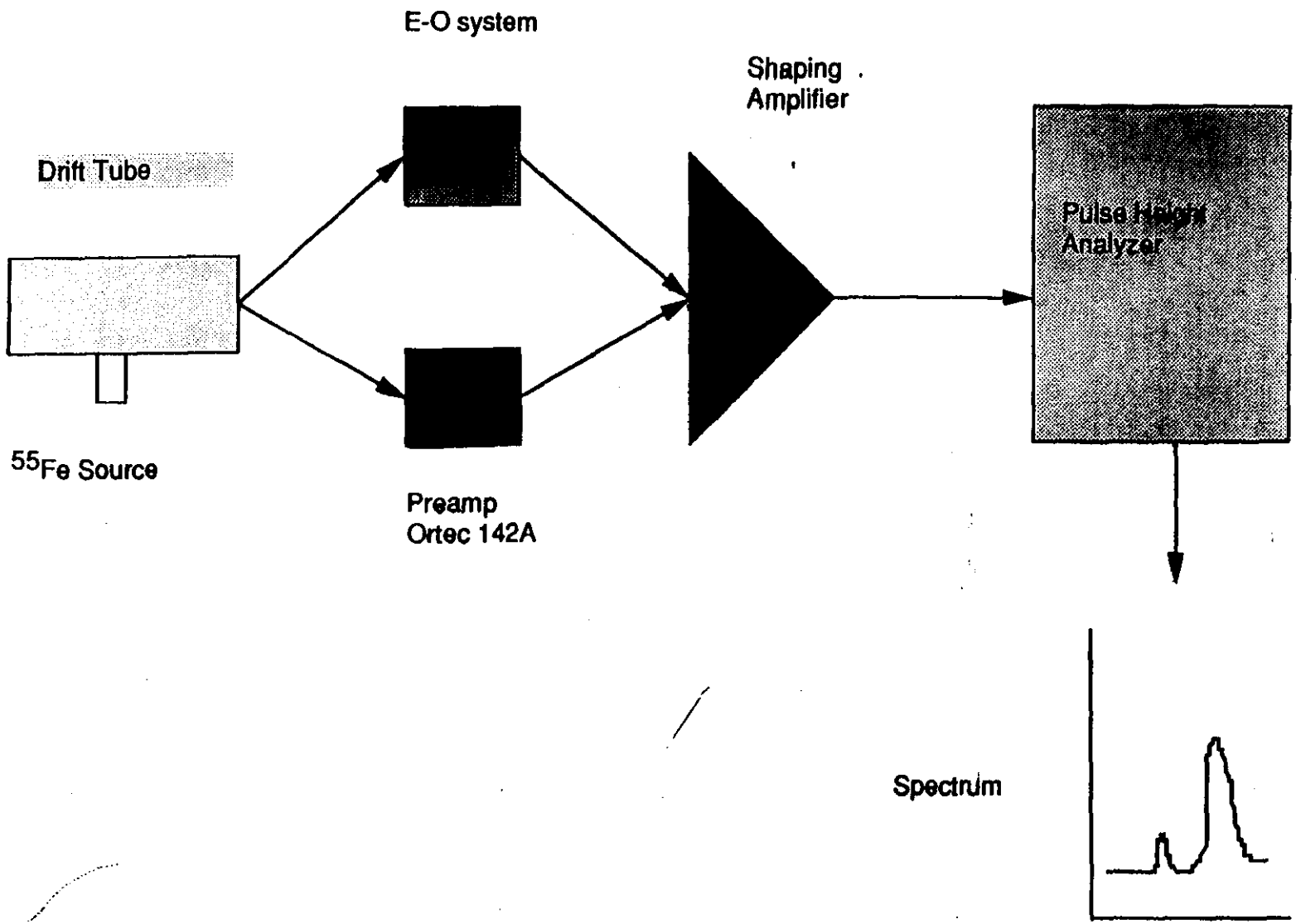
- Some E/O system architecture proposals (extrapolating from M. Seman's proposals)
  - Pr (or Nd) fiber amplifiers (at 1300 nm)
  - unpolarized optical sources (at 1300 nm)


RF Signal
Bias-T
DC Bias
Diode-pumped
Nd:YAG@1320
PRSM
Fiber
SM
Fiber
Laser Source
Modulator
Receiver
LLNL fabricated
Mach Zehnder
E/O modulator
PIN Diode
& Preamp
Highpass
Filter


LLNL Mach-Zehnder Modulator Data Link Output
for 1.9 mV input to modulator
Note risetime ~ 2-3 ns
Receiver Ouput (mV)
2.0 10²
1.5 10²
1.0 10²
50
0
-50
-25
-15
-5
5
15
25
Time (ns)

MIT drift tube signal through LLNL modulator
bias voltage 1790 V,
modulator termination 400 Ohms
5 mW of optical power

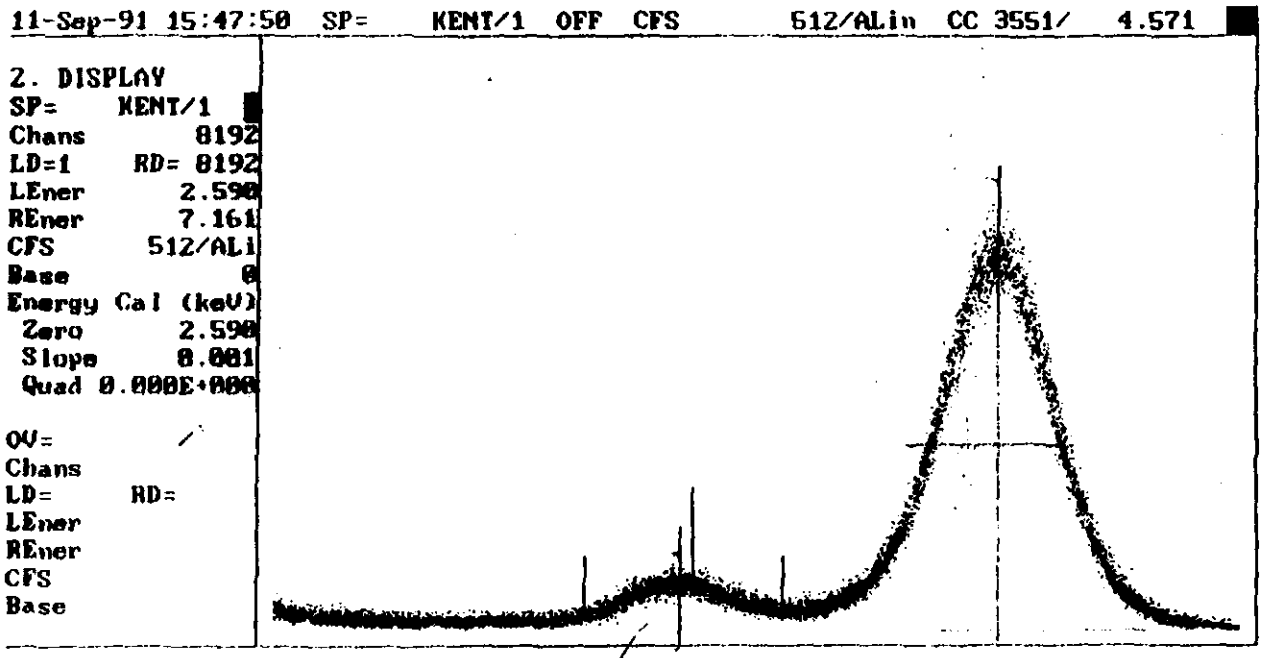



E-O system
Shaping
Amplifier
Drift Tube
Pulse Height
Analyzer
55Fe Source
Preamp
Ortec 142A
Spectrum

Tube Voltage 1790

Fe^{55} Spectrum using preamp.

Ortec 142 preamp



4.31 cm

FWHM = 1.8, 5 cm

$$FWHM = 1.85 \times \left(\frac{3\,KeV}{4.31}\right) = \underline{1.28\,KeV}$$

Tube voltage 17 kV

Link

Fe^{55} Spectrum using LLNL Modulator Link.

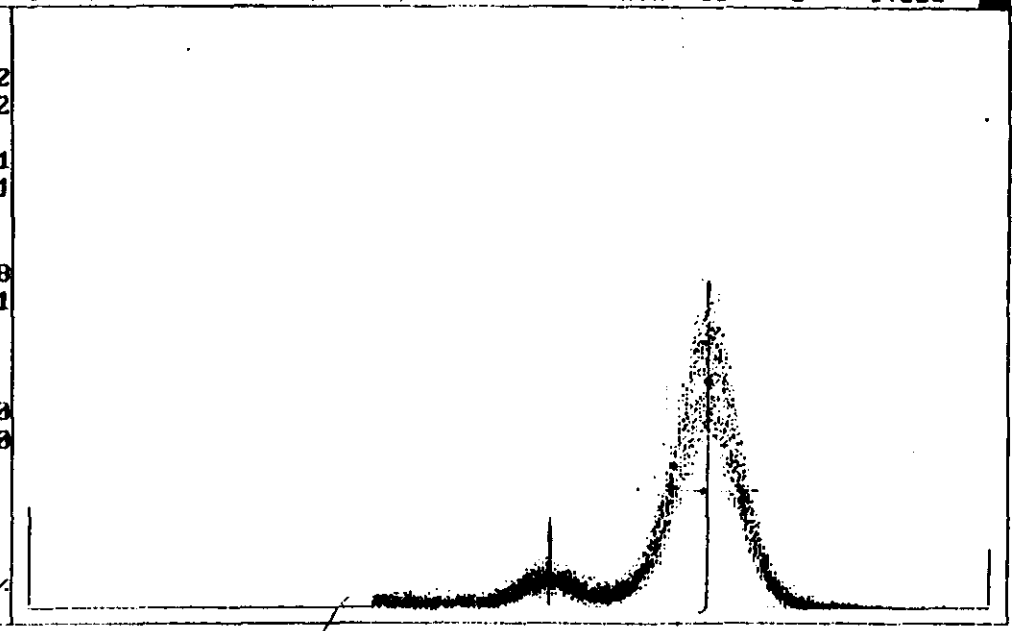
11-Sep-91 16:20:05 SP= LINK/1 OFF CFS 512/ALin CC 1/ 1.000

1. ACQUISITION
Chans 8192
LD=1 RD= 8192
Acq Start
11-SEP-91
16:12:51

ELAPSED
Live 00:06:37.68
Real 00:06:48.91
Totl

PRESET
Live 00:00:00.00
Real 00:00:00.00
Totl
Start
End

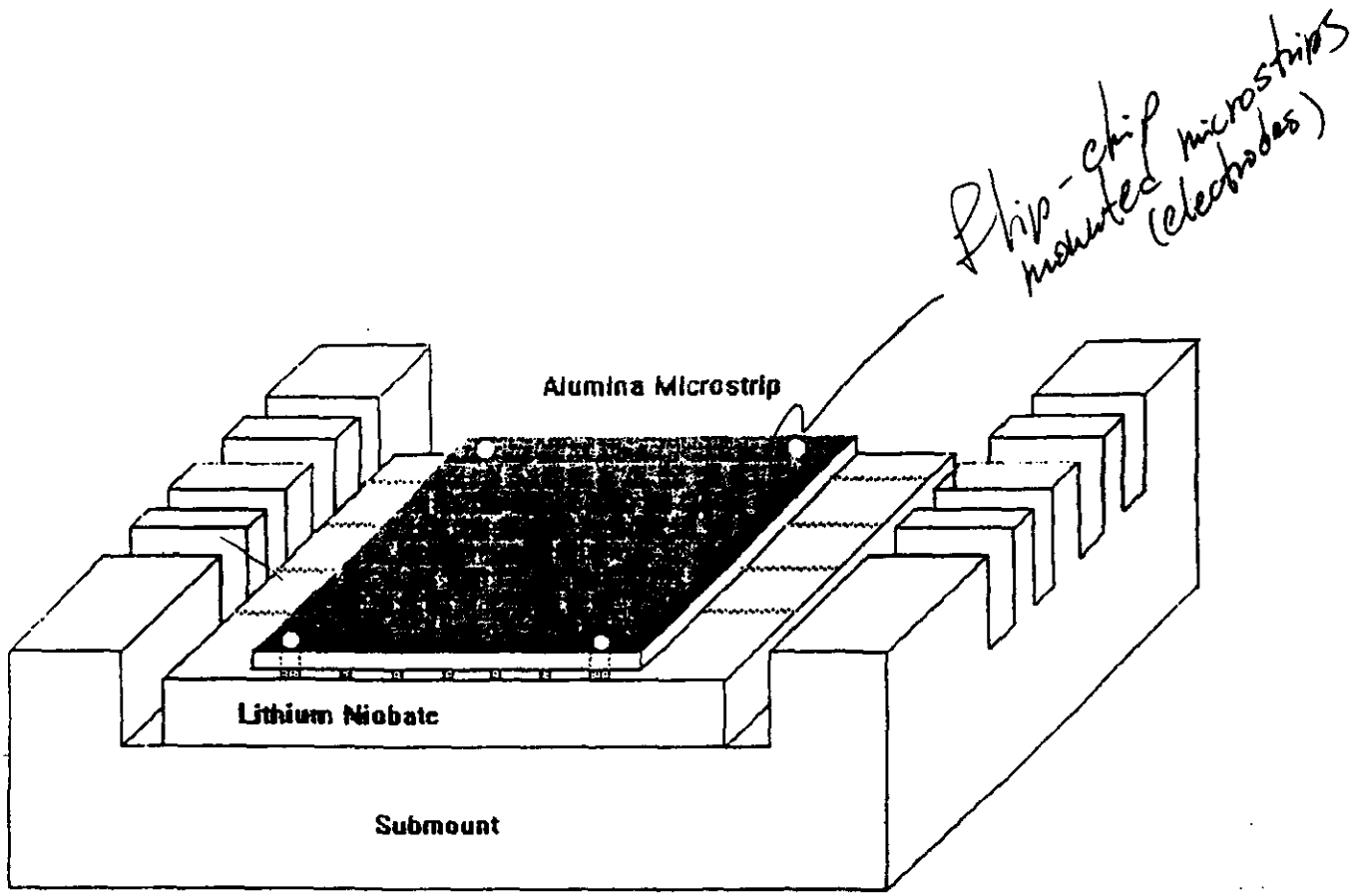
Dead Time 3%



2.18cm

FWHM = 0.98cm (3keV / 2.18keV) = 1.35 keV

IOCC's Multi-channel Modulator Package Approach (courtesy of Rich Becker)

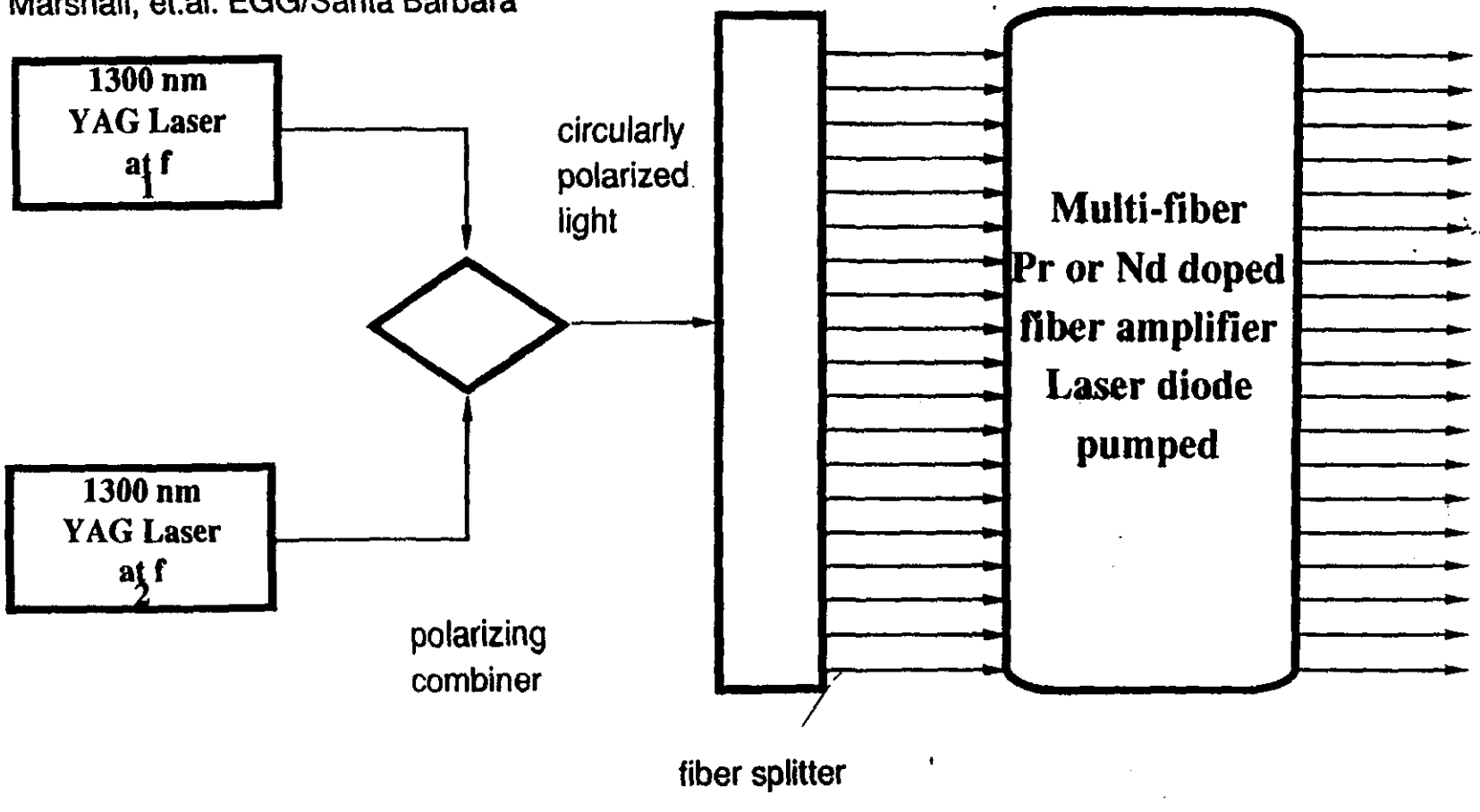


Sketch of Prototype (Fibers Not Shown).

A Proposal for Optical Power Distribution for E/O Modulators, extrapolating from the ideas of M. Seman, Columbia

Already done by Burns et. al NRL
and
Marshall, et.al. EGG/Santa Barbara

see proceedings of OFC '92,
San Jose



Acknowledgements

Yann-Hann Chang, MIT
Boleh Wyslouch, MIT
U. Becker, MIT

Rich Becker, IOCC

Funded by LLNL, LDRD

gem

γeμ

Presentation By:

John Parsons

STATUS OF CAL ELECTRONICS WORK

J. Parsons
Tucson,
Mar. 1/92

→ are continuing series of "working meetings" of those working on development of CAL electronics

→ last meeting was Feb. 13/92 @ BNL

→ next meeting proposed for

APRIL 2 @ NEVIS

GEM Calorimeter Electronics Meeting at BNL, Feb. 13/1992

AGENDA

10:00 - 10:05

Introduction - J. Parsons

10:05 - 11:20

LAr "Front End"

(25') Remote pre-amp option - S. Rescia
(25') Cold pre-amp radiation tests - V. Radeka
(25') Pulse shaping studies - P. O'Connor

11:20 - 11:50

Status of SCA Testing/Development - B. Sippach

11:50 - 12:15

ORNL Measurements - C. Britton

12:15 - 1:30 - LUNCH

1:30 - 1:45

CAL Readout Ideas from L* - Y. Kamyshkov

1:45 - 2:45

CAL Trigger

(20') Reconstruction of jet energy - Y. Kamyshkov
(20') CAL Trigger Schemes - D. Marlow
(20') Status of CAL FLT work - B. Clelland

2:45 - 4:00

Testbeam Electronics

(20') BNL Electronics for LAr tests - D. Lissauer
(20') Sampling electronics for LAr tests - J. Parsons
(20') BaF2 testbeam plan and electronics - D. Marlow/C. Britton
(15') SciFi testbeam plans - E. Hazen
(10') Preradiator testbeam - D. Strom

4:10 Future Plans and Organization

SOME NEWS FROM FEB 13 MEETING

① LAr "Front-End" Work @ BNL

→ Sergio Rescia: looked at noise considerations of placing pre-amp outside cryostat

CONCLUSION: for $\tau_p \sim 40$ ns, use "cold preamp". for $\tau_p \lesssim 20$ ns (eg. in Forward CAL, transmission line is useful.

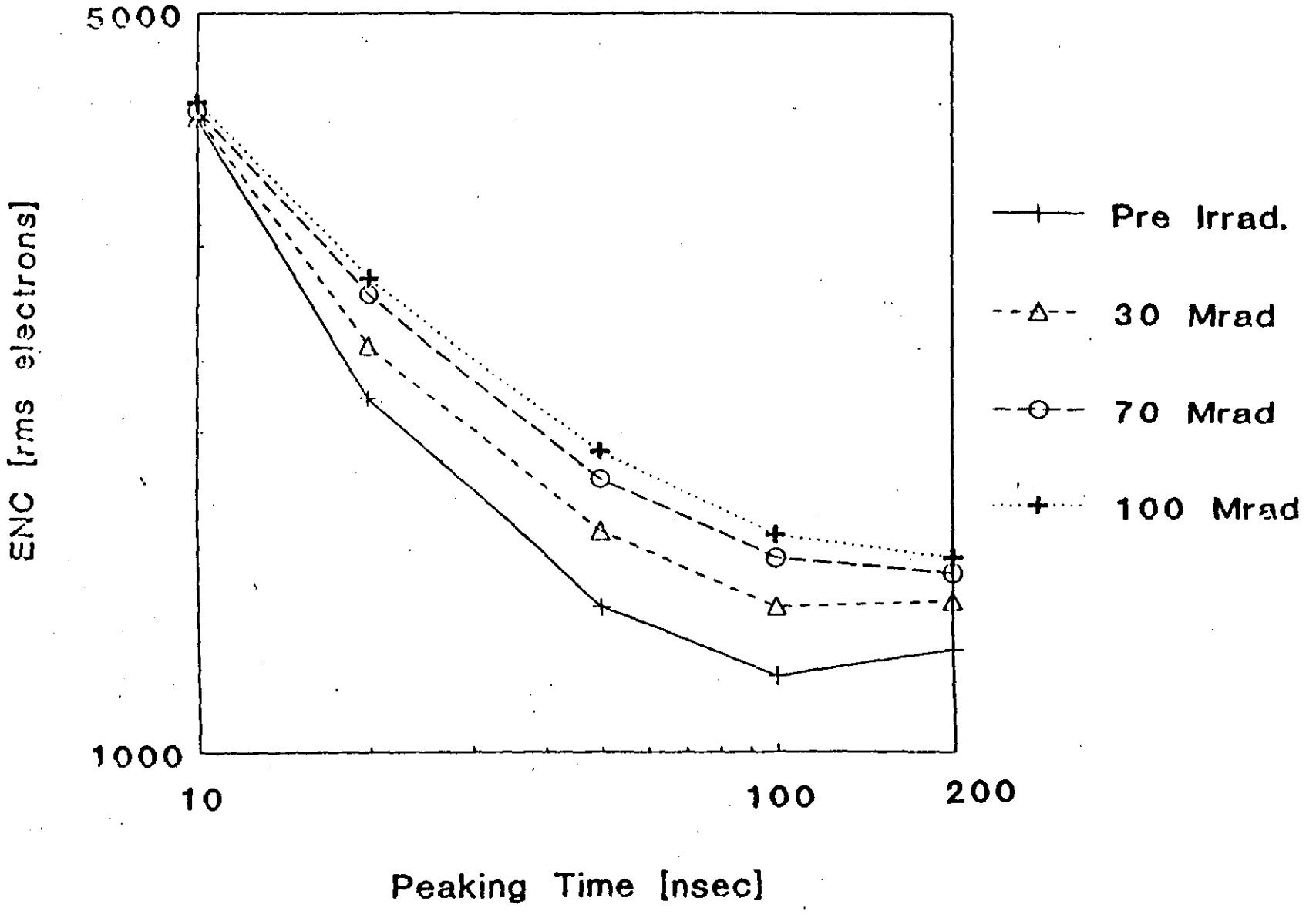
→ Veljko Radeka: presented results of rad'n. studies of FET pre-amps. Noise increases by factor $\lesssim 2$ after 100 MRad. Neutron tolerance also looks quite good.

→ also looking at precise calibration technique ($\lesssim 0.2\%$) using only DC currents + switches.

→ Paul O'Connor: monolithic shapers will have spread in τ_{peak} of $\sim \pm 30\%$. Investigating techniques for electronically tuning τ.

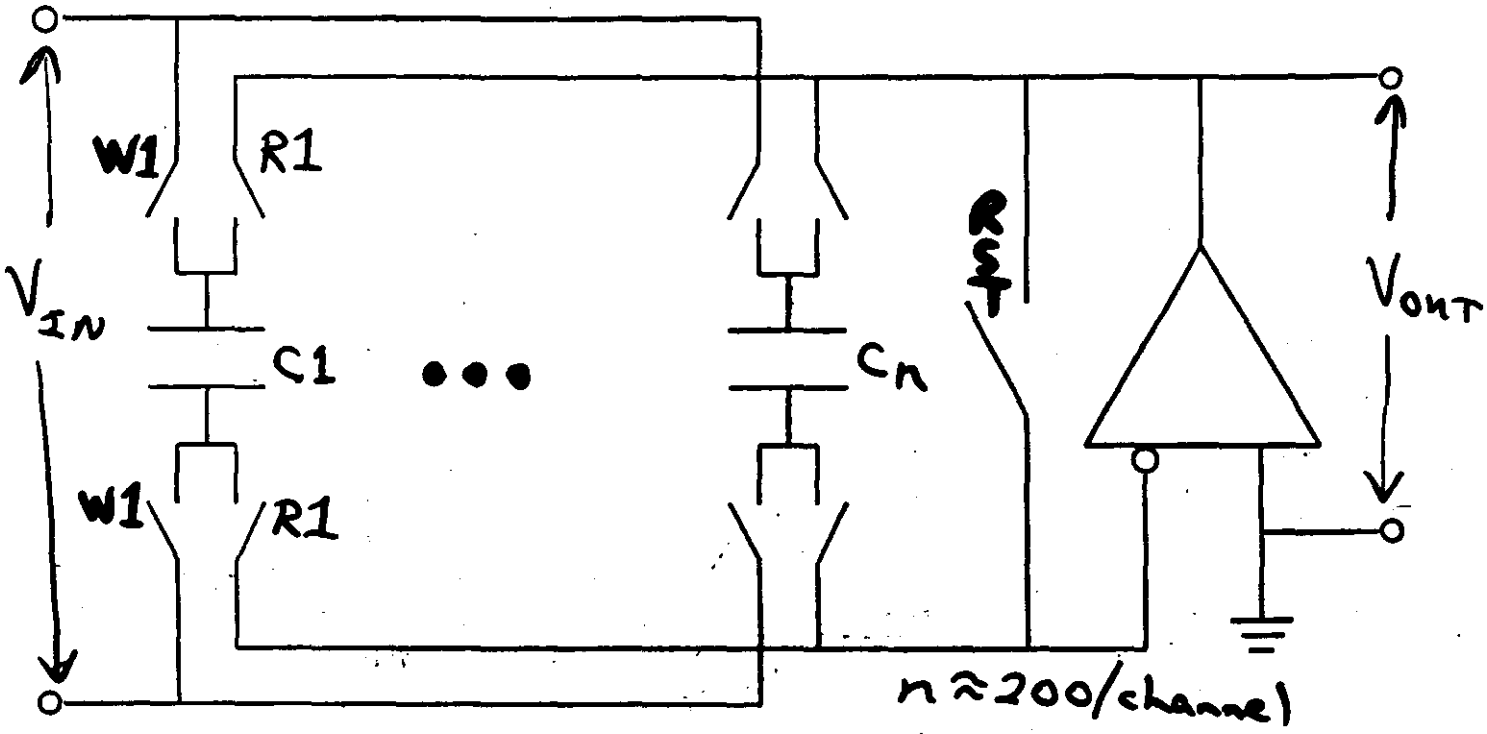
V. RADEKA

Gamma Irradiated Preamplifiers
(powered - warm)



Switched-Capacitor Analog Memory

- sample voltage every 16ns and store in switched-cap. array awaiting L1 decision.



- **deadtimeless** through simultaneous R/W capability + virtual buffer
  - ↳ requires complicated address bookkeeping

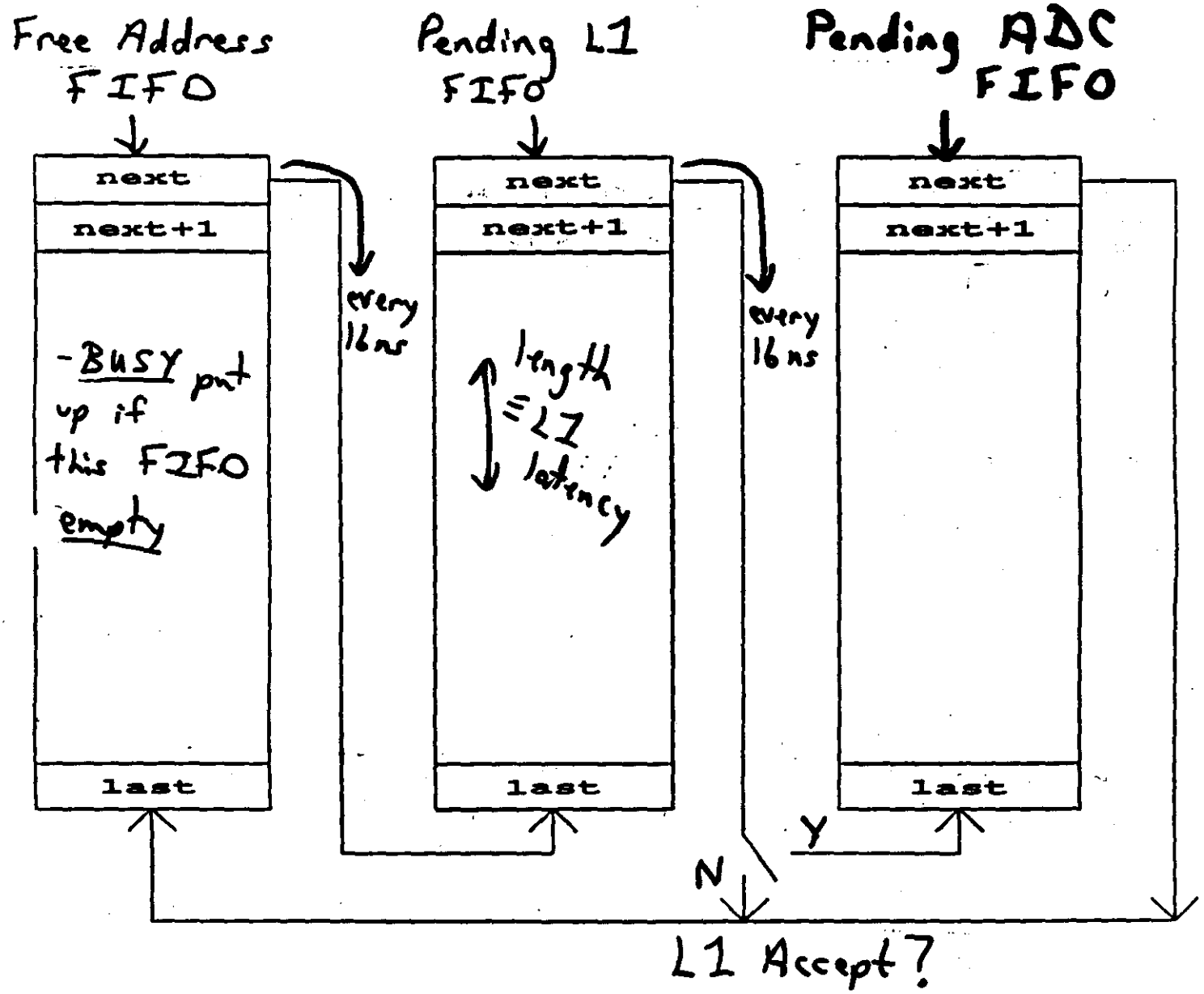
- existence proof provided by LBL.

- can achieve 12-13 bits of dynamic range
  - ↳ need at least 2 gain scales

- may need to correct for cell-to-cell pedestal differences, especially when adding up large number of channels.

Address List Processor (ALP)

- insufficient time to transfer charge to a buffer
  ↳ just transfer address & leave charge (virtual buffer)



- ALP will probably have to be separate chip (put R/W address decoders on SCA)

- are investigating different schemes to minimize fast digital signals which need to be sent to SCA chip, due to worries about noise.

ALTERNATE ADDRESSING SCHEME

GOAL: reduce number of control signals to:

(a) minimize noise introduced into analog measurement due to receiving fast digital signals on same chip,

(b) simplify signal fan-out required to run system ($\sim 10^5$ channels)

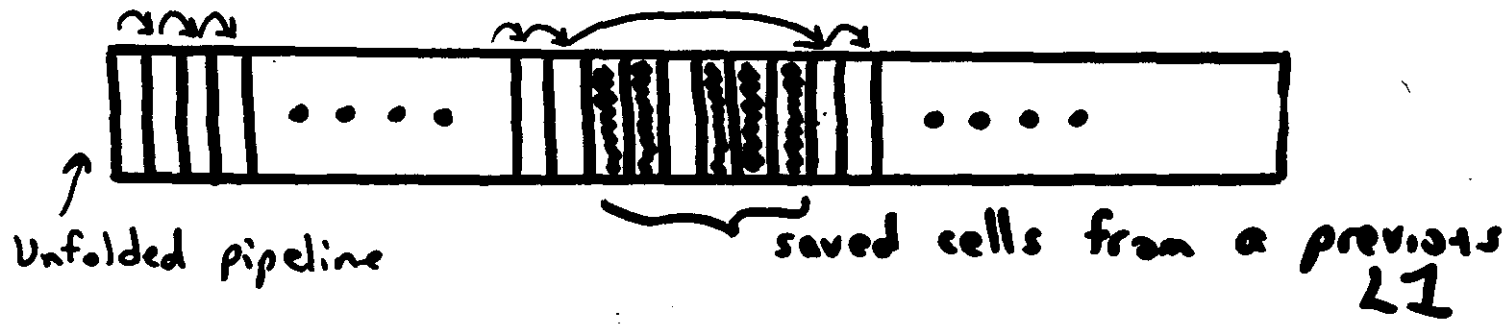
WRITE Address

→ use 3 bits of "Skip Logic":

000 - add 1 to current value of address
001 - add $(n+1)$ " " " " "
010 - add $(2n+1)$ " " " " "
100 - add $(3n+1)$ " " " " "
011 - add $(4n+1)$ " " " " "

101 - Error flag
111 - INIT

$n \equiv$ number of samples reserved for a L1 trigger

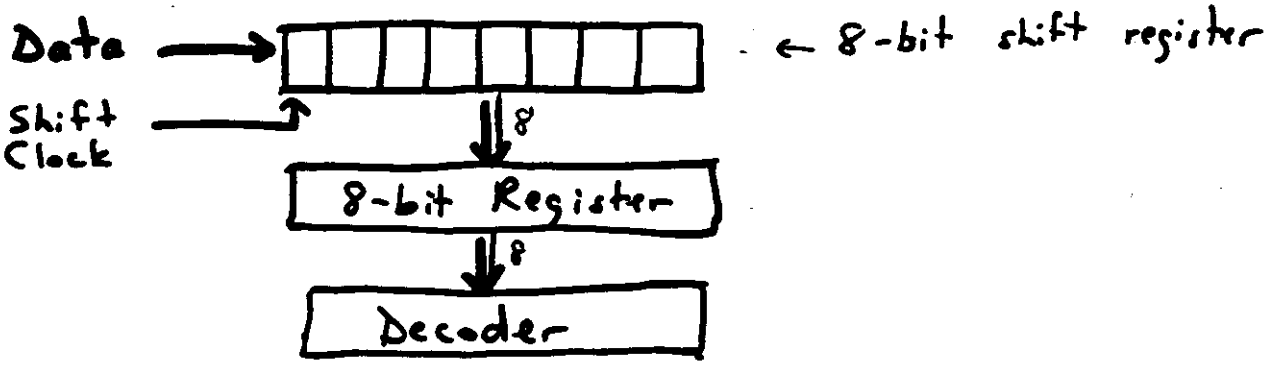


- for $\gg 90\%$ of crossings, "skip" = 000

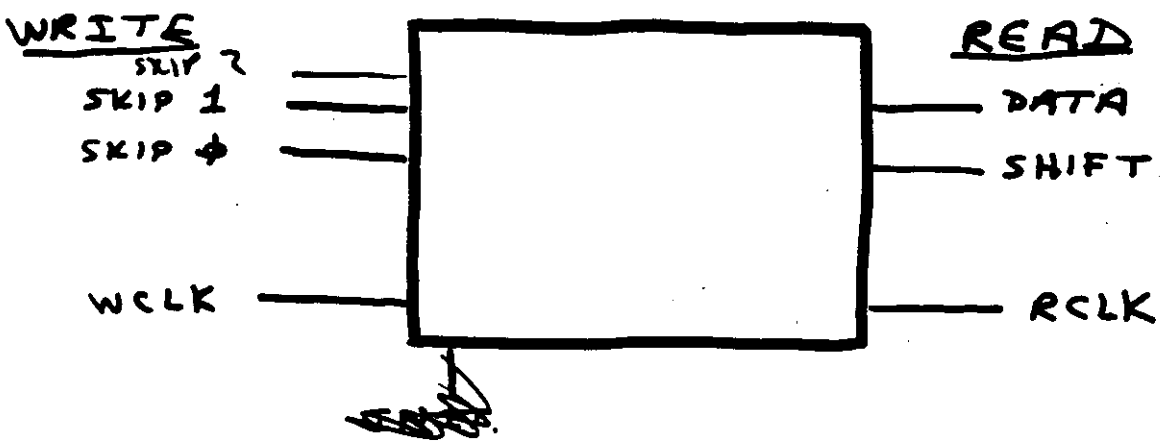
READ Address

→ takes >100 crossings to digitize a single sample.

⇒ lots of time to transfer next Read address bit-serially into a shift register.

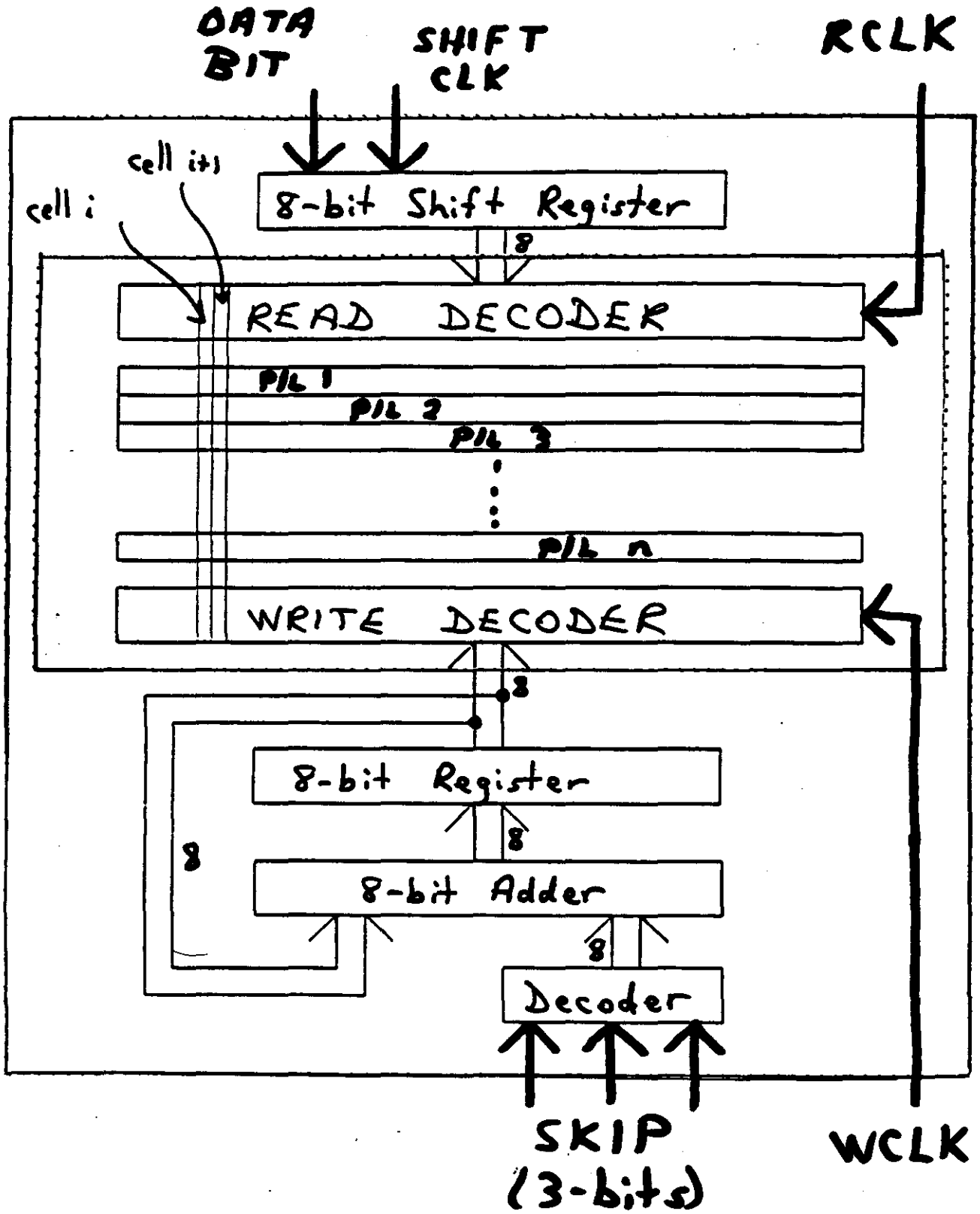


Pipeline Chip Control



→ reduces # of Address lines from 16 (8 for W, 8 for R) to 5.

BLOCK DIAGRAM OF PIPELINE CHIP CONTROL



Test Chip Program

proceed through series of test chips to final design. Orbit Foresight program has 5-6 week turnaround, $1.5 k/"Tiny" chip.

① 4 pipelines, each of 8 cells to:
- study different cell structures,
- look at timing issues (all clocks, n & p, brought off chip)
- look at differential vs. single-ended structure.

→ **submit by end of Feb ⇒ receive mid Apr.**

② 4 pipelines, 48 cells each + DECODER to:
- test decoder
- study noise, ped. variations, etc. as result of addressing

→ **submit mid March ⇒ receive end Apr.**

③ + COMPARATOR + RAMP
- make time over threshold measurement
- start looking at ADC issues.

In parallel, design (using ECL?) and build address bookkeeping logic for generating the WRITE SKIP bits, etc.

March 10th, 1992

D. Crosetto

Programmable

II level Trigger

ARCHITECTURES

SUMMARY

- PARALLEL PROCESSING for II level Trig.
  - Connectivity
  - Bandwidth
  - Computing Capability
- PARALLEL PROCESSING "NODE" DESIGN
- II level Trigger OPTIONS
- PROBLEM DEFINITION
  - Case study of the past
    1 ....
    2 ....
    3 ....
  - Case study for GEM

C. Allen, D. Crosetto, D. Marlow, J. Ritchie

- POSSIBLE SOLUTIONS
  - Examples of architectures studied in the past
  - Present GEM

PARALLEL PROCESSING

Connectivity & Bandwidth

Serial (easy)

Parrallel (fast)

Computing capability

chipest & most efficent processor

($6/Mflop)

Problem:

TO DESIGN

AN ARCHITECTURE

- Programmable
- Flexible
- Fast
- Simple & easy to use
- Economical

That will give the possibility to implement most of the "OPTIONS" for a II level Trigger.

ONE ARCHITECTURE is DESCRIBED and as examples a few CASE STUDY for II level Trigger will be considered.

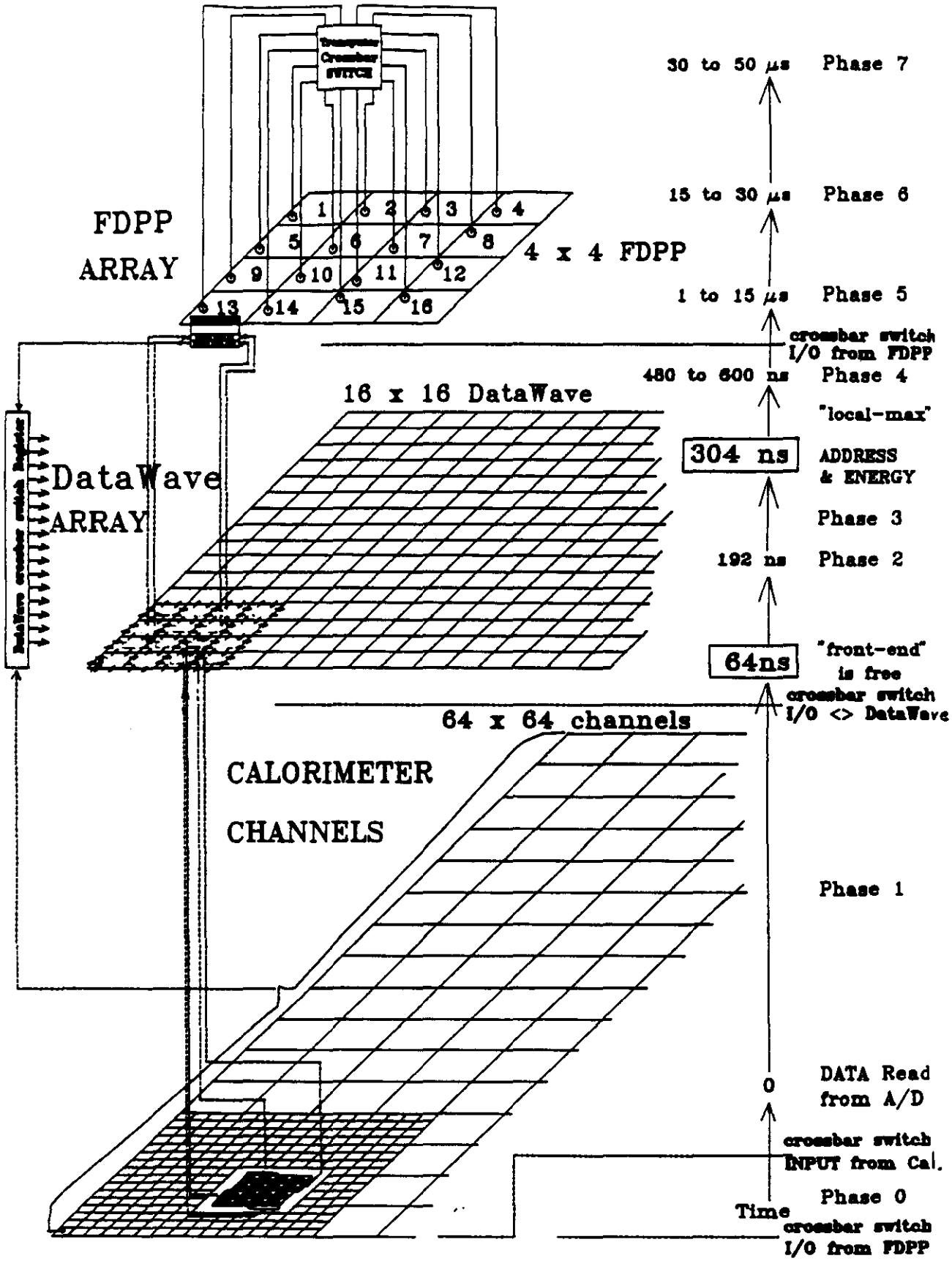
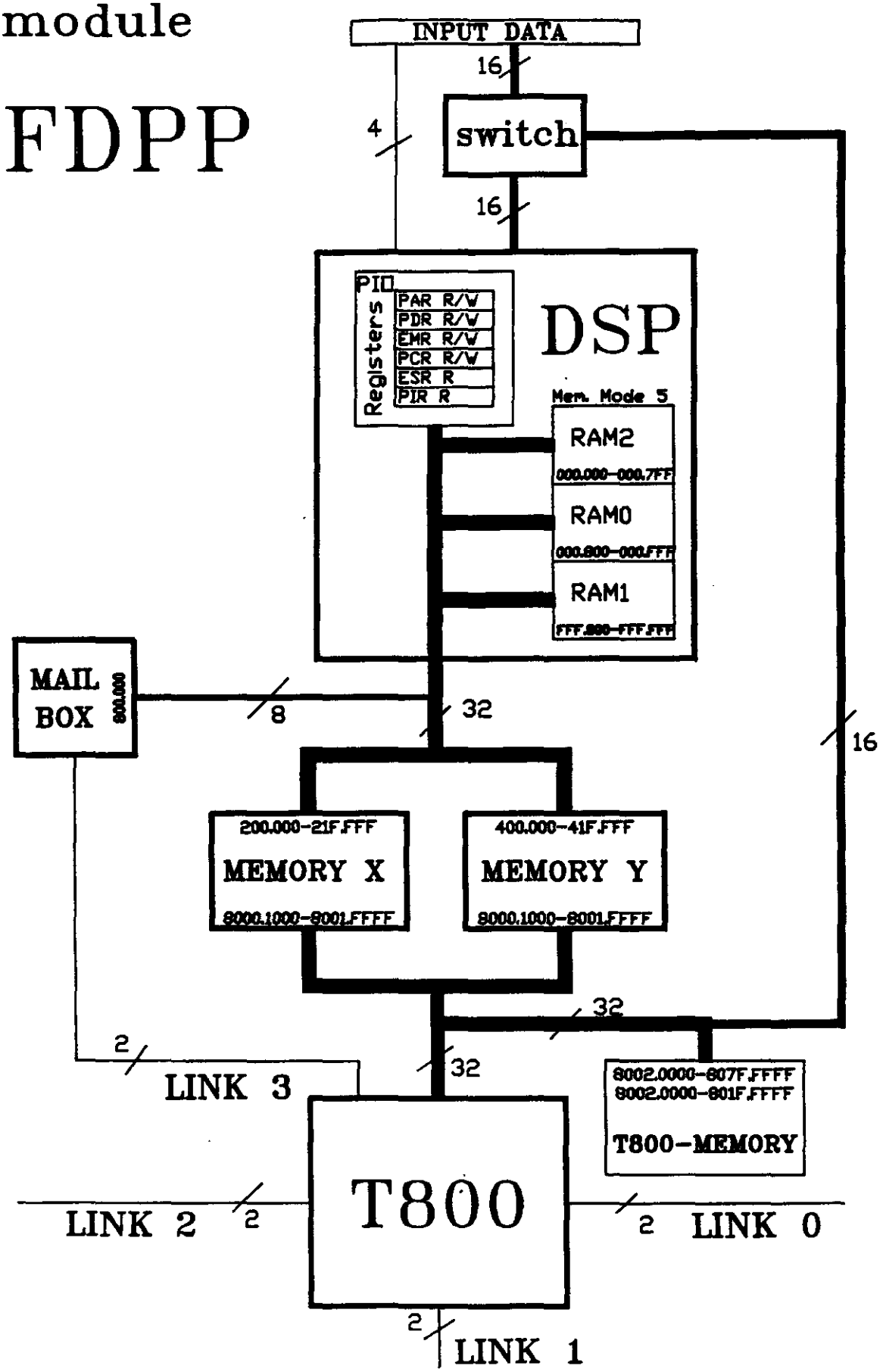


Fig. 1 Fast cluster finding system block diagram. Proceeding from bottom to top, one sees the mapping of calorimeter channels to DataWave processing elements (PE) followed by the mapping of 256 PE's to on FDPP. On the right the data acquisition and reduction phases (described in the text) are aligned in order from bottom to top along with the time duration estimates.

Fast Digital Parallel Processing module

FDPP



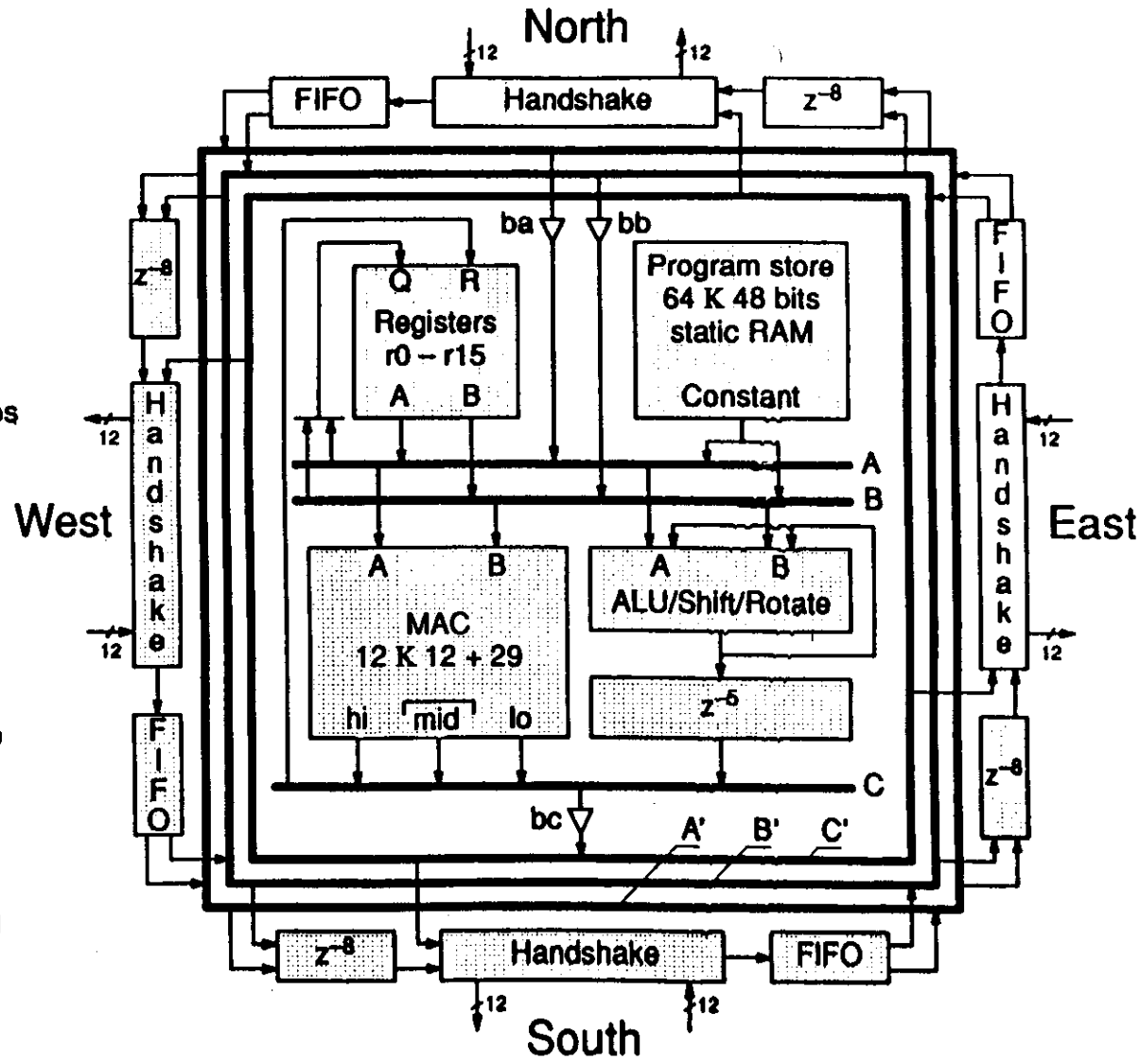
DAVIS Cell Architecture

Architecture

- 125 MHz (8 ns)
- Multiply-Accumulate in every cycle
- 3 ring buses, 3 core buses
- 3 kbits program store (static RAM)
- Four-port register file, 16 registers
- Deep pipeline with short feed-back loops
- 12-bit ALU, 1 cycle delay
- n 1-bit shifts/rotates in n cycles

Intercell Communication

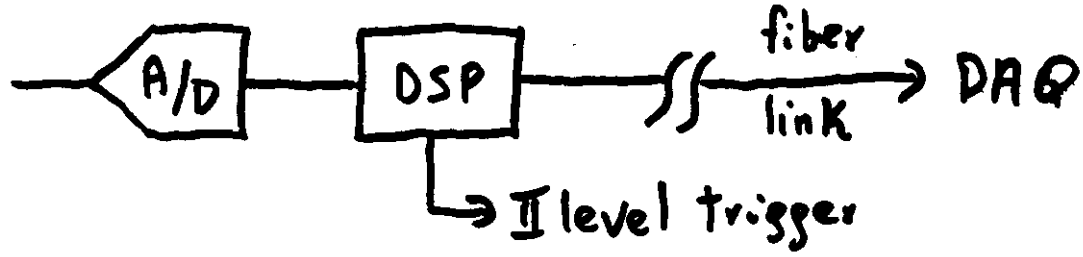
- Up to 6 cell-to-cell transfers every cycle
- Self-timed handshake with FIFOs
- Dual-port circular buffers (8 words)
- Automatic pipeline freeze when waiting



II level Trigger OPTIONS

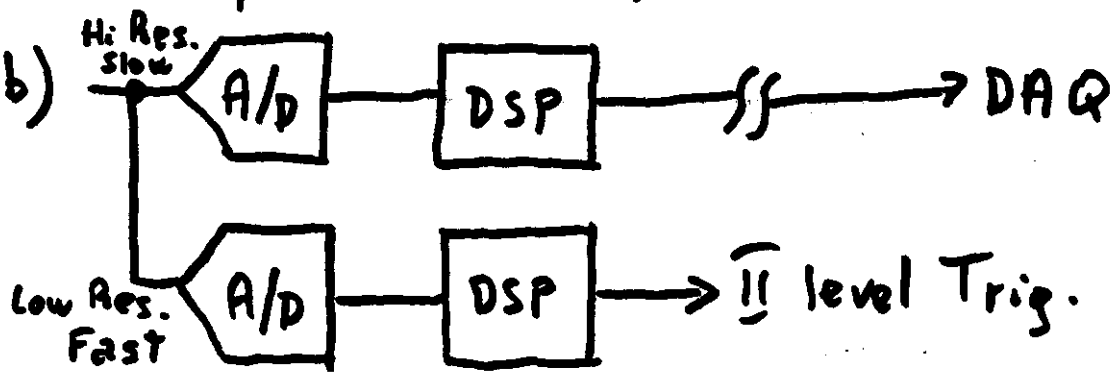
1) Should we have only one electronic chain for DAQ & II level trigger ?

a)



or two separate chains ?

b)



2) Should we have full granularity

a) executing II level trig. on all channels ?

b) or zoom in a particular region ?

3) How many channels do we assign to a processor ~~of~~ the first level trigger

4) How many channels do we assign to a processor of the II level trigger?

5) Should we have more than one sample for each "signal-element" and filter digitally?

6) The filter algorithm, should it be:
   a) on the detector-electronic
   b) or on the II level trigger DSP?

7) Should we have the possibility to exclude the II level trigger algorithm execution?
   (no zero suppression)

8) Should we have no dead-time?

9) Which input frequency should we sustain?
   a) continuously .....?
   b) with intervals ...., ...?

10) How many clusters do we expect (from a Monte Carlo simulation) from the II level Trig. ?

11) For which latency ?

12) How large should be ?

a) the input buffer

b) the output buffer

c) event size

13) No-boundary limitation in the array should be realized with:

a) high bandwidth communication between proc

b) with overlapping areas ?

14) How is coupled with the first level Trig. ? or do we need from Ist level Trig.

a) isolation ?

b) shower-max ?

c) do we use single tower energy threshold for Jet Trigger ?

15) Do we need a large number of array processors in a pipeline mode (e.g. Data Wave) to calculate the above in real-time during the 1st level trigger ?

16) Do we use a small number of array processor not in pipeline mode (e.g. Data Wave) just in order to give the information of the region of interest from the first to the second level trigger. ?

17) Do we need a "Parallel Processing System" for the second level trigger capable to implement all the below II level trigger algorithms, or do we need only part of them ?

II level Trigger Algorithms:

1) $I/C = \left(\frac{1}{8} \sum_{i=1}^{8} I \Big/ C \right)$ exec time $(5\mu s)$

2) $O/C = \left(\frac{1}{16} \frac{\sum_{i=1}^{16} D}{C} \right)$ exec time $(5\mu s)$

3) $E = C + \sum_{i=1}^{8} I + \sum_{i=1}^{16} O$ exec. time $(5\mu s)$

(no wig.)

4) $R_p = \dfrac{\sum_{i=1}^{25} r_i E_i^{0.4}}{\sum_{i=1}^{25} E_i^{0.4}}$ exec. time $(15\mu s)$

(GEM)

5) $\dfrac{\sum_{3\times3} E}{\sum_{5\times5} E} > .9$ exec time $(\ ?\ )$

6) (Ed) for electron

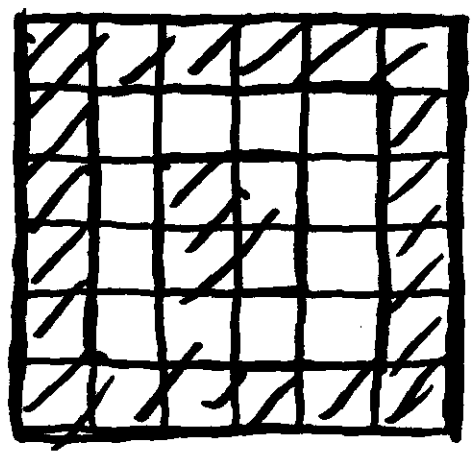
$$\frac{\sum_{20} E_m + Had_{16}}{\sum_{4} E_m} < .2$$

exec time (?)

7) (Ed) for jet

$$\sum_{20} Em + Had > 100 \text{ Gev}$$

exec time (?)



Typical problems of Digital triggers & Data acquisition/compaction in Calorimetry of High Energy Physics.

For any number of channels:

1. Calculate the total energy and the transverse energy

2. Calculate the geographical address of clusters (local maxima).

3. Apply a threshold to the combined energy of a local maxima and of its neighbors.

4. Isolate from the empty calorimeter channels:
   - the clusters found along with their regions of interest and
   - calculate their cluster shape-factors (e.g. to separate pions/electrons).

PROBLEM DEFINITION:

CASE STUDY 1

Options for the Ist level trigger:

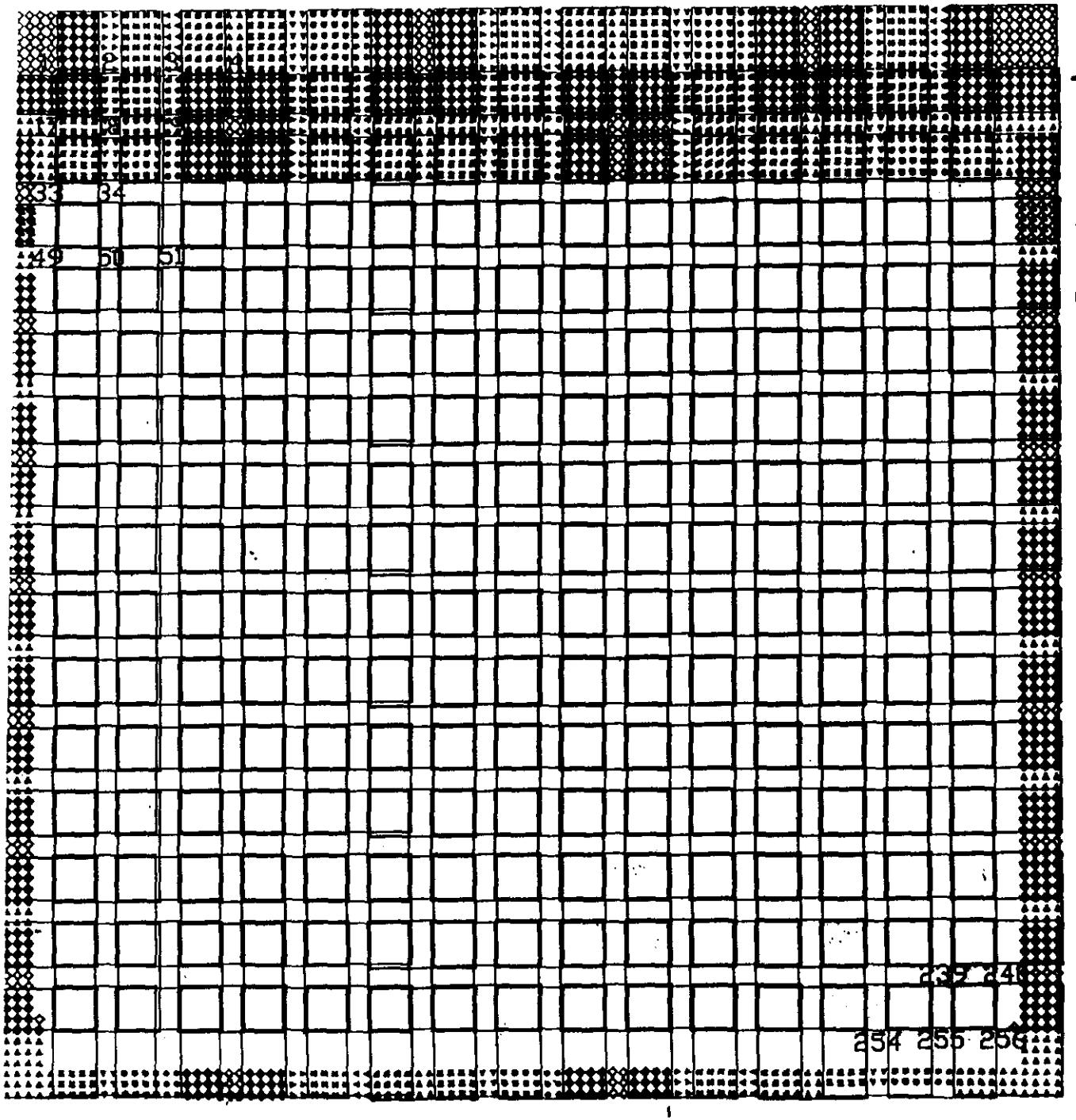
16) no processors at I level

Options for the II level trigger:

1 a) DAQ ≡ II lev. Trig.
2 a) full granularity
4) 1 FDPP = 100 channels
13 b) with ovelapping areas
12 a, b 128 Kbyte (input/output buffer)

POSSIBLE SOLUTION:

e.g. Calorimeter 10,000 Channels



256 x FDPP modules

for HEP real time algorithms

FDPP architecture for an array of 100x100 channels

Each FDPP module analyse 36 channels out of 100 data-in

GENERIC PEAKFINDING

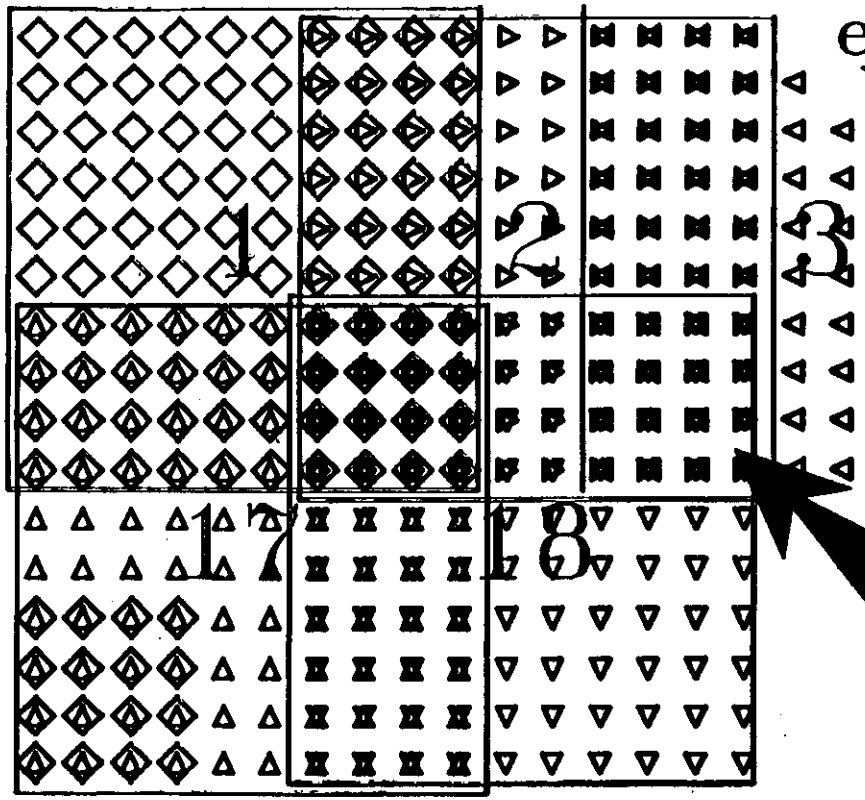
```
  O
 O I O
O I C I O
 O I O
  O
```

All peaks are found in μsec ~55

CLUSTER-ANALYSIS

SIMPLE JET/ELECTRON FINDER

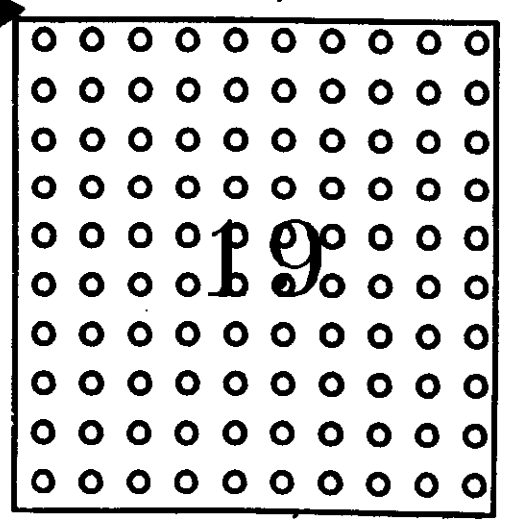
```
O O O O O
O I I I O
O I C I O
O I I I O
O O O O O
```



each FDPP scans

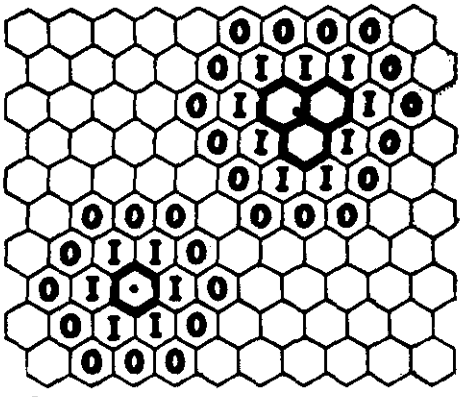
100 channels and find clusters

in 42–48 μsec



Algorithm 3

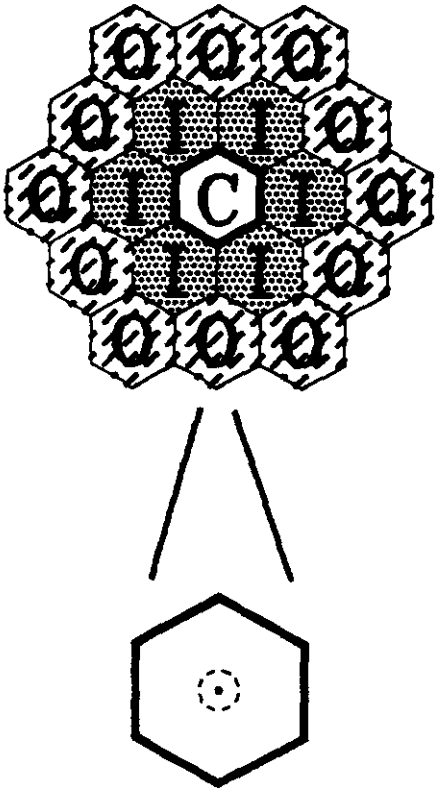
each FDPP



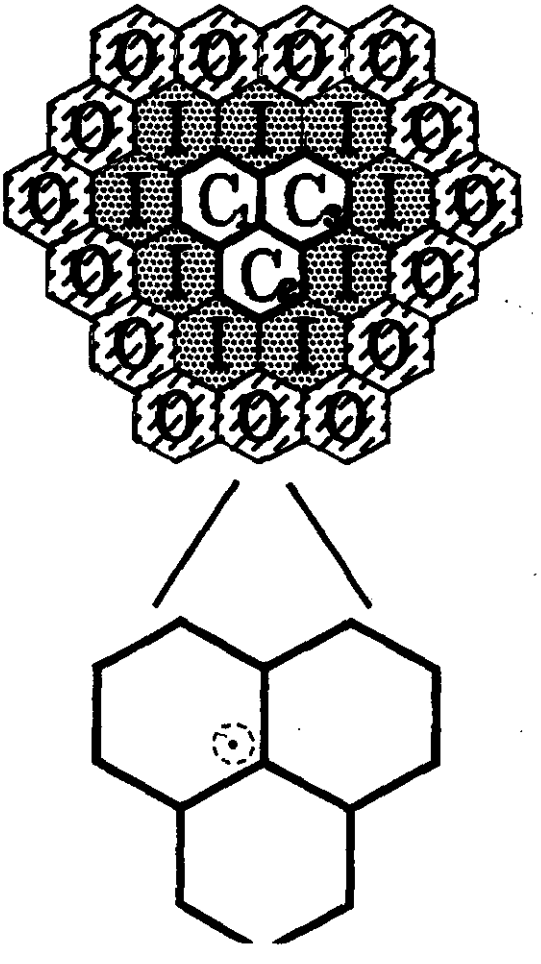
- scans 100 channels
- finds type of hit
- finds local maximum
- calculate E, I/C, O/C for different type of hit

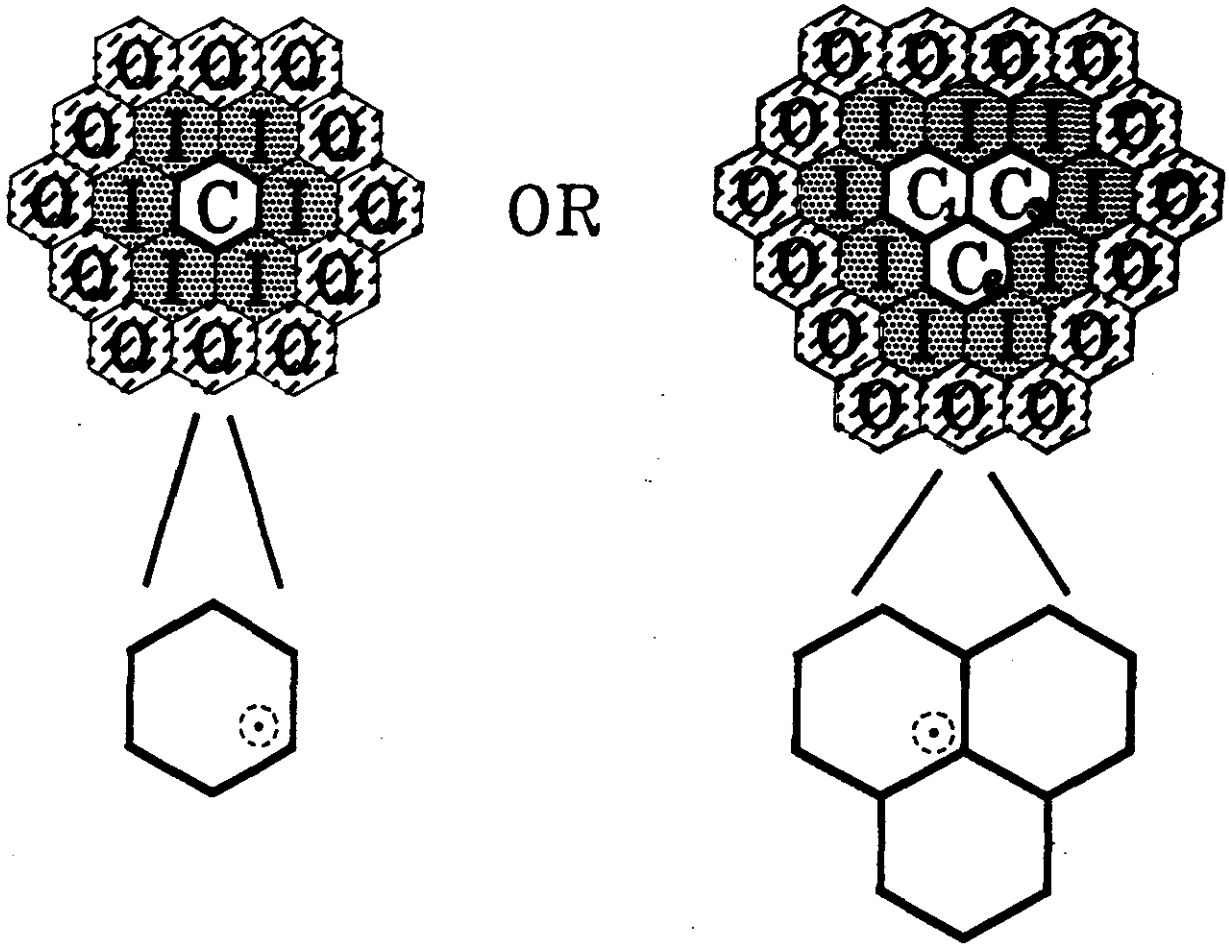
in 62 μsec

(electron events)



OR





$$C = C_1 + C_2 + C_3$$

$$E_1 = C + \sum_{i=1}^{6} I + \sum_{i=1}^{12} O \qquad E_2 = C_1 + C_2 + C_3 + \sum_{i=1}^{9} I + \sum_{i=1}^{15} O$$

$$(I/C)_1 = (1/6 \sum_{i=1}^{6} I)/C \qquad (I/C)_2 = (1/9 \sum_{i=1}^{9} I)/C$$

$$(O/C)_1 = (1/12 \sum_{i=1}^{12} O)/C \qquad (O/C)_2 = (1/15 \sum_{i=1}^{15} O)/C$$

The same event N.32 from RUN 22531 on SPACAL (1990)

$E_1 = 27.25$ Gev	$E_2 = 28.25$ Gev
$(I/C)_1 = 0.1667$	$(I/C)_2 = 0.2874$
$(O/C)_1 = 0.1544$	$(O/C)_2 = 0.0977$

PROBLEM DEFINITION:

CASE STUDY 2

Options for the I level trigger

3) 34 channel to 1 processor (one tower)
16) send Region of Interest Info to II level trig.

Options for the II level trigger

1 a) DAQ ≡ II level trig.
2 b) zoom in a partic. region
4) 49 channel to 1 processor FDPP
6a) filter on detector
7) yes (ON/OFF zero suppr.)
12 a,b 128 Kbyte (input/output buffer)
13b) overlapping areas

POSSIBLE SOLUTION

↳

1. MIMD PARALLEL HYBRID SYSTEM

used for:

- distributing processes over several processors

- concentrating the processing power in the region of the detector where there are some interesting data.

2. DATA FLOW BASED

used in:

(a) CALORIMETER
- fast data correlation

(b) TRACKING DETECTORS
- should be possible to reconstruct tracks using the data flow principle:

Processing Elements execute programs when the input data is available.

FDPP + DATAWAVE system

gives the possibility to realize a

FLEXIBLE ARCHITECTURE

1. MIMD PARALLEL HYBRID SYSTEM

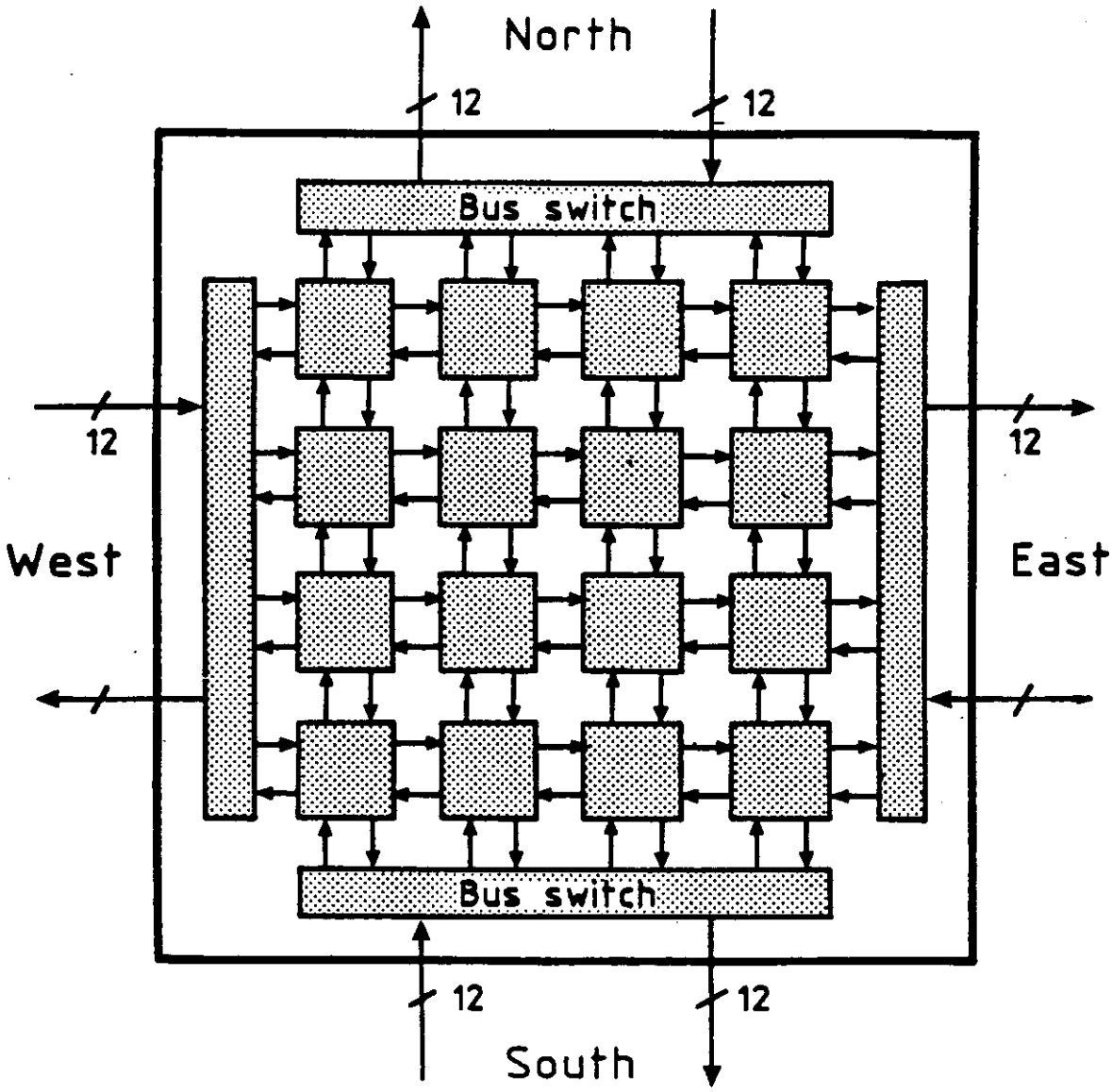
(loosely coupled but with both serial and parallel exchange)
on the higher level array processor
(DSP + Transputers)

- with the possibility to change dynamically the topology of the system (e.g. from a tree structure to a mesh structure)
- with 1.2 Mbyte/s serial links
- with parallel channels of up to 150 Mbyte/s

2. DATA FLOW BASED

on the lower level array processor (DataWave)

- with 750 Mbyte/s maximum transfer rate between chips.


North
12
12
Bus switch
12
West
12
East
Bus switch
12
12
South

DataWave chips

The one described in the magazine Elektronik 12/june 8, 1990 has:

- 16 identical PEs(in program also with one and 64 PEs)

- individually programmable

- working on the data flow principle and organized in a matrix form

each PE is a RISC processor with 12-bit architecture which operates on the pipeline principle

each PE communicate with their four nearest neighbors via asynchronous parallel buses

each PE can have a maximum program length of 64 words of 48-bits each.

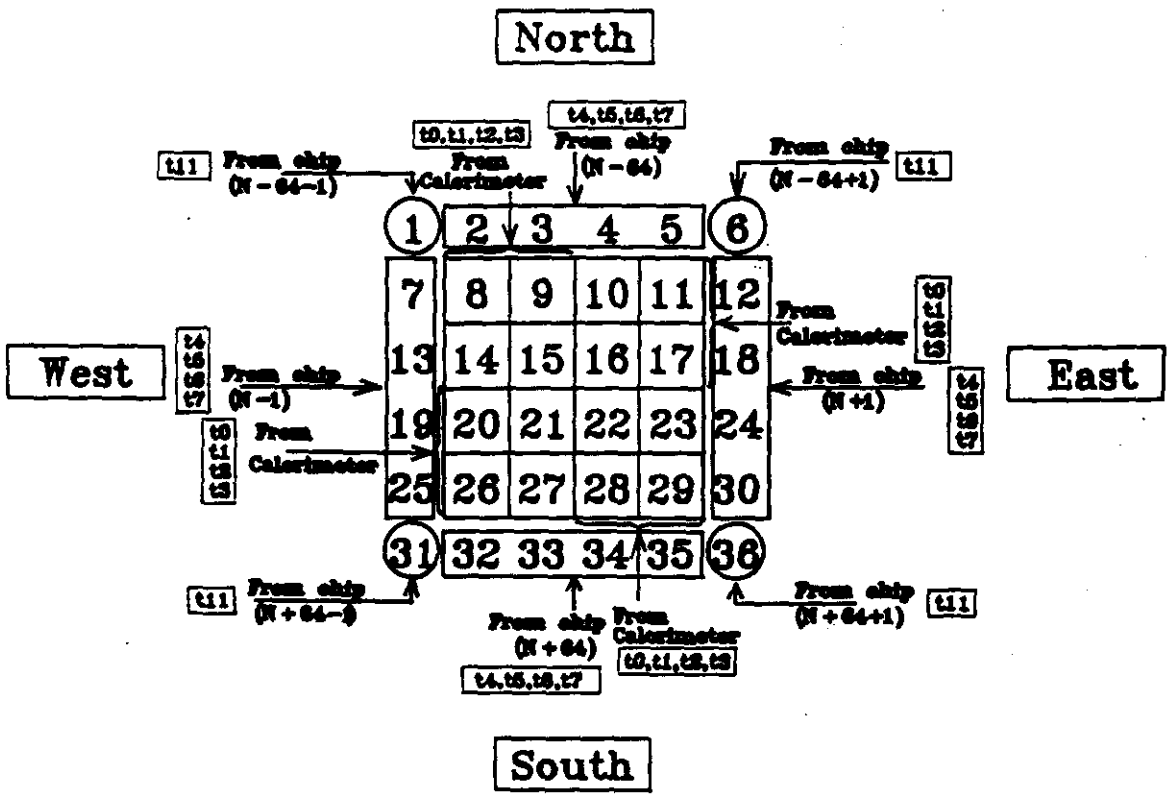
A "local maximum" is a channel value greater than or equal to its neighbors

I	I	I
I	C	I
I	I	I

$$E = \sum_{i=1}^{8} I_i + C$$

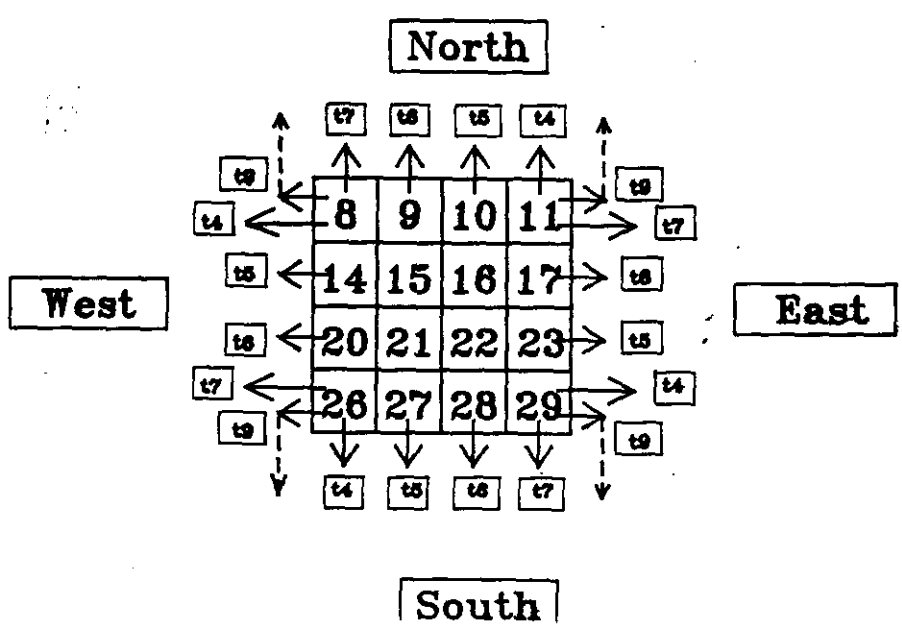
Each DataWave receives DATA from:

- the Calorimeter (A/D converters)
- and from neighboring DataWave chips



Each DataWave sends DATA to:

- neighboring DataWave processors



$E_{TOT} = \sum c_i E_i$ $\qquad$ $E_{\perp} = \sum c_i E_i \cos\theta_i$

DataWave program to transfer input data into PE

```
/* START LOADING FROM READOUT ELECTRONIC */
    t0      alu=alu+n*r11,     e=s=r9=n
    t1      alu=alu+n*r12,     e=s=r8=n
    t2      alu=alu+n*r13,     e=s=r5=n
    t3      alu=alu+n*r14,     e=s=r6=n
/* END LOADING FROM READOUT ELECTRONIC */
```

DataWave program to exchange data with neighboring PE

```
/* START TO EXCHANGE DATA WITH NEIGHBORING PE
    t4      r2=n,              w=r5
    t5      acc=r8+r9
    t6      r3=e,              acc=acc+r5
    t7      s=r4=w,            n=r5
    t8      acc=acc+r3
    t9      w=r5,              acc=acc+r6
    t10     n=w,               r7=s
    t11     r1=n,              acc=acc+r2
    t12     acc=acc+r4,        s=alu
/* END OF DATA EXCHANGE WITH NEIGHBORING PE *
```

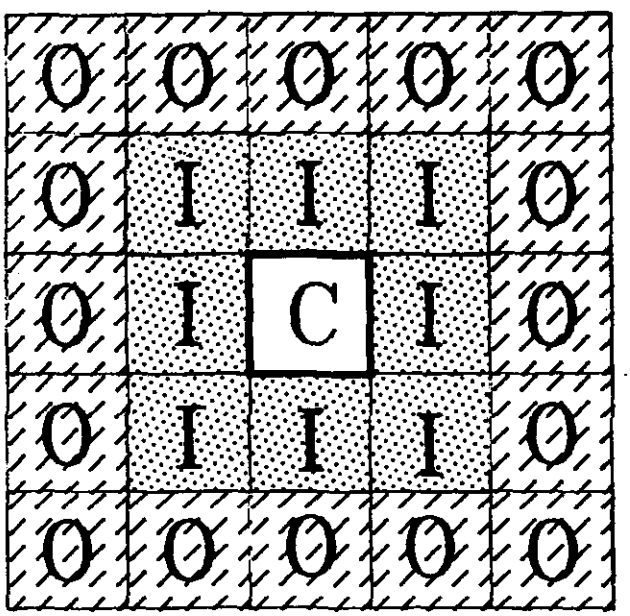
Algorithm 1

each FDPP for the II level trigger

– calculates E, I/C, O/C (in floating point)

SHAPE FACTORS

in 15 μs



$$E = C + \sum_{i=1}^{8} I_i + \sum_{i=1}^{16} O_i$$

5 μs

$$I/C = (1/8 \sum_{i=1}^{8} I_i)/C$$

5 μs

$$O/C = (1/16 \sum_{i=1}^{16} O_i)/C$$

5 μs

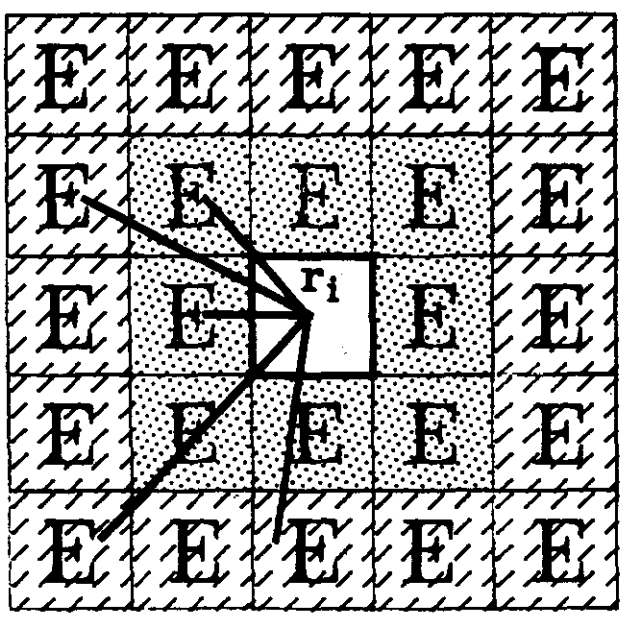
OR

Algorithm 2

each FDPP for the II level trigger

– calculates Rp (in floating point)

in 15 μs



$$Rp = \frac{\sum_{i=1}^{25} r_i E_i^{0.4}}{\sum_{i=1}^{25} E_i^{0.4}}$$

PROBLEM DEFINITION

CASE STUDY 3

Options for the I level trigger

3) 34 channels to 1 processor (1 tower)

15) isolate cluster at I level, give ROI to II

Options for the II level trigger

1 a) DAQ ≡ II level trig.

2 b) zoom in a partic. reagion

4) 49 channels to 1 processor FDPP

6a) filter on detector

7) yes (ON/OFF zero suppr.)

12 a, b 128 Kbyte (input/output buffer)

13 b) overlapping areas

SOLUTION as Case 2 more precise informations from the I level trig. assuming to use a Pipeline array of Data Wave with cycle of 4ns

PROBLEM DEFINITION:

Case study 4

Options for the I level trigger

16) no processor array

Options for the second level trigger

1a) DAQ ≡ II level trig.
2a) algorithm on all channels
4) 1000 channels to 1 processor (FDPP)
6a) filter on detector
7) yes (ON/OFF zero suppression)
12 a,b 128 Kbyte (Input/Output Buffer)
9 a) 10 KHz input rate
8) no dead-time

POSSIBLE SOLUTION

↳

Example of a DAQ for 60,000 channel Calorimeter

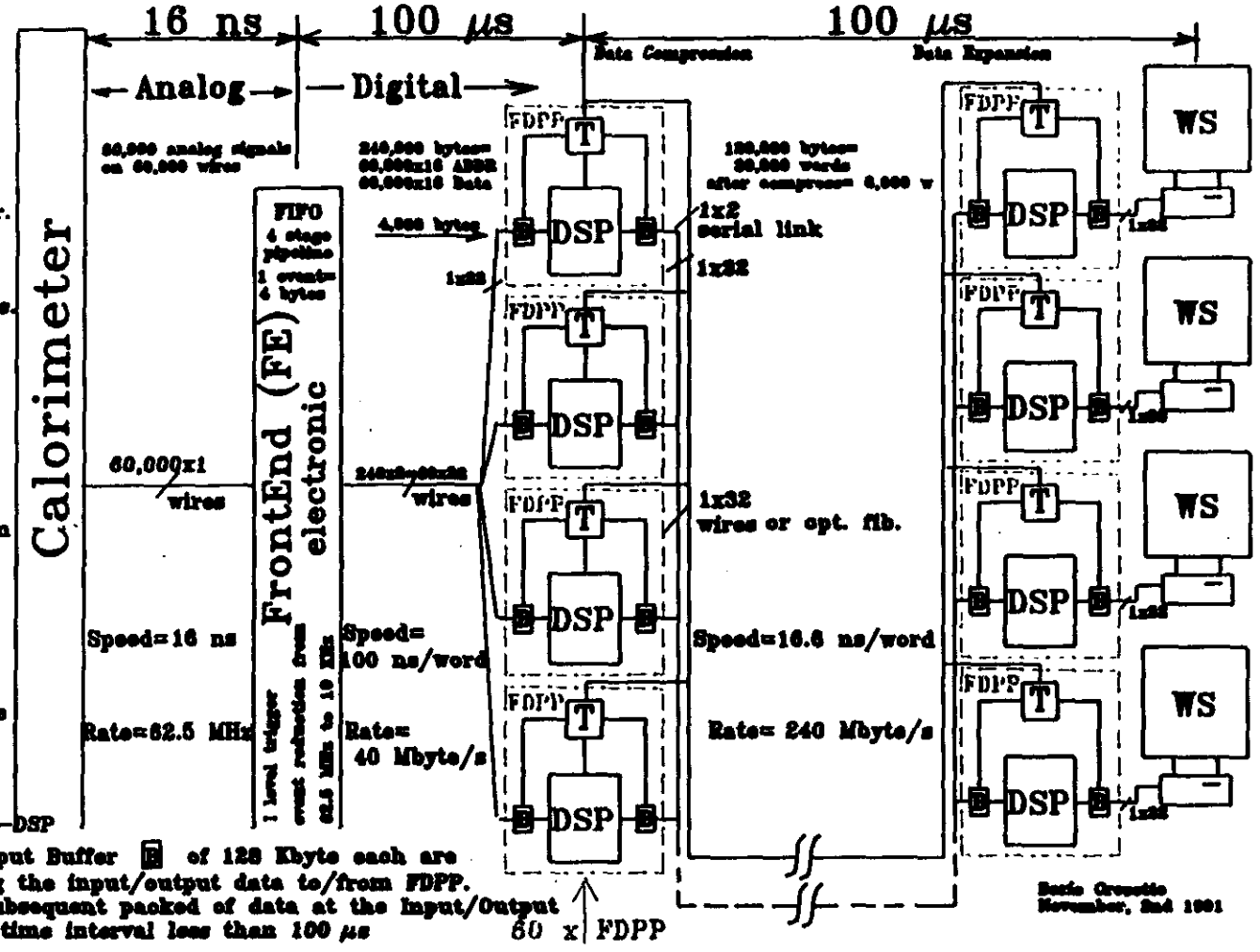
with II level trigger of 10 KHz, no zero suppression and with no dead-time

DSP tasks:

- pedestal subtraction
- calibr. cost.
- suppress addr. & generate lookup-table
- data compress.

T=TRANSPUTER

- data transfer controller
- supervisor & monitoring of the system
- generate the correct seq. among the ACQ-DSP and WS-DSP in order to collect in one WS-DSP all data of an event from different ACQ-DSP



- An Input/Output Buffer ▣ of 128 Kbyte each are derandomizing the input/output data to/from FDPP. This allows subsequent packed of data at the Input/Output to occure at time interval less than 100 μs

Boris Crosetto
November, 2nd 1991

PROBLEM DEFINITION:

Case study 5

Options for I level trigger

3) 34 channels to 1 processor (1 tower)

16) small number of processors

Options for II level trigger

1 a) DAQ ≡ II level trig.

2 a) on all channels

4) 25 channels to 1 processor (FDPP)

5) yes, 5 samples

6 a) → 9 a) filter on detector, rate: 50 kHz

6 b) → 9 a) filter on II level trig. DSP, rate: 20 kHz

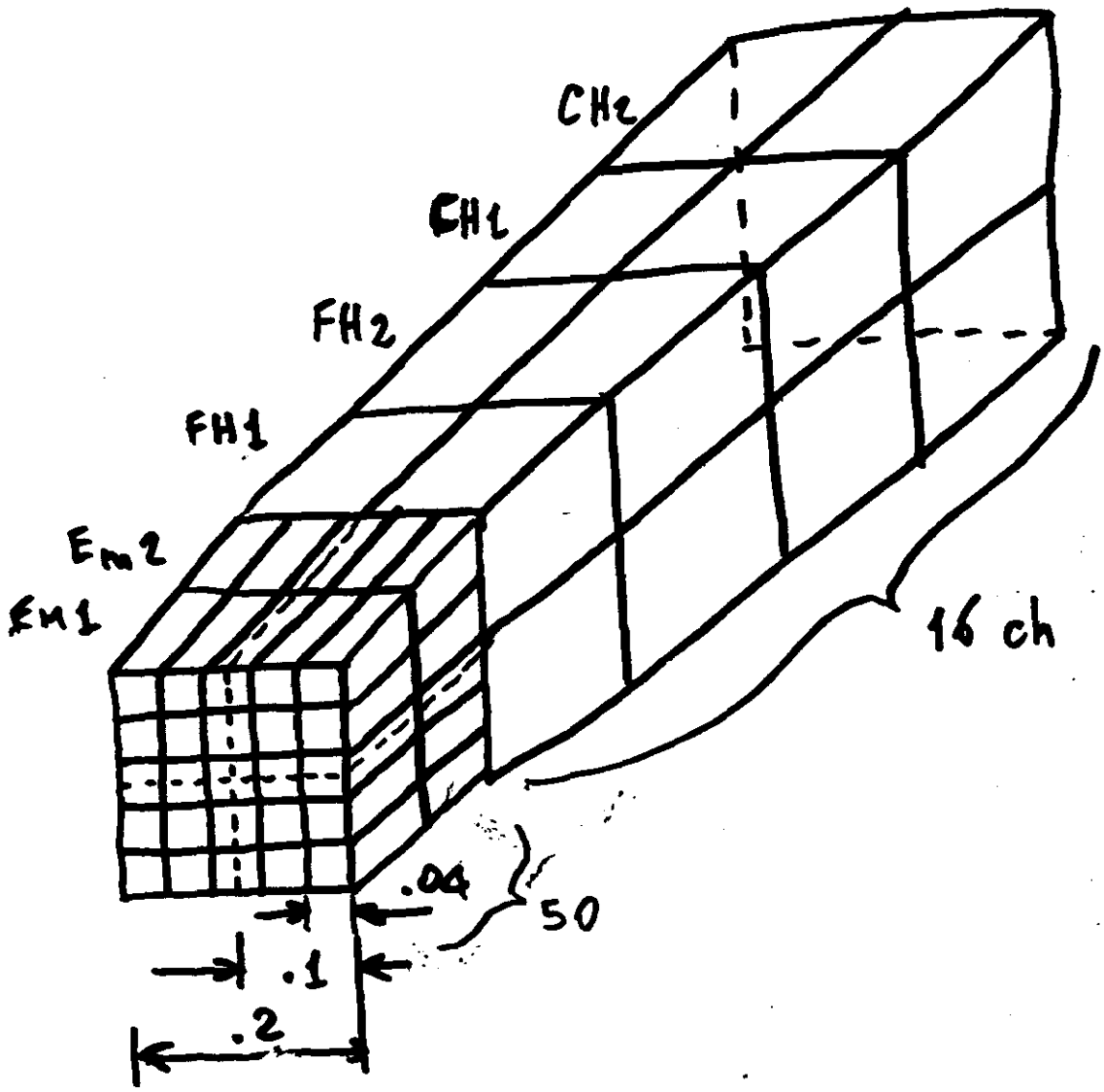
12 a,b 128 Kbyte (input/output buffer)

POSSIBLE SOLUTION

→

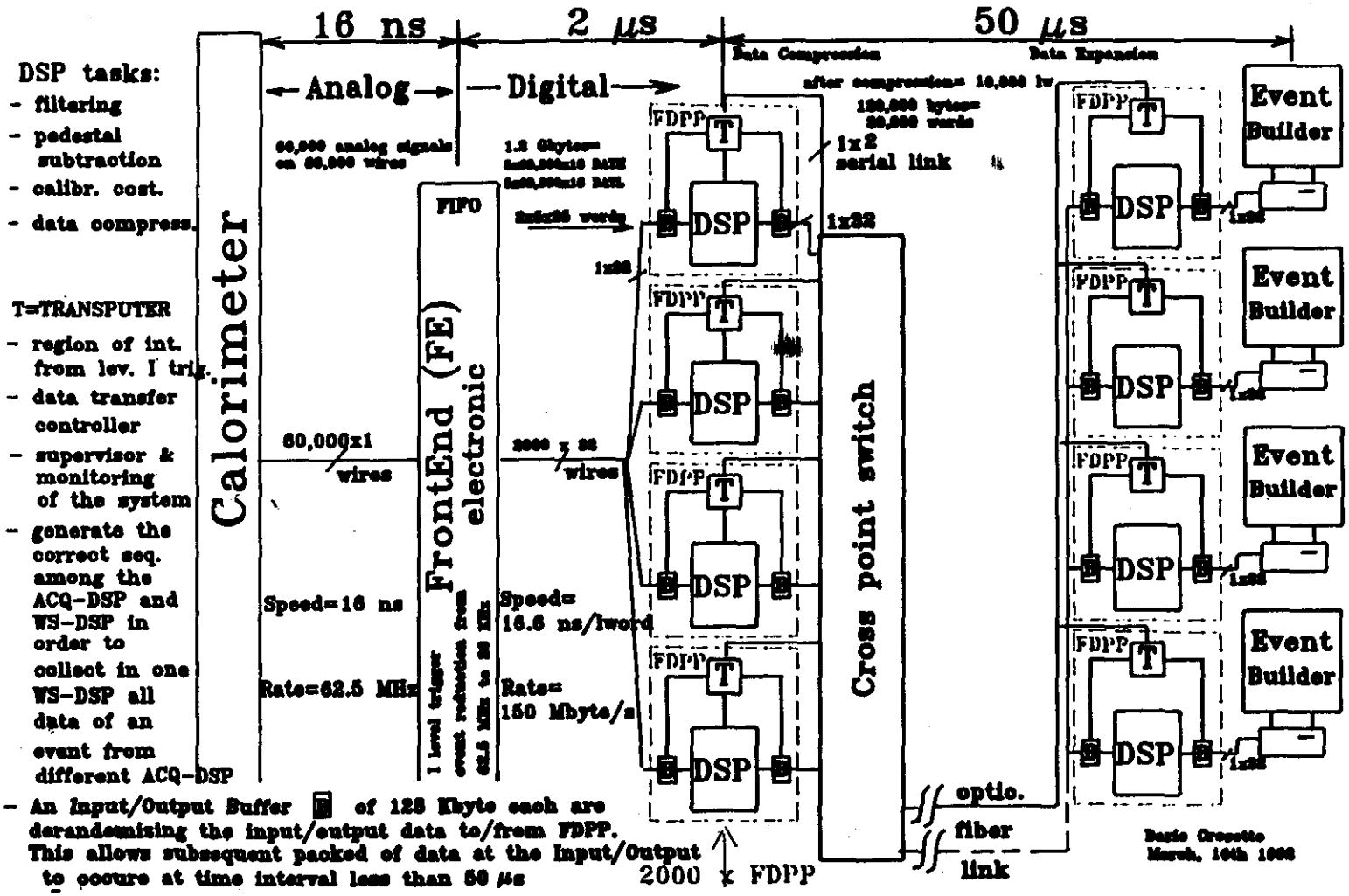
GEM Calorimeter

542 towers



Example of a DAQ for 60,000 channel Calorimeter

with II level trigger of 20 KHz, on/off zero suppression select, no dead-time



ith II level trigger of 20 KHz, on/off zero suppression select, no dead-time

SP tasks:
filtering
pedestal
subtraction
alibr. cost.
lata compress.

TRANSPUTER
egion of int.
rom lev. I trig.
lata transfer
ontroller
upervisor &
monitoring
of the system
enerate the
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ACQ-DSP and
VS-DSP in
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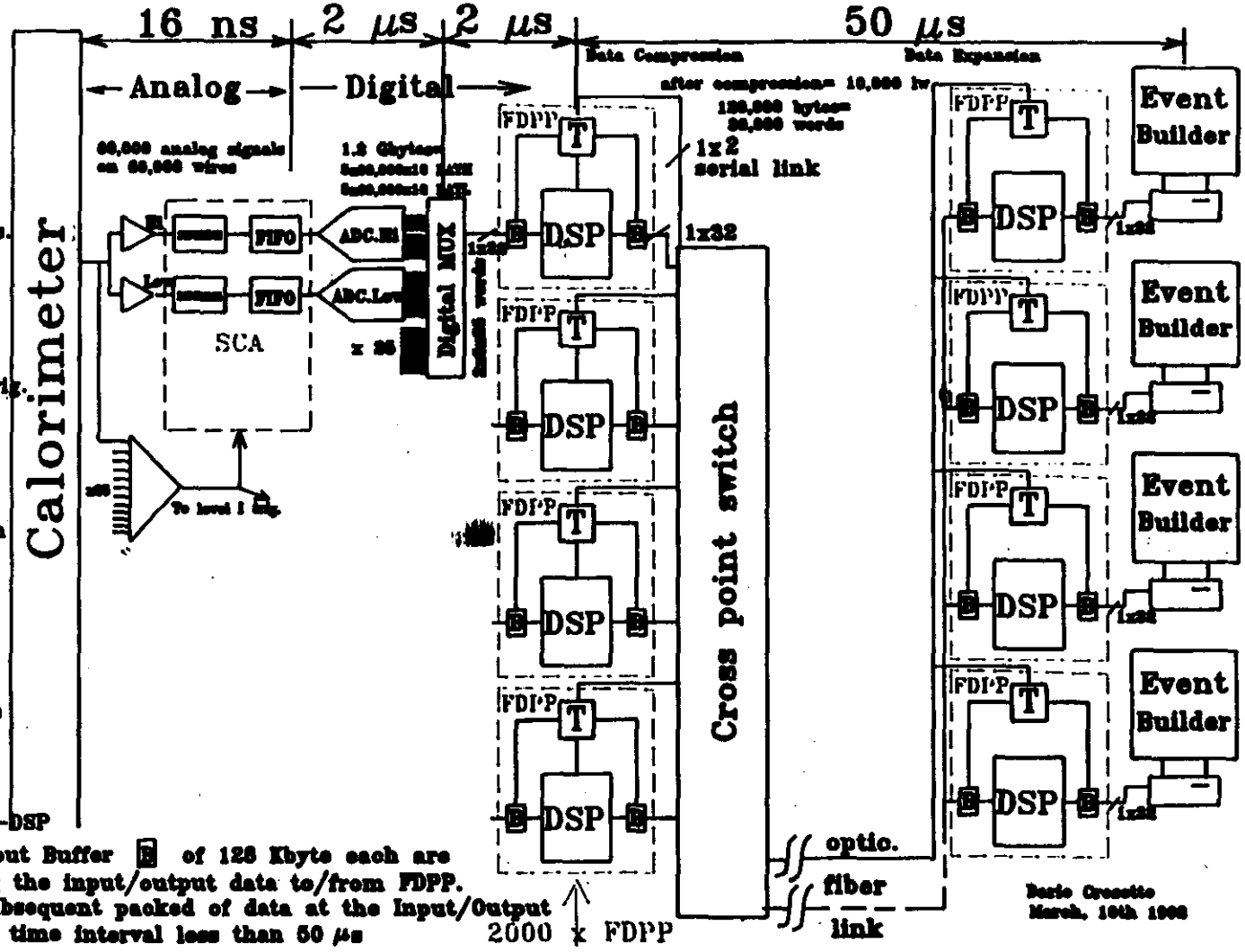
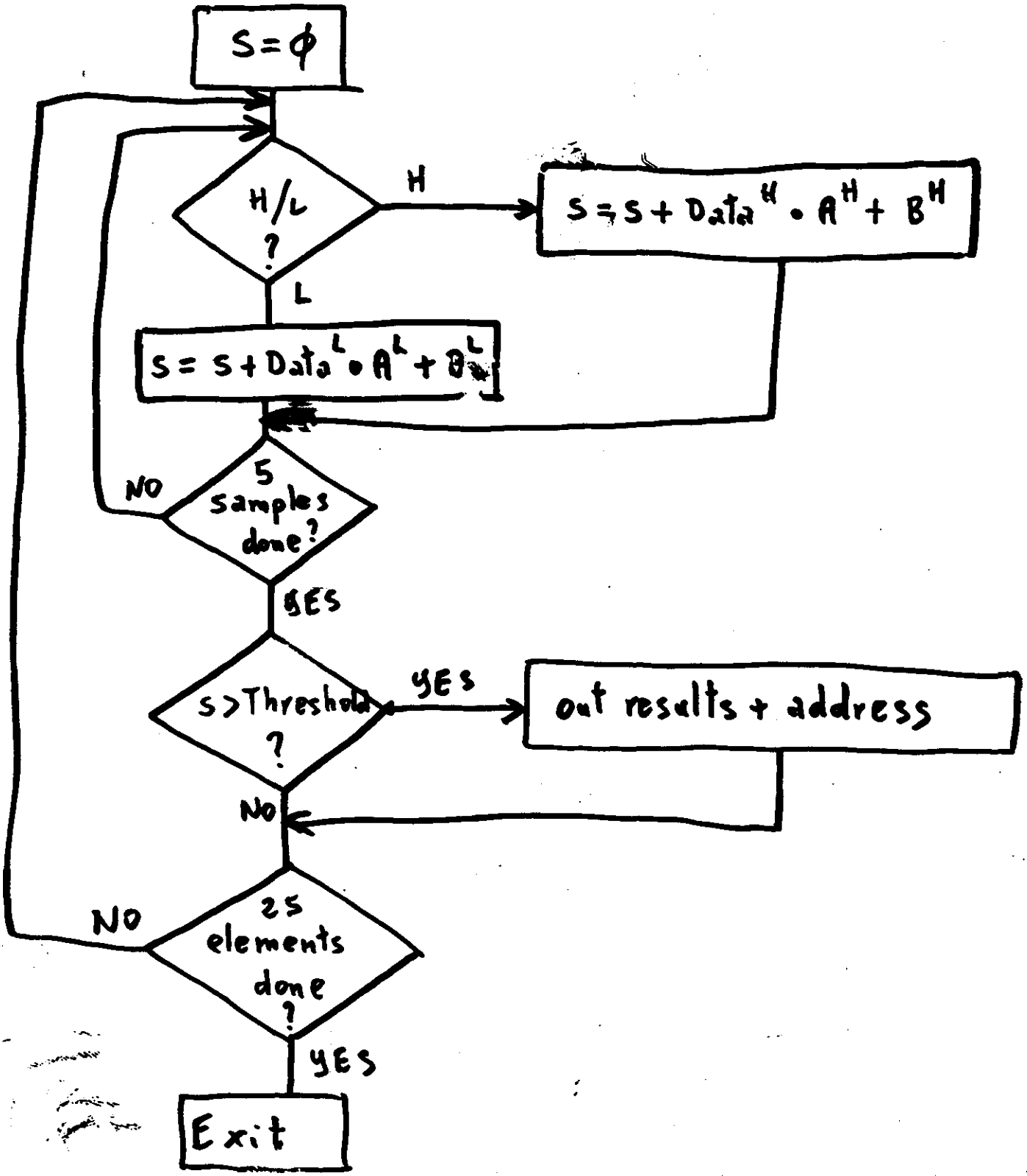


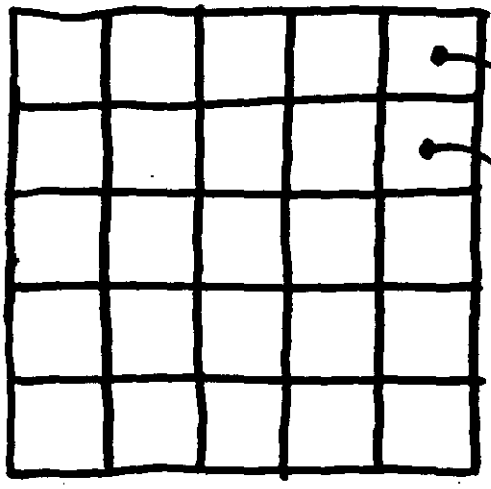
n Input/Output Buffer ▯ of 128 Kbyte each are
erandomizing the input/output data to/from FDPP.
his allows subsequent packed of data at the Input/Output
to occure at time interval less than 50 μs

Dario Crosetto
March, 16th 1992

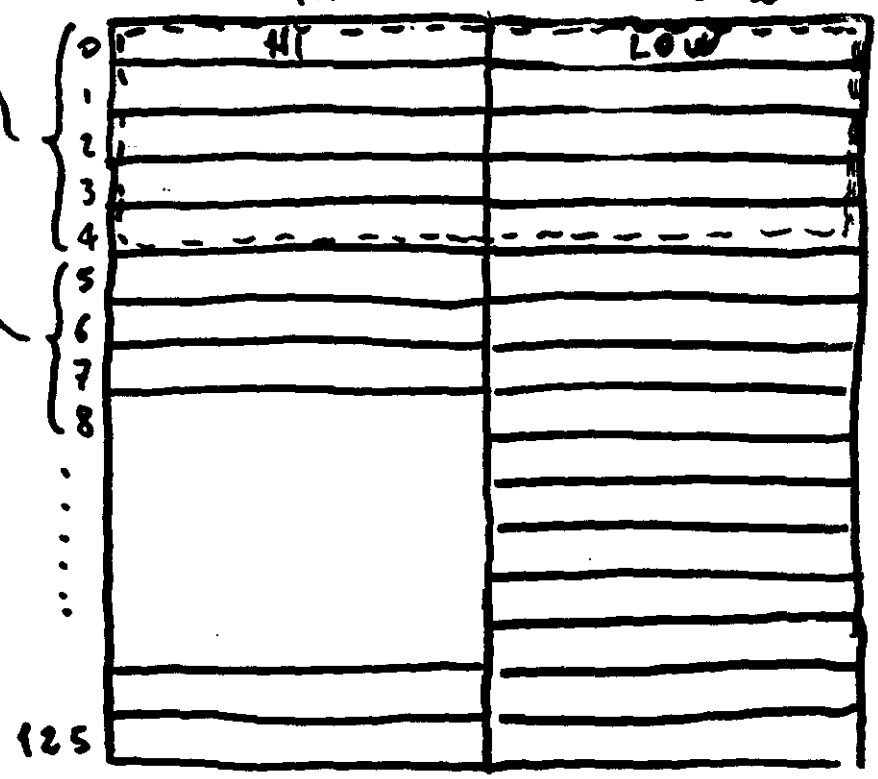
Digital Filter Algorithm



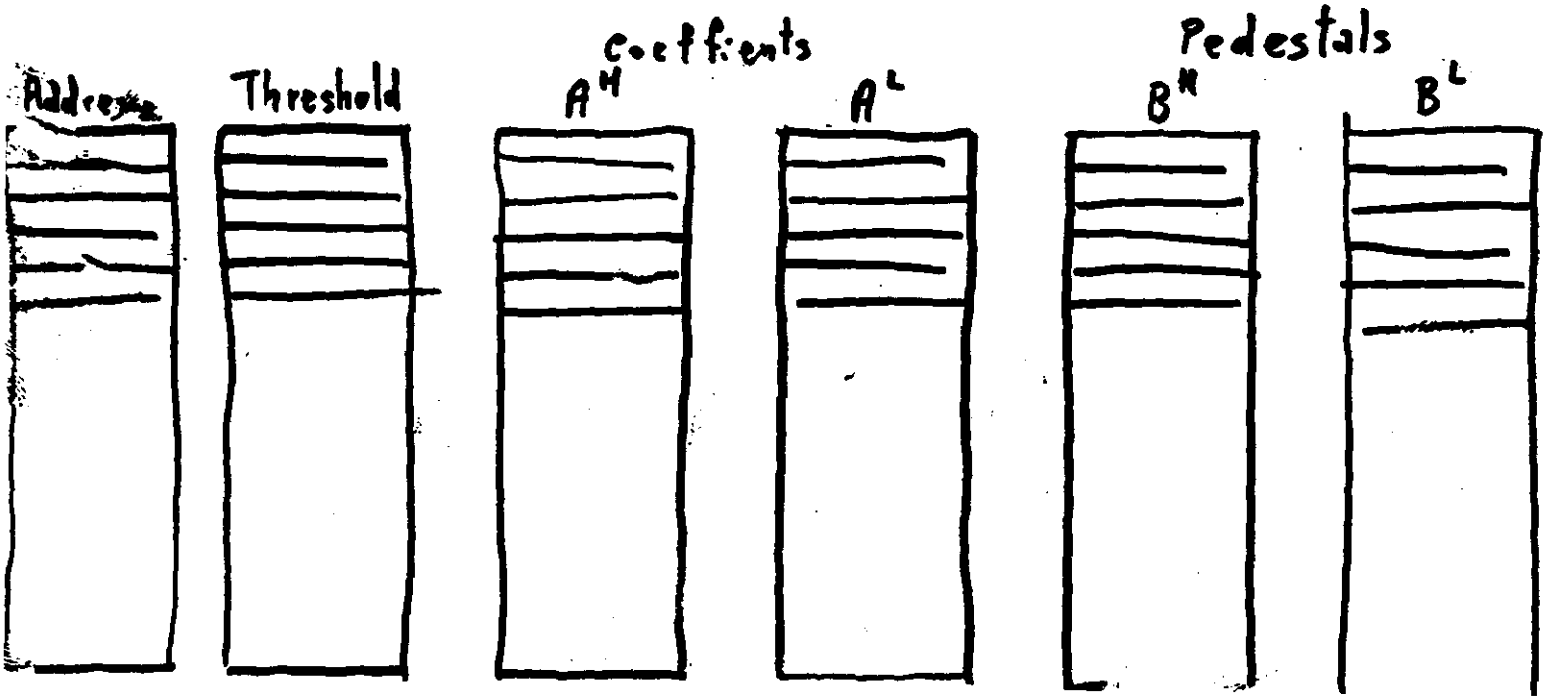
Digital Filter on 5-samples



Raw data



Lookup tables



A - I propose to build a prototype of 4 FDPP_DM because it satisfy all req. for GEM Cal

1) flexibility to test all above algorithms
2) computing capability
3) bandwidth communication of data from front end to VME sys. DAQ.

B To simulate the I level trigger algorithms that I have done on paper (+ others) on a real Data Wave Simulator.

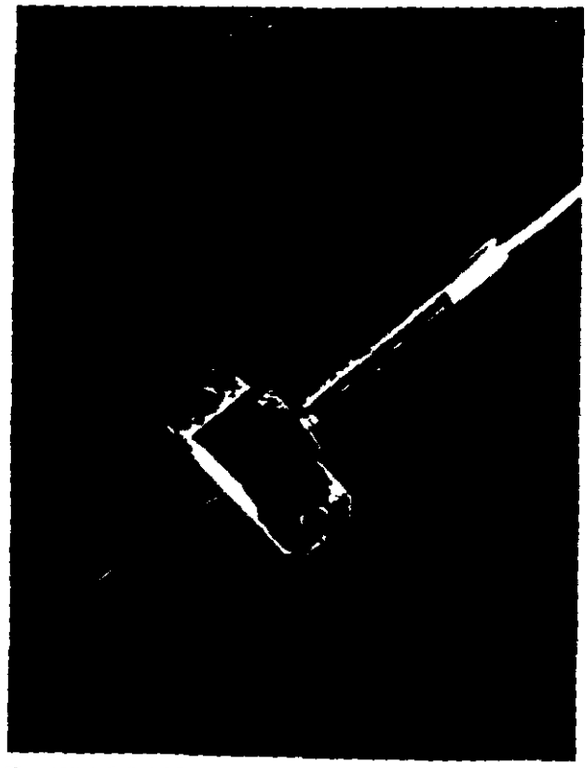
At our Knowledge there are no other chips as close to our need as it is the Data W

Data Sheet
December 1991

$ 1132 127B

AT&T Microelectronics

127A/B/C *ASTROTEC*®
InGaAs Avalanche Photodetectors



The 127 A/B/C APDs are compatible with industry-standard packages.

Features

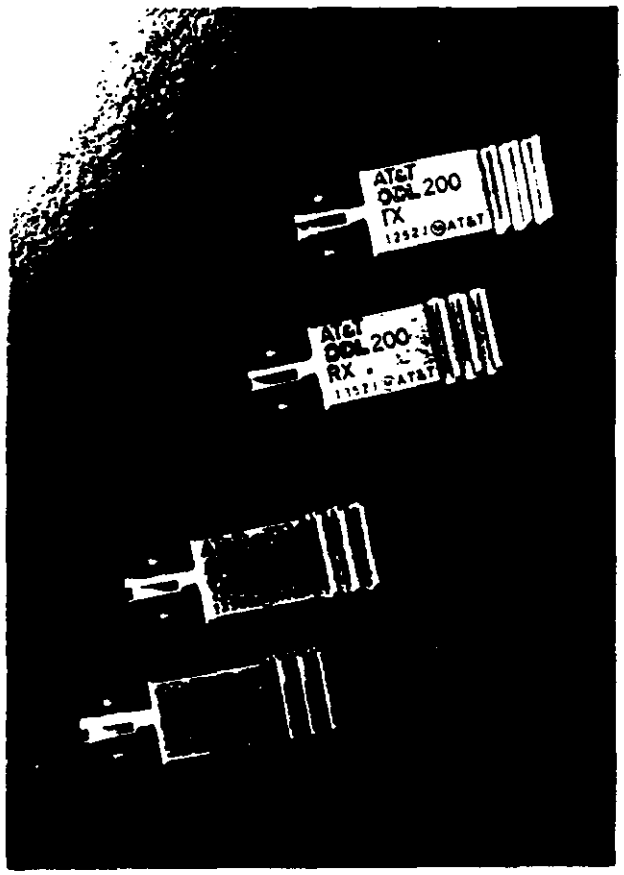
- High performance at both 1.3 µm and 1.5 µm
- Suitable for use in harsh environments
- Higher sensitivity and longer wavelength response than germanium APDs
- Permanently locked fiber alignment and high coupling stability
- Reliable planar structure with InGaAsP layer and guard ring for high-speed performance
- High responsivity from 1.0 µm to 1.6 µm
- Wide bandwidth:
  >1.0 GHz (127A)
  >1.8 GHz (127B)
  >2.5 GHz (127C)
- Compatible with industry-standard packaging
- Applications for high data rates:
  — Up to 1.5 Gbits/s (127A) or 2.5 Gbits/s (127B/C)
- Low capacitance
- Standard pigtail is a multimode fiber with a biconic connector; other pigtails available on request

Applications

- Telecommunications
  — High-speed, long-haul communication systems
  — High-speed metropolitan area networks
  — Submarine cable communication systems
  — High-frequency analog transmission
- Military
  — Very low-noise receivers
  — Satellite transmission
  — Optical radar
  — Free-space optical communication systems

Data Sheet K.t $620

ODL® 200 Lightwave Data Link With Flag



A high-performance optical data link provides electrical isolation and secure transmission between DTE systems.

Benefits

- Data link immunity to EMI/RFI, crosstalk, and ground loops
- Secure data transmission without encryption

Features

- Data rates from 40 Mbits/s to 220 Mbits/s (NRZ) at 1.3 μm wavelength
- New transmitter design with reduced power dissipation
- New receiver design with improved receiver sensitivity and dynamic range
- 100K ECL compatible
- Single power supply
- Ambient temperature: 0 °C to 70 °C (See Thermal Characteristics section.)
- Rugged, connectorized 16-pin DIP
- High reliability (MTBF > 1×10^6 hours)

Applications

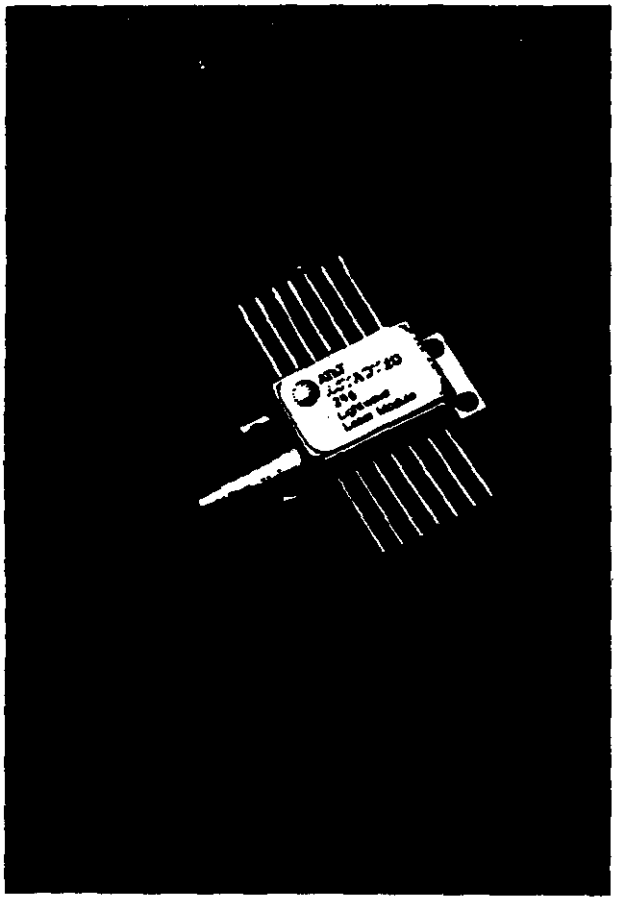
- Telecommunications
  - — Network control and timing
  - — PBX module interface
  - — Local loops
- Data Communications
  - — Local area networks (LANs)
  - — Point-to-point communications
  - — Channel extenders
- Security communications
  - — Banking
  - — Military

Preliminary Data Sheet
December 1991

AT&T Microelectronics

$ 6900

246-Type *ASTROTEC*® Digital Isolated DFB Laser Module



The 246-Type Laser Module is available with a 14-pin, hermetic, butterfly package.

Features

- Isolated package providing a minimum of 30 dB isolation
- SONET compatible
- High-performance, distributed-feedback (DFB) laser
- 14-pin, butterfly package
- 25 Ω, impedance-matched, RF input
- 2.5 Gbits/s data rate (NRZ)
- Epoxy-free, hermetic package
- Wide operating case temperature range: −40 °C to +65 °C
- Operation at 1.3 µm or 1.55 µm wavelength
- InGaAs, PIN, photodetector backface monitor
- Low threshold current
- High reliability

Applications

- Telecommunications
  - — SONET
  - — Long-haul
  - — Interexchange
  - — Undersea
- Military
  - — Space stations
  - — Phased-array radar
  - — Microwave