GEM TN-92-63

GEM Central Tracker: A Progress Report

Central Tracking Group

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Abstract:

The GEM Central Tracker group now has arrived at a new baseline design which employs Silicon Microstrips for the inner detector and Interpolating Pad Chambers for the outer tracker. This baseline design is described in this Progress Report in some detail.

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1 Introduction

The Central Tracker of the GEM detector is designed to operate in the 0.8 Tesla magnetic field of the large GEM superconducting solenoid. The tracker is compact, with a 75 cm outer radius and a total length of 300 cm. It covers a pseudorapidity range of ± 2.5 units. The present baseline design consists of a Silicon Microstrip (SM) inner tracker and an Interpolating Pad Chamber (IPC) outer tracker. The geometry of the Central Tracker in this design is shown in Figure 1.1(a).

Since the submission of the GEM Expression of Interest, a variety of technologies were considered for use in the GEM Central Tracker. For the inner tracker silicon microstrips, silicon pixels and long drift length silicon detectors were discussed. Silicon pixel and long drift silicon detectors were considered to be too immature, with large uncertainties of performance, radiation resistance, and costs, to be a sensible choice at this time. Silicon microstrip detectors were chosen as the baseline design for the following reason:

1. The very fine segmentation possible combined with proven high radiation resistance make this detector ideal as the element closest (10 cm) to the interaction point.

2. Very high spatial resolution allows very precise vertex position and track impact parameter measurement.

3. It is a mature technology, which is presently in use in a number of fixed target and collider experiments with relatively well understood performance, radiation resistance and cost properties.

Silicon detectors were considered to be too expensive for the outer tracker. Technnologies under serious discussion for outer tracker were Straw Tubes, Scintillating Fibers and Interpolating Cathode Pad Chambers. The Interpolating Pad Chambers were chosen for the baseline design for the following reasons:

1. Pad sizes of the order of a few cm^2 in area are quite natural. This allows for a low occupancy even at a luminosity of $10^{34} cm^{-2} sec^{-1}$. Thus, this technology is suitable even at the highest luminosities of the SSC. The other technologies would result in considerabley higher occupancies.

2. The pads, in some approximation, approach 3 dimensional points, which is quite important for good tracking in the high rate and multiplicity environment of the SSC. The two other technologies produce stereo images i.e. all tracks projected onto a plane, which make pattern recognition more difficult in this environment.

3. Interpolating Pad Chambers are not a new technology; they have been demonstrated to have the resolution needed with chamber sizes similar to those required for the GEM tracker design.

In this Progress Report, for the sake of definiteness, we will give values of the various parameters for the Tracker design that are our best estimates at this time. We are now pursuing an R & D program and computer simulations of the tracker to evaluate and optimize these parameters. Some of these parameters are sure to change as a result of this process over the next year or so.

The Silicon Microstrip inner tracker consists of six layers of silicon strip ladders. The geometrical layout of the silicon is shown in Figure 1.2. Each ladder is composed of two back-to-back single sided silicon sensors with a 5 mrad stereo angle between the two sensors. Each sensor is 300 μm thick with a strip pitch of 50 μm. Each pair of sensors provides a space point with a resolution of 10 μm in the $r - \phi$ plane and 3 mm in the $r - z$ projection. The six layers of ladders are organized into three superlayers, each of which provides a track stub to a track finding algorithm. In the forward region, the silicon sensors are mounted into disks with the strips projecting radially inward toward the beam axis. The Silicon Tracker is 200 cm long and extends in a radius from 10 to 35 cm. The total area of silicon ladders in the detector is about 7 m^2 with about 3.5×10^6 strips to be read out. The read-out will be highly multiplexed, with 1028 strips to one fiber optic readout channel, for a total readout channel count of 3500.

The outer tracker consists of 8 layers of pad chambers, both in the barrel region at radii between 35 and 70 cm, and in the forward region which extends from 20 to 70 cm in radius. The 8 layers are arranged in 4 superlayers with 2 layers each. Each barrel layer will consist of 20 chambers, each covering 18° in azimuth, with the largest chamber being 30 cm wide x 200 cm long. The forward layers will be disks divided into ten trapezoidal chambers about 50 cm x 50 cm each.

The IPC's in this system will be very similar in concept and performance to chambers with chevron shaped cathode pads which have been constructed and are now taking data in experiment E-814 at Brookhaven AGS [2]. These chambers have various sizes up to 50 cm x 200 cm

and have obtained a resolution of ~50 μm, or ~1% of the pad size, which is what the GEM design calls for.

Each of the chambers will be tilted in azimuth by the Lorentz angle of the gas (~6 to 9°) so that the $\bar{E}$ x $\bar{B}$ effect in the 0.8 T field does not degrade the resolution. This tilt also allows the chambers to be overlapped, eliminating dead regions due to electronics and structural elements (see Figure 1.1b).

The direction of good resolution in these chevron pad chambers is along the anode wire. Thus, the wires in the barrel chambers will run across the chambers, in the "ϕ direction", keeping the wire length between 15 and 30 cm. In the forward chambers the wires will also run in the "ϕ direction", with wire length between 10 and 40 cm.

In the present design pad sizes are a uniform $\Delta\eta x \Delta\phi = 0.0007$ in all parts of the tracker. This results in a total of just under 400,000 pads for the entire device.

The anode wires will be spaced at 20 mm intervals. To obtain precision better than the pad size in the "Θ direction", readout of the anode wires is planned for at least one layer in each superlayer. A digital readout would provide a precision of ~600 μm in this direction. This precision in each of the superlayers will provide the required δz ~1 mm to separate event vertices at a luminosity of $10^{34} cm^{-2} s^{-1}$, when the silicon tracker is expected to be out of operation. This would require about 100,000 wires to be read out digitally, which will be multiplexed at a level that satisfies the occupancy requirements.

The IPC readout electronics for each pad include a fast front end amplifier and shaper feeding an analog pipeline which is multiplexed at the output by a factor of 256, giving a total of 1600 channels. The present design calls for the multiplexed analog outputs to be routed to Mach-Zehnder electro-optic modulators, each of which is connected by a fiber optic cable to a remote 9 bit flash ADC system. The readout of the IPC wires can be accomplished with a simple comparator on each of the instrumented wires, followed by a multiplexed digital pipeline.

FIGURE 1

GEM Central Tracking

QUADRANT VIEW

NOTE: BARREL ROTATED 11 DEG. ABOUT Z

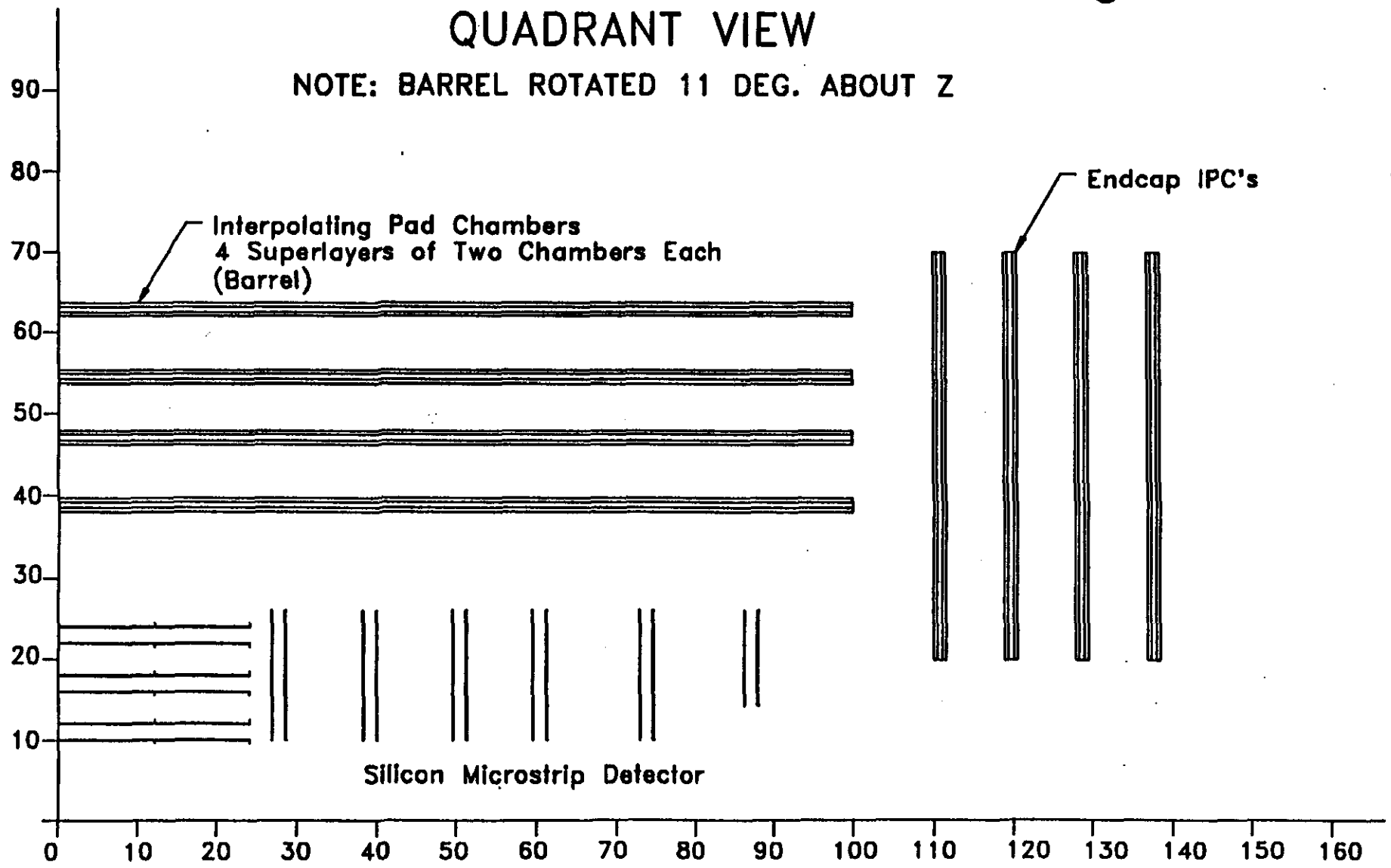

Figure 1.1a

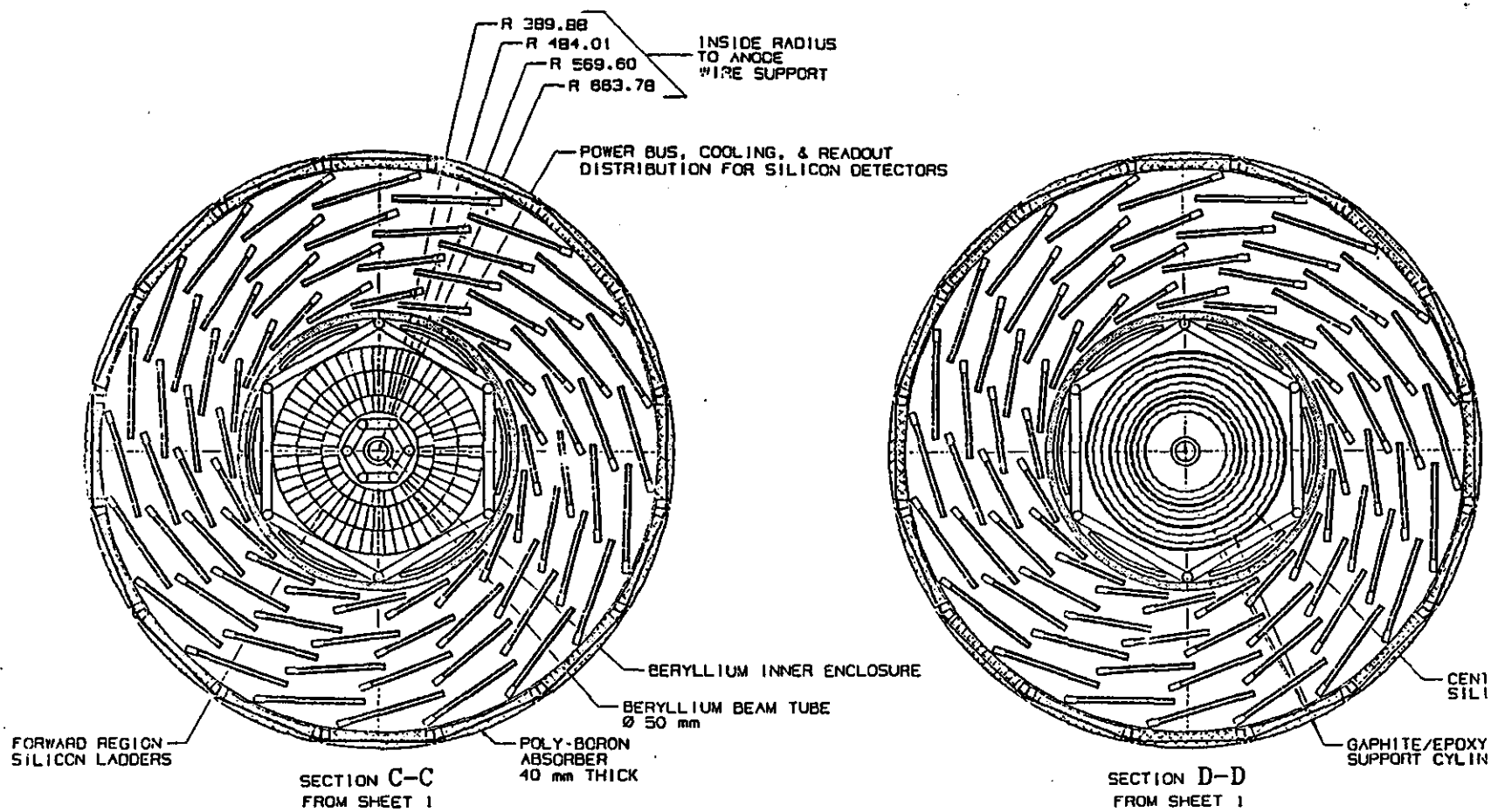
R 389.88
R 484.01
R 569.60
R 663.78
INSIDE RADIUS
TO ANODE
WIRE SUPPORT
POWER BUS, COOLING, & READOUT
DISTRIBUTION FOR SILICON DETECTORS
BERYLLIUM INNER ENCLOSURE
BERYLLIUM BEAM TUBE
Ø 50 mm
FORWARD REGION
SILICON LADDERS
POLY-BORON
ABSORBER
40 mm THICK
SECTION C-C
FROM SHEET 1
GRAPHITE/EPOXY
SUPPORT CYLIN
SECTION D-D
FROM SHEET 1

Figure 1.1b

GEM SILICON INNER TRACKER

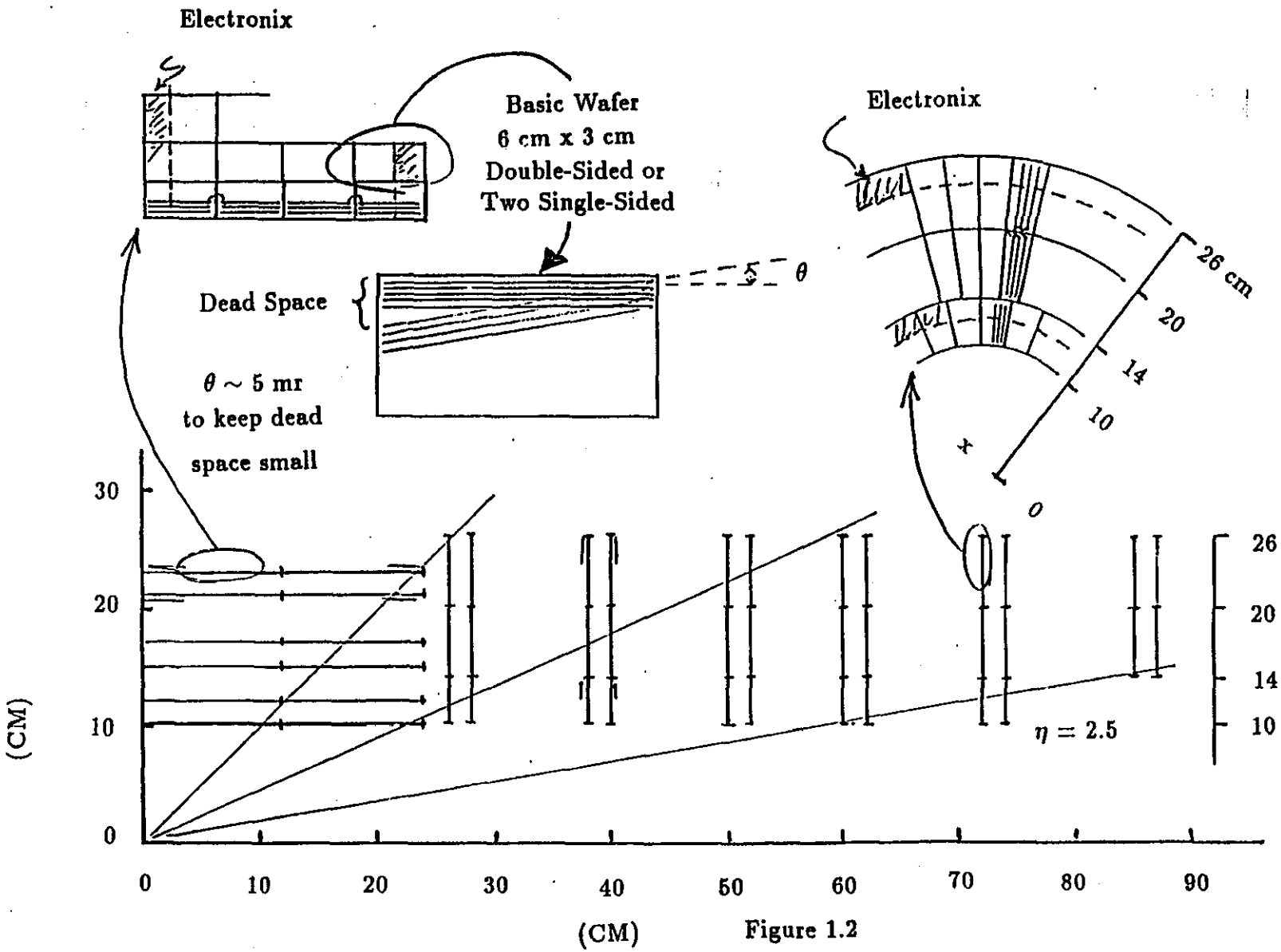

Figure 1.2

2 Physics Goals, Design Parameters, and Detector Performance

2.1 Physics Goals of the Central Tracker

The physics goals for the central tracking in GEM can be divided into two categories. The first are those features that are required to support the primary objectives of GEM, namely the detection of gammas, electrons and muons at high p_T. Some examples of these are:

- Identify the primary vertex of an event of interest, so that it can be separated from other pileup events in the memory time of the detector.

- Separate electrons and gammas using the presence or absence of a charged track pointing to an electromagnetic shower in the calorimeter.

- Provide track information for e, μ or γ isolation cuts, and to help with rejection of conversions and Dalitz pairs.

- Help with electron-hadron separation by providing a momentum measurement that can be compared with the energy deposition in the calorimeter.

- Help with rejection of background by matching the muon momentum measured in the central tracker with the momentum measured in the muon chambers.

- Determine the electron sign up to 400 GeV/c.

The tracker should be able to fulfull these goals well at the design luminosity of $10^{33}\text{cm}^{-2}\text{s}^{-1}$. These capabilities should also survive to luminosities up to $10^{34}\text{cm}^{-2}\text{s}^{-1}$. These minumum goals do not require full pattern recognition, but can be met by looking for hits in the tracker in a specific road extrapolated from the calorimeter or the muon system.

The second category of physics goals are more ambitious:

- Full reconstruction of the charged tracks in the event.

- Secondary vertex finding.

- Tracking at low momenta with good resolution.

These features would enhance GEM's ability to address issues such as b and top physics. They are more demanding in that they require pattern recognition capabilities and very good vertex resolution. It is expected that these more ambitious goals can be met at luminosities up to $10^{33}\text{cm}^{-2}\text{s}^{-1}$, but probably not much higher. This, however, seems satisfactory since the physics topics requiring these more ambitious features have relatively large crossections and can thus be studied at luminosities of $10^{33}\text{cm}^{-2}\text{s}^{-1}$ or below. Some examples of Physics Processes for which these central tracker goals are relevant are summarized in Table 2.3.

2.2 Design Parameters

The design parameters for the central tracker that will satisfy the goals outlined above are summarized in Table 2.1.

An extensive program of Monte Carlo simulations is now underway to demonstrate that these design parameters are appropriate for the physics goals outlined above.

2.3 Detector Performance

A GEANT based Monte Carlo simulation program is now ready and running with a detailed description of the Central Tracker. The simulation includes our current best estimate of the amount of material in the silicon, the pad chambers, the support structures, the cooling loops, and the front end electronics. The amount of material, in units of percents of a radiation length, is shown as a function of ϕ and η in Figure 2.1 and Figure 2.2. The average amount of material at 90^0 is in the vicinity of $\sim$15% of a radiation length, including all the material we are aware of at this time.

Design Parameters for the Central Tracker	
Outer Radius	70 cm
Length	± 150 cm
Rapidity Coverage	$\lvert\eta\rvert \leq 2.5$
Magnetic Field	0.8T
Occupancy at $\mathcal{L} = 10^{33} cm^{-2} sec^{-1}$ at $\mathcal{L} = 10^{34} cm^{-2} sec^{-1}$	 $\leq$1% $\leq$10%
Charge separation at 95% c.l.	$p \lesssim 400$ GeV/c
Momentum Resolution at 90° at high momenta (measurement limited) at low momenta (multiple scattering limited)	 $\Delta p/p^2 \sim$(1 to 3) x 10^{-3} (GeV/c)$^{-1}$ $\Delta p/p \sim$ 2 to 4%
Vertex Resolution along beam direction impact parameter	 $\delta z \sim$1 mm $\delta b \sim 30 \mu$m above 10 GeV/c

Table 2.1

Silicon microstrips resolution	10 μm
Silicon alignment stability	10 μm
Pad chamber resolution	50 μm
Pad chamber alignment stability	25 μm

Table 2.2: Chamber resolutions and alignment stabilities assumed in the simulations.

This simulation assumes the chamber resolutions as shown in Table 2.2. With this input, and the amount of material discussed above, the momentum resolution of the tracker, given the 0.8 T field, was calculated. Figure 2.3 shows the momentum resolution for various momenta as a function of rapidity. For these curves it was assumed that a reconstructed vertex point from several tracks in each event can be used in the best fit for each track. For the highest momentum, the multiple scattering is negligible, and we see that the measurement error near 90° is $\Delta p/p \sim 1.5 \text{ x } 10^{-3} \text{ x } p$ (GeV/c).

The resolution at the lowest momentum is dominated by multiple scattering, which limits the low momentum resolution near 90° to $\Delta p/p \sim 4\%$

Figure 2.4 shows the resolution in the transverse momentum p_t for various values of p_t as a function of η_t. The resolution for high p_t in the forward region is not very good, as one would expect for a solenoidial magnetic field.

The momentum up to which the sign of a particle can be determined to a 95% confidence level has been calculated and is shown in Figure 2.5.

The GEANT Simulation was also used to estimate the occupancy in various parts of the detector. These calculations included the primary tracks produced in the pp collisions as generated by PYTHIA (which agree quite well with $dn/d\eta d\phi \sim 1$ charged track per event) as well as secondaries produced in interactions and gamma conversions in the material of the tracker as well as loopers i.e. low energy particles curling up in the magnetic field producing multiple hits in the tracker. In this calculation, it was assumed that the silicon detector integrates

over one crossing only while the pad detector integrates over two crossings of the beams. Near 90°, the occupancy in the silicon is less than 0.1%, and in the pads it is around 0.3% per pad at a luminosity of $10^{33}\mathrm{cm}^{-2}\mathrm{sec}^{-1}$. The occupancy per pad is shown as a function of y in Figure 2.6 in the innermost layer of pads. The occupancy in the pad chambers is around 3% per pad even at a luminosity of $10^{34}\mathrm{cm}^{-2}\mathrm{sec}^{-1}$. For some applications where a precision measurement of the momentum is important, the relevant cell size is 3 pads, since an additional accidental hit in the same pad or an adjacent pad on either side could compromise the precision of the interpolation. In this case the relevant occupancies are $\lesssim$ 1% and $\lesssim$10% at luminosities of 10^{33} and $10^{34}\mathrm{cm}^{-2}\mathrm{sec}^{-1}$, respectively. We therefore expect that the pad detector would perform well even at the highest luminosities of the SSC.

An effort is now underway with this GEANT Simulation, to study the pattern recognition and track finding efficiency of the tracker as well as two track resolution i.e. how close to each other two tracks can be and still be resolved, and tracking efficiency inside high energy jets.

Another effort has begun in collaboration with the GEM Physics Group (F. Paige and Ken Lane et al.) to evaluate the performance of the central tracker on some selected physics topics of interest to GEM. The initial thoughts on the Central Tracker Performance/Physics Topics Matrix are shown in Table 2.3. This chart will be revised and refined as we proceed.

Physics Processes	Id. Primary Vertex	e/γ Separation	e, μ, γ Isolation Cuts	e/h Separation	Muon Momentum Check	$e\pm$ Sign Separation	Secondary Vertex	Low Momentum Track	Full Event Reconstr.
$H^0 \rightarrow \gamma + \gamma$	X	X	X						
$H^0 \rightarrow e^+e^-l^+l^-, e^+e^-\nu\bar{\nu}, e^+e^-$ *jetjet*	X	X	X	X		X			
$H^0 \rightarrow \mu^+\mu^-l^+l^-, \mu^+\mu^-\nu\bar{\nu}, \mu^+\mu^-$ *jetjet*	X		X		X				
Gluino Pair Prod $\tilde{g}\tilde{g} \rightarrow e^\pm e^\pm, \mu^\pm e^\pm$	X	X	X	X	X	X			
Techni eta $\eta_T \rightarrow b + \bar{b}$ or $t + \bar{t}$	X		X				X		
WW Scattering $W^\pm W^\pm \rightarrow e^\pm e^\pm, \mu^\pm e^\pm$	X	X	X	X	X	X			
$Z^1 \rightarrow e^+e^-$ Asymmetry	X	X	X	X		X			
B Physics, e.g. $B \rightarrow \Psi$, etc.	X						X	X	X
Top Physics $t \rightarrow W + b$, etc.	X		X				X	X	X

CENTRAL TRACKER PHYSICS STUDIES

Table 2.3

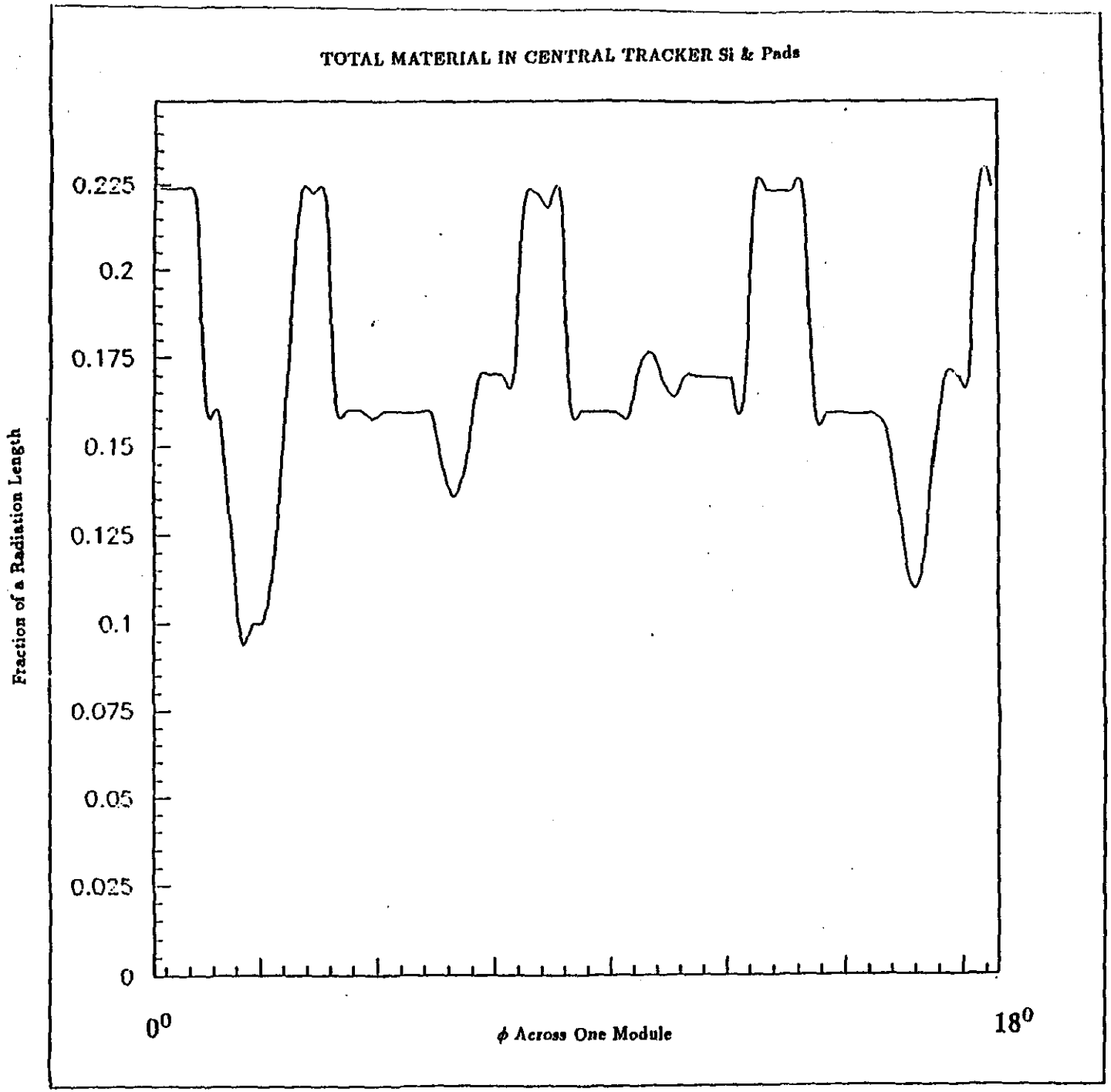
TOTAL MATERIAL IN CENTRAL TRACKER Si & Pads
Fraction of a Radiation Length
0.225
0.2
0.175
0.15
0.125
0.1
0.075
0.05
0.025
0
0^0
ϕ Across One Module
18^0

Figure 2.1

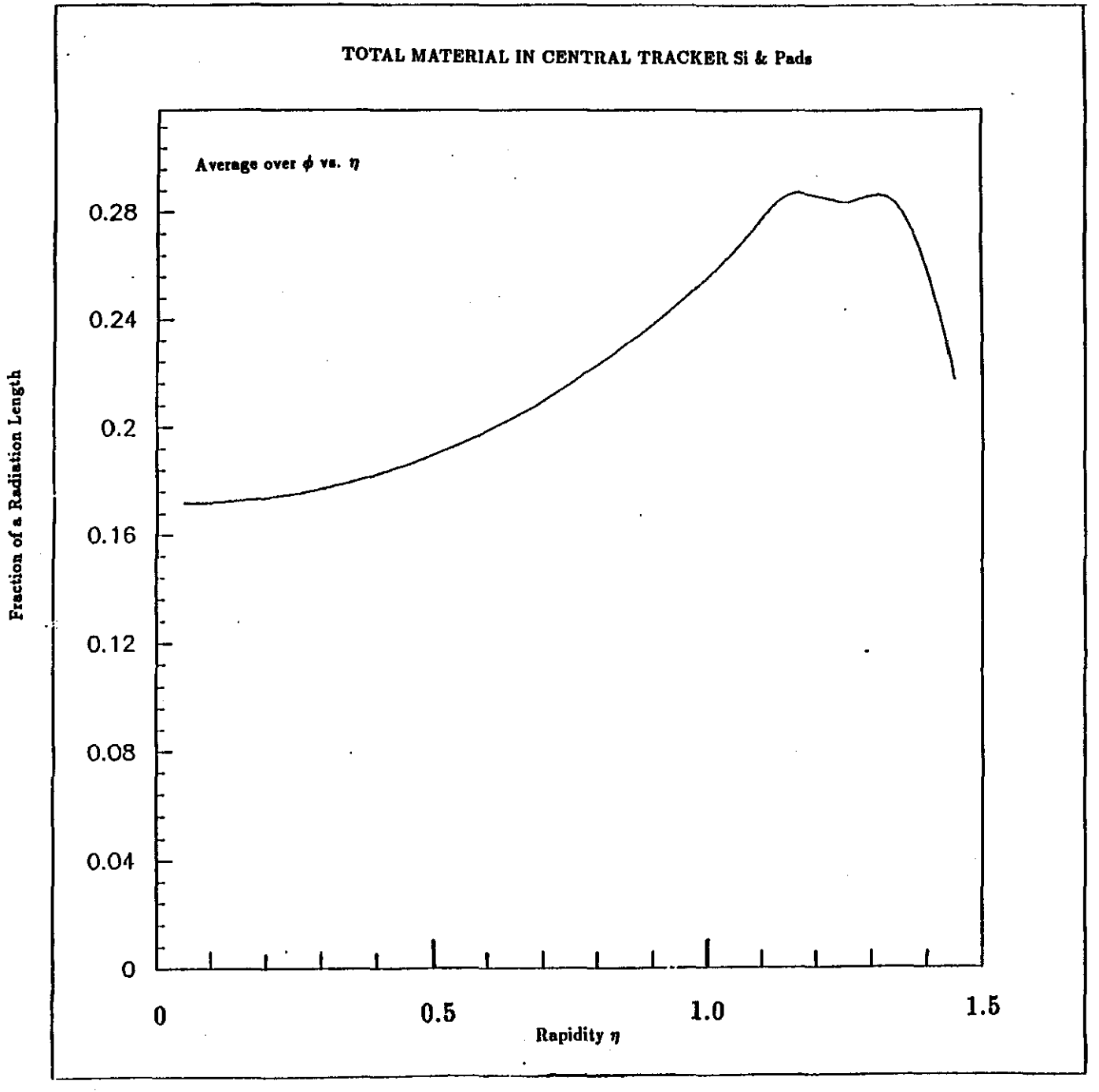
TOTAL MATERIAL IN CENTRAL TRACKER Si & Pads
Average over ϕ vs. η
Fraction of a Radiation Length
0.28
0.24
0.2
0.16
0.12
0.08
0.04
0
0
0.5
1.0
1.5
Rapidity η

Figure 2.2

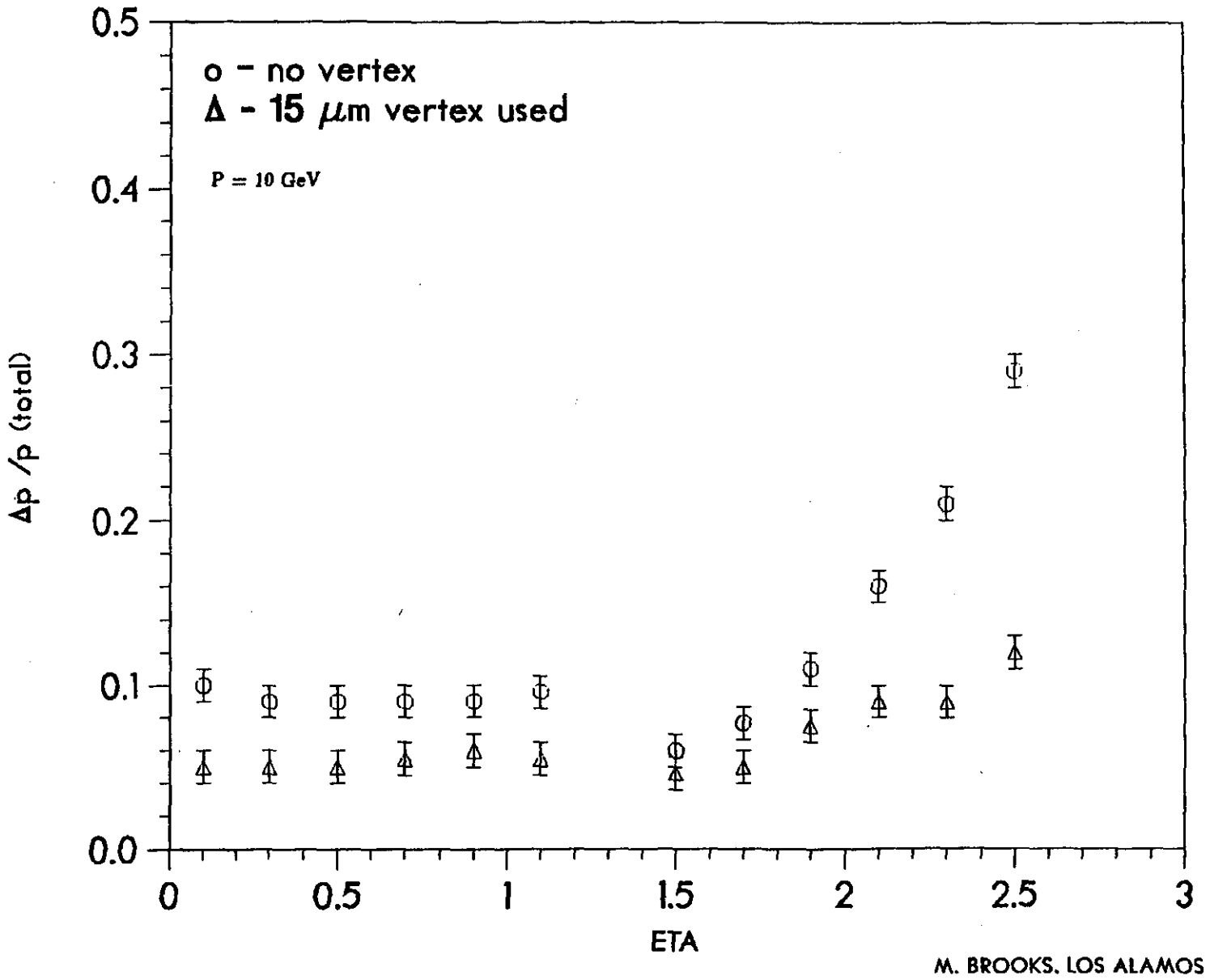
o - no vertex
Δ - 15 μm vertex used
P = 10 GeV
Δp /p (total)
0.0
0.1
0.2
0.3
0.4
0.5
0
0.5
1
1.5
2
2.5
3
ETA
M. BROOKS, LOS ALAMOS

Figure 2.3a

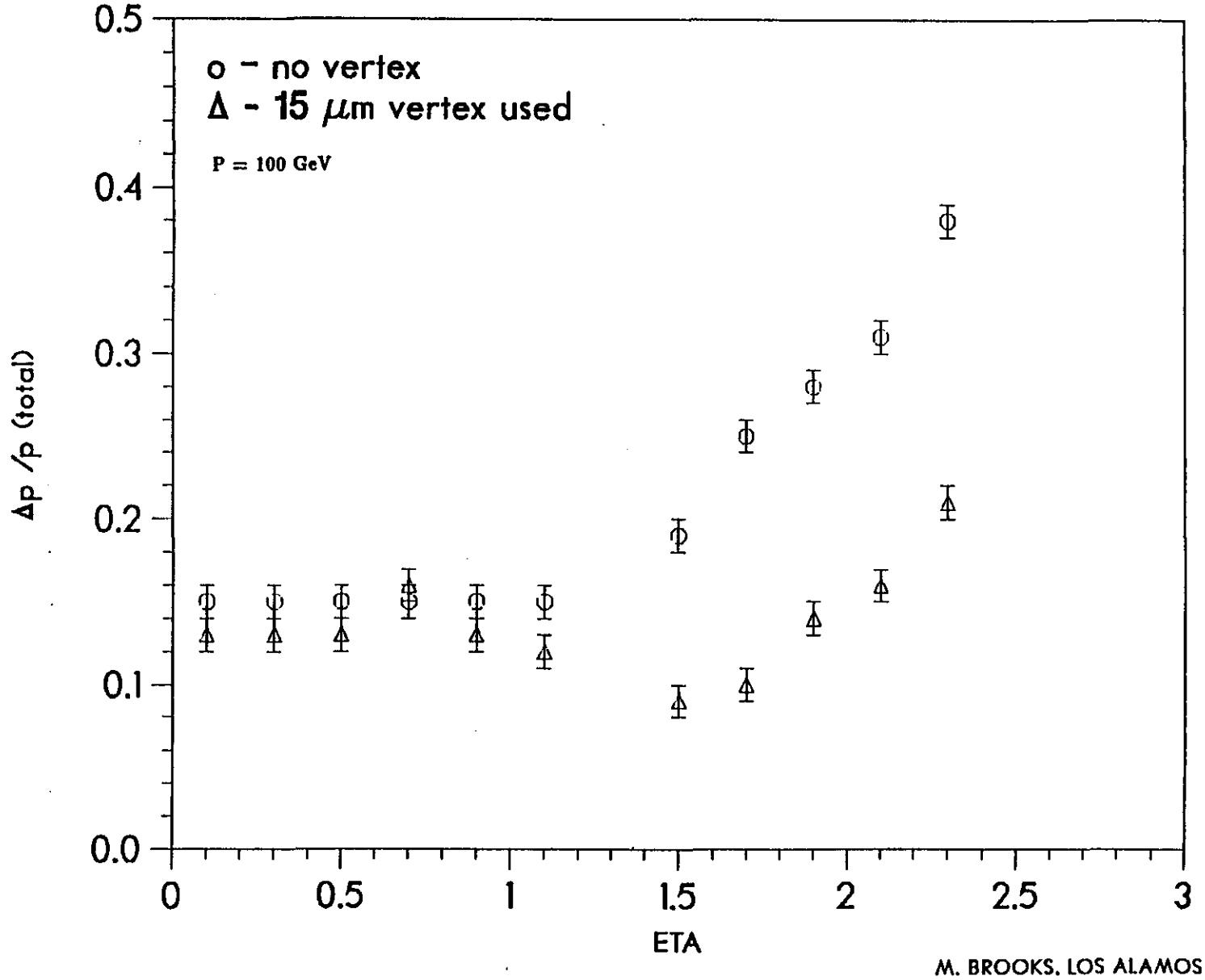
o - no vertex
Δ - 15 μm vertex used
P = 100 GeV
Δp /p (total)
0.0
0.1
0.2
0.3
0.4
0.5
0
0.5
1
1.5
2
2.5
3
ETA
M. BROOKS, LOS ALAMOS

Figure 2.3b

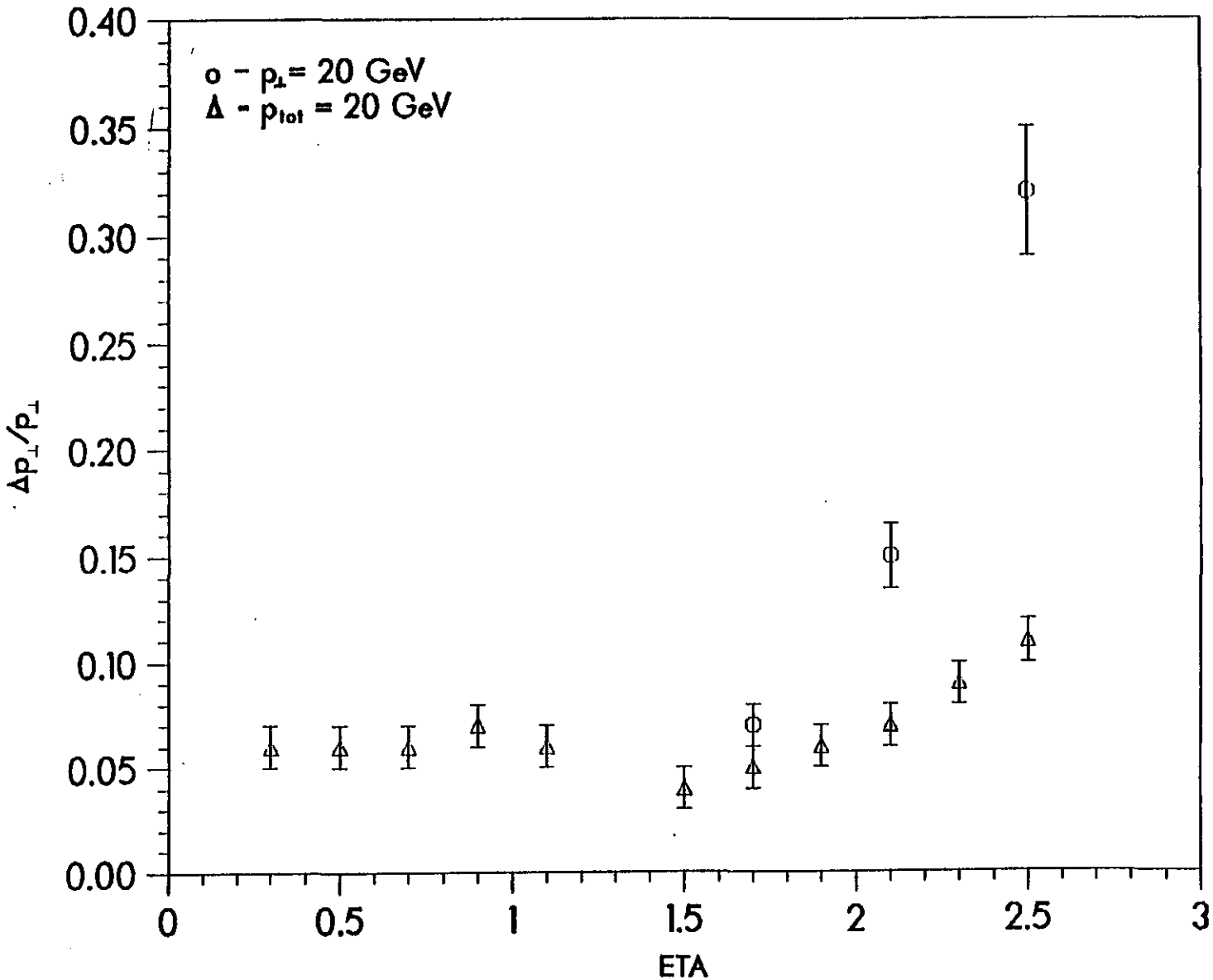

Figure 2.4

M. BROOKS, LOS ALAMOS

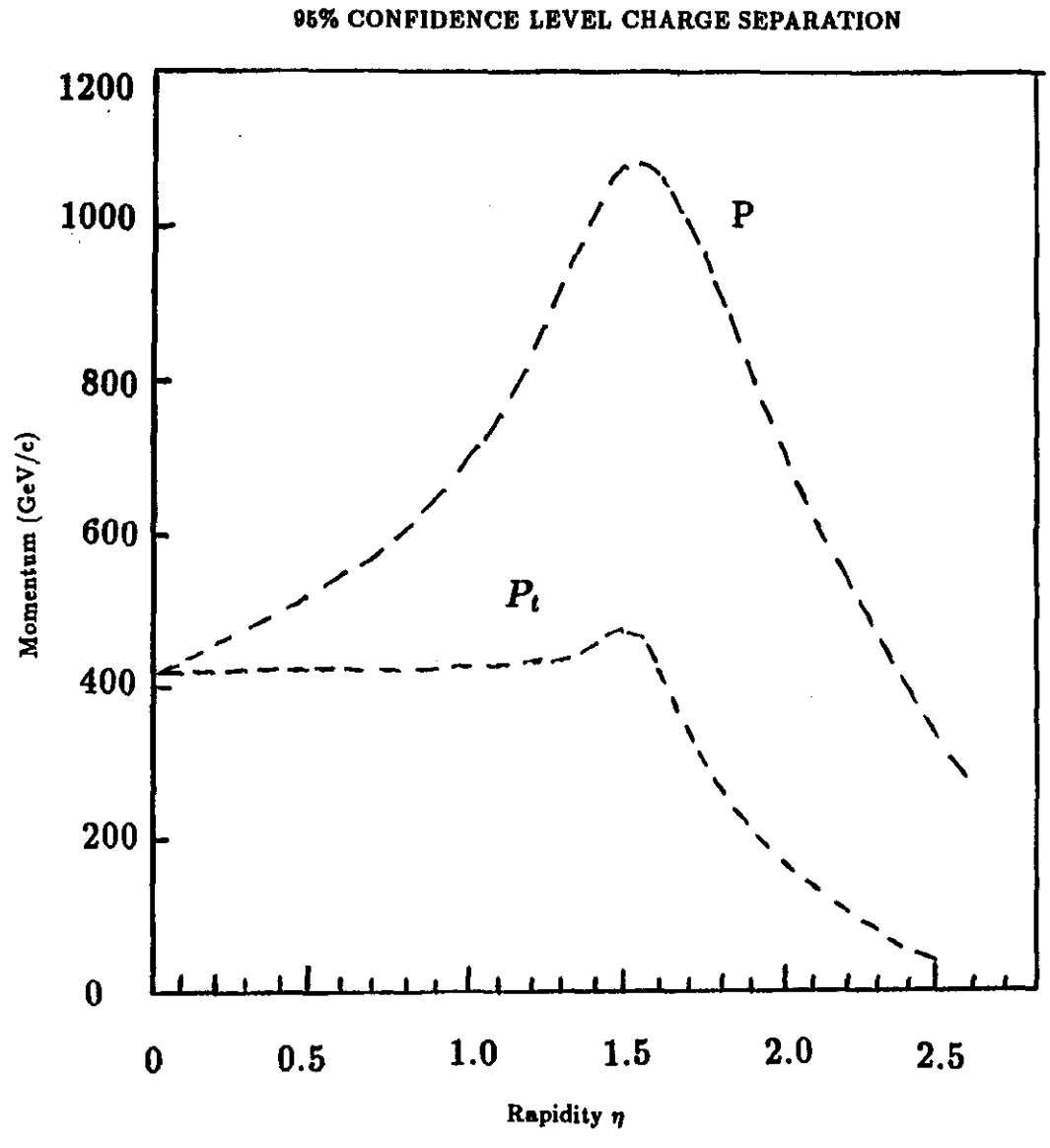
95% CONFIDENCE LEVEL CHARGE SEPARATION
1200
1000
800
600
400
200
0
Momentum (GeV/c)
P
P_t
0
0.5
1.0
1.5
2.0
2.5
Rapidity η

Figure 2.5

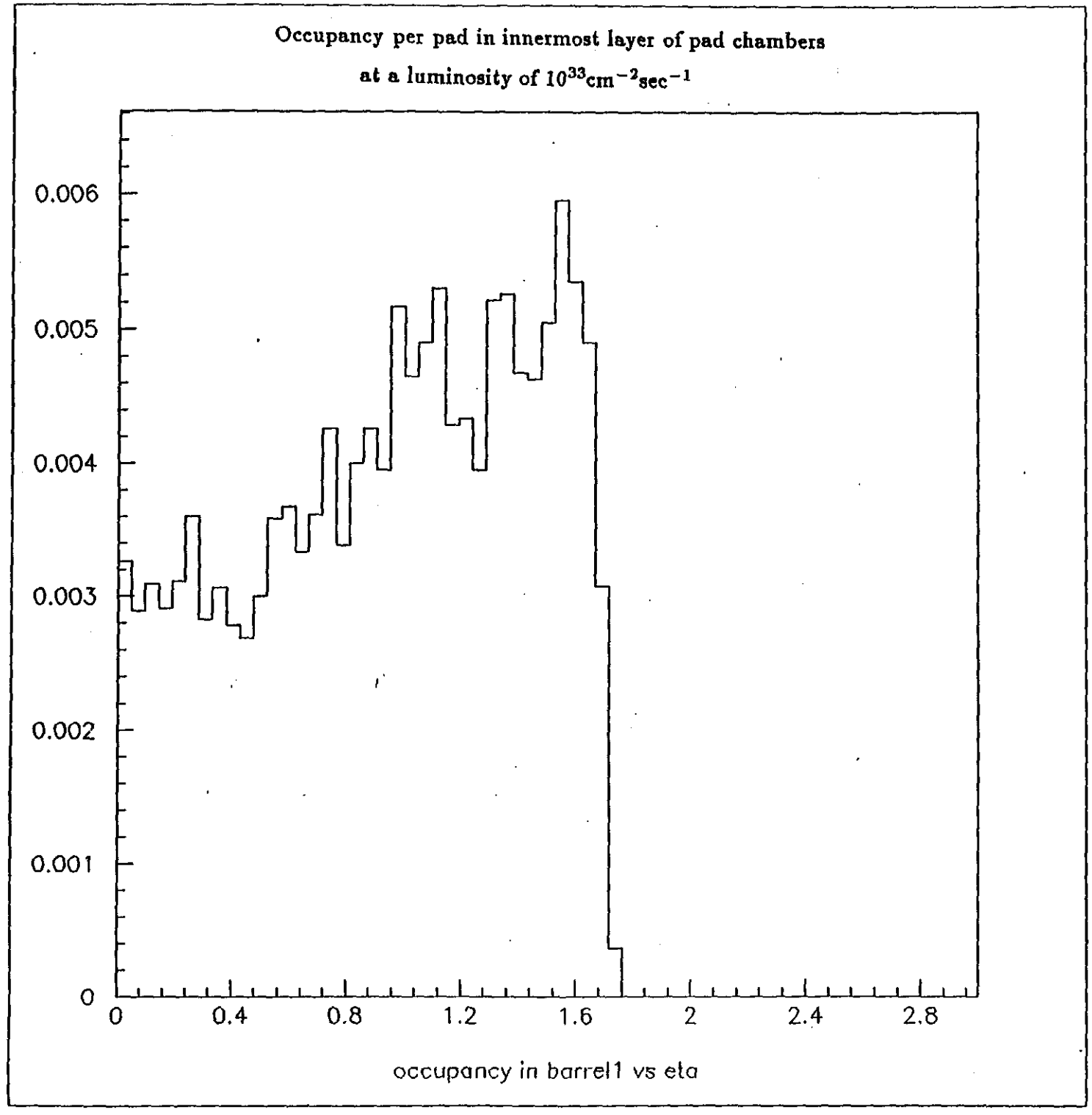
Occupancy per pad in innermost layer of pad chambers
at a luminosity of $10^{33}cm^{-2}sec^{-1}$
0.006
0.005
0.004
0.003
0.002
0.001
0
0
0.4
0.8
1.2
1.6
2
2.4
2.8
occupancy in barrel1 vs eta

Figure 2.6

3 The Silicon Microstrip Inner Tracker

3.1 Design Considerations

The design considerations for the silicon microstrip detector involve compromises between the physics requirements, mechanical constraints, radiation environment, and cost. In general cost has been the overriding concern with the physics a close second. The primary goals of the central tracker and therefore the silicon microstrip detector is to support the primary objectives of GEM of detecting gammas, electrons and muons. The silicon tracker portion of the central tracker aids in these goals by identifying the vertex of the event of interest, by providing accurate space points for the momentum measurement, and by providing good pattern recognition capabilities. The excellent position resolution of the silicon strip detector (~ 10 μm) is the only way to obtain good primary vertex and secondary vertex resolution. The design specifications for the silicon microstrip detector to meet the physics goals at a luminosity of 10^{33} are,

- pattern recognition efficiency > 80%
- z resolution < 1.0 mm
- occupancy < 1%
- $|\eta|$ coverage ≤ 2.5
- position stability in ϕ of ≤ 10 μm
- low mass
- lifetime of 10 years

3.1.1 Physical Dimensions - Silicon Tracker

The outer dimensions for the silicon tracker is 2.0 m long and 0.7 m in diameter (see figure in section 3.2). All detector elements, cooling system, electrical connections are contained in this enclosure. The silicon tracker baseline design consists of a barrel portion with three (3) concentric cylinders and two forward sections with six (6) disks each. Each barrel layer, called a barrel superlayer, has two closely spaced layers of silicon strip detectors in a sandwich configuration. The forward disks, called a forward superlayer, consist of two closely spaced silicon disks of pie shaped silicon detectors rotated 36 degrees with respect to each other. Each individual disk

has 5 pie shaped silicon detectors covering one half of the frontal area. The barrel superlayers start at a radius of 10, 15, and 20 cm and the forward superlayers are at 26.0, 35.5,50.0,60.0,72.0, and 85 cm from the I.P. The butane cooling gas enclosure surrounds the entire detector and extends to 35 cm. The free space between the butane enclosure and the detector is taken up with the electrical distribution network, cooling tubes, and support assembly. The geometrical arrangement of the silicon tracker is designed to insure efficient coverage out to eta of 2.5. The present design has not been optimized. Successive iterations will occur when we understand this design.

3.1.2 Ladder Assembly

The barrel assemblies and forward assemblies consist of 6.0 cm by 3.3 cm silicon detectors fashioned into a ladder configuration 12 cm by 3.3 cm with the strips running the long direction (see figure in section 3.2). The choice of a strip length of 12 cm was dictated by our desire to keep the strips long to conserve readout electronics but short enough to limit the detector capacitance on the front-end electronics. The dimensions of the silicon detectors provide efficient use of the area of the 4 inch silicon wafer. The assembly consists of two single sided silicon wafers bonded in a sandwich configuration, one side measuring r-φ and the other side measuring r-z through the use of small angle stereo. The stereo angle is presently 5 milliradians but could change when we finish our design studies. The choice of the stereo angle will be a compromise between z resolution and a dead region on the wafers.

3.1.3 Single vs. Double Sided Silicon Wafers

The choice of whether we use either single sided or double sided silicon wafers must consider the following,

- Radiation resistance
- Radiation lengths
- Capacitance
- Cost

The radiation resistance for single-sided detectors has been studied and found to be reasonably radiation resistant. The fixed target experiment E789 at Fermilab has accumulated over 1×10^{13} particles/cm ^{2} on their silicon wafers without loss of performance. These detectors were tested in the LAMPF beams and found to operate satisfactorily up to 7×10^{13}particles/cm^2 [Kap]. Studies by the Silicon

Tracking Subsystem R&D program have demonstrated that single-sided detectors can be operated up 6 x 10^{13} particles without serious loss in pulse height[Pit]. These studies have shown that type inversion occurs at ~ 2 x 10^{13} after which an increase in voltage is needed to obtain depletion of the silicon detector. The maximum voltage that can be applied to the detectors before breakdown determines the radiation level that can be tolerated. At a fluence of 6 x 10^{13} the detectors require a depletion voltage of about 150 volts. See figures 3.1.3.1 and 3.1.3.2. A variety of studies have shown that the neutron fluence limit of single-sided silicon detectors is >10^{14} where again the upper limit depends on the depletion voltage required [Lin]. Studies of the radiation resistance of double-sided detectors have recently been completed by several groups and their conclusions show that double-sided detectors have comparable radiation tolerance as the single-sided detectors [Sai].

From PITZL, et.al., SLIPP 91/05

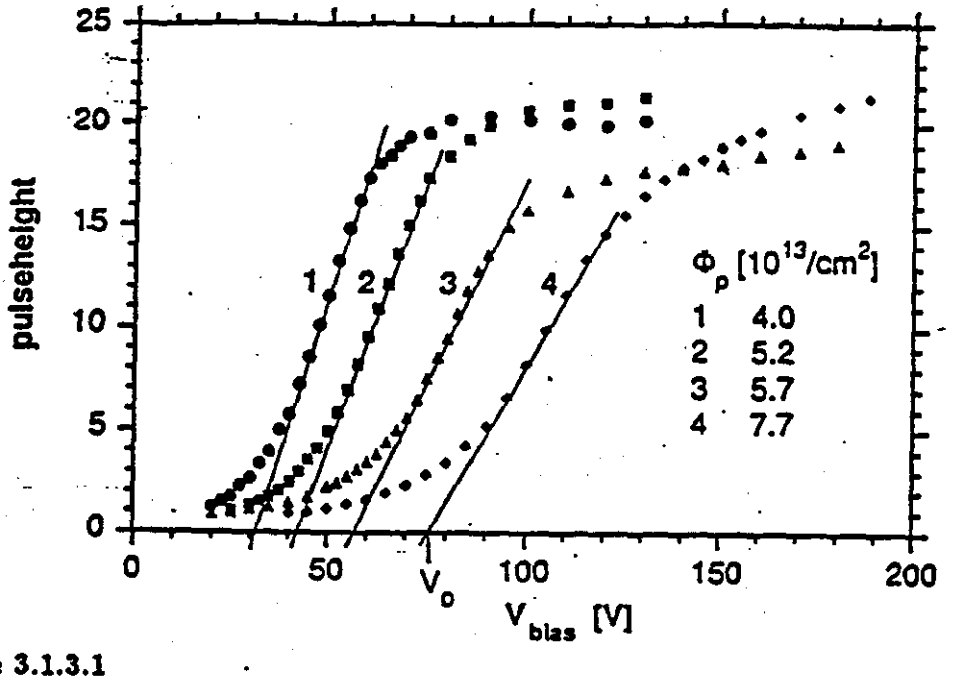

Figure 3.1.3.1

LED shining at 4 spots with different fluences on the front side of an inverted detector. The line fits are used to determine the intersect voltage V_0.

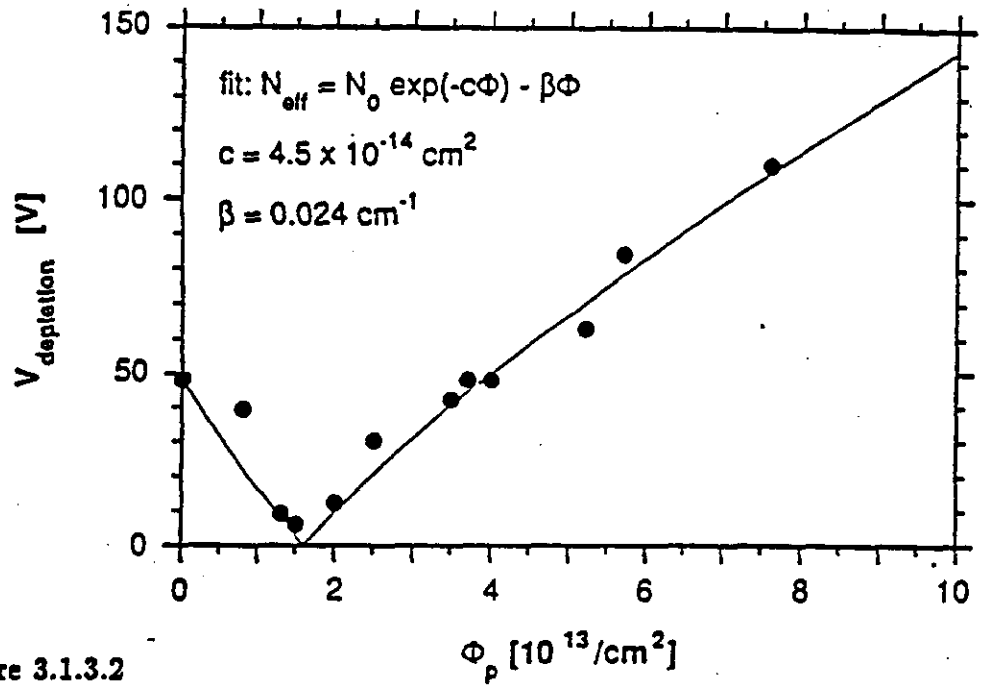

Figure 3.1.3.2

Depletion voltage versus proton fluence for SI detectors. Type inversion occurs at $\Phi = 1.5 \cdot 10^{13}/cm^2$. *The line is the best fit according to equations (1) and (2).*

The capacitance of the strip of the silicon detectors is an important parameter because the noise level of the anticipated front end bipolar preamplifier scales with the square of the detector capacitance and the power requirements the input preamplifier with a shaping time of 20 ns increase with increasing detector capacitance [Spi]. We want to keep the signal to noise (S/N) to >12 and the power requirements for each strip as low as possible. In single-sided detectors the major contribution to the total strip capacitance is the interstrip capacitance (80-90%). Typical values for the capacitance for a 50 micron pitch detector is 1.2 pf/cm. There is little data on the stability of the capacitance under irradiation. For double-sided detectors the p side is the same as the p side for the single-sided detectors but the n side has the additional complication of an intermediate p implant between the n strips to provide the necessary isolation between n strips. The undesirable result of the intermediate p strip is an increase in the strip capacitance to larger values, possibly to values up to 2 times larger. One manufacturer has told us that by

changes in the silicon wafer processing the additional capacitance increase may be kept to values of only 30 to 50% increase over the p side capacitance [Yam]. It appears possible to design an amplifier that will satisfy the S/N requirement for the p side with a power budget of 1-3mW per strip. However, this power budget presents serious problems to the cooling system and structural design. The increase in the S\N and power for the n side is a potential drawback and leads one to favor all single-sided detectors.

The radiation length for a 300 micron thick silicon detector is .0032. In the GEM silicon tracker we have 6 layers of detectors so that if we use double-sided detectors the total radiation length budget for silicon alone would be .0192 and if we use a sandwich of two single-sided detectors the radiation length budget would .0385. We expect the support structure for the two different options to be comparable. The total radiation length budget for the entire Central Tracker has not been fully determined but we expect it to be about .15 excluding the polyethylene shield. We therefore expect the fractional increase of the radiation length to be about 15 %, i.e. from .13 to .15 depending on whether a 300 micron double-sided detector is implemented or a sandwich of 2- 300 micron single-sided detectors is implemented. The increase in radiation length will be studied by Monte Carlo but it doesn't appear to be a serious problem.

The cost for the silicon detectors depends on the complexity of the fabrication process and the yields from the 4 inch silicon ingot. We have requested quotations from a number of possible vendors who have indicated verbally that the cost of a single-sided detector would be between 2 - 5 times less expensive than a double-sided detector due primarily to the increased complexity in the processing for the double-sided detector and consequently a poorer yield. Since the wafer cost for the silicon tracker is a cost leader, any reduction in the wafer cost would be welcome.

Two considerations lead us to prefer single-sided detectors, cost and capacitance. Radiation resistance appears not to be a determining factor and radiation length is a minor problem. If the cost and capacitance issues can be resolved than our preference would be to use the double-sided option. Additional R&D is needed on the double-sided detector. We believe, however, that the single-sided option is viable and a decision could be made in that direction without degrading the performance of the Central tracker.

12

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2(Kap) J. Kapustinsky, private communication, J.Kapustinsky et.al., FERMILAB- Conf-90/214-E (1990)

(Pit) D. Pitzl et.al., UC Santa Cruz preprint SCIPP 91/05

(Lin) G. Lindstrom, et. al. , Radiation Effects in Si-Detectors and Calorimeter Considerations, FERMILAB Conf 90

(Sai) K. Saito, et.al., Development and Test of Double Sided Silicon Detectors, Nagoya University preprint; K. Yamamoto, private communication.

(Spi) H Spieler, private communication

(Yam) K. Yamamoto, private communication.

(GRO) D. Groom, Radiation Levels in SSC Calorimetry, SSC-229, July 1989

3.2 Mechanical Design

The Silicon Tracker baseline design contains over 8,800 Silicon Wafers which are distributed radially and axially about the accelerator interaction region. Our current Tracker design has an overall length of 2 m and an outside diameter of .7 m. The Silicon Microstrip Detectors are arranged in the volume into three distinct groupings in the tracker; the central or barrel region and two forward planar regions. The total number of Silicon wafers in the Central region is approximately 3,000, with 2,900 wafers in each forward region. The Tracker specifications demand that each of these wafers be precisely located relative to each other and located relative to the interaction region. It is also imperative that the alignment of the wafers relative to each other be exceptionally stable over long periods of time. Sources of instability that will be minimized include: thermally induced strains from heat generation sources such as electronics, dimensional changes with thermal shifts, strains induced by non uniform thermal loading, material property changes due to radiation effects, long term creep, dimensional changes due to moisture or other environmental effects, external vibration sources, and external induced strains.

Figure 1 shows shows The Silicon Tracker Baseline design. The Central Region contains 6 layers of Silicon Ladder assemblies, extending 240 mm axially on each side of the interaction region.

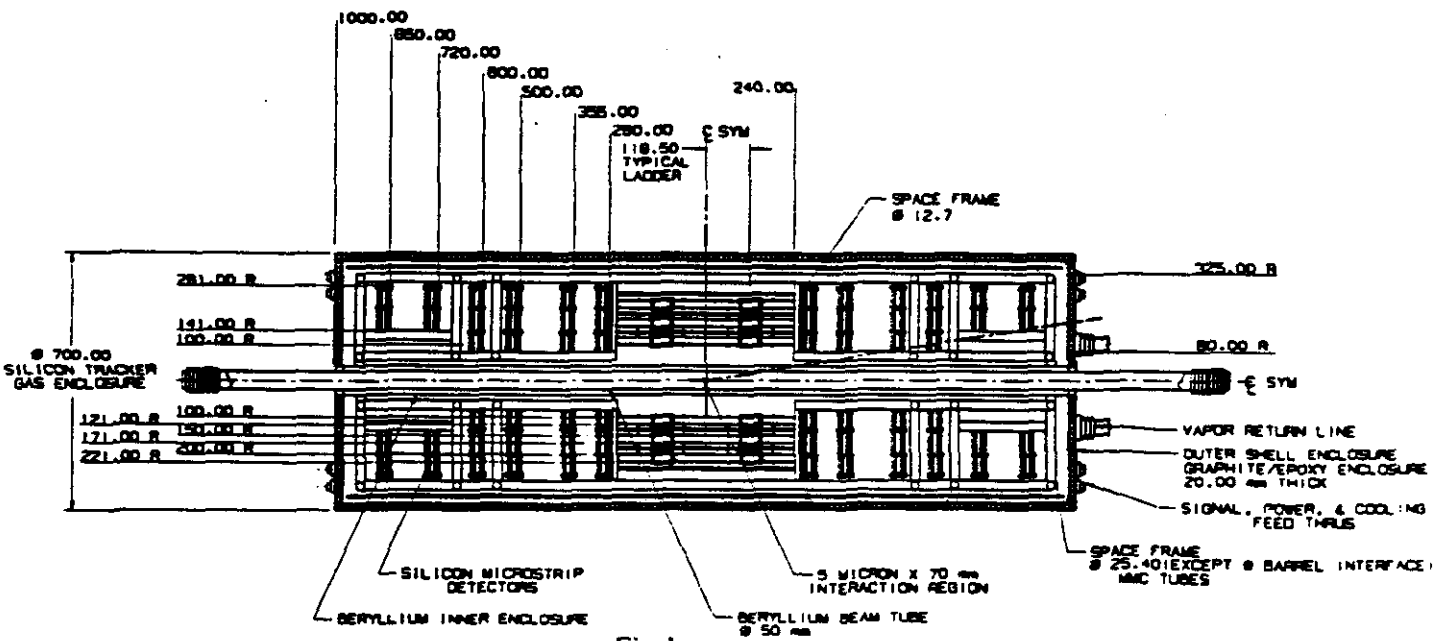

Fig 1

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The radii of each layer as indicated on the figure ranges from a minimum of 100 mm to a maximum of 221 mm. The Forward region contains 12 similar Silicon Ladder assembly layers at each end. These layers are assembled together into 6 superlayers. The Central and Forward region layers are placed so that a single trajectory from the interaction region will intercept 3 superlayers down to an eta coverage of 2.7. A Metal Matrix Composite Space Frame supports and positions the Central and Forward region subassemblies. The entire Tracker is sealed in a Gas Enclosure to contain the Butane, which is the coolant used to remove the heat generated from the electronics. All of the signal cables, power cables, and cooling lines will penetrate the enclosure at the ends.

To meet the high resolution requirements, the individual wafers must meet the following mechanical location tolerances:

Silicon Detector Tolerance	Circumferential	Radial	Longitudinal
Assembly Placement Tolerance	100 μm	50-200 μm	100 - 250 μm
Assembly Optical Inspection Precision	1μm	25 μm 50 μm	
X-Ray Calibration Measurement Precision	1 μm	25 μm 50 μm	
Long Term Relative Stability Tolerance	5 μm	80 μm 250 μm	

The Assembly Placement Tolerance is the requirement for assembling the wafers into a subassembly. Each wafer will then be inspected to the Assembly Optical Inspection Precision requirements. The entire Tracker assembly will be mapped with a highly collimated X-Ray source to the X-Ray Calibration Measurement Precision listed. In order to maintain a high resolution the Tracker subassemblies must meet the Long Term Relative Stability Tolerance. At this point, Long Term is not well defined. The Tracker will be built with a 5-10 year operational life, but occasional recalibrations are expected throughout its life. These calibrations may be in situ or at the surface facility.

3.2.1 Material Considerations (Ref. Superconducting Super Collider Silicon Tracking System Research and Development. LA-12029)

The demanding design requirements for the Silicon Tracker call for the need of specialized high performance materials. The construction materials must have the following

characteristics: low total radiation length, high stability, compatibility with Butane and radiation, specific Coefficient of thermal expansions, and insensitivity to moisture effects. Achieving the design goals will require the application of state-of-the-art material composites with high stiffness to weight ratio construction techniques.

In order to maintain the tight stability requirements, ultrahigh modulus materials with long term stability and radiation compatibility are required. Listed in table1 below are potential material candidates based on high stiffness.

Selected Material Properties							
Material	Elastic Modulus E (GPa)	Density ρ (g/cm^3)	Specific Stiffness E/ρ (10^5cm)	CTE α (ppm/K)	Thermal Conductivity k (W/m-K)	Specific Heat C_p (J/g-K)	Radiation Length (eff.) L_R (cm)
Material Candidates							
Beryllium	290.0	1.84	16.08	11.60	146.0	1.88	35.43
Boron Carbide	448.2	2.52	18.15	4.73	43.0	0.90	19.90
Carbon/Carbon[a]	152.0	1.90	8.16	0.10	246.0	1.00	18.80
Graphite/Epoxy[b]	311.7	1.68	20.00	−1.13	46.2	0.92	25.00
Mg-MMC[c]	190.3	2.03	9.56	−0.35	412.0	1.00	16.80
Al-MMC[c]	196.5	2.39	8.39	0	409.0	1.02	13.22
Reference Materials							
Silicon	**131.0**	**2.33**	**5.74**	**2.60**	**129.0**	**0.70**	**9.37**
Aluminum	68.9	2.70	2.59	23.58	168.0	0.90	8.89
Boron	344.7	2.34	15.03	8.30	1.0	1.29	22.52
Fused Silica	73.0	2.20	3.39	0.50	1.0	0.92	12.30
Copper	117.2	8.91	1.34	16.90	400.0	0.39	1.44
SiC	325.0	3.00	11.05	2.30	200.0	0.89	8.52

[a] Unidirectional properties.
[b] Graphite Fiber (P75)/Epoxy matrix (1939-3), unidirectional, ~60% fiber.
[c] Graphite Fiber (P120) MMC-Metal Matrix Composite, quasi-isotropic, ~60% fiber.

Table 1

The primary candidates are Beryllium, Graphite/Epoxy composites, and Aluminum Metal Matrix composites based largely on ease of fabrication and affordability. Radiation length limits are another primary specification of any construction material to be used in the Tracker. Figure 2 shows the thickness of various material candidates which meet 2% of a radiation length. From a radiation length stand point Beryllium clearly stands out as an advantage, with Graphite/Epoxy as the next optimum. Graphite/Epoxy composites offer the advantage over Beryllium, of being able to have a variable CTE. Where G/E composite structures are bonded to dissimilar materials it is important to match the CTEs to avoid thermal stresses. In other structural applications it is important to minimize the total thermal distortions with zero CTE materials.

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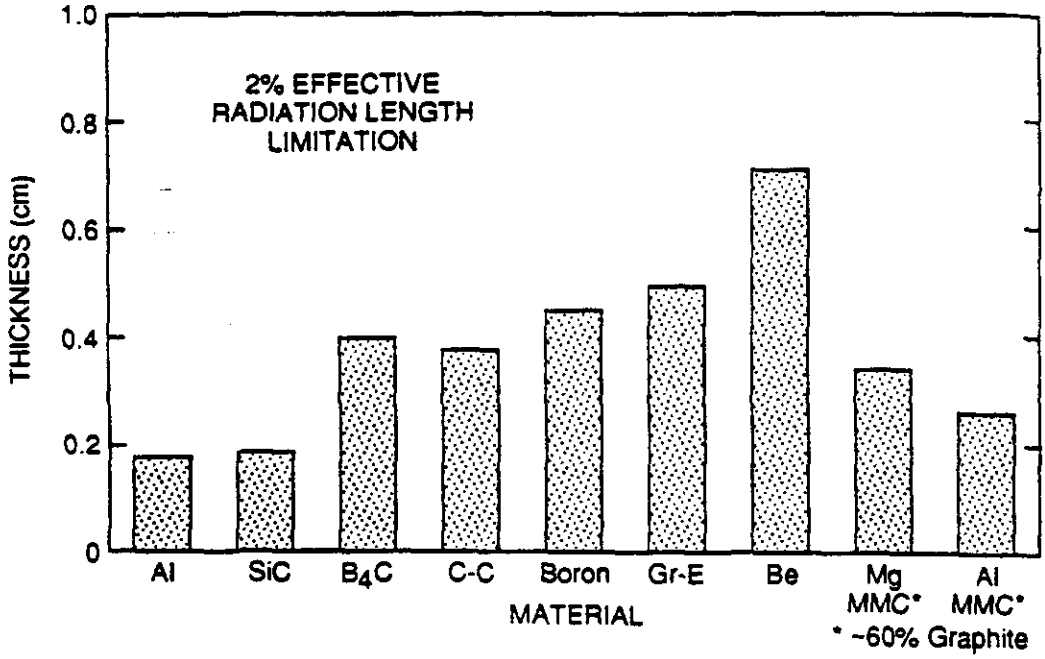

Fig 2

Table 2 shows several G/E candidates considered for the the shell and ring structures for which a quasi-isotropic CTE or silicon matching CTE is needed. Several candidates compare favorably with a silicon CTE of 2.6 ppm/°C. A Graphite /Epoxy composite also offers the opportunity to induce additives into the epoxy binder to modify the thermal conductivity. In critical regions of the cooling ring for example, the transverse thermal conductivity of the G/E composites will be increased to minimize the thermal gradients through the wall.

Graphite/Epoxy Composite Material Systems Quasi-Isotropic Laminate Engineered Parameters

System	Elastic Modulus E (GPa)	Density ρ (g/cm^3)	Specific Stiffness E/ρ (10^8 cm)	CTE α (ppm/°C)	Poisson Ratio ν	Shear Modulus G (GPa)
P75/1939-3	109.2	1.68	6.6	-0.43	0.321	41.3
P75/3501-6	107.8	1.68	6.5	-0.5	0.321	40.8
GY70/3501-6	98.9	1.66	6.1	-0.016	0.318	37.5
UHM3501-6	95.8	1.60	6.1	0.18	0.314	36.4
IM6/3501-6	78.3	1.56	5.1	2.9	0.296	30.2
AS4/3501-6	55.9	1.56	3.7	1.96	0.30	21.5
AS1/3501-6	51.7	1.56	3.4	2.32	0.298	19.9

Table 2

A design consideration with Graphite/Epoxy composites is their higher hygroscopic properties. Beryllium or metal matrix composites present no long term stability issues associated with moisture absorption. Dimensional stability in the Graphite/Epoxy

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composites can be achieved by using a hydrophobic Cyanate Ester binder matrix. Material characterization processes and testing will be carried out to quantify the sensitivity to moisture.

The materials are also required to be compatible in a 100% Butane vapor environment for up to 10 years. Graphite/Epoxy material samples have been fabricated and saturated in the coolant fluids then tensile tested, indicating no apparent incompatibilities. Similar tests need to be performed using the cyanate ester binder in conjunction with a radiation environment similar to the interaction region. Radiation effects on the Graphite/Epoxy structural properties have been carried out on small Truss Core panels. A panel was constructed and measured for flatness prior to radiation exposure. The purpose of the test was to identify any small dimensional changes due to residual stress relaxation, delamination or warping that might occur due to the radiation exposure. After exposure to 3 x 10^{13} neutrons/cm^2, the panel was closely inspected for ply delamination, core debonding, and visible warping, then was reinspected for flatness. No catastrophic conditions were observed. The remapping inspection indicated no relative changes greater than 25 μm which was the initial tolerance of the panel. In the future structural tests will be repeated with the chosen graphite and binder exposed to radiation with a higher tolerance panel structure.

3.2.2 Silicon Wafers

A nominal wafer size of 33 mm x 61 mm was chosen to maximize the use of a 10 cm diameter silicon wafer. Two such wafers will be produced from one 10 cm diameter disk. The baseline design at this time is 2 layers of single sided A/C coupled Totally Depleted Silicon Microstrip Detector with the following specifications:

Active Dimensions:	60 mm x 32 mm
Tolerance:	± 50μm
Thickness:	300μm ± 15μm
Flatness:	± 10μm
# of Strips:	640 (1280)
Strip Pitch:	50 (25) μm
# of Readouts:	640
Readout Pitch:	50 μm
Substrate:	n type, high resistivity silicon

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C(interstrip):	> 5 x C(backplane) < 1.5 pf/cm
C(coupling):	> 10 x C(interstrip)
Depletion Voltage:	< 50 Volts
Maximum leakage/strip:	10 nA
Metalization:	Aluminum
Radiation Hardness:	5×10^{13} neutrons/cm^2 ; 5 Mrad
Strip faults (dead):	< 1% of total Strips
C(coupling) faults:	none

One side of the layer contains axial (x- layer) strips at a 50 μm pitch while the opposite side contains strips at the same pitch but tilted at a 5 milliradian stereo angle. Figure 3 defines the basic features of a typical x- layer wafer. The thickness of each wafer is 300 μm and a maximum width of 33 mm with 640 strips. The strip pitch of 50 μm was chosen as a lower limit for ease of wire bonding. Even at this pitch it is expected that the wire bonding pads will be staggered as shown on the drawing to conform to -standard wire boning machines. Elongated pads or double pads may be eventually incorporated if the need for redundant wire bonds arises.

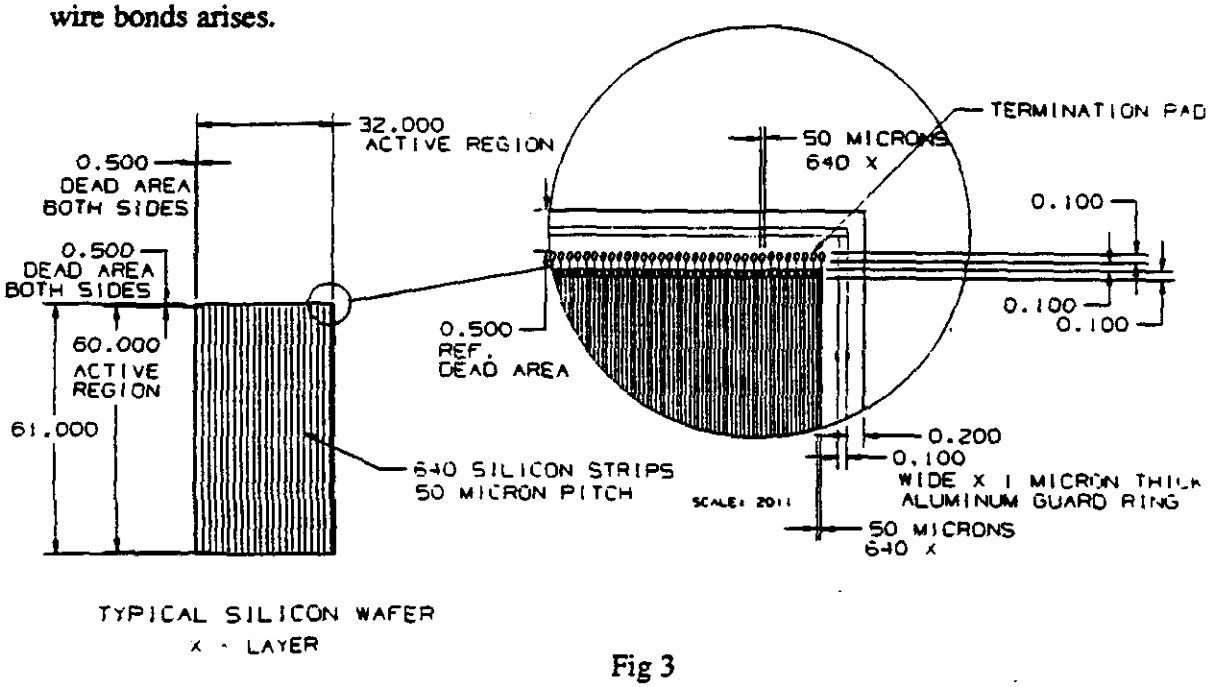

Fig 3

A single or double guard ring with wire bonding pads near the corners would enclose the microstrips. The back plane of the wafer is coated with 2000 - 3000 Angstroms of gold as the conductor for the bias voltage application. Optical alignment fiducials are placed at each corner outside of the guard ring and at the midsections between the corners.

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Features as small as 2 μm wide can be placed on the wafer with a location tolerance to the strips of a few microns or less. The wafers in the central region are rectangular in shape while the forward region shapes are trapezoidal with a maximum width of 33 mm. This uniformity in the width, for both the central and barrel regions, allows us to standardize the electronics packaging design as a cost saving measure. The strips on the forward region wafers maintain a constant 50 μm pitch and do not taper in with the edges; another cost saving measure. The 5 milliradian stereo angle produces a .624 mm wide dead region 12 cm from the readout end, which is covered by overlapping each adjacent wafer.

Preliminary drawings and specifications have been sent to several vendors with requests for technical guidance throughout FY 92. We are requesting cost estimates for both single and double sided detectors, R&D and fabrication planning, as well as technical guidance in improving our design details and specifications. We are asking vendors to itemize the individual cost elements with the intent of identifying production cost savings. We are planning on at least a 1 year R&D effort to refine our design before we engage in another year of joint R&D with a chosen vendor. Compatibility tests between the wafer and selected adhesives in a butane environment will be conducted, including measuring the effects of radiation. Physical measurements of flatness, edge profile and edge to strip dimensions will be conducted on typical production wafers to define specific physical parameters required to assemble the wafers. During the R&D effort with the vendor Photo masks will be produced and prototypes will be fabricated and tested to our standards as a confirmation of meeting our design specifications.

3.2.3 Silicon Ladder Assembly

Two Silicon Wafers are bonded edge to edge to form a 12 cm long ladder that will be read out at one end. In the forward region some of the ladder lengths may be single wafers as short as 4 cm. In the central region the two ladders are bonded end to end and back to back to form a 24 cm long ladder assembly. As shown in figure 4, the electronics are mounted at each end where the strips are read out. The edges of the Silicon Ladder are structurally reinforced with thin Graphite Epoxy rails to increase the transverse stiffness of the assembly. Fundamental to this design, is the plan to carry the fabrication, assembly, and testing of the individual components in parallel as far as possible. This will provide a little relief in the schedule since these are in the critical path, but most importantly this will allow for individual component testing prior to final assembly commitment.

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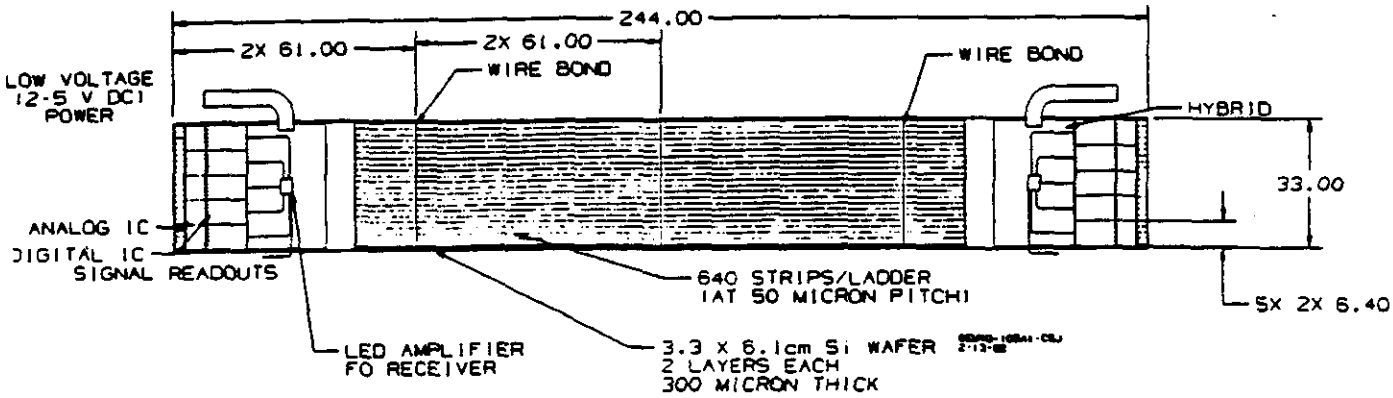

Fig 4

The first step in the assembly is to perform the end to end mechanical bonds of the 24 cm ladder then proceed to the wire bonding. The Silicon wafer strip surfaces are expected to be very thin and delicate, this drives us to do the wire bonding prior to bonding back to back, otherwise the wire bonding pressure would be transferred to the lower facing causing possible damage.

In parallel, the Front End electronics packages would be fabricated and qualified through testing prior to being committed to the wafer assembly. Mounting the electronics directly on the face of the wafer presents a possibility of damaging the very thin (1 μm) SiO_2 coating. Prototype tests will have to conducted during the R&D phase to develop procedures and techniques for the assembly step. The analog, digital and hybrid assembly would be assembled and wire bonded on this platform prior to testing. This assembly will also contain the ribbon cable which delivers the electronics power, timing and calibration signals, and bias voltage for the wafer. We have chosen to attach the cable to the side of the electronics subassembly for several reasons: the cooling ring locally provides adequate wafer transverse stability, ease in the routing down to the ring bus, and keeping the ends free for the final wire bonding to the wafer assembly.

Once this assembly has been qualified it will be mechanically bonded to the wafer assembly and wire bonded to the strip pads. At this stage of the assembly there is the opportunity for additional systems tests before proceeding to the back to back assembly. The back to back assembly will require accurate lateral positioning of the X and Stereo layers. Several techniques will be investigated during the R&D phase, along with prototype assembly tests and evaluation.

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Details of the electronics mounting are shown in figure 5. The major components of each electronic subassembly are: five 128 channel Analog IC chips, 5 Digital IC Chips, a Hybrid circuit assembly and a LED signal transmitter, all mounted on a field plate. Listed below are some of the required thermal and structural design specifications:

Maximum Ladder assembly distortion	< 100 μm
(including gravitation effects, thermal distortion and externally induced strains)	
Maximum Electronics Operating Temp.	35° C
Maximum Wafer Temperature	5 °C

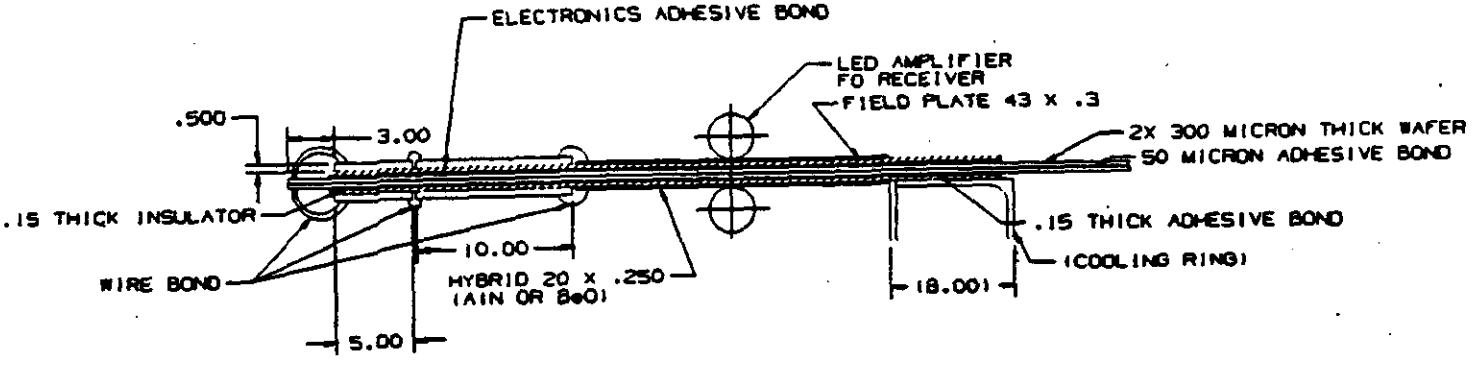

Fig 5

Sources of heat generation are the Analog IC Digital IC and the LED signal transmitter. The specifications for the heat sources are :

Front End Electronics -	total power 3.99 W/Ladder end
2.5 - 4 mWatts/strip	(60%in Analog IC,40% in Digital IC)
Analog IC Area -	5 chips .5 cm x .64 cm .32 cm^2 each
An. Power Density -	128 strips x 60% x 3 mW/.32 cm^2 1.2 W/cm^2
Digital IC Area-	5 chips 1.0 cm x .64 cm .64 cm^2 each
Dig. Power Density-	128 strips x 40% 3mW / .64 cm^2 .24 W/cm^2
LED Readout Driver-	150 mW each
Cooling Ring Power Density	

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3 mW/strip x 1280 strips + 150 mW LED / 2.23 cm^2 = 1.8 W/cm^2

The material selection of the platform on which to mount this electronic assembly is strongly driven by the need for good thermal conduction to the heat sink. 300 µm thick Aluminum was chosen as a starting point for a thermal study based on the above design. As a heat source, 3 mW / channel + one 150 mW LED were assumed. Figure 6 shows several thermal profiles through the electronics assemblies for multiple conduction path options. Case 4 is the initial calculation for this design. The dominant thermal resistance between the heat sources and the cooling ring is the long conduction path through the wafers and Aluminum field plate. This large resistance builds up a thermal gradient of about 20 °C through the Silicon Wafer. Two other prominent thermal gradients are due to the conduction resistance of the graphite cooling ring wall and a convection resistance due to the evaporative film heat transfer coefficient. These thermal resistances raise the Wafer temperature up to 35° C, which is unacceptably high.

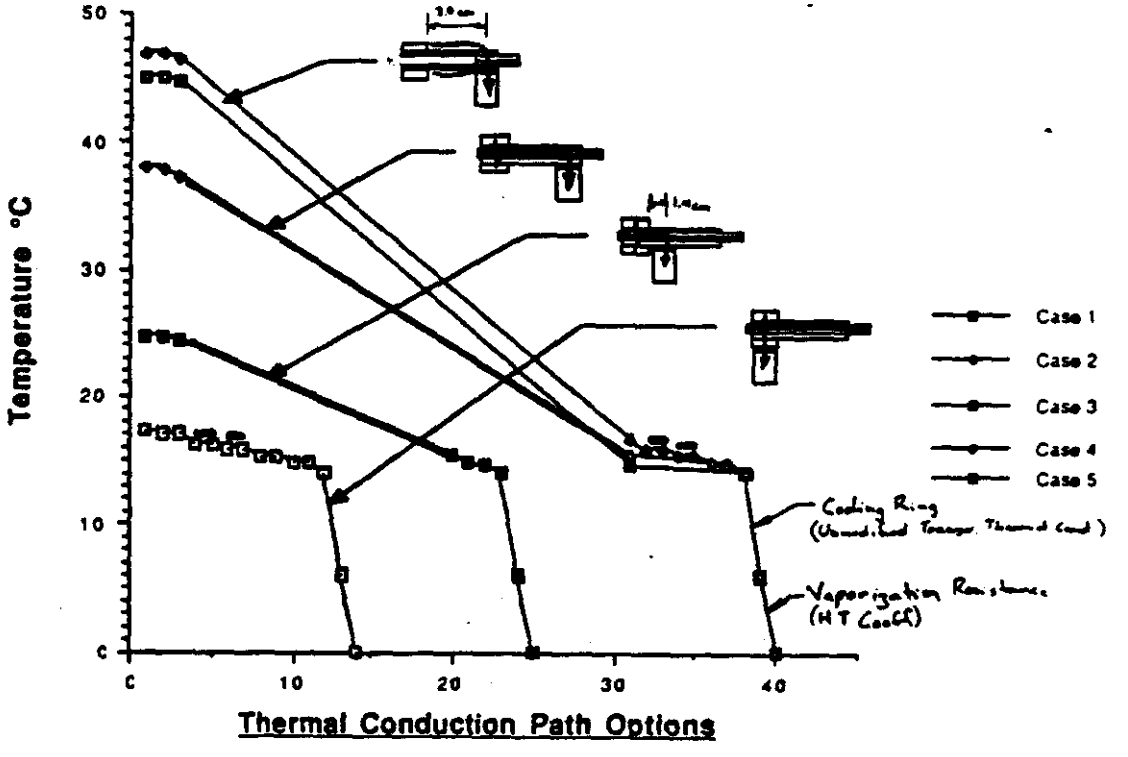

Fig 6

One option for lowering the wafer temperature is to thermally isolate the wafer from the heat sources with a small gap between the Aluminum plate and Wafer. The plate would be bonded to the wafer just above the cooling ring to allow conduction to the heat sink. This resultant thermal gradient is plotted as Cases 2 & 3, showing a thermal gradient along

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the length of the Aluminum. This resistance is due to the long conduction length and small crossectional area. The advantage to this design is that the Silicon Wafer is on the low temperature side of this large gradient, at about 18 ° C. The disadvantage is that the electronics are at the high end of the resistance at 45° C; unacceptably high.
Moving the cooling ring closer to the heat sources reduces the thermal resistance path as shown in case 5. However this would place the ring on top of the Hybrid circuit. We are currently in the process of further refining our design to establish this feasibility.

If it were possible to eliminate the thermal resistance along the plate, a thermal profile as shown in Case 1 would result. The dominant resistances now become the graphite cooling ring and evaporative film resistance. The transverse thermal conductivity of the cooling ring is dominated by the epoxy matrix. An effort is underway to modify this by inducing small amounts of higher (100 times) conductivity additives to the epoxy binder. Other options include penetrating the cooling ring wall with small size, higher conductivity elements which will allow for lower resistance parallel conduction paths. The resistance at the evaporative interface is dependent on the evaporative heat transfer coefficient and heat flux. Increasing the area over which the evaporation takes place is one key to reducing the thermal gradients. A more detailed analysis may indicated that the cooling ring higher inplane thermal conductivity may adequately dissipate the heat flow.

Several options for stiffening the wafer in the transverse direction have been considered, to minimize the lateral deflection and increase the natural frequency. Small thermal gradients, gravity, cooling ring induced strains, and external vibration are potential sources that contribute to the wafer distortion. The ladder assembly stiffness will be increased by the addition of thin graphite/epoxy side rails, which will be edge bonded to the wafers. The graphite/epoxy rails may be as high as 4 mm with a thickness of .4 mm, and bonded the full length of the ladder except at the cooling ring attachment. Figure 7 contains several plots of wafer deflection versus unsupported length for various ladder parameters. The first curve shows the deflection of a single 300 μm thick wafer simply supported at the edges. Our baseline design calls for two 300 μm thick wafers bonded back to back. Curve 2 shows a factor of 4 decrease in deflection due to the increased bending stiffness. The further decrease in deflection due to the addition of the rails is shown in curves 3 and 4. It should be noted that the two layer wafer configuration deflects more than the single wafer since the additional weight is distributed in such a manner that it does not greatly contribute to the lateral stiffness. The rails will be constructed of graphite/epoxy matrix with a closely matching CTE to that of silicon, and will be structurally symmetrical about the neutral bending axis to

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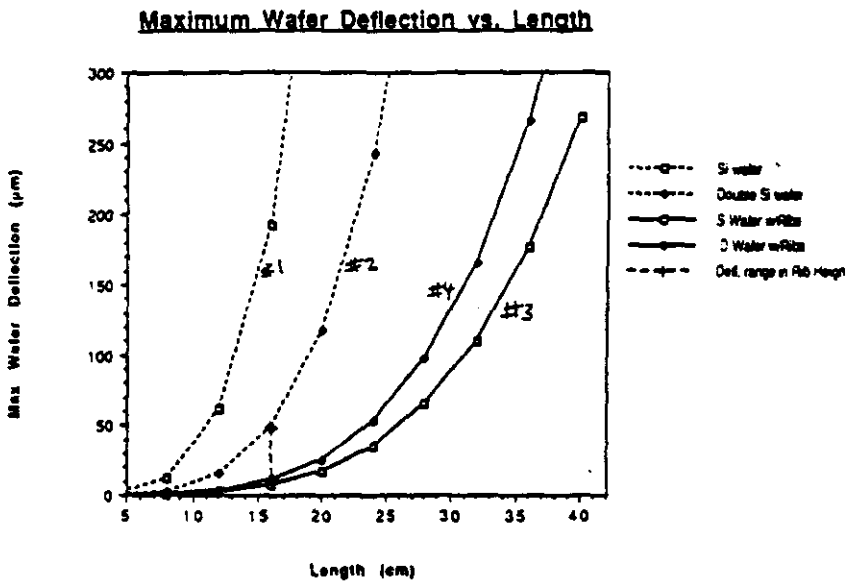

Fig 7

minimize unbalanced thermal distortion of the wafer. Rail interference with adjacent wafers may occur in packaging the wafer and electronics on the cooling ring at small lorenze angles; particularly in regions of the wire bonding. This may necessitate the use of lower height rails or some other stiffening mechanism. Figure 8 shows the effect of rail height on the wafer deflection for rail heights up to 4 mm, for a simply supported 16 cm long assembly. At rail heights of less than 1.5 mm the increase in bending stiffness is not substantial.

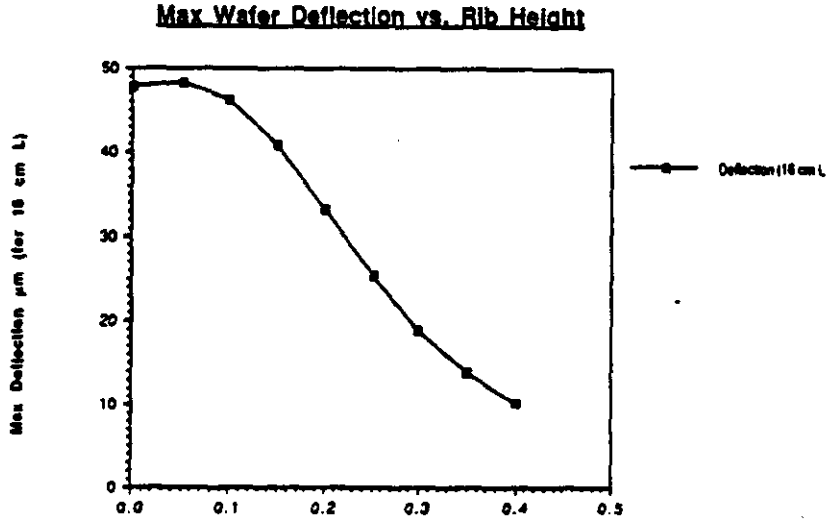

Fig 8

At this point we have not developed an acceptable ladder design to meet the thermal and structural specifications. Further design studies, detailed thermal and structural analysis are required to develop an acceptable baseline design. Prototype design, assembly and

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testing will be conducted throughout the R&D phase to more closely evaluate the options. In mid 1992 a small Silicon Microstrip array may be tested in support of the Texas Test Rig, in which case we will have an opportunity to instrument a working device to benchmark our thermal/structural calculations.

3.2.4 Central Region Subassembly

The Silicon Ladder assemblies are grouped into superlayers consisting of two Ladder layers. There are 3 superlayers radially, in the Central Region which are separated by Graphite/Epoxy support cylinders (refer to GEM Silicon Tracker working Layout). Each superlayer is segmented into either 24 or 12 cm long Shell Assemblies, which are multiples of the ladder lengths. By standardizing the components, the additional cost of custom sizes is eliminated. There are a total of 12 Shell Assemblies; 3 forming the inner super layer, 4 forming the mid super layer, and 5 forming the outer super layer. Figure 9 is a detail of one end of a typical Shell Assembly. The ends of the 24 cm long Ladder assemblies are mechanically bonded to the inside and outside diameter of Graphite/Epoxy Cooling rings. In addition to providing the mechanical support for the Ladders, the hollow cooling ring provides the passage for the wick coolant distribution, and the external surface will contain the signal readout and power distribution bus.

The cooling ring wall thickness and cross sectional height must be minimized from a radiation length consideration, but must be structurally stiff enough to provide adequate

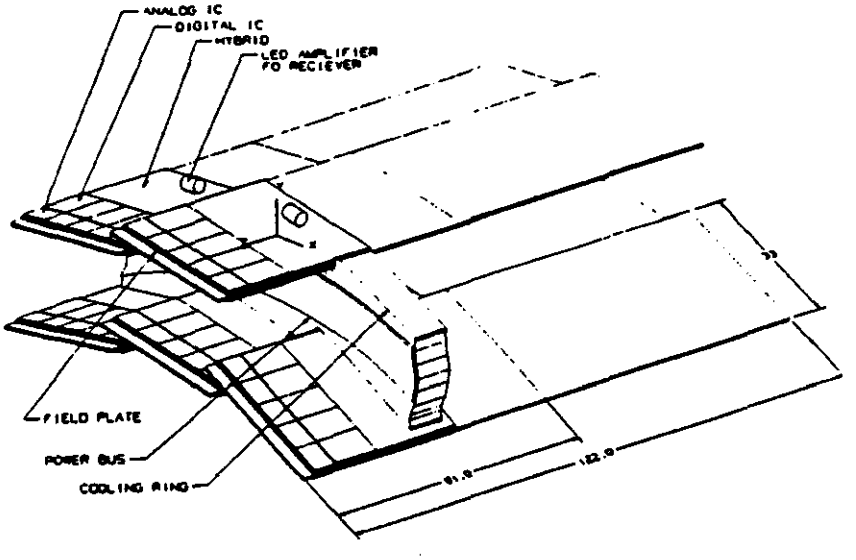

Fig 9

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stability to the ladders. A cross section of the cooling ring is shown in Figure 10. The design requirements for the central region of the Tracker require a very low profile cooling ring with a minimal radial spacing between super layers. The current ring design is based on a wall thickness of .4 mm and height of 2 cm, with outer radii of: 12, 15, and 22 cm. Detail structural analysis has yet to be done to verify the structural stiffness of the design.

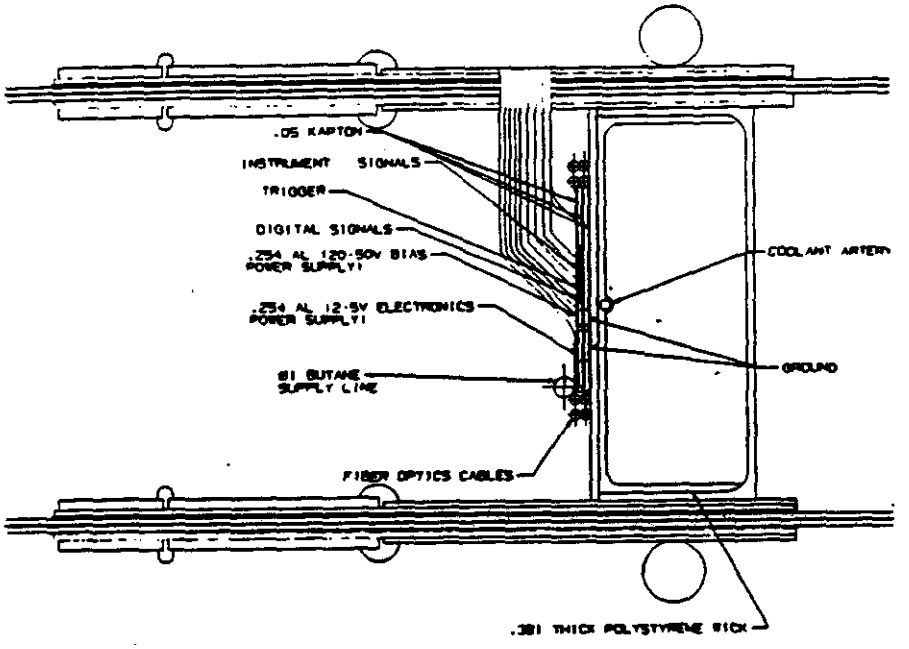

Fig 10

The material of choice is molded graphite/epoxy for many reasons. The Graphite/Epoxy composite formulation will have to match the CTE of the silicon wafers to prevent inducing undesired thermal strains in the detector. The material also provides high stiffness at low radiation lengths and is reasonably priced. Fabricating the rings by compression molding with a chopped fiber epoxy filler is one cost effective method of producing this complicated, high precision, muti-surfaced geometry. A significant portion of the cost is in developing precision dies and molding procedures that will yield accurate and reproducible rings. In our baseline design we have minimized the number of molds to 2 for each super layer or 6 total. Once the molds and procedures are qualified the actual production costs are modest. A G/E chopped fiber material also provides the opportunity to modify the thermal conductivity to reduce the thermal resistance.

The Ladder assemblies will be tilted as much as 9° from tangent to allow for adequate wire bonding and power cable routing clearance, as shown in figure 11.

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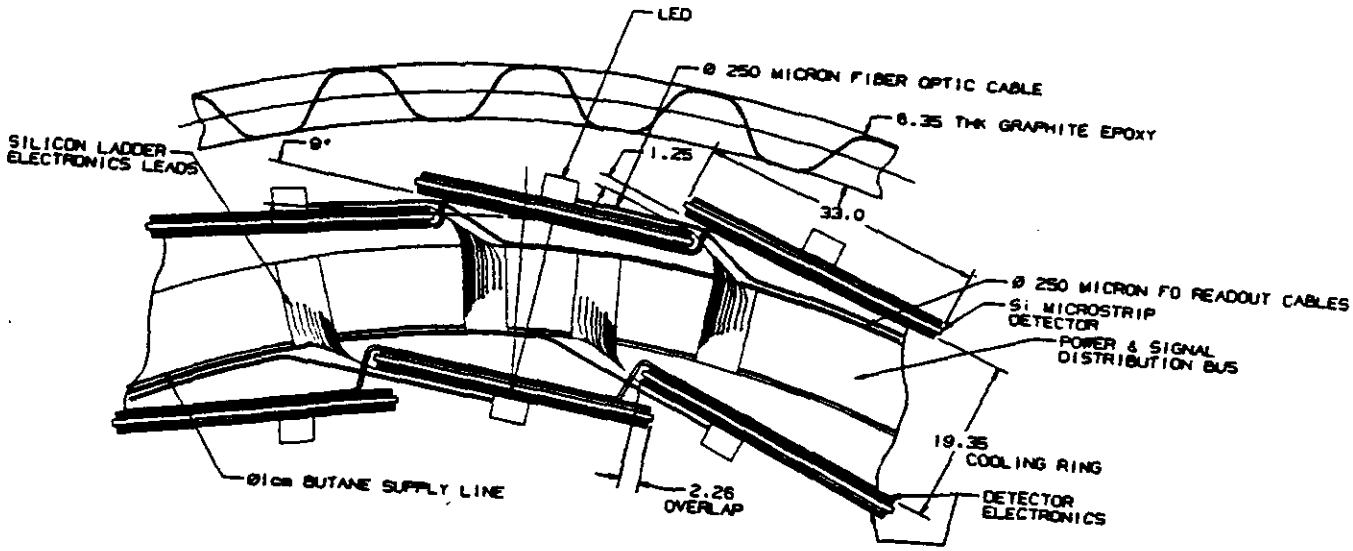

Fig 11

Shown in the figure are two super layers separated by a graphite/epoxy support cylinder. The Ladders are bonded to the top and bottom of the cooling ring and overlapping at the edges. The minimum edge to edge overhang is set by overlapping the inactive regions of the wafer, the inactive region due to the stereo strips, and 5 strips to assure detector coverage. The minimum overlap is 1.9 mm with a tolerance of ± 100 μm, established by a maximum overlap of 7 strips and a minimum of 3 strips. The actual overlap will be established for each layer by keeping the nominal wafer width constant.

Mounted on the outer edge of the cooling ring will be a compact laminated power and signal distribution bus. This small area will contain the 2 - 5 Volt electronics power supply, 50 Volt wafer bias supply, 7 Volt LED power supply, Digital and Trigger signals, thermal instrumentation, transmitting and receiving FO cables, in situ alignment FO cables, and grounding plane and shielding. The ribbon cables attached to the Ladder electronics will be routed down in between the overlaps and connected to the power bus. The design of the ribbon cable to bus connector will require substantial R&D to develop a low radiation length, multi-connector, detachable connection.

The current baseline design incorporates the use of one LED or less per Ladder assembly end. The minimum bend radius for the 250 μm Ø fiber optic cable is 5 cm R., which will require a series of gradual bends from the LED into the cooling ring.

Each Shell Assembly will be supported off of a graphite/epoxy cylinder, designed with an ultra-light truss core design. The baseline design thickness is .635 cm, the diameter and length vary with the 3 shells as shown in figure 12.

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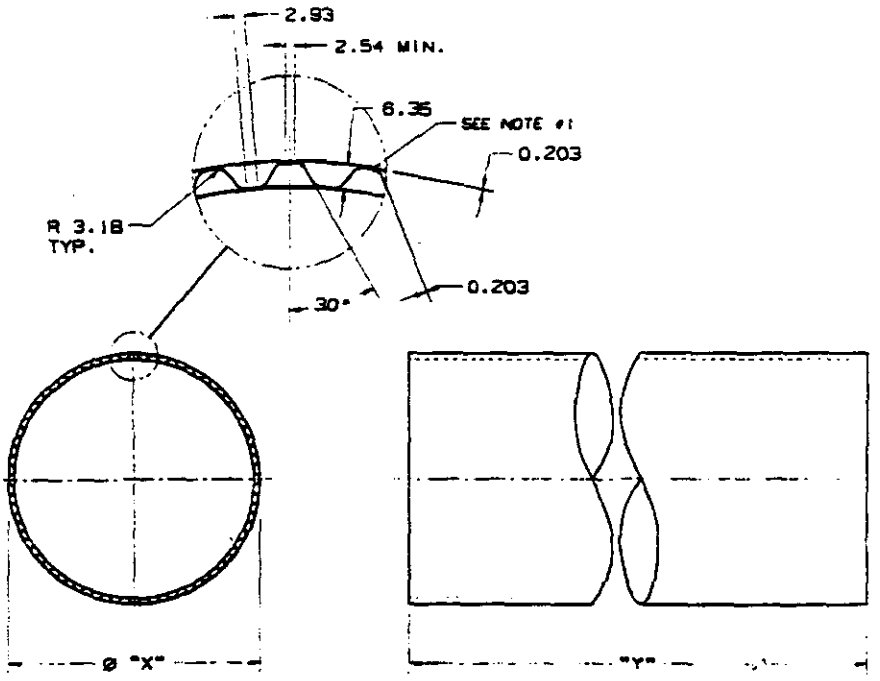

GRAPHITE/EPOXY CYLINDERS		
	DIAMETER "X"	LENGTH "Y"
INSIDE CYLINDER	138.68	480.00
MIDDLE CYLINDER	193.68	720.00
OUTSIDE CYLINDER	253.68	960.00

Fig 12

The laminate thickness chosen is 8 layers of .001" thick plies to minimize the radiation length. At this truss core thickness, the optimum core geometry is between 45° and 65°, in order to minimize the static deflection. 45° is chosen as a baseline design to initiate fabrication drawings and cost estimates. The Shell Assemblies will be kinematically mounted to the cylinders at 6 locations. Three kinematic mounts located 120° apart will be attached to the Shell Assembly cooling rings at each end to structurally isolate the assembly from thermo-mechanical strains induced by the cylinders. The kinematic mount transition from the ring to the cylinder may require small discrete openings through the Silicon Ladder ends. These openings would also serve as a path to route the the power and signal distribution bus from the ring to the exterior of the shell assembly.

Structural analysis of the cylinders will have to be performed to confirm the adequacy of the truss core thickness and to understand the thermo-mechanical distortions due to the temperature shifts as well as non uniform thermal distributions.

Considerable design effort will be required to develop a low radiation length, compact kinematic mount that can be blindly assembled into a cylinder. Very little is understood at this time about the detailed assembly sequence and cable routing of the Central Region Shell Assemblies.

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3.2.5 Forward Region Planar Subassemblies

Design details of the Forward Region Planar Subassemblies are not as well advanced as the Central Region designs. The design specifications for wafer stability, operating temperature, wafer overlap, signal and power cable routing are basically the some, so the same design philosophy will be incorporated. Figure 13 shows the major features of the Forward Region Assemblies. The wafers will be tapered from a maximum of 33 mm wide down toward the centerline, with ladder lengths of 4,6 or 10 cm. In future, a more efficient layout of the tapered geometries on the 10 cm Ø production wafer will probably allow us to use a slightly longer wafer. Identical electronics packages are mounted at the readout end of the wafers. Structural support for the ladders will come from an inner and outer ring constructed of low mass graphite epoxy with 3 interconnected spokes at 120° apart. Kinematic mounts would be installed at the ends of the spokes and attached directly to the Space Frame.

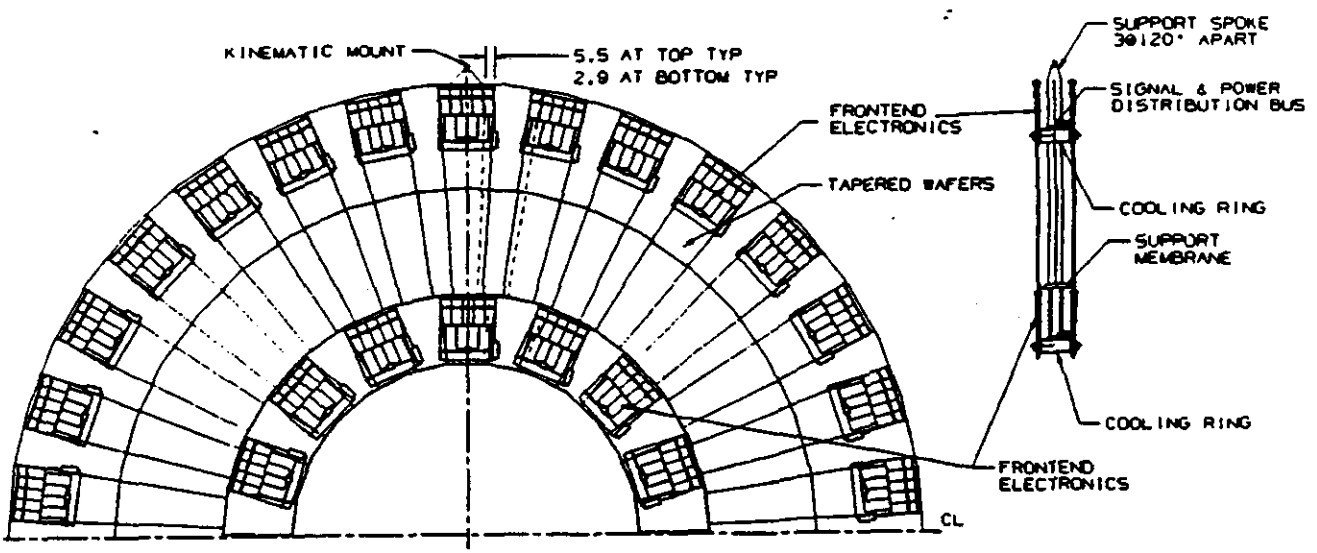

Fig 13

The Forward Region assemblies are grouped into super layers in a similar manner as the Central Region. A minimum number or different inner and outer radii are preferable to minimize the construction costs. The axial placement of the layers is established to maintain 3 super layer intercepts by any ray originating at the IR. Ladders would be alternately bonded to the cooling rings front and back with a 5 strip overlap at the edges. The outer edges of the Ladder Assemblies would be bonded over the cooling ring in much the same manner as the Central Region Ladders. However the inner edges would be attached to small

radially flexible members that would allow for differential thermal expansions due to small mismatches in CTE. Design concepts for the Forward Region have been established, detail thermo-mechanical models will confirm the design concept and help refine the many design details. Details of the coolant distribution, power and signal cable routing are not well established at this time. With the assistance of AT&T, we are beginning to layout the major components of the Fiber Optic readout system. We are asking for technical assistance in radiation hard fiber optic cable technology, Fiber Ribbon connector technology, and fast rad hard LED technology. Figure 14 shows the major mechanical components of the fiber optic readout chain.

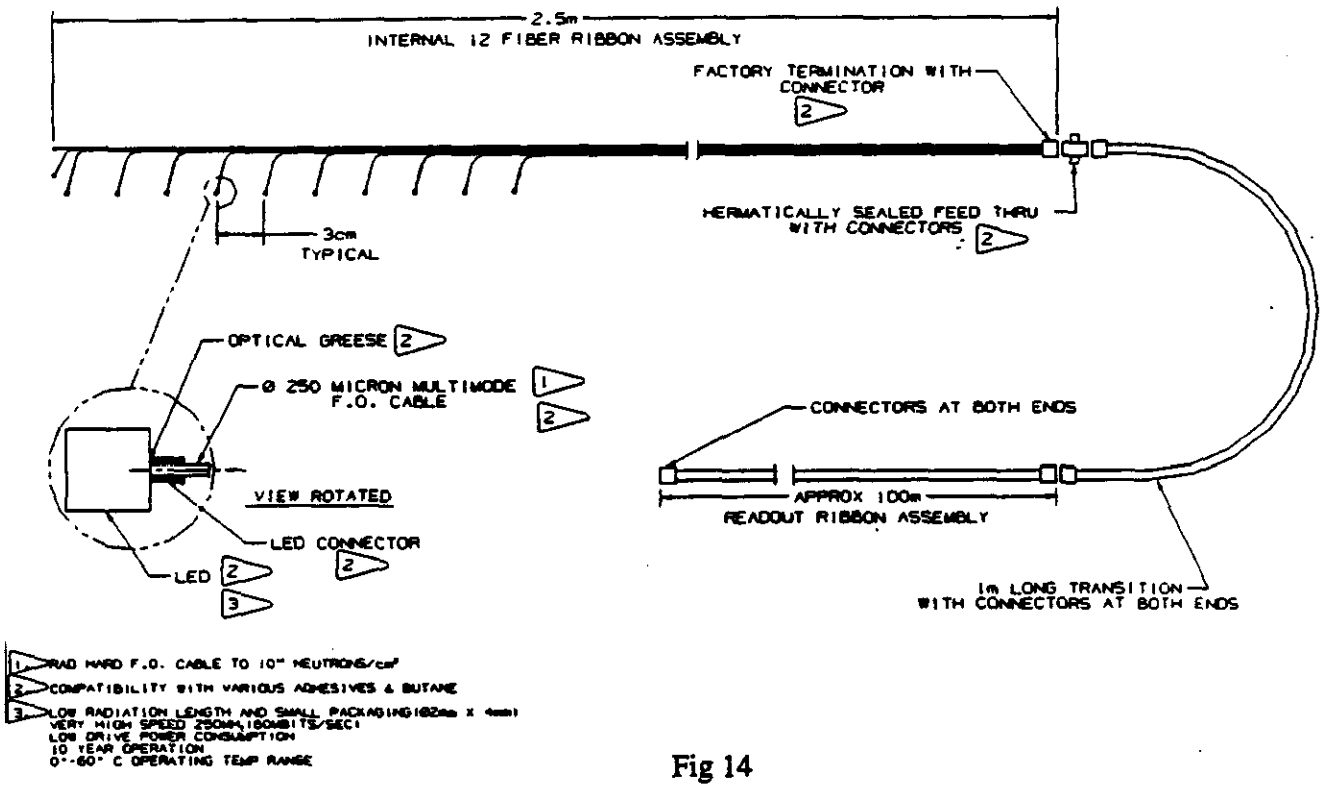

Fig 14

Our proposal is to procure a series of Internal 12 fiber Ribbon Assemblies including factory terminations with a ribbon connector at one end and individual LED connectors at the other ends. A 1 meter transition piece is required to get from the enclosure feedthru to the outside of the IPC Tracker; this will minimize the amount of cable to be attached to the Tracker during assembly. Larger numbers of FO Ribbon cables will be bundled in protective insulators for the 100 meter up run to the surface facilities. The major weakness of the design is the lack of a fiber optic feedthru. This design task presents a major R&D challenge to develop a low radiation length, compact feedthru with connectors at each end to precisely align the fiber optic cables. The design must include materials compatible with various adhesives, butane, and radiation and must contain a double seal for the Butane gas.

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3.2.6 Truss Space Frame

The Central and Forward Planar Subassemblies will be installed into a low mass, highly stable space frame that is capable of maintaining their relative alignments for long periods of time. The design requirements for this space frame include: Butane vapor compatibility, Radiation compatibility, thermal stability, low creep, ease of assembly and installation. Aluminum Metal Matrix Composite material adequately meets the requirements. The material has a high elastic modulus with an acceptable radiation length, it has no moisture sensitivity, and can be modified to a near zero coefficient of thermal expansion. Figure 15 shows a design concept for supporting the Central and Forward Subassemblies.

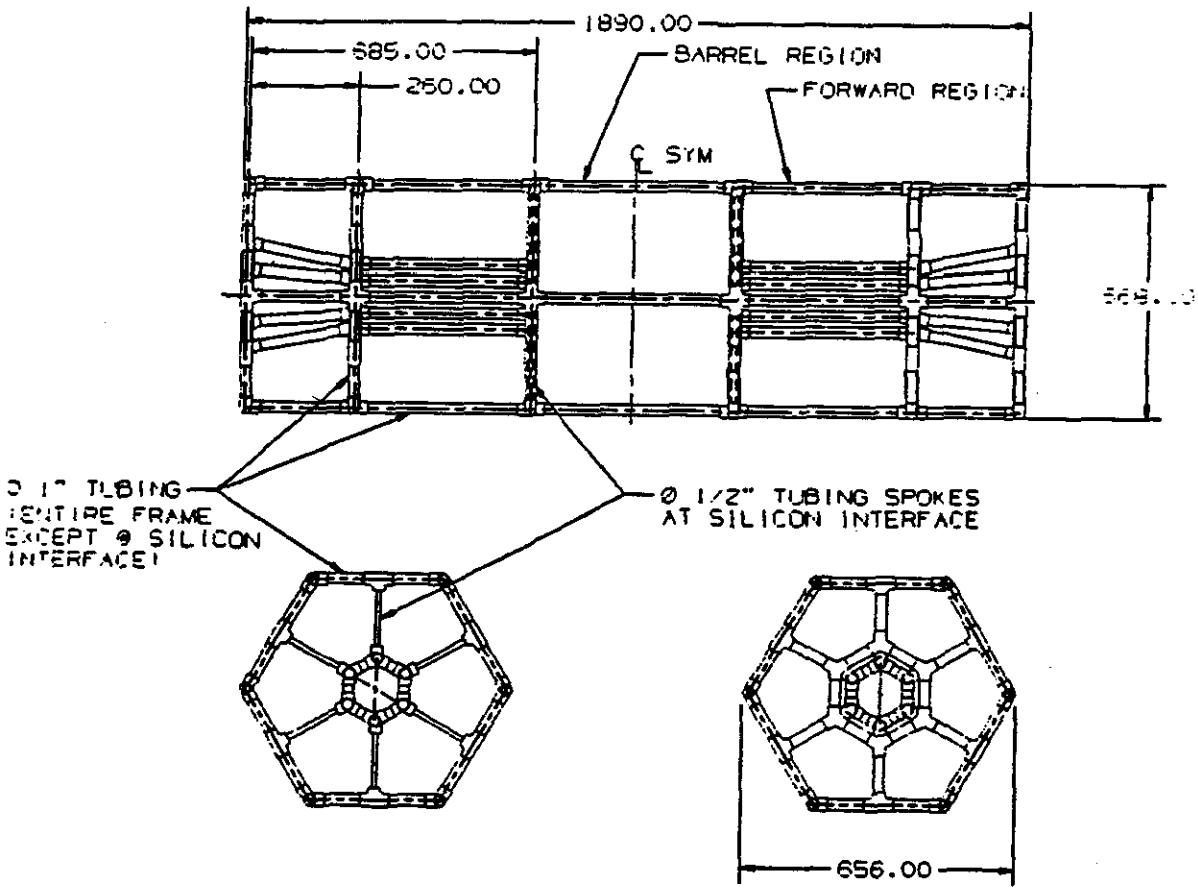

Fig 15

The design is an open frame with hexagonal cross-sections connected by longitudinal stringers. The frame is constructed of thin walled 1" Ø tubes bonded into various types of connectors. The design must include the ability to assemble and

disassemble the frame for maintenance access to the center of the detector. The central to forward region taper has been eliminated in favor of the truncated cylinder design, for cost and assembly advantages.

A near zero CTE frame is required to minimize the thermal distortion due to the cool down of 20° C from assembly to operation. This will minimize the motion of the Central and Forward subassemblies relative to one another. In addition, the subassemblies will be kinematically mounted to the frame to isolate them any thermal distortions. Very little detailed design of the Space Frame will be done until the general Tracker configuration is well understood. No structural analysis has been done to date to verify the design. FEM analysis will be required to determine the tube diameter and wall thickness, maximum load deflection, vibration modes and natural frequency, and mounting points.

3.2.7 Gas Enclosure

A gas enclosure system will be required to contain the Butane vapor and prevent external gasses from contaminating the butane coolant. Unlike the previous structures, the gas enclosure will be designed for strength rather than stability. The space frame attachments will penetrate the gas enclosure at the ends and attach directly to the mounting bulkheads. Figure 16 shows the enclosure design that must meet the radiation

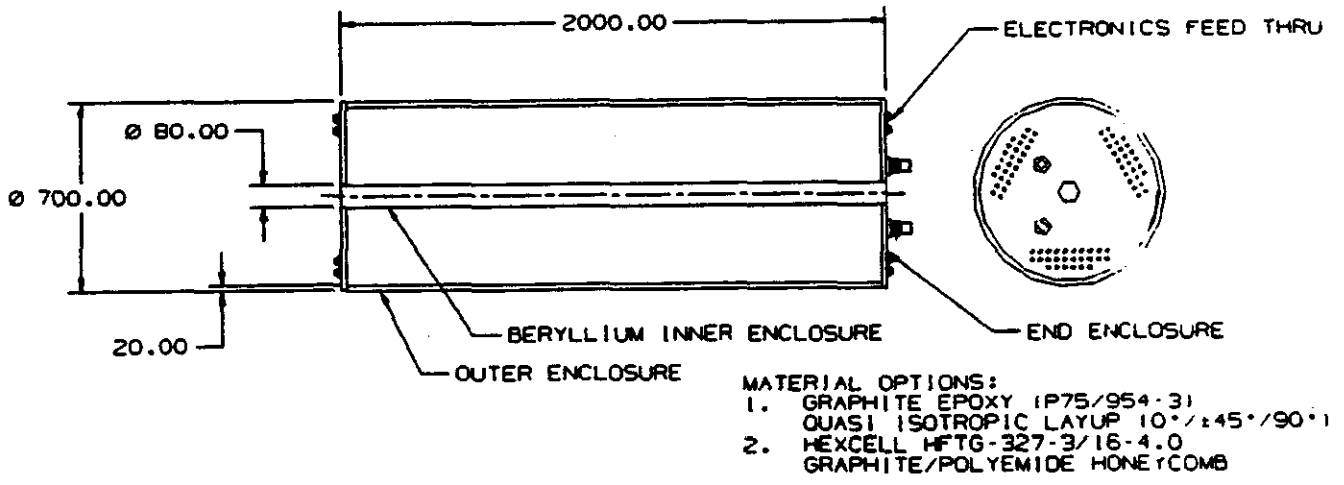

Fig 16

length requirements and be capable of withstanding an atmosphere of external and internal pressure. At operating conditions the pressure will be regulated by the cooling system at

close to atmospheric pressure. Relief valves and controls will be added to the system to ensure the pressure does not exceed the enclosures maximum working conditions.

The outer shell enclosure will be constructed of a single sandwich Truss Core design to minimize the stiffness, with graphite/epoxy materials to meet the radiation length requirements. A structural design to withstand the outside pressure will require the cylinder to be stable against buckling. This may require the addition of circumferential stiffeners to increase the strength of vessel. The inner enclosure will be constructed of all Beryllium to minimize the radiation length or an Aluminum /Beryllium combination to minimize the cost. Removable ends will allow access to the ends of the Tracker where the utilities and signals pass through the gas enclosure.

A secondary gas enclosure is required as a buffer zone for any potential butane gas leak. The double wall truss core design will allow for a layer of flowing Nitrogen gas that will contain a Hydro Carbon sensor. Any leak of the primary gas enclosure will be sensed and contained in this secondary enclosure. The end enclosures will sealed with double o-rings, having the same Nitrogen gas system between the o-rings. In addition, all of the feedthrus will penetrate through the ends with double o-ring seals.

Future work will include detailed designs of the enclosures and the secondary containment, and double o-ring seals. Structural analysis will be required to design in the stability against buckling, and the strength to withstand internal pressurization.

3.2.8 Beam Tube

A vacuum Beam Tube of 5 cm in diameter will penetrate through the center of the Silicon Tracker and be attached to extensions on either end. The vacuum beam line diameter must be large enough to optically align through during the installation phase, and may be misaligned by as much as 3 mm from the centerline. The beam tube must be constructed with a minimum radiation length for eta values < 2.7 and flanges must be kept within eta values > 3.0. The beam tube leak rate and cleanliness specifications will be determined once the system pumping configuration is better defined. A vacuum level of between 1x10-7 and 1x10-8 torr will be required at the interaction region, which will require a vacuum bakeout of the tube after installation. Figure 17 shows the baseline design for an all Beryllium Beam Tube through the Silicon Tracker. An inner diameter of 5 cm and a wall thickness of .020" is chosen as a baseline design, with each end of the beam tube mechanically isolated with bellows.

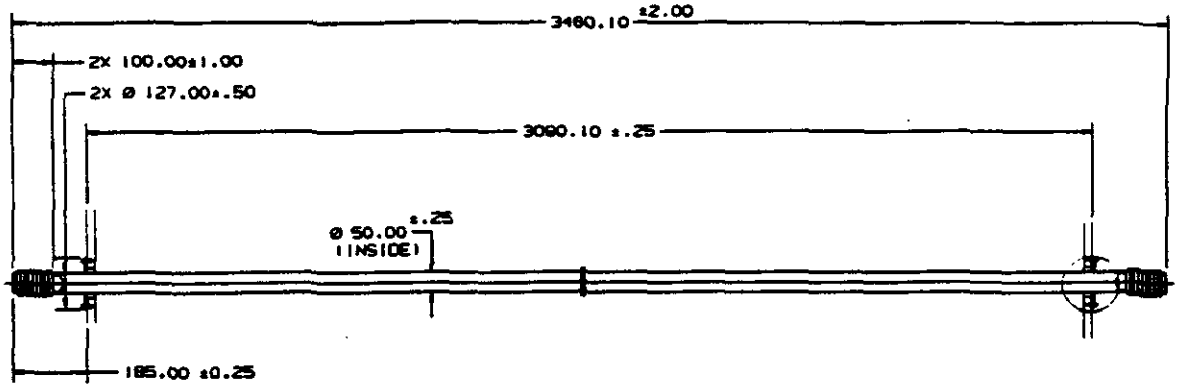

Fig 17

An optional design might be to transition to an Aluminum section at about 30 cm from the center point and then on to Stainless Steel. Other options under consideration include tapering the Aluminum transition outward in a conical geometry. A series of buckling calculations have been performed to map out the various parameters including materials, diameter and wall thickness. Figure 18 is a plot of critical buckling pressure vs. wall thickness for .4, .98, and 2 inch radius tubes of Beryllium S200E, Aluminum 5052, and Stainless Steel 304L. It should be noted that these values are for long, near perfectly round cylinders; out-of-roundness tolerances will be discussed later.

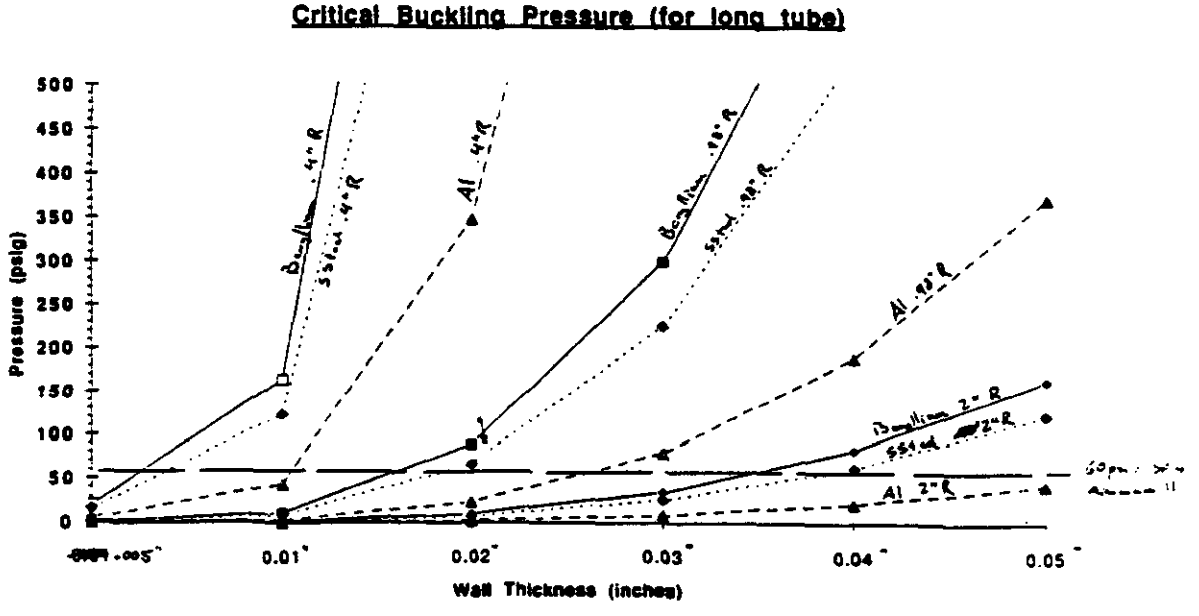

Fig 18

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The horizontal line at 60 psi represents a safety factor to buckling of 4. A safety factor of 4 is considered to rated as "mansafe" for a ductile material presenting a minimal hazard. To meet this specification one must select parameters that are above the 60 psi line. Our baseline design of .98" radius and .020" wall with Beryllium is indeed above the line.

Radiation calculations may indicate a need to further reduce the wall thickness. To offset the decrease in wall thickness, the critical buckling pressure may increased by altering the buckling mode shape. This can be accomplished be adding circumferential ribs at specific axial intervals. The increase in buckling pressure is shown in figure 19. As the rib to rib interval is decreased, the critical buckling pressure is constant up to about 10 tube diameters. At this point the ribs begin to alter the mode shapes and drive the critical buckling pressure to higher values.

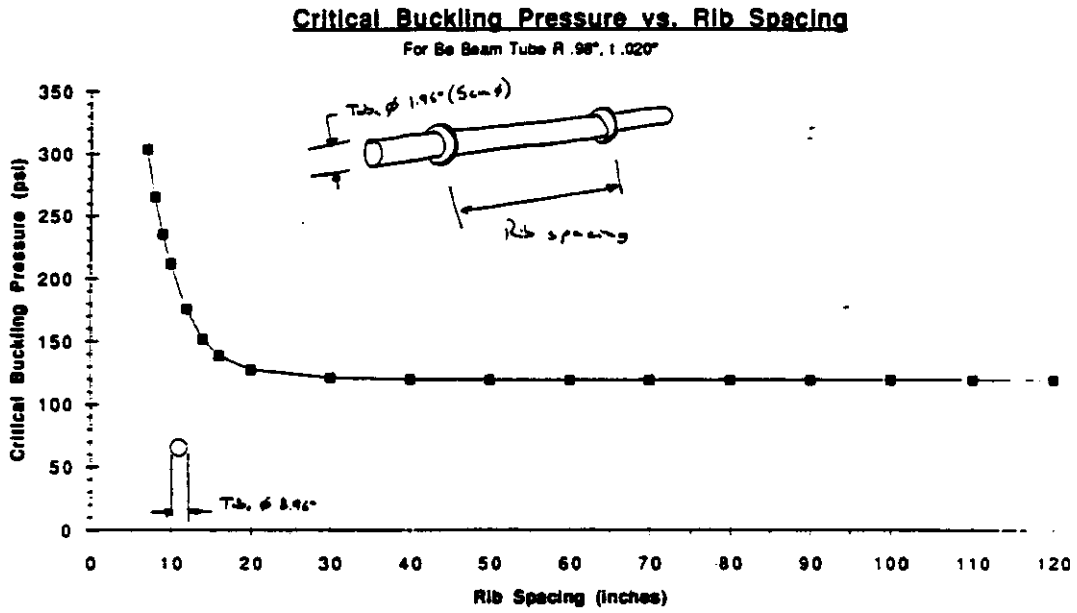

Fig 19

Severe degradation in the buckling pressure can occur when out-of-roundness is taken into account. The decrease is most sensitive for out-of-roundness shapes that approximate the buckling mode shapes. For a long tube configurations the mode of collapse is into an elliptical (2 lobe) shape. Discussions with Electrofusion Corporation regarding their fabrication process have established the potential for tubes to be elliptically out-of-round by as much as .015". Figure 20 is a plot from 3 sources, of critical buckling pressure vs out of roundness for a Beryllium beam tube .98"R and a wall of .020". All of the plots indicate that the design marginally meets the 60 psi specification at .015" radial deviation.

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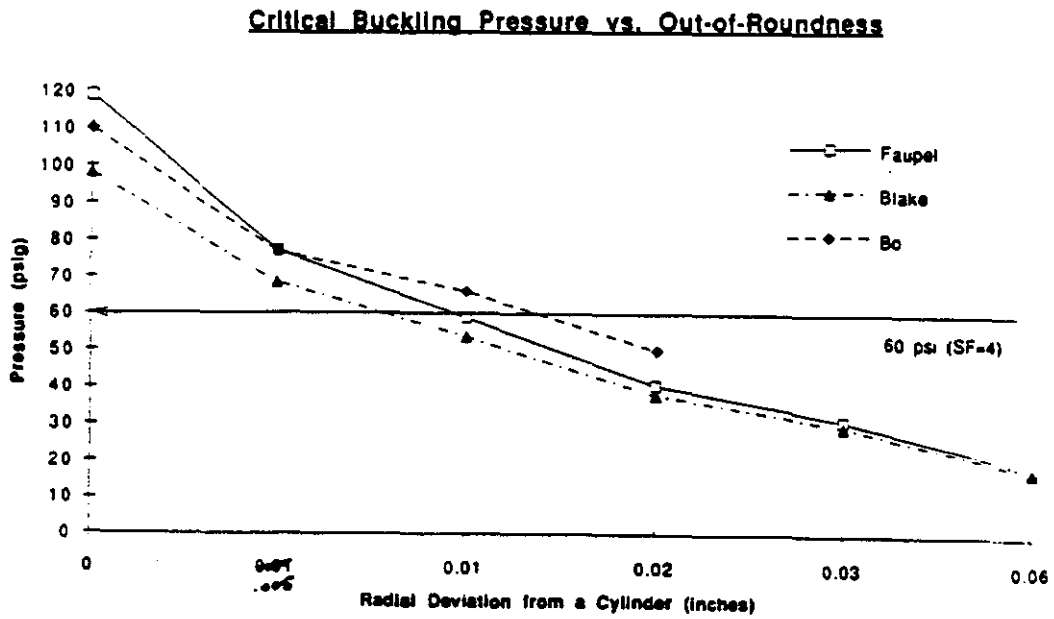


Fig 20

This may drive us to consider the addition of ribs in our baseline design. For this application, considering we are using a brittle material we may decide to go to a higher safety factor.

Unlike a ductile failure, the failure of a brittle tube is likely to cause surrounding damage. The sensitivity of the design to distortions combined with the brittleness of the material is a compelling argument to have mechanical isolation at the ends of the Beryllium section. To obtain a very thin tube to meet the radiation length requirements will involve very tight fabrication specifications and very tight Quality Control procedures. At this time we have only scoped out the design problems and not yet established a baseline design.

3.2.9 Cooling System

The mechanical stability and locating requirements, as specified in the mechanical design section of this report, requires the highest attainable isothermalization of the entire detector array. Furthermore, the Silicon Detector leakage current requirement dictate a reduced operating temperature, specified at this time to be 0 °C. The system pressure should not deviate significantly from 1 atmosphere to prevent the need for a containment structure that can tolerate large pressure differentials. These electronics are located at one end of the silicon wafers. The power per strip is 3 mW and there are 1280 strips per wafer. In addition, each wafer has a 150 mW LED. Total power per wafer end is then 4 W. The total number of Electronics packages in both the barrel and forward regions is

4840. The total thermal load is then 9.7 kW. The system must also meet all state and federal safety requirements.

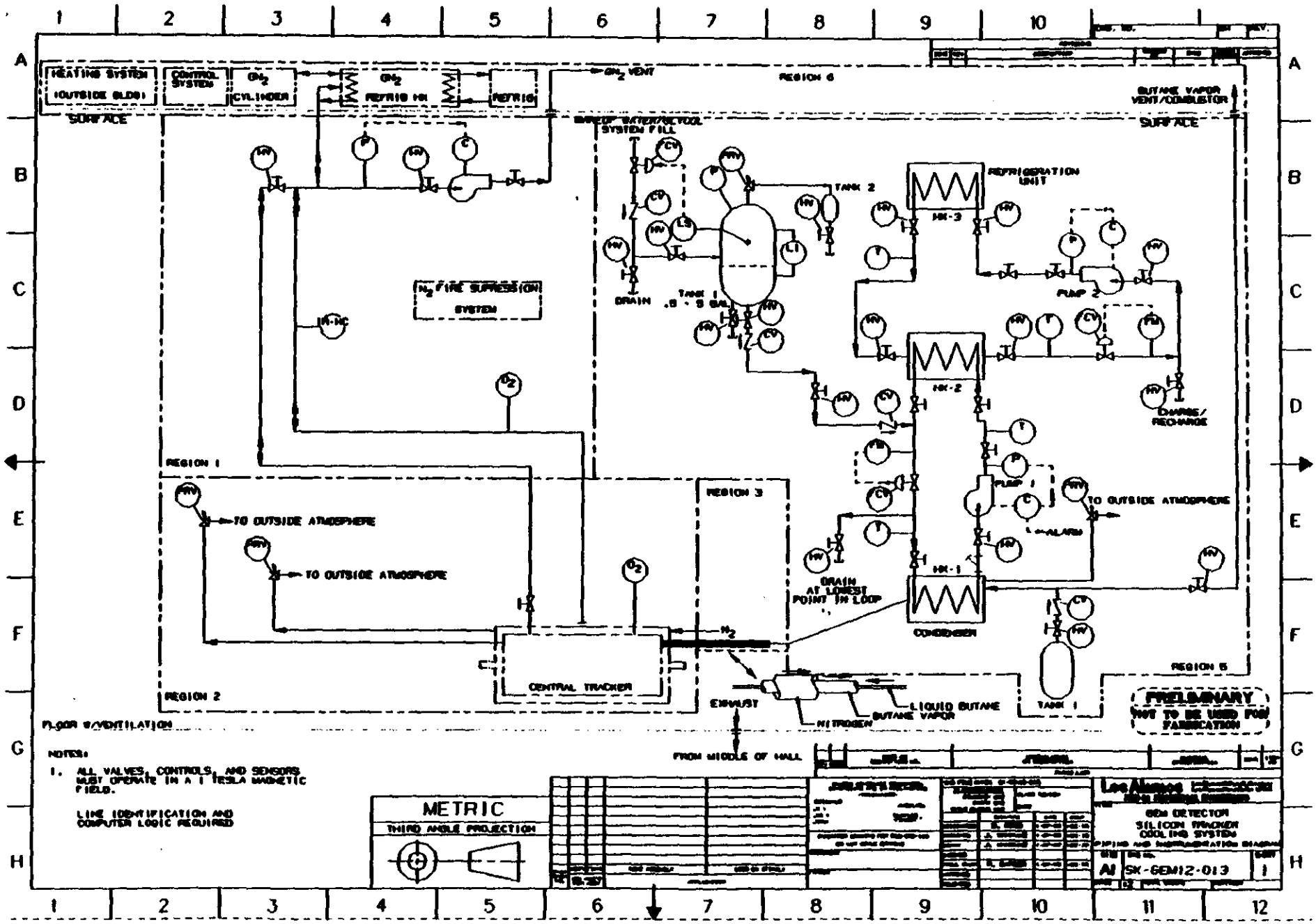
The silicon is supported by and mounted to composite ring structures called cooling rings. These cooling rings are lined with a capillary wicking structure that incorporates a low impedance circumferential flow artery. A volatile liquid is fed into the artery and distributed through the wick structure by capillary forces. The liquid evaporates in response to the electronics heat load. The fluid loop is closed by transporting the resulting vapor to a condenser using the small pressure differential that exists between the silicon tracker containment vessel and the condenser. The condensed liquid is fed back to the detector array through a liquid distribution system. Butane or isobutane will be used as the coolant because of the desire to operate the silicon at near 0° C and at 1 atmosphere pressure.

In the interest of minimizing system mass, the design goal is to supply the circumferential artery with liquid from the liquid distribution system at a single point. Thus, the gravitational pressure drop is a major contribution to the total pressure difference between the liquid and vapor. This total pressure drop must be sustained by the capillary pumping capability of the wick structure. The smaller system diameter reduces the gravitational term proportionately. The maximum pore size must be less than 11.7 microns as opposed to 5 microns.

There are additional pressure drops that must be overcome by the capillary pumping capacity of the wick structure. These are power and power density related in that they are dependent upon the amount of fluid that must be circulated. They are also dependent upon the allowable wick thickness, which is impacted by the allowable radiation length. The power densities, as measured at the cooling ring to silicon wafer interface area is 1.8 W/cm^2, or 0.55 W per cm of cooling ring length. The liquid flow out of the artery is only 1.4 mg/s-cm. However, this liquid must flow through a low permeability wick structure (permeability is related directly to pore size, ie., small pores yield low permeability).

At this time, it is not possible to present a final design because the fluid distribution system pressure drops depend upon the wick structure, which is yet to be determined. The baseline wick material and construction for the wick is a molded polystyrene foam. Tests of this wick option have given encouraging results. A trial and error effort to converge on a suitable pore size and permeability is in progress.

The current configuration of the cooling rings and silicon wafers separates the heat loads from the cooled surface by about 3 cm. This requires that the electronics run hotter than the cooling ring and the silicon by up to 45 and 30 °C, respectively, depending upon the materials of construction and the final layout. Design changes are being considered in


HEATING SYSTEM (OUTSIDE BLDG)
CONTROL SYSTEM
GN_2 CYLINDER
GN_2 REFRIG HX
REFRIG
GN_2 VENT
REGION 6
BUTANE VAPOR VENT/COMBUSTOR
SURFACE
SURFACE
BACKUP WATER/BETOOL SYSTEM FILL
TANK 2
REFRIGERATION UNIT
HX-3
PUMP 2
DRAIN
TANK 1 .5 - 5 GAL
N_2 FIRE SUPPRESSION SYSTEM
HX-2
DRAINS/RECHARGE
REGION 1
REGION 3
TO OUTSIDE ATMOSPHERE
TO OUTSIDE ATMOSPHERE
TO OUTSIDE ATMOSPHERE
ALARM
HX-1
DRAIN AT LOWEST POINT IN LOOP
CONDENSER
CENTRAL TRACKER
REGION 2
REGION 5
EXHAUST
LIQUID BUTANE
BUTANE VAPOR
NITROGEN
TANK 1
PRELIMINARY
NOT TO BE USED FOR FABRICATION
FLOOR W/VENTILATION
FROM MIDDLE OF HALL
NOTES:
1. ALL VALVES, CONTROLS, AND SENSORS MUST OPERATE IN A 1 TESLA MAGNETIC FIELD.
LINE IDENTIFICATION AND COMPUTER LOGIC REQUIRED
METRIC
THIRD ANGLE PROJECTION
Lee Alonso
GEM DETECTOR
SILICON TRACKER
COOLING SYSTEM
PIPING AND INSTRUMENTATION DIAGRAM
A1
SK-GEM12-013
1

an effort to bring the coolant and the evaporating surfaces closer to the head sources. These efforts include changing the spacing between the electronics and the cooling ring or moving the wicks out of the cooling rings and onto or at least closer to the electronics.

Design details hinge in part on the development of the optimum wick structure for liquid distribution and design options that improve the thermal coupling between the electronics and the wetted wicks. A suitable wick structure must be developed and incorporated, liquid and vapor line sizes must be finalized, the condenser must be designed, a suitable start-up and shut-down procedure must be developed, and system component testing must be performed.

3.2.10 Alignment Systems

Mechanical design, alignment systems and assembly procedures must be closely coordinated to build a high resolution silicon tracking system. Concepts for GEM detector alignment/assembly procedures have just been started. The difference between actual placement tolerances and knowledge of position need to be carefully separated and considered. The tolerances requirements will determine where the most effort is placed, either in assembly or in calibration and stability monitoring. The most difficult tolerance will most likely be the circumferential positioning of parts, subassemblies and detectors. Even the easiest tolerances will be quite demanding, probably too demanding for manual placement. Next, six distinct alignment/assembly steps need to be defined and planned. Assembly/alignment procedures depend on a definition of: 1.) a stable assembly reference system, 2.) an assembly procedure, alignment system and mechanical placement machine to attach silicon ladders to support rings and planer arrays, 3.) an assembly/alignment procedure to attach shells and planer array subsystems to a space frame, 4.) a method to place the assembled detector onto the SSC beam line, 5.) alignment monitors to follow alignment changes during assembly, transport, installation and use, and 6.) a calibration procedure to be used for the installed detector. Trade-off's between these steps will influence the cost, assembly time and difficulty of building the detector.

In addition to the alignment/assembly procedures some testing, most likely on prototypes, should be planned to establish the stability of completed subassemblies. A dependable alignment monitoring system will relieve some burden on the mechanical stability of the assembly, but monitoring systems only monitor a few points

on the structure; subassemblies are treated as rigid bodies. TV holography is a test procedure with the required resolution and field of view for testing the stability of completed subassemblies. The technique is basically an optical interferometer for non-optical surfaces. A state of the art system can measure quantitative and qualitative information about object shape, shape changes induced by mechanical or heat loading, mechanical resonance frequencies and resonant Q. State of the art TV holography systems are not available commercially. They have to be custom built to carry out these important tests.

Critically important and challenging is the alignment monitoring system for the calibrated detector. A useful alignment system should monitor detector alignment shifts after assembly, during transport and installation, and between calibration runs. The resolution of the monitor should be sufficient to determine when another calibration is needed. If the rigid body assumption about the subassemblies is valid, and if the alignment monitor has sufficient dynamic range, then after an initial calibration run, the monitoring system can be used to correct particle track information and eliminate the need for continuous time consuming calibrations .

A concept for a continuously monitoring system is shown in Figure 21.

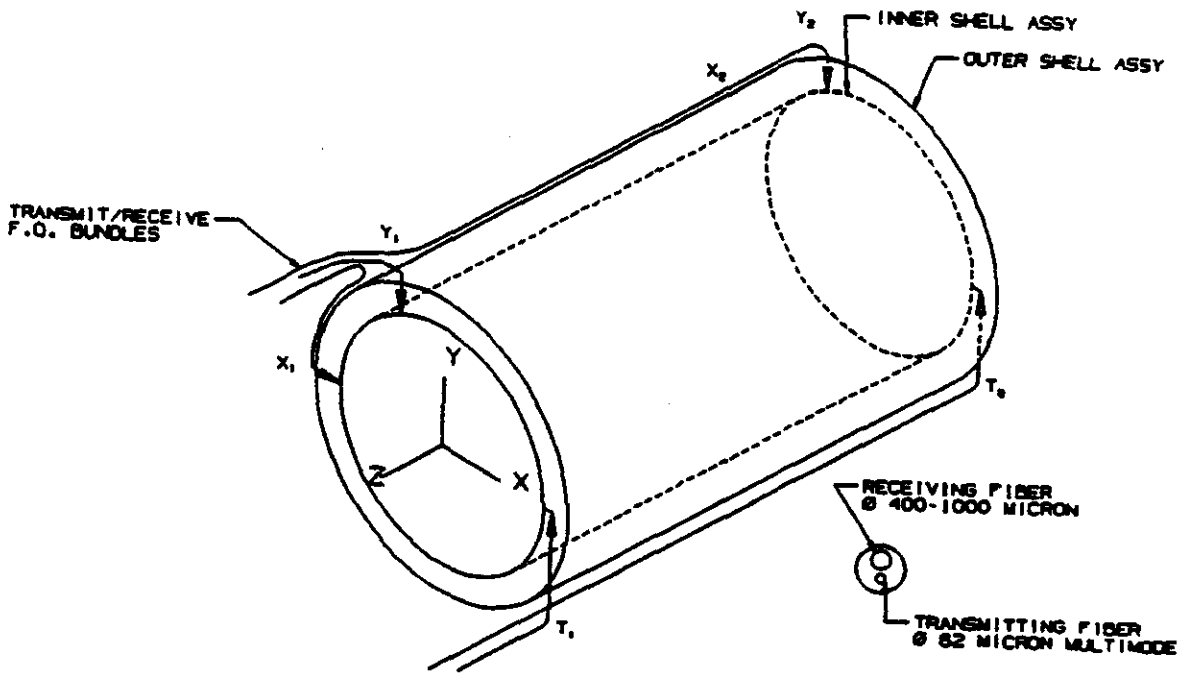


Fig 21

The 3-D positions of one subassembly relative to another, and the position of the silicon detector to the outside world, are monitored with a rad-hard, compact non-intrusive fiber optic motion sensor. As shells are attached to the space frame, fiber optic motion sensors

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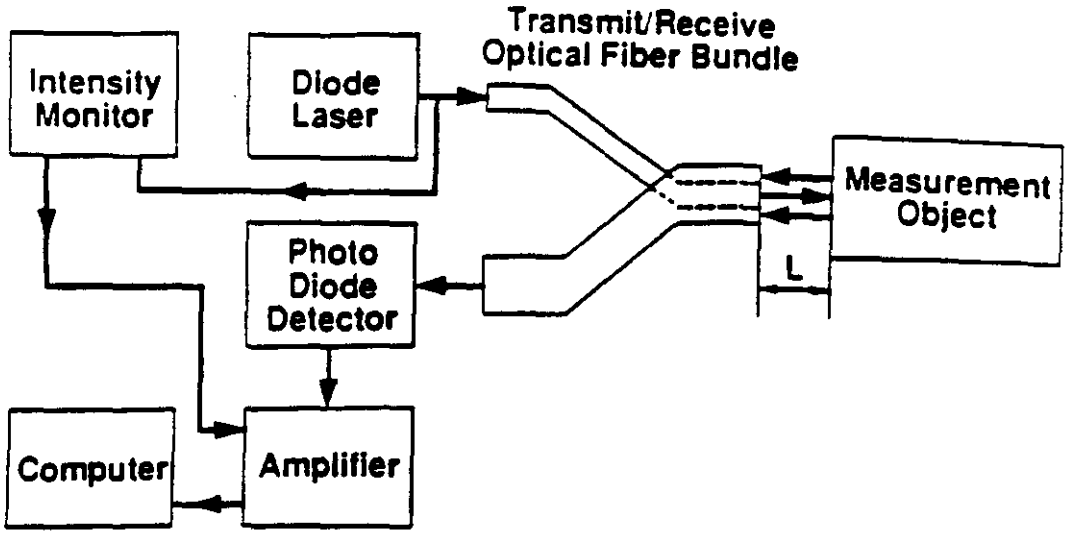

Transmit/Receive
Optical Fiber Bundle
Intensity
Monitor
Diode
Laser
Measurement
Object
Photo
Diode
Detector
L
Computer
Amplifier

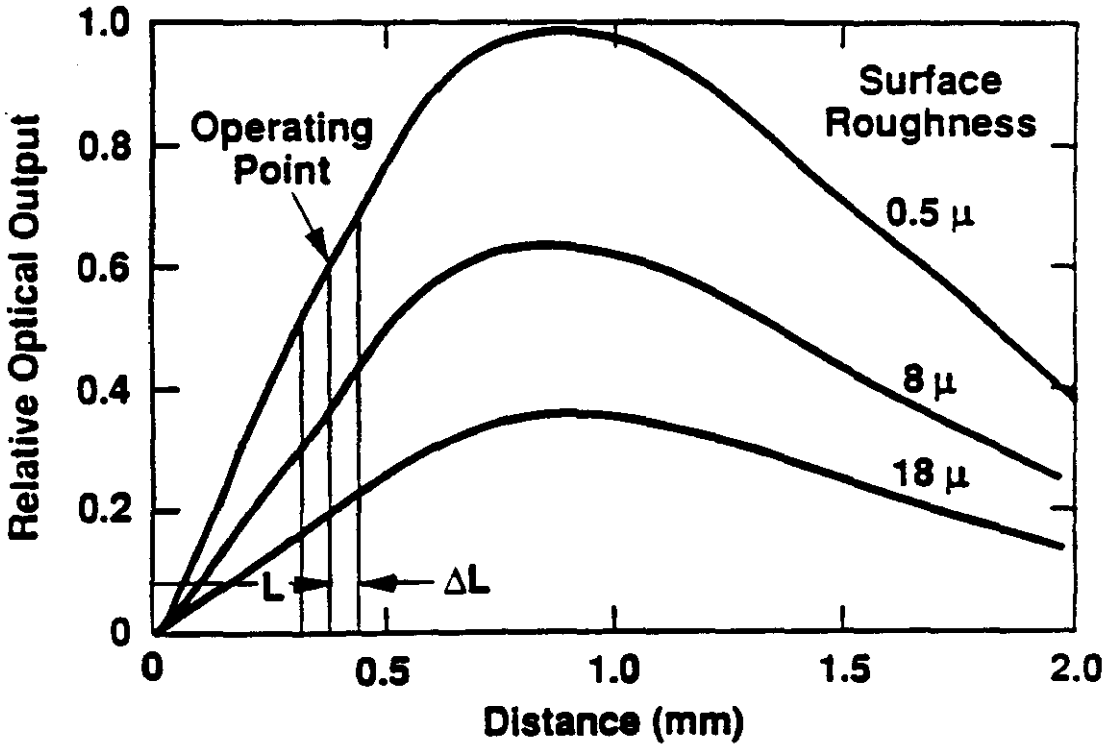

Relative Optical Output
1.0
0.8
0.6
0.4
0.2
0
Operating
Point
Surface
Roughness
0.5 μ
8 μ
18 μ
L
ΔL
0
0.5
1.0
1.5
2.0
Distance (mm)

Fig 22

will also be attached to every rigid body subassembly to monitor relative 3-D outside the detector. At the present stage of development of fiber optic motion sensors, a motion sensor is needed for each degree of freedom to be monitored. With 4 monitors on a rigid assembly all motions except translation along the beam axis and rotation about the beam axis are monitored. Using this technique, detector alignment status can be continually monitored from initial assembly through transport and installation, and during operational use between calibrations.

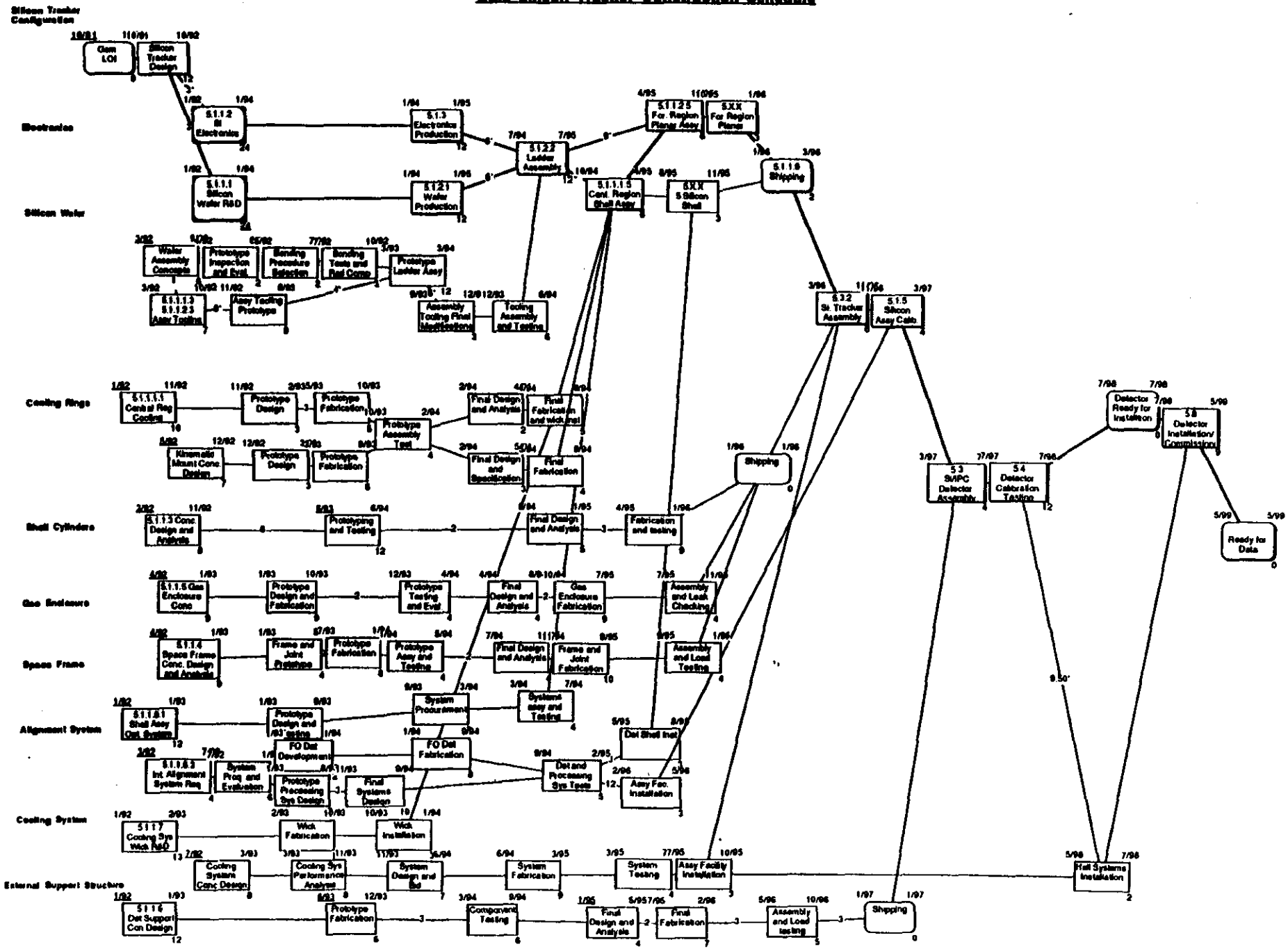
A simplified schematic for a motion sensor system is shown in Figure 22, with typical response curves. For a few mm between fiber and object the response is on the order of 8 mv/μm. The measurement resolution is .05 microns. The response curves are linear on the leading and trailing parts of the curve, either of which are suitable regions for operating points. With automatic gain control any variations in the light output from the diode laser can be monitored and compensated. Calibration can be carried out on a test fiber away from the detector. Installation should be relatively easy, if it is planned into the detector from the beginning. Since all the active hardware is outside of the detector volume, the system will be very robust. The several mm spacing between fiber and object used for published results is smaller than needed for detector applications, but similar results for 2.5 cm spacing and 1 micron resolution, and many mm of dynamic range have been demonstrated. The response curve shape is similar for the larger spacings between the fiber and object. The position of the peak response can be adjusted by choosing an appropriate receiver fiber diameter.

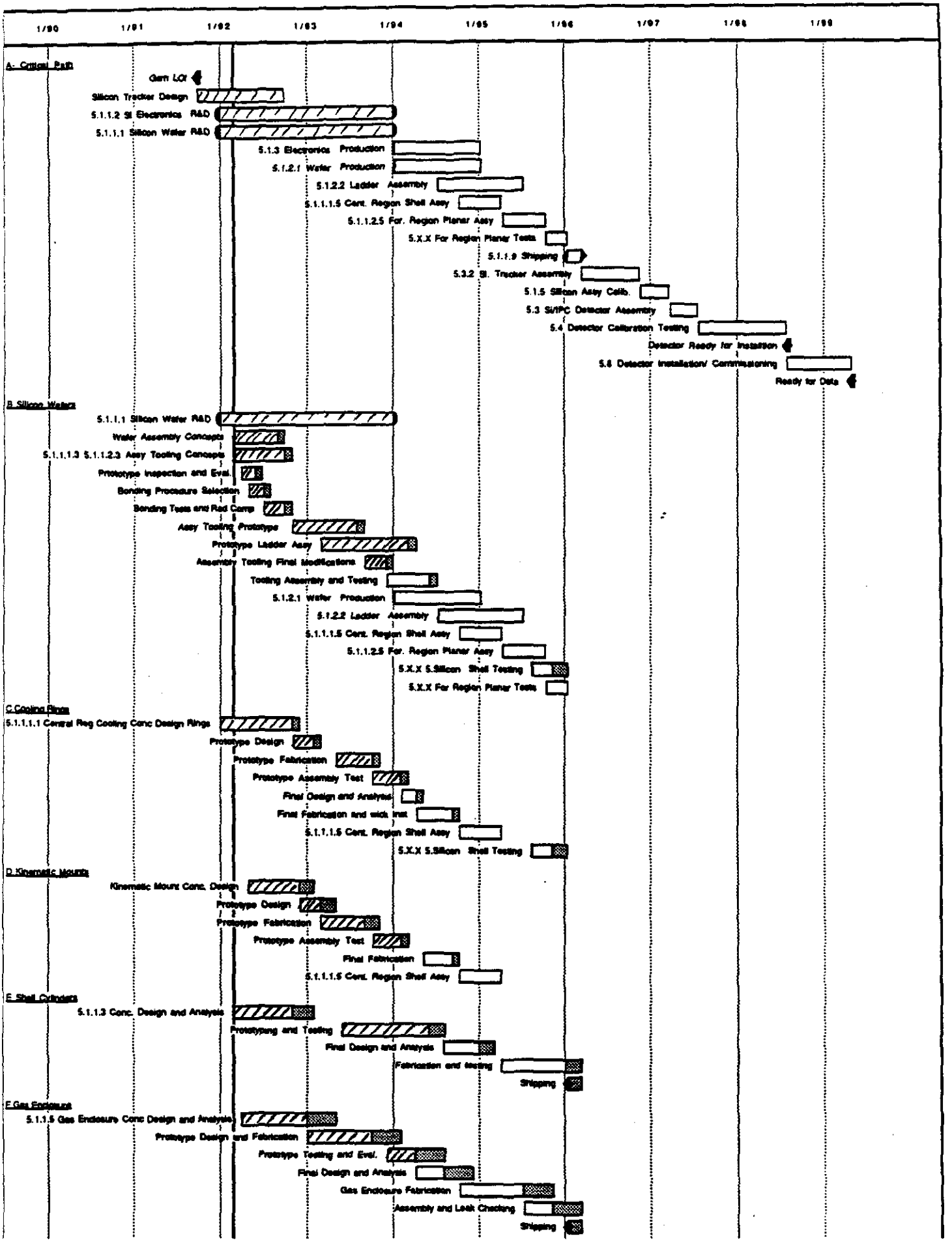
The fiber optic motion sensor is now a research device, not commercially available; research is needed to develop the concept for the detector application and test and calibrate it during prototype tests. Other than this technique there is no known, easy technique to continuously monitor the alignment status of the detector during transport and between calibrations.

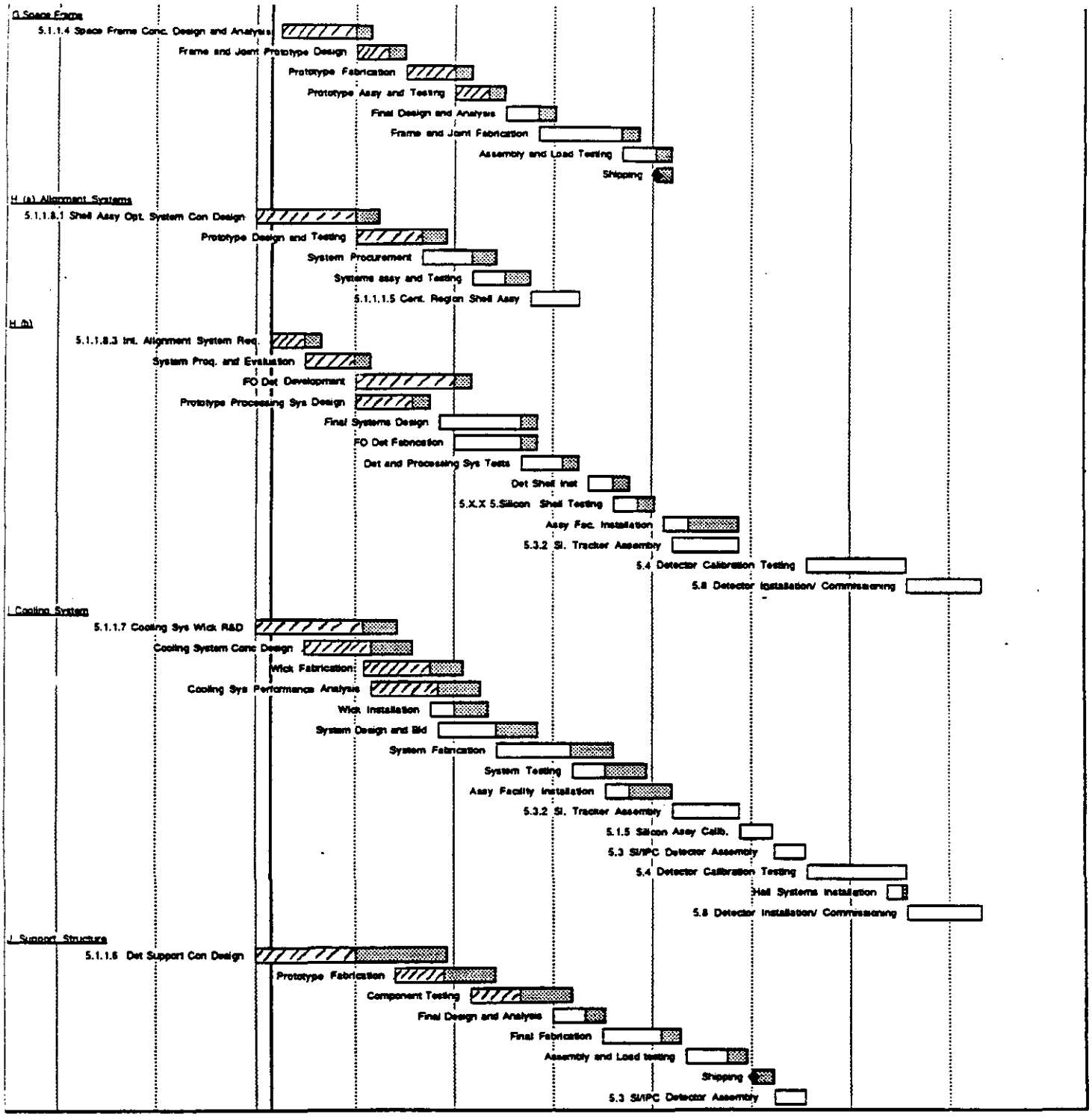
3.2.11 R & D and Construction Schedule

The GEM Silicon Tracker Construction Schedule shows the major R&D, prototyping, fabrication, assembly, and testing schedule elements. Some of the time elements are broken down into additional subtasks, while many others will need to broken down in more detail. The beginning of the schedule is set up with the completion of the LOI, with the ending of the schedule determined by the task duration and dependencies. The early critical path items are the electronics and silicon microstrip detector R&D.

GEM Silicon Tracker Construction Schedule




1/90
1/91
1/92
1/93
1/94
1/95
1/96
1/97
1/98
1/99
A- Critical Path
Gem LOI
Silicon Tracker Design
5.1.1.2 Si Electronics R&D
5.1.1.1 Silicon Wafer R&D
5.1.3 Electronics Production
5.1.2.1 Wafer Production
5.1.2.2 Ladder Assembly
5.1.1.1.5 Cent. Region Shell Assy
5.1.1.2.5 For. Region Planar Assy
5.X.X For Region Planar Tests
5.1.1.9 Shipping
5.3.2 Si. Tracker Assembly
5.1.5 Silicon Assy Calib.
5.3 Si/IPC Detector Assembly
5.4 Detector Calibration Testing
Detector Ready for Installation
5.6 Detector Installation/ Commissioning
Ready for Data
B Silicon Wafers
5.1.1.1 Silicon Wafer R&D
Wafer Assembly Concepts
5.1.1.1.3 5.1.1.2.3 Assy Tooling Concepts
Prototype Inspection and Eval.
Bonding Procedure Selection
Bonding Tests and Rad Comp
Assy Tooling Prototype
Prototype Ladder Assy
Assembly Tooling Final Modifications
Tooling Assembly and Testing
5.1.2.1 Wafer Production
5.1.2.2 Ladder Assembly
5.1.1.1.5 Cent. Region Shell Assy
5.1.1.2.5 For. Region Planar Assy
5.X.X 5.Silicon Shell Testing
5.X.X For Region Planar Tests
C Cooling Rings
5.1.1.1.1 Central Reg Cooling Conc Design Rings
Prototype Design
Prototype Fabrication
Prototype Assembly Test
Final Design and Analysis
Final Fabrication and wick inst
5.1.1.1.5 Cent. Region Shell Assy
5.X.X 5.Silicon Shell Testing
D Kinematic Mounts
Kinematic Mount Conc. Design
Prototype Design
Prototype Fabrication
Prototype Assembly Test
Final Fabrication
5.1.1.1.5 Cent. Region Shell Assy
E Shell Cylinders
5.1.1.3 Conc. Design and Analysis
Prototyping and Testing
Final Design and Analysis
Fabrication and testing
Shipping
F Gas Enclosure
5.1.1.5 Gas Enclosure Conc Design and Analysis
Prototype Design and Fabrication
Prototype Testing and Eval.
Final Design and Analysis
Gas Enclosure Fabrication
Assembly and Leak Checking
Shipping


G Space Frame
5.1.1.4 Space Frame Conc. Design and Analysis
Frame and Joint Prototype Design
Prototype Fabrication
Prototype Assy and Testing
Final Design and Analysis
Frame and Joint Fabrication
Assembly and Load Testing
Shipping
H (a) Alignment Systems
5.1.1.8.1 Shell Assy Opt. System Con Design
Prototype Design and Testing
System Procurement
Systems assy and Testing
5.1.1.1.5 Cent. Region Shell Assy
H (b)
5.1.1.8.3 Int. Alignment System Req
System Proq. and Evaluation
FO Det Development
Prototype Processing Sys Design
Final Systems Design
FO Det Fabrication
Det and Processing Sys Tests
Det Shell Inst
5.X.X 5.Silicon Shell Testing
Assy Fac. Installation
5.3.2 Si. Tracker Assembly
5.4 Detector Calibration Testing
5.8 Detector Installation/ Commissioning
I Cooling System
5.1.1.7 Cooling Sys Wick R&D
Cooling System Conc Design
Wick Fabrication
Cooling Sys Performance Analysis
Wick Installation
System Design and Bld
System Fabrication
System Testing
Assy Facility Installation
5.3.2 Si. Tracker Assembly
5.1.5 Silicon Assy Calib.
5.3 Si/IPC Detector Assembly
5.4 Detector Calibration Testing
Shell Systems Installation
5.8 Detector Installation/ Commissioning
J Support Structure
5.1.1.6 Det Support Con Design
Prototype Fabrication
Component Testing
Final Design and Analysis
Final Fabrication
Assembly and Load testing
Shipping
5.3 Si/IPC Detector Assembly

As a minimum the Silicon Tracker will require a 2 year Silicon wafer R & D effort followed by a 5 year fabrication and assembly schedule. The Task Timelines are grouped to show the critical Path items and the major subassembly items. The A Critical Path grouping shows the 2 years of wafer R&D starting in 92 and finishing in 93, with the wafer production occurring in 94. In parallel to this effort is the Electronics R&D and production. Both components are required to start the ladder assemblies in mid 95. It is assumed that enough components will be available mid way through production to start the assembly. The Ladder assemblies are followed by the Central and Forward Region subassemblies, followed by testing of each subassembly. This will allow us to ship these major subassemblies in early 96 to the SSCL for the final assembly.

The Silicon Tracker will be assembled then systematically inspected and tested. A lengthy period of at least 9 months will be required to do signal calibrations and X-Ray mapping of the Silicon Tracker after it is assembled. This schedule has that task occurring after the Silicon Tracker is assembled to the IPC Tracker in 97. By mid 98 the Central Tracker assembly will be ready for installation into the Detector Hall. A period of at least 9 months will be required to do the systems hookups, final tests, signal calibrations, and initial commissioning. This leads us to a completion date of early 99.

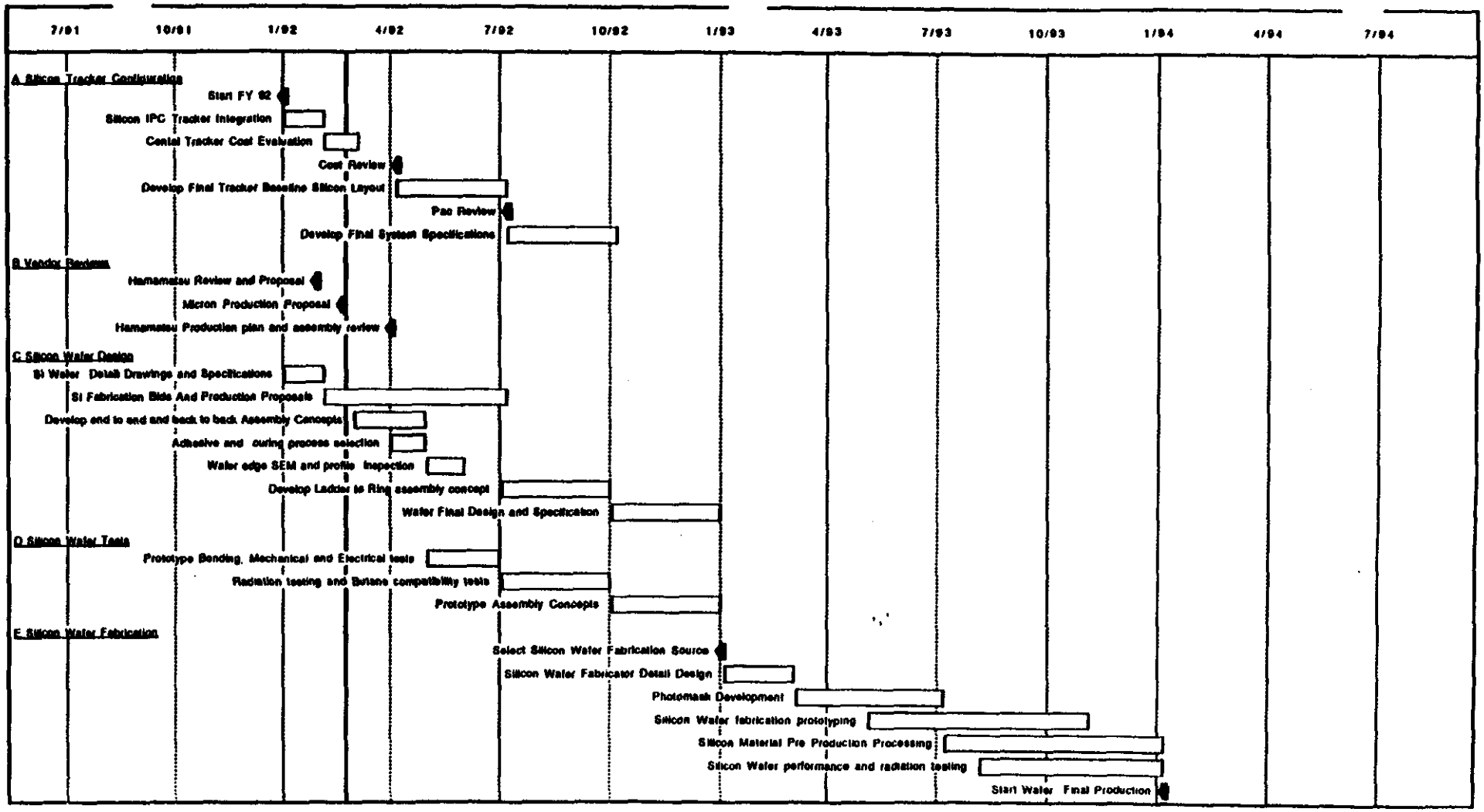
Additional task groupings are: B Silicon Wafers (these are tasks mainly associated with assembly concepts), C Cooling Rings, D Kinematic mounts, E Shell Cylinders, F Gas Enclosure, G Space Frame, H Alignment Systems, I Cooling Systems, J Support Structure.

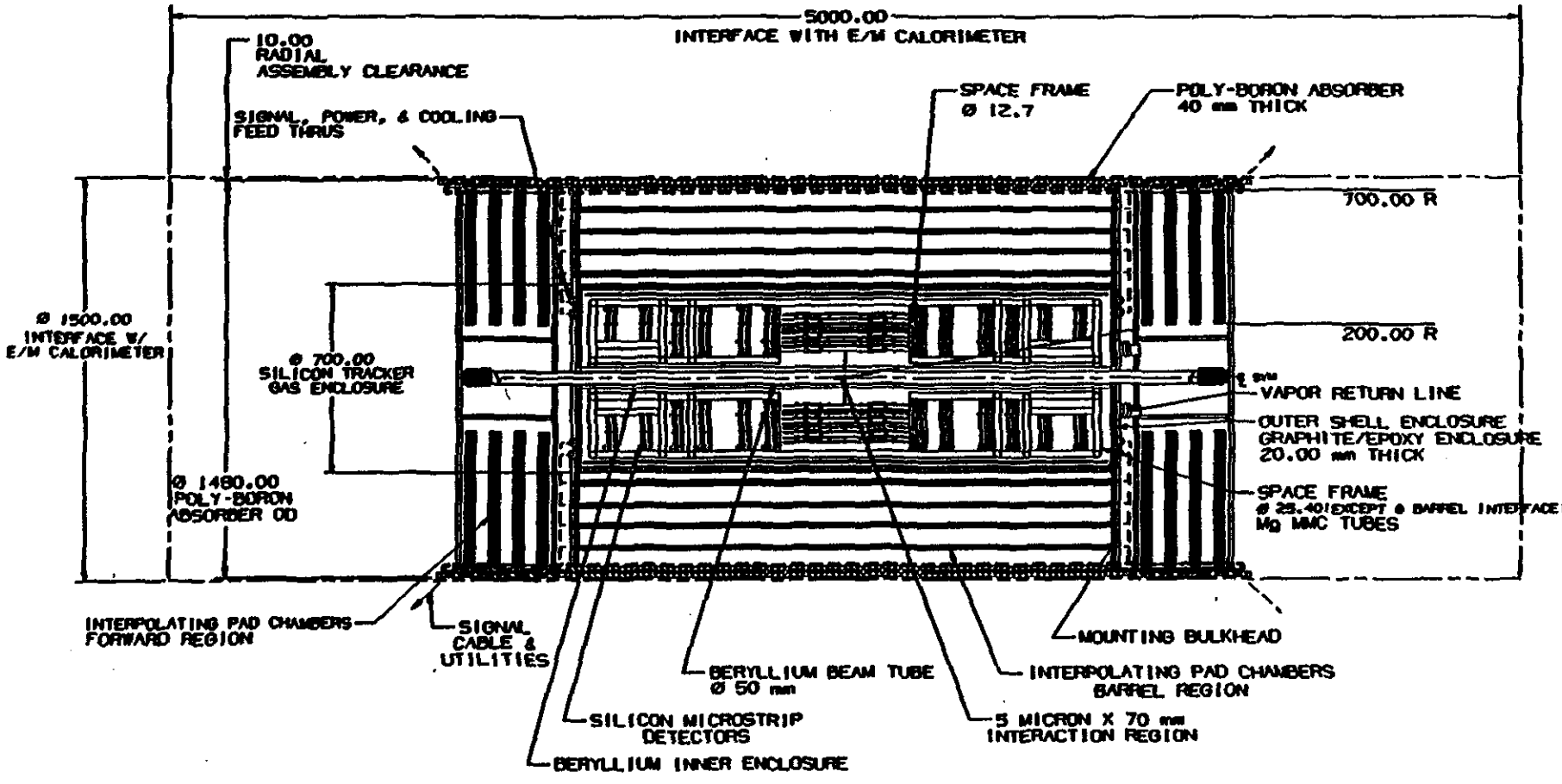
The minimum design and R&D tasks associated with the 2 year Silicon Wafer R&D are broken down in more detail. A one year joint R&D effort between the manufacturer and Los Alamos will be required prior to starting the wafer fabrication.

Silicon Wafer detail drawings and specifications have been sent out to several qualified vendors for cost estimating and fabrication planning. We will continue to meet with prospective vendors throughout 1992 as the final design and specification evolve. The final configuration of the Silicon Tracker will have to be frozen shortly after the July PAC review to finalize the system requirements and generated the final detail drawings and specifications. There will be a final competitive bid for the Silicon microstrip fabrication and the contract will be awarded by January 1993 to start our one year of joint R&D.

RLB 3/2/92

Silicon Wafer R&D 92 - 94





GEM CENTRAL TRACKER

3.3 Silicon Tracker Electronics

3.3.1 Introduction

The silicon tracker electronics involves the application of high speed, low power, integrated micro-electronics in a high radiation environment. The channel count in this system is high so that a careful design is needed in order to minimize cost. The number of options that satisfy the above requirements and which are available in existing technologies are limited. The general parameters of the baseline system electronics are given below in Table 1.

Table 1. GEM Silicon Tracker Parameters

Total Silicon Area	7.61 m^2
Total Number of Strip Electronic Channels	3.23×10^6
Number of VLSI Circuits (CMOS&Bipolar)	50,520
Number of Hybridized Circuits	5052
Number of Layers of Silicon	12 Single Sided (6 Double Sided)

The tracker will need to handle events at a clock rate of 62MHz, to exist in a high radiation field (equivalent to 10^{14} n/cm^2 total dose), to be constructed of very low mass and low radiation length materials, and to have a low power consumption. The following table gives some of the requirements:

Table 2. SSC Operational Parameters for the GEM Central Tracker

Luminosity	10^{33} $cm^{-2}s^{-1}$
Bunch Crossing Frequency	62 MHz
Total Charged Particle Radiation Dose ($R = 10cm$, $\eta = 0$)	.44 MRad/SSC year (charged particle)
Number of tracks in tracker for hard scattering event	100-200 tracks
Power Budget	<3mW per channel

3.3.2 General Properties and Issues

The overall electronics system for the silicon tracker has several components. The primary data path consists of on-board electronics, which include the bipolar amplifier/discriminator, the digital delays for the Level 1 and 2 triggers, output digital data optical links, and finally an external data acquisition system to build data packets for the final event builder. In addition to the primary data path there is a substantial number of control signals which include clock signals, trigger signals, time stamps, and other control signals which are needed to maintain control of the data acquisition. A number of services must also be provided to the on-board electronics such as bias and low voltage power distribution, temperature monitoring, and other housekeeping functions devices, and bias and low voltage power distribution. The detail of these signals depends upon the architecture chosen for the system.

There are several possibilities for data acquisition architectures. The GEM data acquisition architecture allows for 3 levels of buffering and triggering. The following table gives the expected input rates, latency times, and output rates of the various levels of the data acquisition.

Table 3. GEM Trigger Rate Goals

Level	Rate In	Rate Out	Latency	Comments
1	62.5 MHz	10khz	2μs	Synchronous
2	100kHz	300Hz	100μs	Asynchronous
3	3kHz	10Hz	-	CPU Ranch

The above rates will determine the speed at which each level of the electronics buffering and storage must operate. One in principle has the choice between bringing the data out of the detector for each beam crossing, or, one could wait and transmit the data after the first or second level trigger decisions have been made. This choice, along with the multiplexing ratio of the link (number of channels serviced by a single link) will determine the rate at which the on-board digital data link must operate. Table 4 gives several rates at which a data link must operate given a particular architecture. Here, the rate is given for one multichip module (640 bits) which could potentially be compressed to 80 bits. In the case of an LED driver (50 Mbit/s) one is restricted to transmitting compressed data after Level 1 or possibly the full data after Level 2. In the former case, one could potentially multiplex by a factor of 4 to reduce the number of data links, and in the latter case, one could potentially reduce the number of data links by a factor of 20 by multiplexing.

Table 4. Data Flow Architectures

Transmit Trigger Level	Rate	Full Data Stream Rate (640 bits)	Compressed or Trigger Data (80 bits)	Latency
0	62.5 MHz	40 Gbit/s	5 Gbit/s	2μs
1	100kHz	64 Mbit/s	8 Mbit/s	100μs
2	3kHz	1.9 Mbit/s	240 kbit/s	-

3.3.3 Bipolar Analog Circuits

Design Considerations

Baseline design requirements such as radiation-hardness levels, noise performance, discriminator time-walk as well as power consumption are already well established by now. However, the circuit design and implementation has not advanced as much, and various options are still being examined at different levels of developments. Additional design considerations unique to the Central Tracker environments need to be addressed further to achieve the optimal design. Some of the design issues concerning analog bipolar ASIC design are:

The thermal environment where the temporal fluctuation may be quite small, but the thermal gradient over the entire tracker volume may not be.

The rate of damage from radiation is a strong function of location, and, consequently, the gain changes of the transistors will depend on the location of the electronics within the tracker causing non-uniform bias point drifts.

The testability and controllability of each channel while considering the enormous number of channels to scan. The protection of each input line from most transient surges or spikes.

The stability effects of the amplifier due to process variation, radiation damage and detector capacitance.

Thus the front-end analog circuit should incorporate the following design features in addition to the baseline configurations.

1. Gain of each amplifier stage should be tightly controlled with negative feedback and larger than normal open-loop gain to compensate for the effects due to temperature, radiation damage and fabrication processes. The large open-loop gain translates into wide unity-gain bandwidth for preamplifier stage for faster rise time even when the charge conversion capacitance is small.

2. It is better to add a conversion capacitor in addition to the stray capacitance inherent in a feedback resistor (or an FET) even though it results in somewhat reduced charge conversion gain. The capacitor not only provide better control over conversion gain, but also improves the risetime and stability of the preamp stage.

3. The use of higher than nominal current level also helps to reduce the radiation damage effect since the gain degradation in bipolar transistors depends strongly with operating currents.

4. Baseline of the waveform at the input of a level discriminator should be actively controlled. Even though the reference voltage level supplied from outside world may be infinitely adjustable, there is no practical way of individually trimming the levels for each channel. The dependency of the bias points on temperature, radiation damage and IC fabrication processes in a non-controlled design will make the circuit impractical in a long-term, remote operational environment.

5. The availability of complementary bipolar transistors at very high frequency range (3 - 8 GHz cutoff freq) should be exploited for full benefit. Designs with complementary transistors provide better performance in power consumption, bias determination and circuit speed (on both edges of a pulse waveform) over a fast NPN transistor only design.

6. The cost of ASIC fabrication is crucial to meet the budget constraints. Since the die size of the chip design has most influence on unit cost, a compact circuit design is mandatory. The use of passive components such as resistors and capacitors should be at minimum for smaller die size.

7. A protection diode and test injection cap should be incorporated at the input node of each chain. The noise effect of the added capacitance (a fraction of a pF) from the diode is insignificant considering up to 15 pF of existing strip capacitance.

Preliminary Circuit Design

A design incorporating the above considerations was generated for a preamplifier/ shaper combination (Figure 1a), and was simulated using component libraries from AT&T and Harris. Both companies are in the forefront of fabrication technology and produces multi-GHz complementary transistors for custom and semi-custom ASICs. The combination circuit (excluding discriminator) consumes slightly less than 1mW and meets all basic requirements in noise and speed. The input circuit node has a protection diode with a 330-ohm current limiting resistor and calibration injection capacitor. The use of a current limiting resistance causes little noise degradation.

At equal power consumption, the Harris-based design has significantly better performance in open-loop gain and phase margin. Please note that this is a worst-case (or, very conservative) design rather than nominal in order to reduce the degradation effects from various causes as explained earlier. Figure 1b shows the response of the charge sensitive preamp when injected with different amount of charges in 20 ns square pulses repeated at every 1 us. A 0.2 pF discrete capacitance is used in parallel with 200 kohm for better control of charge conversion gain.

The shaper amplifier stage is designed with an active pull-down of the output bias point using a low-frequency feedback loop on a differential input. The pull-down circuit forces the output of the shaper to within a few millivolts of ground level (Figure 1c.) regardless operating conditions within limits. The use of a pull-down poses a slight stability consideration, however, and deserves more study in the future.

The comparator design is in progress with encouraging results. The projected power consumption of the comparator design is less than 0.5 mW, so the total power consumption of the bipolar front-end design is slightly less than 1.5 mW per channel including the level discriminator. This is more from the choice of circuit bias condition than from pushing the performance limits of given transistors.

The circuit design is not yet optimized in reducing the amount of resistances, especially for NiCr types if so chosen. Resistors in an IC design present die size problems, and future designs will incorporate few resistors than are shown in schematics. The fabricated die size depends on foundry design rules and final design, but current projection indicates an approximate die size of 6.4 x 7.0 mm^2 including bond pads.

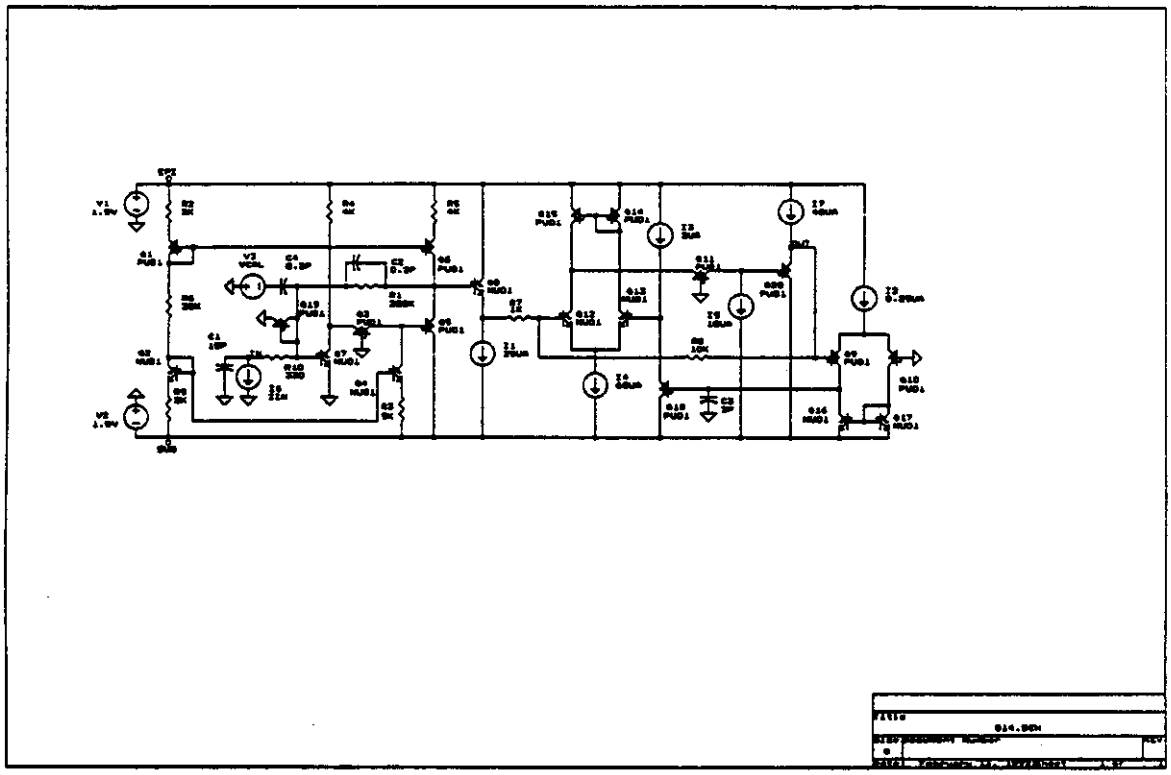


Figure 1a. Preamp/Shaper Schematic Used for SPICE Simulation

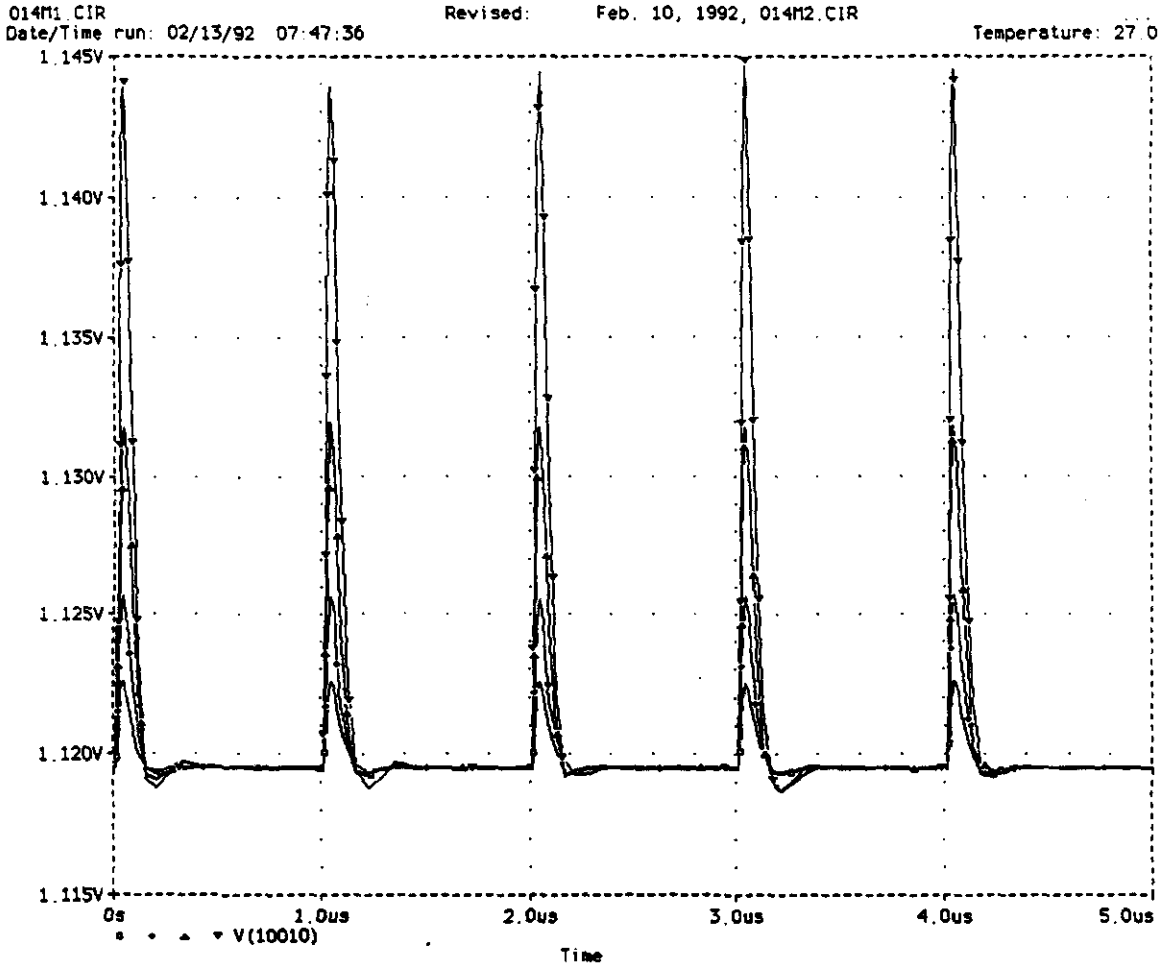


Figure 1b. Preamp Output Waveforms for 1, 2, 4, 8 fC Input Charges

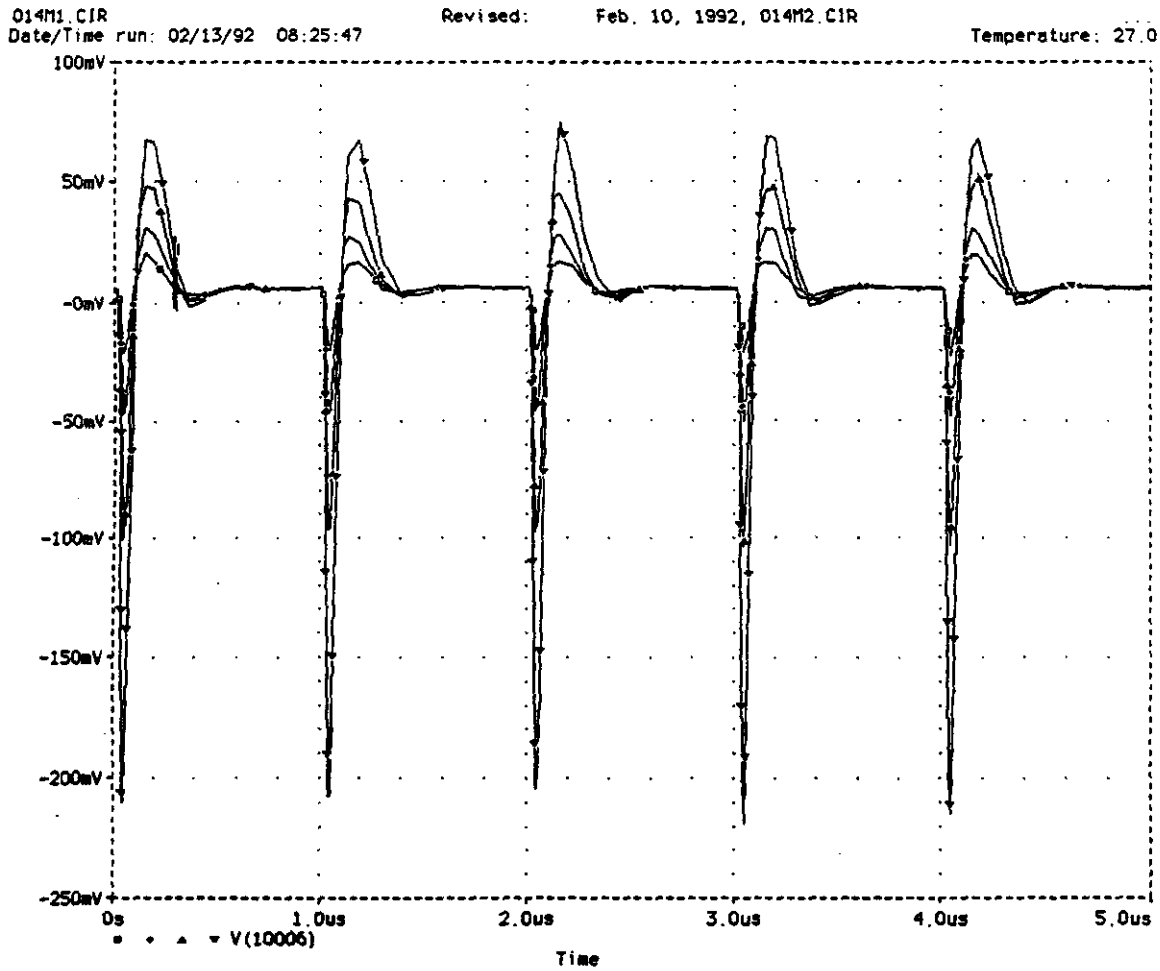


Figure 1c. Shaper Output Waveforms)

3.3.4 Digital Buffering

The digital buffering scheme is evolving at this time. The baseline design is moving toward a level 1 buffer consisting of either a straight dynamic shift register followed by data compression and transmission after the level 1 accept, or, data compression prior to the level 1 accept followed by immediate transmission. It is hoped that a design in a rad-hard CMOS technology will be sufficient for our purposes. Appendix A gives some thoughts on possible CMOS design and layout of a CMOS shift register, and, also, a discussion of a possible data compression scheme to be implemented on the same circuit die. Cost estimates depend dramatically on the precise area that the given die consumes. Estimates of the die area for various designs are in the range of $6.4x7mm^2$ to $6.4x17mm^2$ for a 128 channel die. The base cost of the wafer fabrication scales as the area of the chip die while the yield scales inversely to the die area. The total cost can in some cases scale as $(\text{chip die area})^2$. It is therefore crucial to understand the design precisely before accurate coat estimates can be made.

Digital Architecture Options

The two forms of on-chip, digital data-processing architectures we intend to develop are the straight and compressed delay. The straight delay will utilize standard CMOS shift registers while the compressed delay will use a clustering algorithm for data compression. For both the straight delay and compressed delay architectures we are developing an optional staggered column approach that will allow a 30 MHz clock rate in the event a 60 MHz rad-hard CMOS process is not available.

Straight Delay:

Figure 1 shows the first two stages of an N-Stage CMOS shift register (one stage = one delay) and Figure 2 shows the laid out cell of a single stage. This is a possible scenario which will be evaluated.

Data Compression:

The data compression is accomplished by transmitting cluster information instead of information about individual strips. The algorithm proceeds as follows: The raw data are first edge-detected, reducing the clusters to a series of edges. Then, using a pipelined architecture, the relative offsets of the edge boundaries are found. The resulting compressed data vector is then composed of the number of edges, the offsets of each edge from the previous edge, and, if desired, the total number of hits.

An illustration of the algorithm follows. Figure 3 shows a 16 bit (strip)detector with three "clusters" and a binary data vector representing the cluster edges. As the data vector is "passed through" the pipelined encoding algorithm, the edges are detected and the edge offsets counted. The decimal encoding of the three clusters in terms of pipeline stage, edge count, and accumulated offset reduce to the following:

Stage	# Edges	Offset
0	0	0
1	0	1
2	1	2/0
3	1	2/1
4	1	2/2
5	2	2/3/0
6	2	3/2/1
7	2	2/3/2
8	3	2/3/3/0
9	3	2/3/3/1
10	3	2/3/3/2
11	3	2/3/3/3
12	3	2/3/3/4
13	4	2/3/3/5/0
14	5	2/3/3/5/1/0
15	5	2/3/3/5/1/1.

Note that the "/" denotes an edge boundary and that it also needs to be encoded. The equivalent binary representation of the data vector in Figure 3 is

Stage	Accumulator	# Edges	Data Vector
0[Offset]	0	0	0010010010000110
[Edge]	0		
1	1	0	010010010000110
	0		
2	10	1	10010010000110
	01		
3	101	1	0010010000110
	010		
4	1010	1	010010000110
	0100		
5	1011	10	10010000110
	0101		
6	10111	10	0010000110
	010 10		
7	101110	10	010000110
	010100		
8	101111	11	10000110
	010101		
9	1011111	11	0000110
	0101010		
10	10111110	11	000110
	01010100		
11	10111111	11	00110
	01010100		
12	101111100	11	0110
	010101000		
13	101111101	100	110
	010101001		
14	1011111011	101	10
	0101010011		
15	10111110111	101	0
	01010100110.		

where the input data vector is in the right hand column and the accumulated edge boundary and offset are on the left. The edge location and offset are now represented by two separate binary vectors. Note that a single vector element can be processed per pipeline stage

allowing the algorithm to be implemented with a 60-MHz system clock. Also, note that the compressed data is right (or left) justified.

The prototype compressor architecture is shown in Figure 4. The compressor would accept an N-bit data vector, edge detect, and it compresses the edge data utilizing the previously described compression algorithm. The edge detector and compressor can be implemented with relatively straight-forward digital logic and shift registers for the required pipelined architecture. The resulting two output vectors would then be composed of the number of edges + edge boundaries and the number of hits + edge offsets.

Figures 5 and 6 show the Monte Carlo simulated compression ratios for a single-segment and a 4-segment 512-bit compressor. The single-segment compressor yields a 15:1 compression for a single cluster and 6:1 for five clusters, while the 4-segment provides a 7.5:1 and 4.5:1 for one and five is caused by the reduction in binary encoding efficiency with decreasing vector size and encoding clusters which overlap segment boundaries (such clusters require two or more binary numbers to encode).

Hence, compression efficiency is penalized as the number of segments are increased and data vector lengths are reduced (multiple segments are required to reduce the large input data vector to a manageable length). Techniques to improve segmented compression by combining segments before transmission are under investigation. Note that the sum of the offsets in a segment will always add up to the segment size, thus providing an end-of-transmission sum-check.

Staggered:

In the event that a reliable rad-hard, 60 MHz CMOS process cannot be found, we are developing a double-column, parallel pipeline architecture. Figure 7 shows the concept. The input signal is chopped and alternated between one of the two parallel pipeline columns. This allows the straight or compressed delays to operate at 30 MHz instead of 60 MHz.

N-STAGE CMOS DYNAMIC SHIFT REGISTER

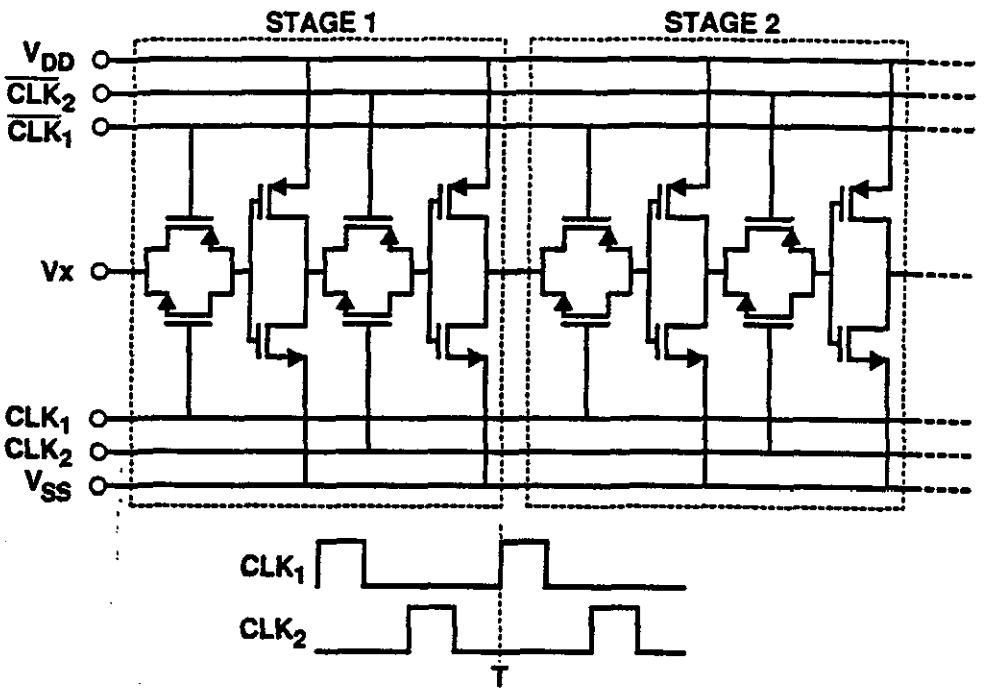


Figure 1. N-Stage CMOS Dynamic shift Register.

SINGLE-STAGE CMOS DYNAMIC SHIFT REGISTER CELL

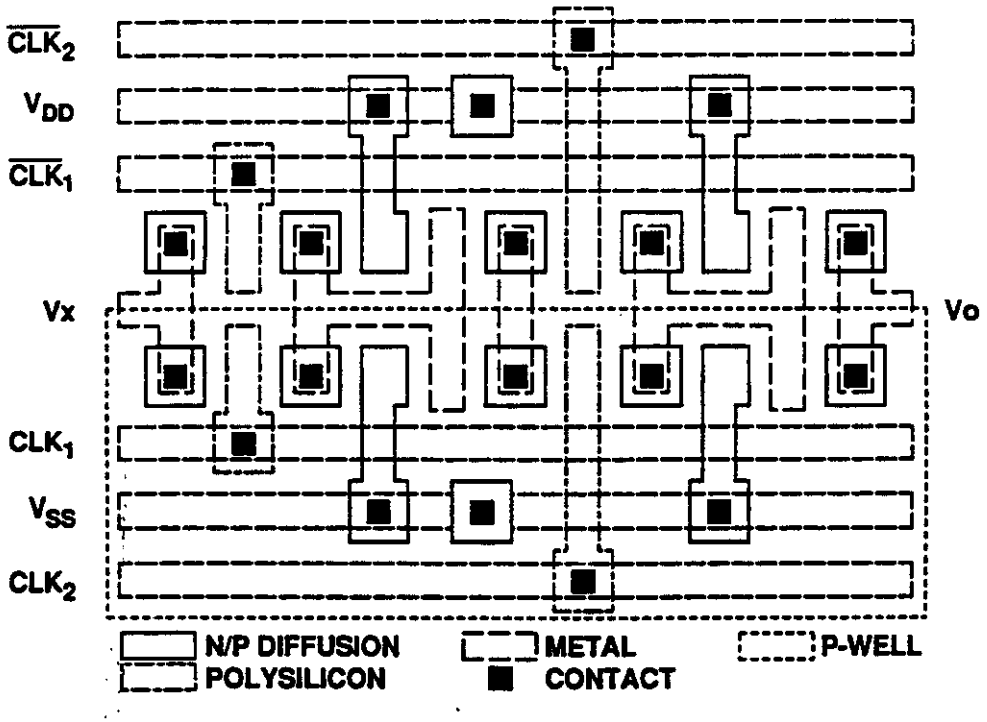


Figure 2. Single-Stage CMOS Dynamic Shift Register Cell.

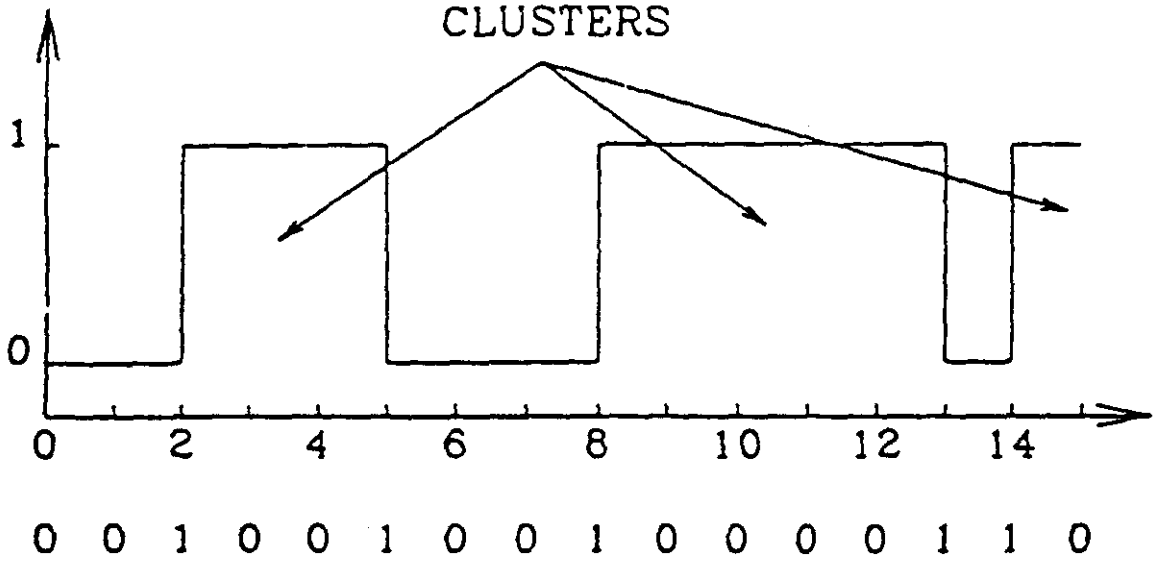


Figure 3. 16-Bit Detector With Three Clusters.

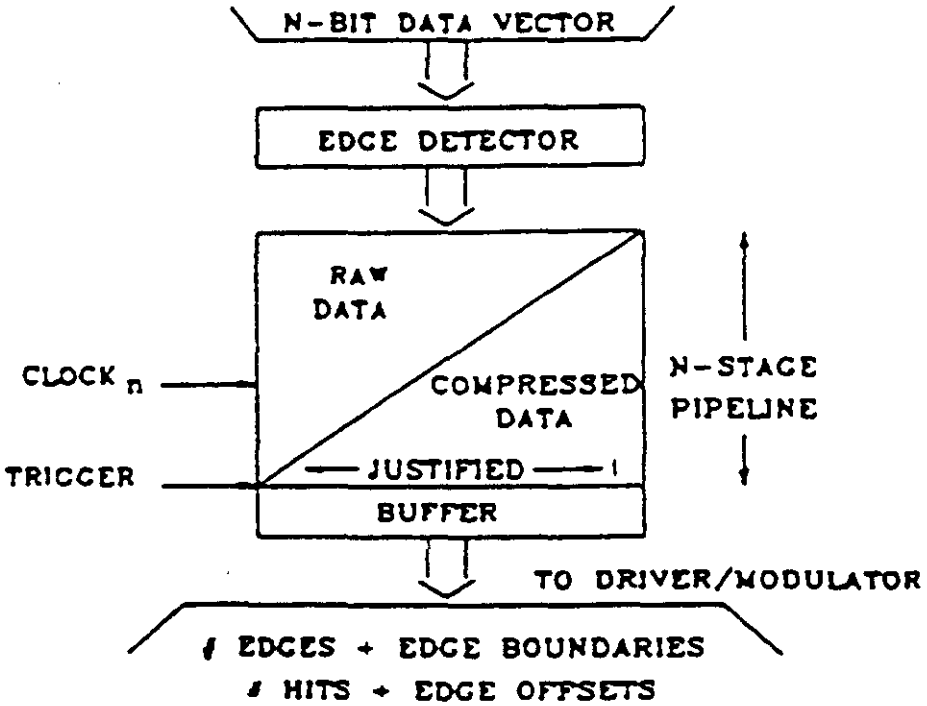
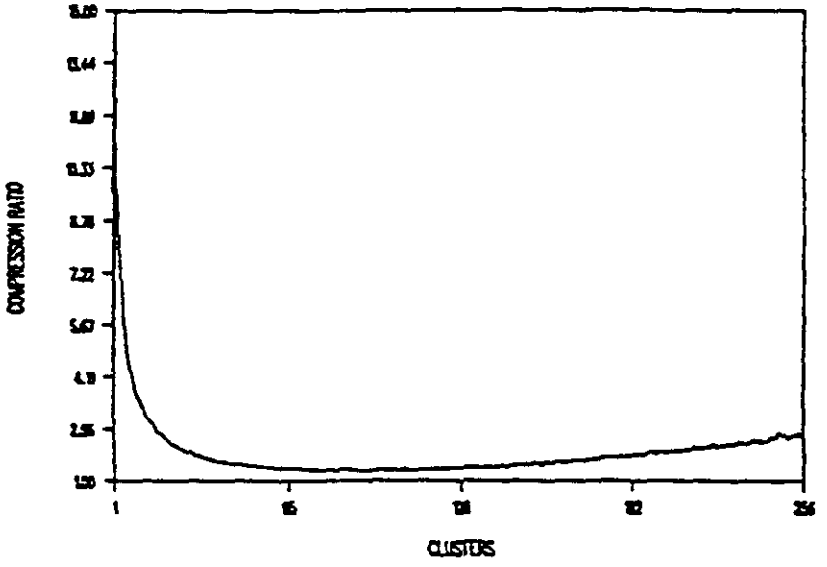


Figure 4. Compressor Architecture.



Fiqure 5. Compression Ratio for a Single-Segment, 512-Bit Vector.

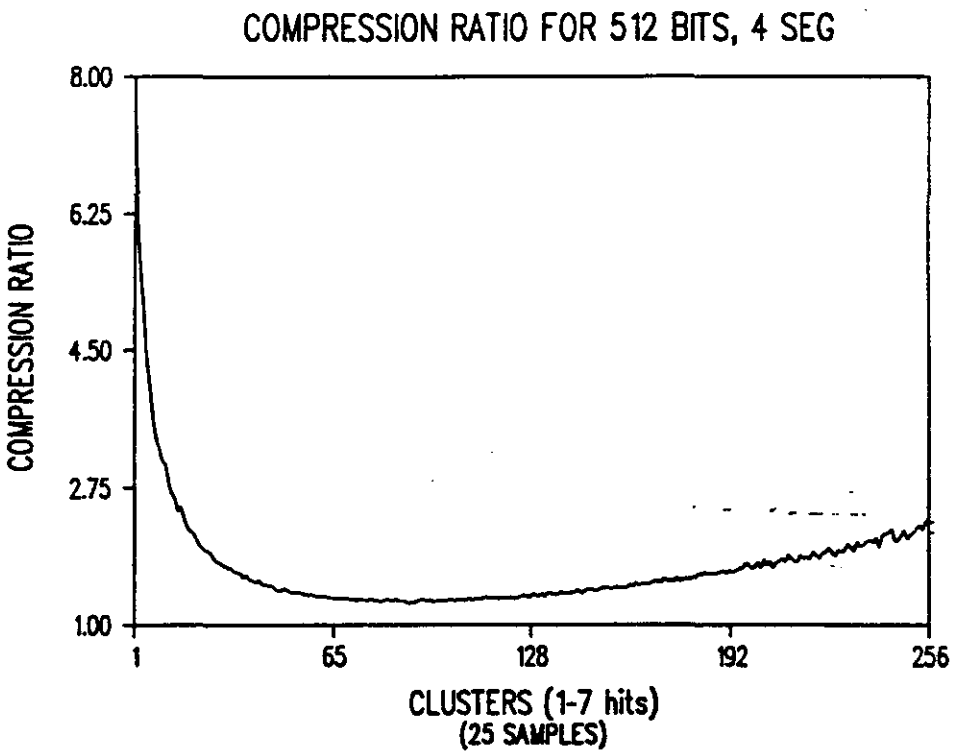


Figure 6. Compression Ratio for are developing a double Four-Segment, 512-Bit Vector.

ALLEVIATE BANDWIDTH CONGESTION WITH INPUT CHOPPING

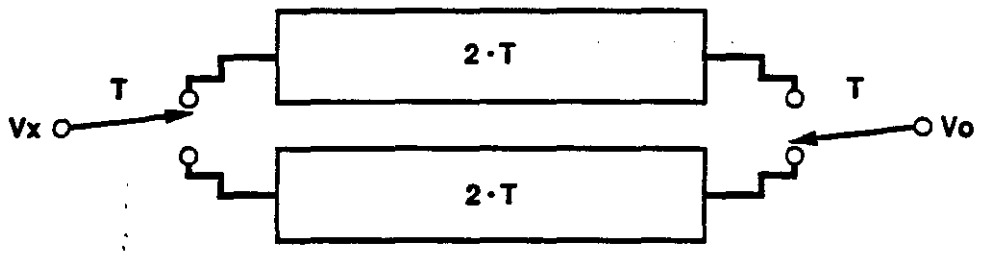


Figure 7. Alternate Input Double-Column, Parallel pipeline.

3.3.5 Optical Data Link

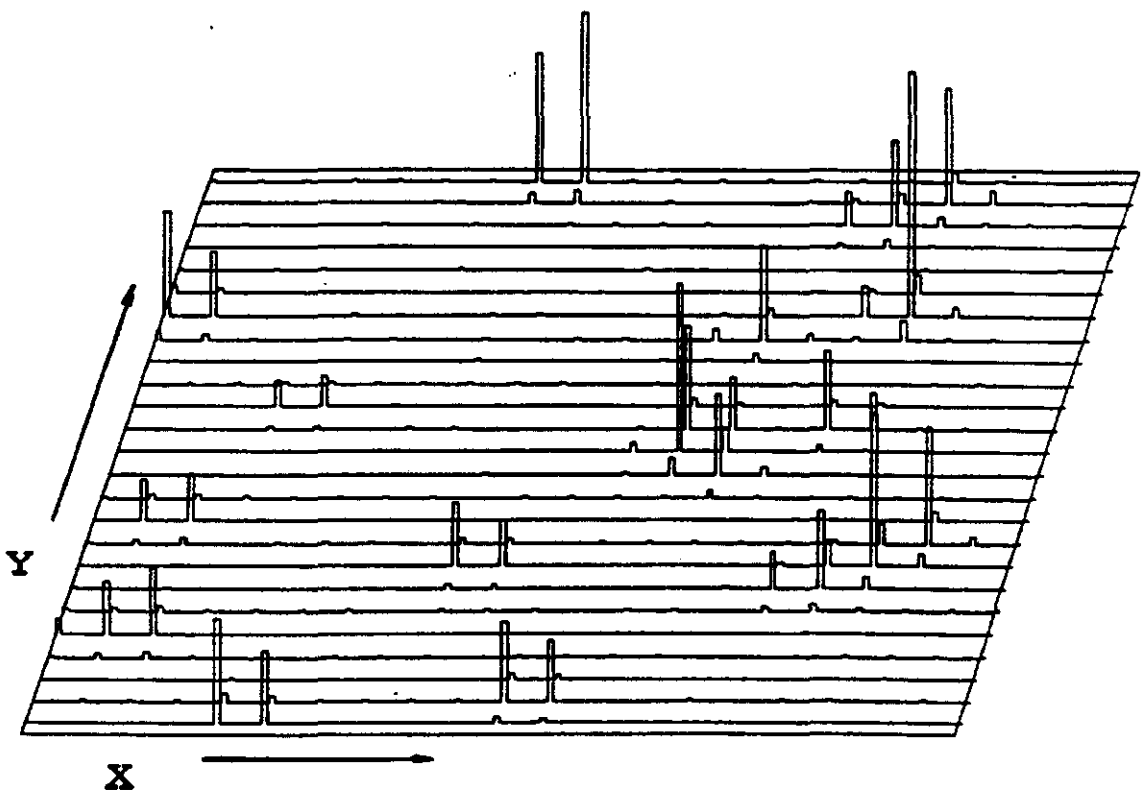
The consideration of the optical data link has made some advances. Several options are under consideration because the overall architecture of the data acquisition depends strongly on the achievable bandwidth of the optical data link. There is a cost tradeoff between system bandwidth and cost for each which we are in the process of understanding. The optical fiber and associated connectors are of concern. Radiation hardened fibers are available within our specifications. A multi-fiber connector is necessary in order to fit into the small volume of our system. AT&T is a source for this type of connector which are an industry standard that can handle either multi-mode or single mode fiber technologies. There does not appear to be a significant cost difference between the single-mode and multi-mode fiber and connectors. The multimode systems are well matched to the somewhat slower LED drivers, while, the single mode fibers are well matched to higher performance LASER diodes and even electrooptic modulators. Thus, to a good approximation, the cost of the fibers and connectors is the same per data link for all systems. Typical costs for an assembled, tested, 50 meter long link are around $380. Given the base cost of the fiber and connectors it is important to increase the bandwidth of the driver/receiver in order to minimize cost. The available radiation hardened LED drivers have been researched and the only suitable driver was found to be a Honeywell LED at roughly $120/link. This device has been designed to withstand the radiation dose which we expect in our system. Its data transfer rate is limited to around 50Mbit/s. LASER diodes and optical modulators are available in the GBit/s range. At the moment the radiation hardness of these devices is under investigation. In the event that these prove usable, there exist GaAs chip sets (e.g.,Vitesse Inc.) which could drive them at 1.25Gbit/s. The GaAs technologies are believed to be inherently radiation hard. This type of system would achieve cost parity with the LED system at a driver/receiver cost of $6500, by assuming redundant readout. This is within the range of modulator systems, so they remain under consideration. They would also require significantly fewer fibers in total, which could allow for an easier assembly and installation.

4 The Interpolating Pad Chamber Outer Tracker

4.1 Interpolating Pad Chamber

An Interpolating Pad Chamber (IPC) is a Multi-wire Proportional Chamber with a cathode plane consists of an array of specially designed pads. These pads sample the localized induced charge on the cathode plane due to an anode avalanche. The charge signals of the cathode pads are processed to provide position information on the location of the avalanche. The position resolution can be a small fraction of the pad size. Unambiguous pattern recognition is achieved because of the two-dimensional segmented cathode layout. Fig. 4.1.1 illustrates a computer simulated event display of such a detector.

An IPC commonly uses one of the following three types of charge division method: resistive charge division, geometrical charge division and capacitive charge division.



4.1.1 IPC with Resistive Charge Division

The cathode plane of an IPC with resistive charge division is divided into an array of rectangular pads, (see Fig. 4.1.2). All pads underneath an anode wire are interconnected by a resistive strip with uniform resistivity. Charge sensing preamplifiers are connected to certain pads at regular intervals along each pad row. Typically, the induced cathode charge is collected by 2–3 preamplifiers, and the centroid of the avalanche x_c can be calculated with the following formula:

$$x_c = \frac{\sum x_k Q_k}{\sum x_k}$$

where x_k is the position of the kth readout pad, and Q_k is the charge collected from that pad.

The position resolution is determined by the total capacitance of each readout channel, the induced charge signal and the shaping time of the electronics. The position linearity is mainly determined by the uniformity of the applied resistive strip over each pad row. The complexity in applying the resistive strips over a large area while maintain a good uniformity in its resistance make this type of cathode less favorable for the GEM tracker.

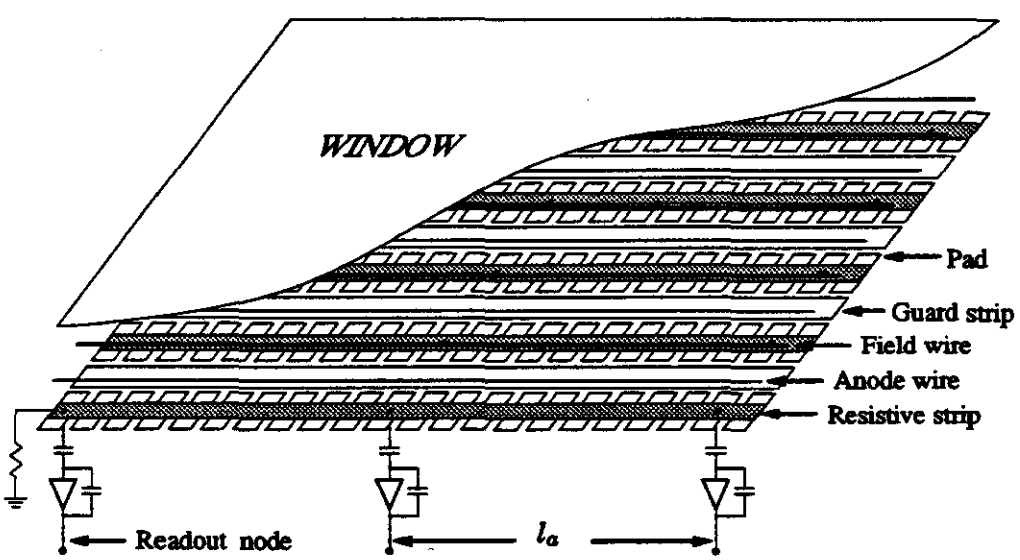


Figure 4.1.2: Illustration of an IPC with resistive charge division

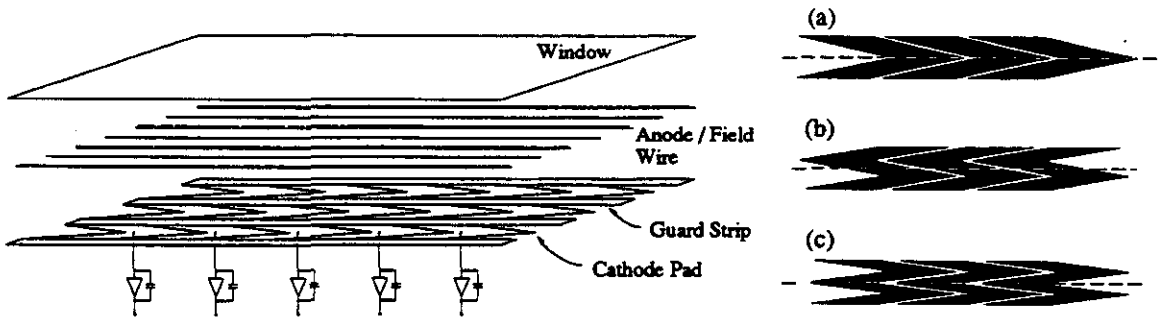


Figure 4.1.3: Illustration of an IPC with geometrical charge division

4.1.2 IPC with Geometrical Charge Division

A "Chevron Pad Chamber" is one example of pad chambers with geometrical charge division. Fig. 4.1.3 shows the schematic structure of a chevron pad chamber, and several possible pad geometries.

Chevron Pad Chambers as large as (2 m×0.5 m) have be used in the heavy ion experiment E814 at the AGS of BNL. Detailed study on position resolution and position linearity have been performed. Fig. 4.1.4 shows the position resolution as a function of the anode charge for one test chamber under 5.4 keV x-ray irradiation. With the proper geometry, the differential non-linearity of the test chamber can be maintained at less than 10%.

The IPC outer tracker use the chevron pad cathode as the baseline design. The cathode layout is illustrated in Fig. 4.1.5. The spacing between readout (along the anode wire direction) is 5 mm. The pad width (across the wire direction varies from $\sim$ 2 cm to $\sim$ 10 cm, depending on location. Detector with similar pad layout has been used in a two-dimensional x-ray imaging experiment with good results. Based on computer simulation, a 50 μm position resolution can be achieved, provided that the electronics noise of individual channel be kept less than 0.5% of the induced cathode charge.

One major disadvantage of the chevron pad cathode design is that the capacitance seen by the preamplifier is very large, due to the long zigzag interfaces between pads. By increase the gap width between pads, one can reduce the capacitive load to the preamplifier. However, experimental measurements indicates that the position linearity degrades with the increase of the gap width. Computer simulation shows that one can modify the pad geometry to compensate the increase of gap width. This needs to be experimentally confirmed.

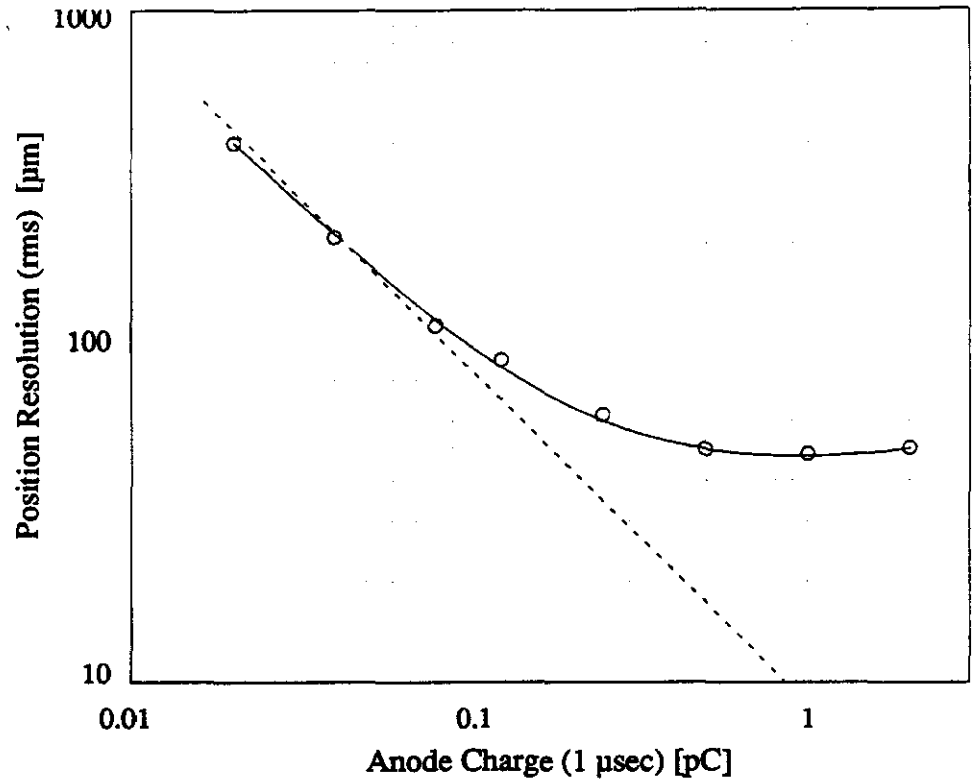


Figure 4.1.4: Position resolution as a function of the anode charge of a chevron test chamber. The readout spacing is 12 mm, shaping time is 1.4 μsec, the radiation is 5.4 keV x-rays.

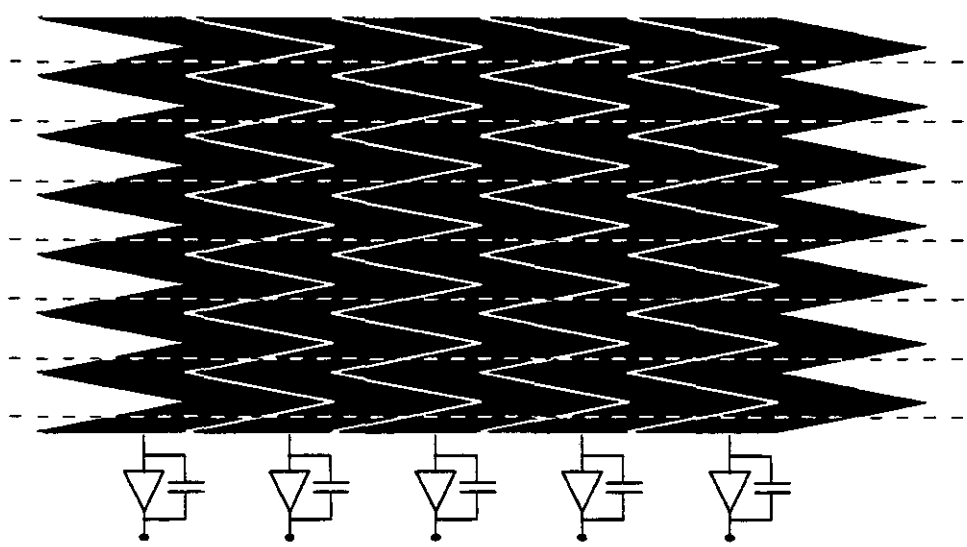


Figure 4.1.5: Chevron pad layout of the baseline IPC design. The dashed lines indicate the anode wire locations.

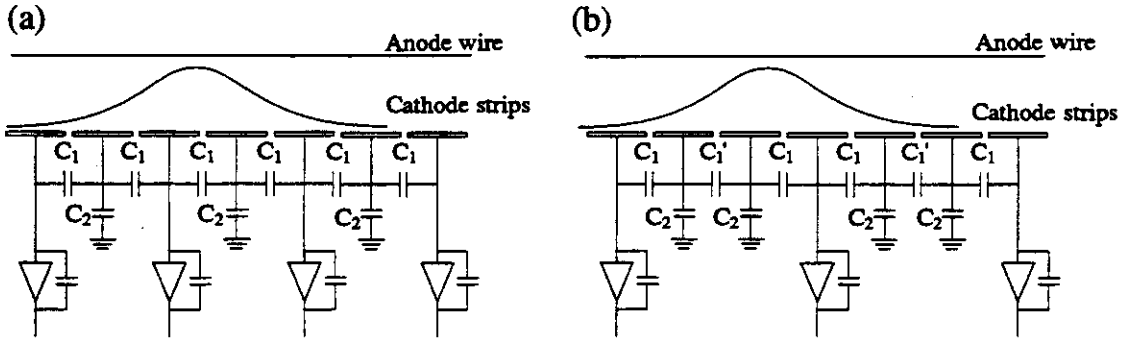


Figure 4.1.6: Examples of the capacitive charge division method. (a) Single Intermediate Strip Cathode; (b) Two Intermediate Strip Cathode.

4.1.3 IPC with Capacitive Charge Division

A very attractive alternative cathode geometry is the Intermediate Strip Cathode developed at BNL. Two examples of this cathode geometry are illustrated in Fig. 4.1.6. In this scheme, the induced charge on the intermediate cathode pad is coupled to the nearest readout pads via the inter-pad capacitances. Good position linearity can be achieved if the inter-pad capacitance is much greater than the pad-to-ground capacitance. Obviously, the width of the pad (across the wire direction) has to be large enough to maintain a strong inter-pad coupling. Its major advantage over the chevron pad design is the significant reduction in the capacitive load to the preamplifiers which translates to a much lower electronics noise. For example, the Two Intermediate Strip method may be used to replace those chevron pads whose widths are more than 5 cm. While the Single Intermediate Strip method is ideal if we choose to reduce the readout spacing from 5 mm to, say, 3 mm.

The thin cathode board and the conductive graphite/epoxy hard back will increase the pad-to-ground capacitance. As a result, a fraction of the induced charge (10~20%) will be lost to the ground, and the position linearity may deteriorate. Experimental testing is needed to evaluate the overall benefit of this cathode design.

4.2 Design Parameters

The design parameters of the IPC system are set by the resolution, occupancy, and speed requirements imposed by the operational goals of the Central Tracker. In this section we discuss the optimization of these parameters. The conditions under which the IPCs must successfully operate, as well as the design goals of the system, are summarized in Table I.

Beam Crossing Rate	62 Mhz
Charged Track Density/Min Bias Event	$dN/d\eta d\phi = 1.2$
# Min Bias Events/ Crossing @10^{34} $cm^{-2}s^{-1}$	16
Tracks/sec-mm wire @10^{34} $cm^{-2}s^{-1}$	1×10^4 $s^{-1}mm^{-1}$
Integrated Charge/yr-cm wire @ $10^{34}cm^{-2}s^{-1}$	1.4 C/cm-yr
Position Resolution - Pads	50 microns
Position Resolution - Wires	600 microns
Occupancy @ 10^{34} $cm^{-2}s^{-1}$	< 10%

Table I

4.2.1 Occupancy

For a minimum bias event cross section of 100 mb, one expects 1.6 minimum bias events per bunch crossing. Each of these min. bias events has an associated primary track density $dN/d\eta d\phi=1.2$, to which a factor of 1.5-2 should be multiplied to account for secondary particles, delta rays, and loopers. In a physics event, the track multiplicity from the rare process must be added to this minimum bias background . As one example, a 300 GeV Higgs event adds roughly 1.9 to the value of $dN/d\eta d\phi$. If an input channel is unavailable for subsequent hits for N_B bunch crossings, then the occupancy in a rare physics event at a luminosity of 10^{33} cm^{-2} s^{-1} is given by:

$$Occupancy = (d\eta d\phi)_{cell}((N_B * 1.2 * 1.6) + N_{physics})f_{sec}$$

Where f_{sec} accounts for secondary particles, and $N_{physics}$ represents the additional background associated with the spectators in the physics event. At a luminosity of 10^{34} cm^{-2} s^{-1} the number of minimum bias events per crossing increases to 16, all other factors remaining the same. The quantity $d\eta d\phi_{cell}$ refers to the cell size required to obtain a track point . Because position reconstruction using cathode readout requires at least three adjacent pads, the cell size is set to three times the size of the pads. One expects to do better than this in practice, as measurments of the double track resolution of IPC s have shown that tracks can be resolved when the track separation is significantly less than one pad width. Extensions to this study are now underway to determine the relationship between track separation and resolution. For now, taking the worst possible case of a three pad wide cell size, the resulting occupancy values are summarized in Table II.

For a pad size of $d\eta d\phi_{pad}$=0.0007, and assuming N_b=2 and $N_{physics}$=1.9, we obtain an occupancy of 2% at

Luminosity	Occupancy
10^{33}	$9*d\eta d\phi_{pad}(N_B+1)$
10^{34}	$90*d\eta d\phi_{pad}(N_B)$

Table II

a luminosity of $10^{33}cm^{-2}s^{-1}$, and 12% at $10^{34}cm^{-2}s^{-1}$.

4.2.2 IPC Response Time

It should be clear from the discussion in the last section that a fast detector response is a critical aspect of the Central Tracker IPC system. The value of N_b=2 assumed in the occupancy calculation requires a response time of less than 40 nsec. This is quite different from the shaping times normally used in reading out the induced cathode signal in wire chambers. Shaping times in the microseconds are common, allowing a more complete integration of the induced signal. A lower limit to the integration time which can be used is given by the characteristic time for collection of the ionization electrons at the wire. Integration times shorter that this will result in a large reduction in the observed signal, large event to event differences in the peak signal, and a strong dependence of the peak signal on the shaping time. A operational requirement of the IPCs, therefore, is that they have an electron collection time of order 20 nsec. At the same time, the Lorentz angle of the gas at 0.8 kG must be kept under 10 degrees, as the chambers must be canted at this angle with respect to the magnetic field to minimize the position resolution degradation due spreading of the induced signal along the cathode, and mechanical constraints make an cant angle larger that 10 degrees difficult. A gas mixture suitable for Central Tracker use in the IPCs must, therefore, be relatively fast, with a small Lorentz angle. These two requirements are contradictory, at least to first order, as the Lorentz angle of a gas mixture scales with the mean time between collisions of the electrons with atoms in the gas. However, it appears that suitable gas mixtures do exist which satisfy our requirements. An example are CF_4 - CO_2 mixtures, which the GEM Central Tracker Group at Indiana University has been investigating using a chamber designed to make precision drift velocity and Lorentz angle measurements. Results show that these gas mixtures are relatively fast, and exhibit Lorentz angles below 10 degrees at 8 kG over a wide CF_4 concentration range. The results are summarized below. Figure 4.2.1 shows the dependence of Lorentz angle on mixture at a fixed value for the electric field. Figure 4.2.2 shows the dependence of drift velocity on relative concentrations at a fixed value of the electric field. Figure 4.2.3 shows the drift velocity as a function of field for a 50-50 mixture, and Figure 4.2.4 shows the behavior of the Lorentz angle on field for a 50-50 mixture.

The results of the gas study summarized here have been used in a simulation of the strawman IPC chamber using the wire chamber simulation program GARFIELD. The critical operational parameters used in this simulation are listed in Table III.

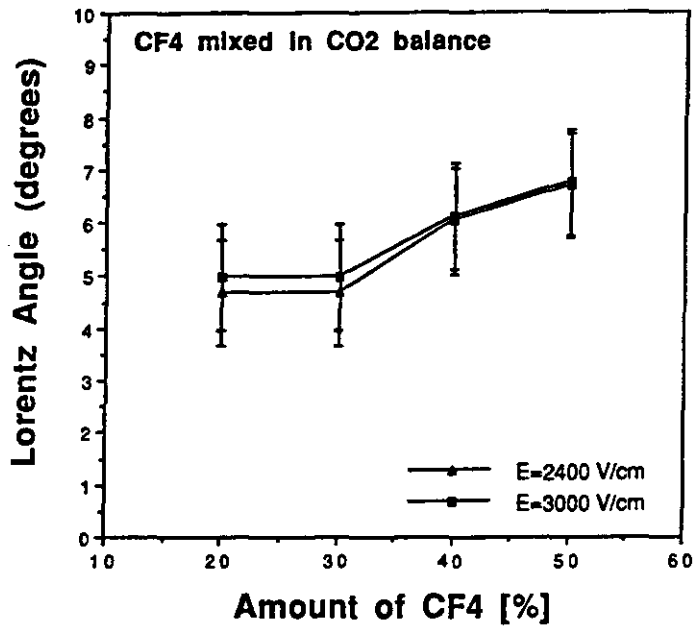


Figure 4.2.1
Lorentz Angle vs Freon Concentration

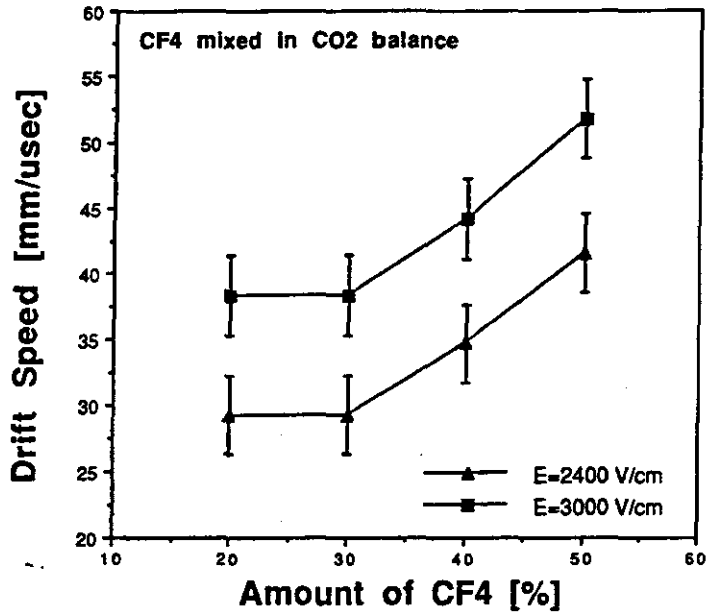


Figure 4.2.2
Drift Velocity vs Freon Concentration

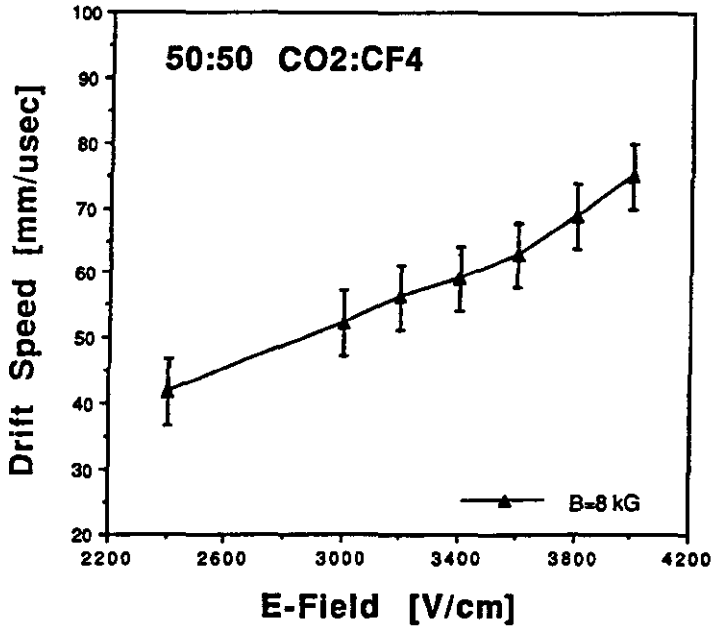


Figure 4.2.3
Drift Velocity vs Electric Field

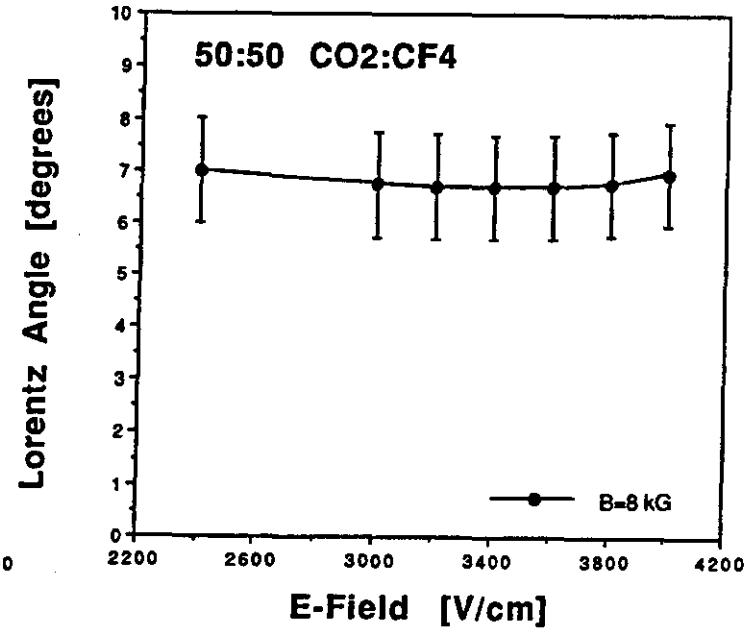


Figure 4.2.4
Lorentz Angle vs Electric Field

Wire Spacing	2 mm
Anode-Cathode spacing	2 mm
Wire Dia.	40 microns
Voltage	3000 V
Gas	50-50 CO_2-CF_4

Table III

The results of the GARFIELD simulation are summarized in Figures 4.2.5 and 4.2.6. Figure 4.2.5 shows the equipotential lines calculated for this chamber geometry, and Figure 4.2.6 shows the contours of equal electron drift time. Contours in Figure 4.2.6 are at 5 ns intervals. Figure 4.2.6, which is the primary result of this study, demonstrates that a very large fraction of the chamber volume is contained within the 20 ns contour. It is apparent from this figure that the maximum delay between the traversal of the particle and the arrival of the first electron at the wire is less than 20 ns, as is the spread in arrival times for electrons coming from a given particle track.

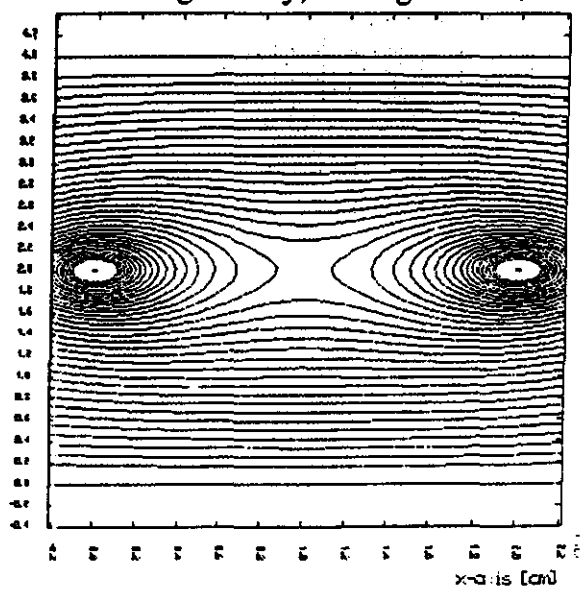


Figure 4.2.5
Equipotential Lines in Baseline Chamber

The chamber geometry is set by the requirement of a fast electron collection time on the one hand, and by mechanical tolerances on the other. It is clear that a significantly larger anode to cathode distance would result in an unacceptably long electron collection time. A significantly smaller separation would result in unacceptably tight mechanical tolerances, due to the increase in chamber capacitance. The chamber gain is given approximately by

$$M = ke^{CV_0}$$

so that a large chamber capacitance results in a more rapid increase in gain for a given voltage change, with correspondingly larger sensitivity to mechanical tolerances. It can be shown that

$$\Delta M/M = (\Delta Q/Q)\ln M$$

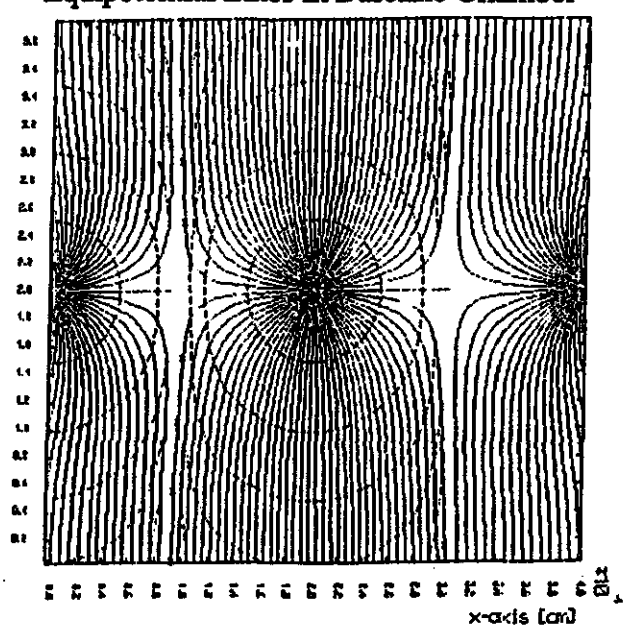


Figure 4.2.6
Equal Drift Time Contours in Baseline IPC

and,

$$\Delta Q/Q = C/2\varepsilon_0 \Delta a/a$$
$$\Delta Q/Q = (Cl/2\varepsilon_0 s)\Delta l/l$$

where $Q = CV_0$ is the charge per unit wire length, M is the chamber gain, a is the wire radius, l is the anode/cathode spacing, and s is the spacing between wires. For the baseline geometry, which has a capacitance of 7.6 pf/m, a 2 mil variation in the anode/cathode spacing results in a 10% variation in the gain of the chamber. The wire diameter is also constrained at large values by limits set by mechanical tolerances. On the other hand, a large wire diameter results in a larger field at given chamber gain, and hence a shorter electron collection time. Other factors which are usually considered in setting the wire diameter, such as the tension required and forces on the support structure, are not particularly relevant here due to the very short wires used in the IPCs. Because the chamber capacitance is not strongly dependent on the wire diameter, having a value of 6.8 pf for a 20 micron wire, and 7.6 pf for a 40 micron wire, the operating voltage for a given gas gain is only slightly higher for the thicker wire. It is not clear whether the slight increase in chamber speed is worth the tighter mechanical tolerances at this point, and the ultimate choice of wire diameter remains an open issue.

The operating voltage in the baseline has been determined by calculating the relative capacitance of the chamber used to make the Lorentz angle measurements described above, and the baseline chamber. The test chamber has a capacitance of 5.71 pf/m and operates at 4 kV, while the baseline has a capacitance of 7.6 pf/m. Chamber gain is fixed for a given charge per unit length on the anode wire, leading to a 3 kV estimate for the operating point of the baseline detector.

4.2.3 Chamber Gain

The proper value for the IPC gas gain is constrained, in this case, by aging and space charge effects on the one hand, and by signal to noise considerations on the other. We'll consider first the minimum allowable chamber gain. It can be shown that 1 percent of pad width position resolution requires approximately a 0.5% signal to noise ratio in the induced signal measurement. A lower signal to noise ratio results in a position error dominated by measurement errors and not by irreducible processes. This effect is shown in Figure 4.2.7, which plots the observed position resolution in an IPC chamber versus the gas gain. At low values for the gas gain the resolution is measurement error dominated, and hence varies roughly as the inverse of the gas gain. Under the operating conditions used to generate the data in Figure 4.2.7, the position resolution of the chamber under study approaches an asymptotic value at a gas gain of 2×10^4. The gas gain above which the chamber

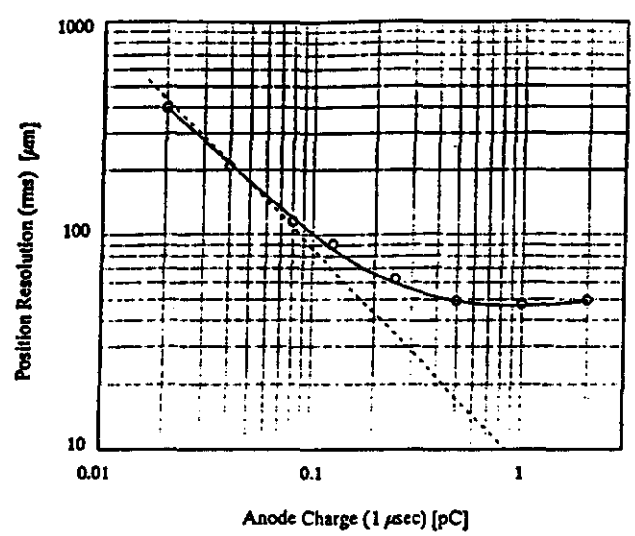


Figure 4.2.7
Chamber Resolution vs Gas Gain

resolution is dominated by irreducible effects is determined by the noise in the front end readout electronics, normally expressed in equivalent electrons. The dominant noise component, due to the input transistor of the preamplifier, can be expressed as

$$\delta_{series} \propto C_{in}/(g\sqrt{t_{shaping}})$$

Three points should be made about the expression above. First, it is apparent that noise increases with the inverse square root of the shaping time. The short shaping times required in this application will result in a decrease in the signal to noise ratio, all other things being equal. Second, noise is proportional to the input capacitance. Each pad has a mutual capacitance with adjacent pads, and noise considerations dicatate that this capacitance be kept as small as possible. We consider this in some detail in the next section. Finally, this noise component can be decreased by increasing the transconductance of the input transistor. That is, decreased noise can be bought at the expense of increased power. Based on small extrapolations from the performance of existing designs it is reasonable to expect a noise figure of 1000 electrons for an input capacitance of 10 pf, with a peaking time of 20 ns. Using this value for the expected noise in the readout chain, we require a signal of roughly $2x10^5$ electrons to obtain a 1% measurement error. The number of ion pairs produced in a 4 mm gap in 50-50 CO_2-CF_4 is 60. The integrated signal on the wire for a gas gain G, therefore is 60 G. The induced signal on a cathode pad is smaller than this, however, as a result of two factors. First, the induced signal is divided between the two cathodes, plus the adjacent wires, so the induced signal on a given cathode is one third the total. Second, the integration time is a small fraction of the development time of the induced signal, set by the ion drift time. The time development of the induced signal can be shown to be:

$$q(t)/q_{tot} = (2\ln(r_c/r_a))^{-1}\ln(1+t/t_0)$$
$$t_0 = (r_a^2/2\mu_+V)\ln(r_c/r_a)$$

Where r_a and r_c are the anode and cathode radii, V is the operating voltage, and μ_+ is the ion mobility. The time scale for development of the induced signal is set by the ion mobility, with the characteristic time being the time taken for the ions to drift a distance of one wire diameter. This equation can be used to estimate the fraction of the total induced signal which would result from a 20 ns integration time. For the baseline chamber geometry and nominal values for the ion mobility, this fraction is found to be 20%. The total signal on a cathode pad , therefore is equal to

$$Q_{cathode} = 60G \times 0.2 \times 0.3 = 2x10^5$$

From this result, we find that the gain required to obtain a signal to noise ratio of 200 is 50,000. This value must now be checked against wire aging and space charge constraints, which set an upper limit on the gas gain. This discussion is presented in section 4.2.5.

4.2.4 Input Capacitance

As discussed in the previous section, the capacitance seen at the input of the preamplier plays a critical role in determining the position resolution of the IPCs. This capacitance includes the

mutual capacitance between pads, along with the capacitance between a pad and the readout lines, ground planes, etc. The present design of the cathode calls for readout lines lying on the opposite side of a 0.5 mm thick sheet from the pad plane, with no ground plane between the readout and pad layers. Under these conditions, the pad-to-pad capacitance dominates. The capacitance between adjacent conductors having thickness t, width w, and separation s, lying on a dielectric with constant k, is approximately given by

$$C(pF/in) = 0.31t/w + 0.23(1+k)\log_{10}(1+2w/s+w^2/s^2)$$

Using nominal values for the parameters above, one obtains a capacitance of roughly 1 pf/cm. Measured values of interpad capacitance in IPCs tend to be smaller than this value, with 0.5 pf/cm being typical. Using this measured value, the range of pad capacitances in the IPC baseline is 10-70 pf. The upper end of this range presents a definite challenge - designing a 20 ns peaking time preamplifier with sufficiently low noise at this input capacitance. A serious effort is now underway at BNL to design a preamplifier which meets these requirements. This potential problem can be alleviated to a large extent by a modification to the design of the cathode plane. The use of chevron pads, rather than the more conventional rectangular pads, is dictated by the large ratio of pad width to anode-cathode separation in the baseline design. Under these conditions, a rectangular pad would exhibit substantial position non-linearities across the pad. However, the use of chevron pads results in a much larger pad capacitance, compared with rectangular pads, due to the larger edge length. An alternative to the present 0.5 cm chevron pad design would employ roughly 0.2 cm rectangular pads, with correspondingly longer lengths. A 0.2 cm wide rectangular pad would exhibit acceptable non-linearities, while the range of pad capacitance in a rectangular pad design would be 5-35 pf. In addition to the factor of 2 decrease in capacitance, the use of a narrower pad also improves the position resolution in the obvious direct way. The primary drawback of a narrow rectangular design is a further departure from the "space point" ideal. It should be noted parenthetically that, due to the effect of capacitance on noise and, therefore, position resolution, one does not have infinite freedom to enlarge the pad area to satisfy cost constraints.

4.2.5 Rate Effects

The effects of the high rate SSC environment on IPC performance falls into two categories. These are chamber aging, and the effects of space charge on chamber gain. Chamber aging refers to a gradual decrease in the gas gain in the chamber due to a buildup of deposits on the electrodes, resulting in narrowing operating plateau and eventual chamber breakdown. This effect is directly proportional to the integrated charge collected per unit length of wire. At a luminosity of $10^{34}cm^{-2}\,s^{-1}$ the amount of charge collected per SSC year per cm of wire in the IPCs, assuming a gas gain of 50,000, is 1.4 C/cm at a radius of 30 cm. For a given integrated charge, chamber aging depends primarily on gas composition. Measurements have been carried out on chamber aging using the gas currently proposed for the IPCs, namely, CF_4-CO_2 mixtures. For a 50-50 mixture the measured decrease in the operating current of a test chamber was found to be

$$(I_0 - I)/I_0 = 0.07C^{-1}cmYr$$

This result confirms the expectation that these gases should exhibit very small aging effects. It is well known, in fact, that Freon can be used to recover a chamber which suffers from aging. The conclusion is that even at the rather high gas gain required by signal to noise requirements, the chambers should be able to operate for a number of years at 10^{34} $cm^{-2}s^{-1}$ while suffering minimal aging effects.

The buildup of space charge in the IPC s also results in a decrease in gain of the chamber at high rates. At a luminosity of $10^{34}cm^{-2}s^{-1}$, the charged track rate in the IPCs is $2x10^9$ s^{-1} in each IPC, or $1x10^4$ s^{-1} mm wire $^{-1}$ in the innermost layer of IPCs. At this rate, the buildup of space charge can be expected to result in some decrease in gain. Measurements conducted on gases with ion clearing times similar to that of Freon - CO_2 mixtures indicate that the reduction in gain should be small. To confirm this, a critical part of our R&D plan during the coming year is an investigation of space charge effects on chamber operation at high particle fluences.

4.3 Mechanical Design

4.3.1 Introduction

The following sections describe the interpolating pad chamber tracker array that has been proposed as a part of the GEM detector for the Superconducting Super Collider (SSC) project. The IPC array consists of four major sections: the barrel chambers, the barrel array support structure, the endcap (or forward) chambers and the endcap array support structure. In addition, there are utilities for both the forward and barrel regions (high voltage for anode wires, signals, low voltage and cooling for "on-board" electronics, and gas for the chambers).

4.3.2 Interpolating Pad Chamber Design Parameters

Table 1 summarizes the design parameters for the IPC tracker (barrel and endcap). Note that $d\eta d\phi$ was assumed to be 0.0007 when numbers of channels were calculated. Figure 1 is a quadrant view of the tracker. Figure 2 is an end view of the barrel section and shows the proposed barrel superlayer arrangement. The locations of the various layers of pads are shown in Table 4.

4.3.3 GEM IPC Tracker Design Constraints

The GEM IPC tracker is designed to operate in a high radiation (1 Mrad/year), high magnetic field (0.8 Tesla) environment for an extended period of time with maximum dimensional stability. In addition, the radiation length must be minimized through judicious use of materials. Table 2 shows the proposed stability requirements for the IPC tracker.

4.3.4 Description of GEM IPC Tracker Array

The GEM IPC tracker array consists of a total of 80 barrel and 80 endcap (or forward) chambers arranged in tandem units (ie. superlayer). The barrel superlayers are rotated 4.5 degrees per superlayer to reduce concentrations of higher radiation length material at specific azimuthal angles. The endcap chambers are rotated 9 degrees per level. There are four levels of superlayers for both the barrel and forward regions.

The endcap IPC modules are trapezoidal in shape and are arranged as shown in figure 3. The electronics are on the outside perimeter of the endcaps (end of module) as opposed to being located along the side of a module (barrel section). This feature reduces the radiation length-intensive material at lower angles of θ and permits relatively easy access to the electronics for troubleshooting.

4.3.5 Description of GEM IPC Module Design

The GEM interpolating pad chamber module is designed to minimize radiation length while maximizing mechanical stability. Composite materials are used throughout to achieve this end.

Figure 4 shows a typical barrel module cross-sectional view. The module consists of the following components for each of the two chambers: gas envelope, gas envelope supports, outer cathode plane, anode wires, anode wire supports, and the chevron cathode pad pc board. In addition, a graphite-epoxy corrugated core sandwich hardback is used to add rigidity.

The "on-board" electronics are arranged on either side of a rectangular cross sectioned aluminum cooling tube and are designed to be mechanically and thermally isolated from the pad chambers. Connection between the cathode pads and electronics is via flexible printed circuits (mylar or kapton).

The anode wires (25 to 40μ diameter gold-plated tungsten) could operate at a potential of 3 Kv. The distance between the anode wires and cathode planes is nominally 2 mm. Therefore, the anode wire supports need to be relatively good insulators. Graphite-epoxy (Lrad of 25 cm) has a volume resistivity on the order of 10^{-3} ohm-cm. One way to significantly increase this is to coat the laminate with epoxy (volume resistivity approx. 10^{14}ohm-cm). This is somewhat risky, due to possible voids in the epoxy or danger of stray graphite fibers. Surface breakdown must also be considered.

Kevlar (aramid)-epoxy composite laminate is a strong possibility. Volume resistivity of Kevlar is in the 10^{15} ohm-cm range. Furthermore, the CTE of Kevlar-epoxy laminates is on the order of $-1\text{x}10^{-6}\ C^{-1}$, similar to that of graphite-epoxy. The modulus is about one third of graphite epoxy. The radiation length of Kevlar-epoxy is approximately 30 cm.

The design of the chevron pad cathode printed circuit board is still being researched. Some of the current thinking includes an aluminized Mylar chevron

pad skin and an aluminized Mylar signal trace skin with a 10 mil polymer rigid foam layer in between. Mylar is also available with other coating materials (copper, gold, etc.) if aluminum becomes a liability. Other ideas for the cathode pads include Kevlar/aluminum (DuPont Thermount©technology), Mylar/aluminum or Mylar/copper multilayer boards.

The gas envelope has been included to contain the chamber gas mixture (CO_2 and CF_4) while preventing distortion of the outer cathode plane due to gas pressure. The cathode plane will be perforated, allowing gas into the cavity between the cathode and the gas envelope.

The worst-case superlayer module deflection was calculated. Assuming a uniformly-loaded simply-supported composite beam, the relationship is:

$$y = \frac{5\omega l^4}{384EI}$$

where: y is the deflection, ω is the loading per unit length, l is the length, E is the composite modulus of elasticity and I is the composite area moment of inertia.

The deflection is approximately TBD mm.

Parameter	Quantity
Lorenz angle	12 degrees
Number of sectors - barrel superlayer	20
Number of sectors - endcap superlayer	10
Number of superlayers - barrel and endcap	4
Number of chambers per superlayer	2
Chamber depth (cathode to cathode)	4 mm
Anode wire pitch - barrel and endcap	2 mm
Anode wire diameter	$25 \leq$diam.$\leq 40\ \mu$
Anode wire potential	3 Kv
Barrel IPC superlayer length	200 cm
Barrel IPC array inner radius boundary	35 cm
Barrel IPC array outer radius boundary	70 cm
Endcap IPC minimum axial boundary	110 cm
Endcap IPC maximum axial boundary	140 cm
Chevron pad width in ϕ	0.5 cm
Number of barrel pads	222360
Number of pads (each endcap)	87280
Electronics power dissipation - barrel	13.6 Kw
Electronics power dissipation - each endcap	5.3 Kw

Table 1: GEM IPC Array Design Parameters

Parameter	Quantity
Between superlayer modules in ϕ	25μ
Between superlayer modules in z	100μ
Between endcaps and barrel in ϕ	25μ
Between endcaps and barrel in z	100μ
Maximum superlayer module deflection	1000μ
Module transverse flatness	160μ
-or-	20μ over adjacent pads

Table 2: GEM IPC Array Stability Requirements

FIGURE 1

GEM Central Tracking

QUADRANT VIEW

NOTE: BARREL ROTATED 11 DEG. ABOUT Z

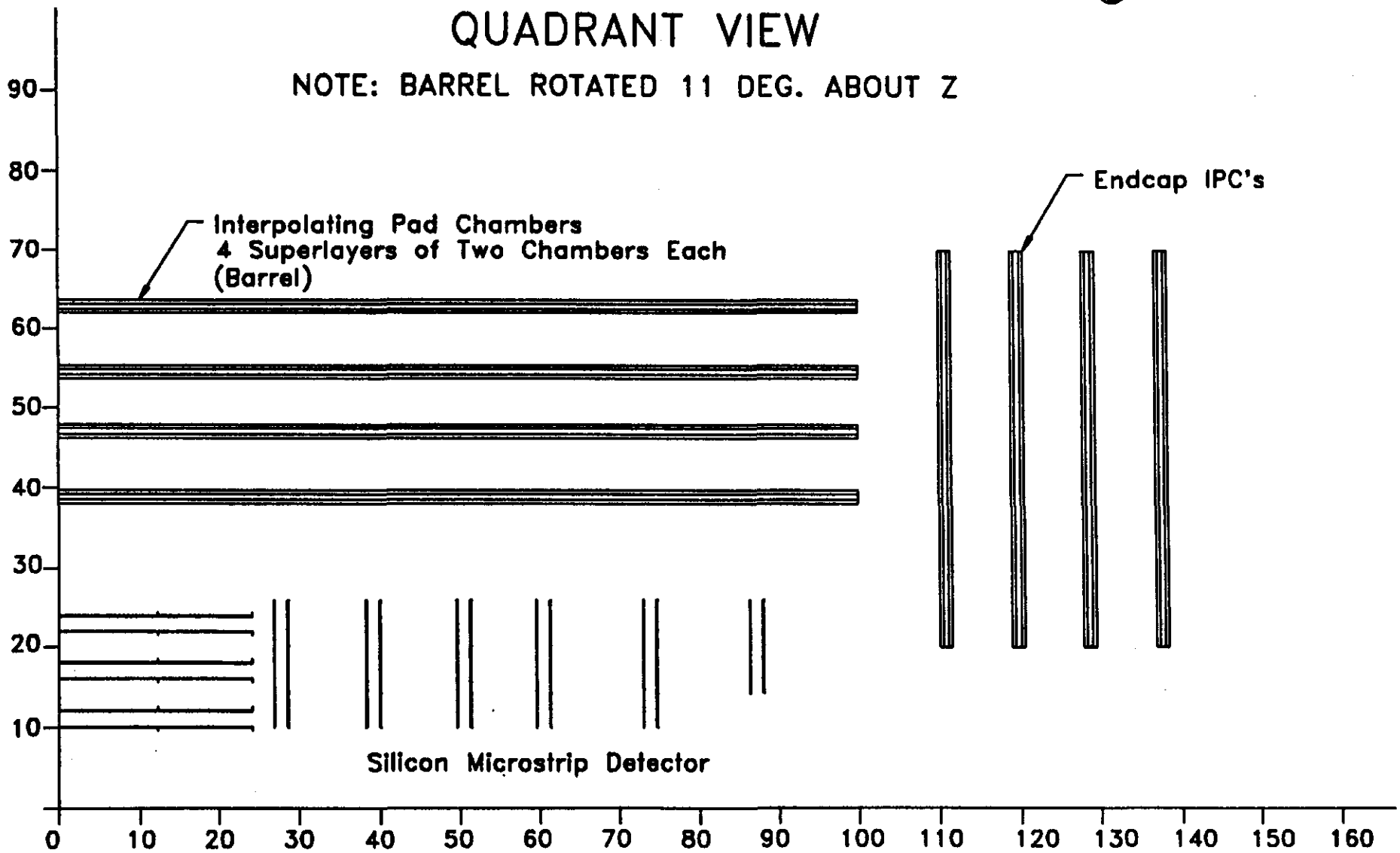
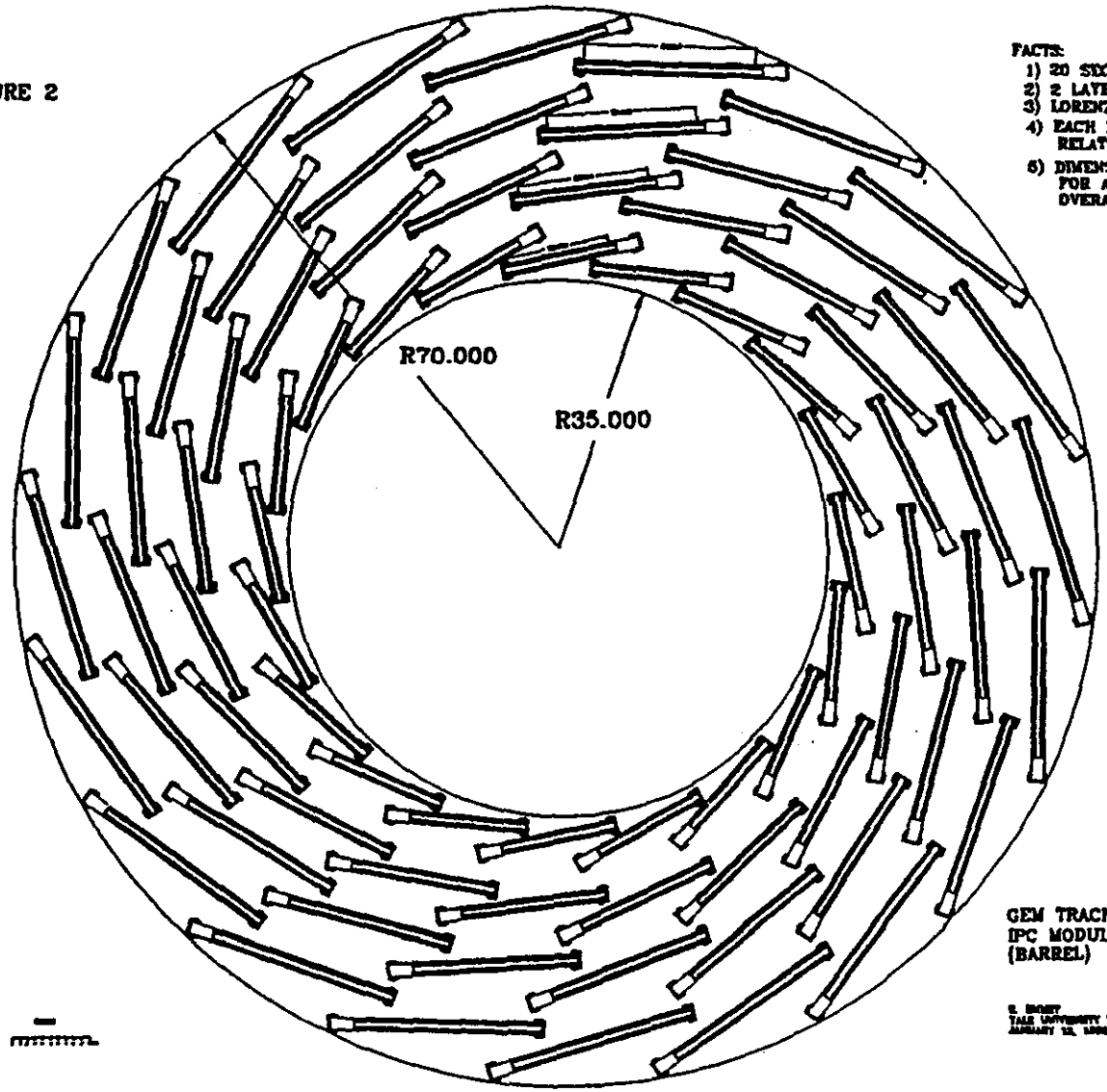


FIGURE 2



FACTS:
1) 20 SECTORS OF 4 SUPERLAYERS EACH
2) 2 LAYERS PER SUPERLAYER
3) LORENZ ANGLE~12 DEGREES
4) EACH LEVEL ROTATED 4.5 DEGREES RELATIVE TO ADJACENT LEVELS
5) DIMENSIONS FOR CHAMBERS ARE FOR ACTIVE WIDTHS (ADD 5 CM FOR OVERALL WIDTHS)

GEM TRACKER
IPC MODULE LAYOUT
(BARREL)

E. BIGNEY
YALE UNIVERSITY PARTICLE PHYSICS GROUP
JANUARY 12, 1990

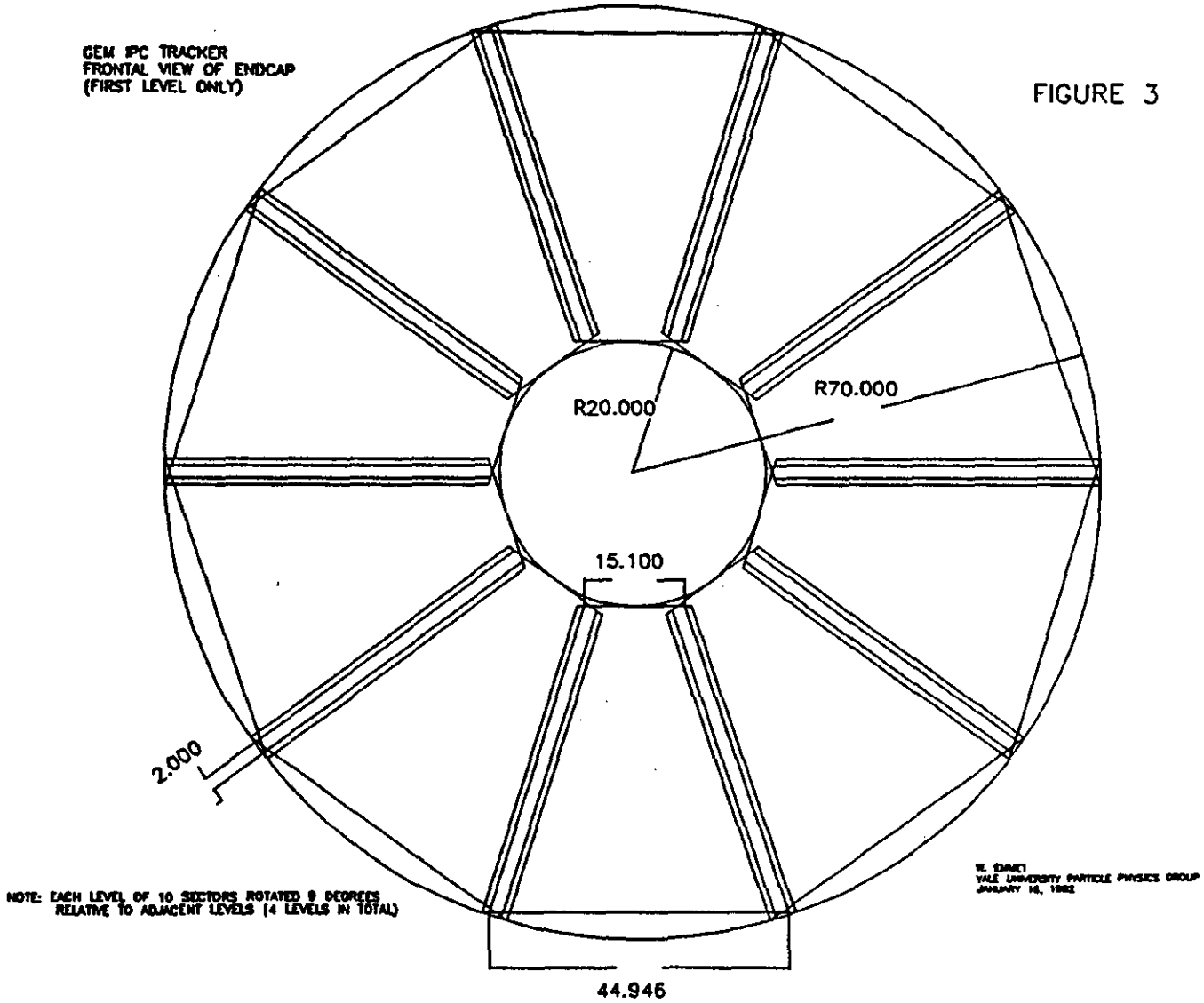

GEM IPC TRACKER
FRONTAL VIEW OF ENDCAP
(FIRST LEVEL ONLY)
R20.000
R70.000
15.100
2.000
44.946
NOTE: EACH LEVEL OF 10 SECTORS ROTATED 9 DEGREES
RELATIVE TO ADJACENT LEVELS (4 LEVELS IN TOTAL)
YALE UNIVERSITY PARTICLE PHYSICS GROUP

FIGURE 3

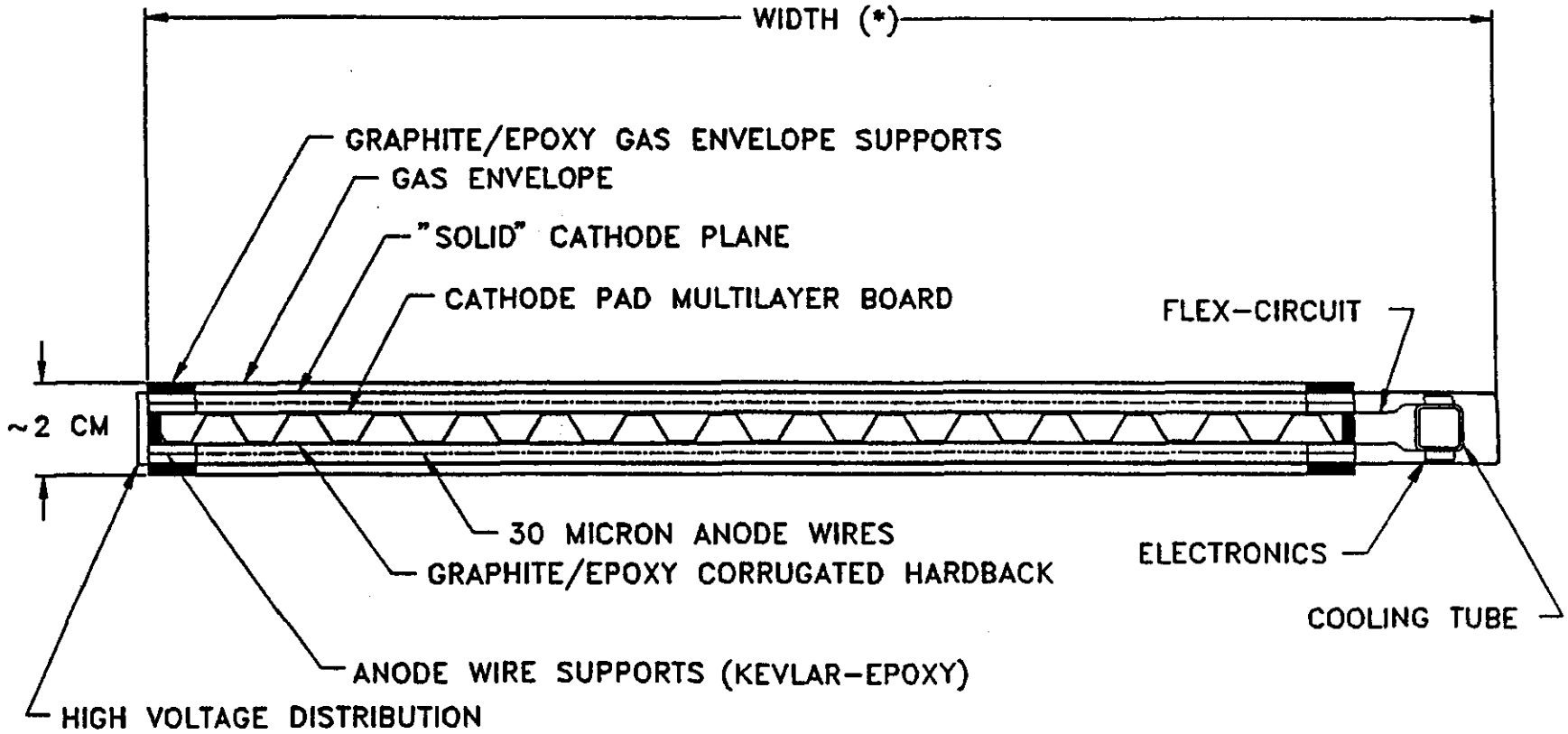


FIGURE 4:

GEM TRACKING IPC SUPERLAYER

SECTIONAL OF TYPICAL BARREL MODULE

*NOTE: LEVEL I = 18 CM
LEVEL II = 21.8 CM
LEVEL III = 24.5 CM
LEVEL IV = 27.4 CM
(SUBTRACT 5 CM FOR ACTIVE WIDTH)

W. EMMET
YALE PPG 22-JAN-1992

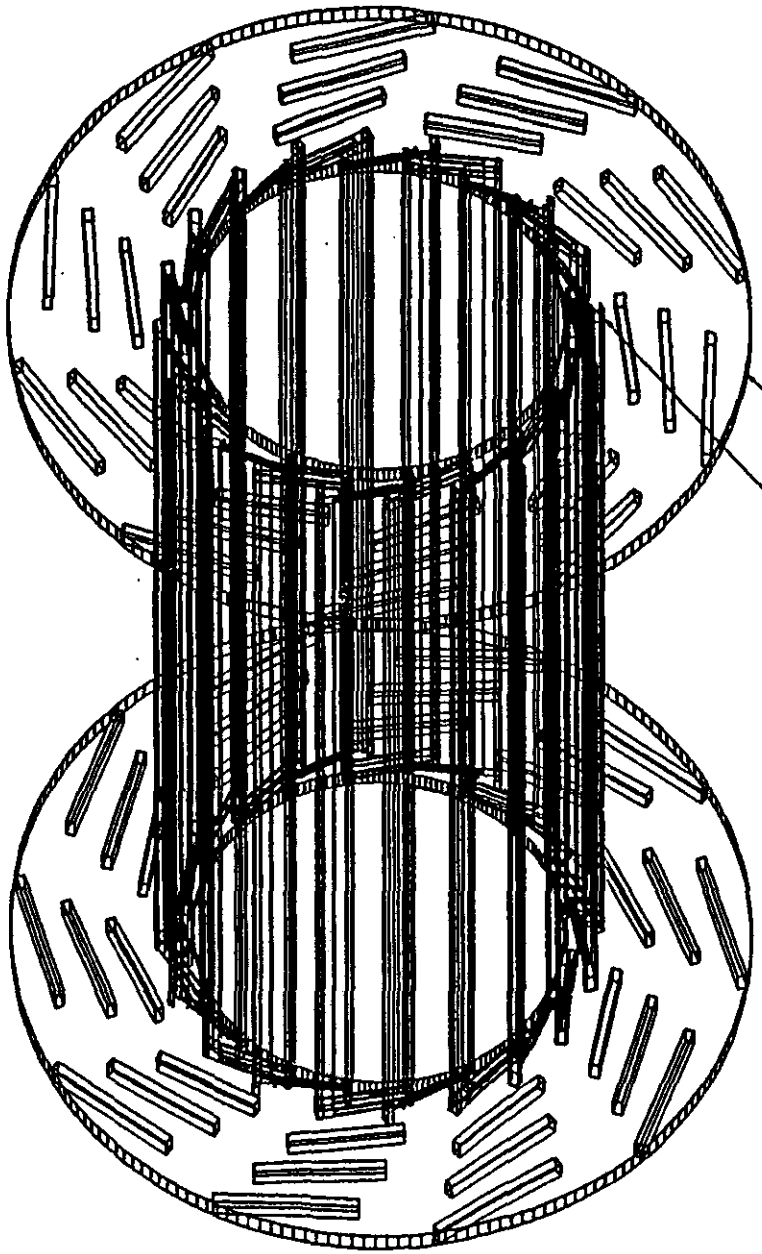


FIGURE 5

GEM TRACKER
INTERPOLATING PAD CHAMBER ARRAY (BARREL)
20 SECTORS
4 SUPERLAYERS PER SECTOR
2 LAYERS PER SUPERLAYER
LORENZ ANGLE = 12 DEGREES

NOTE: ONLY THE INNERMOST LAYER OF MODULES HAVE BEEN SHOWN FOR PURPOSE OF CLARITY.

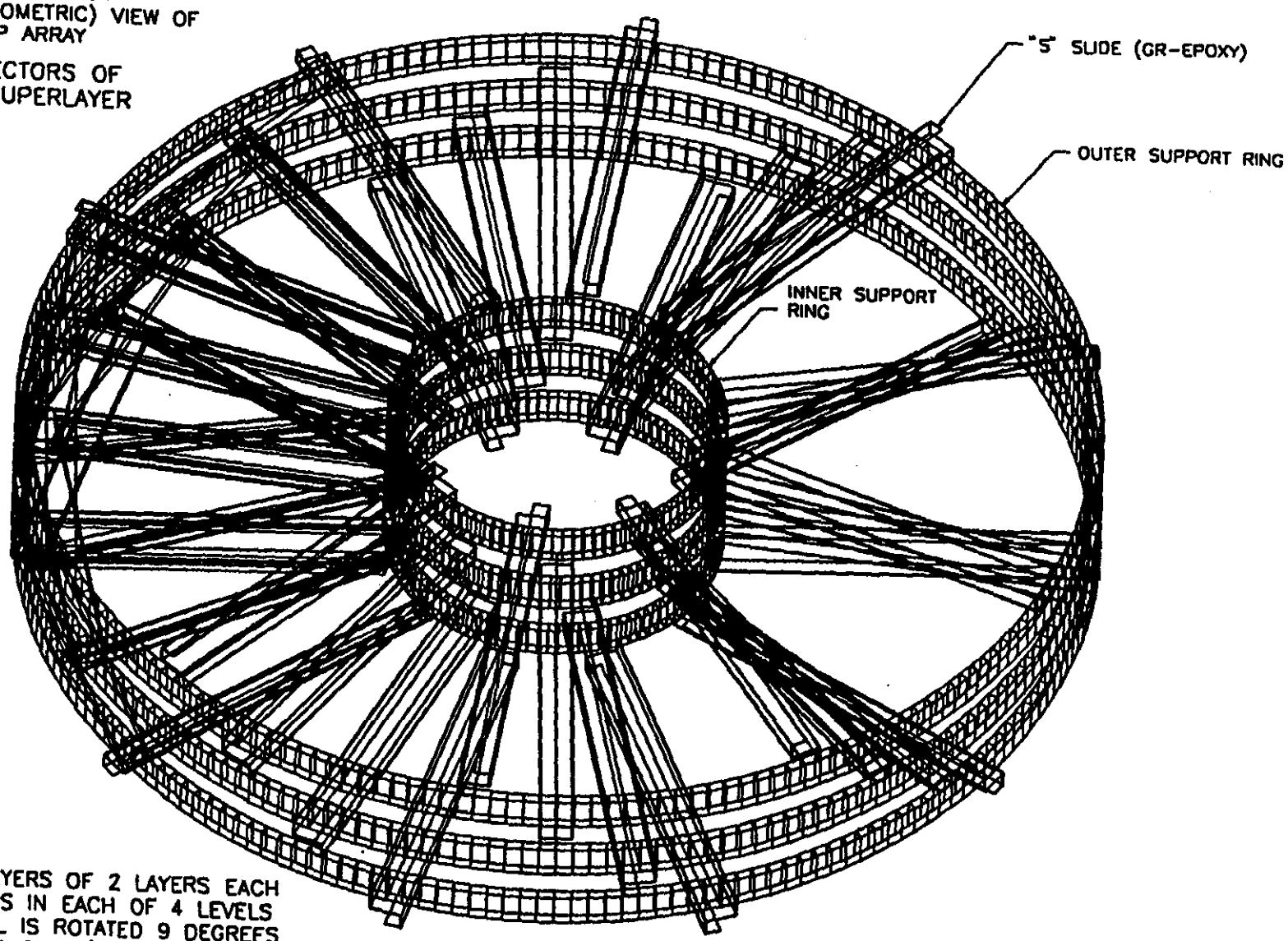
HOLLOW GRAPHITE/EPOXY END SUPPORTS DOUBLE AS STRUCTURAL AND GAS CONDUITS
ALTERNATE SECTORS ARE INSTALLED THROUGH ALTERNATE END SUPPORTS

GRAPHITE/EPOXY SLIDES FOR GUIDING MODULES INTO POSITION

W. DIMET
YALE PARTICLE PHYSICS GROUP
JANUARY 19, 1992 (REV. 2)

FIGURE 6:
GEM IPC TRACKER
3-D (ISOMETRIC) VIEW OF
END CAP ARRAY

TWO SECTORS OF
EACH SUPERLAYER
SHOWN



FACTS:

1) 4 SUPERLAYERS OF 2 LAYERS EACH
2) 10 SECTORS IN EACH OF 4 LEVELS
3) EACH LEVEL IS ROTATED 9 DEGREES
4) Z(min)=110 CM; Z(max)=140 CM
5) R(min)=20 CM; R(max)=70 CM

Figure 6

4.3.6 Radiation Length Budget

One of the design constraints imposed on the GEM IPC tracker array is the minimization of radiation length. Table 3 shows the percentage of a radiation length from r=35 cm to r=70 cm in the barrel section. Note that the electronics and anode supports were averaged over ϕ. Including air at STP, the grand total is 10.2%. The electronics contribute nearly 3.8% on avarage and have not been designed in detail at this point.

IPC Radiation Length Budget

Layer Material	Thickness (cm)	Lrad (cm)	% Lrad
1)Hardback			
Graphite/epoxy (skin)	0.0508	25.00	0.203
Graphite/epoxy (corrugated core)	0.0508	25.00	0.203
Graphite/epoxy (skin)	0.0508	25.00	0.203
2)Upper Chamber			
Chevron cathode pads (0.5 mil alum.)	0.0013	8.9	0.0146
Foam insulator (10 mil)	0.0254	150.00	0.0169
Signal plane (0.5 mil alum.)	0.0013	8.9	0.0146
Mylar insulator (2 mil)	0.0051	28.7	0.0178
Outer cathode plane (0.5 mil alum.)	0.0013	8.9	0.0146
Mylar insulator (2 mil.)	0.0051	28.7	0.0178
3)Lower Chamber			
Chevron cathode pads (0.5 mil alum.)	0.0013	8.9	0.0146
Foam insulator (10 mil)	0.0254	150.00	0.0169
Signal plane (0.5 mil alum.)	0.0013	8.9	0.0146
Mylar insulator (2 mil)	0.0051	28.7	0.0178
Outer cathode plane (0.5 mil alum.)	0.0013	8.9	0.0146
Mylar insulator (2 mil.)	0.0051	28.7	0.0178
4)Gas Envelope Windows			
Upper chamber (5 mil mylar)	0.0127	28.7	0.0443
Lower chamber (5 mil mylar)	0.0127	28.7	0.0443
Subtotal per superlayer:			0.891%
% due to hardback:			68.44
% due to pad material:			9.84
% due to insulator material:			21.72
5)Module sides (anode supports, etc):			5.13%
6)Electronics section:			7.82%
7)Average of module side effects:			
Superlayer I:			0.8%
Superlayer II:			0.65%
Superlayer III:			0.55%
Superlayer IV:			0.47%
7)Average of electronics:			
Superlayer I:			1.22%
Superlayer II:			1.0%
Superlayer III:			0.85%
Superlayer IV:			0.73%
8)Grand Total:			9.82%
-or at 12 degrees Lorenz angle:			10.04%

Table 3

GEM IPC Locations (middle of anode wire plane)

Superlayer Number	Effective Width (cm)	Distance to Interaction Point (cm) R for barrel; z for endcaps	
1)Superlayer I			
Inner chamber	13.0	37.2	
Outer chamber	13.0	38.3	
2)Superlayer II			
Inner chamber	16.8	46.2	
Outer chamber	16.8	47.3	
3)Superlayer III			
Inner chamber	19.5	54.4	
Outer chamber	19.5	55.5	
4)Superlayer IV			
Inner chamber	22.4	63.5	
Outer chamber	22.4	64.6	
5)Endcap Superlayer I			
Inner chamber			110.2
Outer chamber			111.4
6)Endcap Superlayer II			
Inner chamber			119.2
Outer chamber			120.3
7)Endcap Superlayer III			
Inner chamber			128.1
Outer chamber			129.2
8)Endcap Superlayer IV			
Inner chamber			137.0
Outer chamber			138.2

NOTE: Endcap chambers overlap; add approx. 2 cm to z for second array.

Table 4

4.3.7 Support Structure

The barrel IPC modules are supported by two hollow disks (one at z=100 cm, one at z=-100 cm). The disks are tied together by "drawer slides" at each module location. The slides permit easy module insertion and removal and provide additional support for the superlayer units. The disks function both as structural members and as utility conduits (gas distribution manifolds). Because of the ovelap of superlayers, modules in one sector are inserted through one end and those in the next sector are inserted at the opposite end. Figure 5 shows the concept.

Each support disk consists of two thin (20 mil) skins with internal supports arranged to direct the chamber gas to and from each barrel module. Molded inserts will be used for the module installation slots. Graphite epoxy is the material of choice due its superior structural and thermal stability characteristics.

At this time, the endcap support structure is somewhat sketchy. The concept involves the use of "S" cross-sectioned graphite-epoxy module guides arranged radially about two concentric support rings at the inner and outer radii. This represents one superlayer level. The entire endcap support structure would consist of four of these subtructures joined together with each unit rotated 9 degrees relative to adjacent units. See figure 6 for details.

4.3.8 SSC Interpolating Pad Chamber Cooling System Design Report

Design Specifications and Requirements

There are 2 distinct heat loads associated with the IPC detectors. The first is due to the ionization of the fast gas; the second due to electronic resistance heating in the channel power supply chips. These thermal loads differ significantly in both spatial distribution and power density. For proper IPC performance and to assure accurate knowledge of IPC location, it is imperative that the thermal energy from these sources be removed with a minimum of thermal gradients, additional materials, and structural influences such as vibrations or pressure loading. Note that, in these early stages of the design development, design specifications are changing rapidly. The information in this report is updated to reflect to some extent the most recent design changes. Further design modifications are inevitable are a true conceptualization of a workable system evolves.

The heat load due to fast gas ionization is expected to be only a few Watts throughout the system. This represents a significant change in the specification of this heat load from the time the problem was first analysed. Because this heat load is small, it is understood that a slight warming of the fast gas as it circulates will provide an adequate heat sink. If there remains unacceptable thermal gradients within the supermodule as a result of limitations on fast gas circulation rate, additional cooling will be provided by passing a cooling gas through the open channels in the structural stiffening composite.

The signal readout electronics represent a significantly larger heat source, both in total load and in load density. At this point in time, the evolution of the electronics layout is resulting in rapid changes in the specification of both the geomertry and the heat load. The initial conception consisted of small packages or chips, each serving 64 channels, with each channel generating 30 mW of heat. The total package heat load was then1.9 W, with a power density between 1.9 and 5.3 W/cm^2. The nominal heat load per supermodule was 50 W.

This preliminary discription has been replaced, after several iterations, with a layout that is approaching a final design that is significantly different in geometry and heat load. The current discription consists of 2 electronics chips per 16 channels, one a preamp/shaper at 50 mW/channel and the other an analog storage device at 10 mW/channel.

These chips together have a footprint of 1.6X5.0 cm. Because of the close channel spacing, these electronics are currently laid out on a 6 cm wide board with repeated pairs of chips the entire length of the supermodule (2 m). The total heat load per chip pair is 0.96 W, and the thermal power density is 0.12 W/cm^2. The total heat load per IPC layer due to these chip pairs is120 W. With 2 IPC layers per supermodule, the heat load per supermodule is 240 W.

In addition, every 256 channels, or 16 of the above described chip pairs, must be served by a multiplexer chip. This chip has a heat load of 300 mW. The size and placement of this chip is unknown at this time, but it is anticipated by the channel count that 8 multiplexers per IPC layer will be required, resulting in only 2.4 W per IPC layer. The total heat load per superlayer is then 244.8 W.

In the barrel region there is a total of 80 superlayers, with a resulting heat load of 19584 W. In the forward region the superlayers are are wedge shaped so as to form a disk pattern with 10 superlayers per disk. The wedged superlayers are 50 cm long. There is a total of 8 disks, or 80 superlayers, in the 2 forward regions. Assuming the same electronics configuration, ther will be the same power density but 1/4 of the total heat load per supermodule. Therefore, the total heat load on the forward regions will be 4896 W, with the electronics configured radially outward instead of axially as in the barrel region. The total IPC heat load is 24600 W.

Cooling System Design Description

Three practical options exist for cooling electronics configured as described above. The first is gas cooling, either by flowing the gas directly over the electronics or by blowing the gas through cooling tubes or passages connected as closely as possible to the electronics. The second is cooling with liquid, which, practically speaking, must be confined to cooling tubes or passages. The third is a liquid-to-vapor phase change cooling system. Again, practical considerations of this system dictate closed cooling tubes for phase change cooling.

There are many factors that will influence the choice of cooling system and its configuration or geometry. Many of these factors are only partially resolved at this time. These factors include radiation length restrictions, temperature gradient restrictions, and geometric or access restrictions. Radiation length restrictions constrain the choice, amount, and distribution of materials. Temperature gradient restrictions are dictated by the mechanical and thermal coupling between components at different temperatures, the desired or limiting operating temperatures of the various components, and the tolerances on the desired operating

temperature of the IPC's. Geometric restrictions influence coolant distribution options, manifolding requirements, and system temperature gradients.

In short, the cooling system design must integrate with the mechanical and electronics designs. The final overall design will meet the system requirements at an acceptable cost by an iterative process of design modifications and improvements in the mechanical structure, the electronics layout, and the cooling system.

The philosophy for developing the best cooling system for the overall system design began with choosing a baseline design based on a preliminary analysis of the alternatives. This baseline design has been updated and modified to accomodate design and specification changes. In addition, the effect of design changes on the cooling system design are fed back to the electronics and mechanical design teams. This closes the loop to insure that optimization of one aspect of the system is consistent other system component opimization.

The baseline cooling system design is to cool the electronics by flowing water through rectangular tubes in close proximity to the electronics heat loads. This baseline design was established in response to the earlier system concept that employed smaller electronics packages with a higher power density than is now proposed. The lower power density of the current configuration suggests a reconsideration of air cooling as a system baseline. Therefore, a preliminary analysis of an air cooled system will be presented before describing the baseline water cooling system.

Air cooling is an attractive coolant for this system because it is a low density fluid and an electronic insulater. It can conceivably be directed over the electronics with a minimum of manifolding, channeling, containment, and pressure differential. However, the heat capacity and heat transfer capabilities are severly limited. This is illustrated in Figure 1, which shows the temperature difference between the air and the electronics as well as the temperature difference between the air at the detector array inlet and outlet. This calculation is based on flow through the annular spaces in the barrel region and assumes perfect mixing of heated air with nonheated air at any circumferential location. Peak air temperatures will actually be higher than indicated.

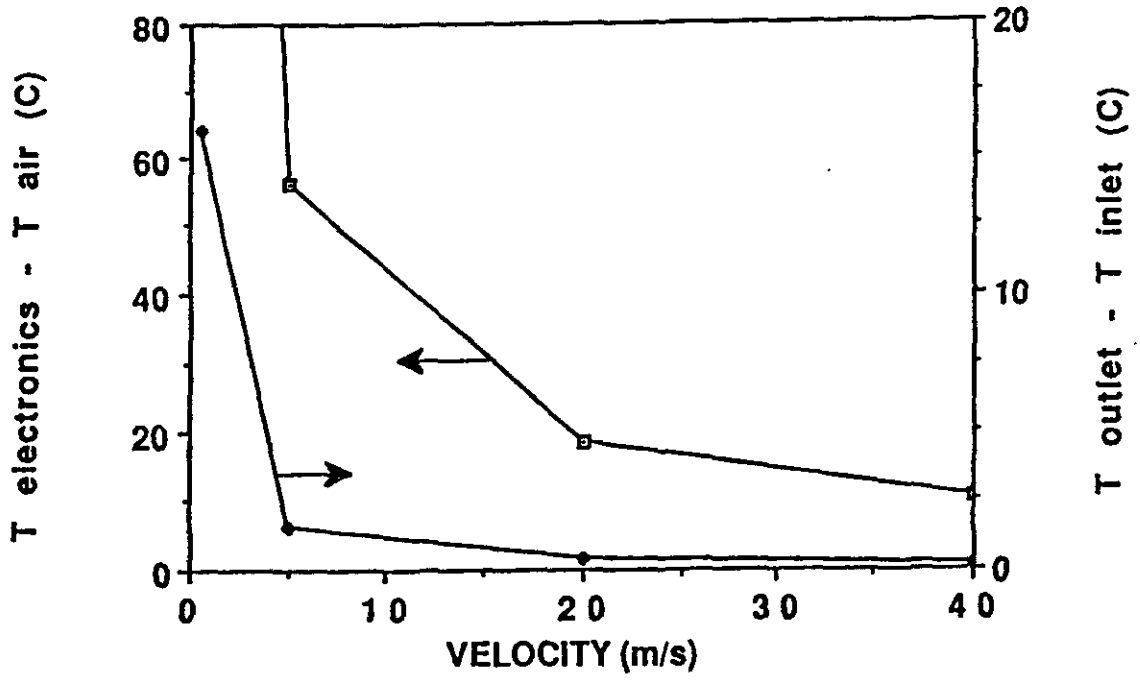


FIGURE 1. Electronics to air temperature differences at .12 W/cm2 and air outlet-to-inlet temperature differences at 240 W/supermodule as a function of air velocity with air flowing through the annular spaces in the detector array in the barrel region.

Air cooling cannot be ruled out on the basis of these calculations alone. The acceptable air velocity based on flow induced vibrations is a function of system geometry and stiffness must be assertained. Peak acceptable electronics temperature, both in terms of the operation of the electronics and in terms of the heat thermally conducted to other system components must also be understood. Also, air cooling can be enhanced by augmenting surface area, effectivly reducing power density. However, it appears that air velocities near 20 m/s will be necessary to adequately cool this system. This is a gale-force wind that must be channeled and manifolded so as to assure adequate flow over all heated surfaces without inducing unacceptable vibrations and temperature gradients.

The remaining options are water cooling and 2-phase flow or evaporative cooling. In both cases, the practical approach is to confine the fluid flow to tubes or otherwise configured closed flow passages. One alternative is to flow an evaporating liquid directly over the electronics and removing the vapor that fills the surrounding open spaces. In practice, implementing such a system introduces as much complexity as it eliminates. Distributing the liquid and containing and processing the vapor

both contribute design problems and final system complexity. Also, all candidate fluids have some environmental or safety issues associated with their use.

Containing a 2-phase fluid within a flow passage is advantageous to water cooling only by virtue of a lower radiation cross-section. The 2-phase flow can be a high quality (high vapor mass fraction) flow, significantly reducing the relative contribution of the coolant to the total system mass. However, that fraction of the system radiation cross-section attributable to the coolant can be kept small enough to be insignificant in any case. Although the 2-phase system allows for cooling without temperature rise as the coolant moves through the system, this is not a major advantage because, as will be seen, the end-to-end temperature rise with a single-phase, water cooled system is small enough that it is not considered a design problem. Proper mechanical support will be able to accomodate small temperature gradients over the 2 m length of the detector.

2-phase cooling through rectangular passages was given a preliminary analysis in reference to the system concept wherein the electronics were relatively small packages at high power density. This analysis was modified to reflect the current design power and power density (Table 1). R-11 (CCl_3F) was chosen as the coolant because of it boils at room temperature and pressure. Near-ambient pressure operation is essential to minimizing tube wall thicknesses. The coolant passage geometries considered may not be good choices for the current configuration. Nonetheless, the information in the table adequately scopes the performance of this cooling option. The conclusion is that this approach will work and has some advantages to water cooling, but that these advantages do not outweigh the safety, simplicity, and environmental soundness of a water cooled system.

TABLE 1. Perfarmance map of a R-11 2-phase cooling system at 0.12 W/cm2 in rectangular tubes.

GEOMETRY (cm)	G (kg/m2-s)	X*	ΔP (kPa)	ΔT (C)**
1 X 0.2	50	0.8	3.5	0.50
1 X 0.1	50	0.5	1.7	0.50
1 X 0.2	300	0.5	41	0.25
1 X 0.2	400	0.5	69.4	0.20

* Volume mass fraction.

** Temperature drop between the inside tube wall and the bulk fluid.

Water cooling through rectangular passages in close proximity to the electronics heat loads is the baseline cooling system design. This approach was also analyzed in reference to an electronics configuration that was more compact and of a higher power density and lower overall power level. Those scoping calculations have been modified to suit the current power and power density, as shown in Table 2. Again, the geometry of the cooling tubes may be modified to conform to the more recent electronics layout or, if possible, the electronics layout may be modified to expedite the cooling process.

GEOMETRY (cm)	V (m/s)	ΔP (kPa)	ΔT (C)*	Tout-Tin
1 X 0.2	1.0	11.4	0.21	1.7
1 X 0.1	1.0	27.5	0.18	3.1
1 X 0.05	1.0	52.8	0.45	6.2
1 X 0.1	2.0	86.0	0.11	1.6

* Temperature difference between the tube wall and the bulk fluid.

Using 1 cm wide tubes to cool the 5 cm wide electronics requires conduction from the electronics into the tubes and results in temperature gradients that may be unacceptable, depending upon materials. A detailed analysis will be performed with respect to this new electronics configuration. One possibility is to widen the tube to 5 cm. However, effect of pressure on tube deformation changes with the tube width. An approximate analysis shows that the stress in a rectangular tube is proportional to the tube width squared and inversely proportional to the tube thickness squared. That is, the required thickness of a tube designed to hold a given gage pressure increases linearly with tube width. Figure 2 shows the minimum tube wall thickness as a function of gage pressure for the 1 cm wide tubes analysed above. Thus, those tue wall thicknesses must be increased by a factor of 5 for 5 cm wide tubes, increasing significantly the importance of minimizing pressure drop so as to minimize tube wall thickness. Another consideration is the radiation cross-section increase.

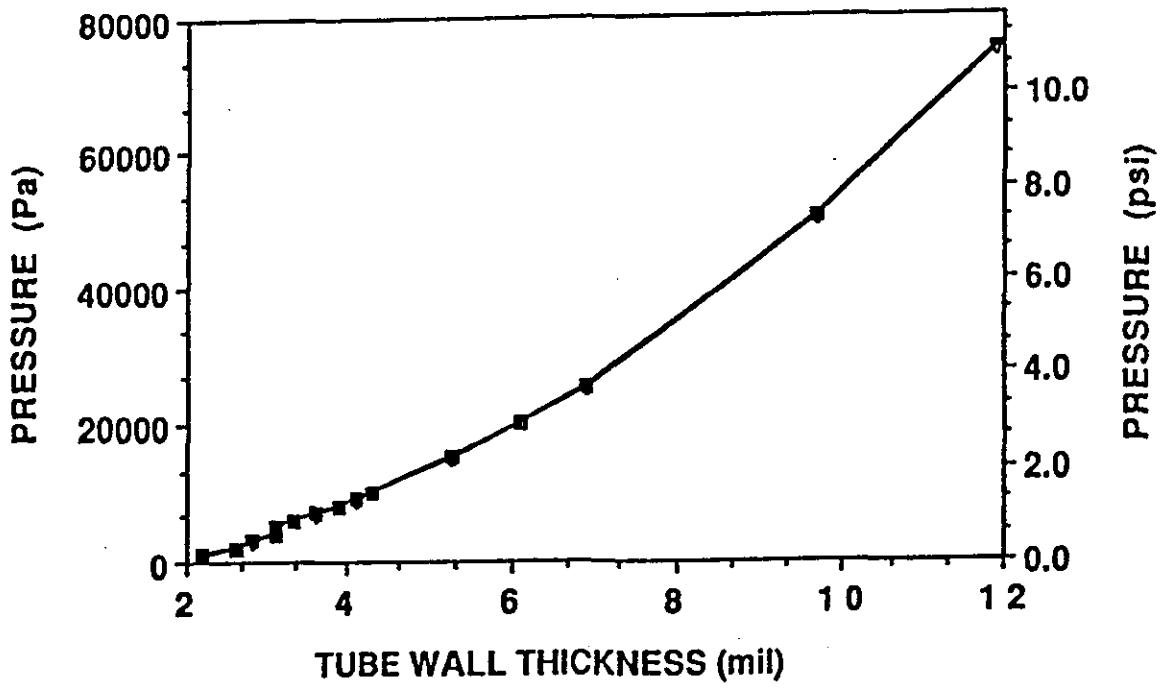


FIGURE 2. Minimum tube wall thickness as a function of gage pressure. Assumptions: Hardened aluminum alloy (5052-H38), maximum stress=1/3 yield stress.

Summary and Engineering Issues

The baseline design for cooling of the IPC electronics is forced convection cooling by water flowing in tubes to which the electronics are mounted. This is superior to cooling by a 2-phase flow through similar tubes because the performance advantages to a 2-phase flow for this system are small and do not outweigh the problems associated with the use of the available phase change coolants. Recent changes in the conceptual layout of the system electronics have significantly reduced the thermal power density. This change makes air cooling a more attractive alternative, but surface enhancements to further reduce the power density are required to keep the necessary air velocities to an acceptable level.

System optrimization will require continuous refinement of the system design in conjunction with similar refinements in the mechanical structure (electronics and cooling system support materials and configuration) and the electronics layout. The major engineering issues that will be addressed in this optimization process are listed in Table 3.

Optimization within this multiparametric field will require compromising design objectives and carefull integration.
FIGURE 3. Listing of the major engineering issues in the cooling system design for the IPC detector array.

1. Thermal load and load distribution.
2. Electronics layout.
3. Cooling system and electronics support structure.
4. Maximum allowable electronics temperature.
5. System stiffness and vibration characteristics.
6. Allowable IPC temperature gradients.
7. Radiation length considerations.
8. Environmental and safety issues.
9. Coolant supply and return manifolding considerations.

R&D Effort.

The near-term R&D effort will focus on a detailed cooling system design analysis. This analysis will center on the baseline water cooling system yet continue to examine the merits of alternative cooling systems as the overall system configuration evolves. This cooling system analysis will be shared with the mechanical and electronics design team so that design decisions can be made on the basis of an overall system optimization perspective. An itemized listing of the engineering R&D issues is as follows:

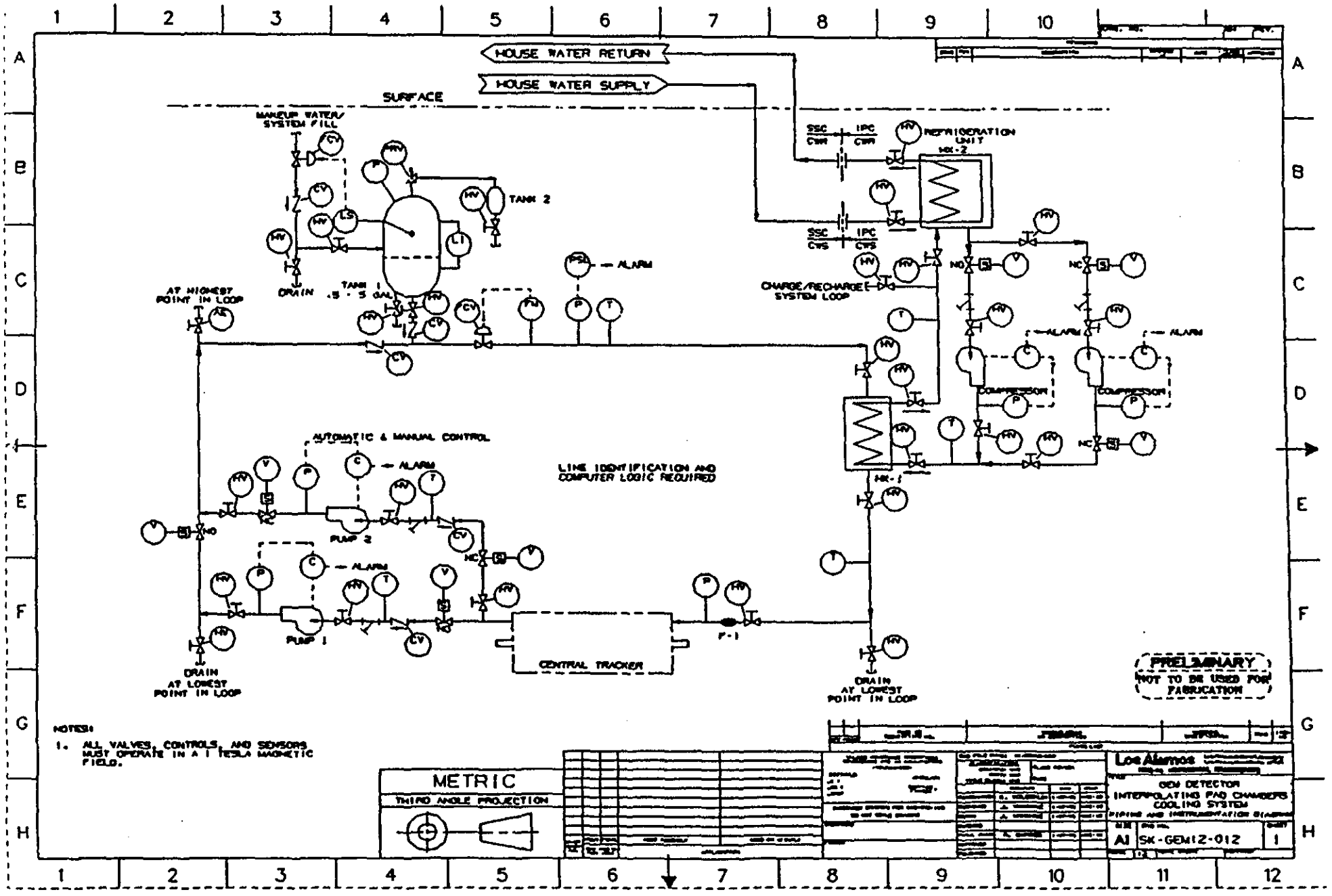
1) Work as a team member with other IPC array designers in the effort to refine and integrate the system design and its components. Involves adapting the cooling system as necessary to conform to design improvements and constraints as they arise, and expressing to the other designers the effect of design changes on the operation and implementation of the cooling system.

2) Analytically develop the cooling scheme for the fast gas ionization thermal load, and perform crucial experiments as they affect concept viability.

3) Perform a complete analysis of the forced convection water cooling loop for the electronics heat load. To the extent possible, map the field of design trade-offs with the intent of performing a first-cut optimization. This includes heat transfer and hydrodynamic analysis, material selection, cooling channel wall thickness requirements, and the effects of power

density over the expected range. Analyze and compare the use of forced 2-phase and air cooling of the electronics heat load.

4) Design and implement an experimental investigation of the baseline cooling system. With a simulated thermal load representing the electronics packages, experimentally determine heat transfer coefficients, peak temperatures,, pressure drops, system vibrations, effects of channel geometry, etc, with the intent of verifying and optimizing actual performance.


HOUSE WATER RETURN
HOUSE WATER SUPPLY
SURFACE
MAKEUP WATER/ SYSTEM FILL
TANK 2
TANK 1 .5 - 5 GAL
DRAIN
AT HIGHEST POINT IN LOOP
ALARM
REFRIGERATION UNIT
HX-2
SSC CWR
IPC CWR
SSC CWS
IPC CWS
CHARGE/RECHARGE SYSTEM LOOP
COMPRESSOR
HX-1
AUTOMATIC & MANUAL CONTROL
LINE IDENTIFICATION AND COMPUTER LOGIC REQUIRED
PUMP 2
PUMP 1
CENTRAL TRACKER
F-1
DRAIN AT LOWEST POINT IN LOOP
PRELIMINARY
NOT TO BE USED FOR FABRICATION
NOTES:
1. ALL VALVES, CONTROLS, AND SENSORS MUST OPERATE IN A 1 TESLA MAGNETIC FIELD.
METRIC
THIRD ANGLE PROJECTION
Los Alamos
GEM DETECTOR
INTERPOLATING PAD CHAMBERS
COOLING SYSTEM
PIPING AND INSTRUMENTATION DIAGRAM
A1
SK-GEM12-012
1

4.3.9 GEM IPC Tracker Assembly and Installation

The key to the IPC tracker array is that it is designed to be modular. Superlayer modules will be assembled and tested mechanically and to some extent, electrically at collaborating institutions. The support structure will also be fabricated off-site. All components and subassemblies will arrive at the SSC site and final module-level electrical tests will take place in a specially-designed facility. The barrel support structure will be installed first and individual barrel modules inserted as soon as possible. Barrel module position surveying would be accomplished at this point.

The endcap modules will be installed in their support structure prior to installation within GEM. This is because the modules are installed radially and there would not be enough clearance between the calorimeter and the IPC tracker. The negative side of this is that the endcap assembly would have to be moved and modules could become misaligned in transit.

4.3.10 Alignment

Methods of alignment of the GEM IPC tracking array and between the IPC tracker and other GEM subsystems are not clearly defined at this juncture. There are two general schools of thought: active alignment and passive alignment.

Active alignment would entail the use of on-board laser/optical apparatus which could be activated in-situ before a run to yield position data. The alignment system might be similar to that used in the silicon tracker (section).

Passive alignment would be accomplished by using tracks from PP collisions to calibrate the position of all of the chambers. This would be adequate if the tracker could maintain adequate mechanical stability between calibrations.

4.4 Readout Electronics

The readout electronics for the IPC system must satisfy four basic requirements. The first and most important is that the signal to noise ratio be maintained below 0.5% throughout the readout chain. It is likely that the position resolution of the IPCs will be determined by the noise inherent in the readout process. The second requirement is that the IPCs be read out in time to participate in a level 2 trigger decision. A third consideration which plays a key role in the design of the front end electronics is the requirement that it be rad-hard. Recent studies of the radiation environment in the GEM central cavity indicate that the charged particle radiation dose is approximately 0.44 $(10cm/r)^2$MRad/ SSC Yr. To allow several years of operation at $10^{34}cm^{-2}s^{-1}$, IPC electronics at a radius of 25 cm must survive a radiation dose of 2 Mrad, while maintaining the noise specification above. Finally, the power requirements of the electronics must be compatable with the use of a low mass cooling system. We are now investigating several options which satisfy these requirements. The IPC baseline design calls for reading out roughly 400,000 pad signals, along with 100,000 wires for Z coordinate information. The pad readout is much more critical, and we concentrate on it below.

The noise requirement has its most critical impact on the design of the preamplifier and shaper. The gain required by the front end preamplifier/shaper can be determined by the discussion of the required pad signal charge in section 4.2.3. There, we found that a a signal of $2x10^5$ electrons was required by noise considerations. This corresponds to 0.03 pC, which should be approximately one fifth full scale at the output of the amplifier to allow for Landau fluctuations in the signal. Taking a 2 V full scale, we find that a gain of roughly 10 V/pC is needed. As discussed in section 4.2.3 , the dominant noise source occurs at the input transistor of the preamplifier, and is dependent on the input capacitance, peaking time, and transconductance. The input capacitance is fixed by the chamber design, while the peaking time is set be the requirement on response time. One can, up to a point, decrease the noise occurring in the front end amplification by increasing the transconductance, which is done by increasing the bias current of the input transistor. Noise considerations favor the use of bipolar designs for the amplifier electronics, and we are in the process of investigating the availability and expense of bipolar processes which meet our rad-hardness requirements. One which looks quite good to us at the moment is the Harris UHF process. Access to processes of this type tends to.be expensive and difficult. This has has led us, at least during the preliminary design stage, to work in

CMOS. The design of a preamplifier using a CMOS process with specifications set by the requirements detailed in section 4.1 is now well underway. The design of a preamp and shaper developed at BNL as part of the IPC R&D program is shown in Figure 4.3.1. Figure 4.3.2 shows the impulse response of this design. Prototypes of this design will be fabricated in a run occurring in late February.

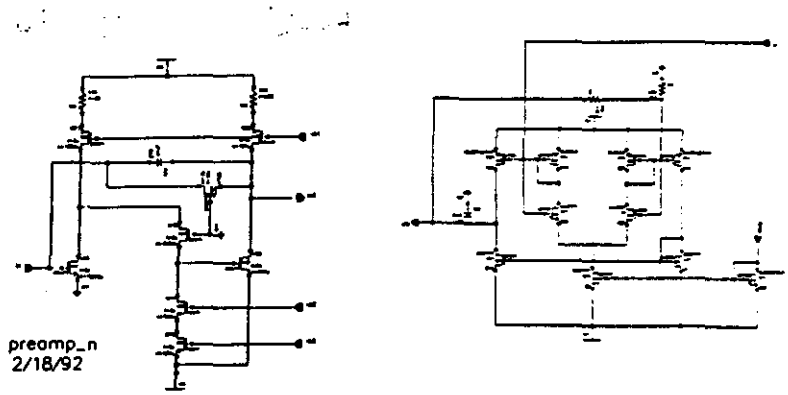


Figure 4.3.1
IPC Preamp and Shaping Amp Prototype

Several options are under consideration for the overall cathode readout architecture. All are based on the use of an analog pipeline clocked at the 62 Mhz spill rate. One configuration under study includes a sequence of analog multiplexers at the output of the pipeline, with the analog signals being ported out of the detector using optomodulators such as those now under study at BNL and elsewhere. A block diagram of this architecture is shown in Figure 4.3.3. The alternatives all include some form of digitization on the detector, with digital data links out of the detector, as illustrated in Figure 4.3.4. Two versions are under consideration, one using fast successive approximation ADCs on each channel, the other employing a fast analog multiplexer at the output of the pipeline feeding a single FADC per 16 readout channels. In these architectures the readout electronics consists of three primary functional blocks. The first is the preamp/shaper, which in the current design would consist of an 8 channel bipolar surface mount chip. The second functional unit would consist of the analog pipeline, multiplexing, and digitization functions, all in CMOS. A design goal will be to place as much of this functionality as possible on a single monolythic. A Block diagram of the multiplexed version of the analog pipeline/digitization function is shown in figure 4.3.5. A single chip or chip set would service 16 readout channels. The final functional block, referred to here as the readout supervisor, consists of a set of address FIFOs for the analog pipeline, which drive the read and write address lines of the analog pipeline, zero suppression circuitry,

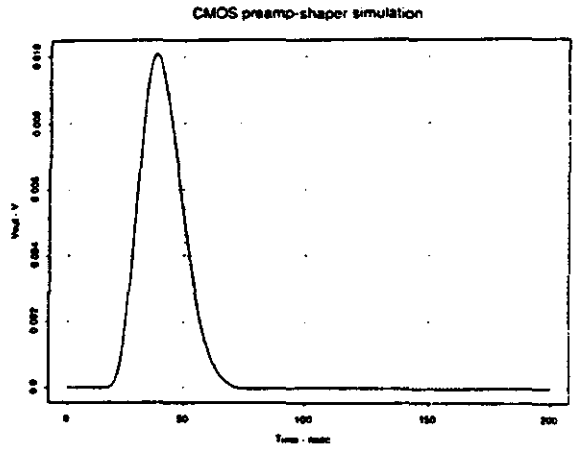


Figure 4.3.2
Impulse Response of Prototype Amplifier

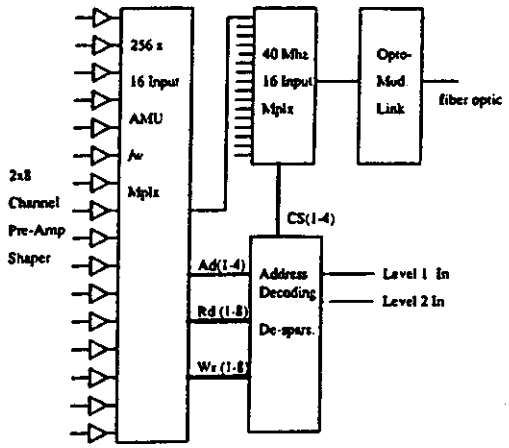


Figure 4.3.3
IPC Readout with Remote Digitization

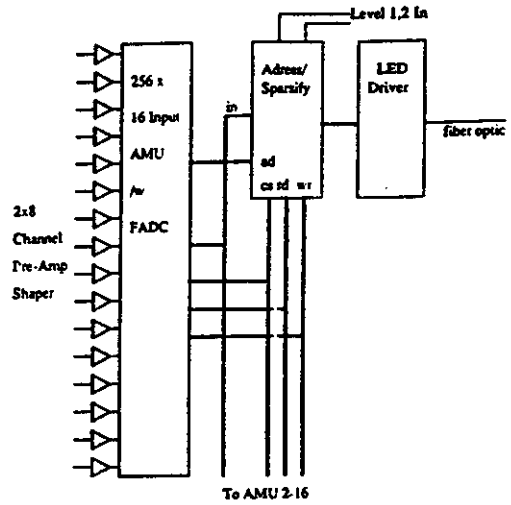


Figure 4.3.4
IPC Readout with Onboard Digitization

and an LED/fiber optic link. In the baseline this functional block occurs in units of 256 readout channels, or 16 pipeline chips.

The analog pipeline, common to all architectures under study, is based on the recent work done at LBL. Study of the LBL chip is now underway at Nevis Laboratory by members of the GEM electronics group, and is already indicating ways in which this design can be improved, for example, the use of differential pipes. The Central Tracker R&D plan calls for Oak Ridge National Laboratory to work to develop a rad-hard version of this chip having 16 input channels by 256 buckets during the next year.

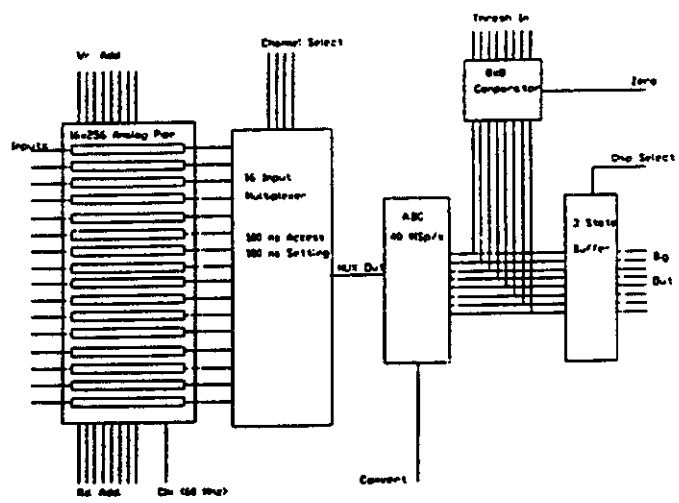


Figure 4.3.5
Pipeline Archetecture

4.4.1 Readout Timing

One of the primary requirements of the IPC readout electronics is the ability to ship the data out to 2nd level trigger processors in a time short compared with the 2nd level trigger latency period, which has been set at 100 microseconds. In this section we will examine in some detail the readout timing for several of the architectures under study, determining from this the specifications for the speed of the readout hardware. We assume here that the readout of the pipeline is performed at the 62 Mhz accelerator clock rate. It is assumed that four 16 ns time slices will be read out for each hit pad. This assumption is based on a 20 ns maximum delay before collection of the first electron at the wire and a 20 ns peaking time. We examine first the multiplexer plus FADC system. In the event of a 1st level trigger, the readout supervisor initiates a readout sequence by

asserting the chip, time slice, and channel address on the address bus connecting the supervisor with the 16 pipeline chips it services. As we will show, the access and settling time of the multiplexer is the time critical operation in the readout , and therefore, we wish to pipeline this process to the extent possible. This dictates a readout sequence in which the pipeline chip # is clocked at the highest rate, followed by the time slice address, with the channel number within the pipeline chip clocked at the slowest rate. The supervisor contains a 256x8 bit buffer holding threshold values for each channel, which it asserts on a bus during the readout cycle. A comparator on the pipeline chip compares this threshold with the output of the FADC, and provides a yes/no answer to the supervisor on one bit of a 16 bit bus. The supervisor only asserts channel addresses corresponding hit channels, resulting in a reduction of the number of clock cycles needed to read out the system. Below, we detail the readout cycle, including timing estimates for each step. The multiplexer access times are based on the Harris HI516, a fast 16 input CMOS multiplexer. A 40 Mhz FADC is assumed.

	Delta t
Assert Channel # (1-16)	0
Assert Time Slice # (1-4)	0
Wait for MUX Settle	200 ns
Convert FADC	25 ns
Compare	17 ns
Assert hit chip #	0
Load Data/Add	17 ns
Increment chip Add	0
Increment Time Slice Add	0
Increment Channel #	0

Pipeline/MUX/FADC Timing Sequence

The total time taken for this readout sequence can be expressed as

$$\Delta t = 16N_s[(1+16f)17ns + (200ns + 25ns + 17ns)] \ .$$

where f is the fraction of non-zero suppressed hits, and N_s is the number of time slices read out. For f=0 (no zero suppression) the total readout time is 34 μs. For f=0.1, a conservative estimate at a luminosity of 10^{33}, the readout time in 18 μs. The rather small benefit of zero suppression in the readout time is due to the pipelining of the multiplexer settling time. It should be pointed out, however, that one would really like a readout time in the area of 10 μs given a total level two latency of 100 μs. The non-multiplexed Wilkinson ADC architecture could provide a readout time in that range by allowing full pipelining of the time critical process, in this case the conversion of the ADCs. We assume a conversion time of 2 μs. Faster conversion rates are possible, but require a very large power dissipation per channel. The readout sequence in this scheme is:

	delta t (ns)
Assert Time Slice Add (1-4)	0
Digitize All Chips	2000
Assert Channel # (1-16)	0
Assert hit Chip # (1-16)	0
Load Data/Add	17
Increment Chip #	0
Increment Channel #	0
Increment Time Slice Address	0

Pipeline/Wilkinson ADC Timing Sequence

The time taken to execute this sequence can be expresses as

$$\Delta t = N_s(2000ns + 17ns \times 16 \times (1 + 16f))$$

For f=0, the readout time in this scheme is 26 μs, while for f=0.1 the readout time is 11μs. An important issue to be addressed here is the design of a low power, fast Wilkinson ADC. Commercially available units exist at this speed with power dissipation of roughly 40 mW. This represents a large fraction of the total power budget of the IPC front end electronics. Units with conversion times of 5 μs have, typically, a 15 mW power dissipation figure, and would provide a 20 ns readout time at f=0.1.

4.4.2 Readout Bit Rate

In the baseline design, each readout link services 256 pad channels. With no zero suppression, and assuming four time slices read out for each hit, the number of bits being transmitted per channel per event is n=256x(8 bits)x(4 samples)=8Kbits. If we assume a 20 μs readout time, the worst cast bit rate required by the link is 0.5 Gbit/s. Handling this bandwidth requires very expensive technology, and it would be highly desirable to avoid these rates by zero suppressing on the detector. The basic scheme for doing this in the digital archetectures has been described above. Zero suppression requires a very low bandwidth link running into the detector, through which the thresholds are adjusted. The thresholds are stored in a buffer located on the supervisor module, and are used during the readout sequence by comparators located on the pipeline chip. Zero suppression in the analog readout scheme would be done in a similar way, but would require a DAC on the supervisor, and analog comparators on the pipeline chip. This seems less desirable due to the necessity for routing analog thresholds to the pipeline chips. In a zero suppressed system, the bit rate required is given by $r=256x(f_{zero})x(N_s x8 \text{ bits}+8 \text{ bits}_{add})$. For $f_{zero}=0.1$ and $N_s=4$, we find that a 50 Mbit/s link is required. This is within the capabilities of a simple LED based system, as described under the Silicon Strip Optical Data Link in this document. The Central Tracker group at LANL has looked into rad-hard LED drivers, which are available from Honeywell at $120 per link. In this case, the cost of the data link is dominated by the cost of the fiber optic cable and connectors, estimated at $400 per link.

4.4.3 Wire Readout

In order to obtain Z coordinate information for the IPCs, the baseline design calls for reading out one layer of wires in each IPC superlayer. This results in approximately 100,000 channels of wire readout. The readout chain would consist of a decoupling capacitor, preamp/shaper, comparator, digital pipeline, and readout link. The preamp/shaper requirements are much less restrictive than those which apply to the pad amplifiers. First, the wire signals are a factor of three larger for the same shaping time, and the amplifier gain can be lower by a corresponding factor. Second, since only digital information is required, the noise specification can be higher. The bandwidth required to read out the wire information is a small fraction of that required for the pads, and it is expected that an LED based system such as described above would be used for the wire readout.

5 Integration into the GEM Detector

5.1 Surface Facilities

The Central Tracker will require a dedicated facility on site to complete the initial detector assembly and to disassemble and conduct maintenance operations throughout its expected ten year life time. The facility will contain two 10 x 10 m Class 10,000 Clean Rooms for parallel assembly operations of the Silicon Tracker and Interpolating Pad Chamber System. A highbay, 20 x 20 m, with a 5 ton crane covering the entire floor area will be used to combine the two subsystems and to perform systems tests and calibration. Within the highbay will be an X-ray Calibration Lab lined with personnel shielding blocks, an Electronics power supply area with appropriate safety features, and a cooling systems/gas area which will house the Butane and IPC cooling and gas systems. A storage room of about 150 m^2 is needed to house components at various stages of assembly. The entire assembly facility will require thermal and humidity control. The total space needed is approximately 750 m^2 and the facility should be available by early 1996. A more extensive description of the facility can be found in a memo of January 24, 1992 to Mike Harris regarding Central Tracker Surface Facilities Justification.

5.2 Central Tracker Installation/Access and Schedule

The Central Tracker is one of the most delicate and sophisticated systems in the entire GEM detector. Many of its components have very long fabrication times, the final assembly requires the highest precision alignment in the entire detector, and the device must be thoroughly understood before it is installed in GEM. Given these considerations the earliest date that the Tracker can be completed and fully prepared for installation into the GEM detector is mid 1998. This fact dictates the need for an assembly scenario for the GEM detector which will allow the Central Tracker to be installed after the other major components of the detector are in place. Once installed, the tracker team will require at least nine months priority access to the detector for connections and alignment and for tests of electronics, cooling systems, voltage delivery systems, and gas systems.

The Central Tracker, expected to provide the highest precision information in GEM, sits in the worst radiation environment. Silicon technology offers the only possibility of survival under these conditions; however it is still expected that some detector failures will occur over time. Access to the detector will be necessary annually for exchange of faulty components or other maintenance required to keep this device performing at its full potential.

5.3 Services Access to the Central Tracker

Signal cables, voltage distribution cables, gas and cooling supply lines will connect with both ends of the tracker in the GEM detector. These services must be routed along the interface between the Central Calorimeter and the End Cap Calorimeter. From that point they will run to the central membrane in the case of a split magnet and exit vertically along the eta=0 split. In the case of an integral magnet the services must continue along the interface between the barrel and forward muon chambers and exit the detector at the end of the magnet.

5.4 Beam Pipe

5.4.1 General Description

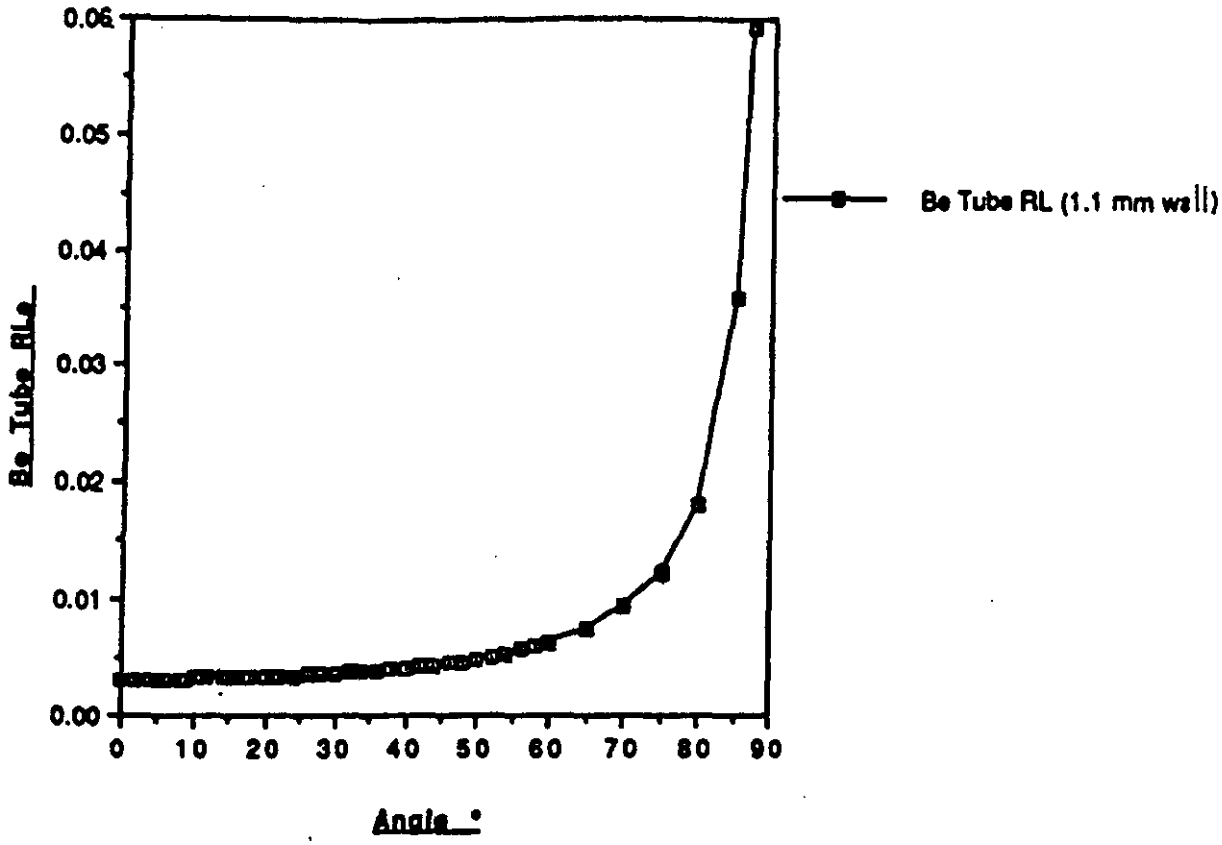
The beam pipe for the Central Tracker will be a 1 mm thick, 50 mm diameter, 3m long Beryllium tube. The tube's most critical parameter, the radiation lengths seen by a particle traversing the thickness is shown in Figure 5.4.1. Further studies are underway to determine if the radiation lengths can be reduced by use of thinner Beryllium for the pipe.

In the current design, the tube will be fabricated by Electrofusion of California using a rolled sheet of Be with a brazed longitudinal joint. Soft aluminum transition pieces will be brazed to the ends of the Beryllium section to facilitate coupling with the remainder of the beam pipe in the experiment. Bellows are required at either end to avoid stresses on the brittle Beryllium. Due to the extremely delicate nature of the pipe and its alignment requirements with respect to the machine the Central Tracker will be constructed independently of the beam tube with a separate inner gas enclosure, also of Beryllium. The inner diameter of the tracker must allow passage of the beam pipe with its bellows attached. Once installed in GEM, additional sections of pipe can be welded to the aluminum transition pieces taking appropriate precautions to protect the tracker and to ensure the quality of the welds. The design and fabrication of the beam tube must be coordinated with the accelerator. Joe Weaver and Kate Morgan have been designated the contact persons on the accelerator and detector sides respectively. Further mechanical details on the Beryllium pipe are available in the Mechanical Design section of this report.

5.4.2 Vacuum Quality

The final specification of the required vacuum quality has not been determined by the GEM collaboration, however it is clearly desirable to have a high quality vacuum, in the range of 10^{-8}, especially near the interaction point. Preliminary calculations on the vacuum quality achievable with different beam pipe and pumping configurations have been done by Gerry Chapman of CERN.(Ref. GGT-000001). These calculations assumed optimum

Figure 5.4.1 Be Beam Tube Radiation Length



conditions with a baked out Stainless Steel beam pipe. They indicated that with the proposed constriction of the beam pipe (33 mm) in the area of an integrated Forward Calorimeter, pumps near the Central Tracker would be required in order to achieve a vacuum of near 10^{-9} torr/l/s at the interaction point under these optimum conditions. Experience has shown that the reality will likely be an order of magnitude worse. This problem is under further study by the GEM Integration Team.

5.4.3 Installation and Removal

The beam tube must be inserted in the Central Tracker, aligned and fixed in position before the tracker is installed in GEM. It should remain untouched during the lengthy commissioning of the tracker and only be welded to its neighboring sections of beam pipe during the final closure of the experiment. Provisions must be made for the in situ alignment of the beam pipe by the machine surveyors. Two proposals for this alignment are under consideration. In one plan, the beam pipe will be fixed to the Central Tracker and alignment capability will be provided by moving the entire Central Tracker inside the Central Calorimeter cavity. It appears that this method may be preferred by the surveyors. In another plan, the Central Tracker would be fixed to the Central Calorimeter and the alignment is provided by moving the Beryllium tube within the tracker. Obviously, the beam pipe will have to be sawed open, breaking the vacuum, in order to remove this or any other section of beam pipe in the experiment. This is not a negligible consideration in calculating the minimum time required for access to the Central Tracker.

5.5 Total Material in the Central Tracker

The total amount of material in the Central Tracker will affect parts of the detector outside the tracker and is therefore an important issue for the entire detector. In the current design, the total thickness near 90^0 is about 15% of a radiation length. This issue is discussed in detail in the previous sections.

5.6 Magnetic Field

The GEM design includes a large solenoidal field of 0.8T in the entire detector. This field has two direct influences on the tracker. The first is that the choice of a gas for the IPC's is partly dependent on the Lorentz angle of the gas in the magnetic field. The second consideration reflects natural limits on the momentum resolution and charge discrimination imposed by the bending power of the B field. The performance of the Central Tracker would be enhanced by an increase in the B field as long as a suitable gas can still be found and the additional problems caused by loopers do not become too severe.

5.7 Safety and Environmental Impact

The Central Tracker presents a concentration of various safety concerns in its compact volume. In addition to the Butane used to cool the electronics of the Silicon Tracker, there is the high voltage of the IPC's, the heat generated in the combined electronics, and the proximity of the vacuum and the power stored in the two proton beams of the SSC. Safety evaluations and failure analyses of the various Central Tracker systems are under way. Some obvious safety hazards such as the Butane Cooling system for the Silicon Tracker are well understood and their solutions are already in design stage. For example, a double walled containment system for the Butane collection is being designed integrally with the rest of the Butane circulation system. In other areas the design is less advanced, for example the coolant for the IPC system has not yet been identified pending the evaluation of several possible coolants which pose minimal environmental hazards. As the systems of the tracker are better defined, their safety implications will be studied in detail and coherent measures adopted to mitigate any hazards.

5.8 Alignment with Respect to the Muon System

This is a question of mutual concern to the entire detector, which is however not yet well understood.

6 Radiation Environment

The lifetime of the Central Tracker depends on controlling the radiation environment in the central cavity. The radiation environment comes from three sources; charged particles from the interaction point (mostly hadrons), neutron albedo entering the central cavity from the calorimeters, and low energy debris (gammas, photons, and protons) from the outer wall of the central tracker. We have investigated the neutron albedo and the charged hadron dose but have not yet begun to look at the low energy debris.

6.1 Radiation Dose Due to Charged Particles

The major constraint that determines the inner radius of the Central Tracker is the flux of charged particles from the primary P-P interactions. One also has to take secondary interactions and γ conversions in the detector as well as soft particles trapped in the magnetic field (loopers) into account.

The flux of charged particles at a radius R from the beam line (R=rsin θ, where r is the distance from the interaction point) can be written as

$$\text{Charged Particle Flux} = \frac{KL\sigma}{2\pi R^2}\,\frac{dn}{d\eta}\ \text{particles/cm}^2$$

where L is the integrated luminosity, σ is the total pp crossection, $\frac{dn}{d\eta}$ is the number of primary charged particles per unit of rapidity per interaction and K is the factor by which the flux is increased due to secondary interactions, γ conversions, loopers, etc.

From Monte Carlo simulations of the GEM Central Tracker, K is estimated to be around 1.5. For one year of SSC running (10^7 seconds) at $\mathcal{L}=10^{33}/\text{cm}^2/\text{sec}$ and a total pp crossection of $\sigma=10^{-25}\text{cm}^2$, and the expected value of $\frac{dn}{d\eta}\sim 6.5$ charged particles per event, we calculate at R=10cm from the beam line a flux of charged particles of

$$\text{Charged Particle Flux} = 1.5 \times 10^{13}\ \text{particles/cm}^2/\text{year}$$

To convert this to a radiation dose i.e. the energy deposited per unit mass by ionization energy loss of the particles, we use the definition of the Gray

$$1 \text{ Gray} = 1 \text{ joule/kg}$$

$$= 6.24 \text{ x } 10^9 \text{ Mev/gram}$$

A more usual unit is the rad,

$$1 \text{ Gray} = 100 \text{ rads}$$

For long term doses at the SSC, the Megarad is appropriate

$$1 \text{ Mrad} = 6.24 \text{ x } 10^{13} \text{ Mev/gram}$$

We can then write the radiation dose corresponding to a flux of charged particles as

$$\text{Radiation Dose (Mrads)} = \frac{charged\ particles/cm^2}{6.24x10^{13}} \text{ x } \frac{dE}{dx}$$

where $\frac{dE}{dx}$ is the energy loss of charged particles in a given material in units of Mev/gram/cm^2.

In Silicon, the energy deposited by a minimum ionizing particle is

$$\frac{dE}{dx} = 1.66 \text{ Mev/gram/cm}^2$$

thus the radiation dose in silicon can be written as

$$\text{Radiation Dose (Mrads)} = \frac{no\ of\ min.\ ion.\ particles/cm^2}{3.8x10^{13}}$$

The charged particle flux calculated above (1.5x10^{13} particles/cm^2/year) for one year of SSC of $\mathcal{L}$=10^{33} at a radius of R=10cm from the beams then corresponds to a radiation dose of

$$\text{Radiation Dose} = 0.4 \text{ Mrads/year}$$

At a tolerable lifetime dose of 2 to 4 Mrads for silicon this corresponds to a 5 to 10 year lifetime for the inner layer of silicon detectors at a radius of 10cm and a luminosity of 10^{33}/cm^2/sec.

6.2 Neutron Flux in the Central Cavity

Several simulation codes available at Los Alamos are now being used to evaluate various particle currents and fluxes in the GEM detector. The Los Alamos High Energy Transport (LAHET) code is a monte carlo simulation package which also interfaces with the low energy neutron library based code MCNP. Electromagnetic processes are analyzed with EGS4. The residual nuclei produced by these codes may be input into CINDER90, another Los Alamos code which provides activation calculations for detector components. Please note that although only neutron flux and current are results described as of this writing, similar tallies may be obtained for any other particle, charged or neutral. Such results will be reported in the near future.

II) Input and Running Conditions

The results presented in this report are based on input from 50 ISAJET events, run in the TWOJET mode with cuts on Pt from 4 to 100 GeV/c. Exactly the same events are used for each study, and presently, only incident charged pions, protons and neutrons are used. Figure 1 illustrates the $dn/d\eta$ spectra for these particles, plots which are helpful in evaluating how the input fluctuates in various acceptances. Electrons and photons may also be tracked with the EGS4 code, but the present studies do not depend on electromagnetic processes. No magnetic field has been implemented. This is not considered crucial for the present studies since the detector is azimuthally symmetric, which is the same direction charged particles will bend. A gaussian approximation to energy straggling is used, and multiple scattering is applied to all tracked charged particles. Particles are tracked down to the following thresholds:

Particle	Threshold
prot, deut, trit, ^{3}He,α, pbar	0.1 MeV
neutrons in Lahet	20.0 MeV
neutrons in MCNP	0.0 MeV
charged pions	0.149 MeV
muons	0.113 MeV
K+,K-	0.527 MeV

III) GEM Geometry and Materials

Every effort is made to keep up with the most current geometry and materials specifications in the detector. The present results are based on drawings of the barrel and end-cap calorimeters from the 2/19/92 Engineering and Integration Meeting (drawing dated 2/23/92), and the drawing of F. Nimblett (GEM920217) for the muon tracking and field shaper . Figure 2 shows a complete overview of the LAHET geometry. Closeups of this will be displayed as appropriate later in this report.

Supports are modeled with Al5083, which is 96% Al, 4% Mg. The outer beampipe radius is 2.0 cm, containing 1.65 cm vacuum and .35 cm beryllium. Natural iron is used in the field shaper and shield connection since cross section windows in ^{56}Fe are compensated by ^{54}Fe. The excluder regions are presently filled with borated polyethylene. Material specifications in the major components for various elements are tabulated below (note the LAR contains liquid argon and G10/copper readout material, and is contained in the spaces surrounding the calorimetric elements):

	EM	Hadronic	FCAL	LAR
density (gm/cm^3)	4.369	11.861	17.022	1.532
elements (#/b/cm)				
^{1}H	.00155	.00595	.0000904	.01519
^{12}C	.00139	.00355	.000199	.01309
^{14}N		.00029	.0000181	.00074
^{16}O	.00082	.00328	.0000362	.00837
^{28}Si	.00020	.00139		.00356
^{28}Si	.00135	.00453	.00135	.01266
^{52}Cr	.00112	.00140		
^{56}Fe	.00366	.00461		
^{59}Ni	.00062	.00079	.00607	
^{64}Cu			.00257	.003395
^{184}W			.0526	
^{208}Pb	.00844			
^{238}U		.02703		

IV) Applications

The present status of various code applications are presented below. This report will be continually updated as more results are obtained, and as previously produced results are redone to reflect changes in the GEM setup and material specifications.

A) Neutron Flux through Silicon Vertex Detector

The neutron albedo through the cylindrical surface 35 cm in radius and ±100 cm in Z is being evaluated for the GEM configuration described in section II. This study has been undertaken to ascertain what thickness of borated polyethylene lining in the vertex tracking region is needed to suppress this flux. Two quantities are most useful in establishing the potential damage to silicon; the flux of neutrons greater than 100 keV, and the flux less than 100 keV. As shown in figure 3, the displacement threshold in silicon for neutrons increases by over an order of magnitude above 100 keV, and keeps on increasing. Neutrons in this energy region are therefore potentially the most damaging. However, one must also keep in mind that the cross section for displacement is non zero below 100 keV, and if the ratio of lower to higher energy neutrons is large, even these low energy particles may be of consequence.

The composition of the shielding material used in these simulations is taken from data given by Reactor Experiments, Inc., catalogue #201, 5% boron-polyethylene. By weight it consists of 61.2% C, 11.6% H, 4% ^{11}B and 1% ^{10}B. The main shielding effect comes from the $^{10}B(n,\alpha)^{7}Li$ reaction which has a kilobarn cross section for thermal neutrons. The reaction is also accompanied by a .48 MeV gamma. Initial thermalization of the neutrons is achieved through scattering on hydrogen and carbon in the polyethylene.

50 ISAJET events were run both in LAHET and MCNP, with particle thresholds as described in section III. Three cases were considered, no B-poly lining, an overall 5 cm lining, and finally, 5 cm lining the cylindrical surface with 20 cm in the forward directions. The cylindrical portion of the lining extends from a radius of 75 cm to 80 cm, while the forward thicknesses end at z=±235 cm. This area is illustrated in figure 4. The table below summarizes the flux for each case. Please note, the first three lines of the table were studied for the GEM configuration according to LLMASDON 11/8/91- BWEASOM 1/9/92. This is a slightly larger setup than the one described in section III, and tungsten instead of uranium is used. Data for the setup of section III is presented in the fourth line, for the no poly case. Overall suppression factors are expected to remain the same, although magnitudes will differ. The 5cm and 5/20cm data for the present setup will be available shortly.

SETUP	flux < 100 keV	flux > 100 keV	Total Flux
no shield	45.30×10^{12}	15.97×10^{12}	61.27×10^{12}
5 cm	5.27×10^{12}	4.03×10^{12}	9.30×10^{12}
5 + 20 cm	3.30×10^{12}	1.90×10^{12}	5.2×10^{12}
no shield, new setup	23.31×10^{12}	13.96×10^{12}	37.27×10^{12}

Table 1: Neutron flux across cylindrical silicon vertex detector surface. Data are per cm^2 per year. The first three lines represent the GEM configuration as of 1/91.

Figure 5 shows the differential flux for the three cases as a function of neutron energy. Note the small difference between the 5cm and 5/20cm cases, indicating little is to be gained from larger thicknesses of B-poly. Figure 6 is an analysis of the 5 cm case, in which the composition of the shielding was varied to study the effect of the thermalization provided by the polyethylene, and the absorption of the boron. If the shielding is composed solely of polyethylene, the higher neutron energies are shifted to thermal energies. With the shield composed solely of boron, the extent of the reduction of the thermal component may be seen.

B) Particle Currents in the Forward Calorimeter

Figure 7 shows an enlargement of one foward calorimeter, with the beam direction directed upward. The FCAL has been divided into three segments, and the number of neutrons crossing the interfaces at Z=491.0cm (beginning of sec. 1), Z= 525.32cm (sec. 1 to sec. 2), and Z=599.64cm (sec.2 to sec.3). Arrows beside the numbers indicate the direction of the Z momentum component of each neutron. Three numbers are given at each surface, the total number of neutrons/event, the number with kinetic energies less than 100 keV and the number with kinetic energies greater than 100 MeV.

B) Particle Currents at Calorimeter Borders

Neutron current data has been obtained at various surfaces of endcap and barrel calorimeter elements.

C) Particle Currents through Muon Chambers

Neutron current data has been obtained at the first muon drift chamber located at Z=5.75 meters.

D) Activation of Elements

The various types of residual nuclei produced in elements of the calorimeter have been tabulated with the LAHET code. These will serve as input into the CINDER90 code, which will follow their decay in order to get an activation profile through time. As of this writing the CINDER90 code is being updated to improve cross section files, and to implement the ability to interpret results in terms of federal radiation standards.

Figure 8 presents the LAHET Z and A distribution of the residual nuclei in the last coarse hadronic section closest to the beampipe in one endcap. Figure 9 shows the N vs Z distributions. Note the typical Z distribution of fissioning ^{238}U. The data represent number of residual nuclei per event. Calculations are also available for the electromagnetic section of one endcap, and for one forward calorimeter volume.

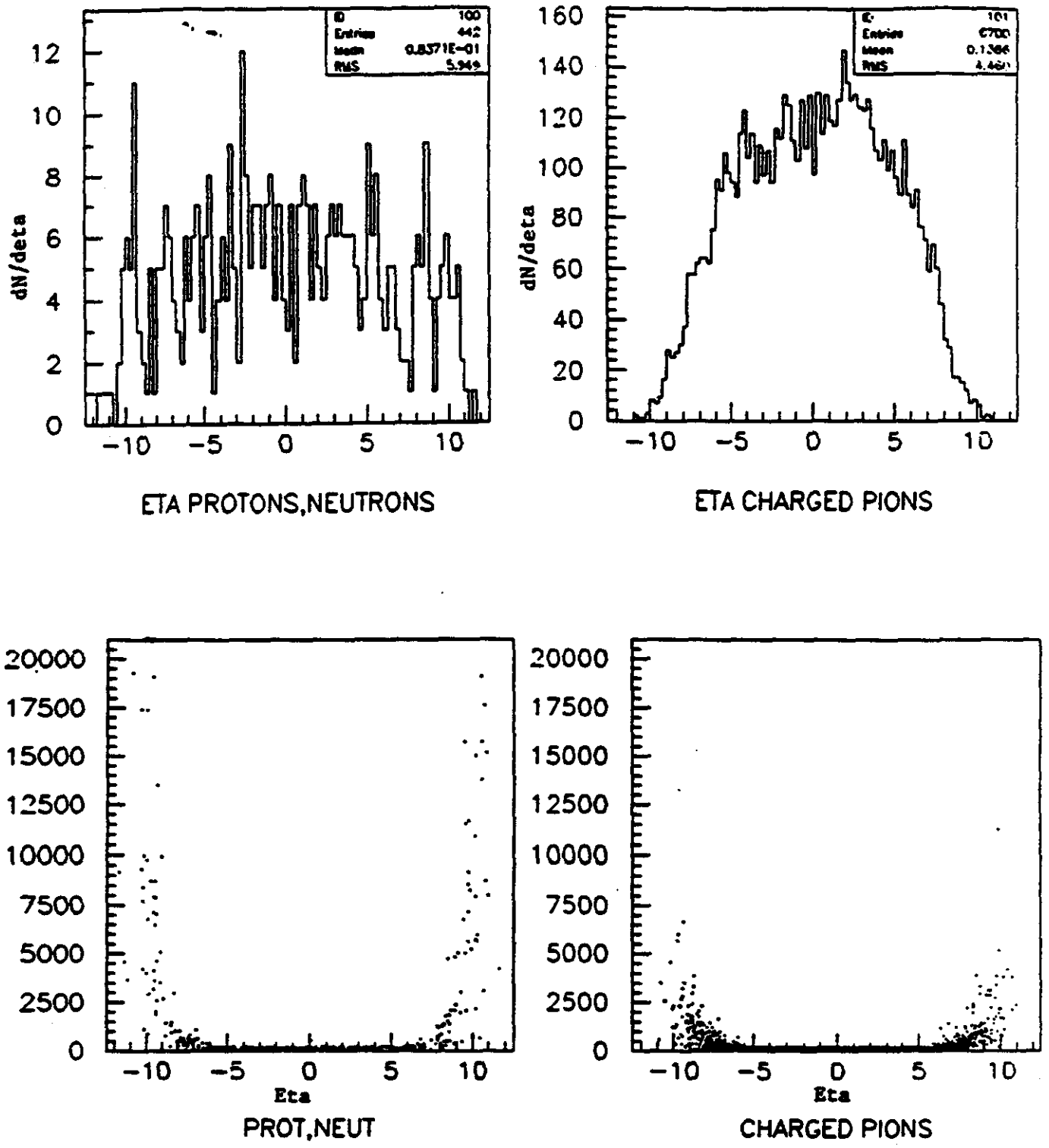


Figure 1: Pseudorapidity distributions, and energy versus η for all protons, neutrons and charged pions from the 50 ISAJET events used in these simulations.

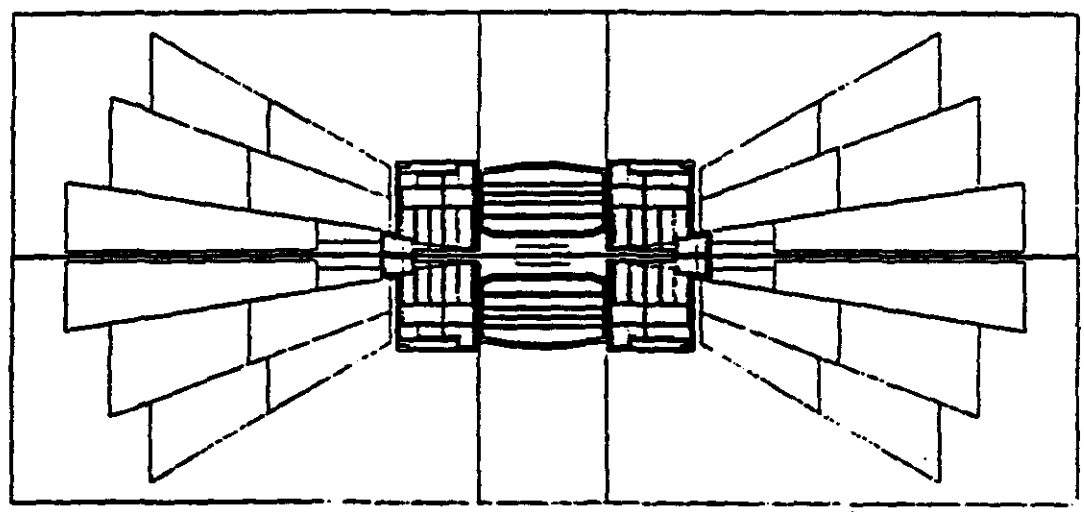


Figure 2: Geometry simulation for LAHET/MCNP

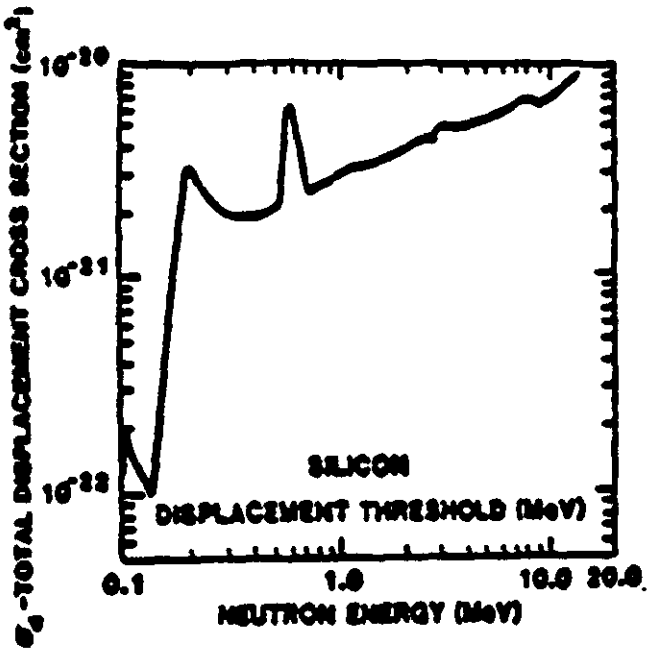


Figure 3 Neutron displacement cross section in Silicon

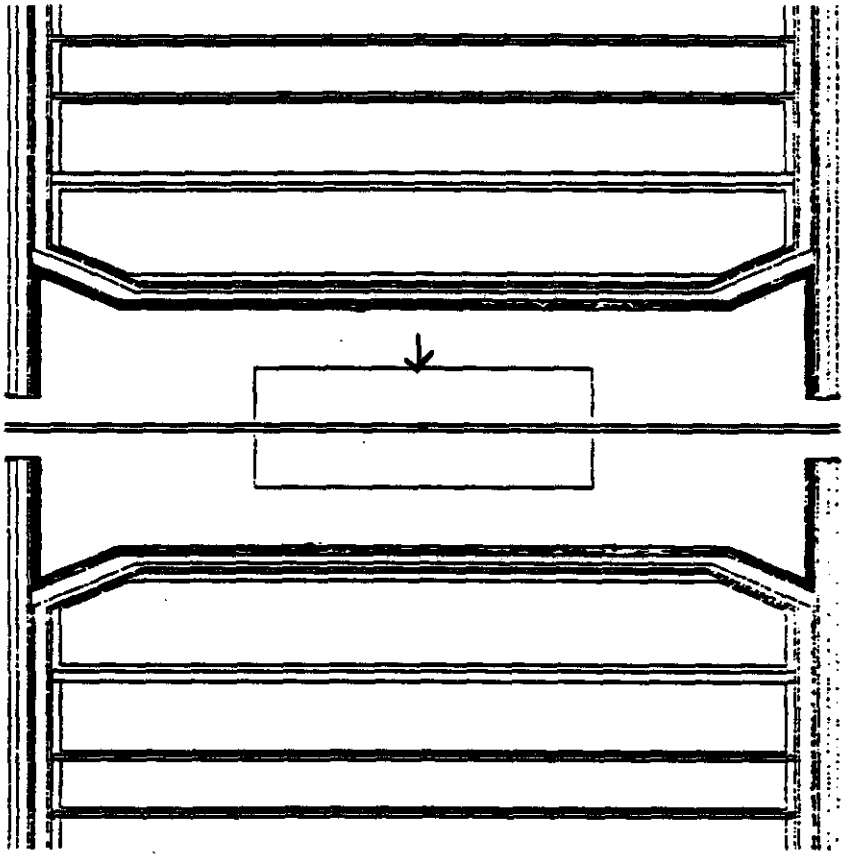


Figure 5 Expanded view of vertex region. B-poly shielding is shaded, and flux is taken across the cylindrical surface marked with an arrow.

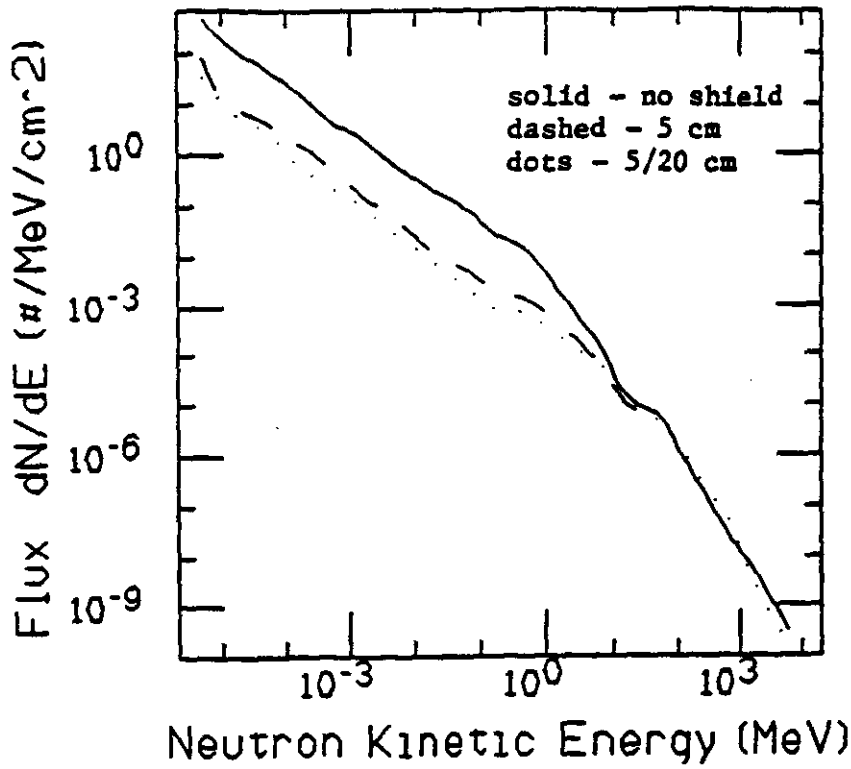


Figure 5: Differential neutron flux is compared for the no shield, 5 cm and 5/20 cm cases.

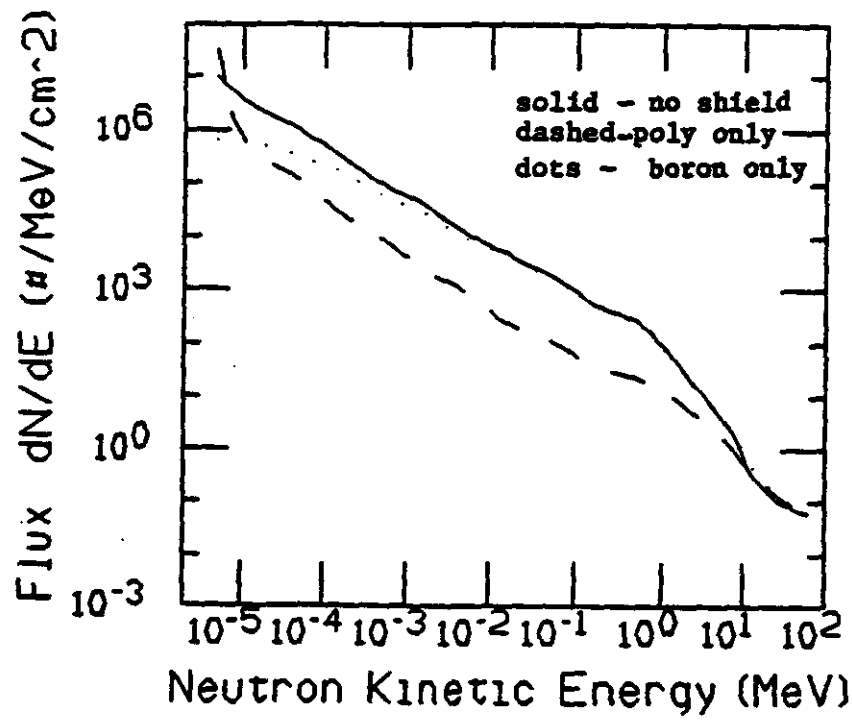


Figure 6: The thermalization effects of shielding composed of just polyethylene, and the supression of the thermal neutrons with a shield composed of just boron are compared to the no shield case.

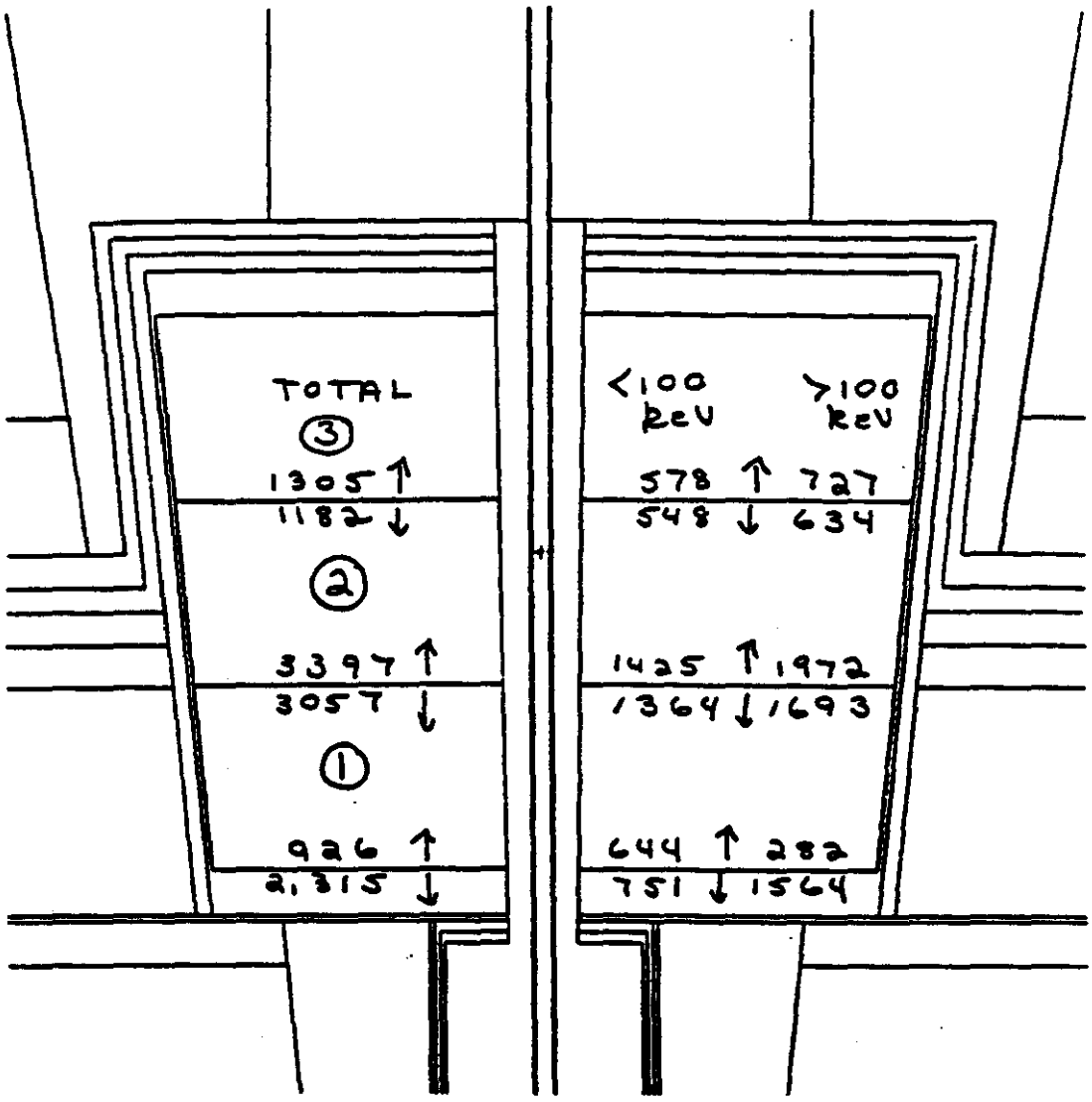


Figure 7: Numbers of Neutrons per event in the forward calorimter. Beam axis is directed upward. Totals are given at 3 surfaces. Total number is given on the left, number with kinetic energies less than 100 keV in the middle, and with kinetic energies greater than 100 keV on the right.

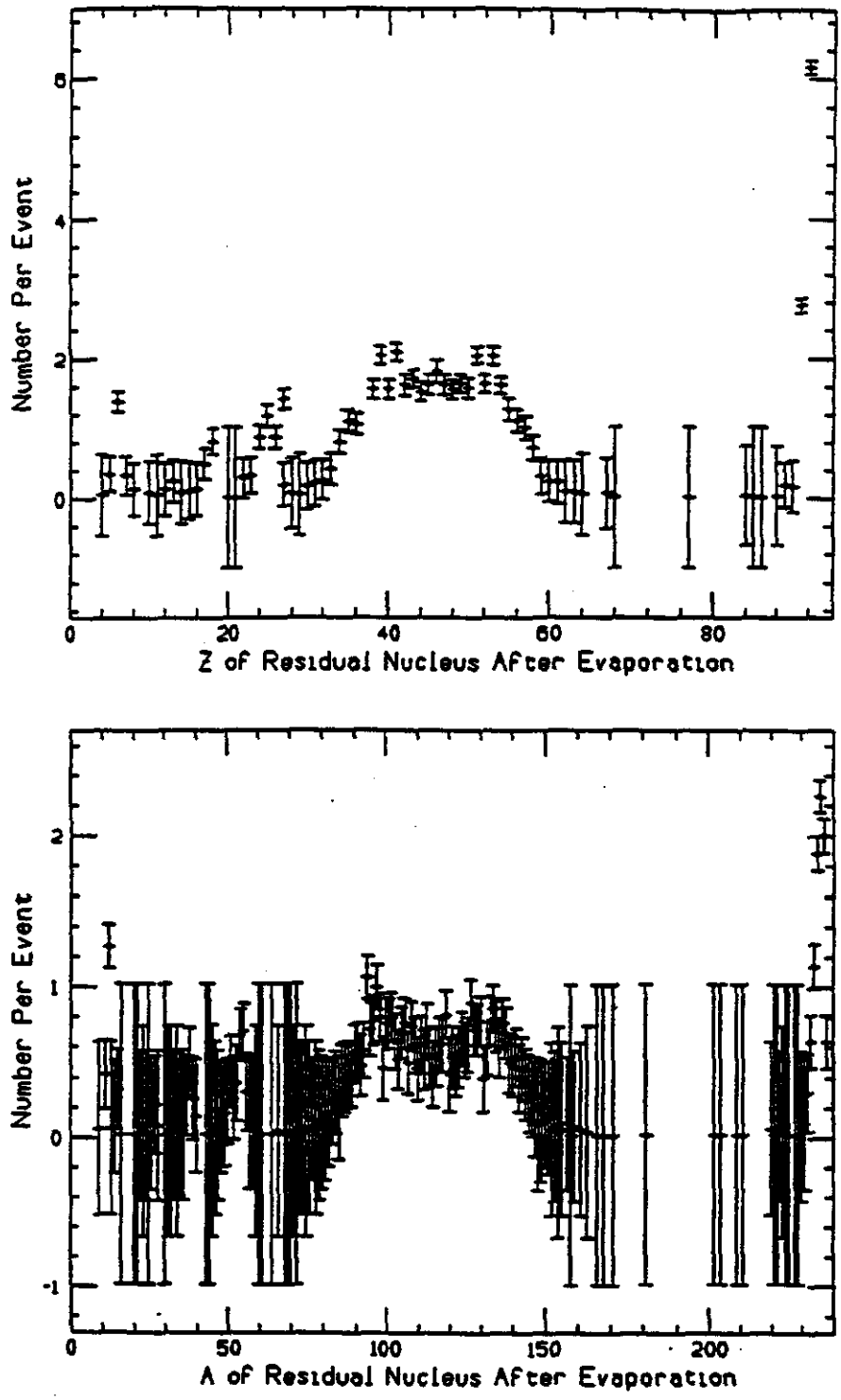


Figure 8: Distribution of residual nuclea as a function of Z and A for the last coarse hadronic section closest to the beamline in an endcap calorimter.

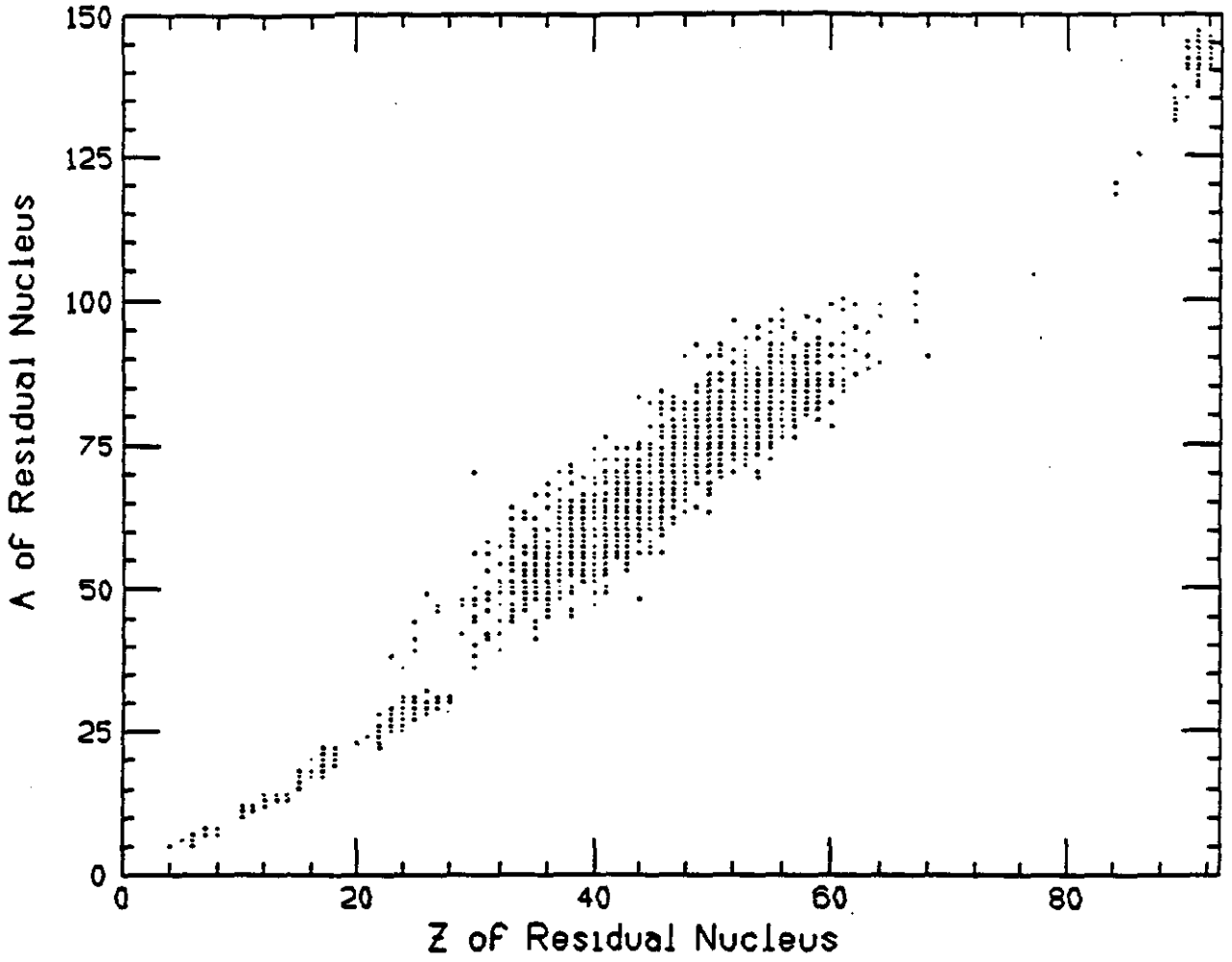


Figure 9: Mass versus Charge distribution of residual nuclei in the last coarse hadronic section closest to the beamline in the endcap calorimeter.

7 GEM Central Tracker Simulations

7.1 Introduction

Design and planning for the GEM central tracker requires knowledge of the physic s implications of specific design choices. Detailed simulations can answer import ant questions regarding the capabilities of the tracker. The central tracking simul ation group was formed in the fall of 1991 with many goals in mind.

- Provide design optimization in terms of cost versus capability
- Verify planned detector parameters under realistic circumstances
- Evaluate the performance of the central tracker using specific physics processes

7.2 Participants

To achieve our goals in a timely manner the simulations effort is receiving acti ve support from six institutions and seventeen physicists. Below is a list contain ing those who are participating in the simulation effort. Those underlined can be c onsidered to be 50% or more on central tracker simulations.

- Indiana University

  Dick Heinz, Stuart Mufson, Jim Musser

- Los Alamos National Laboratory

  Melynda Brooks, Wayne Kinnison, David Lee
  Geoff Mills, Dick Prael, Laurie Waters

- SSC Laboratory

  Peter Dingus, Jenny Thomas

- University of Michigan

Shawn McKee

- Yale University

  Charlie Baltay, Dan Dong, Sumit Sen, Elliot Wolin

- Washington University

  Dave Ficenec

7.3 Progress

Over the course of three meetings the CT (central tracker) Simulations group has started to make significant progress toward demonstrating the feasibility of the CT design presented in the LOI. Accomplishments include:

- Integration of current central tracker design into GEANT
- Central code repository at the SSC lab
- Studies of momentum resolution versus η and particle momentum
- Studies of impact parameter resolution versus η and particle momentum
- Studies of momentum and impact parameter resolution versus detector geomet ry
- Preliminary tracking efficiency tests
- Preliminary charge determination efficiency tests
- Definition of CT subroutine for use in quick physics simulations
- Initial occupancy estimates including secondaries and loopers

7.3.1 Coordination of Simulation Efforts

Since the LOI the central tracker design has been modified. These changes have been reflected in new software using GEANT. Initially most o f our effort was directed toward placing the LOI geometry into GEANT and ensuring that the code was as error free as possible. Once the initial work of inserting geometries

and materials into GEANT was finished it became easy to implement des ign changes quickly. The current code has just been updated to use the most current baseline design with 6 layers of silicon in three superlayers and 8 layers of IPCs in 4 superlayers.

Since work is proceeding at six different institutions it will be necessary to m aintain a common source code area. The SSC PDSF (Physics Detector Simulation Facility) was chosen to house the working code area. A central code repository allows everyon e the opportunity to have access to the latest code improvements done anywhere els e. Our initial organization is modeled after the CERN directory structure which mai ntains separate directories for OLD, PRODUCTION and NEW code. As the group develops, c oding standards and revision control software will be chosen in conjunction with the whole GEM simulations group. The long term goal is to have collaboration wide agreement on coding standards and software development tools.

7.3.2 GEANT Simulations

The GEANT code The GEANT code that we have used to do simulations is set up to generate an event using PYTHIA, ISAJET, or single particle generation. The particles are tracked through the detector and whenever a detector volume is entered the "HIT" is stored in a bank. Following tracking of an event through the volume, digitization, which is the detector response (determined by user code) is stored, and the digitizations are transformed into coordinates and also stored. After calculation of coordinates is completed, the set of all coordinates is used to do pattern recognition (i.e., determine how the coordinates cluster together to form tracks). After the tracks have been found, analysis code is called to calculate momentum and impact parameter resolutions, track finding efficiencies, etc. A schematic of the flow of the code that is input by the user can be seen in figure 7.3.1.

Data cards are used to input event type, geometry variables (e.g. the number of layers in each detector section, the radii at which they are located, etc.), pad chamber resolutions, interaction processes to be turned on , magnetic field magnitude, vertex smearing, and what parts of the detector are to be included in geometry setup, digitization, and pattern recognition.

Detector Geometry The central tracker of the GEM detector is made of silicon strip wafers in the inner part with interpolating pad chambers (IPC's) surrounding the silicon. There are two regions of both silicon and pads: a central region where the wafers and pads are arranged in cylinders that are concentric to the beam axis, and forward regions where the pads and wafers are arranged in discs that are perpendicular to the beam axis.

In the central (barrel) region there are six silicon layers from 10 cm radius to 22 cm and constant length in z, and eight IPC layers from 35 cm to 70 cm (also constant length in z). The forward regions are made up of twelve silicon layers extending to 87 cm and eight pad layers extending from approximately 1m to 1.4m. A picture of the tracker geometry that is in the GEANT code can be seen in figure 7.3.2.

The geometry of the silicon portion of the tracker is very detailed in the GEANT code. Each individual wafer is represented, with the strip pitch, dead regions on the wafer edges, thickness of the wafer, and stereo angle all input via data cards. The structural support of the silicon is currently included as a carbon volume that surrounds each silicon ladder, and the material from the electronics is included as an overall increase in density in the silicon.

The pads in the current work are represented by copper tubes that are 1.0% radiation length thick. This thickness is input via a data card and can be changed to more accurately represent the thickness of the chambers. Much work needs to be done to get a more accurate pad geometry and pad response to particles passing through it.

Detector Digitization In GEANT the detector response to a particle passing through it, which is called a digitization, is provided by the user. The response of the silicon strip detectors is simulated by looking at how much energy a particle deposits in each silicon wafer and how it is distributed among the strips in that wafer. If the energy deposited on a strip is above a threshold level the strip is said to be turned on. Space points are found by interpolating (digitally) between hit strips. The space point resolution is found to be approximately 10 μm in the r/phi plane (in the barrel region) and 3 mm in the z coordinate. The error in the space point due to detector alignment capabilities is included by adding an error to each coordinate in r, phi and z that corresponds to the expected alignment capabilities of the detector. The alignment errors that are currently in the code are 10 μm in the phi coordinate, 50 μm in the r coordinate in the barrel and the z coordinate in the forward region, and 100 μm in the z coordinate in the barrel and the r coordinate in the forward region.

The pad chamber response is currently very simple. All particles that pass through the chamber produce a hit and the hit is smeared by a resolution of 56 μm in the r/phi plane (50 μm detector resolution plus 25 μm alignment resolution) and 1 mm in the z plane to produce a digitization. This digitization then directly translates into coordinates. The resolutions of the pad chambers are input via data cards so that they may easily be changed from run to run.

Pattern Recognition The current pattern recognition algorithm in the code builds trees of vectors that start at a coordinate on one of the inner layers of the detector and end at an outer silicon or pad layer. The tree is then searched to find the set of vectors that have the best chi-square match in ϕ_0 (the angle phi of the track at the vertex), κ (the curvature of the track), and $\cos(\theta)$ (θ is the angle relative to the z axis). The coordinates that made up this set of vectors are then sent to a fitting routine where a helical fit is done.

With the current baseline which has a barrel silicon that is in the shape of a right circular cylinder, many tracks pass through several detector regions, e.g. a track may pass through the barrel silicon into the forward silicon then into the barrel pads and out to the forward pads. Therefore, it is necessary to search many more regions in the tracker for track points than if the ends of the barrel region layers were at constant theta. To do this, tracks are found in the silicon and the pads separately and then the track parameters in the two regions are compared to see if there are tracks from each region that should be joined. In each region, if a track is more or less pointing from the barrel region into the forward region, then the forward region as well as the barrel region will be searched for additional track points.

The track finding efficiency of the detector depends upon such things as the geometric efficiency, the detector efficiencies, the number of tracks passing through the detector, the dead time of the detectors, the number of layers and spacing in the detector and the pattern recognition algorithm itself. Work is currently being done to improve the pattern recognition algorithm so that the last variable can be reduced as much as possible.

7.3.3 Detector Response Studies (Old Baseline)

Impact Parameter and Momentum Resolution (Barrel Region) The impact parameter and momentum resolution of the central tracker were calculated for various detector geometries in the barrel region so that the geometry requirements of the tracker could be better understood. The impact parameter was defined as being the distance of closest approach of the fitted track to the z axis, in the coordinate frame where the vertex is at (0,0,0). The momentum of the particle was calculated from the helical track that was fit using just the detector coordinates, and again with a track that used the detector coordinates as well as the vertex point (smeared with the impact parameter resolution divided by two).

To determine the resolution vs. geometry, single muons were tracked through the detector at various energies. Therefore, the resolutions determined do not include pattern recognition capabilities.

In the barrel region, the resolutions were calculated for the baseline detector (six layers of silicon and nine pad layers (old baseline now)). The resolutions at 20 GeV were found to be 27 μm impact parameter and 6% momentum resolution for single tracks. The same resolutions were found when pad layers and silicon layers were removed, as long as there was an inner silicon layer and an outer pad layer left and a silicon layer approximately half-way between the two (see Table I). This implies that only three space points are needed for adequate impact parameter and momentum resolutions, so the number and spacing of layers between the three will be determined by how well pattern recognition can be done in various configurations.

The impact parameter and momentum resolutions (for single track events) vs. energy can be seen in figures 7.3.3 and 7.3.4.

Impact Parameter and Momentum Resolution (Forward Region) The impact parameter and momentum resolutions were also calculated in the forward region for the baseline detector. It was found that the momentum resolution is comparable to the barrel portion, but the impact parameter is significantly degraded (see figures 7.3.5 and 7.3.6 where the impact parameter and momentum resolutions are shown for 20 GeV muons). The degradation in the impact parameter comes partly from the fact that the closest space point formed from a track is at best 28 cm from the origin and many times is 40 cm or more since the first silicon detector that is hit is many times the second, third, or even fourth forward detector. Therefore, the projection distance from the track to the vertex is much longer than in the barrel region, causing more error. Also, although the phi resolution in the forward region is the same as in the barrel, the r resolution is no longer good and this reduces the ability to track in the r/phi plane (bend plane).

The impact parameter and momentum resolutions over the entire eta range of the detector can be seen in figures 7.3.7 and 7.3.8 where the impact parameter is shown for constant total momentum and constant perpendicular momentum (20 GeV/c) and the momentum resolution is shown for constant total momentum (20 GeV/.

Track Finding Efficiencies (Barrel Region) For our initial studies of pattern recognition capabilities, the track finding efficiency has been defined as (in just the barrel, silicon portion)

$$\text{efficiency} = \frac{\text{\# of found tracks with n correct points}}{\text{\# of tracks that passed through 5 or more silicon layers}}$$

where n is typically 4 or 5. For the efficiency in silicon plus pad barrel, n in the numerator would be between 8 and 12 and the denominator would require 5 silicon layers and 7 pad layers to have been passed through.

When track finding efficiencies were found to be low, (70% for Higgs + 1.6 minimum bias events) the pattern recognition algorithm was looked at to see if it could be improved. The chi-square cuts which determine if there is a good match in ϕ_0, κ, and $\cos(\theta)$ were adjusted first. It was then noticed that the algorithm did not allow layers to be skipped when doing a tree search, so if a coordinate was not formed, because of a dead region, for example, then only part or none of the track would be found. This was corrected so that if there is no point found on an adjacent layer when building the tree, the next layer will be searched. Up to two layers can now be skipped while building the tree. However, layer skipping when joining silicon to pads is not currently implemented. The algorithm also has difficulty finding tracks from secondary particles since ϕ_0, κ, and $\cos(\theta)$ for a vector are estimated by assuming a vertex at (0,0,0). This needs to be fixed to get true track finding efficiencies.

Currently, the track finding efficiency in the barrel/silicon region (for the tracker that has silicon barrel layers that extend to constant theta) is found to be approximately 85% to 95% over the momentum interval 5 GeV/c to 400 GeV/c for Higgs events overlayed with 1.6 (Poisson distribution) minimum bias events when secondaries are included (see figure 7.3.9). Work is currently being done to do pattern recognition with multiple tracks in the current baseline configuration which has the silicon barrel layers in the shape of a right circular cylinder.

The efficiency for finding tracks in the silicon and pads is still somewhat poor and this needs to be looked at.–It could be a problem with secondaries, and it could be that a joining of clusters must be done between the two detector types to overcome the layer skipping problem at the boundary of the two.

Future Work There are two primary areas where work is currently being focused: understanding the problems with the pattern recognition algorithm so that it can be improved and understanding the performance of the forward region of the tracker. This work has been delayed somewhat since it has been necessary to change the pattern recognition rather significantly to accomodate the new baseline tracker. When the pattern recognition algorithm becomes more stable and acceptable, we hope to put in dead times, dead strips, etc. to get more realistic efficiencies, look at some physics events and answer questions such as What is the tracker's ability to separate electrons from gammas in the calorimeter?

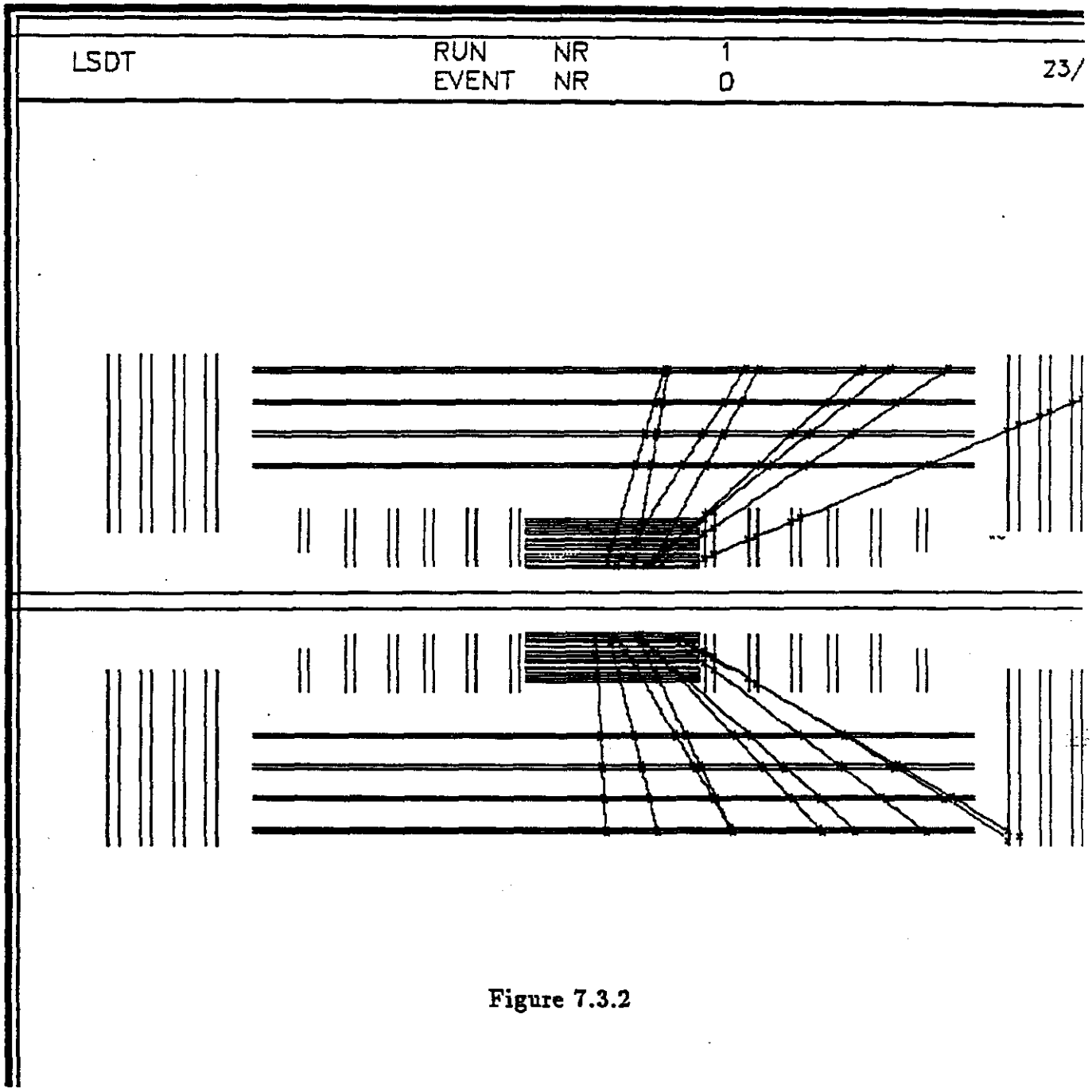


Figure 7.3.2

7.3.4 Parameterization of Central Tracker Response

While GEANT simulations realistically model high energy physics processes and detector responses, they are not very fast in execution. Since the number of important questions which need to be resolved is very large a "fast" Monte-Carlo is required. The computing/simulations/physics group has asked each detector subsystem (tracking, calorimetry, muons, etc.) to provide a subroutine which parameterizes each subsystem response. The central tracking simulations group has proposed a subroutine and work is in progress to implement the planned routine. Information concerning the CT response will be compiled from full GEANT runs. This information can then be put into lookup tables or fit by functions and incorporated into the CT subroutine. Anyone wishing to use the subroutine will merely input a particle vertex and four-momentum and the parameterized tracker information will be returned.

7.3.5 Occupancy Studies

Of great importance to the central tracker is the occupancy of tracking channels we can expect. At some level of occupancy the ability to track particles efficiently stops. Simulations can help answer questions concerning what occupa ncy a given detector geometry can expect as well as how efficiently the detector can track particles at a given occupancy. Occupancy calculations have been made using a factor for secondaries and loopers of 1.5 (50% additional tracks due to secondaries and loopers). This factor was determined using GEANT and counting additional hits not due to primary particles.

Occupancy

Silicon	$\Delta\eta\Delta\Phi$ cell	Occupancy (%)	Fraction of Time Dead (%)
$L = 10^{33} cm^{-2}s^{-1}$	$0.9–8.0\times10^{-4}$	0.6–0.22	.6–2.2
$L = 10^{34} cm^{-2}s^{-1}$	$0.9–8.0\times10^{-4}$	0.26–2.2	2.6–22
IPC			
$L = 10^{33} cm^{-2}s^{-1}$	0.0007	$\lesssim$1%	0
$L = 10^{34} cm^{-2}s^{-1}$	0.0007	$\lesssim$10%	0

7.4 Further Work

Further simulation work can be divided into two broad categories: Detector Response and Physics. We intend to pursue both types of simulation in parallel wherever possible. Detector response simulations gauge the capabilities of the central tracker:

- Momentum resolution as a function of η or momentum
- Vertex resolution in Z / $R - \Phi$ plane as a function of η or momen tum
- Energy for charge separation at the 95% confidence level for $e^{\pm}$ or $\mu^{\pm}$
- Occupancy levels at various luminosities and detector geometries
- Number of radiation/interaction lengths as a function of η
- Average amount of material as a function of η

This information can be found independent of specific physics processes. Though we already have some of this information, we will continue to improve the realism our our detector model and thereby improve the reliability of these results.

More realistic predictions of the central tracker capabilities require a physics context under which the simulation will operate. Physics simulations model interesting physics processes complete with average background contamination. This allows us to examine how effectively the central tracker can be used to aid in extracting the interesting physics from the background. Interesting questions involving the central tracker involve a coupling between the physics processes and the capabilities of the detector.

- What are the track recognition efficiencies in and out of jets?
- How well can the CT isolate tracks in the SSC environment?
- What are the charged track backgrounds for locating gammas?
- How well can the CT measure charge, momentum and impact parameter with "real" backgrounds?

- What information is available for the trigger?

These are necessary for predicting how well the central tracker can perform in the real environment of the SSC. Answering these questions, especially the pattern recognition capabilities, are one of the CT simulations groups highest priorities.

7.5 Physics and the Central Tracker

The information from the central tracker is ultimately used to extract physics results from the data. Through our program of simulations we can determine how the information from the central tracker can be optimally used to find interesting physics. From a detector viewpoint the central tracker provides a momentum and position measurement for each charged track. When exami ned from a physics viewpoint the central tracker, along with all the other detectors , define and measure a physics event. The question we need to answer is how important the measurements from the central tracker are relative to the interest ing physics events GEM wishes to examine. Our task can be viewed as a matrix with interesting physics processes cross referenced with central tracker capabilities .

	CT Capability								
Physics Processes	1	2	3	4	5	6	7	8	9
$H^0 \rightarrow \gamma\gamma$	√	√	√						
$H^0 \rightarrow e^+e^-l^+l^-, e^+e^-\nu^+\nu^-, e^+e^-jj$	√	√	√	√		√			
$H^0 \rightarrow \mu^+\mu^-l^+l^-, \mu^+\mu^-\nu^+\nu^-, \mu^+\mu^-jj$	√		√		√				
Gluino Pair Prod $\tilde{g}\tilde{g} \rightarrow e^\pm e^\pm \mu^\pm e^\pm$	√	√	√	√	√	√			
Technieta $\eta_T \rightarrow b + \bar{b}$ *or* $t + \bar{t}$	√		√				√		
W Scattering $W^\pm W^\pm \rightarrow e^\pm e^\pm \mu^\pm e^\pm$	√	√	√	√	√	√			
$Z' \rightarrow e^+e^-$ *asymmetry*	√	√	√	√		√			
B Physics, e.g. $B \rightarrow \Psi\kappa$ etc	√						√	√	√
Top Physics $t \rightarrow W + b$ etc	√		√				√	√	√

1) ID Primary Vertex
2) e/γ Separation
3) e, μ, γ Isolation cuts
4) e/h Separation
5) Muon momentum check
6) $e^\pm$ Sign separation
7) Secondary vertex location
8) Low momentum tracking
9) Full event reconstruction

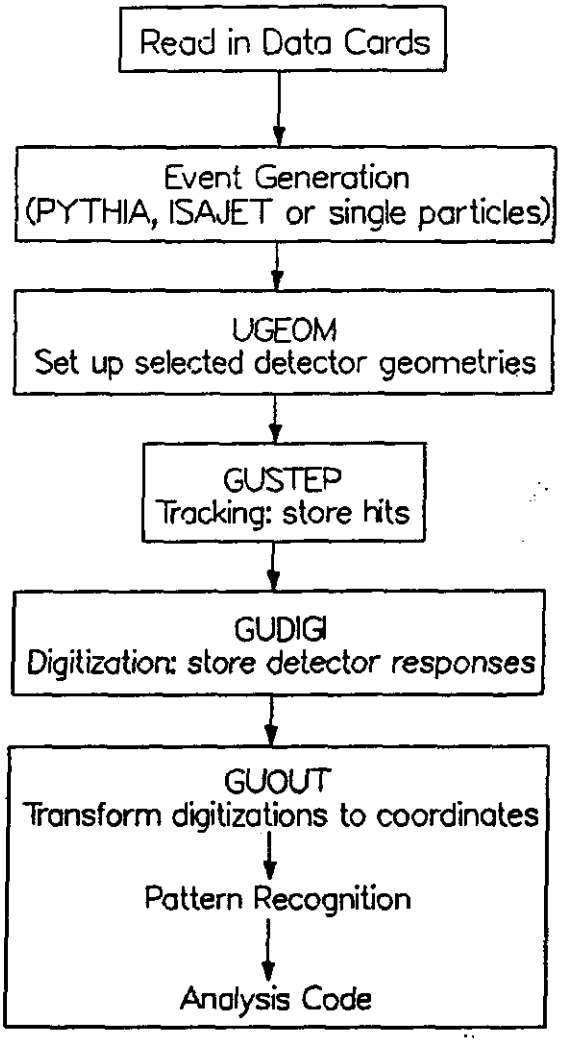


Figure 7.3.1

M. BROOKS, LOS ALAMOS

Impact Parameter and Momentum Resolution for Various Geometries in the Barrel Region

(Single track muons at 20 GeV)

Si layers	Si radii*	Pads layers	Pads radii	impact param.**	Δp/p	Δp/p w/ vert
Baseline 1						
6	10,16,22	9	35,50,65	26	0.07	0.06
		9	25,45,64	26	0.07	0.06
		6	47,67	25	0.11	0.05
Baseline 2						
6	13,20,28	9	35,50,65	27	0.08	0.06
		4	64-67	28	0.09	0.04
		6	40,65	26	0.07	0.06
Minimal Number of Layers						
4	13,28	4	64-67	28	0.15	0.06
Just Silicon						
6	13,20,28	0	—	79	0.31	0.12
Just Pads						
0	—	9	35,50,65	400	0.26	0.10
0	—	9	25,45,65	180	0.15	0.07

* in cm
** microns
***Errors are approximately 20%

THREE POINTS ARE NECESSARY FOR IMPACT PARAMTER, P RESOLUTION. TOTAL NUMBER NEEDED AND SPACING WILL BE DETERMINED BY PATTERN RECOGNITION CAPABILITIES.

Table I

M. BROOKS, LOS ALAMOS

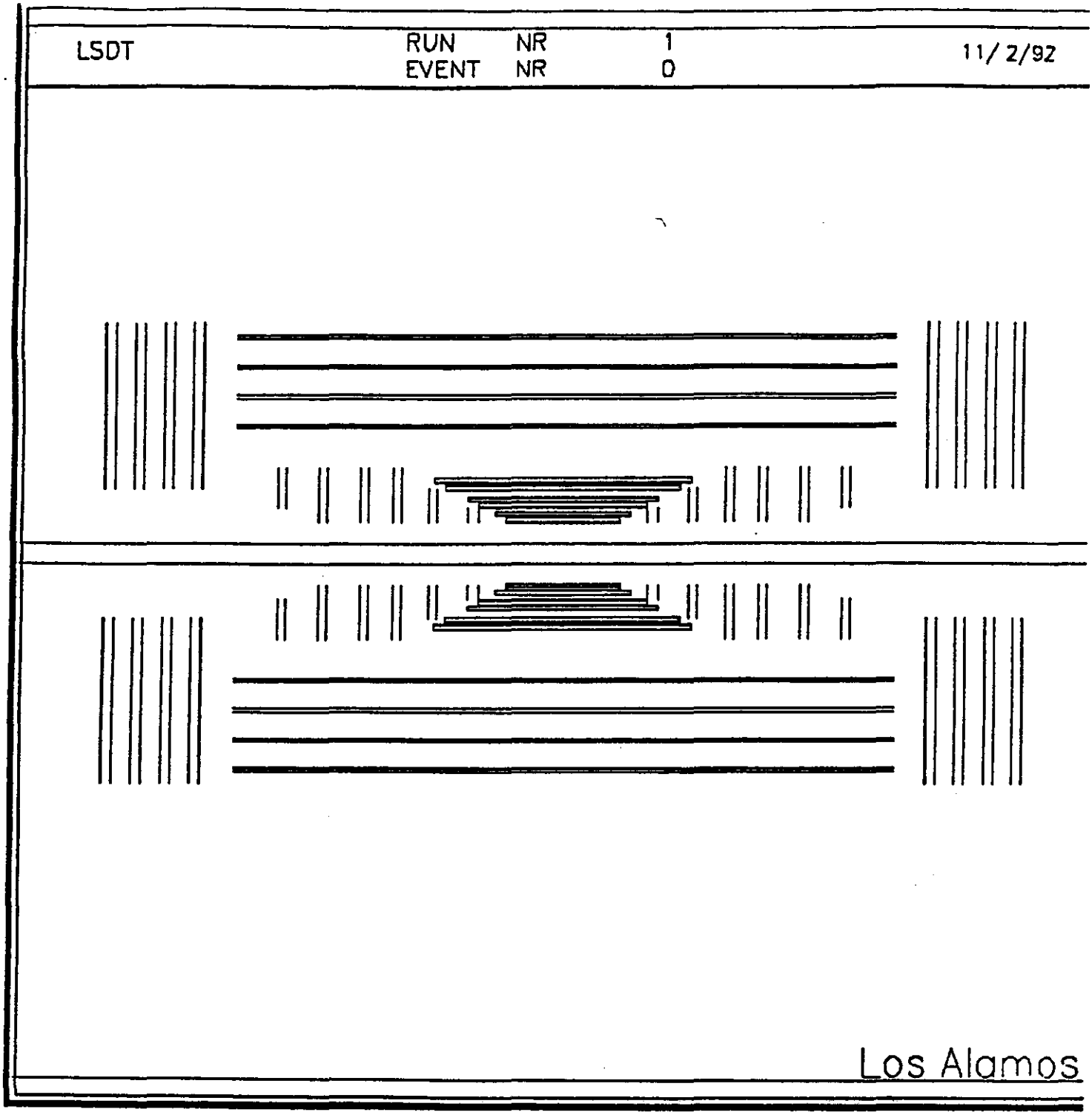


Figure 7.3.2

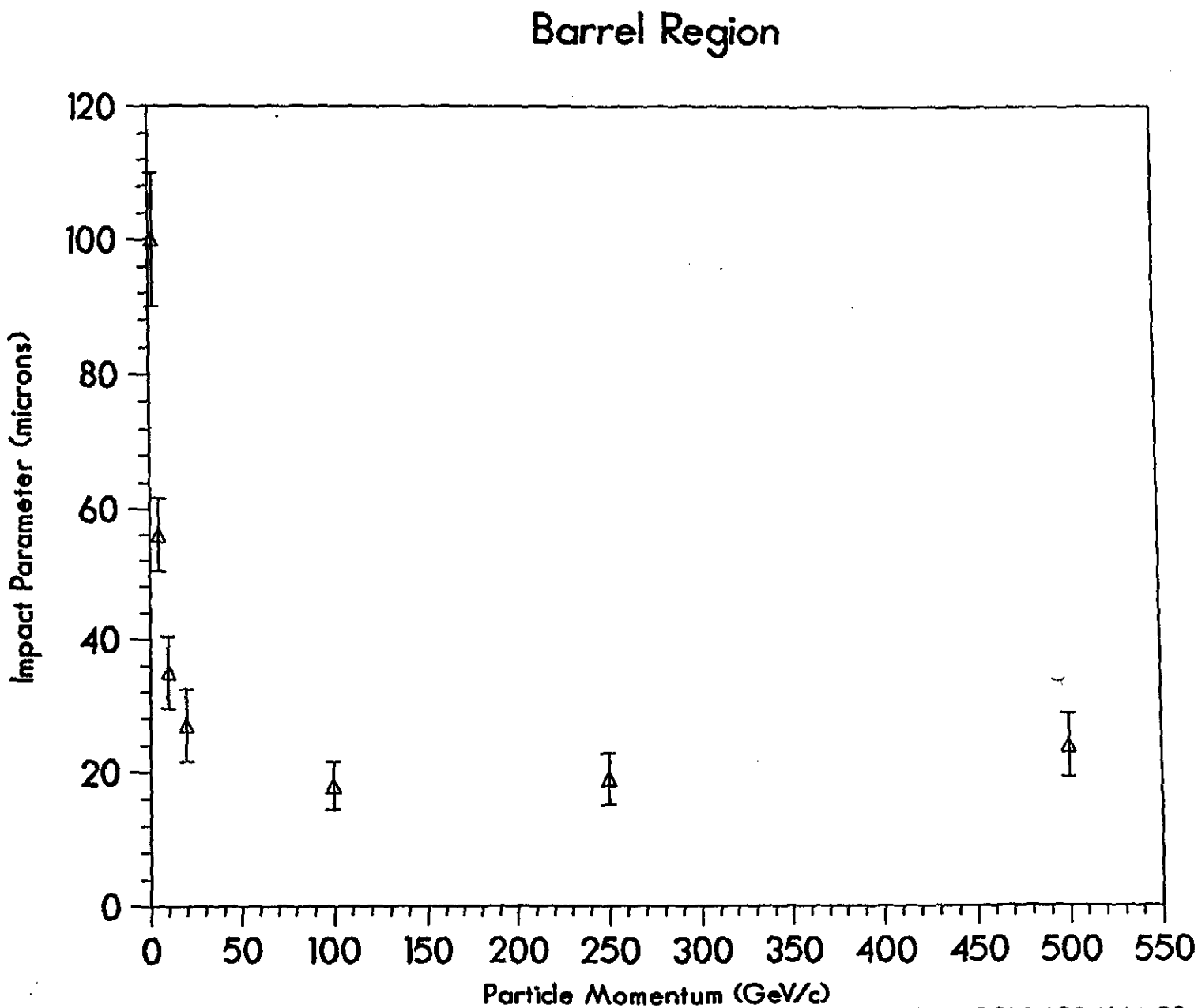


Figure 7.3.3

M. BROOKS, LOS ALAMOS

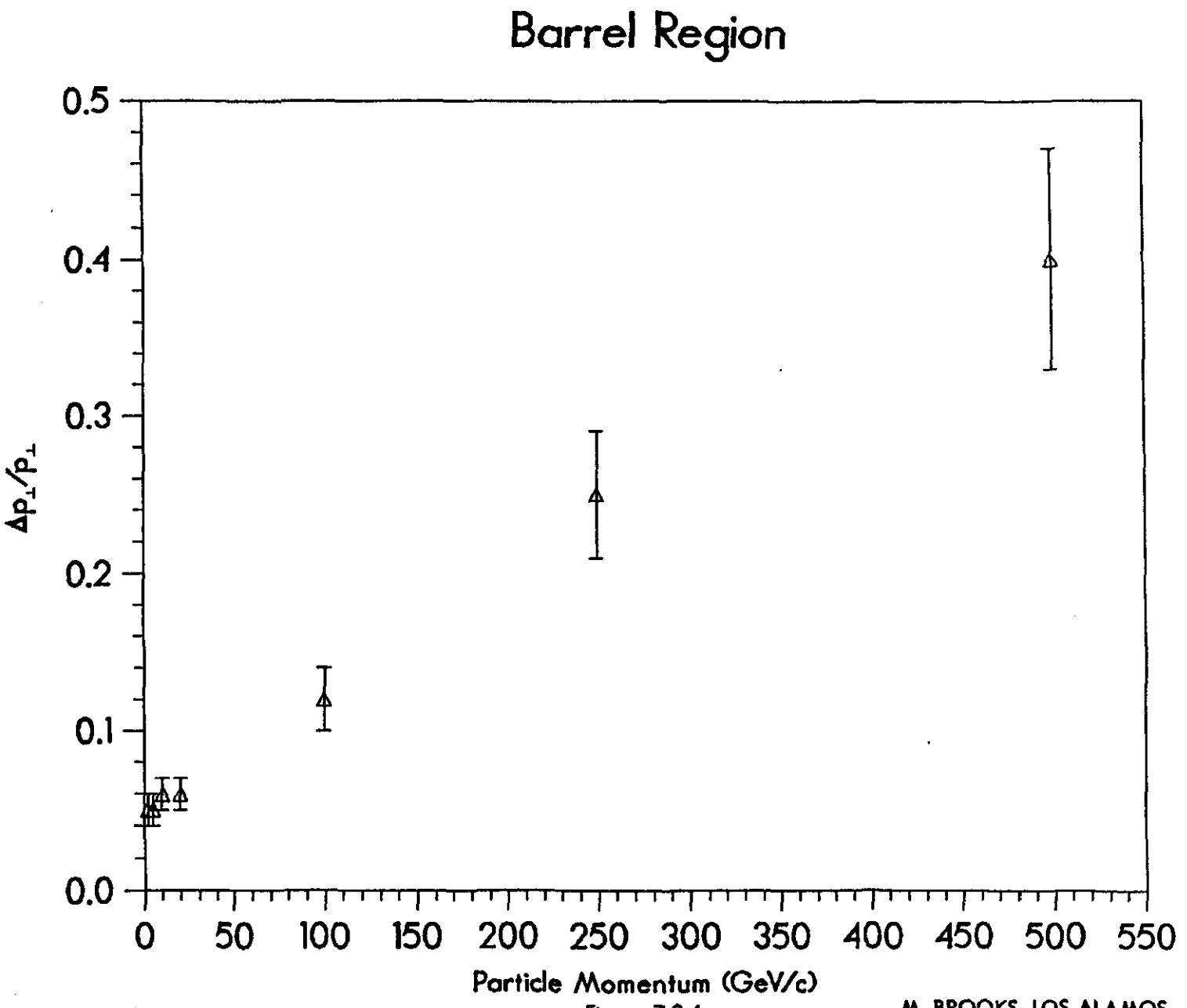
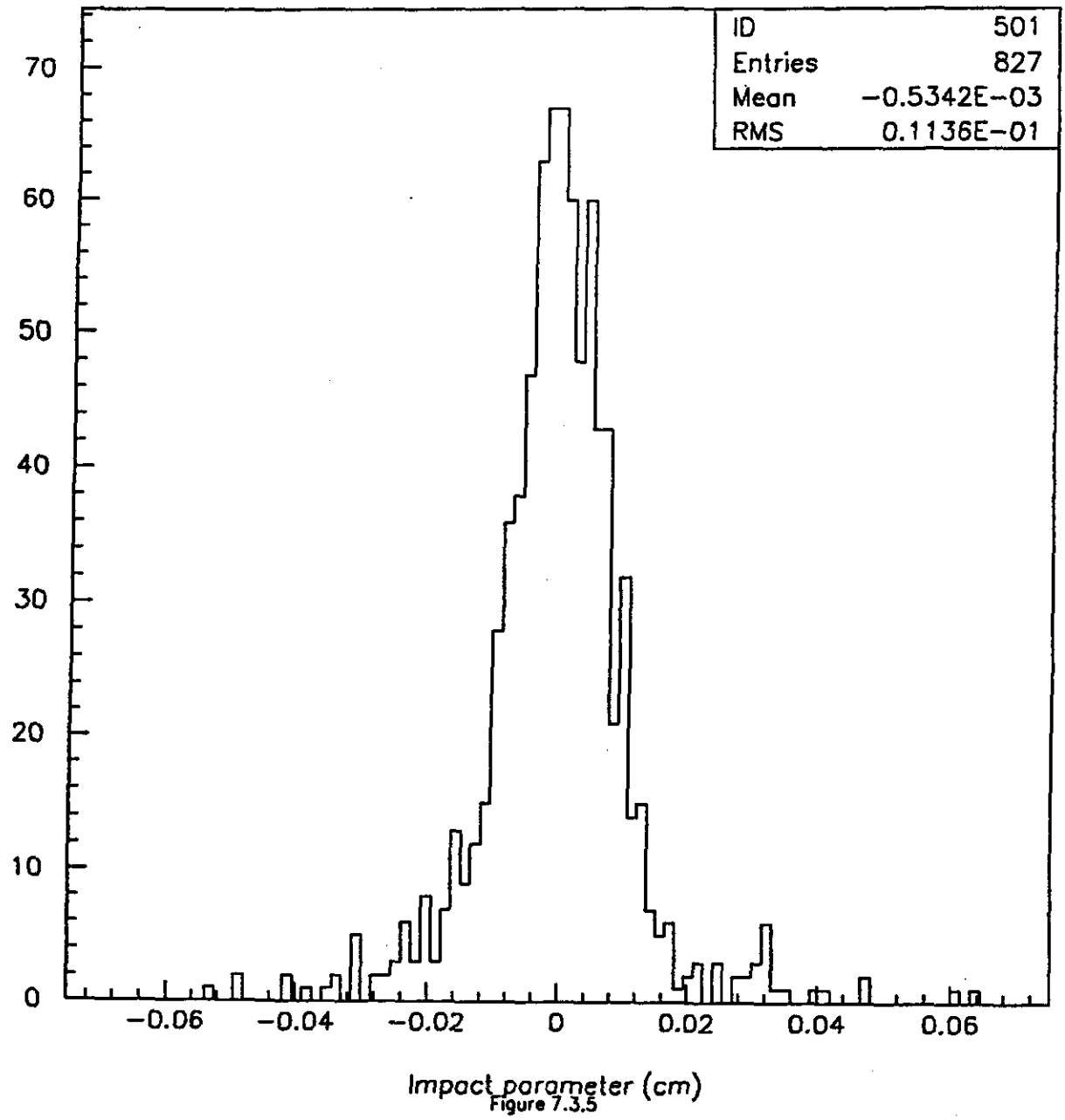
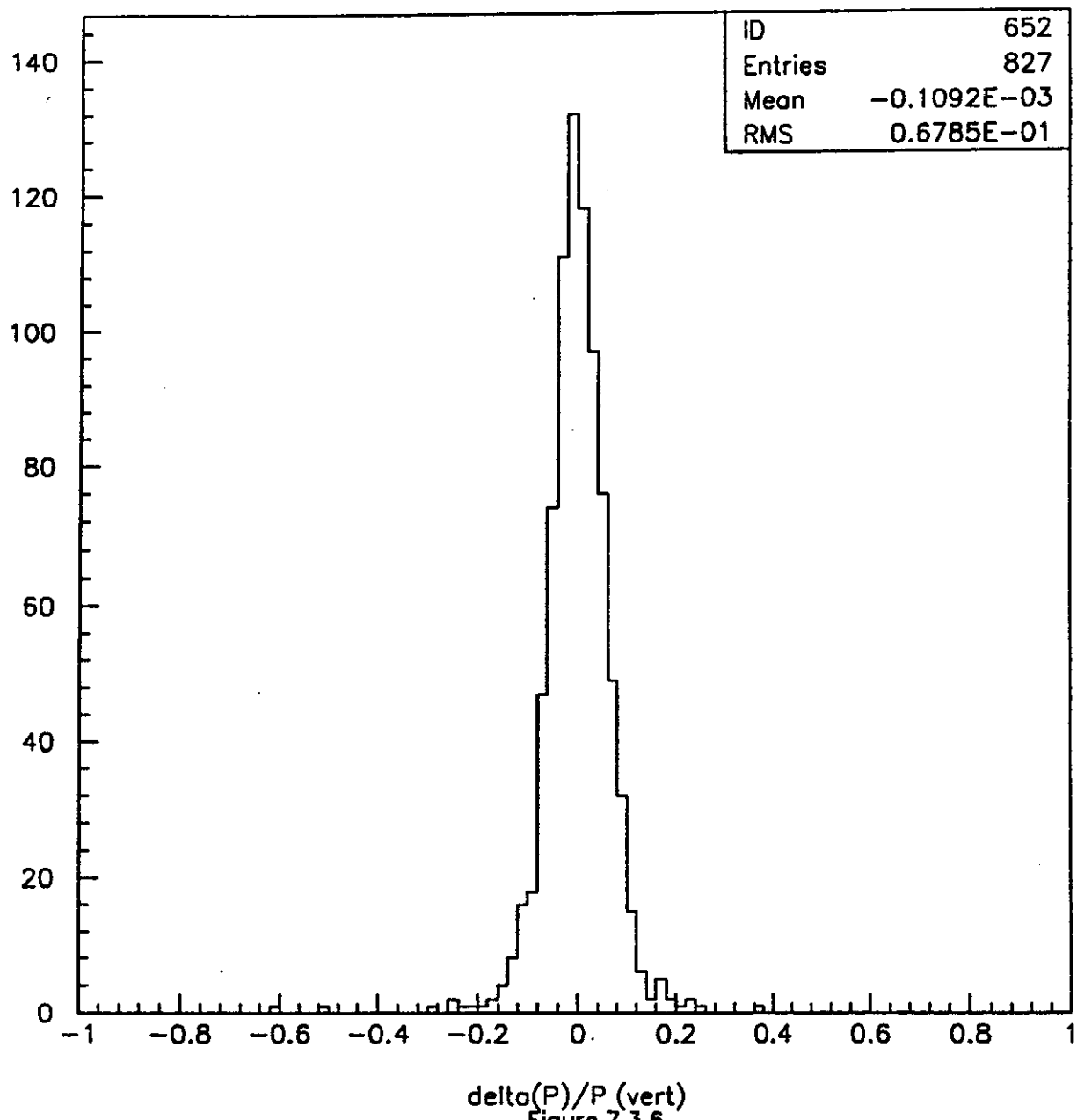


Figure 7.3.4

M. BROOKS, LOS ALAMOS


ID 501
Entries 827
Mean −0.5342E−03
RMS 0.1136E−01
70
60
50
40
30
20
10
0
−0.06
−0.04
−0.02
0
0.02
0.04
0.06
Impact parameter (cm)
Figure 7.3.5


ID 652
Entries 827
Mean −0.1092E−03
RMS 0.6785E−01
140
120
100
80
60
40
20
0
−1
−0.8
−0.6
−0.4
−0.2
0
0.2
0.4
0.6
0.8
1
delta(P)/P (vert)
Figure 7.3.6

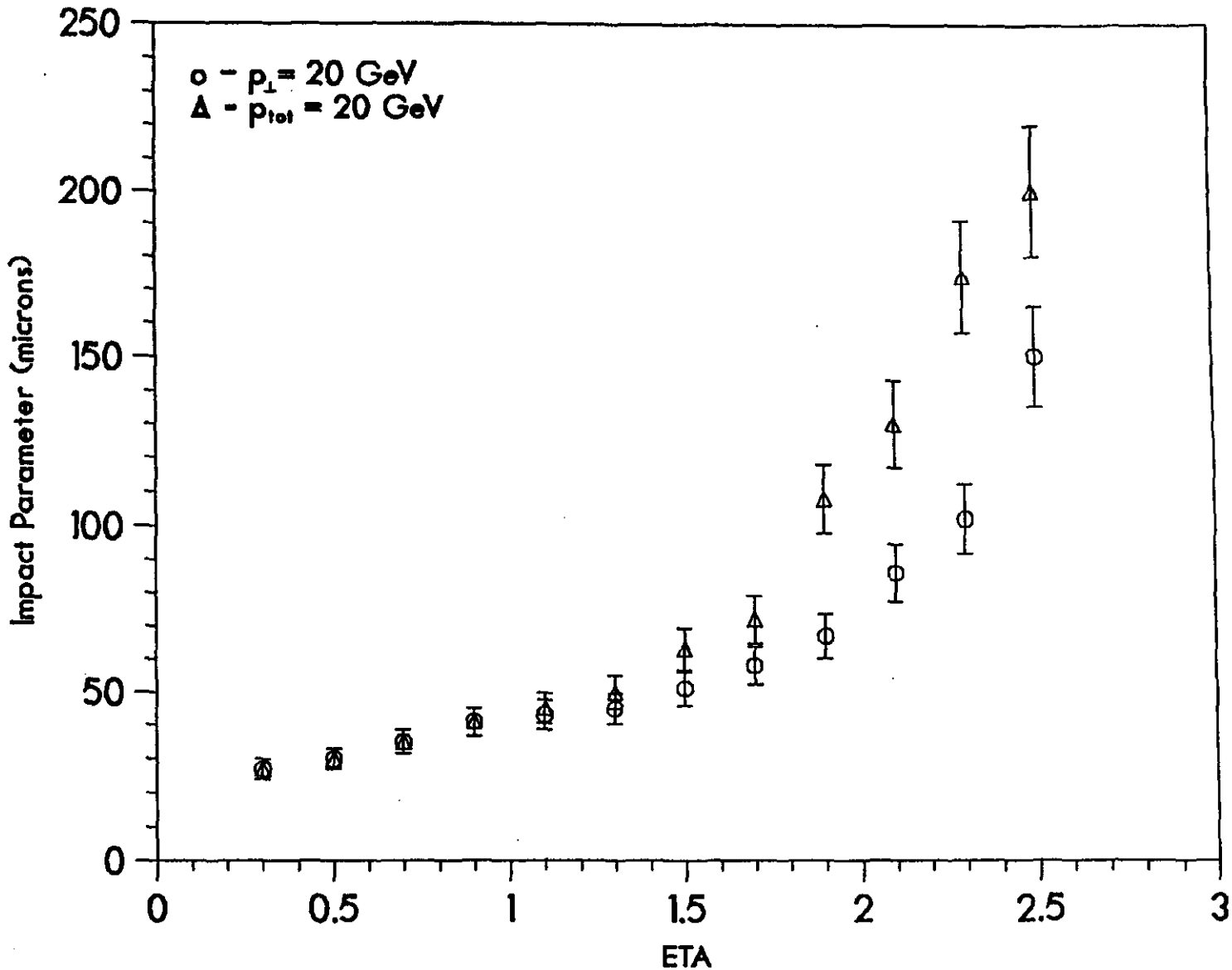


Figure 7.3.7

M. BROOKS, LOS ALAMOS

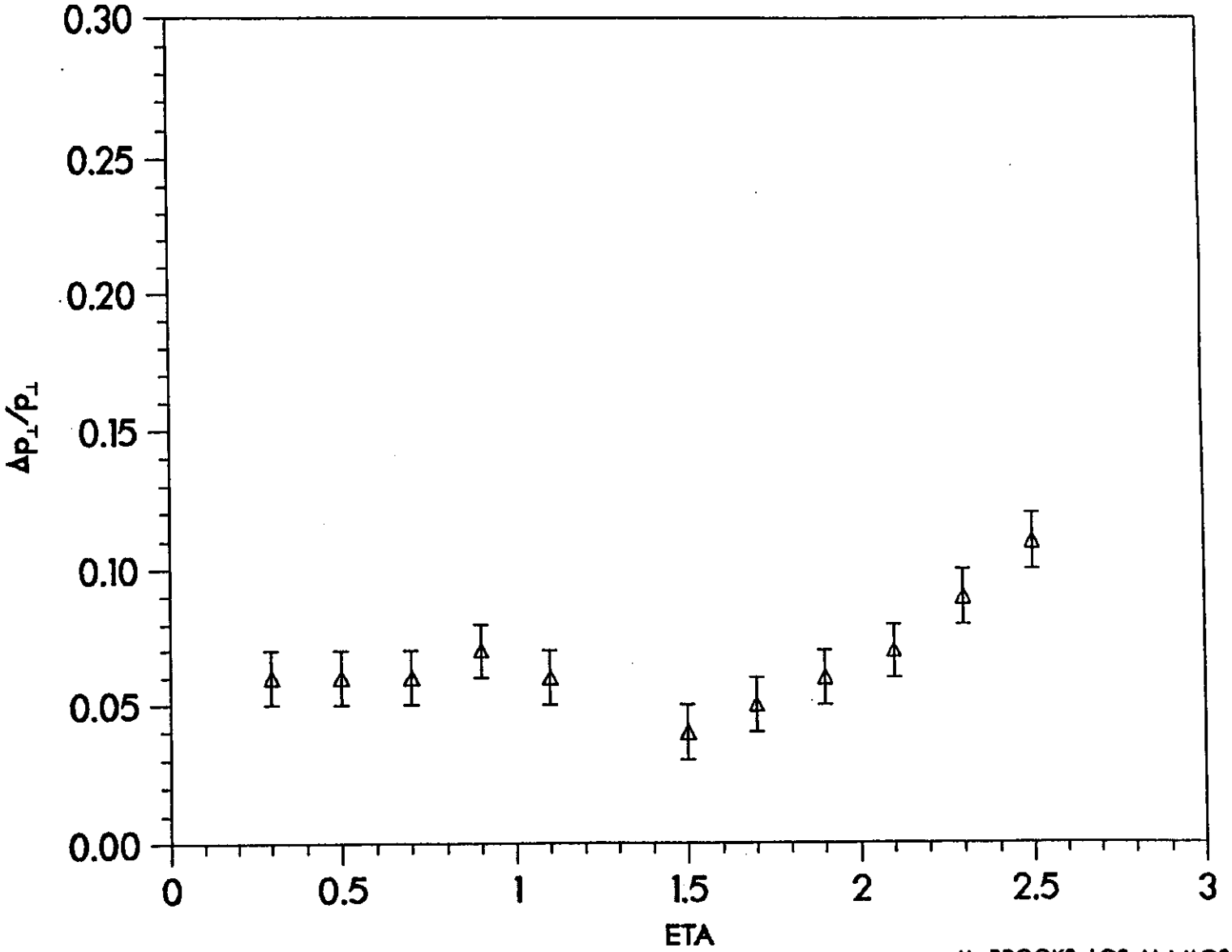
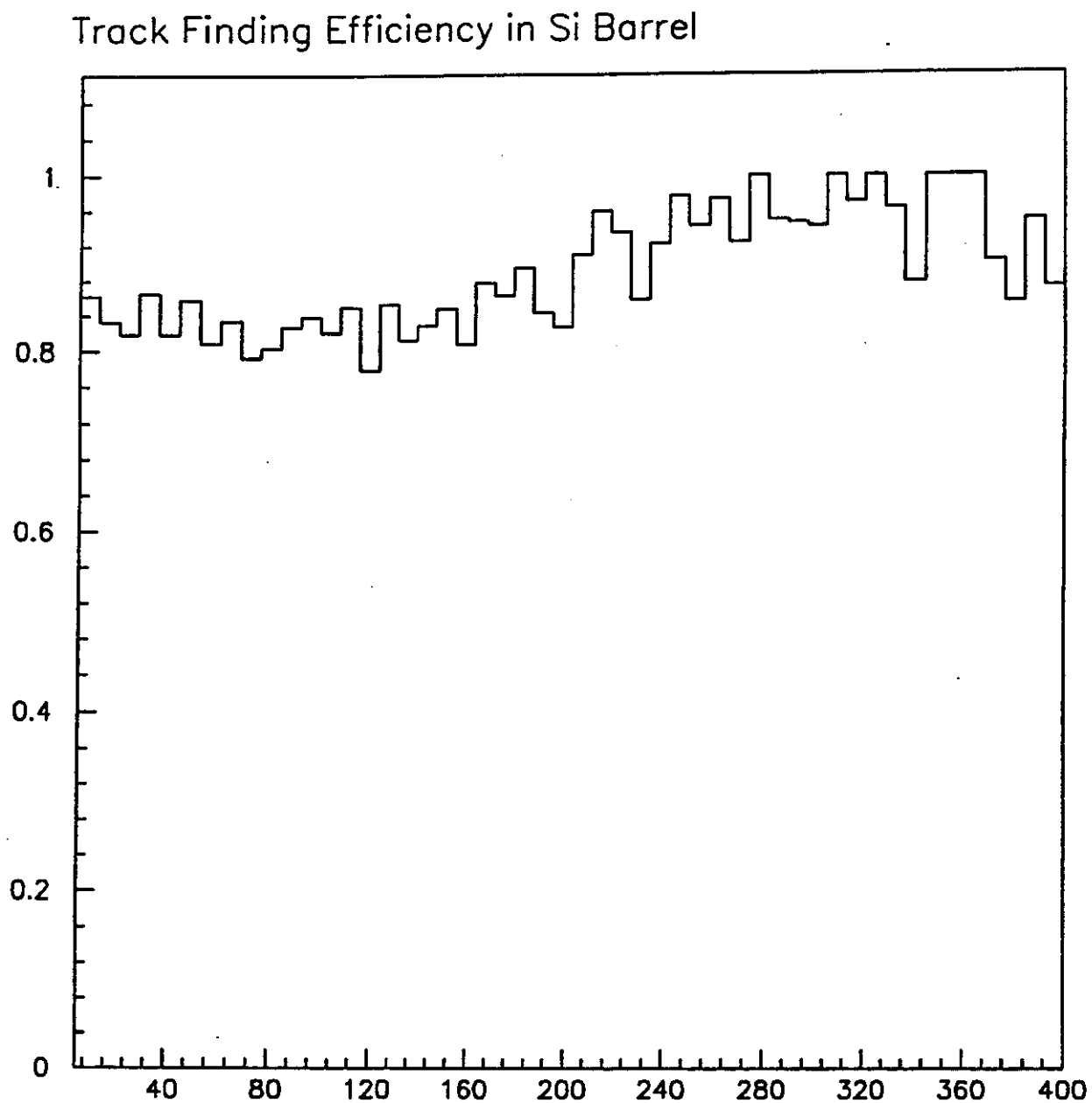


Figure 7.3.8

M. BROOKS, LOS ALAMOS



M. Brooks, Los Alamos

Figure 7.3.9

Physics Processes	Id. Primary Vertex	e/γ Separation	e, μ, γ Isolation Cuts	e/h Separation	Muon Momentum Check	e± Sign Separation	Secondary Vertex	Low Momentum Track	Full Event Reconstr.
$H^0 \to \gamma + \gamma$	X	X	X						
$H^0 \to e^+e^-l^+l^-, e^+e^-\nu\bar{\nu}, e^+e^-$ *jetjet*	X	X	X	X		X			
$H^0 \to \mu^+\mu^-l^+l^-, \mu^+\mu^-\nu\bar{\nu}, \mu^+\mu^-$ *jetjet*	X		X		X				
Gluino Pair Prod $\tilde{g}\tilde{g} \to e^\pm e^\pm, \mu^\pm e^\pm$	X	X	X	X	X	X			
Techni eta $\eta_T \to b + \bar{b}$ or $t + \bar{t}$	X		X				X		
WW Scattering $W^\pm W^\pm \to e^\pm e^\pm, \mu^\pm e^\pm$	X	X	X	X	X	X			
$Z^1 \to e^+e^-$ Asymmetry	X	X	X	X		X			
B Physics, e.g. $B \to \Psi$, etc.	X						X	X	X
Top Physics $t \to W + b$, etc.	X		X				X	X	X

CENTRAL TRACKER PHYSICS STUDIES

Table 2.3

8 R & D Progam and Test Beam Needs

8.1 Central Tracker R & D

The GEM Central Tracker R&D program supports the development of the two technologies included in the Central Tracker baseline design, Interpolating Pad Chambers (IPCs), and Silicon Microstrip Detectors. Backup Central Tracker designs incorporate detector technologies which are all under active development in the SDC R&D program , allowing us to focus our efforts on detectors which hold the most promise for the GEM Central Tracker. An important consideration in developing our R&D program was determining ways in which our work can be made complimentary to the SDC effort, particularly in the development of the Silicon Microstrip detectors. Our efforts will be directed towards those aspects of the GEM Central Tracker design which differ significantly from the SDC design, as well as areas in which it is important to develop independent expertise, such as front end electronics. The ultimate goal of our program is the development and testing of full scale working prototypes by the end of 1994. Progress towards that goal will proceed in parallel for the IPCs and Silicon Microstrips through a number of stages, which we outline below. It should be noted that the R&D programs for the IPCs and the Silicon Microstrip detectors are structured somewhat differently in the early stages, in recognition of the fact that Silicon Microstrip detectors have been undergoing development for use at the SSC for some time, while IPCs do not have the same long history of generic SSC detector development.

The first stage of IPC development for the GEM Central Tracker involves addressing a number of performance issues which arise from the unique characteristics of the tracking environment at the SSC. These issues are discussed at some length in section 4, and include the high beam crossing rate, high track density, and high radiation levels which must be tolerated at the SSC. Addressing these issues is necessary in order to demonstrate proof of principle for IPC usage, and therefore has the highest priority in our short term R&D plans. We are now in the final stages of designing a set of prototype IPC detectors which will be used to carry out a series of studies, both in the laboratory using Cosmic Ray muons, and in test beam exposures at the IU cyclotron and at LAMPF in mid-1992. Details of these studies will be found below in the description of the FY 92 R&D program. In addition to these proof of principle studies, the first stage of the IPC R&D program includes the development of a mechanical design for the chamber and support structure which minimizes material thickness, along with the initial design of the front end readout electronics. The second stage of the IPC R&D program involves the fabrication of a full scale prototype chamber, incorporating the results of the initial prototype studies, including optimal cathode layout, wire spacing, and other chamber parameters into the mechanical design. This detector will be instrumented with the same hybrid front end electronics used for the initial prototype studies. A beam test of this prototype would occur in early to mid 1993. During this time period the readout electronics development will progress to the point where prototypes can be fabricated. The final stage of the IPC R&D program involves the integration of this front end electronics with a full scale IPC chamber. The culmination of the IPC R&D program will consist of a series of beam tests using this chamber, to take place in mid 1994.

The Silicon Microstrip R&D plan extends through 1994. In 1992, silicon bonding procedures will be investigated, including tests for radiation tolerance. In addition, a detailed design of the Silicon readout electronics will be undertaken, along with an investigation of rad-hard IC fabrication processes. Further details of the FY 92 Silicon R&D plan are found below. In 1993, R&D will be carried out on the cooling systems for both the Silicon Microstrips Detectors and IPC's. At this time, the electronics design will have progressed to the point where detailed thermal modeling will be possible. The active alignment system will be prototyped during FY 93 and FY 94, as will the Silicon ladder assembly. During this period, the readout electonics design will proceed though a series of fabricated prototypes to a final tested design in FY 94.

8.1.1 FY92 R & D Plan

The GEM Central Tracker R&D plan has three major objectives for FY 92. These are to fully evaluate the capabilities of IPCs for use as the outer tracking detector, resolve critical mechanical design issues in both the IPCs and Silicon Microstrips, and design the readout electronics for both systems, including the production of rad-hard prototypes of critical components. Below, we outline the program proposed to accomplish these objectives.

8.1.2 Silicon Microstrip Detector Electronics R & D

The program of electronics development for the Silicon Microstrip Detectors during FY 92 includes:

- Defining the front-end electronics architecture under thermal, radiation tolerance, and cabling constraints.
- Conducting radiation studies of critical transistors in the IC fabrication processes under consideration.
- Design Proof-of-Principle ASICs for both analog and digital readout circuits.

The radiation studies will be conducted at facilities available at LANL. The design of the front end electronics will be undertaken at LANL under the direction of Sankoo Hahn. Significant progress has already been made in the definition of the front end electronics, as discussed in section 3.3. In particular, several amplifier designs have now been modeled with encouraging results. In addtion, means of data compression in the digital buffer circuit are now being studied. A preliminary design of a digital buffer design coming out of this study is presented in the appendix of section 3.3.

8.1.3 FY 92 Silicon Microstrip Detector Mechanical R & D

The program of mechanical R&D and engineering for the Silicon Microstrip Detectors will proceed in the following areas:

- Modeling of the cooling system.
- Developing techniques for bonding the single sided wafers together which maintain mechanical tolerances.
- Design of an in-situ alignment system.

The baseline cooling design will be similar to the SDC design. However, a detailed thermal analysis of the electronics mounted on the Silicon Microstrip Detectors will be required to determine the thermal gradients through the wafer/electronics/adhesive layers. The baseline design proposal for the Silicon ladder bridge includes the use of two layers of 300 micron single sided detectors bonded back to back. The use of dual single detectors is unique to GEM, and must be developed. The integration of the silicon wafers with the graphite stiffening rib also needs to be investigated. This work will include the selection of radiation resistant, fast curing adhesives compatible with high production rates, minimal curing stresses, and low creep rate. A structural analysis of the bonded wafer assembly followed by mechanical tests will be performed to ensure that mechanical tolerances for the final design are maintained over the expected operational temperature range. The stability requirements of the Silicon Tracker will require an in-situ alignment system to verify the wafer positions. It is unlikely that a radiation source can be used to map the wafer positions once the detector is installed, so an active alignment system must be developed. An alignment system will be designed to measure any relative motion of the silicon shell subassemblies, and a study will be conducted to understand the performance limits of the proposed system. A system now under study uses speckle interferometry to obtain a three dimensional space map of detector elements in real time. A prototype of the selected design will be assembled and tested to demonstrate the performance of an integrated system. Mechanical R&D and engineering for the Silicon Microstrip Detectors will be performed by engineers at Los Alamos National Laboratory, and will be supervised by the Central Tracker Group physicists there.

8.1.4 Interpolating Pad Chamber Prototype R & D

During FY 92, a series of studies will be conducted using IPC prototypes constructed at Indiana University. These studies are designed to address the outstanding issues regarding IPC performance in the GEM Central Tracker, detailed in Section 4 of this document. Specifically, the results of these studies will include:

- Determination of a suitable chamber gas.
- Measurement of the detector resolution using a high bandwidth front end.
- Measurement of the detector resolution in an 8 kG magnetic field.
- Measurement of the space charge effects at high singles rates.

Most of these studies require that a suitable chamber gas be used, as the results are gas-dependent. This work is already underway at Indiana University using a chamber designed

to make precision Lorentz angle measurements, and a 10 kG magnet on loan for the IU cyclotron., with some preliminary results presented in section 4 of this document. Lorentz angle and gain measurements will be perfomed initially for Freon/CO_2 mixtures, which have been shown to combine a large drift velocity with a small Lorentz angle. This study will be conducted without support from FY 92 GEM R&D funds. Following the selection of a gas, the IPC prototype studies will begin. Construction of the prototypes used in these studies is now underway at IU. The initial measurements will be made using an X-ray source and long shaping time amplifiers to establish a baseline for determining the effects of short shaping times on detector resolution. Several pad geometries, including chevron pads of various lengths, and straight rectangular pads, will be used in a set of prototype chambers to determine the properties of various pad geometries. Using the X-ray source, the differential nonlinearity of the chambers will be measured as a function of position across the pads. Next, the fast front end electronics will be installed on the prototypes. The fast front end hybrids are being supplied by Brookhaven National Laboratory, and readout boards using these hybrids will be fabricated at IU. These hybrid front ends will be designed to mimic as closely as possible the chamber electronics used on the final detector. Initial resolution studies of the fast chambers will be conducted using the X-ray source, and the results of this measurement will be compared with the resolution of the same chamber using long shaping times. Subsequent studies will use Cosmic Ray muons and an 8 kG magnet to determine the effects of a magnetic field on position resolution, and the dependence of position resolution on incident angle. Next, a prototype chamber will be exposed to a high incident particle flux at the IU cyclotron to determine the effects of space charge on chamber gain as a function of incident flux. Finally, a series of beam tests LAMPF, conducted in association with the GEM Central Tracker Group at Los Alamos, will be performed to determine the double track resolution of the chambers at high incident flux.

8.1.5 Interpolating Pad Chamber Mechanical R & D

The engineering of the IPC chambers will be conducted at Yale during FY 92, with coordination of the engineering effort by Will Emmet. The goal of this program is the construction of a full scale mechanical prototype of a barrel IPC during FY 92. In addition, Yale will carry out a design study of the mechanical support for the IPC system. A critical aspect of the IPC system design is the minimization of material thickness in the chamber and support structures. To this end, the Central Tracker Group at the University of Michigan is working to develop a low mass IPC cathode. They are presently investigating the use of a multi-layer Kapton cathode, or thin films on a low mass substrate, such as Rhoacell foam. Techniques for feeding through the signal lines from the cathode plane to the readout lines must be developed. Emphasis will be placed on minimizing material thickness while keeping electronics crosstalk to acceptable levels. The engineering and technical work at UM will be conducted by Dave Kouba. In addition, the Washington University group will design a power and high voltage distribution system for the IPC system, and assist Yale in the chamber and support engineering.

8.1.6 Interpolating Pad Chamber Electronics R & D

The electronics R&D program for the IPCs is being directed by the GEM Electronics Group, which includes members of the Central Tracker Group. The FY 92 R&D program of IPC electronics development is presently divided into three areas. These are the front end amplifier

design, development of a rad-hard analog pipeline, and the design of the overal l readout archetecture. At BNL, the front end preamplifier and shaping amplifier are being designed by Paul O'Connor. Significant progress has already been made, as discussed in section 4. Prototype CMOS implimentations of a preamp and shaping amp have been developed, and we are now in the process of fabricating prototypes on MOSIS. These prototypes will be evaluated at BNL. Following this, a rad-hard process will be selected from a list of possibilities, including the Harris UHF process and the rad-hard CMOS process offered by UTMC. The goal of this program is the fabrication of an eight channel preamp/shaper prototype in a rad-hard process by the end of 1992. The development of the rad-hard pipeline and FADC chip which is at the heart of the IPC readout electronics is being developed at Oak Ridge National Laboratory under the direction of Chuck Britton. ORNL had established contacts with several vendors of rad-hard IC fabrication processes, and has non-disclosure agreements with Harris and UTMC, a prerequisite for proceeding with a rad-hard design. ORNL will first fabricate a small prototype of the pipeline in a non-radhard process, preferably one which has the same or similar design rules to an appropriate rad-hard process. An implimentation in the rad-hard process selected for use will then be developed, with the goal of fabricating a rad-hard prototype by the end of 1992. Given the cost of rad-hard fabrication runs, it would be highly advantagous if the prototype fabrication runs of the preamp/shaper, the analog pipeline,and possibly, components of the Silicon Microstrip readout, could be combined. It is not clear at present that a single rad-hard process will satisfy the requirements of these various applications, but in light of the substantial cost savings that would result, a serious effort will be made to determine whether a single process can be used, and to coordinate fabraction runs.

8.2 Test Beam Needs

The Central Tracker test beam program is designed to provide answers to critical questions concerning the performance and viability of Interpolating Pad Chambers and Silicon Strip Detectors and their associated electronics in the GEM environment.

8.3 Interpolating Pad Chamber Test Beam Plans

8.3.1 IPC Test Beam Activities in 1992

The first task is to establish the chamber operating parameters using a small IPC. This device is being prepared at Indiana and will be installed in a Lampf test beam at Los Alamos in the summer of 1992. Preliminary studies conducted at Indiana have indicated that a gas mixture of CO2:CF4 (70:30) shows promise. In the Los Alamos test further gas studies will be done and HV parameters will be explored and defined. The modest beam requirements for these studies can be met at the Lampf Test Channel, which provides a low rate of electrons, muons, and pions of a few hundred MeV's. One month of beam time should be adequate to complete this work.

8.3.2 IPC Test Beam Activities in 1993

By early 1993 a realistic prototype of a barrel IPC will be available for resolution studies in a test beam. The chamber will be moveable with respect to the beam to allow scanning of the entire active area. These studies require minimum ionizing particles and very good beam definition. The beam must be instrumented with a silicon telescope to define particle trajectories to about 10 microns. A rate of a few particles per second and about three months beam time will be necessary.

8.3.3 IPC Test Beam Activities in 1994

A full sized prototype of both barrel and end cap IPC's with final electronics will be available for rate capability studies in 1994. A high rate secondary beam is required with about 10^9 particles per second. The beam will be spread over a 30 cm^2 region of the chambers to simulate the effects of the expected charged particle rate at a luminosity of $10^{34}\ cm^{-2}s^{-1}$. Three months beam time should be adequate to complete the tests.

8.3.4 IPC Test Beam Activities in 1995

Full systems tests are planned for 1995. Final designs of all cooling, alignment, connection and supply systems will be fully tested in a realistic beam environment. The beam requirements are the same as for 1994 and it is preferred to use the same beam to reduce additional set up delays.

8.4 Silicon Tracker Test Beam Plans

To ensure the viability of the Silicon Tracker, one of the first issues to be explored is that of radiation hardness. Studies will be begun at Lampf in Los Alamos in the summer of 1992. Additional test beam requirements for the Silicon are not well defined at the present.

GEM Central Tracker
Interpolating Pad Chamber
Test Beam Needs 1992 - 1995

Time	Device/Test	Beam Location or Parameters	Required Beam Time
mid 1992	operating parameters of a small chamber	Los Alamos, low rate secondary beam, a few hundred MeV e's, μ's, π's	1 month
early 1993	Resolution of full sized prototype of barrel pad chamber, scan over the full length of the device	e's, μ's, π's of a few GeV, protons $\geq$ 5 GeV, rate: a few particles/sec. well collimated beam with position measurement	3 months
early 1994	rate capabilities of full sized prototype, both barrel and end caps, with final electronics	high rate secondary beam ~10^9 particles/sec. which can be spread over ~30 cm^2 in the chamber	3 months
1995	Systems Tests: gas, cooling, mechanics, etc. of final design	same as 1994	3 months

2/18/92-KM

9 Central Tracker Schedule

The first version of the GEM Central Tracker schedule is shown in Table 9.1.

We envision a three-year conceptual design and R & D period, 1992, 1993 and 1994. The bulk of the detailed engineering design will also take place during these three years, although some engineering design will stretch out through 1997. Building and testing of various prototypes will also take place from 1992 to 1994.

The construction of the various components of the tracker is anticipated to take place at the various collaborating institutions away from the SSC site over a four-year period from 1994 to 1997. The various components will be shipped to the SSC Lab and the assembly of the central tracker will occur in the surface building designed for this purpose at the experimental site between mid 1997 and mid 1998. Calibration, alignment and various test activities will also take place during this year.

We expect that the complete central tracker, including the pad chambers and the silicon detector, will be installed in GEM in mid 1998. This will be followed by a year of finishing up the cabling, cooling, and gas connections and the final commissioning of the detector. The schedule calls for the detector to be ready for data-taking by mid 1999. This schedule will be refined and updated as appropriate as the central tracker, the GEM detector and the SSC collider progress.

REV. 1 (2/13/1992)

GEM CENTRAL TRACKER SCHEDULE

ACTIVITY	91	92	93	94	95	96	97	98	99
Expression of Intent	Δ								
Conceptual Design/R&D Effort	├	─	─	┤	- - -	- - -			
Letter of Intent	Δ								
Choice of Technologies		Δ							
Detailed Engineering Design		├	─	┤	- - -	- - -	┤		
DESIGN REPORT		Δ							
Build Prototypes		├	─	┤					
Test Prototypes			├	─	┤				
Construction (off-site)				├	─	─	┤		
Assembly (at SSCL)						├	─	┤	
Installation in GEM								Δ	
Commissioning								├	┤
Ready for Data									Δ

Table 9.1

10 Budget Estimates

10.1 R & D Budgets

The R & D and conceptual Engineering Design Plan for the Central Tracker for 1992 is now in place. The budget agreed to for this activity is summarized in Table 10.1. This budget includes both GEM R & D funds (842 K$) and non-GEM funds from Yale and Indiana Universities (336 K$) for a total program in 1992 of 1178 K$.

The requests for R & D funds from GEM for 1993 and 1994 are 2600 K$ for each year. The overall R & D Budget Plan for the central tracker for the three years is summarized in Table 10.2.

10.2 Central Tracker Fabrication Budget

A Work Breakdown Structure (WBS) has been developed for the central tracker. This WBS has been used to generate the first budget estimate for the fabrication of the central tracker. This is a "bottoms up" budget. Some of the estimates, especially those for materials and supplies, are based on vendor quotations. Many other items are expert estimates by the designing engineers.

In interpreting this budget it must be kept in mind that we are at a very early stage of this project and most of the detailed engineering design and evaluation of prototypes is still ahead of us. This budget is thus at best preliminary at this time. This budget will be updated and refined as our design progresses in the near future.

The budget is presented at WBS level 3 in Table 10.3 and at WBS level 5 in Table 10.4.

The breakdown of the budget into the various subsystems is shown in Fig. 10.1. In Fig. 10.2 we show how the budget breaks down into various categories such as engineering and design costs, materials, labor, inspection and quality assurance and contingency.

Subsystem	GEM	Non GEM	Total
Silicon Tracker			
Mechanical	270	0	270
Electronics	270	0	270
Pad Chambers			
Mechanical	150	226	376
Electronics	110	110	220
Test Beam Work	42	0	42
Total	842	336	1178

Table 10.1: Central Tracker R & D Budget for 1992 (in units of 1000$)

Subsystem	1992	1993	1994	3-Year Totals
Silicon Tracker				
Mechanical	270	600	600	1470
Electronics	270	600	600	1470
Pad Chambers				
Mechanical	376	600	600	1576
Electronics	220	600	600	1420
Test Beam Work	42	200	200	442
Total	1178	2600	2600	6378

Table 10.2: Central Tracker R & D Plan (in units of 1000$)

LEVEL III REPORT

WBS No.	Title	Engineer & Design				Inspection Q/A			Proc/Fab	Installation/ Assembly					Totals				
		Labor	Rate	Total	M & S	Labor	Rate	Total	Material	Labor	Rate	Subtotal	Material	Total	Labor	Material	Subtotal	Contin.	Total K$
5.2.2.3.5	CENTRAL TRACKER	53.2	106.4	5662	1762	30.3	91.0	2757	18611	55.8	63.1	3521	680	4201	11939	21053	32992	12562	45555
5.1	Silicon Tracker	29.5	104.4	3080	590	10.4	91.5	952	9279	26.4	72.8	1922	530	2452	5954	10399	16353	5556	21909
5.1.1	Mech Struct & Cooling	18.2	104.2	1896	364	4.5	90.2	406	3486	12.5	72.9	911	330	1241	3213	4180	7393	2541	9934
5.1.2	Silicon Detector	3.3	110.3	364	66	2.0	84.0	168	3010	4.4	84.5	372	110	482	904	3186	4090	1227	5317
5.1.3	Detector Electronics	4.5	102.2	460	90	1.8	97.8	176	1825	3.0	82.3	247	40	287	883	1955	2838	1135	3973
5.1.4	Data Aquisition	3.0	100.0	300	60	0.6	86.7	52	778	4.5	60.4	272	30	302	624	868	1492	448	1940
5.1.5	Det Calibration & Test	0.5	120.0	60	10	1.5	100.0	150	180	2.0	60.0	120	20	140	330	210	540	205	745
5.2	Pad Tracker	20.6	108.3	2229	1110	5.0	64.8	324	8932	21.4	51.9	1111	50	1161	3664	10092	13756	5944	19700
5.2.1	Superlayer modules	5.0	93.0	461		0.2	51.0	12	2235	14.1	35.6	502		502	975	2235	3210	1284	4494
5.2.2	Support structure	4.0	93.0	372		0.2	51.0	8	272	0.9	51.0	44		44	424	272	696	278	974
5.2.3	Electronics	9.0	120.0	1084	1060	1.0	120.0	120	6025	1.0	80.0	80	50	130	1284	7135	8419	3873	12292
5.2.4	Gas system & cooling	1.6	137.1	219	50	0.0				3.0	120.0	360		360	579	50	629	189	818
5.2.5	Alignment Systems	1.0	93.0	93					400						93	400	493	197	690
5.2.6	Subsystem Assembly	0.0				0.0				2.5	102.0	125		125	125		125	50	176
5.2.7	Calibration and Testing	0.0				3.6	51.0	184		0.0					184		184	73	257
5.3	Detector Assembly	2.1	110.7	233	42	0.9	101.1	91	170	4.0	61.9	248	70	318	571	282	853	341	1194
5.3.1	Assembly Tooling	1.5	107.0	161	30	0.2	90.0	18	120						179	150	329	131	460
5.3.2	Assembly	0.3	120.0	36	6	0.5	110.0	55		2.5	60.0	150	30	180	241	36	277	111	388
5.3.3	Alignment Verification	0.3	120.0	36	6	0.2	90.0	18	50	1.5	65.0	98	40	138	152	96	248	99	347
5.4	Subsystem Installation	1.0	120.0	120	20	1.0	120.0	120	230	4.0	60.0	240	30	270	480	280	760	213	973
5.4.1	Detector Installation	0.5	120.0	60	10	0.5	120.0	60	200	2.0	60.0	120	10	130	240	220	460	129	589
5.4.2	Detector Support Sys Installation	0.5	120.0	60	10	0.5	120.0	60	30	2.0	60.0	120	20	140	240	60	300	84	384
5.5	Subsystem Project Management	0.0				13.0	97.7	1270							1270		1270	508	1778
5.5.1	Silicon Tracker	0.0				5.0	94.0	470							470		470	188	658
5.5.2	Pad Tracker	0.0				5.0	94.0	470							470		470	188	658
5.5.3	Integration	0.0				3.0	110.0	330							330		330	132	462

Table 10.3

CENTRAL TRACKER SYSTEM COST ESTIMATE

WBS No.	Title	Engineering & Design				Inspection Q/A			Proc/Fab	Installation / Assembly					Totals				
		Labor	Rate	Total	M & S	Labor	Rate	Total	Material	Labor	Rate	Subtot	Mat'l	Total	Labor	Mat'l	Subtot	Conting.	Total K$
5.2.1.1.3.13	Module assembly									1.6	34.0	54		54	54		54	22	76
5.2.1.1.4	Level IV	0.5	93	45.6		0.0	0.0	0.0	245.6	1.6	34.0	54.4		54.4	100.0	245.6	345.6	138	484
5.2.1.1.4.1	Anode wire	0.0	93	5		0.0	0	0	20						5	20	25	10	34
5.2.1.1.4.2	Anode wire supports	0.0	93	5					25						5	25	29	12	41
5.2.1.1.4.3	Anode wire terminal strips	0.0	93	5					2						5	2	7	3	9
5.2.1.1.4.4	Cont cathode plane	0.0	93	5					10						5	10	15	6	20
5.2.1.1.4.5	Gas window	0.0	93	5					8						5	8	13	5	18
5.2.1.1.4.6	Cathode pad plane	0.0	93	5					80						5	80	85	34	118
5.2.1.1.4.7	Graphite epoxy composite hrdbck	0.0	93	5					51						5	51	56	22	78
5.2.1.1.4.8	End plates	0.0	93	5					20						5	20	25	10	34
5.2.1.1.4.9	Gas connectors	0.0	93	5					10						5	10	15	6	20
5.2.1.1.4.10	LV (signal) connectors	0.0	93	5					10						5	10	15	6	20
5.2.1.1.4.11	HV (anode) connectors								5							5	5	2	7
5.2.1.1.4.12	Alignment pins, misc. hard								5							5	5	2	7
5.2.1.1.4.13	Module assembly									1.6	34.0	54		54	54		54	22	76
5.2.1.1.5	Tooling and fixtures	0.5	93	46.5		0.1	51.0	6.1	135.0	0.5	51.0	24.5		24.5	77.1	135.0	212.1	84.8	296.9
5.2.1.1.5.1	Anode wire wind. machine	0.1	93	9		0.0	51	2	10	0.2	51	8		8	20	10	30	12	41
5.2.1.1.5.2	Gluing fixtures	0.2	93	19		0.0	51	2	25	0.2	51	8		8	29	25	54	22	75
5.2.1.1.5.3	Graphite/epoxy hrdbck fab. tooling	0.2	93	19		0.0	51	2	100	0.2	51	8		8	29	100	129	52	180
5.2.1.2	Endcap modules	2.5	93.0	232.5		0.1	51.0	6.1	1117.4	7.2	187.0	259.4		259.4	498.0	1117.4	1615.4	646.2	2262
5.2.1.2.1	Level I	0.5	93	46.5		0.0	0.0	0.0	245.6	1.6	34.0	54.4		54.4	100.9	245.6	346.5	138.6	485
5.2.1.2.1.1	Anode wire					0.0	0	0	20						0	20	20	8	28
5.2.1.2.1.2	Anode wire supports								25							25	25	10	34
5.2.1.2.1.3	Anode wire term strips								2							2	2	1	3
5.2.1.2.1.4	Continuous cathode plane								10							10	10	4	14
5.2.1.2.1.5	Gas window								8							8	8	3	11
5.2.1.2.1.6	Cathode pad plane								80							80	80	32	112
5.2.1.2.1.7	Graphite epoxy comp hardback								51							51	51	20	71
5.2.1.2.1.8	End plates								20							20	20	8	28
5.2.1.2.1.9	Gas connectors								10							10	10	4	14
5.2.1.2.1.10	LV (signal) connectors								10							10	10	4	14
5.2.1.2.1.11	HV (anode) connectors								5							5	5	2	7
5.2.1.2.1.12	Align. pins, misc. hardware								5.0							5	5	2	7
5.2.1.2.1.13	Module assembly	0.5	93.0	46.5						1.6	34.0	54		54	101		101	40	141
5.2.1.2.2	Level II (same as Level I)	0.5	93.0	46.5		0.0	0.0	0.0	245.6	1.6	34.0	54.4		54.4	101	245.6	346.5	138.6	485
5.2.1.2.3	Level III (same as Level I)	0.5	93.0	46.5		0.0	0.0	0.0	245.6	1.6	34.0	54.4		54.4	101	245.6	346.5	138.6	485
5.2.1.2.4	Level IV (same as Level I)	0.5	93.0	46.5		0.0	0.0	0.0	245.6	1.6	34.0	54.4		54.4	101	245.6	346.5	138.6	485
5.2.1.2.5	Tooling and fixtures	0.5	93	46.5		0.1	51.0	6.1	135.0	0.8	51.0	41.8		41.8	94.4	135.0	229.4	91.8	321.2
5.2.1.2.5.1	Anode wire wind. machine	0.2	93	19		0.0	51	2	10	0.2	51	8		8	29	10	39	16	54
5.2.1.2.5.2	Gluing fixtures	0.2	93	19		0.0	51	2	25	0.2	51	8		8	29	25	54	22	75
5.2.1.2.5.3	Graphite/epoxy hardback fab. tool	0.1	93	9		0.0	51	2	100	0.5	51	26		26	37	100	137	55	192
5.2.2	Support structure	4.0	93	372.0		0.2	51.0	8.2	271.5	0.9	51.0	43.9		43.9	424.0	271.5	695.5	278.2	974

CENTRAL TRACKER SYSTEM COST ESTIMATE

WBS No.	Title	Engineering & Design				Inspection Q/A			Proc/Fab	Installation / Assembly					Totals				
		Labor	Rate	Total	M & S	Labor	Rate	Total	Material	Labor	Rate	Subtot	Mat'l	Total	Labor	Mat'l	Subtot	Conting.	Total K$
5.2.2.3.5	CENTRAL TRACKER	53.2	106	5662	1762	30.3	91	2757	18611	55.8	63	3521	680	4201	11939	21053	32992	12562	45555
5.1	Silicon Tracker	29.5	104	3080	590	10.4	92	952	9279	26.4	73	1922	530	2452	5954	10399	16353	5556	21909
5.1.1	Mech Struct & Cooling	18.2	104	1896	364	4.5	90	406	3486	12.5	73	911	330	1241	3213	4180	7393	2541	9934
5.1.1.1	Cent Region Sub-Assemblies	3.5	109	380	70	0.8	85	68	720	2.9	69	199	90	289	647	880	1527	501	2028
5.1.1.1.1	Cen Reg Cool Rings	1.2	97	116	24	0.3	80	24	479	0.5	96	48	35	83	188	538	726	290	1016
5.1.1.1.2	Kinematic Mounts	0.5	96	48	10	0.1	80	8	81	0.2	80	16	10	26	72	101	173	43	216
5.1.1.1.3	Assembly Tooling	1.3	123	160	26	0.2	80	16	120	0.5	83	41	25	66	217	171	388	85	474
5.1.1.1.4	Assembly	0.5	112	56	10	0.2	100	20	40	1.7	55	94	20	114	170	70	240	82	322
5.1.1.2	Fwd Region Sub-Assemblies	2.5	99	248	50	0.9	93	84	552	2.6	69	180	75	255	512	677	1189	406	1595
5.1.1.2.1	Fwd Reg Cool Rings	1.0	96	96	20	0.5	96	48	383	0.4	90	36	35	71	180	438	618	247	865
5.1.1.2.2	Kinematic Mounts	0.5	96	48	10	0.1	80	8	109	0.2	80	16	10	26	72	129	201	50	251
5.1.1.2.3	Assembly Tooling	0.5	96	48	10	0.1	80	8	40	0.3	80	24	10	34	80	60	140	31	171
5.1.1.2.4	Assembly	0.5	112	56	10	0.2	100	20	20	1.7	61	104	20	124	180	50	230	78	308
5.1.1.3	Cent. Reg. Support Cylinders	1.3	105	136	26	0.3	93	28	282	0.4	75	30	10	40	194	318	512	163	675
5.1.1.3.1	Composite Cylinders	0.8	105	84	16	0.2	100	20	250	0.2	70	14	5	19	118	271	389	132	521
5.1.1.3.2	Kinematic Mounts	0.5	104	52	10	0.1	80	8	32	0.2	80	16	5	21	76	47	123	31	154
5.1.1.4	Space Frame	1.0	100	100	20	0.3	80	24	450	0.8	81	65	10	75	189	480	669	268	937
5.1.1.5	Gas Enclosure	3.4	108	368	68	0.6	87	52	504	0.8	71	57	40	97	477	612	1089	378	1467
5.1.1.5.1	Outer Enclosure	2.0	110	220	40	0.4	90	36	344	0.4	75	30	15	45	286	399	685	233	918
5.1.1.5.2	Inner Enclosure	0.8	110	88	16	0.1	80	8	98	0.2	68	14	10	24	110	124	234	84	318
5.1.1.5.3	End Enclosure	0.6	100	60	12	0.1	80	8	62	0.2	68	14	15	29	82	89	171	61	232
5.1.1.6	Detector supports	1.1	98	108	22	0.2	80	16	102	0.5	76	38	15	53	162	139	301	106	407
5.1.1.6.1	End Supports	0.6	100	60	12	0.1	80	8	85	0.1	80	8	5	13	76	102	178	75	253
5.1.1.6.2	Kinematic Mounts	0.5	96	48	10	0.1	80	8	17	0.4	75	30	10	40	86	37	123	31	154
5.1.1.7	Cooling System	1.9	103	196	38	0.3	93	28	466	2.1	74	156	50	206	380	554	934	215	1149
5.1.1.8	Align Sys & Instrumentation	3.4	104	352	68	1.0	98	98	380	1.9	78	149	20	169	599	468	1067	482	1549
5.1.1.8.1	Shell Assembly Optical System	1.3	108	140	26	0.3	93	28	130	0.7	86	60	10	70	228	166	394	225	619
5.1.1.8.2	Internal Optical System	1.5	101	152	30	0.3	100	30	155	0.8	78	62	5	67	244	190	434	191	625
5.1.1.8.3	Assy & Instal - Alignment System	0.6	100	60	12	0.4	100	40	95	0.4	68	27	5	32	127	112	239	67	306
5.1.1.9	Shipping	0.1	80	8	2	0.1	80	8	30	0.5	74	37	20	57	53	52	105	22	127
5.1.2	Silicon Detector	3.3	110	364	66	2.0	84	168	3010	4.4	85	372	110	482	904	3186	4090	1227	5317
5.1.3	Detector Electronics	4.5	102	460	90	1.8	98	176	1825	3.0	82	247	40	287	883	1955	2838	1135	3973
5.1.4	Data Aquisition	3.0	100	300	60	0.6	87	52	778	4.5	60	272	30	302	624	868	1492	448	1940
5.1.5	Det Calibration & Test	0.5	120	60	10	1.5	100	150	180	2.0	60	120	20	140	330	210	540	205	745

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Table 10.4

CENTRAL TRACKER SYSTEM COST ESTIMATE

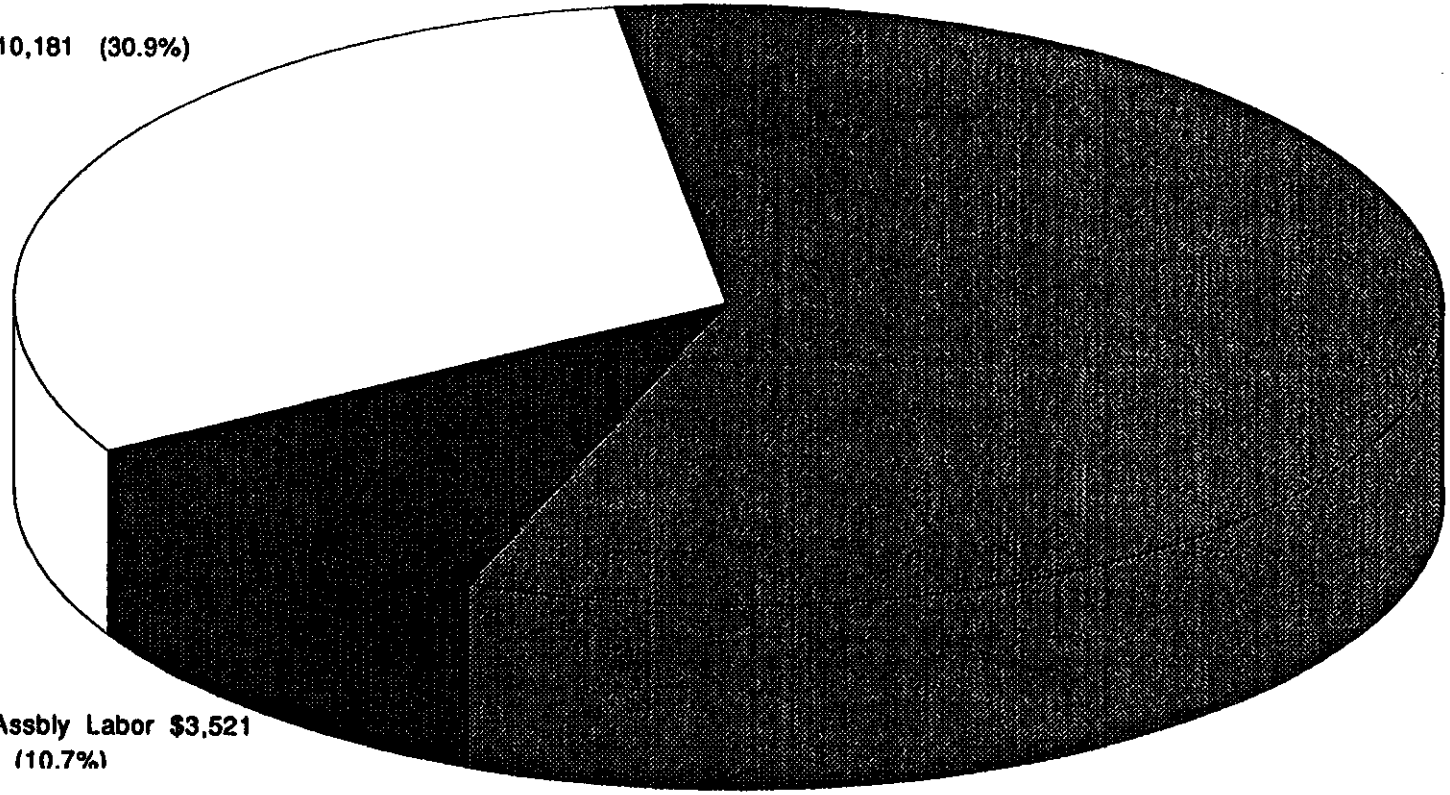
WBS No.	Title	Engineering & Design				Inspection Q/A			Proc/Fab	Installation / Assembly					Totals				
		Labor	Rate	Total	M & S	Labor	Rate	Total	Material	Labor	Rate	Subtot	Mat'l	Total	Labor	Mat'l	Subtot	Conting.	Total K$
5.2	Pad Tracker	20.6	108	2229	1110	5	65	324	8932	21	52	1111	50	1161	3664	10092	13756	5944	19700
5.2.1	Superlayer modules	5.0	93	461		0.2	51	12	2235	14.1	36	502		502	975	2235	3210	1284	4494
5.2.1.1	Barrel modules	2.5	93	228.8		0.1	51.0	6.1	1117	6.9	35.2	242.1		242	477	1117	1594	638	2232
5.2.1.1.1	Level I	0.5	93	45.6		0.0	0.0	0.0	246	1.6	34.0	54.4		54	100	246	346	138	484
5.2.1.1.1.1	Anode wire	0.0	93	5		0.0	0	0	20						5	20	25	10	34
5.2.1.1.1.2	Anode wire supports	0.0	93	5					25						5	25	29	12	41
5.2.1.1.1.3	Anode wire termination stripe	0.0	93	5					2						5	2	7	3	9
5.2.1.1.1.4	Cont cathode plane	0.0	93	5					10						5	10	15	6	20
5.2.1.1.1.5	Gas window	0.0	93	5					8						5	8	13	5	18
5.2.1.1.1.6	Cathode pad plane	0.0	93	5					80						5	80	85	34	118
5.2.1.1.1.7	Graphite epoxy composite hrdbck	0.0	93	5					51						5	51	56	22	78
5.2.1.1.1.8	End plates	0.0	93	5					20						5	20	25	10	34
5.2.1.1.1.9	Gas connectors	0.0	93	5					10						5	10	15	6	20
5.2.1.1.1.10	LV (signal) connectors	0.0	93	5					10						5	10	15	6	20
5.2.1.1.1.11	HV (anode) connectors								5							5	5	2	7
5.2.1.1.1.12	Alignment pins, misc. hard								5							5	5	2	7
5.2.1.1.1.13	Module assembly									1.6	34.0	54		54	54		54	22	76
5.2.1.1.2	Level II	0.5	93	45.6		0.0	0.0	0.0	245.6	1.6	34.0	54.4		54.4	100.0	245.6	345.6	138	484
5.2.1.1.2.1	Anode wire	0.0	93	5		0.0	0	0	20						5	20	25	10	34
5.2.1.1.2.2	Anode wire supports	0.0	93	5					25						5	25	29	12	41
5.2.1.1.2.3	Anode wire terminal stripe	0.0	93	5					2						5	2	7	3	9
5.2.1.1.2.4	Cont cathode plane	0.0	93	5					10						5	10	15	6	20
5.2.1.1.2.5	Gas window	0.0	93	5					8						5	8	13	5	18
5.2.1.1.2.6	Cathode pad plane	0.0	93	5					80						5	80	85	34	118
5.2.1.1.2.7	Graphite epoxy composite hrdbck	0.0	93	5					51						5	51	56	22	78
5.2.1.1.2.8	End plates	0.0	93	5					20						5	20	25	10	34
5.2.1.1.2.9	Gas connectors	0.0	93	5					10						5	10	15	6	20
5.2.1.1.2.10	LV (signal) connectors	0.0	93	5					10						5	10	15	6	20
5.2.1.1.2.11	HV (anode) connectors								5							5	5	2	7
5.2.1.1.2.12	Alignment pins, misc. hard								5							5	5	2	7
5.2.1.1.2.13	Module assembly									1.6	34.0	54		54	54		54	22	76
5.2.1.1.3	Level III	0.5	93	45.6		0.0	0.0	0.0	245.6	1.6	34.0	54.4		54.4	100.0	245.6	345.6	138	484
5.2.1.1.3.1	Anode wire	0.0	93	5		0.0	0	0	20						5	20	25	10	34
5.2.1.1.3.2	Anode wire supports	0.0	93	5					25						5	25	29	12	41
5.2.1.1.3.3	Anode wire terminal stripe	0.0	93	5					2						5	2	7	3	9
5.2.1.1.3.4	Cont cathode plane	0.0	93	5					10						5	10	15	6	20
5.2.1.1.3.5	Gas window	0.0	93	5					8						5	8	13	5	18
5.2.1.1.3.6	Cathode pad plane	0.0	93	5					80						5	80	85	34	118
5.2.1.1.3.7	Graphite epoxy composite hrdbck	0.0	93	5					51						5	51	56	22	78
5.2.1.1.3.8	End plates	0.0	93	5					20						5	20	25	10	34
5.2.1.1.3.9	Gas connectors	0.0	93	5					10						5	10	15	6	20
5.2.1.1.3.10	LV (signal) connectors	0.0	93	5					10						5	10	15	6	20
5.2.1.1.3.11	HV (anode) connectors								5							5	5	2	7

CENTRAL TRACKER SYSTEM COST ESTIMATE

WBS No.	Title	Engineering & Design				Inspection Q/A			Proc/Fab	Installation / Assembly					Totals				
		Labor	Rate	Total	M & S	Labor	Rate	Total	Material	Labor	Rate	Subtot	Mat'l	Total	Labor	Mat'l	Subtot	Conting.	Total K$
5.2.2.1	Barrel section	2.8	93	260.4		0.1	51.0	3.1	218.5	0.6	51.0	31.6		31.6	295.1	218.5	513.6	205.4	719
5.2.2.1.1	End support disk I	1	93	112		0	0.0	0	88	0	51.0	13		13	124	88	212	85	297
5.2.2.1.1.1	Gluing fixtures	0.4	93.0	37		0.0	0	0	38						37	38	75	30	105
5.2.2.1.1.2	Graphite/epoxy fabrication tooling	0.4	93.0	37					50						37	50	87	35	122
5.2.2.1.1.3	Assembly	0.4	93.0	37						0.3	51	13		13	50		50	20	70
5.2.2.1.2	End support disk II	1	93	112		0	0.0	0	85	0	51.0	13		13	124	85	209	84	293
5.2.2.1.2.1	Gluing fixtures	0.4	93.0	37		0.0	0	0	35						37	35	72	29	101
5.2.2.1.2.2	Graphite/epoxy fabrication tooling	0.4	93.0	37					50						37	50	87	35	122
5.2.2.1.2.3	Assembly	0.4	93.0	37						0.3	51	13		13	50		50	20	70
5.2.2.1.3	Module slides	0.2	93.0	19		0.0	51.0	2	40.0	0.1	51.0	4		4	25	40	65	26	91
5.2.2.1.4	Module slide struts	0.2	93.0	19		0.0	51.0	1	5.5	0.0	51.0	2		2	22	6	27	11	38
5.2.2.2	Endcap section	0.8	93	74.4		0.1	51.0	5.1	53.0	0.2	51.0	12		12	92	53	145	58	203
5.2.2.2.1	Inner support ring	0.4	93	37		0.0	51	2	23	0.1	51	4		4	43	23	66	27	93
5.2.2.2.2	Outer support ring	0.2	93	19		0.0	51	2	23	0.1	51	4		4	25	23	48	19	67
5.2.2.2.3	Radial struts	0.2	93	19		0.0	51	1	7	0.1	51	4		4	24	7	31	12	43
5.2.2.3	Integration	0.4	93	37											37		37	15	52
5.2.3	Electronics	9.0	120	1083.6	1060.0	1.0	120.0	120.0	6025.4	1.0	80.0	80.0	50.0	130.0	1284	7135	8419	3873	12292
																		46%	
5.2.3.1	IPC Pad Front End	5.5	120	660	690	1	120	120	3837						780	4527	5307	2441	7748
5.2.3.1.1	Amplifier	0.5	120	59	180				1200						59	1380	1439	662	2101
5.2.3.1.2	AMU	2.1	120	250	290	1.0	120	120	2400						370	2690	3060	1407	4467
5.2.3.1.3	MUX / Readout Chip	1.3	120	155	190				50						155	240	395	182	576
5.2.3.1.4	Readout Link	1.6	120	197	30				187						197	217	414	190	604
5.2.3.2	IPC Wire Front End	1.8	120	212	370				438						212	808	1021	470	1490
5.2.3.2.1	Amplifier / Comp.	0.5	120	59	180				252						59	432	491	226	717
5.2.3.2.2	Digital Pipeline	1.3	120	154	190				168						154	358	512	235	747
5.2.3.2.3	MUX / Readout Chip								4							4	4	2	6
5.2.3.2.4	Readout Link								15							15	15	7	21
5.2.3.3	IPC Front End Hybrid	1.8	120	211					1750	1.0	80	80	50	130	291	1800	2091	962	3053
5.2.4	Gas system & cooling	1.6	137	219.3	50.0	0.0				3.0	120.0	360.0		360.0	579.3	50.0	629.3	188.8	818
5.2.4.1	Gas Distribution System	0.05	93	5		0.0				0.0					5		5	1	6
5.2.4.2	Electronics cooling sys	1.5	140	210	50	0.0				1.5	120	180		180	390	50	440	132	572
5.2.4.3	Monitoring and control	0.1	93.0	4.7		0.0				1.5	120	180.0		180	184.7		184.7	55.4	240
5.2.4.3.1	Gas pressure									1.5	120	180		180	180		180	54	234
5.2.4.3.2	Gas flow rate																		
5.2.4.3.3	Gas temperature	0.1	93	4.7											5		5	1	6
5.2.4.3.4	Electronics temperature																		
5.2.4.3.5	Coolant flow rate																		
5.2.4.3.6	Coolant pressure																		

CENTRAL TRACKER COST ESTIMATE

% of Total Project Cost without Contingency



Note: Contingency $12,562 (38%)

Revised:2/24/92

Figure 10.2

CENTRAL TRACKER SYSTEM COST ESTIMATE

WBS No.	Title	Engineering & Design				Inspection Q/A			Proc/Fab	Installation / Assembly					Totals				
		Labor	Rate	Total	M & S	Labor	Rate	Total	Material	Labor	Rate	Subtot	Mat'l	Total	Labor	Mat'l	Subtot	Conting.	Total K$
5.2.5	Alignment Systems	1.0	93	93					400						93	400	493	197	690
5.2.6	Subsystem Assembly	0.0				0.0				2.5	102.0	125.5		125.5	125.5		125.5	50.2	176
5.2.6.1	Barrel Pad Tracker	0.0				0.0				1.2	51.0	62.7		62.7	62.7		62.7	25.1	88
5.2.6.1.1	Support structure assembly	0.0				0.0				0.3	51	13		13	13		13	5	18
5.2.6.1.2	Level I module installation									0.1	51	6		6	6		6	3	9
5.2.6.1.3	Level II module installation									0.1	51	6		6	6		6	3	9
5.2.6.1.4	Level III module installation									0.1	51	6		6	6		6	3	9
5.2.6.1.5	Level IV module installation									0.1	51	6		6	6		6	3	9
5.2.6.1.6	Gas connection									0.1	51	4		4	4		4	2	6
5.2.6.1.7	HV (anode) connection									0.1	51	4		4	4		4	2	6
5.2.6.1.8	LV (electronics power) connection									0.1	51	4		4	4		4	2	6
5.2.6.1.9	LV (signal) connection									0.1	51	4		4	4		4	2	6
5.2.6.1.10	Cooling connection									0.1	51	4		4	4		4	2	6
5.2.6.1.11	Fiberoptic connection									0.1	51	4		4	4		4	2	6
5.2.6.2	Endcap Pad Tracker	0.0				0.0				1.2	51.0	62.7		62.7	62.7		62.7	25.1	88
5.2.6.2.1	Support structure assembly	0.0				0.0				0.3	51	13		13	13		13	5	18
5.2.6.2.2	Level I module installation									0.1	51	6		6	6		6	3	9
5.2.6.2.3	Level II module installation									0.1	51	6		6	6		6	3	9
5.2.6.2.4	Level III module installation									0.1	51	6		6	6		6	3	9
5.2.6.2.5	Level IV module installation									0.1	51	6		6	6		6	3	9
5.2.6.2.6	Gas connection									0.1	51	4		4	4		4	2	6
5.2.6.2.7	HV (anode) connection									0.1	51	4		4	4		4	2	6
5.2.6.2.8	LV (electronics power) connection									0.1	51	4		4	4		4	2	6
5.2.6.2.9	LV (signal) connection									0.1	51	4		4	4		4	2	6
5.2.6.2.10	Cooling connection									0.1	51	4		4	4		4	2	6
5.2.6.2.11	Fiberoptic connection									0.1	51	4		4	4		4	2	6
5.2.7	Calibration and Testing	0.0				3.6	51.0	183.6		0.0					183.6		183.6	73.4	257
5.2.7.1	Barrel Section	0.0				2	51	92		0					92		92	37	129
5.2.7.1.1	Level I module test	0.0				0.2	51	10							10		10	4	14
5.2.7.1.2	Level II module test					0.2	51	10							10		10	4	14
5.2.7.1.3	Level III module test					0.2	51	10							10		10	4	14
5.2.7.1.4	Level IV module test					0.2	51	10							10		10	4	14
5.2.7.1.5	Barrel subsystem test	0.0				1	51	51		0					51		51	20	71
5.2.7.1.5.1	Gas leak check	0.0				0.2	51	10		0.0					10		10	4	14
5.2.7.1.5.2	HV test					0.2	51	10							10		10	4	14
5.2.7.1.5.3	LV (power) test					0.2	51	10							10		10	4	14
5.2.7.1.5.4	LV (signal) readout test					0.2	51	10							10		10	4	14
5.2.7.1.5.5	Fiberoptic test					0.2	51	10							10		10	4	14
5.2.7.2	Endcap section	0.0				2	51	92		0					92		92	37	129
5.2.7.2.1	Level I module test	0.0				0.2	51	10							10		10	4	14
5.2.7.2.2	Level II module test					0.2	51	10							10		10	4	14
5.2.7.2.3	Level III module test					0.2	51	10							10		10	4	14
5.2.7.2.4	Level IV module test					0.2	51	10							10		10	4	14

CENTRAL TRACKER SYSTEM COST ESTIMATE

WBS No.	Title	Engineering & Design				Inspection Q/A			Proc/Fab	Installation / Assembly					Totals				
		Labor	Rate	Total	M & S	Labor	Rate	Total	Material	Labor	Rate	Subtot	Mat'l	Total	Labor	Mat'l	Subtot	Conting.	Total K$
5.2.7.2.4	Level IV module test					0.2	51	10							10		10	4	14
5.2.7.2.5	Endcap subsystem test	0.0				1	51	51		0					51		51	20	71
5.2.7.2.5.1	Gas leak check	0.0				0.2	51	10		0.0					10		10	4	14
5.2.7.2.5.2	HV test					0.2	51	10							10		10	4	14
5.2.7.2.5.3	LV (power) test					0.2	51	10							10		10	4	14
5.2.7.2.5.4	LV (signal) readout test					0.2	51	10							10		10	4	14
5.2.7.2.5.5	Fiberoptic test					0.2	51	10							10		10	4	14
5.3	Detector Assembly	2.1	111	233	42	0.9	101	91	170	4.0	62	248	70	318	571	282	853	341	1194
																		40%	
5.3.1	Assembly Tooling	1.5	107	161	30	0.2	90	18	120						179	150	329	131	460
5.3.2	Assembly	0.3	120	36	6	0.5	110	55		2.5	60	150	30	180	241	36	277	111	388
5.3.3	Alignment Verification	0.3	120	36	6	0.2	90	18	50	1.5	65	98	40	138	152	96	248	99	347
5.4	Subsystem Installation	1.0	120	120	20	1.0	120	120	230	4.0	60	240	30	270	480	280	760	213	973
																		30%	
5.4.1	Detector Installation	0.5	120	60	10	0.5	120	60	200	2.0	60	120	10	130	240	220	460	129	589
5.4.2	Detector Support Sys Installation	0.5	120	60	10	0.5	120	60	30	2.0	60	120	20	140	240	60	300	84	384
5.5	Subsystem Project Management	0				13	98	1270							1270		1270	508	1778
																		40%	
5.5.1	Silicon Tracker	0.0				5	94	470							470		470	188	658
5.5.1.1	Subsystem Mgt and Admin	0.0				2.0	110	220							220		220	88	308
5.5.1.2	Resource Management					1.0	80	80							80		80	32	112
5.5.1.3	E,S & H Compliance Cntrls					1.0	90	90							90		90	36	126
5.5.1.4	Quality Assurance					1.0	80	80							80		80	32	112
5.5.2	Pad Tracker	0.0				5	94	470							470		470	188	658
5.5.2.1	Subsystem Mgt and Admin	0.0				2.0	110	220							220		220	88	308
5.5.2.2	Resource Management					1.0	80	80							80		80	32	112
5.5.2.3	E,S & H Compliance Cntrls					1.0	90	90							90		90	36	126
5.5.2.4	Quality Assurance					1.0	80	80							80		80	32	112
5.5.3	Integration	0.0				3	110	330							330		330	132	462

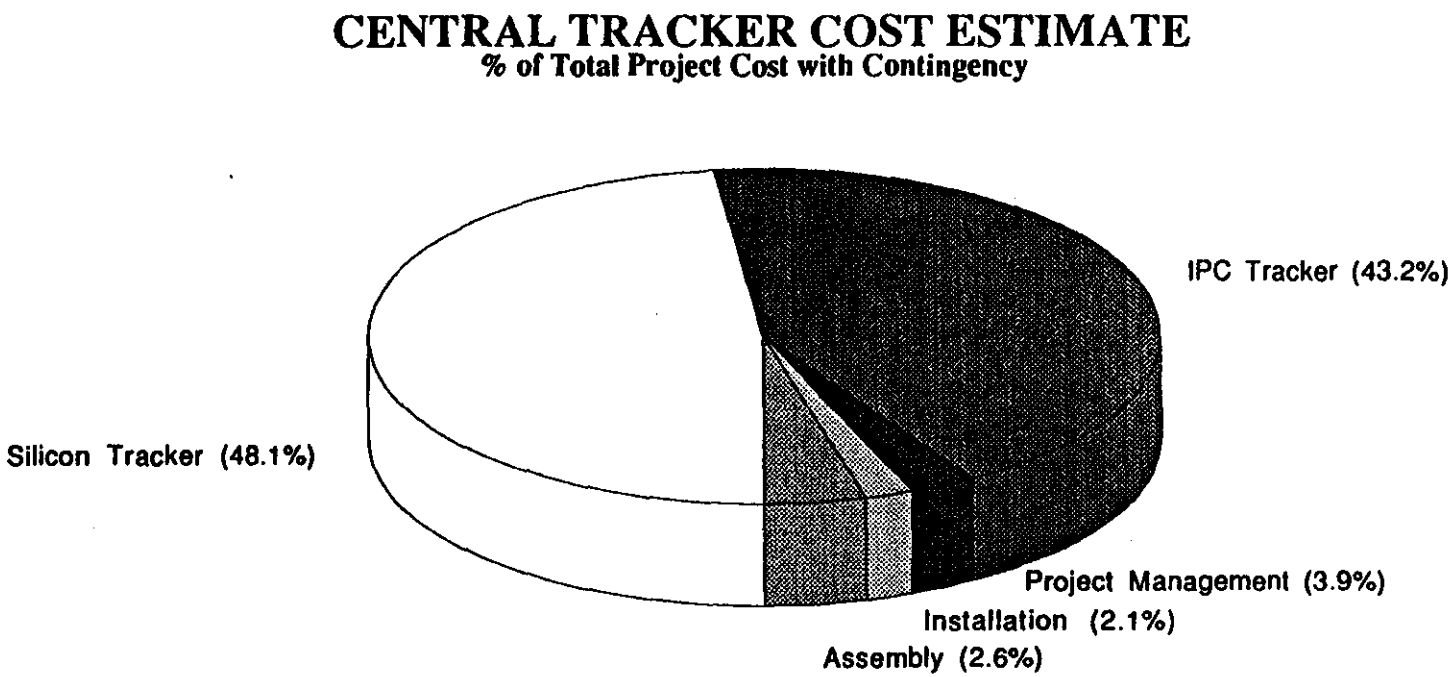

CENTRAL TRACKER COST ESTIMATE
% of Total Project Cost with Contingency
IPC Tracker (43.2%)
Silicon Tracker (48.1%)
Project Management (3.9%)
Installation (2.1%)
Assembly (2.6%)

Figure 10.1