GEM TN-91-40

Gem Tracking Meeting
SSCL

November 5, 1991

Abstract:

Agenda, list of participants and transparencies contributed to the Tracking Meeting held at the SSC Lab on November 6, 1991.

Nov 6, 1991 Tracking

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GEM Central Tracking Meeting
SSCL Director's Conference #1
November 6, 1991, 10:00 am
Agenda

Morning Session:

Current mechanical design of Si + Interpolating Pad Chamber	Ron Barber	30 min
~~Simulations~~	~~Shawn McKee and company~~	~~60+ min~~
LOI Cost and Methodology	Ron Barber	30 min

Afternoon Session:

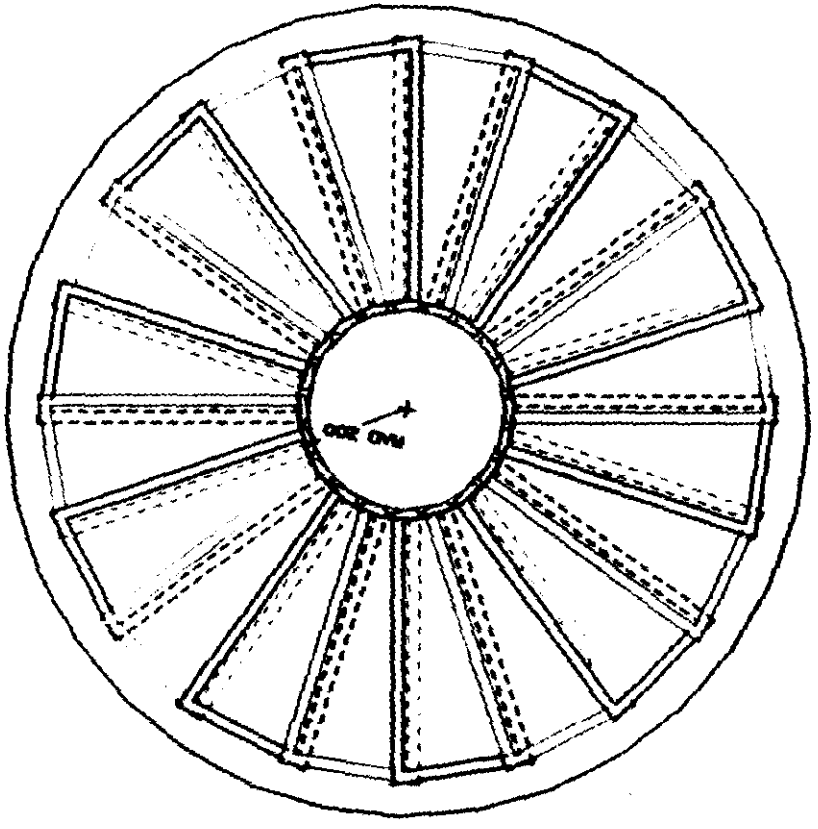
R+D	Gary Sanders	15 min
News from Yale	Charlie Baltay	
Si + Pad Engineering		30 min
Simulations		30 min
Si Pixels	Steve Shapiro	30 min
LOI Tracking Section	Kate Morgan	60+ min

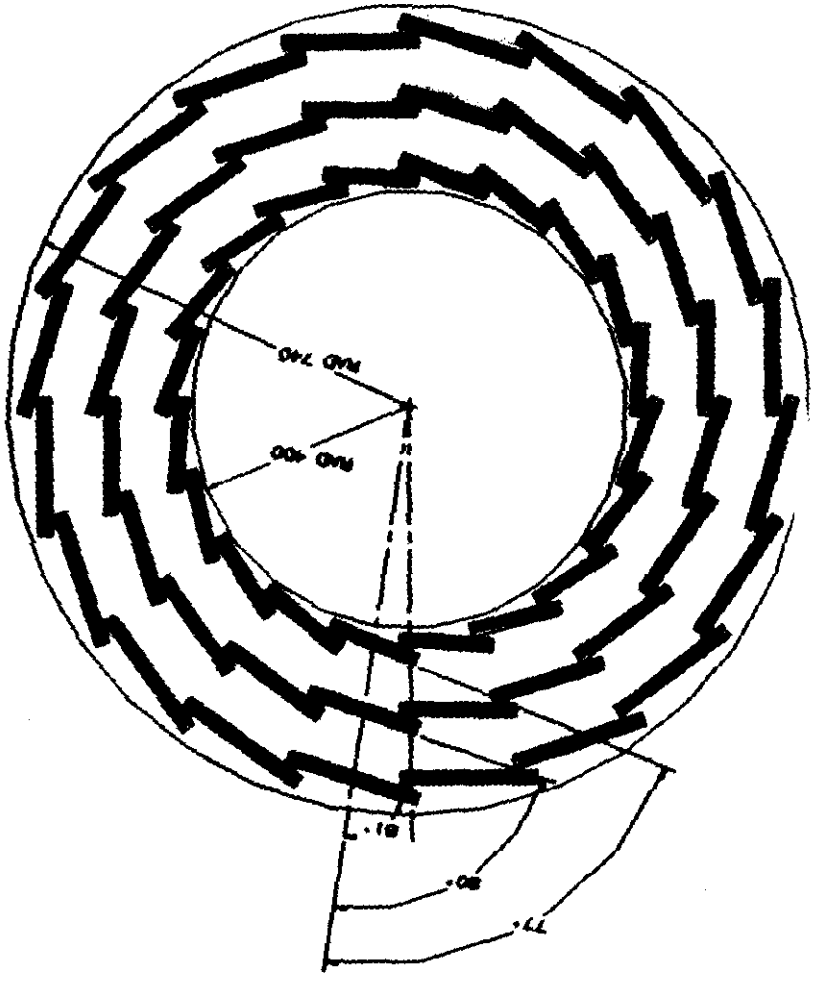
11/6/91-KM

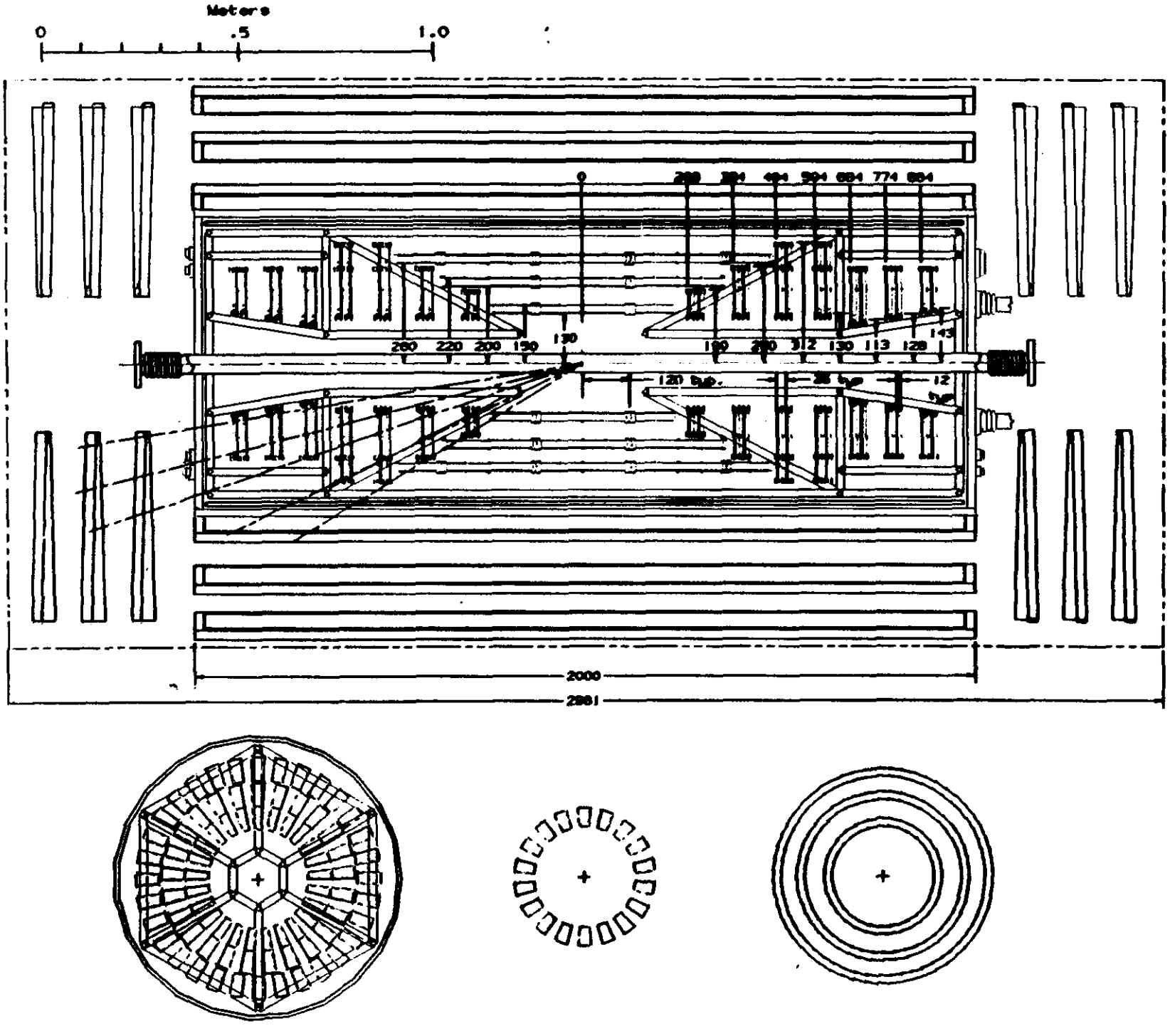
Pad Chamber Design Status

Ron Barber

- Reviewed Design and Specifications
- Identified Major Design Issues
- Proposed Specific Design Concepts
- Identified Design Gaps
- Identified Specific R&D Areas
- Begin defining proposals for R&D






Meters
0
.5
1.0
0
774
260
220
200
150
130
190
312
130
113
128
143
120 typ.
12
2000
2981

Identified Major Design Issues

- Need to generate design specifications
- Stability Requirements ~ 25 microns
- Wire to pad tolerance, +- 1% over 2cm, +-5% over 25 cm.
- Low Radiation Length requirement ~ 1.5% per superlayer
- Electronics Cooling (high heat flux)
- Gas ionization heating
- FWD and Central region alignment
- End Support Structure
- Assembly

Design Proposal

Modular Assembly Of Components

- Chevron Pad and signal traces fabricated into a conductor / Insulator laminate with readout traces/connectors.

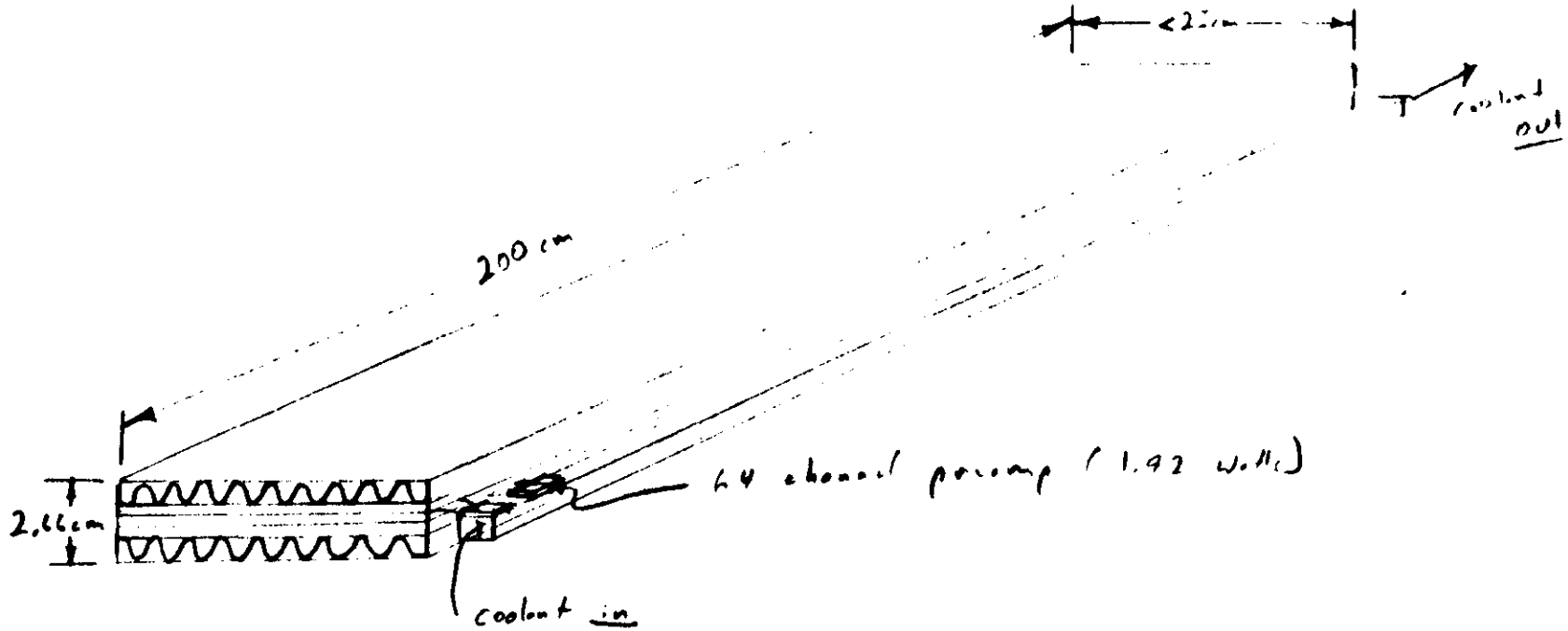
- Pad and trace laminate bonded to graphite epoxy structures.

- Modular chamber construction of o CTE Graphite Epoxy.

- Chamber modules supported at the ends.

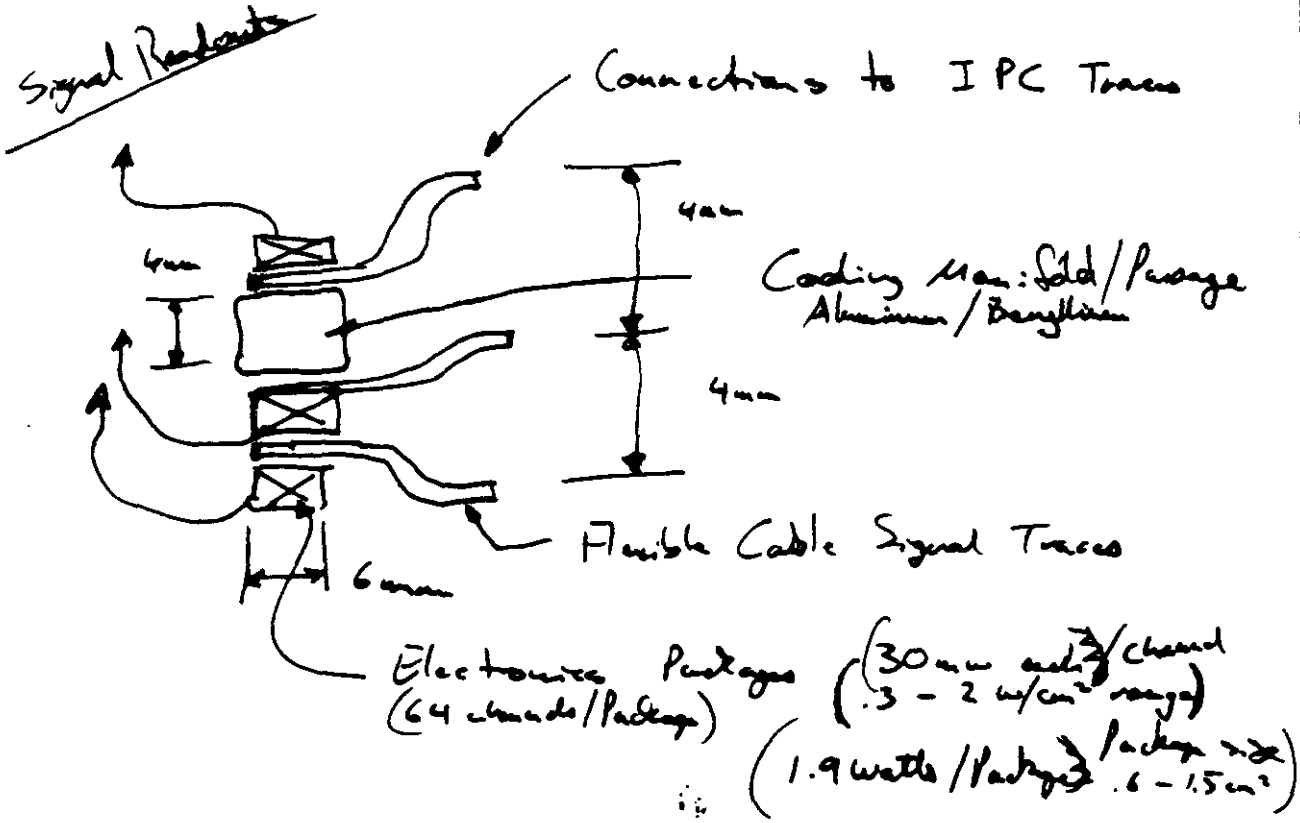
- Single piece cooling manifold with mounted electronics, power supply and signal readouts.

- Self-contained 2 phase room temperature evaporative cooling system.



— Isometric View of Typical Planar IPC Topology —

Cooling Manifold (Electronics)



Manifold lengths - Max 2 m Barrel Region
Min .5m Fwd Region

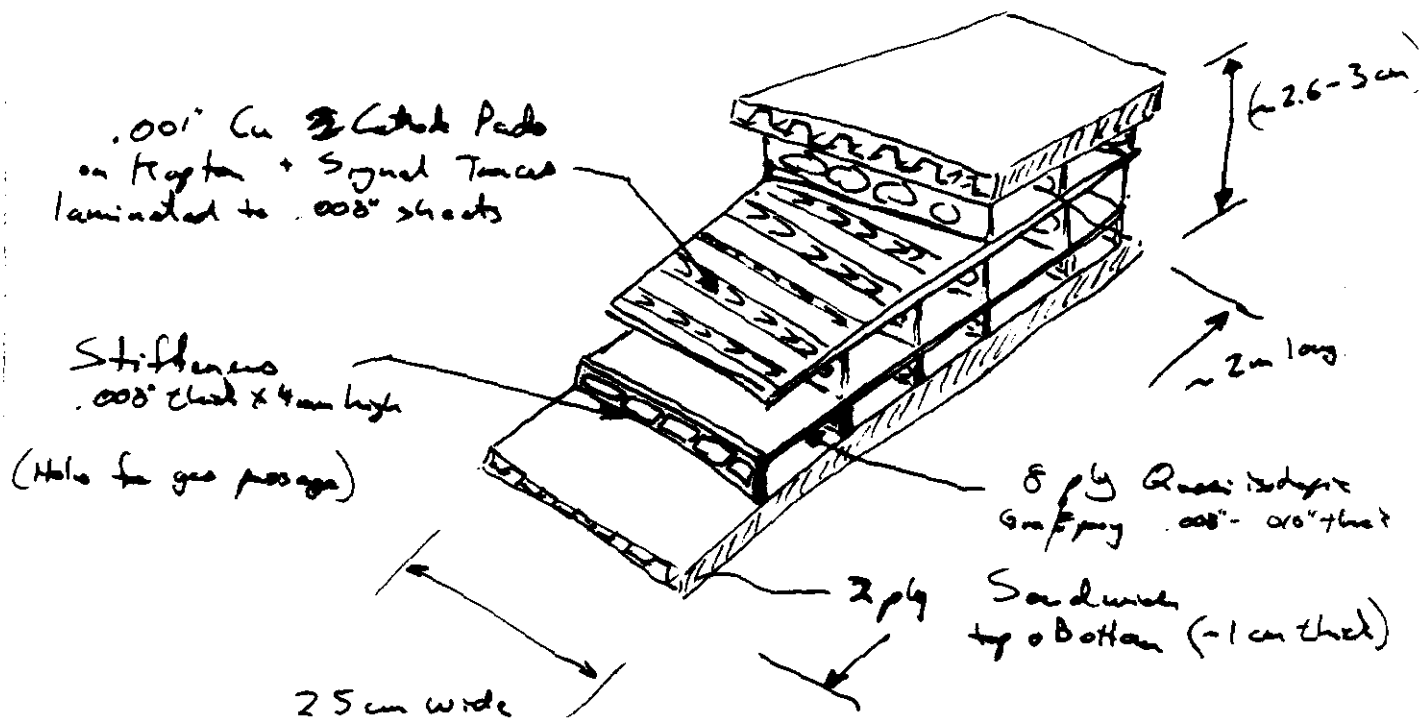
Total Heat load/length Max 50 watts ~~[illegible]~~/Super layer module
(3 layers/Super layer)

Room Temperature Operation

Self Contained 2 phase evaporative System From 11 74°F

Monolithic Module Construction

O CTE Structure



Design Gaps

- Wire bias voltage supply and termination design.

- Gas temperature rise due to ionization.

- Relative alignment and stability of Central and FWD region may lead to an integral support structure.

- Chamber Module stacking interference.

- Forward Region Modules.

- Variation of Pad area and total number of readouts.

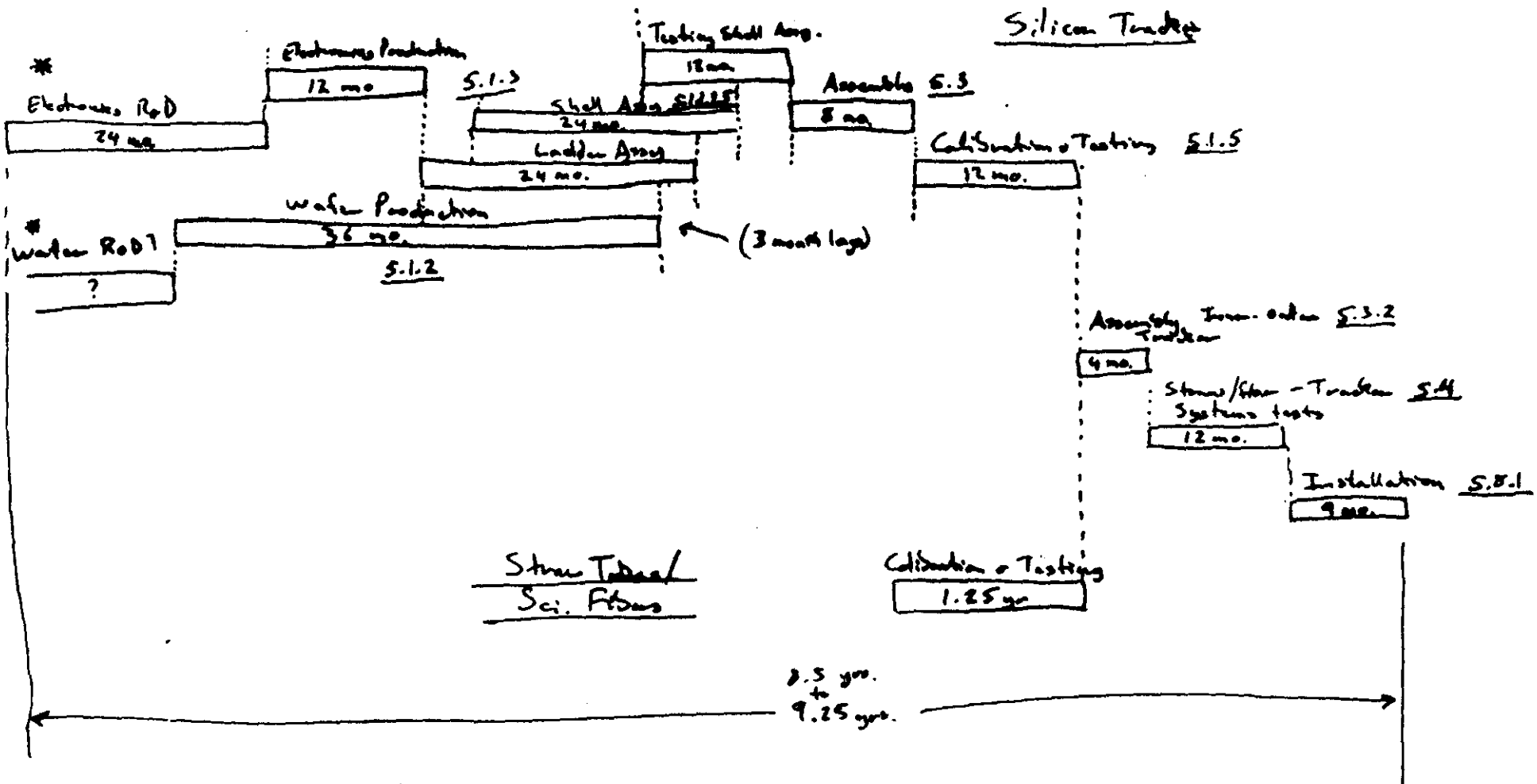
Central Tracker R&D Plan Development

- Description of design requirements
- Description of R&D issues
- Proposal to meet design requirements and address the issues
- Proposal for R&D support in FY 92 (93 & 94) including:

  Manpower

  Hardware costs

  Milestones



Critical Path Items for the Central Tracker

* 2 potential Critical path Items
  - Need to refine all assembly, Calib, testing, Installation Tasks
  - Need to refine Wafer production schedule/feasibility
  - Need to refine Critical Path R&D tasks.

Silicon Tracker R&D

FY 92 Tasks	Manpower	M&S
Electronics		
1. 8 channel wide Semi-custom Analog rad hard circuit design and testing. Heat load specification.	.5	100
2. 8 channel wide Semi-custom Digital rad hard circuit design and testing. Heat load specification.	.5	100
3. Output driver technology review, selection, and prototype design. Heat load specification.	.5	
Mechanical		
1. Silicon Tracker Conceptual design, analysis, and systems studies for the TDR.	1.9	20
2. GEM subsystems Integration (Funded through Integration)	(.75)	(15)
and management.	.25	15
3. Silicon Ladder prototype including: design, analysis, specification, production planning, bonding, thermal analysis.	.8	30
4. In-situ alignment measurement system design and prototype evaluation.	.5	40

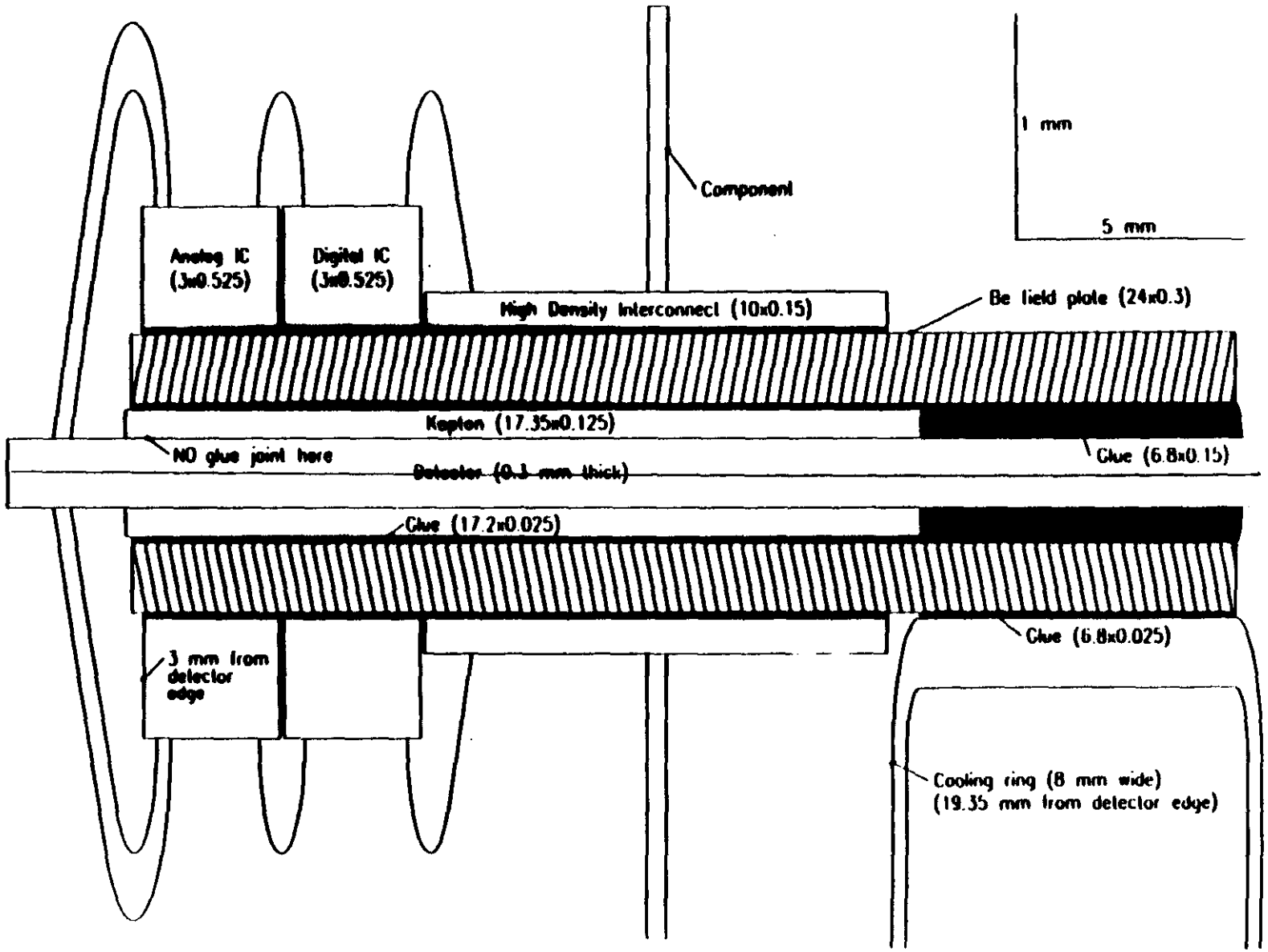
Pad Chamber Engineering and R & D

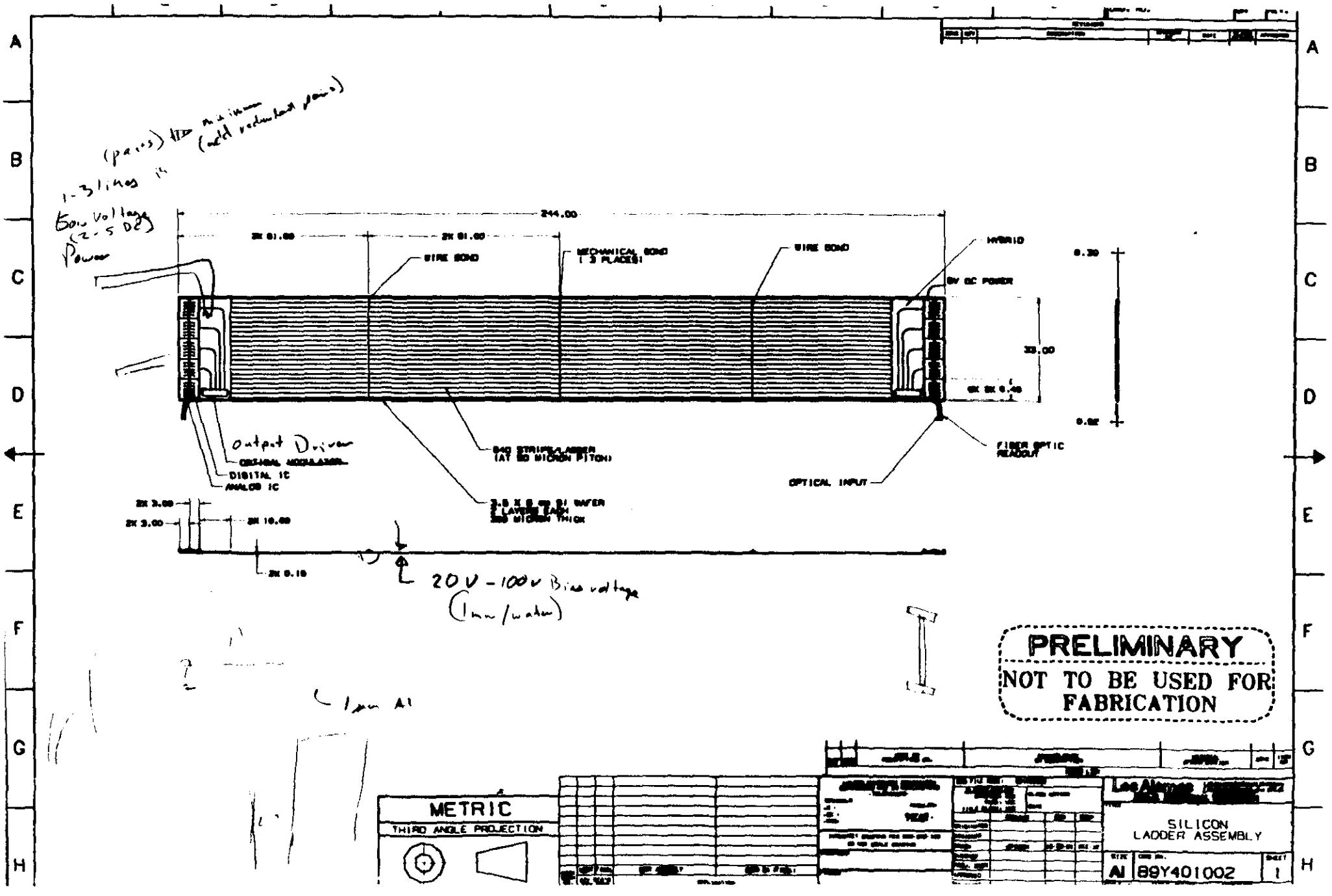
Mechanical		
1. Cooling System design and prototype testing.	.4	20
2. Structural Chamber design, analysis and materials study. (Yale Coordination)	.3	20
Totals	**5.65**	**345**
K$ Total (140 K$/FTE)		**1136**

Silicon Tracker Mechanical R&D

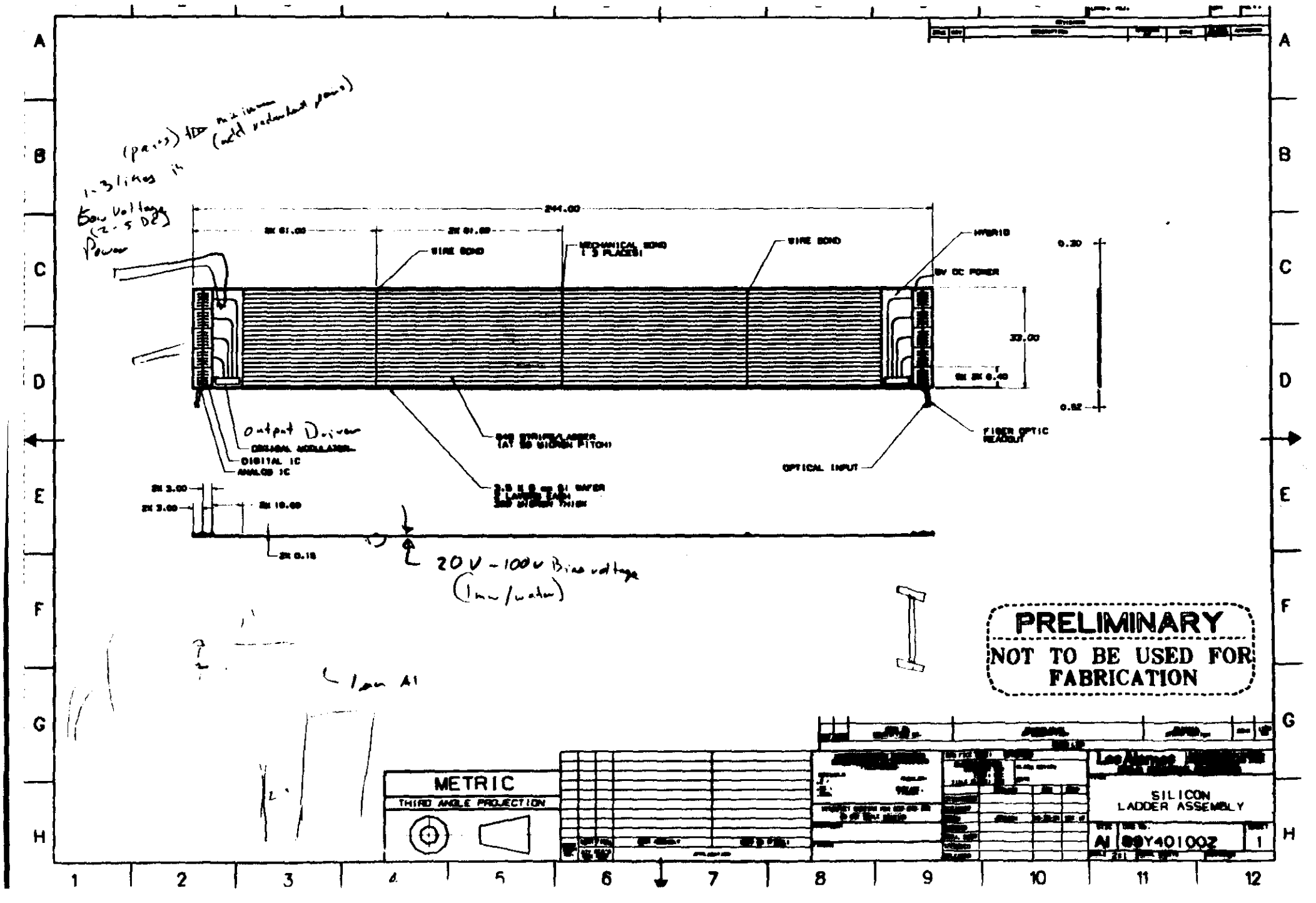
Develop and Test a Silicon Ladder Prototype

- Ladder Structural design and analysis
- Design and specification of Silicon Wafers
- Evaluation of fabrication sources and production planning
- Prototype development
- Develop assembly and bonding process to maintain back to back alignment
- Wafer bonding adhesive tests
- Assembly tooling fabrication and testing
- Prototype Structural Test
- Thermal modeling of multiple heat sources on the wafer
- Thermal mock up and measurement evaluation
- Power input cabling design for electronics and bias voltage
- Signal cable output and strain relief
- Local power distribution and connections.
- Develop Electronics assembly tooling


Analog IC
(3x0.525)
Digital IC
(3x0.525)
Component
1 mm
5 mm
High Density Interconnect (10x0.15)
Be field plate (24x0.3)
Kapton (17.35x0.125)
NO glue joint here
Glue (6.8x0.15)
Detector (0.3 mm thick)
Glue (17.2x0.025)
Glue (6.8x0.025)
3 mm from
detector
edge
Cooling ring (8 mm wide)
(19.35 mm from detector edge)



(pairs) minimum
(add redundant pairs)
1-3 lines
Low Voltage
(2-5 DC)
Power
244.00
2X 61.00
2X 61.00
WIRE BOND
MECHANICAL BOND
(3 PLACES)
WIRE BOND
HYBRID
5V DC POWER
33.00
Output Driver
DIGITAL IC
ANALOG IC
FIBER OPTIC
READOUT
OPTICAL INPUT
2X 3.00
2X 3.00
2X 10.00
2X 0.15
20V - 100V Bias voltage
(1mm/water)
1μm Al
PRELIMINARY
NOT TO BE USED FOR
FABRICATION
METRIC
THIRD ANGLE PROJECTION
SILICON
LADDER ASSEMBLY
A1
89Y401002
1


244.00
WIRE BOND
MECHANICAL BOND
WIRE BOND
HYBRID
5V DC POWER
0.20
32.00
0.52
FIBER OPTIC READOUT
OPTICAL INPUT
Output Driver
DIGITAL IC
ANALOG IC
20V - 100V Bias voltage
PRELIMINARY
NOT TO BE USED FOR FABRICATION
METRIC
THIRD ANGLE PROJECTION
SILICON LADDER ASSEMBLY
A1
1

Silicon Tracker Conceptual Design

Mechanical Design Effort

- Truss Space Frame
- Central and Forward Region subassemblies
    - Wafer Ladder design
    - Global Power Distribution
    - Signal cable readout routing
    - Cooling ring design
    - Kinematic mounts
- Central region support cylinders
- Outer gas enclosure
- End enclosures with signal, power, and cooling system feed thrus
- Detector end supports
- Assembly Alignment systems
- Thermal analysis
- Materials engineering analysis
- Structural and dynamic modal analysis
- Development of fabrication techniques
- Beam Tube design

Ron Barber

CENTRAL TRACKER COST ESTIMATE

BROUGHT TO YOU BY

THE CENTRAL TRACKER DESIGN GROUP

10/28/91

Estimate Status

Completeness

R&D	FY 92 $ Estimated, Preliminary Task list completed FY 93-94 Project Plan Dependent (not done)
Conc/Prelim Engr.	FY 92 $ Estimates and Task list complete (Including allocation from Integration)
Construction	Hardware estimates in good detail, but lack documentation Some Tasks need better definition

Schedule

Construction Plan	Identified Critical Path Items Need to develop Integrated Construction / R&D Plan

Manpower Rates

Engineering and Design

Based on LANL Engineering and Design effort
Included 20K$ / FTE for M&S support

Inspection Q/A

Combination of LANL Engr, Tech and SSCL or Industrial effort
M&S included under Project Management but not well defined

Assembly/ Installation

Extensive use of 55K$ Craft rate to minimize cost
Effort will come from SSCL, Contract, or Industrial effort
Also included some LANL Engineering and Technician Effort
We have <u>not</u> yet itemized SSCL labor support

Level of Definition of Tasks

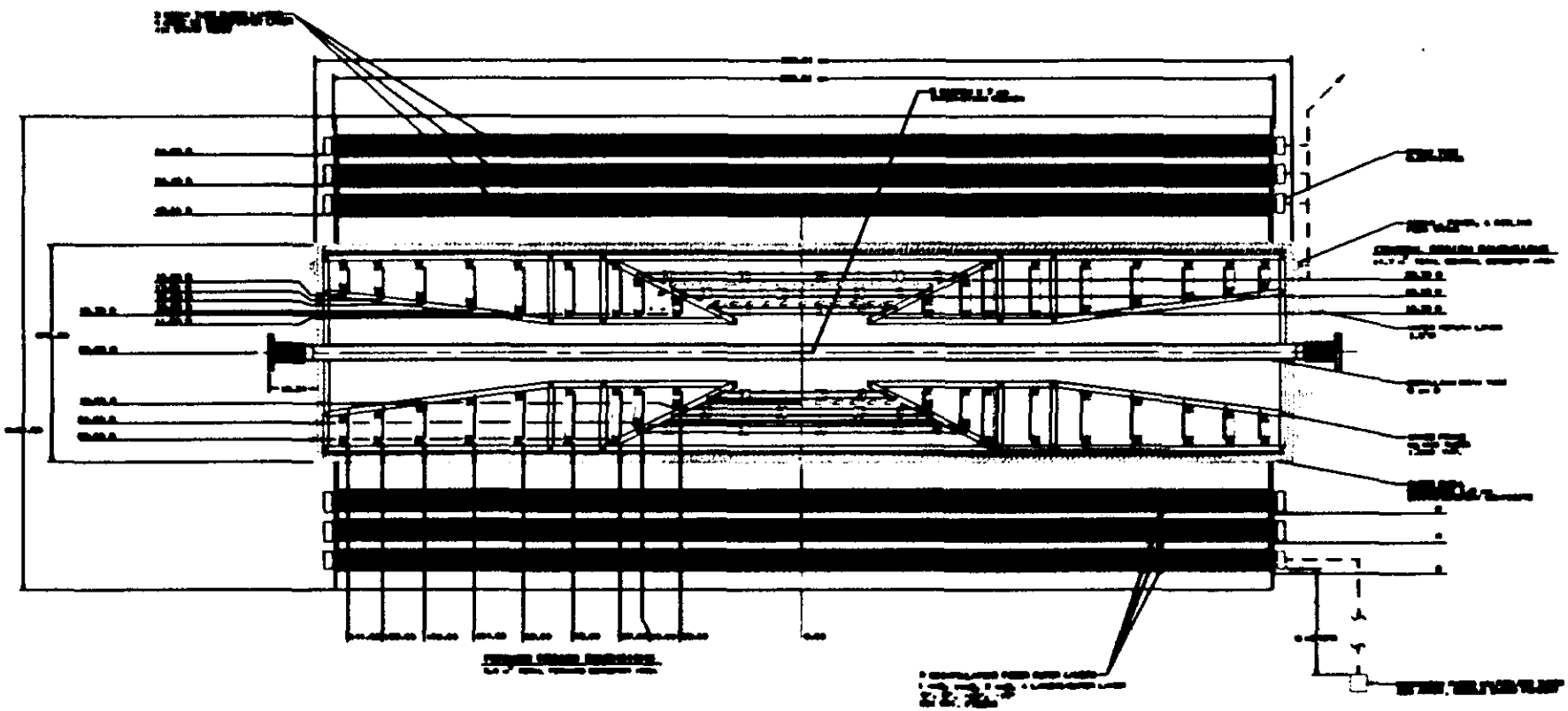
Components

Engineering, Design and Analysis	Well understood when tied to components # of Drawings not estimated
Inspection Q/A	Well understood when tied to components
Assembly / Installation	Need to establish clearer rates for assembly, handling and testing operations

WBS Elements

Systems Testing	Some test are defined in detail others are not Need better breakdown of labor tasks

SILICON TRACKING SYSTEM



ALL DIMENSIONS ARE IN mm

LOS ALAMOS

MECHANICAL AND ELECTRONIC ENGINEERING DIVISION

10-18-91

WBS No.	Title	Engineering & Design			M & S	Inspection Q/A			Proc/Fab	Installation/Assembly					Totals				
		Labor	Rate	Total	Materials	Labor	Rate	Total	Material	Labor	Rate	Subtotal	Material	Total	Labor	Material	Subtotal	Contin.	Total K$
5.2.3.2.6	Central Tracker Subsystem	54.34	110	5984	1944.8	30	102	3060	18757	62.6	66.4304	4158.4	1263	5342.4	13133.4	21954.8	35088.2	12871	47959
5.1	Silicon Tracker	28.89	110.488	3192	577.8	10.4	91.8386	955	12745	26	72.3462	1884.4	520	2411.4	6325.4	13842.8	19878.2	8326.27	28204.47
5.1.1	Mechanical Struc. & Cooling	17.59	114.156	2008	351.8	4.5	90.2222	406	4188	12.1	72.7603	880.4	320	1200.4	3294.4	4859.8	8154.2	2746.51	10900.71
5.1.1.1	Central Region SubAssemblies	3.5	109	380	70	0.8	85	68	852	2.9	69	199.4	90	289.4	647.4	1012	1659.4	532.798	2192.198
5.1.1.1.1	Si Detectors (Ref. only)																		
5.1.1.1.2	Cen. Reg. Cooling Rings	1.2	97	116	24	0.3	80	24	493	0.5	96	48	35	83	188	552	740	296	1036
5.1.1.1.3	Kinematic Mounts	0.5	96	48	10	0.1	80	8	99	0.2	80	16	10	26	72	119	191	48	239
5.1.1.1.4	Assembly Tooling	1.3	123	160	26	0.2	80	16	220	0.5	83	41	25	66.4	217.4	271	488.4	107	596
5.1.1.1.5	Assembly	0.5	112	56	10	0.2	100	20	40	1.7	55	94	20	114	170	70	240	82	322
5.1.1.2	Forward Region Subassemblies	2.5	99	248	50	0.9	93.3333	84	669	2.6	69	180	75	255	512	794	1306	440.8	1746.8
5.1.1.2.1	Si. Detectors (Ref. only)																		
5.1.1.2.2	Fwd. Reg. Cooling Rings	1	96	96	20	0.5	96	48	424	0.4	90	36	35	71	180	479	659	264	923
5.1.1.2.3	Kinematic Mounts	0.5	96	48	10	0.1	80	8	150	0.2	80	16	10	26	72	170	242	61	303
5.1.1.2.4	Assembly Tooling	0.5	96	48	10	0.1	80	8	75	0.3	80	24	10	34	80	95	175	39	214
5.1.1.2.5	Assembly	0.5	112	56	10	0.2	100	20	20	1.7	61	104	20	124	180	50	230	78	308
5.1.1.3	Central Region Support Cylinders	1.3	105	136	26	0.3	93.3333	28	380	0.4	75	30	10	40	194	416	610	196.33	806.33
5.1.1.3.1	Composite Cylinders	0.8	105	84	16	0.2	100	20	348	0.2	70	14	5	19	118	369	487	166	653
5.1.1.3.2	Kinematic Mounts	0.5	104	52	10	0.1	80	8	32	0.2	80	16	5	21	76	47	123	31	154
5.1.1.4	Space Frame	1	100	100	20	0.3	80	24	542	0.8	81	65	10	75	189	572	761	304	1065
5.1.1.5	Gas Enclosure	3.4	108.235	368	68	0.6	86.6667	52	642	0.8	71.25	57	40	97	477	750	1227	426.3	1653.3
5.1.1.5.1	Outer Enclosure	2	110	220	40	0.4	90	36	430	0.4	75	30	15	45	286	485	771	262	1033
5.1.1.5.2	Inner Enclosure	0.8	110	88	16	0.1	80	8	135	0.2	68	14	10	23.5	109.5	161	270.5	97	368
5.1.1.5.3	End Enclosures	0.6	100	60	12	0.1	80	8	77	0.2	68	14	15	28.5	81.5	104	185.5	67	252
5.1.1.6	Detector Supports	1.1	98	108	22	0.2	80	16	102	0.5	76	38	15	53	162	139	301	105.51	406.51
5.1.1.6.1	End Supports	0.6	100	60	12	0.1	80	8	85	0.1	80	8	5	13	76	102	178	75	253
5.1.1.6.2	Kinematic Mounts	0.5	96	48	10	0.1	80	8	17	0.4	75	30	10	40	86	37	123	31	154
5.1.1.7	Cooling System	0.19	1032	196	3.8	0.3	93.3333	28	466	2.1	74	156	50	206	380	519.8	899.8	216	1116
5.1.1.7.1	Detector Hall Systems				0														
5.1.1.7.2	Surface Systems				0														
5.1.1.8	Alignment System and Instrumenta	4.4	104	456	88	1	98	98	586	1.9	78	149	20	169	703	613	1316	502.22	1818.22
5.1.1.8.1	Shell Assy Optical System	2.3	106	244	46	0.3	93.3333	28	255	0.7	86	60	10	70	332	311	643	244	887
5.1.1.8.2	Internal Optical System	1.5	101	152	30	0.3	100	30	155	0.8	78	62	5	67	244	190	434	191	625
5.1.1.8.3	Assy and Installation Alignment Sy	0.6	100	60	12	0.4	100	40	95	0.4	68	27	5	32	127	112	239	67	306
5.1.1.9	Shipping	0.2	80	16	4	0.1	80	8	30	0.1	60	6	10	16	30	44	74	22	96
5.1.2	Silicon Detector	3.3	110	364	66	2	84	168	4668	4.4	85	372	110	482	904	4844	5748	2874	8622

5.1.3	Detector Electronics	4.5	102	460	90	1.8	98	176	2604	3	82	247	40	287	883	2734	3617	1664	5281
5.1.4	Data Acquisition	3	100	300	60	0.6	87	52	1105	4.5	60	272	30	302	624	1195	1819	837	2656
5.1.5	Detector Calibration and Testing	0.5	120	60	10	1.5	100	150	180	2	60	120	20	140	330	210	540	205	745
5.2	Straw Tube/ Sci Fiber Detector	21	109	2290	420	4.2	110	462	5472	28	60	1380	513	1893	4132	6405	10537	3161	13698
5.2.1	Straw Tube Detector Subsystem	11	109	1200	220	2.2	110	242	2677	15.9	60	954	293	1247	2396	3190	5586	1676	7262
5.2.1.1	Straw Tube Mechanical Assembly																		
5.2.1.1.1	Support Cylinders																		
5.2.1.1.2	Manifold Ends																		
5.2.1.1.3	Straw Tubes																		
5.2.1.1.3.1	Module Assy Tooling																		
5.2.1.1.3.2	Straws																		
5.2.1.1.3.3	Straw End Plates																		
5.2.1.1.4	Anode																		
5.2.1.1.4.1	Anode Wire																		
5.2.1.1.4.2	Wire Tue Interface																		
5.2.1.1.5	Assembly Tooling																		
5.2.1.1.6	Assembly																		
5.2.1.1.7	Gas Suppy System																		
5.2.1.1.8	Electronics Cooling																		
5.2.1.3	Straw Tube Electronics																		
5.2.1.3.1	Front End Electronics																		
5.2.1.3.2	Signal Readout																		
5.2.2	Scintillating Fiber Subsystem	8	110	880	160	1.5	110	165	2720	5.1	60	306	200	506	1351	3080	4431	1329	5760
5.2.2.1	Sci Fiber Mech System																		
5.2.2.1.1	Support Cylinder																		
5.2.2.1.2	Scintillating Fiber																		
5.2.2.1.2.1	Scintillating Fiber Ribbons																		
5.2.2.1.2.2	FO Pigtail																		
5.2.2.1.2.3	FO Terminator																		
5.2.2.1.3	Assembly Tooling																		
5.2.2.1.4	Assembly																		
5.2.2.2	Sci Fiber Readouts																		
5.2.2.2.1	Photo Multiplier Tubes																		
5.2.2.2.2	Data Acquisition System																		
5.2.2.2.3	Assembly Installation																		
5.2.2.2.4	Calibration and Testing																		
5.2.3	Detector Calibration and Testing	2	105	210	40	0.5	110	55	75	2	60	120	20	140	385	135	520	156	676
5.3	Detector Assembly / Integration	2.1	110	232	42	0.9	101	91	170	4	62	248	70	318	571	282	863	241	1194
5.3.1	Assembly Tooling	1.5	107	160	30	0.2	90	18	120			0		0	178	150	328	131	459
5.3.2	Assembly	0.3	120	36	6	0.5	110	55	0	2.5	60	150	30	180	241	36	277	111	388
5.3.3	Alignment Verification	0.3	120	36	6	0.2	90	18	50	1.5	65	98	40	138	152	96	248	99	347

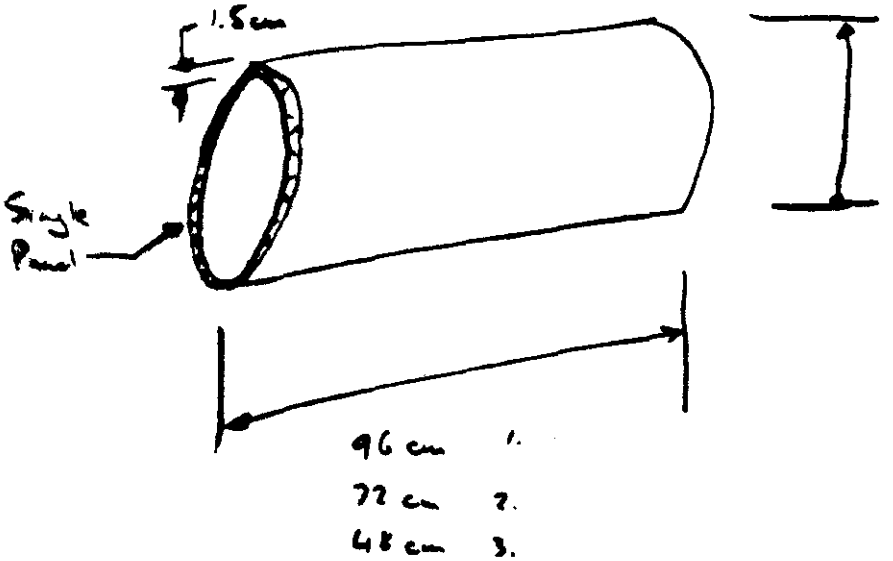
5.4	Detector Calibration/Testing	1.25	120	150	25	3.5	90	225	140	6.5	60	300	130	510	765	285	1050	315	1365
5.4.1	Mechanical Systems Tests	0.25	120	30	5	1	90	90	30	2	60	120	50	170	240	85	325	98	423
5.4.2	Electrical Systems Tests	0.5	120	60	10	1	90	90	60	2.5	60	150	30	180	300	100	400	120	520
5.4.3	Detector Calibrations	0.5	120	60	10	0.5	90	45	50	2	60	120	40	160	225	100	325	98	423
5.8	Subsystems Installation	1	240	120	20	1	240	120	230	3	120	180	30	210	420	290	709	210	919
5.8.1	Detector Installation	0.5	120	60	10	0.5	120	60	200	1.5	60	90	10	100	210	220	430	129	559
5.8.2	Detector Support Systems Installati	0.5	120	60	10	0.5	120	60	30	1.5	60	90	20	110	210	60	270	81	351
5.9	Subsystems Project Management	0		0	860	11	110	1210	0	0	0	0	0	0	1210	860	2070	518	2588
5.9.1	Proj. Management and Administration				150	4	130	520				0		0	520	150	670	168	838
5.9.2	Resource Management				450	1	80	80				0		0	80	450	530	133	663
5.9.3	HS&H Compliance Controls				50	1	90	90				0		0	90	50	140	35	175
5.9.4	Quality Assurance				50	1	80	80				0		0	80	50	130	33	163
5.9.5	Subsystems Integration				160	4	110	440				0		0	440	160	600	150	750

1.3.1 Composite Cylinders [redacted] WORK SHEET
meters (weight, length, area, [redacted]) 3 Cylinders

Date 26-Oct
Prep. by R Barber

Task	[redacted]	[redacted]	[redacted]	[redacted]	Total PY		Cost	Mat Disc	Fab & Ext	Tot Mat		Total Cost
Rates	[redacted]	[redacted]	[redacted]	[redacted]	PY		K$	k$	k$	K$		k$
							0			0		0
Design	0.[redacted]	0.1					32			0		32
Analysis	0.3						36			0		36
Detailing		0.2					16			0		16
							0			0		0
							0			0		0
							0			0		0
E & D Total	0.5	0.3	0	0	0.8		84	0	0	0		84
Inspection QA							0			0		0
	0.1		0.1				20			0		20
							0			0		0
Materials							0			0		0
Cylinder 1							0	6		6		6
Cylinder 2							0	3.3		3.3		3.3
Cylinder 3							0	0.8		0.8		0.8
							0			0		0
Testing							0			0		0
Cylinder 1							0		130	130		130
Cylinder 2							0		105	105		105
Cylinder 3							0		~~[illegible]~~	78		78
							0			0		0
Fabrication							0		50	50		50
							0			0 348		0
[redacted]							0		5	5		5
[redacted] Total	0.1	0	0.1	0	0.2		20	10.1	368	~~[illegible]~~ 378.1		398.1
							0			0		0
							0			0		0
							0			0		0
							0			0		0
Cylinder prep for Kinematic mounts							0			0		0
			0.1	0.1			13.5			0		13.5
							0			0		0
							0			0		0
Sealing							0		5	5		5
							0			0		0
							0			0		0
							0			0		0
							0			0		0
							0			0		0
[redacted]							0			0		0
[redacted] Total	0	0	0.1	0.1	0.2		13.5	0	5	5		18.5
[redacted]	0.6	0.3	0.2	0.1	1.2	0	117.5	10.1	373	383.1	0	[redacted]
Contingency							0			0		0
[redacted]							0			0		[redacted]
[redacted]							0			0		[redacted]
[redacted]							0			0		[redacted]
[redacted]							0			0		0
Cont. Total	0	0	0	0	0	0	0	0	0	0	0	[redacted]
[redacted]	0.6	0.3	0.2	0.1	1.2		117.5	10.1	373	383.1		[redacted]

5.1.1.3 Central Region Support Cylinders



60 cm ⌀ 1.
48 cm ⌀ 2.
[illegible] cm ⌀ 3.

	1.	2.	3
Vol = π D L t (cm³)	27.1 x 10³	16.3 x 10³	3.8 x 10³
Fiber Vol ~ 2% Vol (cm³)	542	326	76
Fiber wt = Fiber Vol (1.8 g/cm³) x 2.2 lbs/kgm.	2.2 (lbs)	1.3	.3
Material cost = fib wt (2 K$/lb) + 30% waste	6 (K$)	3.3	.8

Tooling Costs

Inner Skin	30	20	10
Outer Skin	30	20	10
Waffle	50	50	20
Bonding tooling	20	15	7
	110	105	[illegible]
Assy, Insp, Machining	30	15	5
Sub Totals K$	166	123	64
Structure Cost/lb. K$/lb (Alum costs 85 K$/lb)	75	93	213

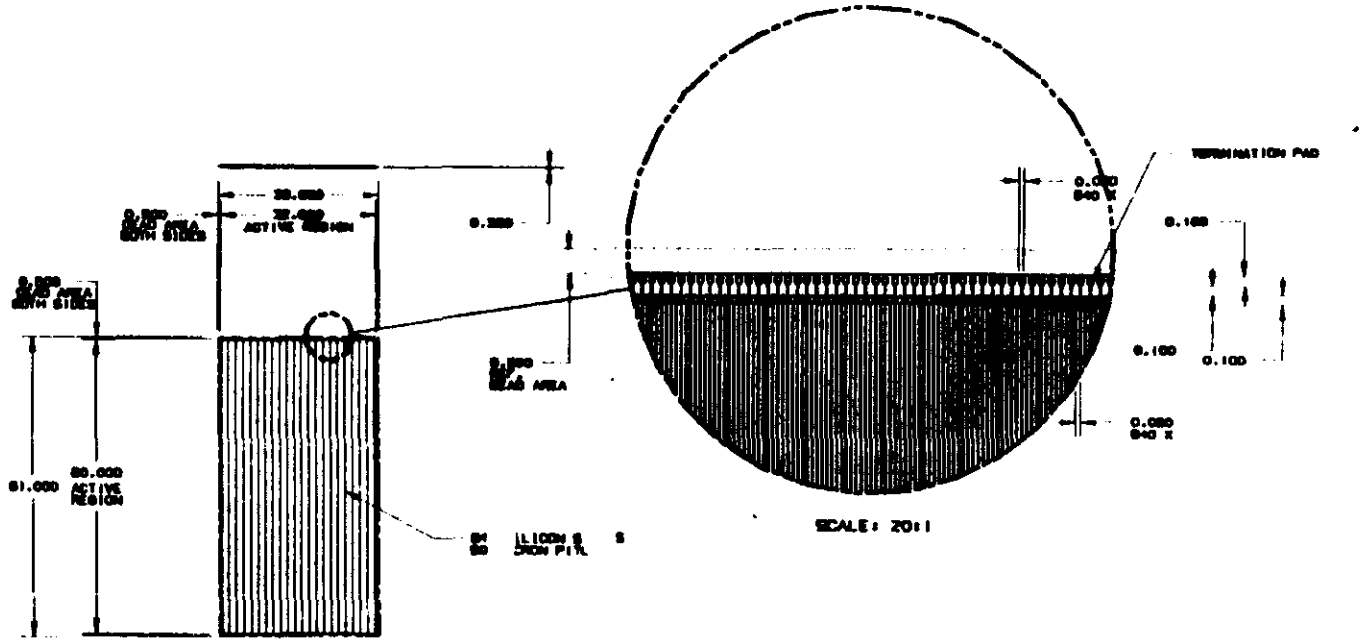
1.2 Silicon Ladder Assembl COMPONENT WORK SHEET

ımeters (weight, length, area, number) 22.27 sq m. =Total fwd & bwd Si area =2x10.14 Date 26-Oct

= 12984 # Wafers 3246 # Ladders Prep. by D Lee

TASK CENTRAL TRACKER CONSTRUCTION

	Engr.	Design	Tech.	Crafts	Total PY		Cost	Mat Proc	Fab & Exp	Tot Mat		Total Comp
Rates	120	80	80	55	PY		K$	K$	K$	K$		K$
							0			0		0
Design	1.5	0.3					204			0		204
Analysis	1						120			0		120
Detailing		0.5					40			0		40
							0			0		0
							0			0		0
							0			0		0
F & D Total	2.5	0.8	0	0	3.3		364	0	0	0		364
	0.5		1	0.5			167.5			0		167.5
							0			0		0
Materials							0			0		0
200 K$/sq M x # sq Meters							0			0		0
200							0	4454		4454		4454
Fabrication							0			0		0
Wire Bond .5 hr /Ladder side x K$ .060/hr # Ladders x 2 sides							0	194.76		194.76		194.76
0.03							0			0		0
Graphite Ribs							0		10	10		10
							0			0		0
Tooling							0			0		0
							0			0		0
							0			0		0
							0			0		0
Inspection							0			0		0
Travel-10							0		10	10		10
Total	0.5	0	1	0.5	2		167.5	4648.76	20	4668.76		4836.26
Wafer Bonding (.5 hr/ladder x 2 tech)							0			0		0
	0.2		2				168.267			0		168.267
Electronic Bonding (.5 hrs. / ladder x 2 tech)							0			0		0
	0.2		2				168.267			0		168.267
Electrical Burnout (8 hr automated system)							0			0		0
	0.1		0.3				36			0		36
							0			0		0
							0			0		0
Wafer Assy Tooling							0		50	50		50
							0			0		0
							0			0		0
Automated Burnout and Calibration							0	50		50		50
							0			0		0
							0			0		0
Travel-10							0		10	10		10
Subassy Tot	0.5	0	3.9067	0	4.4067		372.533	50	60	110		482.533
Subtotal	3.5	0.8	4.9067	0.5	9.7067	0	904.033	4698.76	80	4778.76	0	5682.79
Contingency							0			0		0
10							0			0		1704.84
6							0			0		681.935
8							0			0		454.623
50%							0			0		0
Cont Total	3.5	0.8	4.9067	0.5	9.7067		0	0	0	0	0	2841.4
TOTAL	7	1.6	9.8133	1	19.413		904.033	4698.76	80	4778.76		8524.19
										0		



TYPICAL SILICON WAFER

PRELIMINARY

NOT TO BE USED FOR FABRICATION

METRIC

THIRD ANGLE PROJECTION

Los Alamos

GEM DETECTOR
TYPICAL SILICON WAFER
WITH STRIPS
CONFIGURATION

A1 | 69Y401000 | 1

.3 **Detector Electronics** **COMPONENT WORK SHEET**

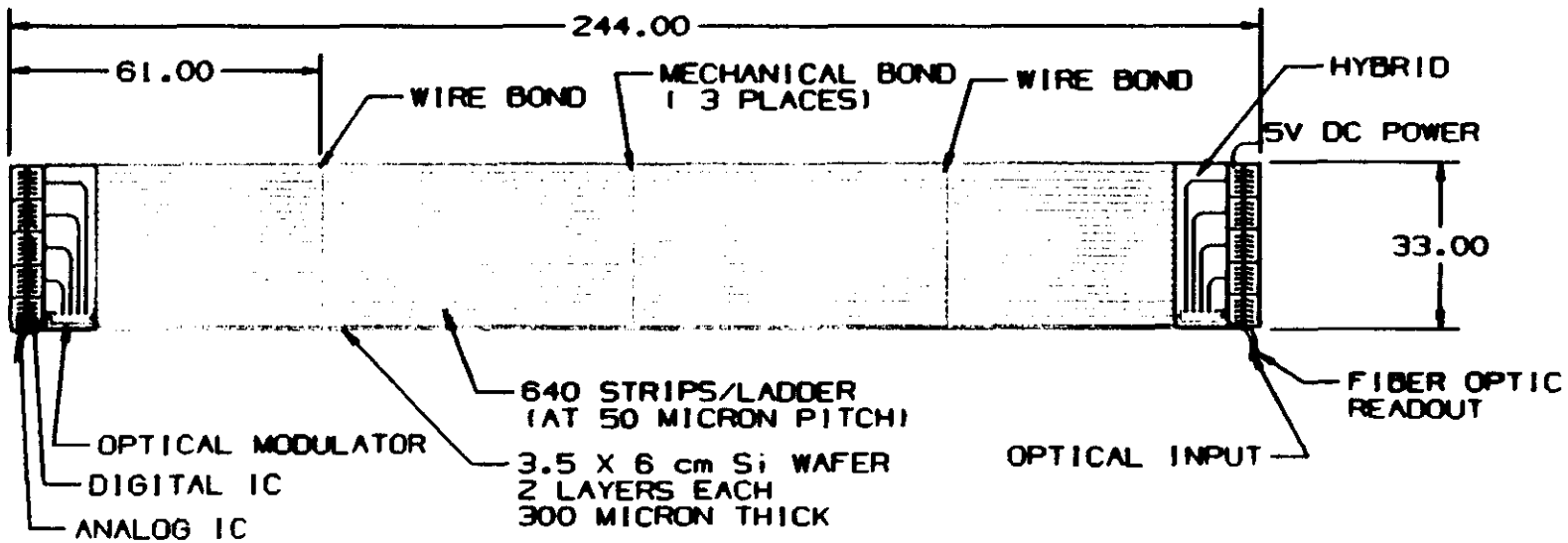
ameters (weight, length, area, number) 6877 # Readouts (50 µm) 4.4 # M Strips

Date 26-Oct
Prep. by D Lee

TASK CENTRAL TRACKER CONSTRUCTION

	Engr.	Design	Tech.	Crafts	Total PY		Cost	Mat Proc	Fab & Exp	Tot Mat		Total Comp
Rates	120	80	80	55	PY		K$	K$	K$	K$		K$
							0			0		0
Design	2.5	2					460			0		460
Analysis							0			0		0
Detailing							0			0		0
							0			0		0
							0			0		0
							0			0		0
E & D Total	2.5	2	0	0	4.5		460	0	0	0		460
Materials	0.8		1.8				240			0		240
# Strips x (Ampl $.25 + Dig Elec $.27)							0	2288		2288		2288
0.52							0			0		0
							0			0		0
Wire Bending .5 hr/ Readout x .06 K$/hr x # Readouts							0			0		0
0.03							0	206.31		206.31		206.31
							0			0		0
							0			0		0
							0			0		0
5K$/KW power Supply x 10 KW							0	50		50		50
							0			0		0
Power Distribution System							0	50		50		50
Testing							0			0		0
							0			0		0
Inspection							0			0		0
Travel -10							0		10	10		10
Total	0.8	0	1.8	0	2.6		240	2594.31	10	2604.31		2844.31
Prototype Assembly							0			0		0
							0			0		0
							0			0		0
							0			0		0
							0			0		0
Power Supply Installation							0			0		0
			0.5				40			0		40
							0			0		0
Subassembly							0			0		0
							0			0		0
Power Distribution Installation							0			0		0
	0.5		1.5	0.5			207.5			0		207.5
Testing Equipment							0	30		30		30
							0			0		0
Travel-10							0		10	10		10
Subassy Tot	0.5	0	2	0.5	3		247.5	30	10	40		287.5
Subtotal	3.8	2	3.8	0.5	10.1	0	947.5	2624.31	20	2644.31	0	3591.81
Contingency							0			0		0
10							0			0		1077.54
4							0			0		287.345
8							0			0		287.345
40%							0			0		0
Cont Total	0	0	0	0	0	0	0	0	0	0	0	1652.23
TOTAL	3.8	2	3.8	0.5	10.1		947.5	2624.31	20	2644.31		5244.04

SILICON LADDER ASSEMBLY



LOS ALAMOS

MEE-12
MECHANICAL AND ELECTRONIC
ENGINEERING DIVISION

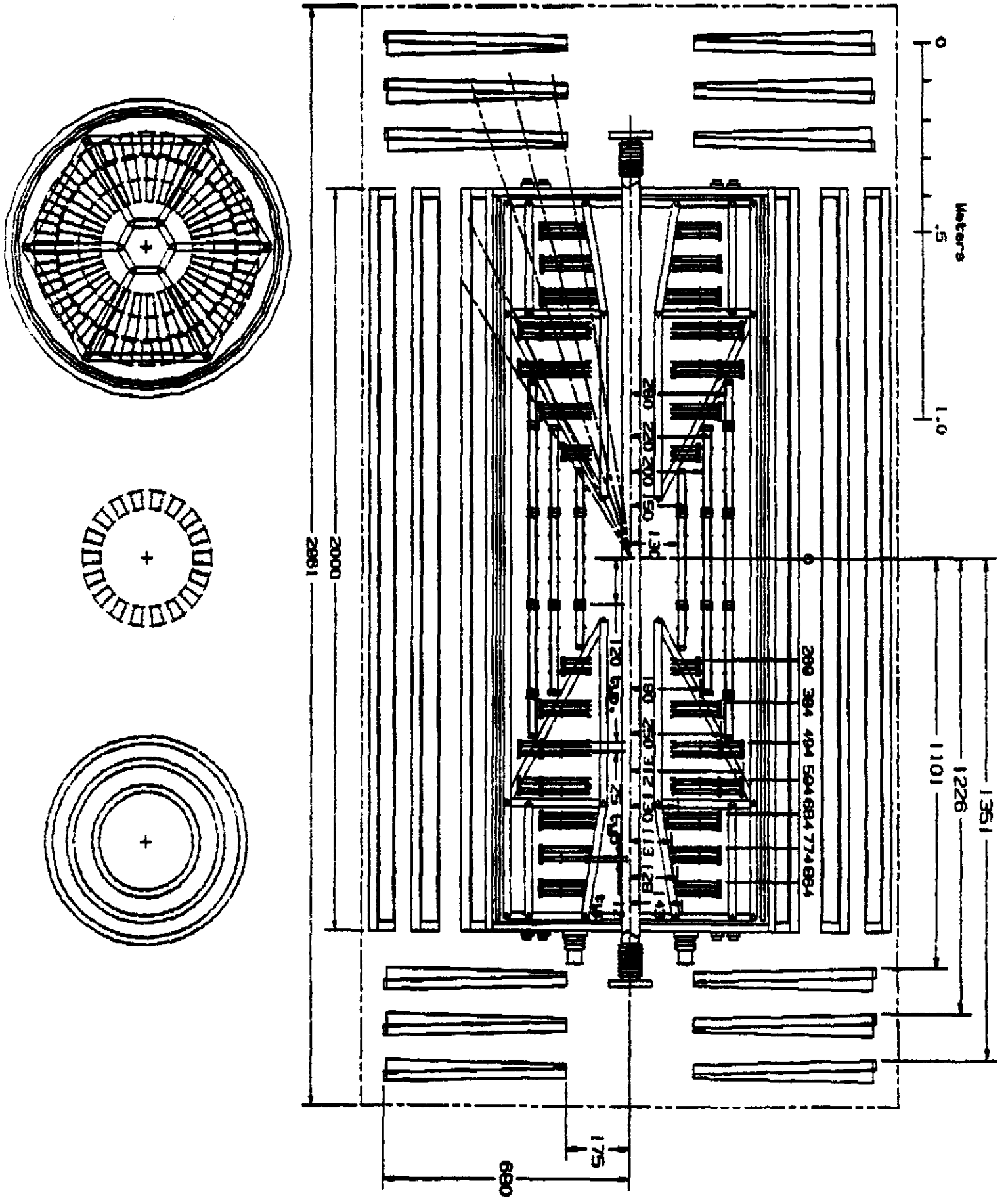
10-25-01

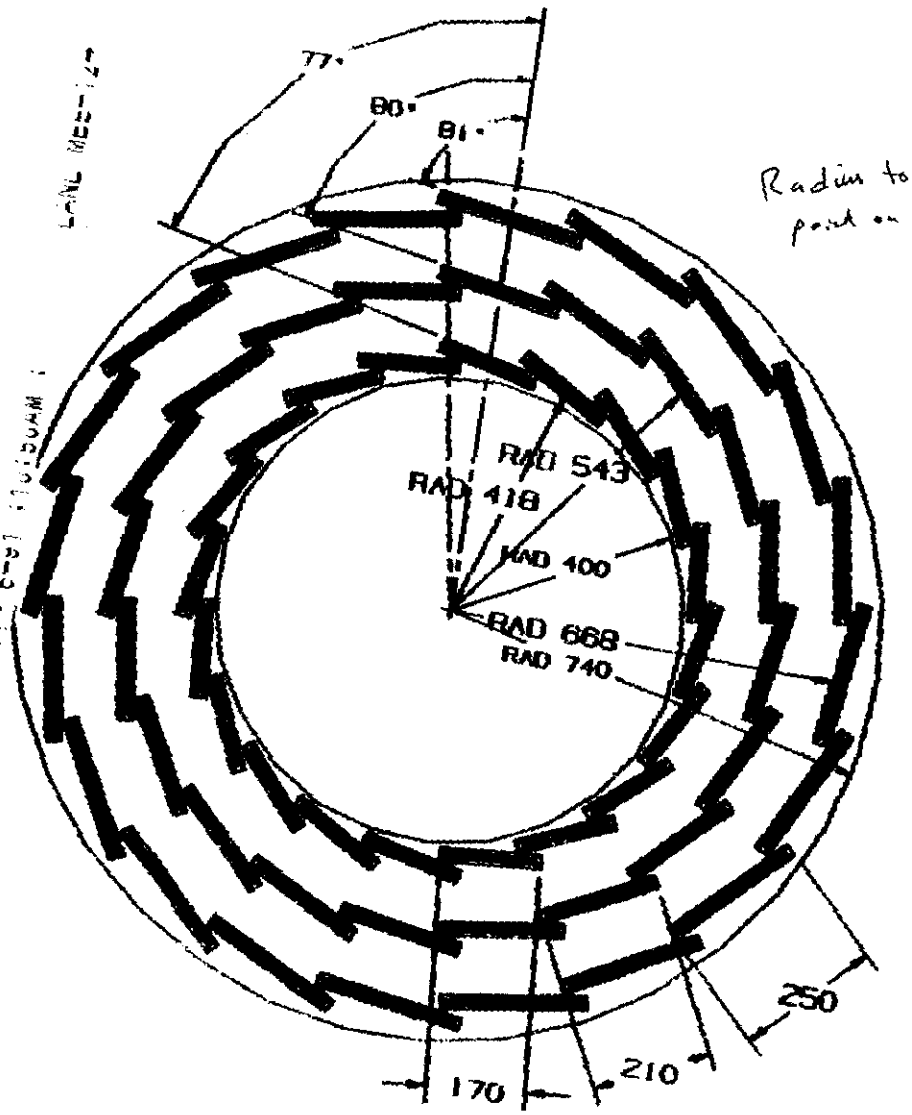
GEM Central Tracker

Pad Chamber Dimensions

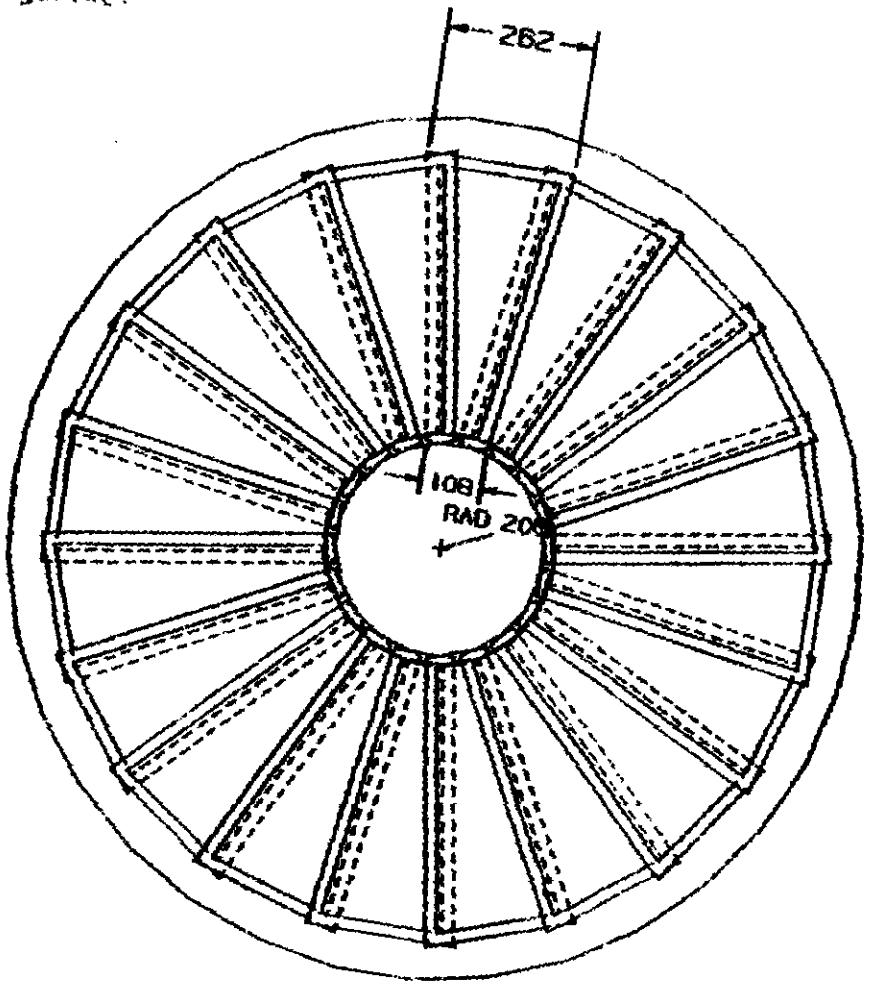
1 6/91

Jan Boissevain LANL (505) 667-6057
Ron Barber


Meters
0
.5
1.0
2961
2000
1101
1226
1351
175
680
280
220
200
150
130
120 typ.
25 typ.
180
250
312
130
113
128
289
384
494
594
684
774
884



Radius to the center point on inside surface.



Simulations and Engineering at Yale

November 6, 1991

Charlie Baltay

Engineering Design Effort at Yale

Will Emmet	ME	~ full time
Andy Disco	ME	~ 1/4
Bill McDonald	ME	~ 1/4 - 1/2
Ted Petersen	Designer	as needed
John Sinott	Super Tech	~ full time

+ very fruitful collaboration with Los Alamos eng.

+ help from Brookhaven

- Pad engineering meeting at Brookhaven

  thursday Nov. 14 ~ 10:00 AM

Design Proposal

Modular Assembly Of Components

- Chevron Pad and signal traces fabricated into a conductor / Insulator laminate with readout traces/connectors.

- Pad and trace laminate bonded to graphite epoxy structures.

- Modular chamber construction of o CTE Graphite Epoxy.

- Chamber modules supported at the ends.

- Single piece cooling manifold with mounted electronics, power supply and signal readouts.

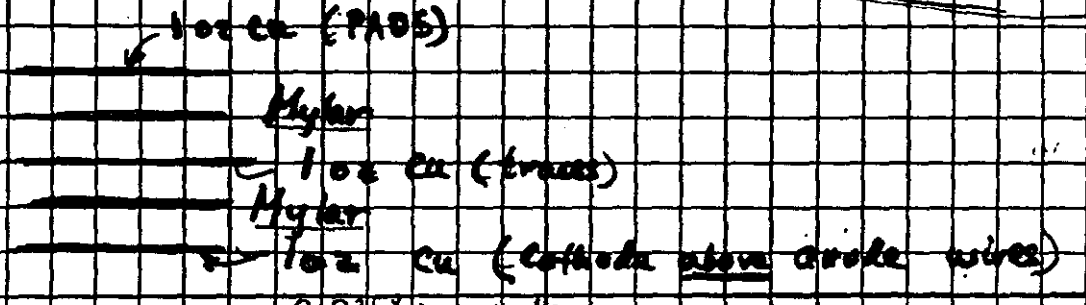
- Self-contained 2 phase room temperature evaporative cooling system.

Estimate of % Radiation Length / Superlayer (3 layers)

Layer Material	thickness (cm)	L_R (cm)	% L_R	
Graphite/epoxy	0.0254	25.0	0.102	Upper Handbac
"	"	25.0	0.102	
"	"	25.0	0.102	
Graphite/epoxy	"	"	"	Lower Handback
"	"	"	"	
"	"	"	"	
* Copper (1oz)	0.0036	1.43	0.252	2 cathode planes / (6 per sup
"	"	"	0.252	
"	"	"	"	
"	"	"	"	
"	"	"	"	
"	"	"	"	
Mylar	0.0127	28.7	0.044	2 × 5 mil Mylar / la (6 per Superlay
"	"	"	"	
"	"	"	"	
"	"	"	"	
"	"	"	"	
"	"	"	"	
** Graphite/epoxy	0.0203 × 3	25.0	0.244	Anode wire supports

Total: 2.63% / Superlayer

↳ Does not include electronics or cooling



Graphite/epoxy anode wire support cross-section

Ratio of support width / min superlayer

$= (2)(1\text{ cm}) / 10\text{ cm} = 0.2$

$(0.0254)(2)(1)(2)(2) = (t_{L(avg)})(10\text{ cm})$

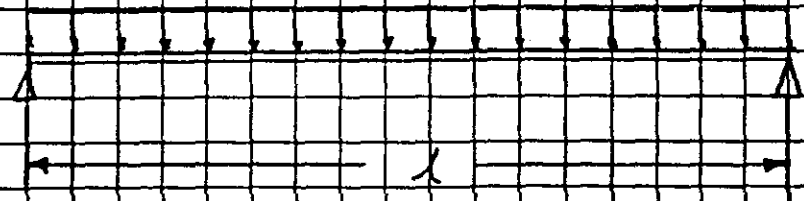
$t_{L(avg)} = 0.0203\text{ cm}$

* Assume no ground planes, signal traces negligible

11/5/01

Estimate of Deflection / Superlayer – 1 g static loading

Assume simply-supported, uniformly-loaded composite beam



$l = 2$ m (full length)
$l = 1$ m (half length)
width = 20 cm (outer kernel module)
" = 16 cm (center module)
= 12 cm (inner module)

$$\boxed{y_{max}\ (\text{deflection}) = \frac{5\, w\, l^4}{384\, EI}}$$

* (Light load) ~ 10.2 lbs max / module (full length)

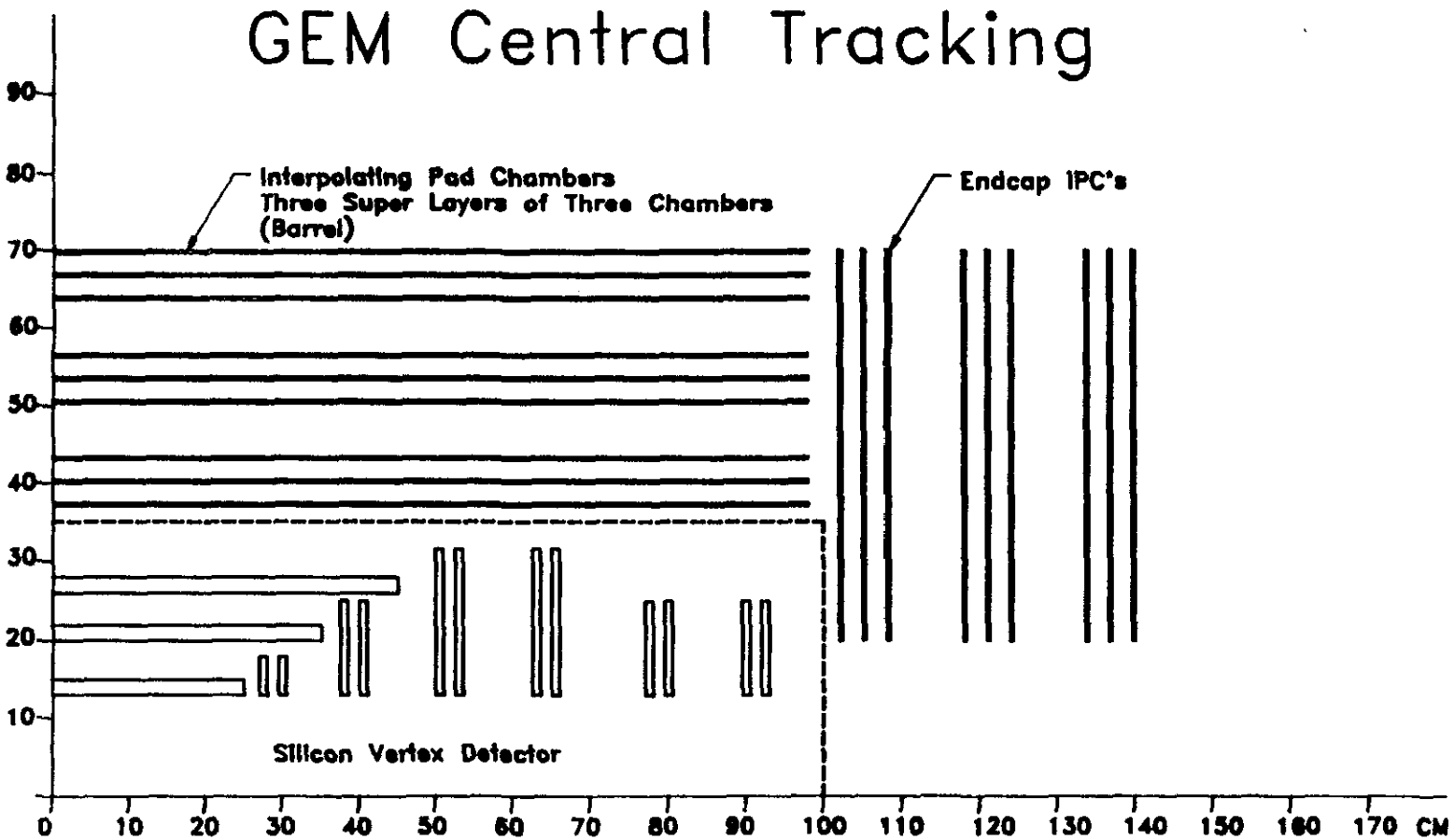
Condition	Deflection (ins / cm)
1) $l = 2$ m / width = 20 cm	0.085" / 0.216 cm
2) $l = 1$ m / width = 20 cm	0.005 / 0.0135
3) $l = 2$ m / width = 16 cm	0.0966 / 0.245
4) $l = 1$ m / width = 16 cm	0.006 / 0.0153
5) $l = 2$ m / width = 12 cm	0.124 / 0.315
6) $l = 1$ m / width = 12 cm	0.008" / 0.0197 cm

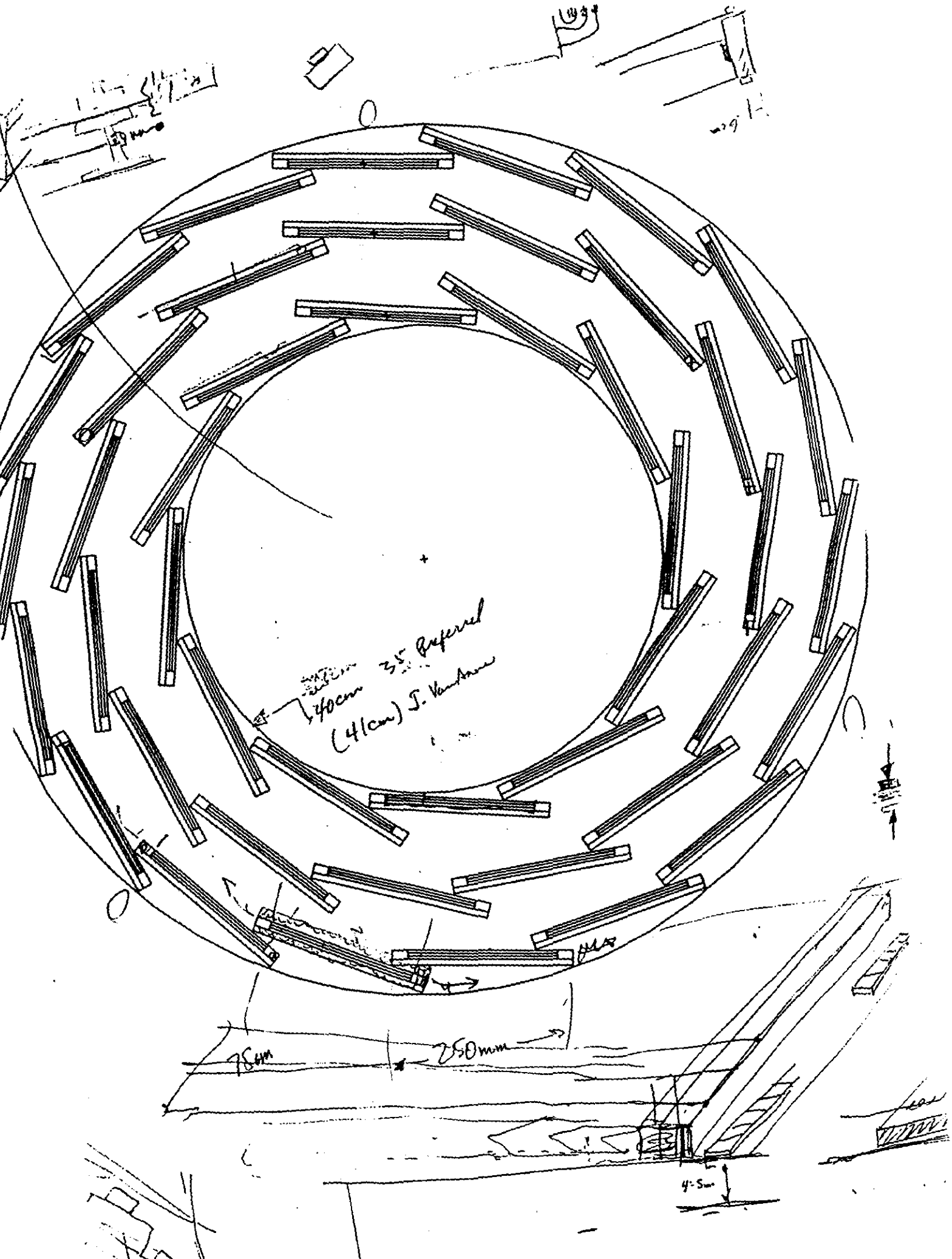
Conditions (1), (3) & (5) are for full length modules

Conditions (2), (4) & (6) are for half-length modules

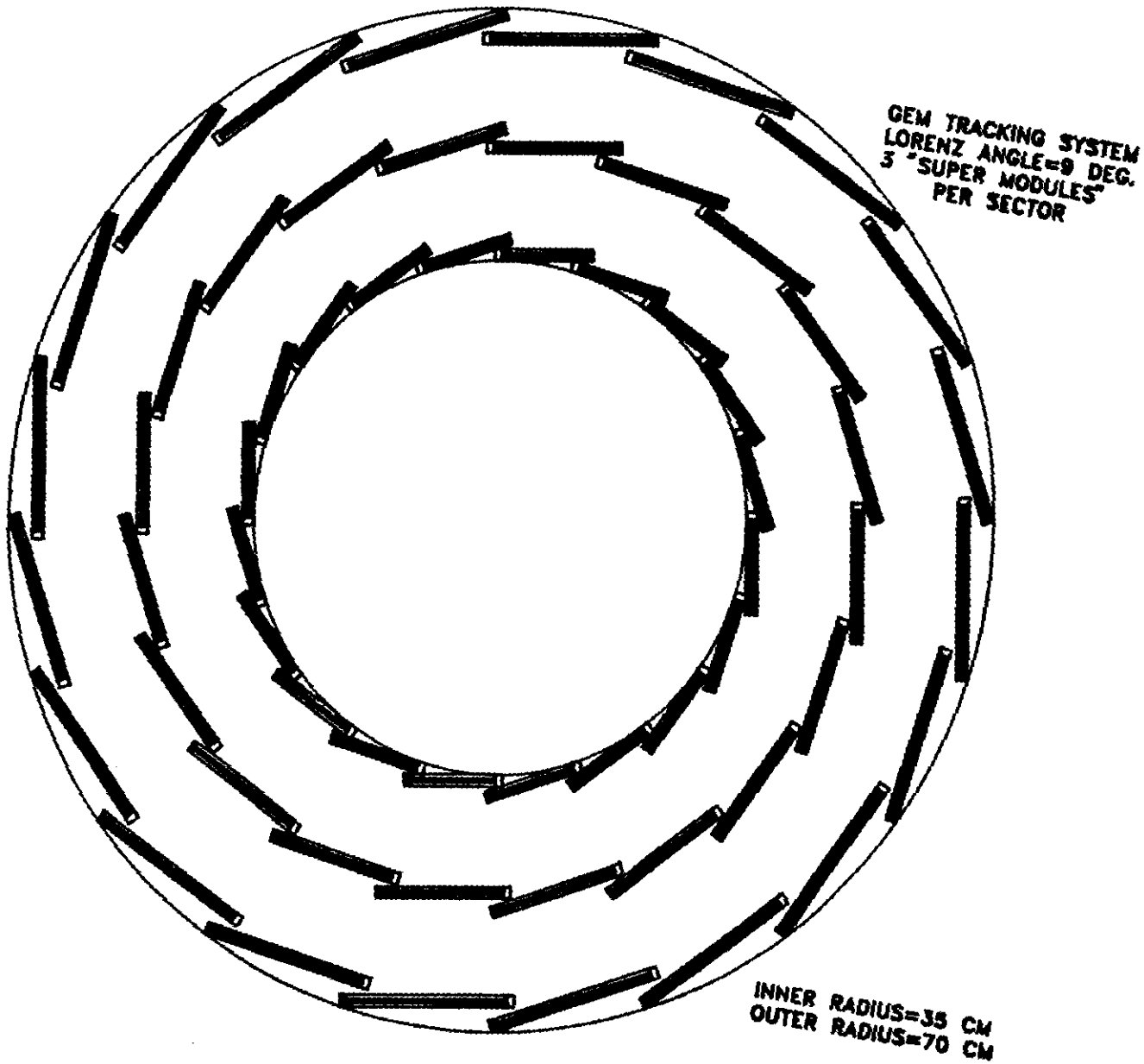
* Assumes 5 lbs for electronics & 2 lbs for cooling –

GEM Central Tracking



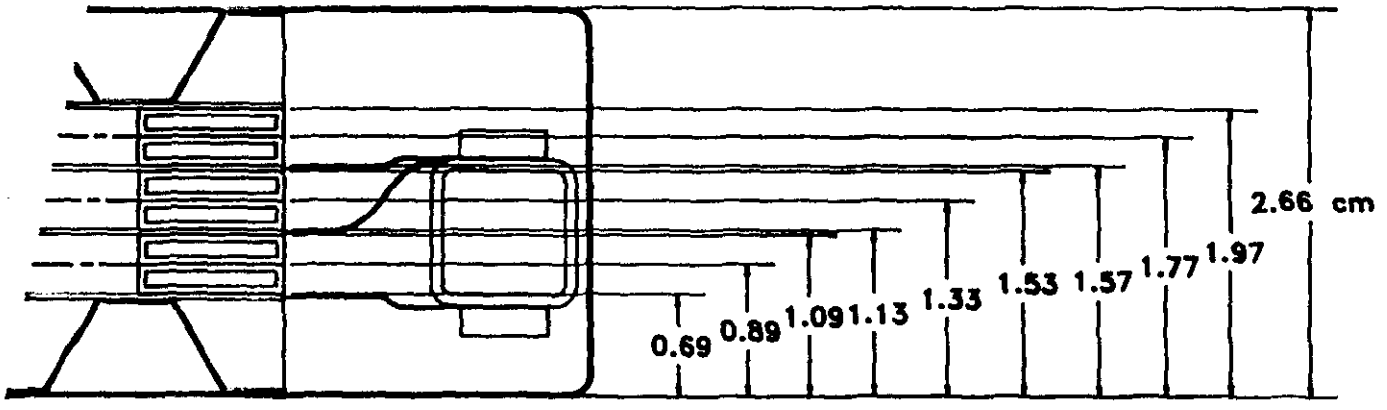


40cm 35 Preferred
(41cm) J. Van Amer
250mm


GEM TRACKING SYSTEM
LORENZ ANGLE=9 DEG.
3 "SUPER MODULES"
PER SECTOR
INNER RADIUS=35 CM
OUTER RADIUS=70 CM

YALE UNIVERSITY

PARTICLE PHYSICS GROUP
W. EMMET 11/5/1991



GEM TRACKER

DETAIL OF IPC SUPERLAYER MODULE
–EDGE w/CATHODE PAD AMPLIFIERS

Tracking Simulation work at YALE

1. Tracking inside jets, multitrack resolution
   Dan Doug, Steve Manly

   Uses ISAJET now running at Yale

2. Resolution studies (without multiple scatt)
   Sumit Sen, Jeff Turk, Steve Manly

   uses homemade fitting program

   Assumes: Silicon

   $$\left.\begin{array}{l} 7 \text{ to } 8\,\mu \text{ per layer} \\ 10\,\mu \text{ alignement} \end{array}\right\} \sigma = 13\,\mu$$

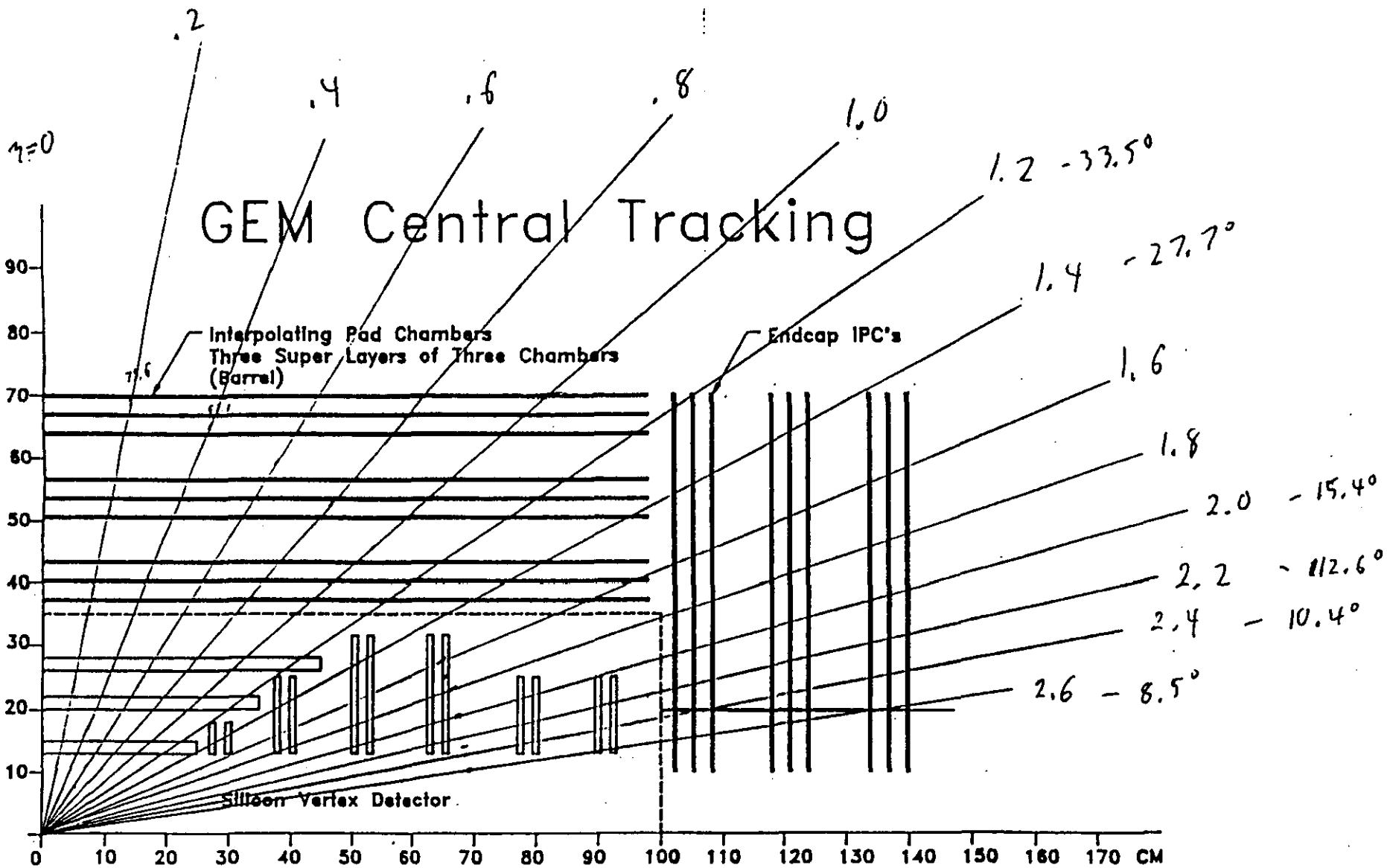
   Pads

   $$\left.\begin{array}{l} 50\,\mu \text{ per layer} \\ 25\,\mu \text{ alignement} \end{array}\right\} \sigma = 56\,\mu$$

3. Detailed simulation with GEANT + ISAJET
   Sumit Sen, Eliot Wolin, Steve Manly
   Rochelle Lauer

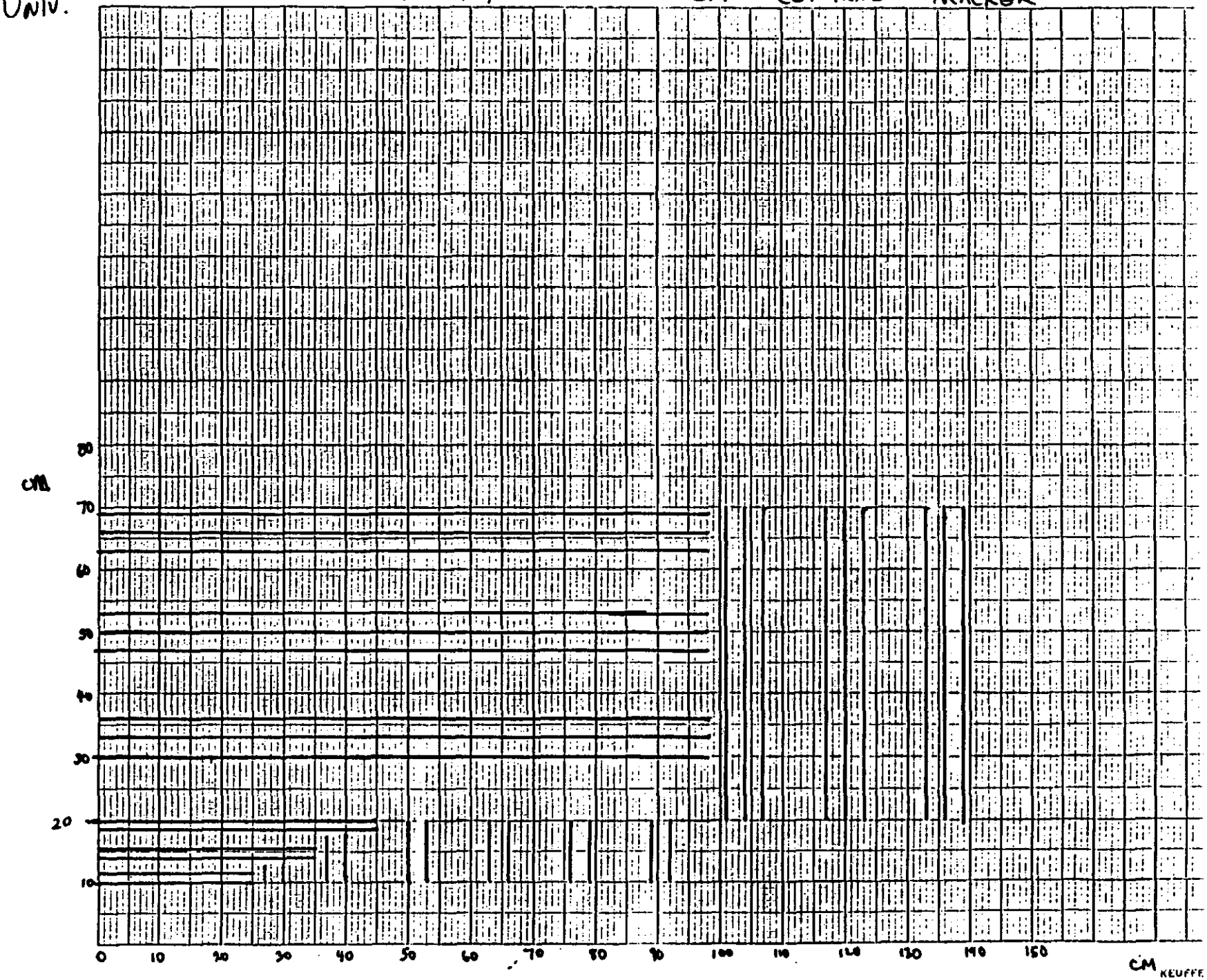
   Now have a version of GEANT running at Yale

   → Need to integrate effort with others in Tracking


GEM Central Tracking
η=0
.2
.4
.6
.8
1.0
1.2 - 33.5°
1.4 - 27.7°
1.6
1.8
2.0 - 15.4°
2.2 - 12.6°
2.4 - 10.4°
2.6 - 8.5°
Interpolating Pad Chambers
Three Super Layers of Three Chambers
(Barrel)
Endcap IPC's
Silicon Vertex Detector
90
80
70
60
50
40
30
20
10
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150
160
170
CM

SUMIT DEN
YALE UNIV.

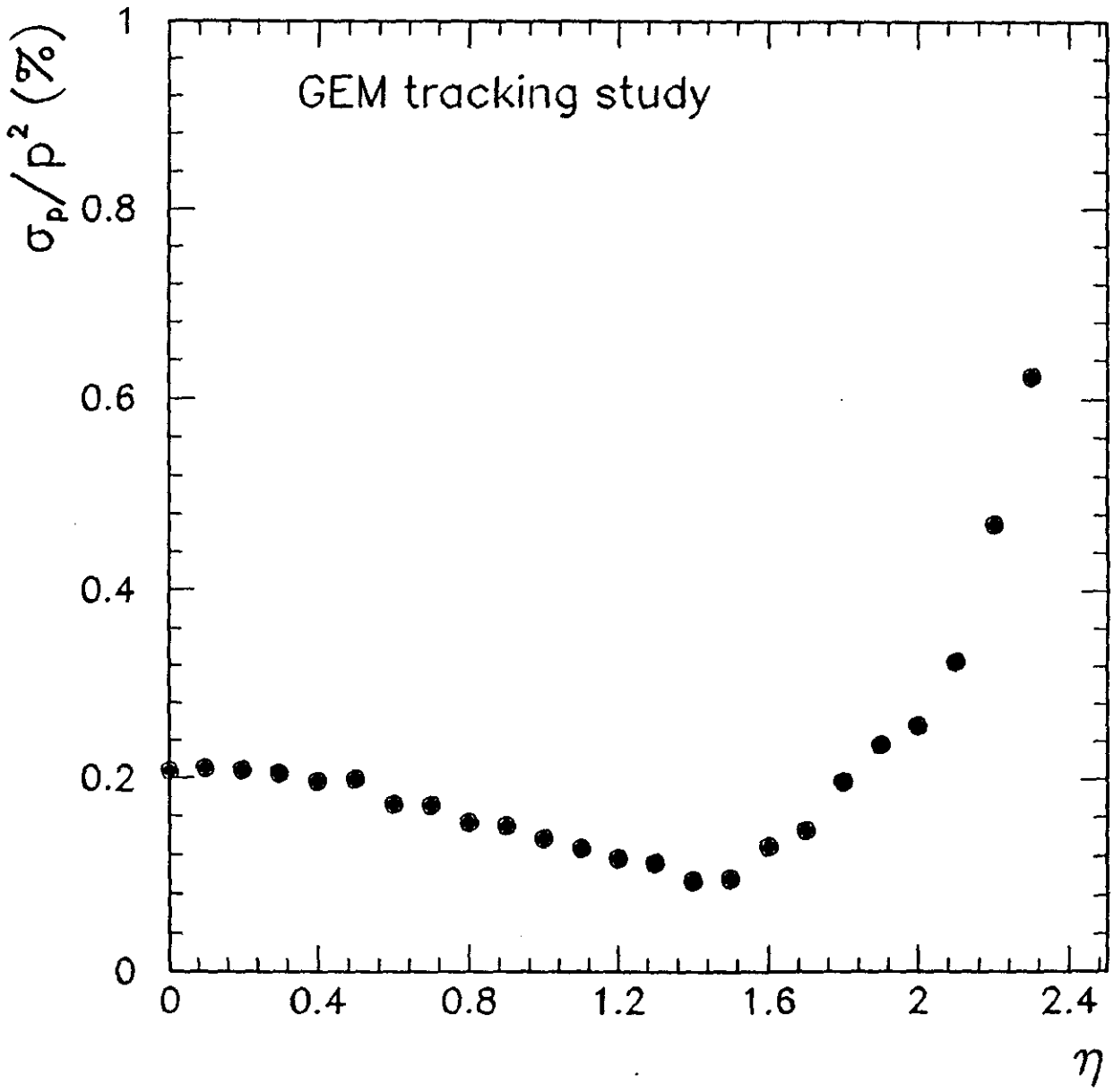
NEW GEOMETRY FOR GEM CENTRAL TRACKER



NO. 334-2TR, 10 X 10 TO THE HALF INCH.
MADE IN U.S.A.
100% RAG PAPER
KEUFFEL

SUMIT SEN
YALE UNIV.

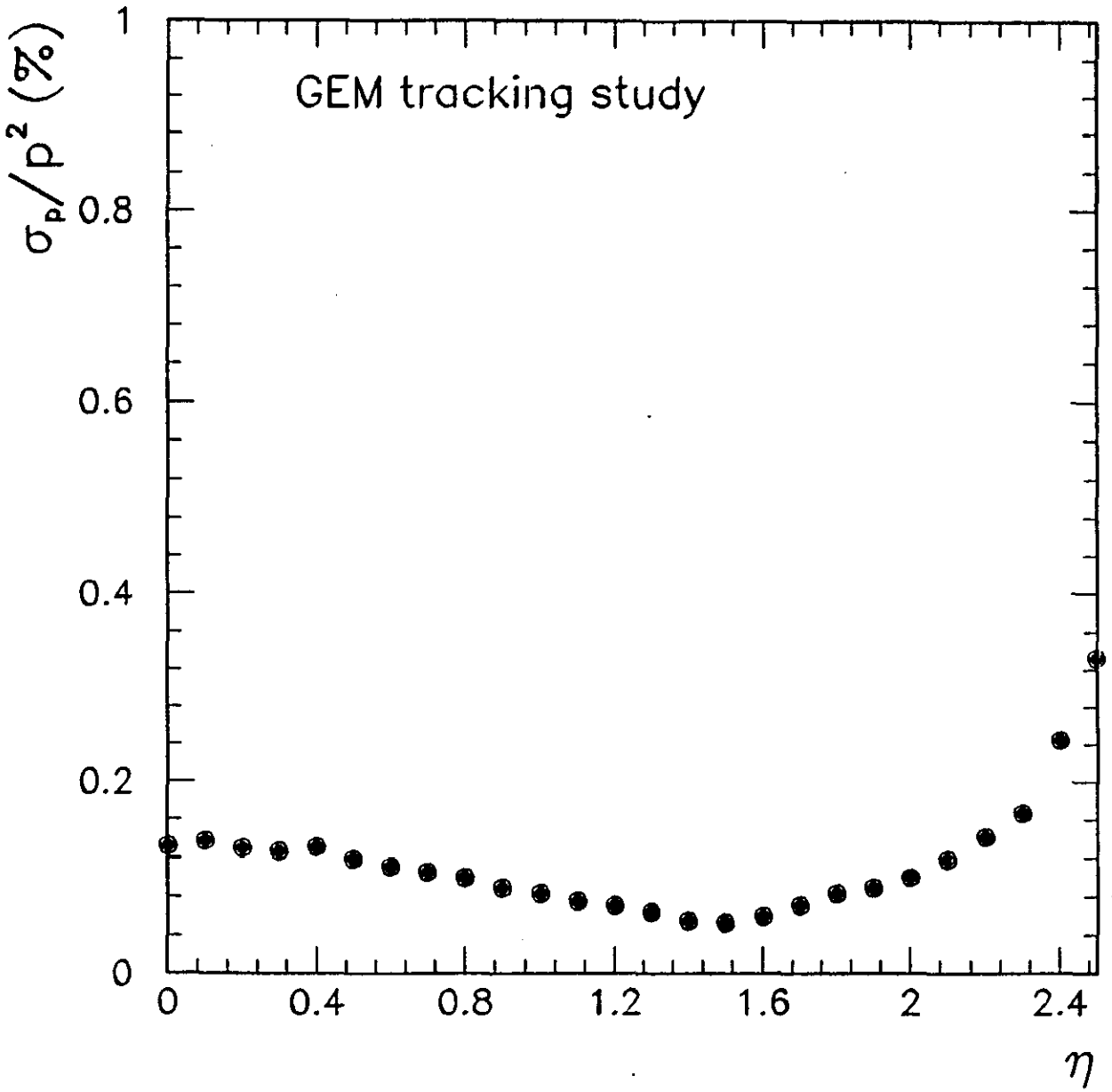
● $p = 20$ GeV/c
no vertex



Sumit Sen
Yale Univ.

$p = 100\,GeV$

with vertex constr.



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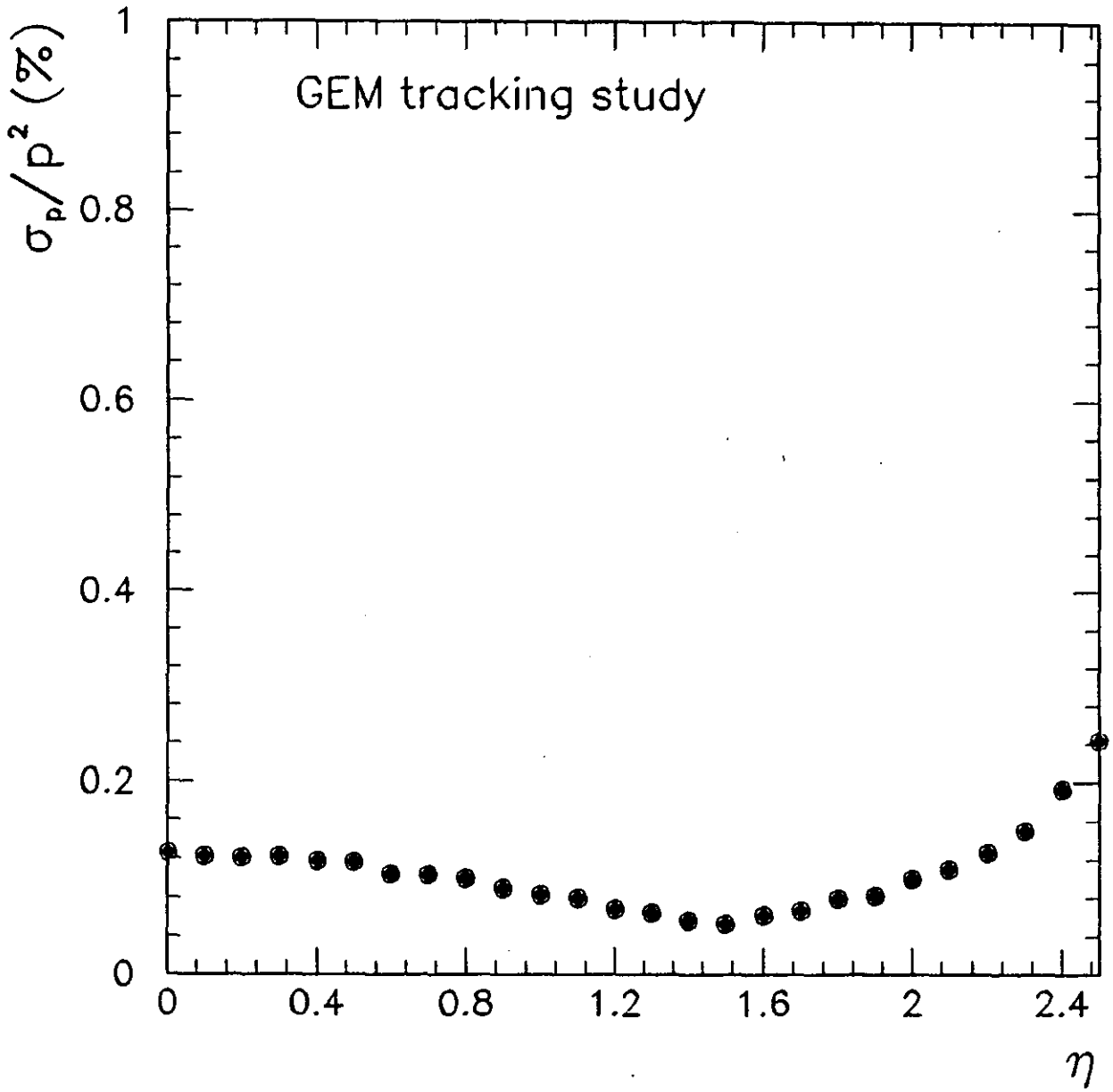
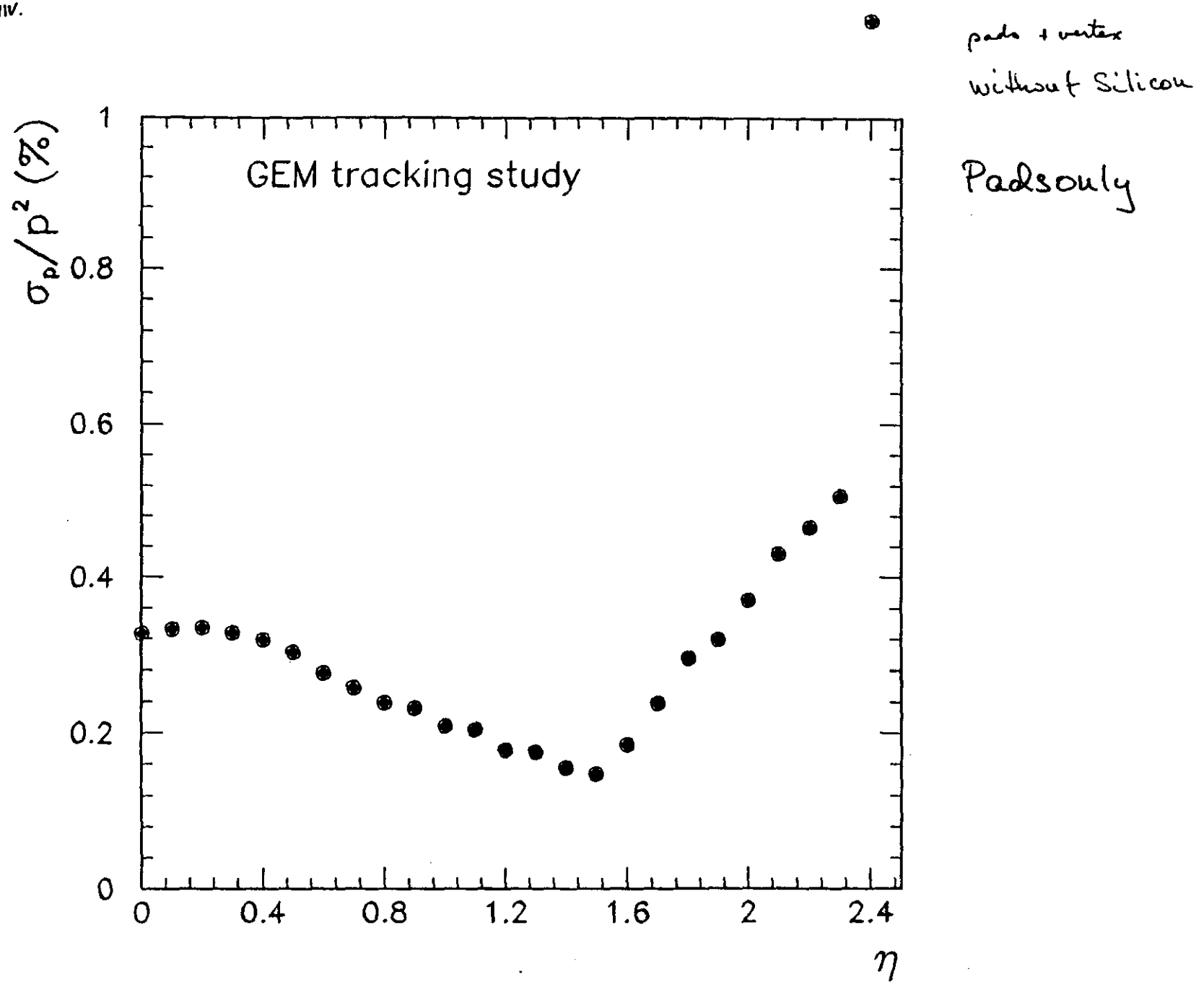
p = 20 GeV
vertex constraint.



SUMIT SEN
YALE UNIV.



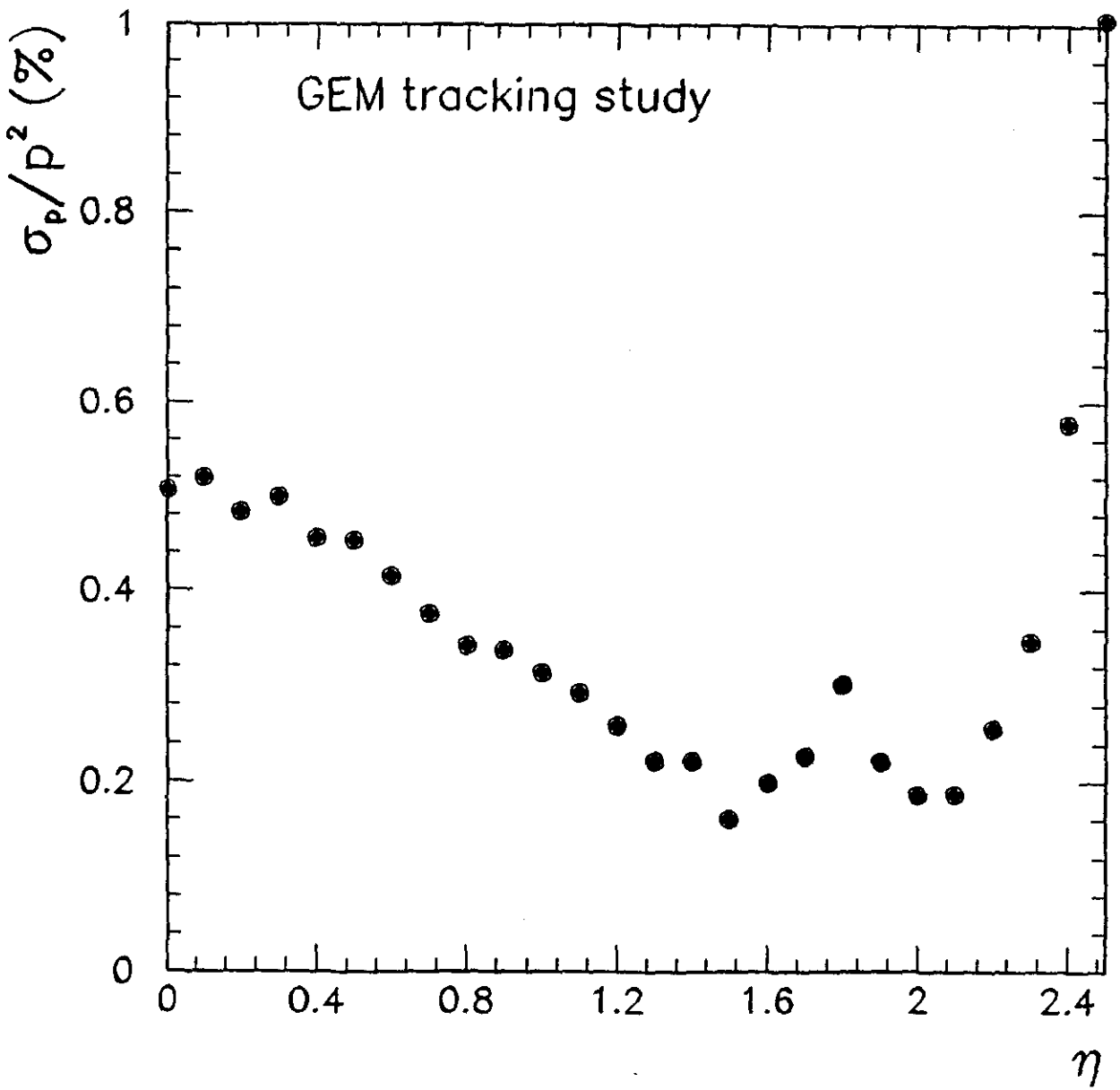
SUMIT SEN
YALE UNIV.

Si + vertex

20 GeV/c

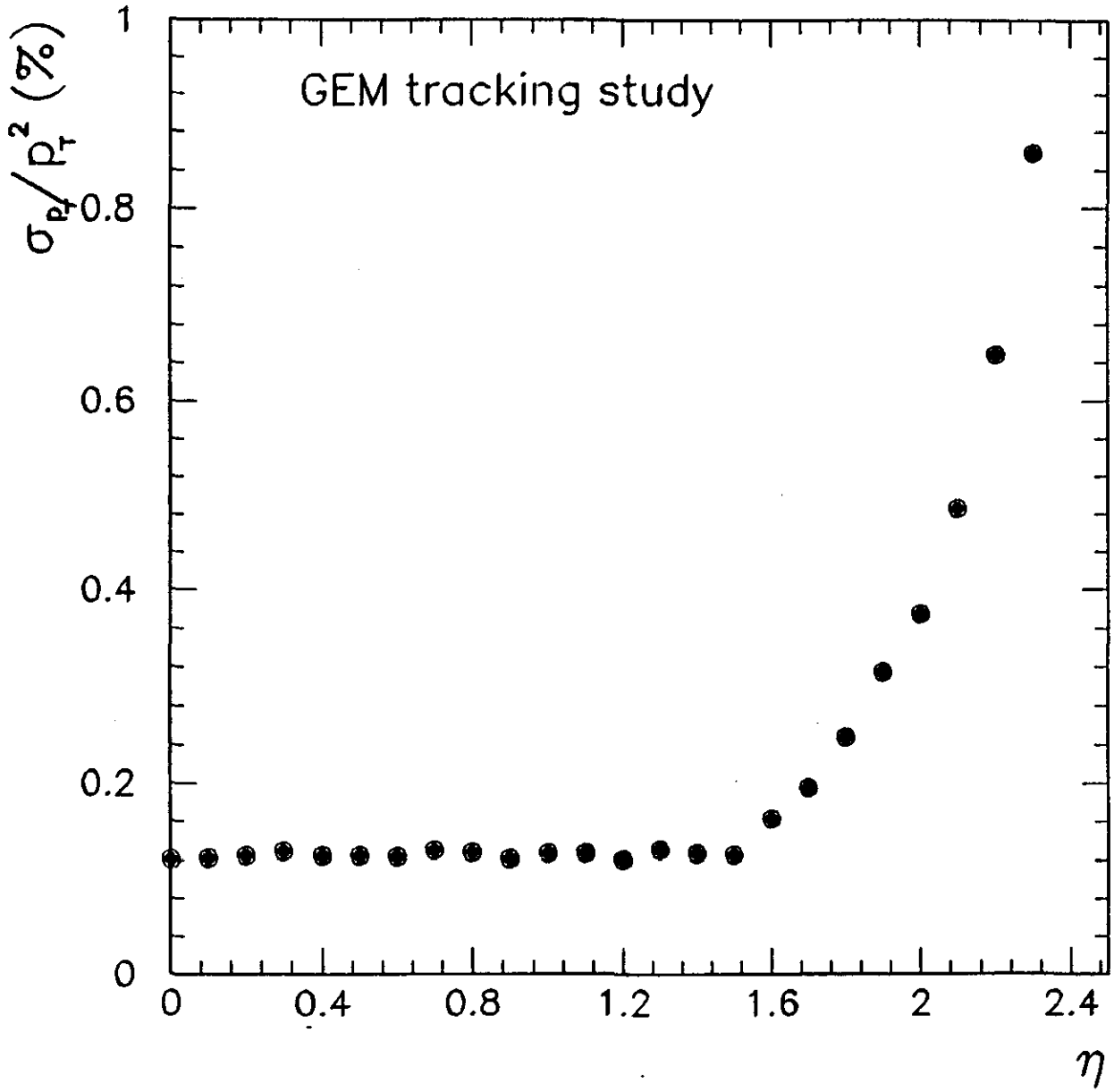
Vertex constraint

Silicon only



SUMIT SEN
YALE UNIV.

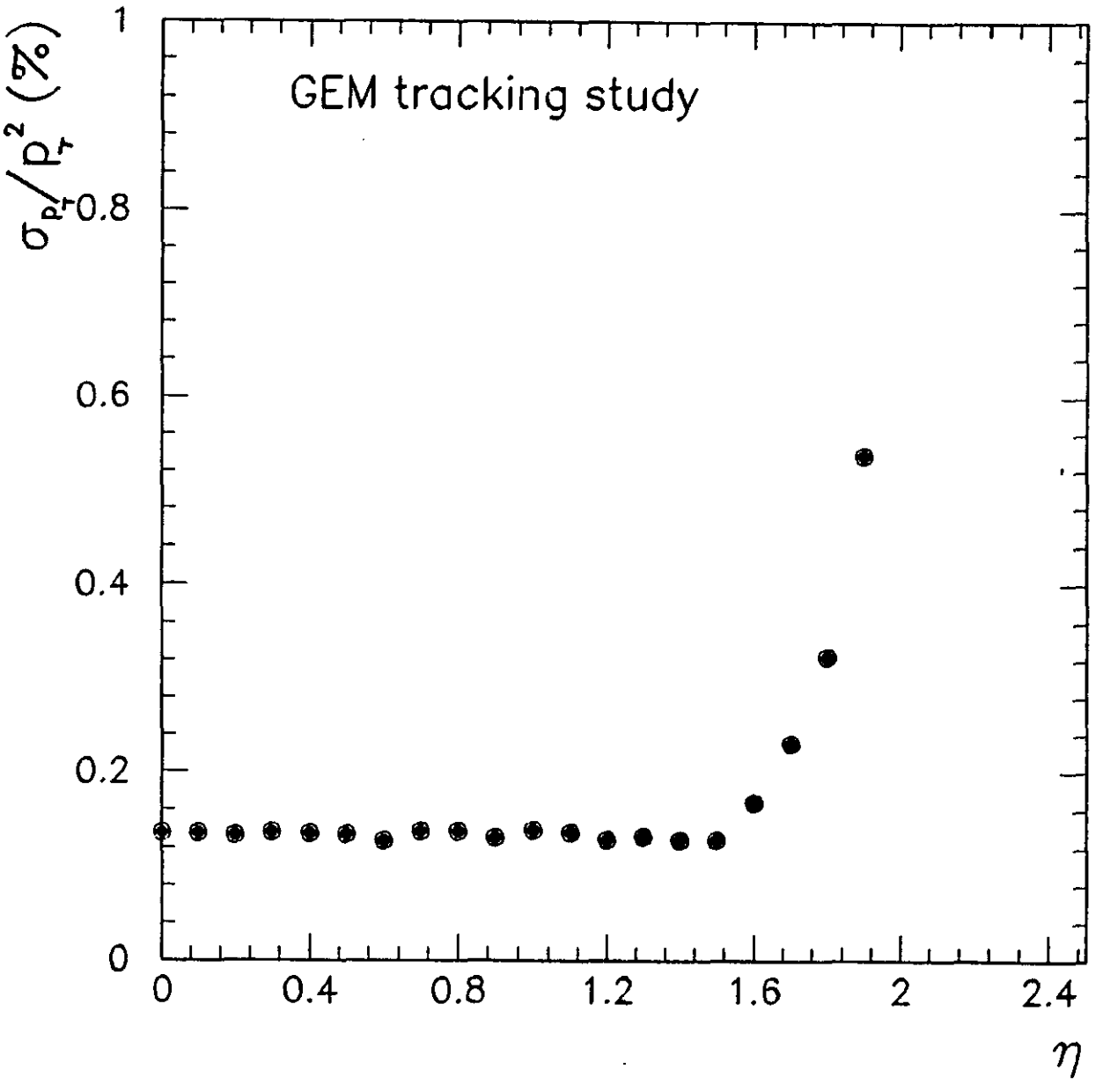
p_T = 20 GeV
Vertex constraint



SUMIT SEN
YALE UNIV.

p_T = 100 GeV

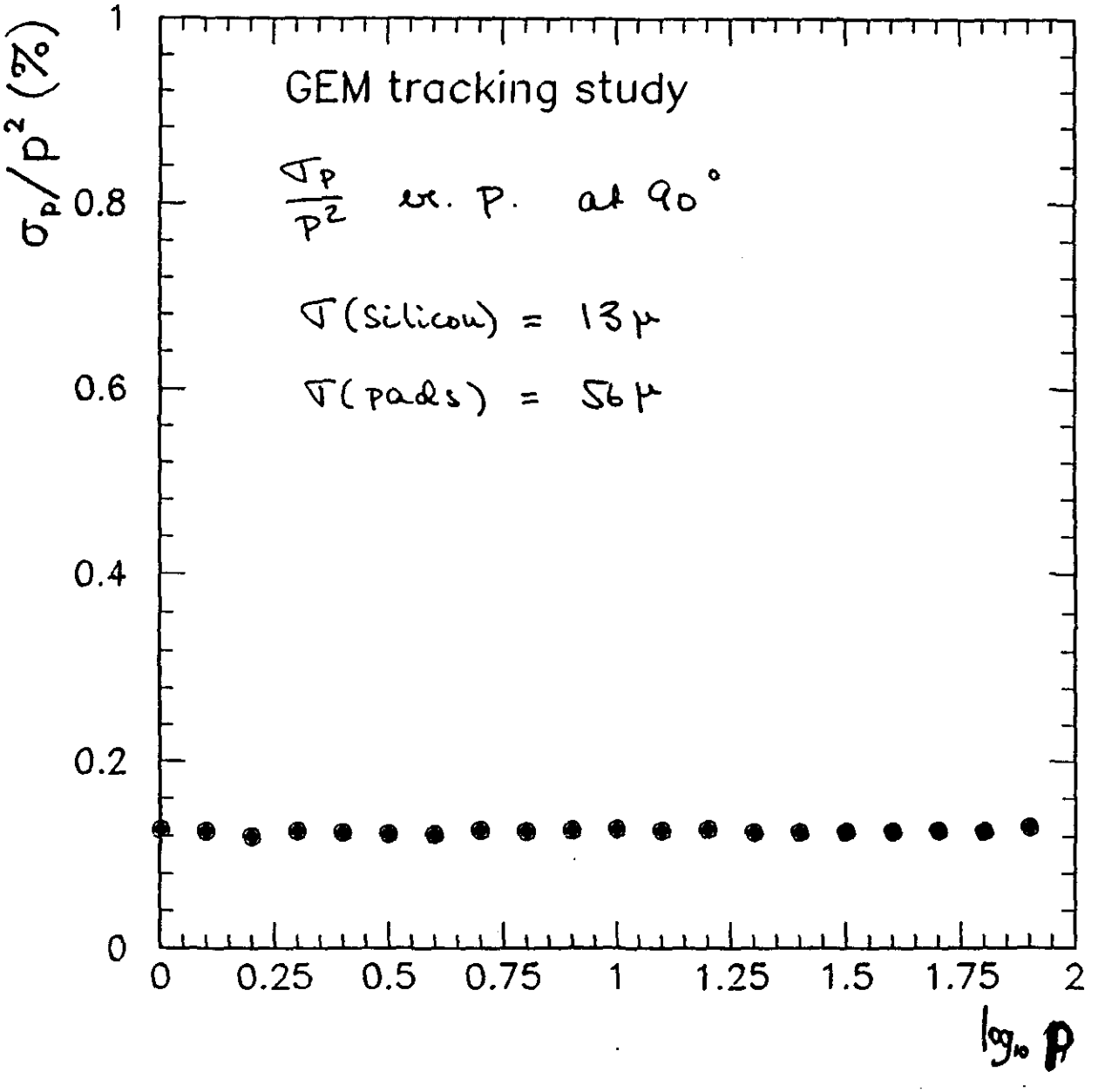
Vertex constraint



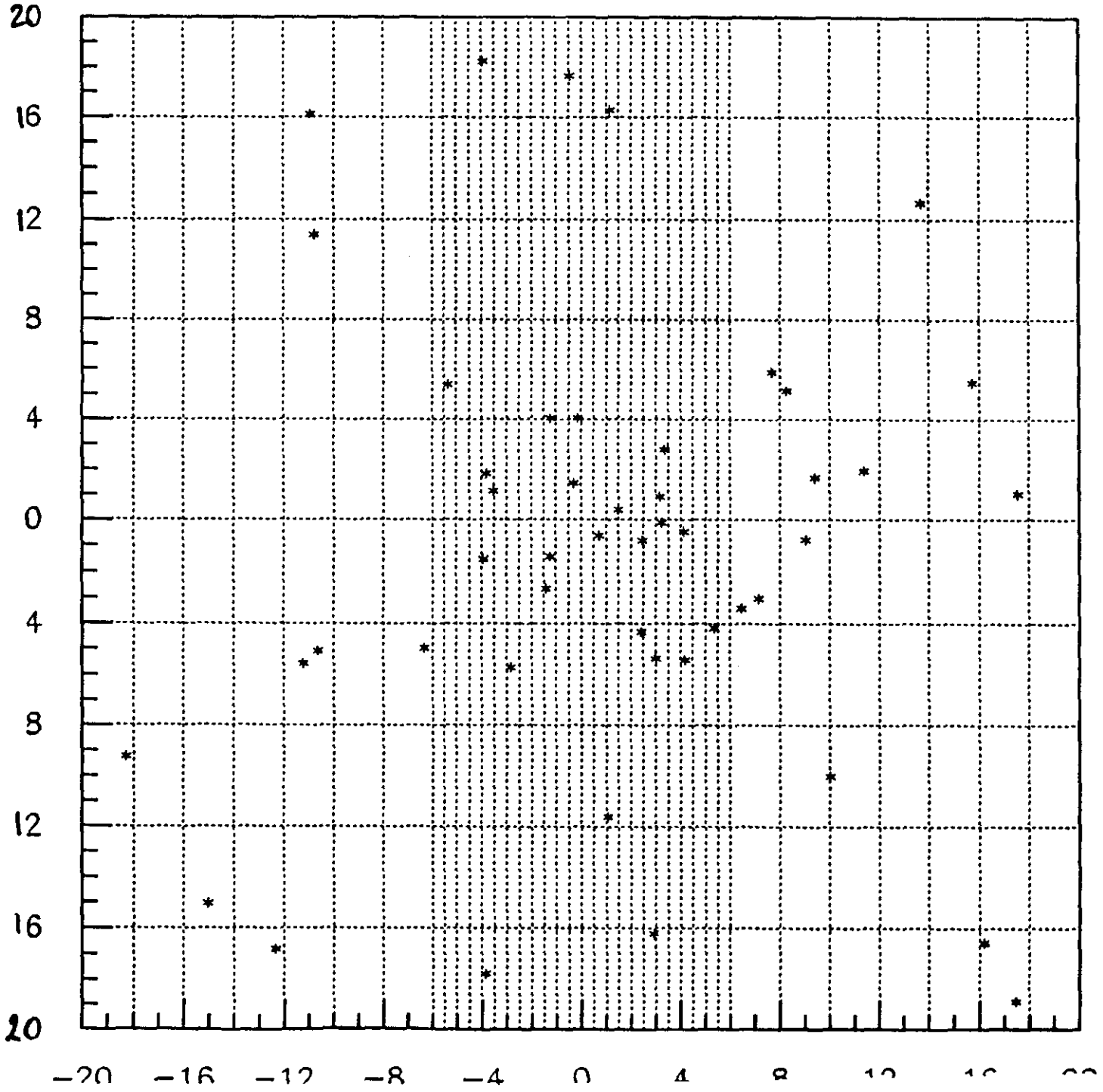
Sumit Sen
Yale Univ.

P = variable
wider vertex Constr

σ(silicon) = 13μ
σ(pads) = 56μ



Dan Dong, Yale Univ



ISAJET

$t\bar{t}$ jets

$P_t \sim 116$ GeV/c

$P_{\bar{t}} \sim 330$ GeV/c

this is the t or $\bar{t}$ jet (not sure which)

48 tracks intersecting one plane of pad chambers with 0.5 cm × 4 cm pads

Silicon Tracker R&D

FY 92 Tasks	Manpower	M&S
Electronics		
1. 8 channel wide Semi-custom Analog rad hard circuit design and testing. Heat load specification.	.5	100
2. 8 channel wide Semi-custom Digital rad hard circuit design and testing. Heat load specification.	.5	100
3. Output driver technology review, selection, and prototype design. Heat load specification.	.5	
Mechanical		
1. Silicon Tracker Conceptual design, analysis, and systems studies for the TDR.	1.9	20
2. GEM subsystems Integration (Funded through Integration)	(.75)	(15)
and management.	.25	15
3. Silicon Ladder prototype including: design, analysis, specification, production planning, bonding, thermal analysis.	.8	30
4. In-situ alignment measurement system design and prototype evaluation.	.5	40

Pad Chamber Engineering and R & D

Mechanical		
1. Cooling System design and prototype testing.	.4	20
2. Structural Chamber design, analysis and materials study. (Yale Coordination)	.3	20
Totals	**5.65**	**345**
K$ Total (140 K$/FTE)		**1136**

2. Interpolating Pad Chambers

a. Mechanical - chambers and support structure

	FTE	Cost Estimate Total	GEM	OTHER
i. Engineering & Design				
R. Barber (Los Alamos)	0.5	75	75	0
D. Makowiechi (BNL)	0.25	32	32	0
W. Emmet (Yale)	0.75	70	0	70
A. Disco (Yale)	0.25	24	0	24
T. Petersen (Yale)	0.50	25	0	25
J. Sinnott (Yale)	0.75	32	0	32
Kouba (Michigan)	0.50	30	30	0
		288	137	151
ii. M&S for Prototypes (Yale)		75	0	75
M&S (Michigan)		40	40	0
		115	40	75
b. Readout Electronics		403	177	226
i. Engineering $ Design				
Engineer (BNL)	1.0	125	125	0
Chuck Bower (Indiana)	1.0	40	0	40
Mark Gebhard (Indiana)	0.6	20	0	20
Jim Pitts (Indiana)	0.7	25	0	25
3 Engineers (Wash. Univ.)	0.75	50	50	0
		260	175	85
M&S (BNL)		50	50	0
M&S (Indiana)		50	50	0
M&S (Washington Univ.)		13	13	0
		113	113	0
		373	288	85
Total Interpolating Pad Chambers		776	465	311

CENTRAL TRACKING R&D REQUEST SUMMARY

Technlogy	GEM	Other	Total
1. Silicon Microstrips	625	0	625 K$
2. Pad Chambers	465	311	776
3. Scintillating Fibers	100	210	310
4. Straws	75	25	100
Totals	1265	546	1811 K$
Add'l LAM	508		
	1773		

Nov. 6, 1991
Steve Shapiro

HYBRID PIXEL DETECTOR DEVELOPMENT

I WHAT IS A HYBRID ?

II THE GENERIC PROGRAM

III THE ROAD TO THE SSC CHIP

IV WHY PIXELS ?

V ARE THEY REAL ?

Stephen L. Shapiro

Stanford Linear Accelerator Center, Stanford, CA 94309

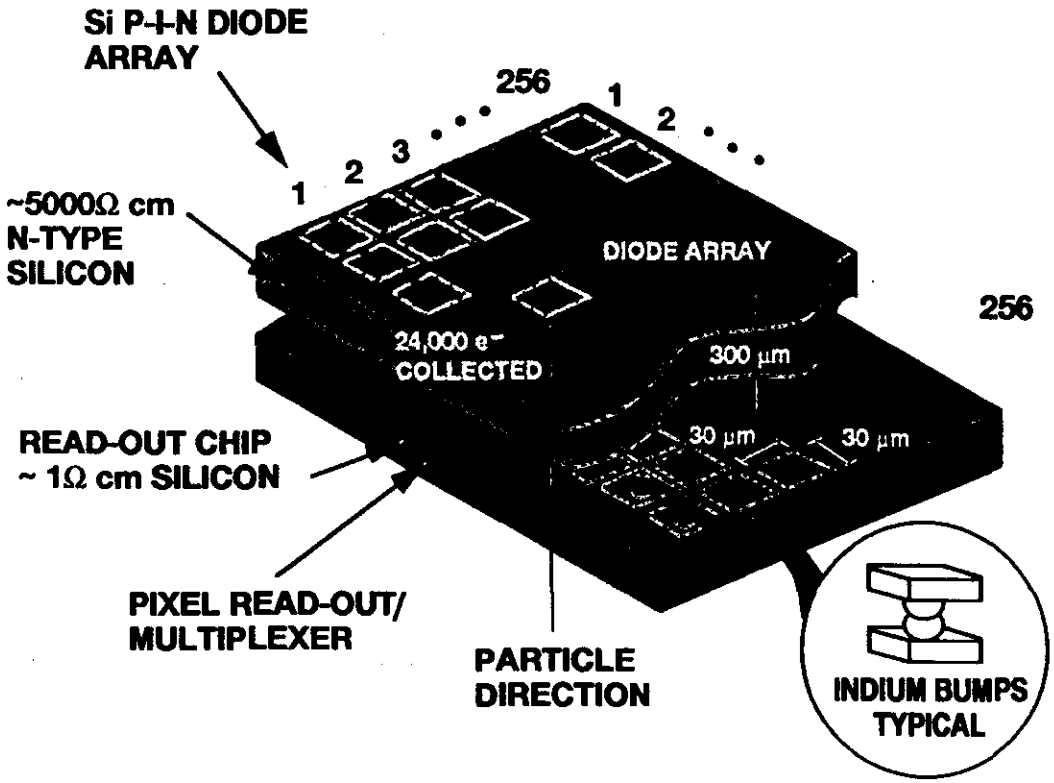
John F. Arens, J. Garrett Jernigan

Space Sciences Laboratory, University of California, Berkeley, CA 94720

Hybrid Detector Approach Optimizes Performance

HUGHES

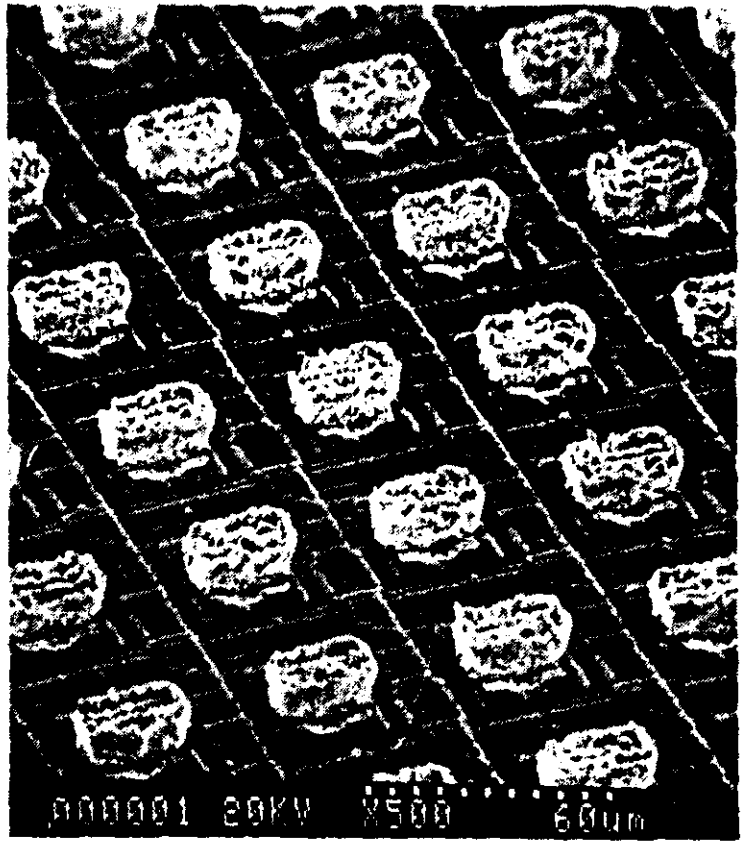
7729-SP9 MC18

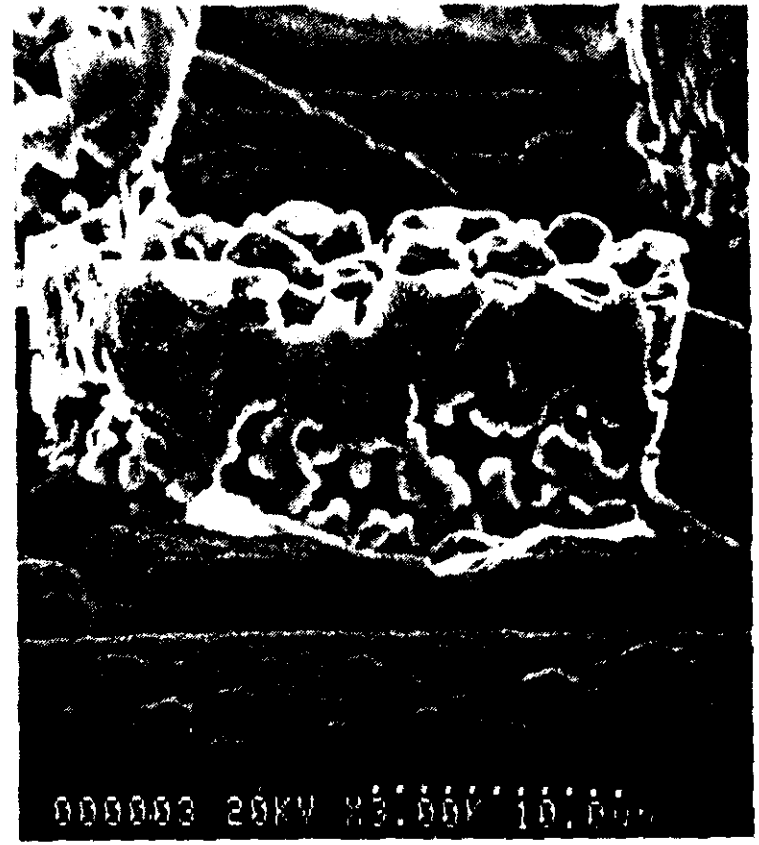


- Each element separately optimized
- Changes in detector or readout easily accommodated
- Yield losses in detector and readout processing not compounded

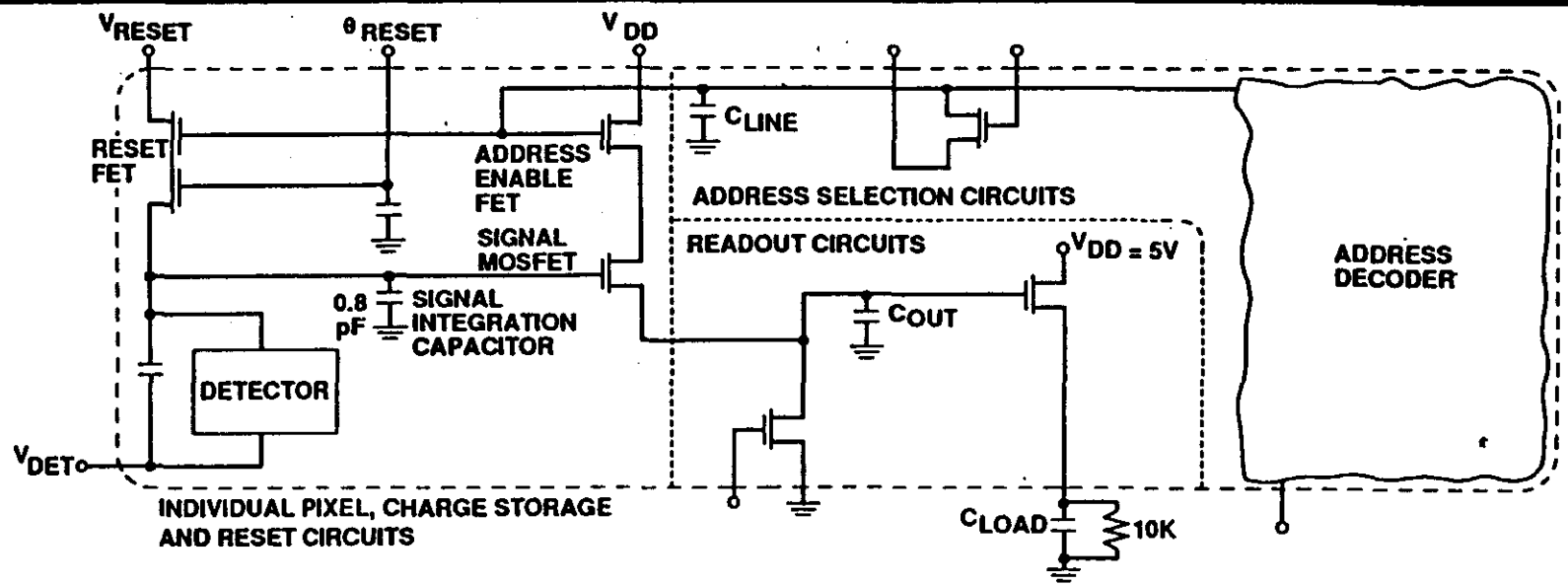
CRC-305
9 MICRON INDIUM BUMPS

HUGHES





HYBRID ARRAYS PROVIDE OPTIMAL PERFORMANCE IN A VARIETY OF CONFIGURATIONS

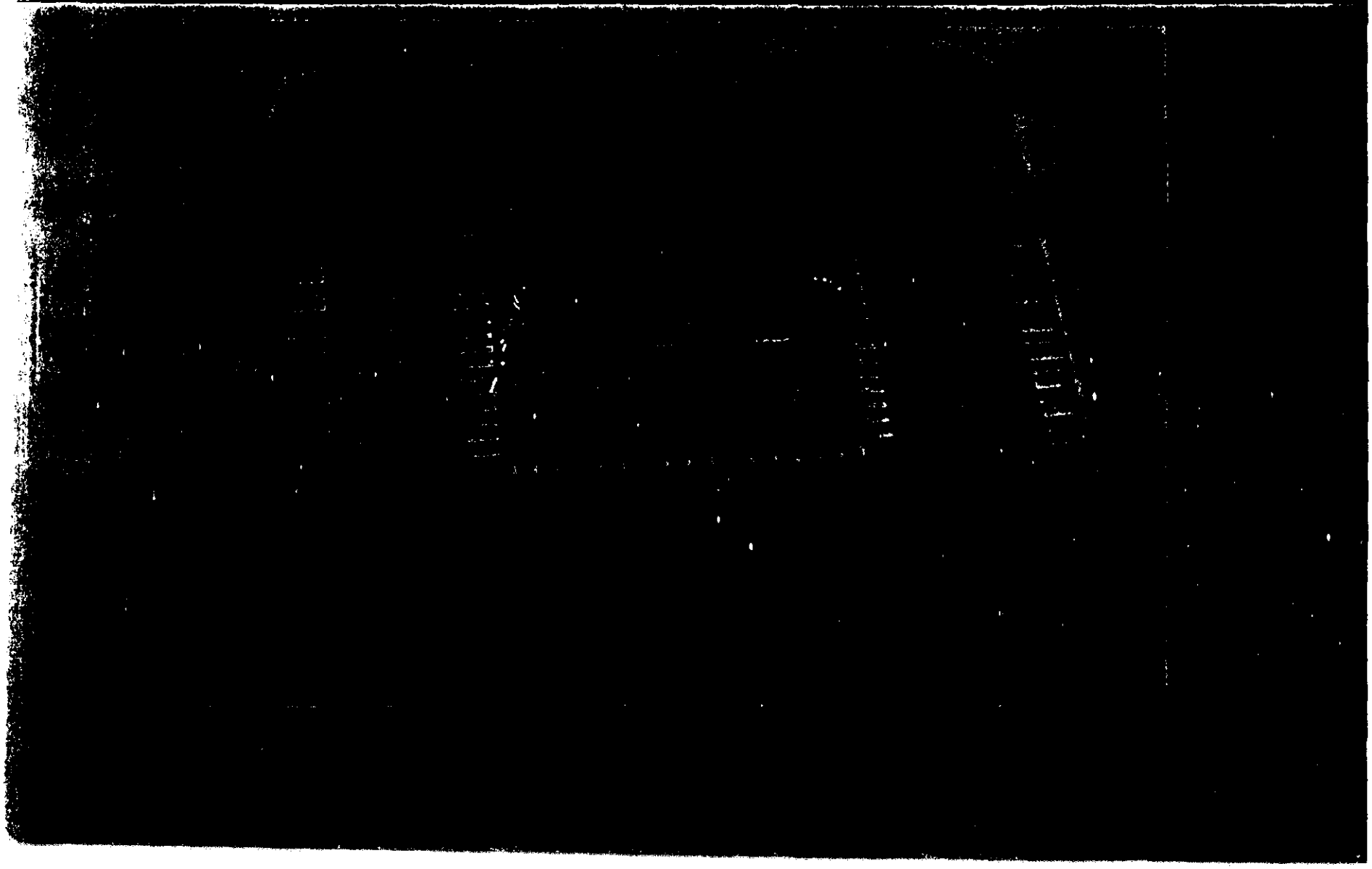


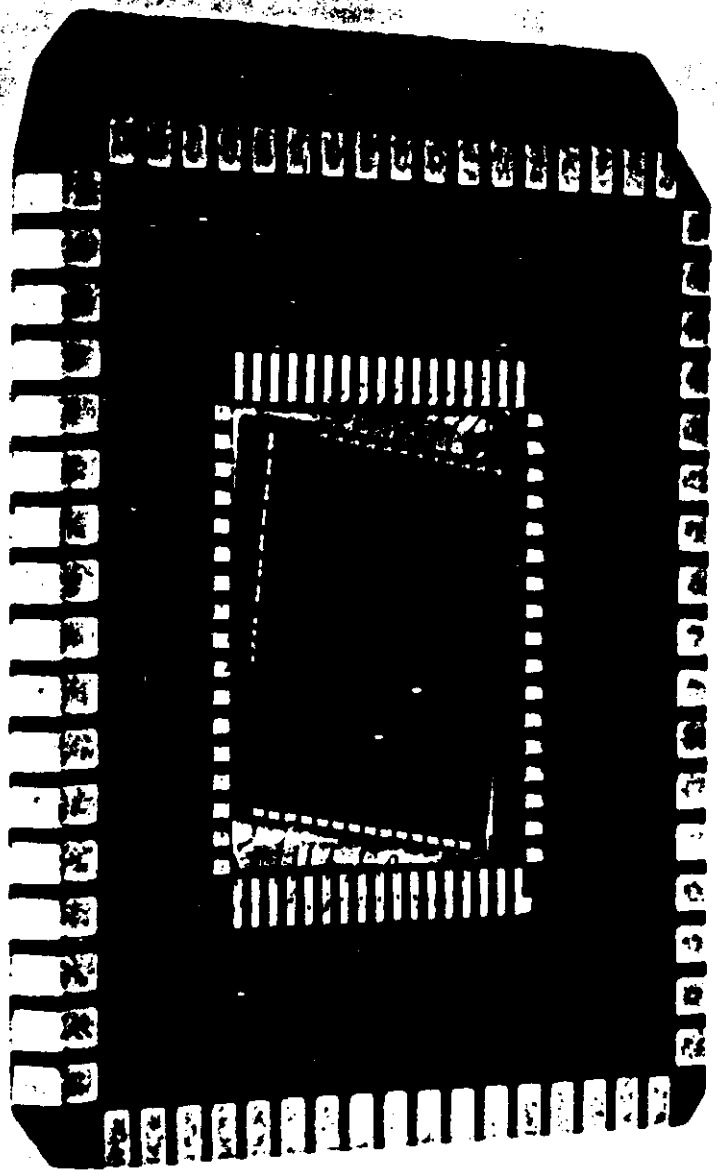
SUMMARY OF DEVICE PARAMETERS

ARRAY DIMENSION	10 X 64	256 x 256
PIXEL SIZE	120 MICRONS	30 MICRONS
DETECTOR MATERIAL	GERMANIUM, SILICON	SILICON
NUMBER OF READOUT CHANNELS	10	2
POWER DURING "WRITE" CYCLE	0 mW	0 mW
POWER DURING READ CYCLE	10 mW	2 mW
PERESENT CLOCK SPEED	1 MHz	2 MHz
THEORETICAL CLOCK SPEED	10 MHz	10 MHz
RADIATION HARDNESS	1 MRad	?
NOISE AT ROOM TEMP	<300 ELECTRONS	<300 ELECTRONS

SOLID STATE PIXEL DETECTOR

100x64 ARRAY 100μ x 100μ PIXEL





UNCLASSIFIED

RESENTATION _____

QUESTER ORIGINATOR _____ DATE _____ VG NO _____

SIGNAL RESPONSE

HYBRID ID: IVA 137

15-JUL-1987 13:58:41.03

TEMP (K) 300.0

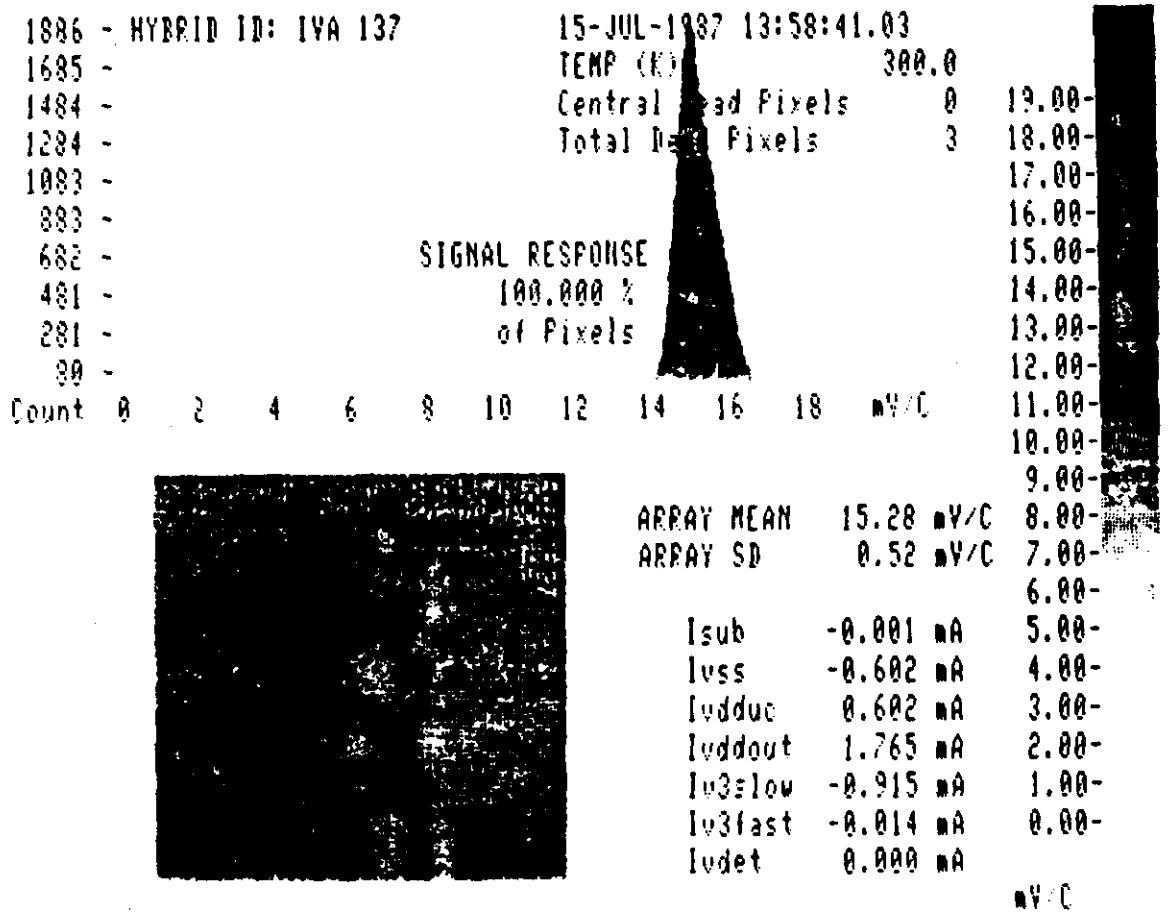
Central Dead Pixels 0

Total Dead Pixels 3

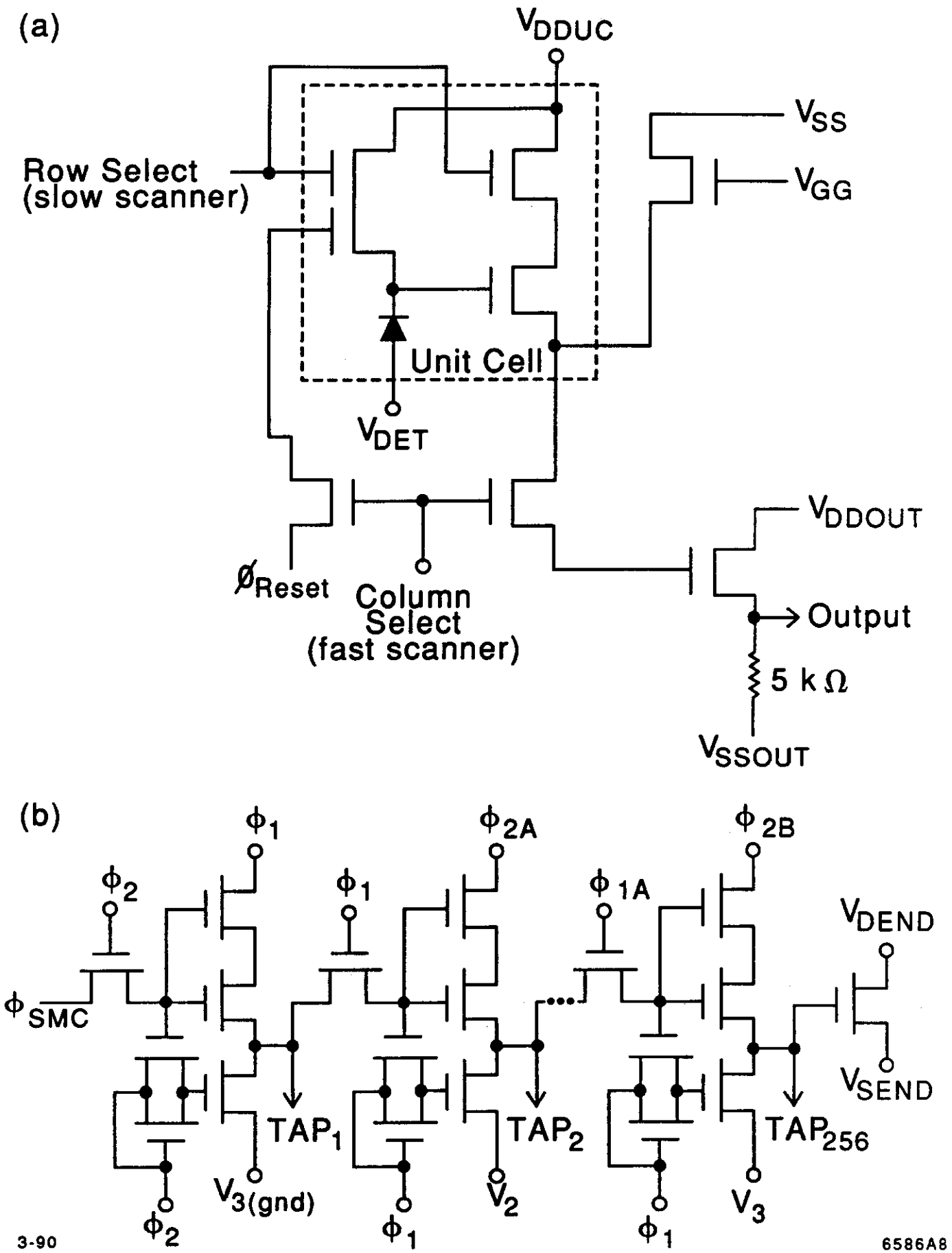
SIGNAL RESPONSE

100.000 %

of Pixels



ARRAY MEAN	15.28	mV/C
ARRAY SD	0.52	mV/C
Isub	-0.001	mA
Iuss	-0.602	mA
Iuddue	0.602	mA
Iuddout	1.765	mA
Iu3slow	-0.915	mA
Iu3fast	-0.014	mA
Iudet	0.000	mA


(a)
VDDUC
VSS
VGG
Row Select
(slow scanner)
Unit Cell
VDET
VDDOUT
ØReset
Column
Select
(fast scanner)
Output
5 kΩ
VSSOUT
(b)
φ1
φ2A
φ2B
φ2
φ1
φ1A
VDEND
φSMC
VSEND
TAP1
TAP2
TAP256
V3(gnd)
V2
V3
φ2
φ1
φ1
3-90
6586A8

PIXEL DETECTOR ANALOG AND DIGITAL SIGNAL PROCESSING ELECTRONICS

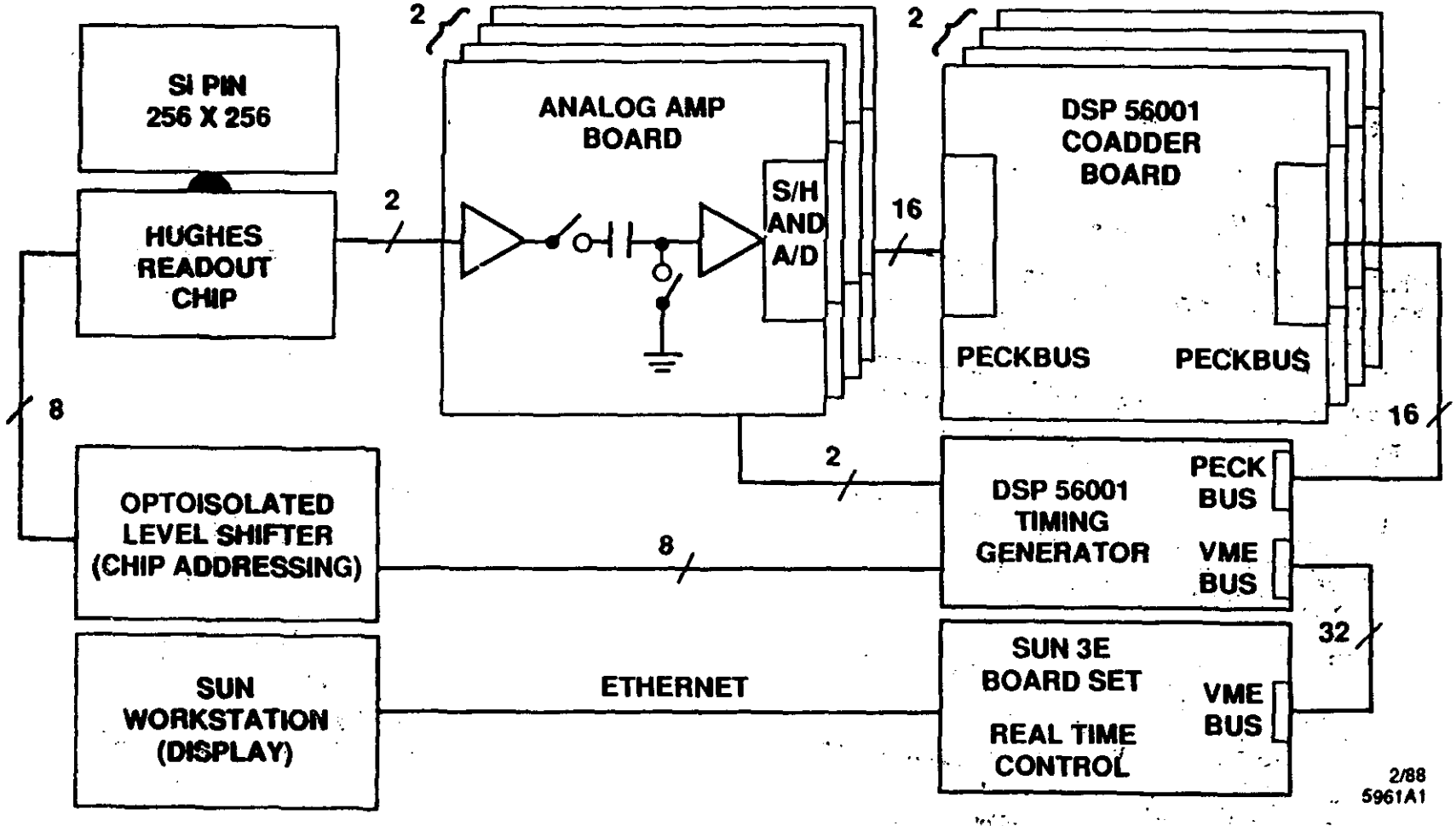


Figure 6.10 A Three Dimensional Plot of A Number of Minimum Ionizing Particles Incident on A Detector Array Demonstrating Excellent Signal-to-noise And the Power of Two Dimensional Arrays to Eliminate Confusion in Complex Events.

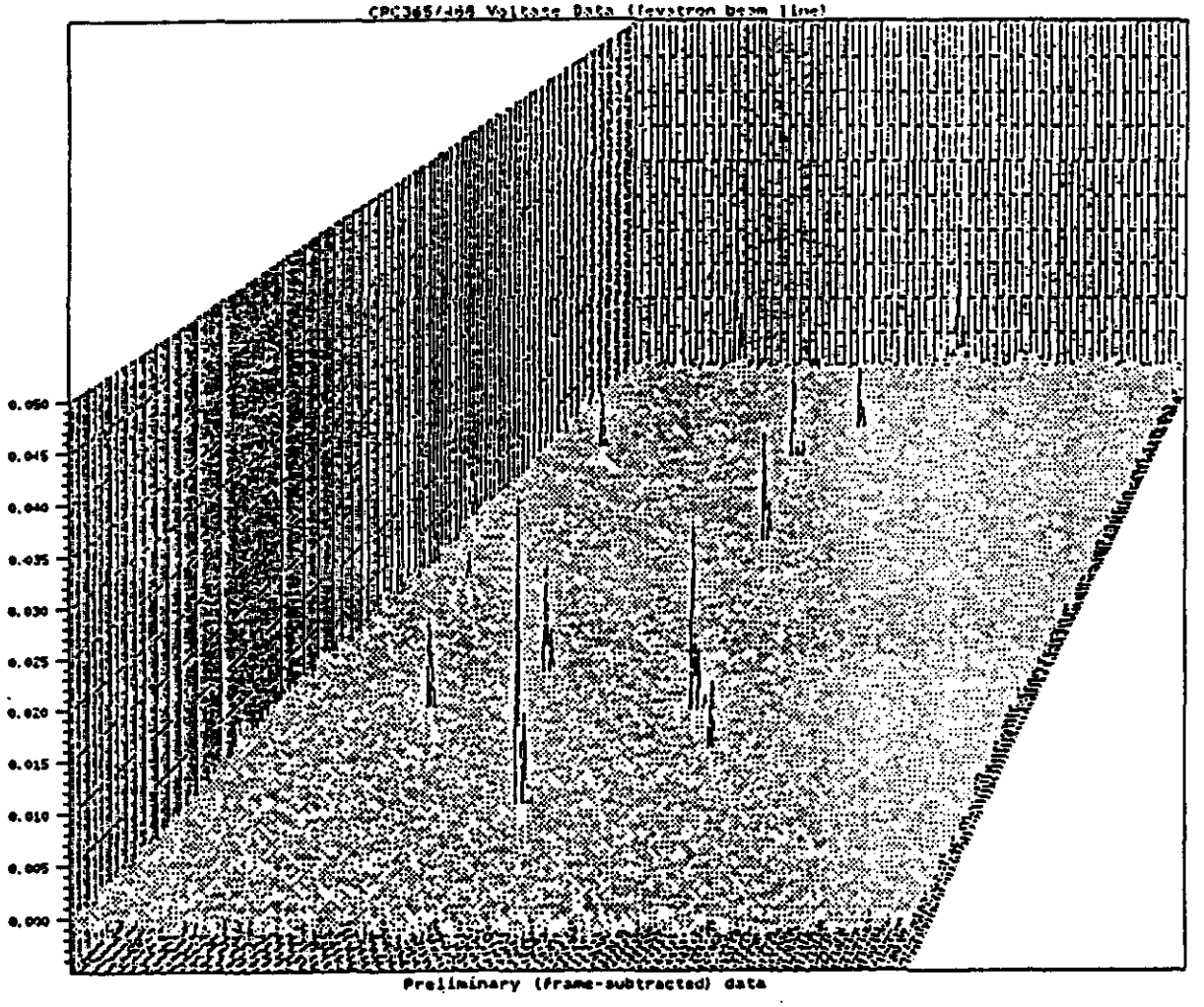
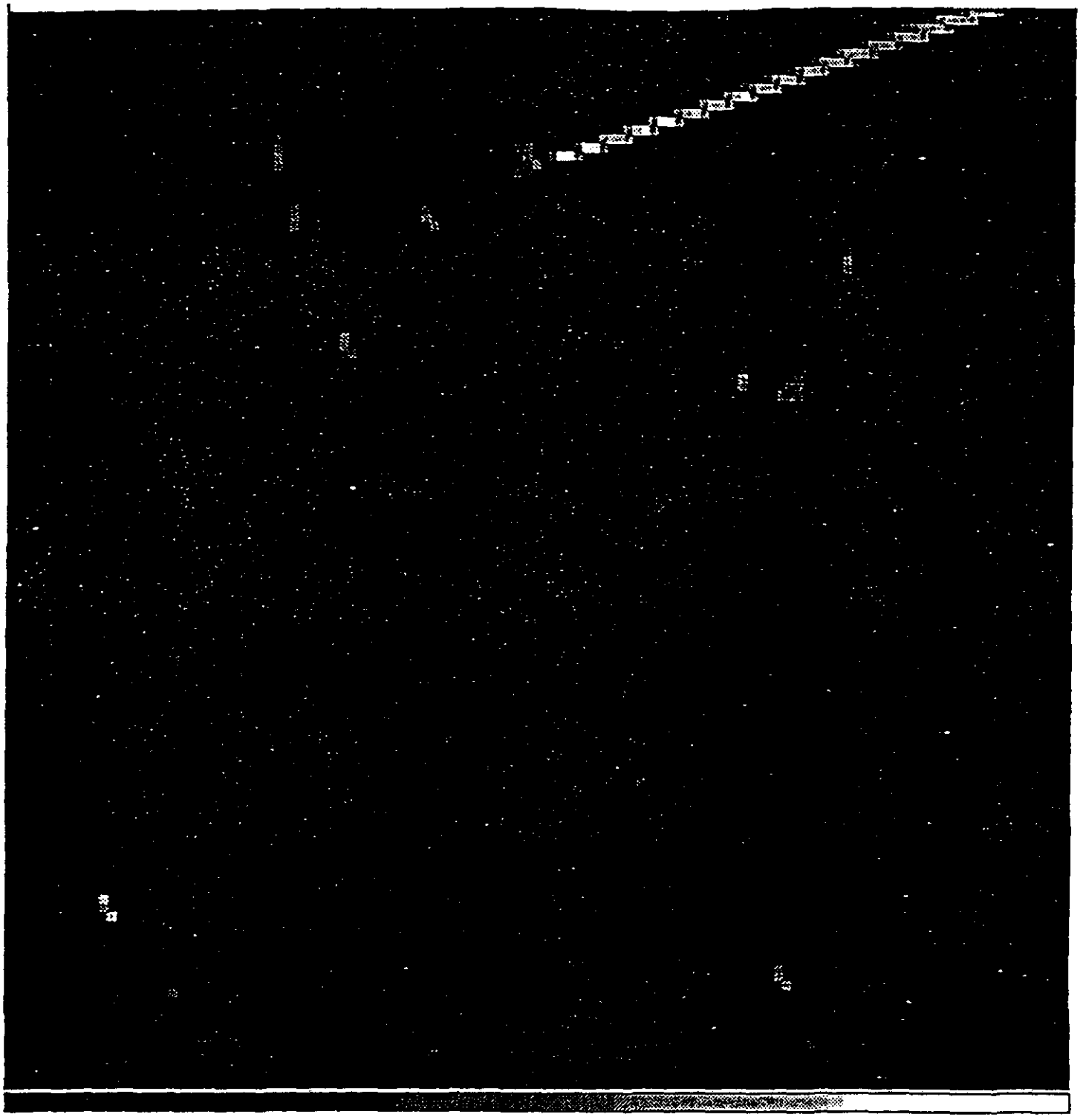
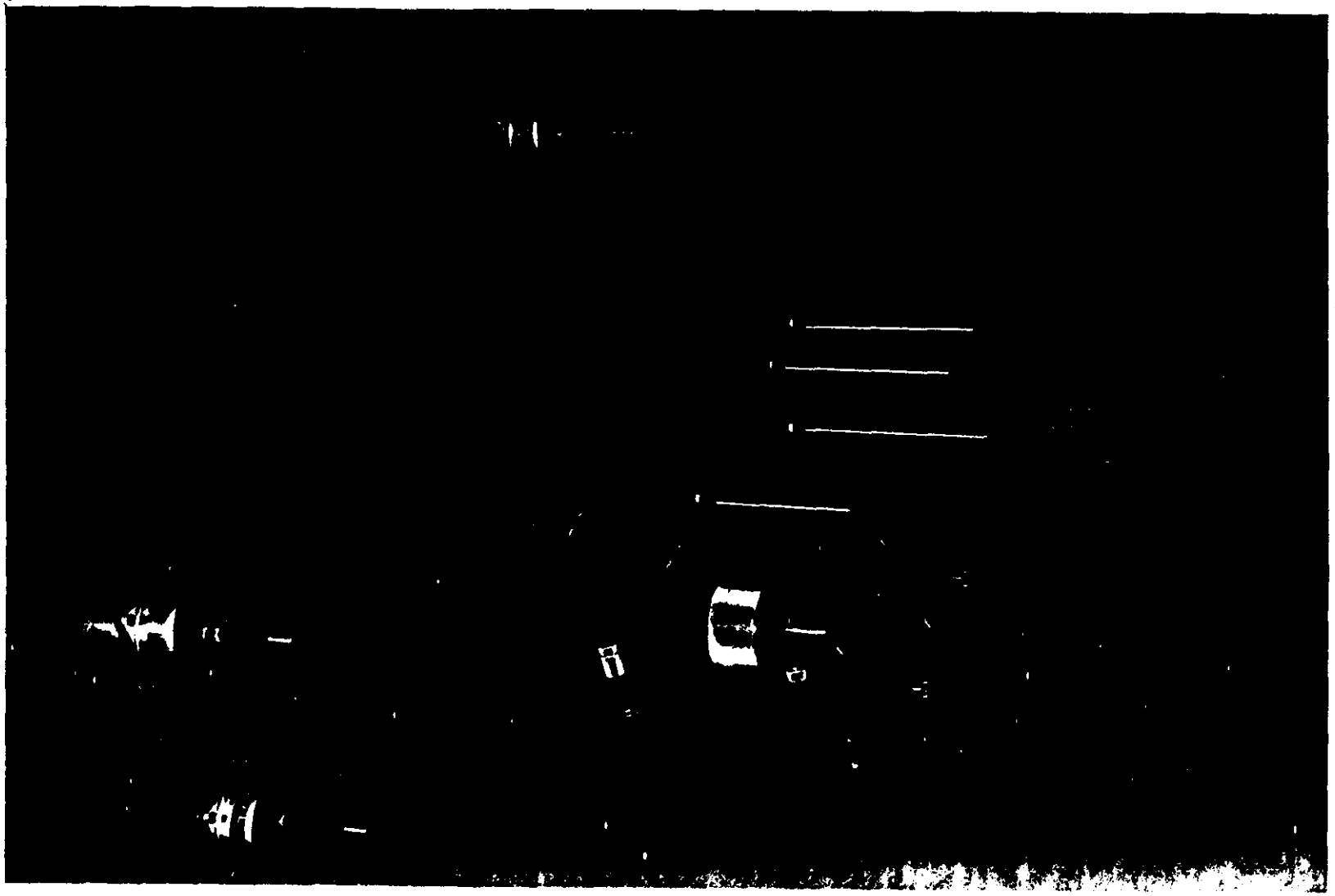


Figure 6.11 A Two Dimensional Plot of A Minimum Ionizing Track Traversing the Detector Array at an Angle, Demonstrating Potentially Excellent Spatial Resolution .





PIXEL DETECTOR DEVELOPMENT COLLABORATION

- Hughes Aircraft Co.

  G. Kramer, C. Pfeiffer, B. Wheeler, J. Gates, S. Augustine, T. Collins, O. Barkan, S. Worley, G. Atlas, G. Yacoub, D. Wolfe

- Lawrence Berkeley Laboratory

  D. Nygren, H. Spieler, S. Holland, M. Wright

- University of California - Berkeley Space Sciences Laboratory

  E. Arens, G. Jernigan

- Stanford Linear Accelerator Center

  S. Shapiro

- University of Pennsylvania

  N. Lockyer

- University of Oklahoma

  J. Gutierrez, P. Skubic

- University of California, Davis

  D. Pellett

- Yale University

  P. Karchin

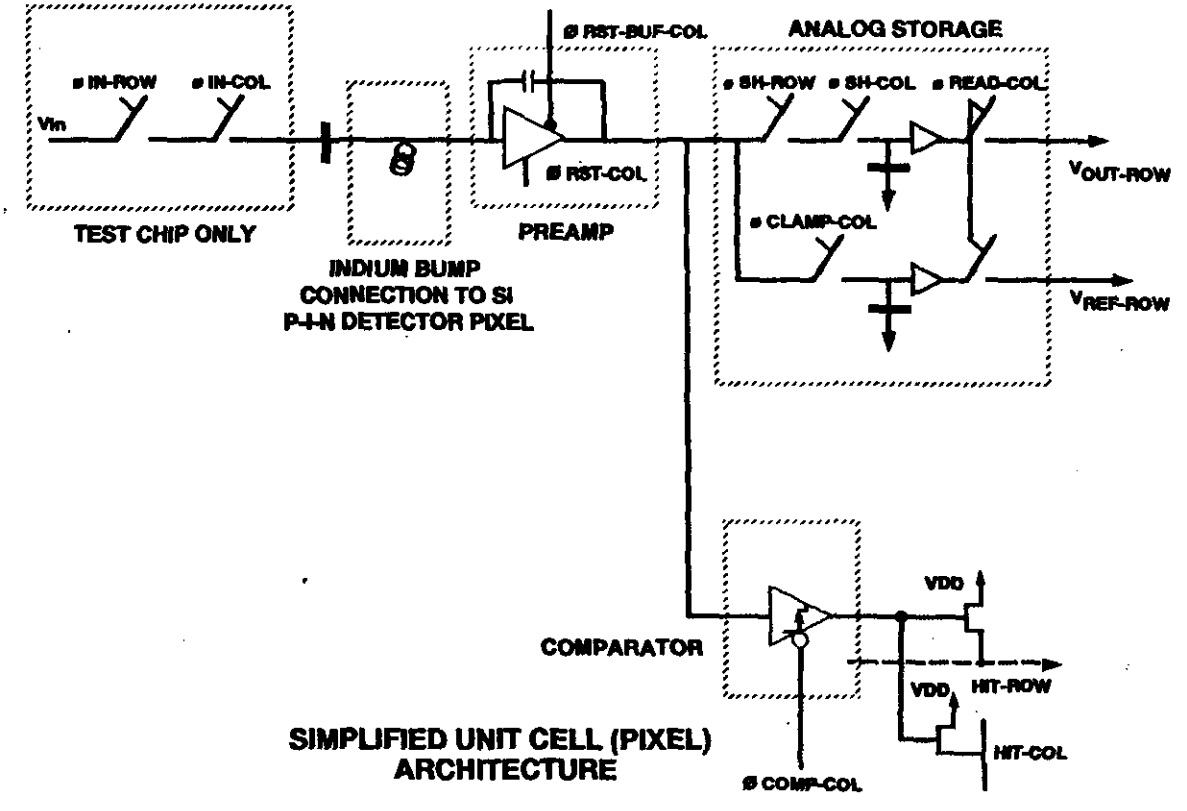
- University of Washington

  P. Mockett, V. Cook

PIXEL PROTOTYPE UNIT CELL FOR SMART SPARSE READOUT

HUGHES

12504-CV1 MC97



SIMPLIFIED UNIT CELL (PIXEL) ARCHITECTURE

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PIXEL DETECTOR READOUT DESIGN PERFORMANCE REQUIREMENTS

SPECIFICATION	PROTOTYPE	GOAL
NOISE	≤ 200 e^- rms	≤ 200 e^- rms
PIXEL SIZE	50 μm x 150 μm	40 μm x 40 μm
SPARSE SCAN	YES	YES
SELF CLOCKING	YES	YES
PRIORITY SELECTION	YES	YES
NEIGHBOR READOUT	YES	YES
TIME RESOLUTION	≤ 50 ns	16 ns
TIME STAMP	16 ns	16 ns
READOUT SPEED	≤ 10 μs	1.5 μs
ARRAY SIZE	32 x 64	512 x 512 (1 in^2)
RADIATION HARDNESS	NO	10 MRAD
TECHNOLOGY	1.2 μm CMOS	0.5 μm SOS/CMOS
CLOCK SPEEDS	>100 MHz	1 GHz (MAX)
FILL FACTOR	NA	≥ 94%
POWER	≤ 20 μW/Pixel	≤ 1 WATT/CM^2

UNIT CELL (PIXEL) SUMMARY

A. BASIC PIXEL:

20 FETS
4 CAPS
17 LINES

4 POWER RAILS,
3 BIASES
6 CLOCKS
4 OUTPUTS

B. FOR TEST PURPOSES:

2 FETS
1 CAP
2 LINES

C. RESULTS:

NOISE	~150 e^- (rms)
POWER	~18 μW
RESPONSE	≤ 50 ns
SIZE	50 μm x 150 μm
DEAD TIME	400 ns
FEEDBACK CAP	10 fF
OPEN LOOP GAIN	200

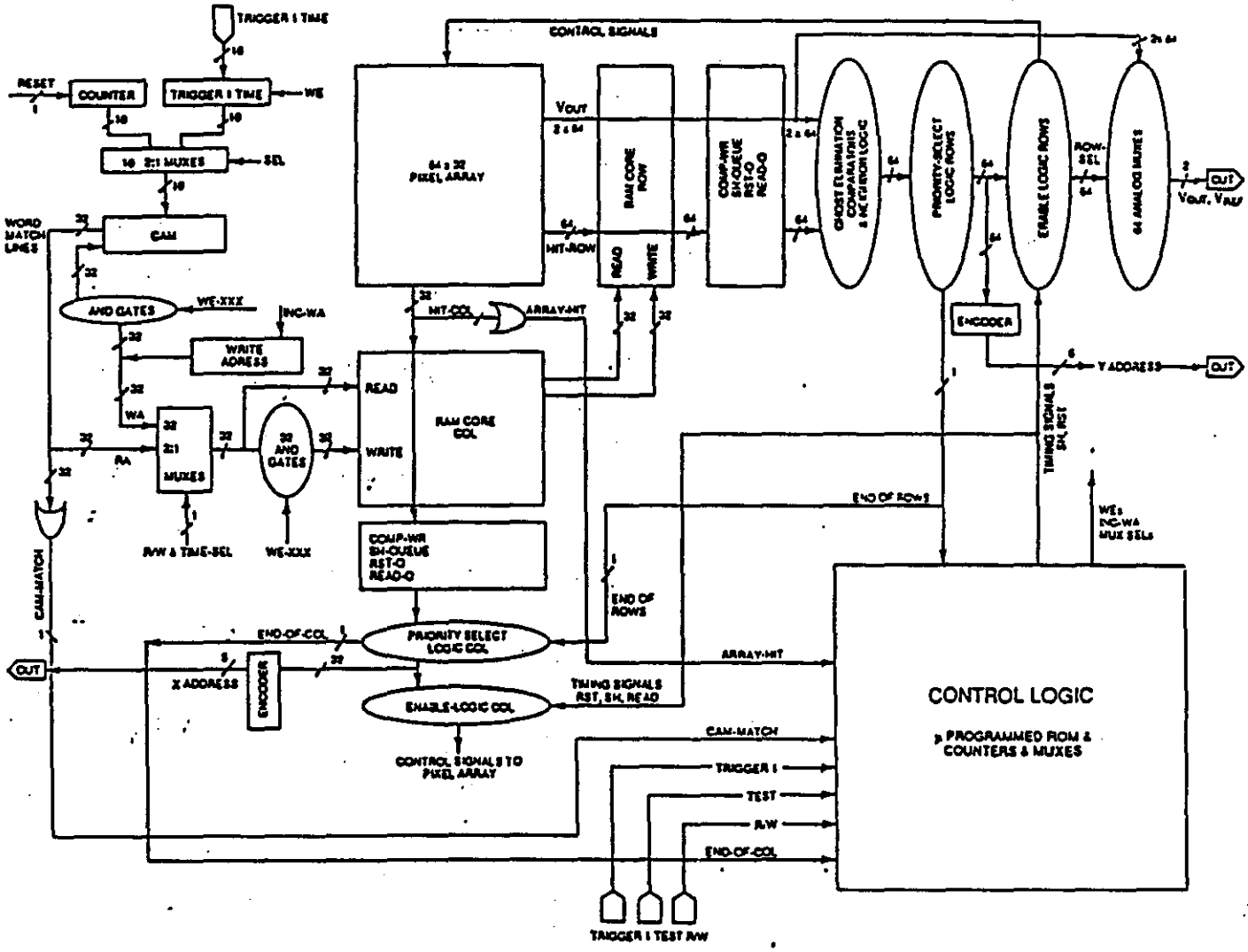
D. MISCELLANEOUS:
PRESENTLY FABRICATED IN 1.2μm SINGLE POLY-DOUBLE METAL (pitch=3.5 μm) CMOS PROCESS

100 MHz OPERATION AT ROOM TEMPERATURE FOR WORST CASE PROCESSING CONDITIONS

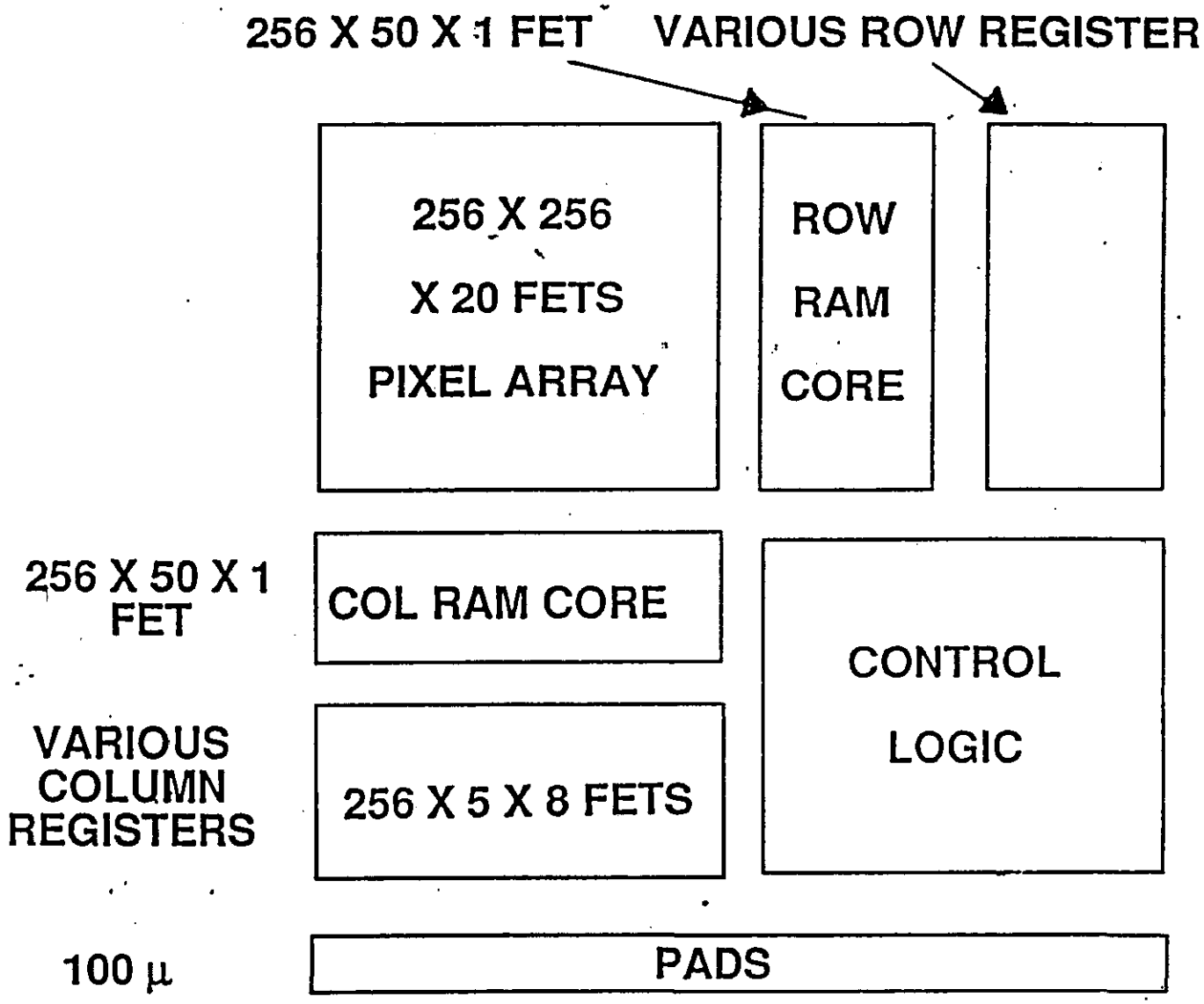
CONTAINS TRANSIMPEDANCE AMPLIFIER, CHARGE STORAGE, ANALOG BUFEFERING, FAST COMPARATOR

IN GOD WE TRUST

Pixel Detector SSC Prototype Architecture.



FILL FACTOR



256 x 20 = 5120 FETS / COLUMN IN PIXEL ARRAY

50 X 1 = 50 FETS / COLUMN IN COL RAM CORE

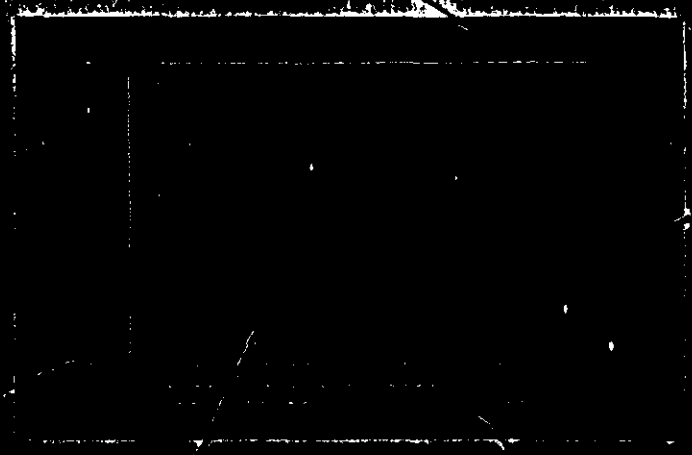
5 X 8 = 40 FETS / COLUMN IN COL REGISTERS

$\% \frac{90}{5120} = 1.75\%$ FILL FACTOR = $\frac{100X100}{102X102} = 96\%$

WITH PAD AREA => 94%

Test Chip Under Evaluation

HUGHES



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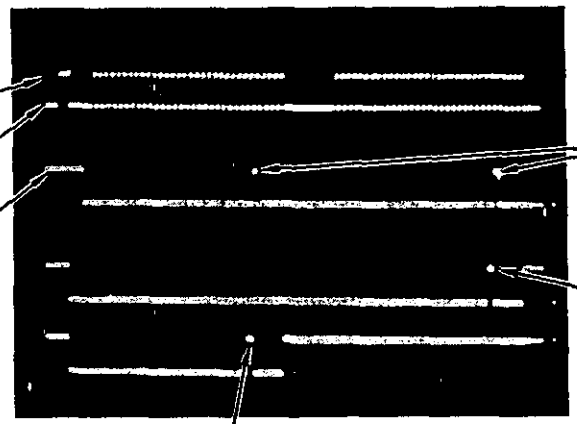
Test Chip Illustrates Smart Readout

HUGHES

12496

Input simulated hit ($\Delta Q = 5000\ e^-$) in pixel at position column 5, row 5



- Array indicates hit at specific time
- Hit pixel information outputted to memory
- Analog information stored in unit cell for later retrieval

Thinned Readout for Minimum Mass

HUGHES

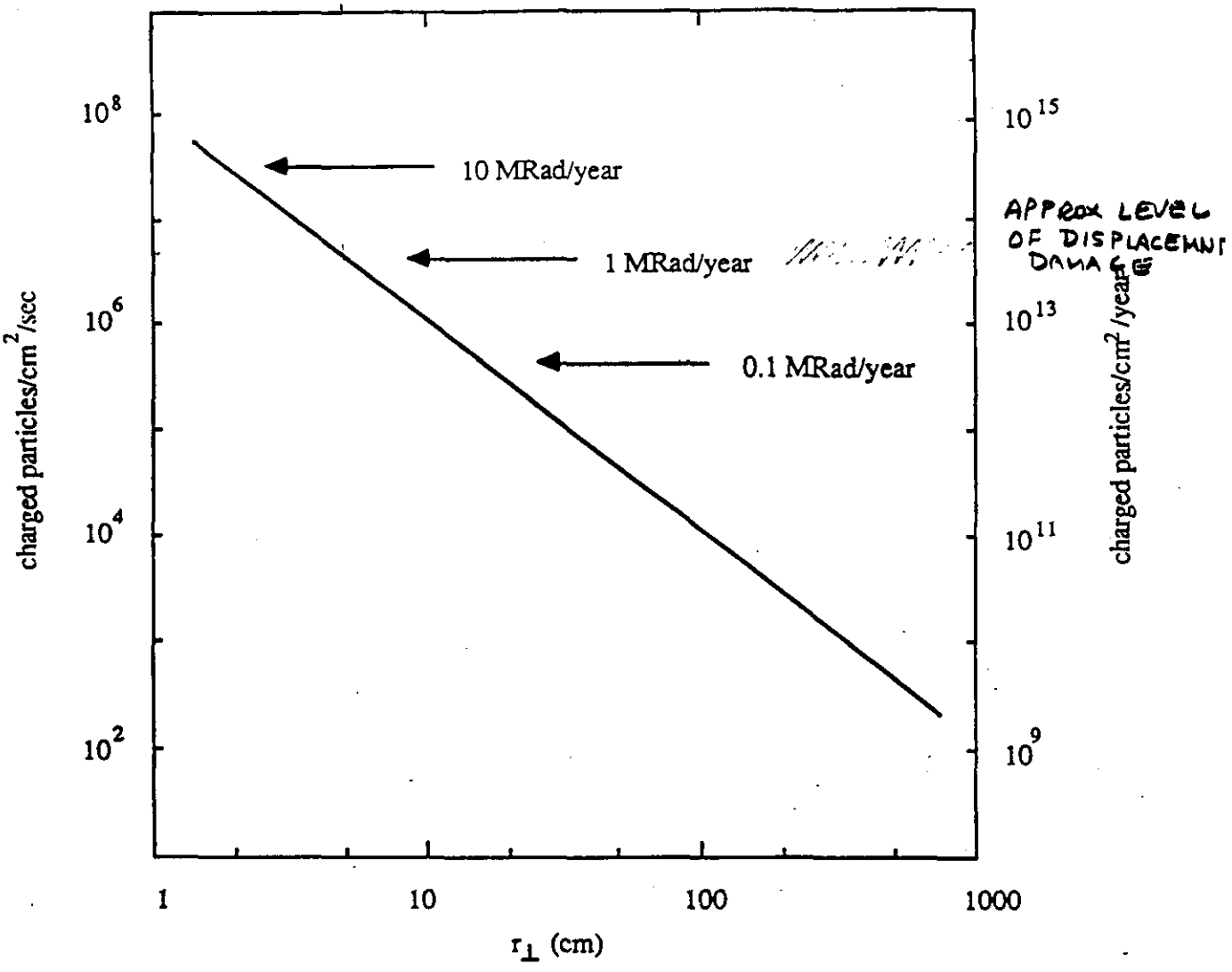
Pixel detector hybrid

Detector

Readout

Thickness reduced

from 300 μm to 50 μm



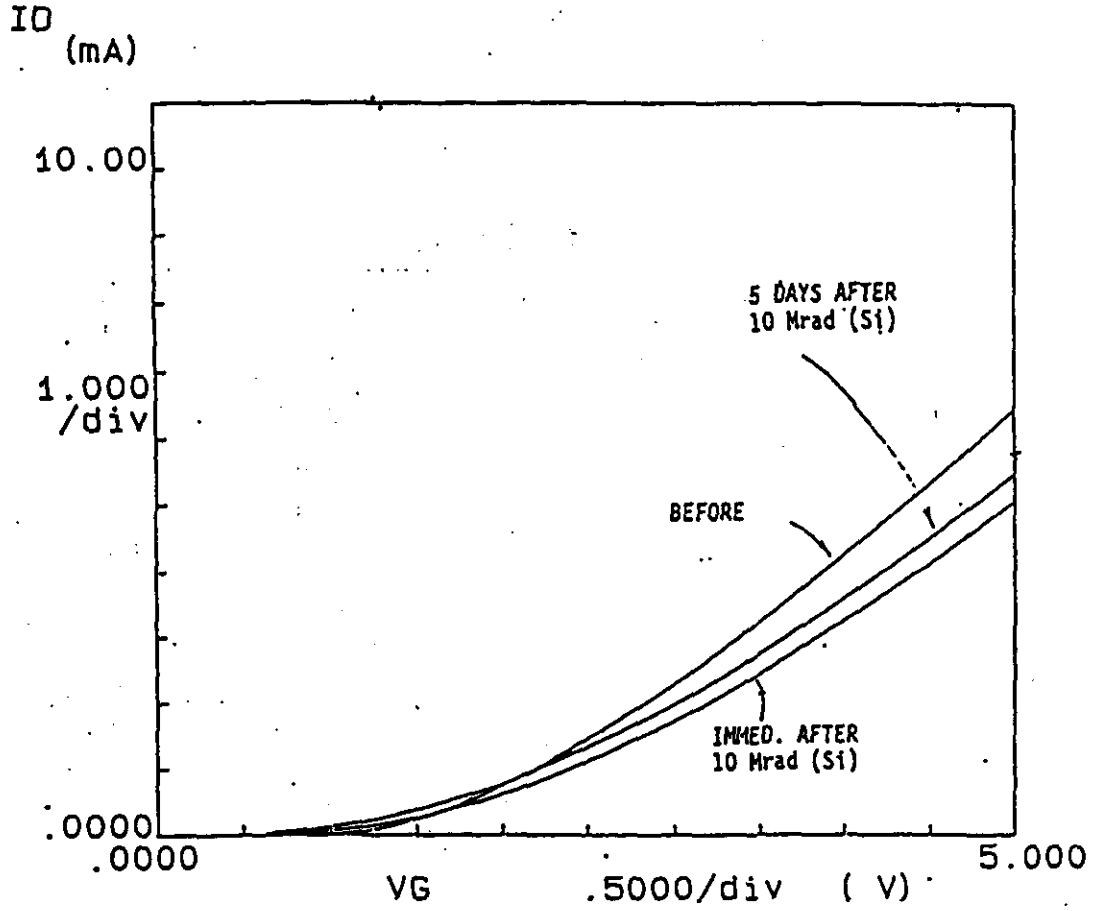
Charged particle rate at $L = 10^{33} cm^{-2} s^{-1}$.

NEUTRON FLUENCE $\cong 2 \times 10^{12}$ n/cm^2 yr + "reflection"

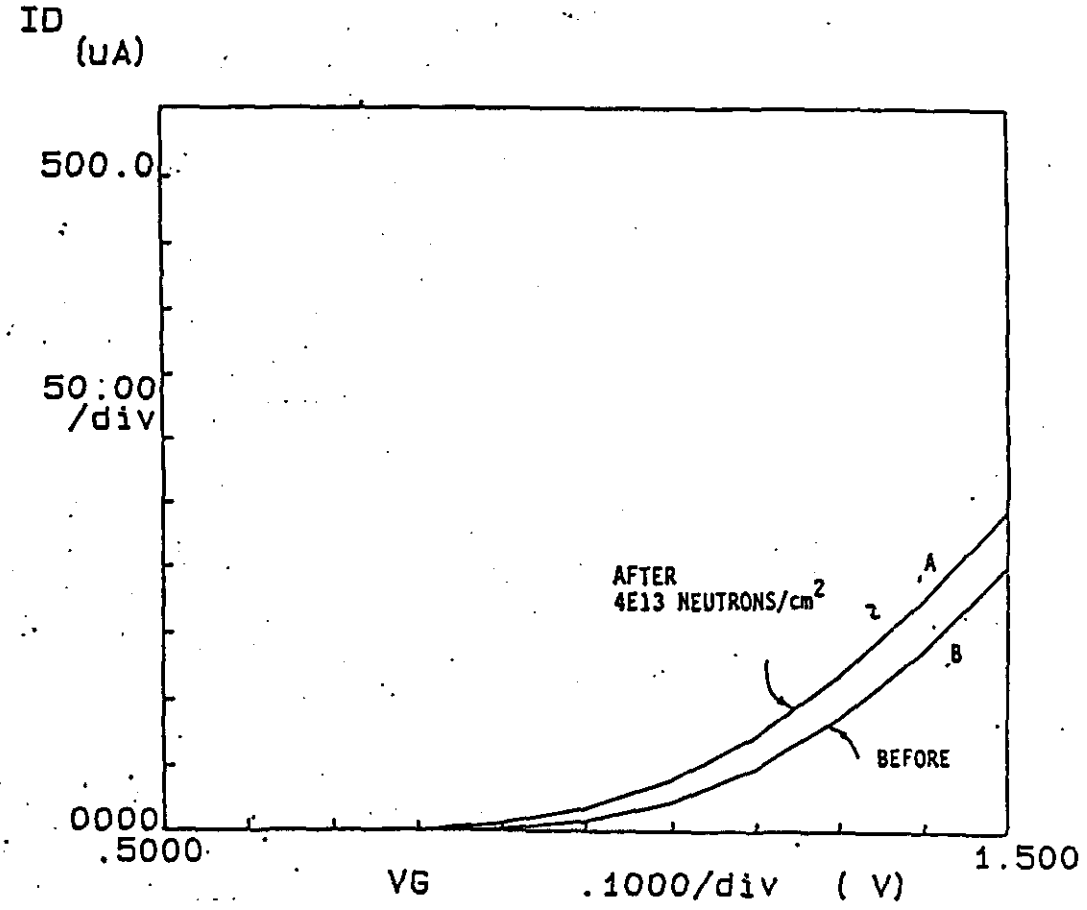
$\cong 10^{13}$ n/cm^2 yr

Photon FLUENCE $\cong 10^{12}$ γ/cm^2-yr

EFFECT OF NEUTRONS: $\frac{N}{e} \cong 30$ $\frac{N}{p} \cong 6$



Performance Characteristics of a Hughes BIMOS NMOS Transistors Before and After 10 Mrad Si Shows Satisfactory Operations at this Radiation Level.



Performance Characteristics of a Hughes BIMOS NMOS Transistor Before and After 10^{13} n/cm^2 (Average 2.5 MeV) Shows Satisfactory Operation at this Radiation Level.

TYPE INVERSION IN SILICON DETECTORS

D. PITZL et. al.

SCIPP 91/05

July 1991

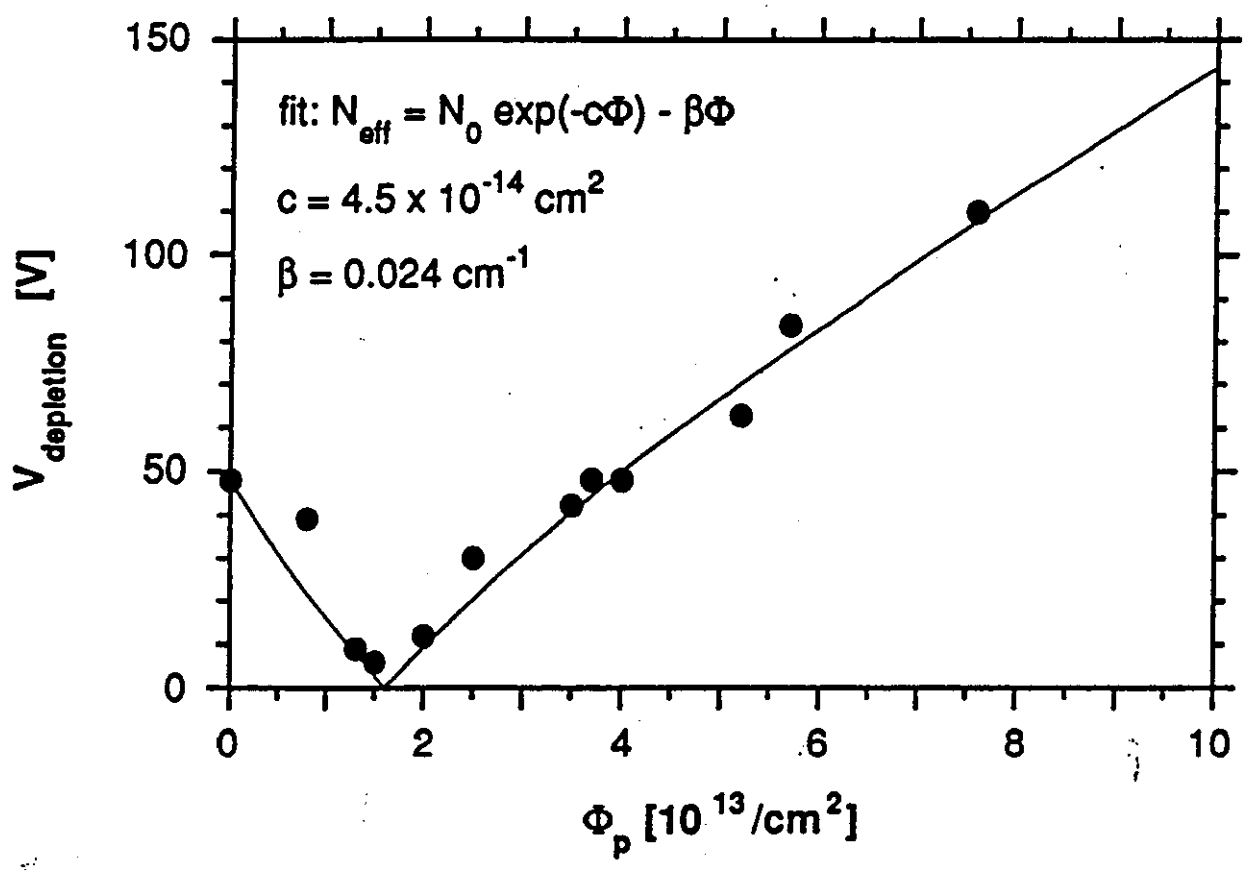


Fig. 9. Depletion voltage versus proton fluence for SI detectors. Type inversion occurs at $\Phi = 1.5 \cdot 10^{13}/cm^2$. *The line is the best fit according to equations (1) and (2).*

CMOS/SOI HARDENING AT 100 MRAD(SiO_2)

J.L. Leray, E. Dupont-Nivet, J.F. Péré, Y.M. Coïc, M. Raffaelli
CEA, Centre de Bruyères-Le-Châtel,BP-12, F91680-Bruyères-Le-Châtel, France
and
A.J. Auberton-Hervé, M. Bruel, B. Giffard, J. Margail
CEA, 85X, F38019, Grenoble, France

Abstract

Hardened CMOS/SOI 29101 microprocessor, elementary cells and transistors have been irradiated at levels between 10 Mrad(SiO_2) and 1 Grad(SiO_2) (^{60}Co and 10 keV x-rays). SIMOX buried oxide behavior in the range of 100 Mrad(SiO_2) and a channel-stopped MOS/SOI structure avoiding lateral leakage current are presented. These two items indicate the feasibility of a CMOS/SOI technology operating in the hundred Mrad(SiO_2) range.

I. Scope of the Study

A. Need for Very High Total Dose Levels.

10 to 100 Mrad (SiO_2) (or above) of total dose hardness must be considered in domains such as :
1) Core instrumentation in nuclear power reactors (containment accident may lead to 100 Mrad(SiO_2) or above [1,2]),
2) Control electronics and actuators in space-based nuclear power generators,
3) Reaction chamber instrumentation for future super particle colliders,
4) Tokamak fusion reactor instrumentation [3].

These very high levels may be associated with high-temperature environments [4] that might give S.O.I. particular advantages over standard GaAs or hardened CMOS-Bulk devices : very reduced active volumes and full insulation provide smaller junction leakage current even at 300°C [5].

B. The Irradiation Condition Dilemma.

For very high dose assessments, irradiation time is a key parameter. This paper aims at exploring the 100 Mrad(SiO_2) domain. For that purpose, there must be a trade-off between irradiation duration and dose rate : at 10 rad(SiO_2)/s, which is typical under normal radiation exposure, 100 Mrad(SiO_2) represents a third of a year. Such a duration is excessive and cumbersome.

0018-9499/90/1200-201

Thus, very high dose testing requires a high dose rate. If the test is performed in a short time, MOS threshold voltage may recover or rebound due to charge detrapping and interface state build-up or recovery. Therefore, the reliability of the test is distorted. This precludes a priori the exclusive "high dose rate" tests. A utopia would consist of a test duration equal to the operational lifetime.

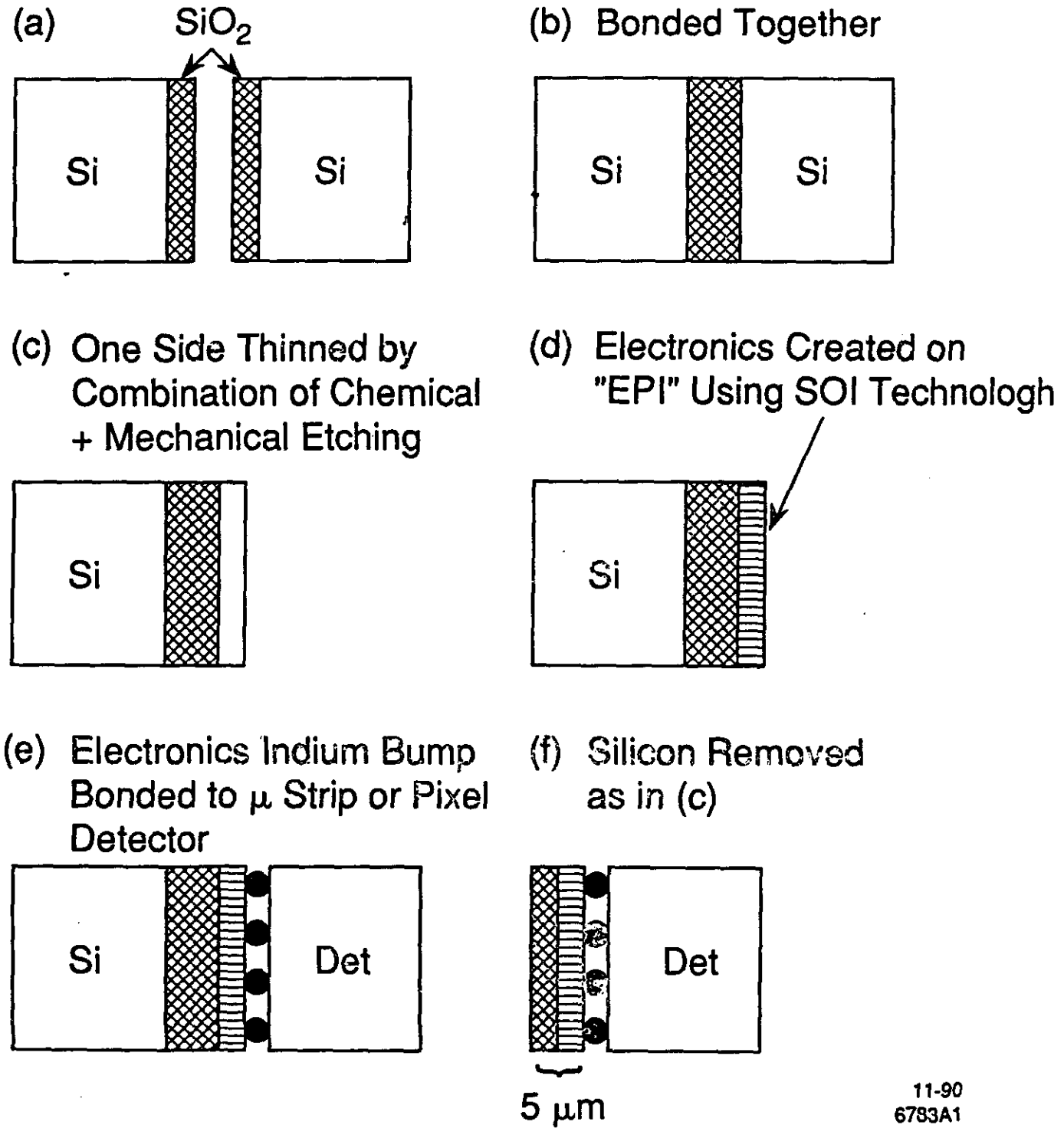
A trade-off must be found. As CMOS/SOI consists of front thermal oxide, buried oxide, and lateral insulator, there might be discrepancies for recovery kinetics among them. A special study must be done in each cases.

THE FORESIGHT 1 CELL HAS BEEN FABRICATED IN AN SOS/CMOS TECHNOLOGY.

WE HAVE TEN DEVICES AND ARE HAVING THEM BONDED THIS MONTH.

I WILL BE TESTING THEM THIS YEAR AT SLAC.

THEY SHOULD BE HARD TO BETTER THAN 1 MRAD.


(a)
SiO_2
Si
Si
(b) Bonded Together
Si
Si
(c) One Side Thinned by Combination of Chemical + Mechanical Etching
Si
(d) Electronics Created on "EPI" Using SOI Technologh
Si
(e) Electronics Indium Bump Bonded to μ Strip or Pixel Detector
Si
Det
(f) Silicon Removed as in (c)
Det
5 μm
11-90
6783A1

WHY A PIXEL VERTEX DETECTOR ?

* MORE RADIATION HARD THAN MICROSTRIPS BY VIRTUE OF THEIR SMALL SIZE.
  INITIAL S/N = 120 : 1

* THE INNERMOST BARREL OF PIXELS CAN BE PLACED AT A SMALLER RADIUS THAN CAN STRIPS, e.g. 5 CM. RESULTING IN LESS EXTRAPOLATION ERROR.

* A PIXEL VERTEX DETECTOR WILL HAVE LESS MASS, SINCE EACH PIXEL LAYER IS EQUIVALENT TO AT LEAST TWO LAYERS OF STRIPS (THREE ?)

* THE COST IS APPROXIMATELY THE SAME AS STRIPS, SINCE THE AREA COVERAGE IS SO MUCH LESS.

* A FEW CLEAR, HIGH RESOLUTION TWO DIMENSIONAL DATA POINTS ALLOW UNAMBIGUOUS ROAD FORMATION FROM THE INNER RADIUS OUTWARD TO LARGER RADII. 10 MICRON RESOLUTION IMPLIES < 200 MICRON ERROR AT A RADIUS OF ONE METER.

* HYBRID TECHNOLOGY ALLOWS REPLACEMENT OF THE PIN DIODES, WHILE RETAINING THE READOUT ARCHITECTURE.

HYBRID SCHOTTKY FPA HISTORY
- HUGHES -

HUGHES

7760-SP9 MC18

DESIGN	ARRAY SIZE	PIXEL SIZE	READOUT	YEAR
CRC-205	58 x 62	75 x 75 μm^2	SCCD / GM	1982
CRC-228	58 x 62	75 x 75 μm^2	DRO / SFD	1983
CRC-234	128 x 128	50 x 50 μm^2	DRO / SFD	1984
CRC-304	256 x 256	30 x 30 μm^2	DRO / SFD	1985
CRC-350	256 x 256	30 x 30 μm^2	DRO / SFD	1986
CRC-352	24 x 400	24 x 24 μm^2	DRO / SFD	1986
CRC-365	256 x 256	30 x 30 μm^2	DRO / SFD	1986
CRC-389A	244 x 400	24 x 24 μm^2	DRO / SFD	1987
CRC-389B	512 x 512	20 x 20 μm^2	DRO / SFD	1987
CRC-412	488 x 640	20 x 20 μm^2	DRO / SFD	1988

IS THIS TECHNOLOGY REAL ?

* THERE ARE MANY EXAMPLES OF EXISTING ARRAYS FOR DETECTION IN THE INFRA RED, OF X-RAYS, AND CHARGED PARTICLES.

* 256 X 256 ARRAYS HAVE BEEN DETECTING CHARGED PARTICLES FOR YEARS.

* A TELESCOPE OF THREE 256 X 256 ARRAYS WILL BE PLACED IN A FERMILAB BEAM NEXT WEEK.

* <u>NON-RAD HARD</u>, <u>SMART</u> ARRAYS HAVE BEEN FABRICATED AND TESTED. (FORESIGHT 4)

* FORESIGHT 5 - THE IMPROVED ARRAY HAS BEEN FABRICATED, AND IS BEING TESTED.

* A <u>RAD HARD</u> <u>SMART</u> PIXEL CELL HAS BEEN FABRICATED IN SOS/CMOS AND IS BEING PREPARED FOR TESTING. (FORESIGHT 1)