GEM IN-92-4

Electronics Cost Review

April 23, 1992

Abstract:

Agenda, attenders and presentations of the GEM Electronics Cost Review Meeting held at the SSC Laboratory on April 23, 1992. Agenda items included: Review of Costing Method; Costs by Subsystem; Discussion of IPC Costs; Discussion of CSC Costs; Level 2 & DAQ Costs; Plans for DAQ Design Work; Si Vtx Electronics Costs; Per-channel Cost Summaries & Discussion; and Plan for the Future.

PRELIMINARY Agenda for GEM Electronics Cost Review

Thursday, April 23, 1992 at the SSCL

		Discussion Leader
9:00 AM	Introduction, Review of Agenda	Sanders
9:15 AM	Review of Costing Methodology	Marlow
10:00 AM	Costs by Subsystem IPC's, Calorimeter, Muons, Level 1 Trigger	Lau
11:00 AM	Discussion of IPC Costs	Musser
11:30 AM	Discussion of CSC Costs	Polychronakos
12:00 PM	Lunch	
1:00 PM	Level 2 & DAQ Costs (current status)	Marlow
1:15 PM	Plans for DAQ Design Work	Botlo
1:45 PM	Si Vtx Electronics Costs	Hahn/Mills
2:45 PM	Per-channel Cost Summaries & Discussion	Marlow
3:15 PM	Plan for future work	Sanders
3:45 PM	Adjourn	

Note: In general the format will be one of informal discussion. Those wishing to raise and discuss particular questions may want to bring along supporting materials (write-ups, slides, etc.)

Electronic Cost Models

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GEM Electronics

LeCroy Corporation

April 22, 1992 10:30 PM

1. Introduction
2. Generic development and production costs
3. Support systems in the experimental hall
4. Resistive Plate Chambers
5. Barrel Muon chambers
6. Endcap Muon chambers
7. Inner central tracker (Silicon strips)
8. Outer central tracker (interpolating pads)
9. Calorimeters
10. Pre-Radiator
11. Trigger systems
    a. Muon chambers
    b. Calorimeter

1. Introduction

All parts of this detector must operate at the SSC beam crossing rate of 60 MHz.

The 1st level trigger must be deadtimeless (fully pipelined). The design goal for the Level 1 trigger output rate is 10 KHz. If necessary, an intermediate "Level 1.5" trigger stage will be added to accomplish this. To provide an operating margin, all detectors must be designed to accept Level 1 triggers at an average rate of 100 KHz. The muon system, the calorimeter, and at least part of the central tracker must digitize at this rate, to provide the data required by the Level 2 trigger. A pipelined delay of up to 3 microseconds is required in every signal channel to accommodate the Level 1 trigger delay, and an asynchronous buffer must be provided for the Level 2 delay, where required. All systems which participate in the 1st level trigger decision must identify the beam crossing uniquely. Initially, only the calorimeter and the muon systems will be used in the Level 1 trigger. This beam crossing information determines which of the pipelined signals are digitized and stored.

The 2nd level trigger will be designed to achieve an output rate of 300 Hz or less. To allow for design margin, the readout into Level 3 must be designed to accept events at a rate of 3 kHz. For each accepted 2nd level trigger, any remaining detectors are read out and the entire event is submitted to the Level 3 trigger, which will be a processor farm.

All systems will have test and calibration facilities included as part of the system design. These will allow quick verification of function in all cases and provide a complete calibration for some. This detector must operate reliably for many years. The approach to the electronics design reflects our concern for serviceability of the components. The calorimeter and muon electronics are located where access is possible. Only the minimum electronics is located in the detector, where access time is measured in weeks, not hours or minutes. Those components which must be inaccessible, the calorimeter preamps, and the central tracker, must be designed and tested for reliability. Redundant components and communication paths must be designed in at the system level, to permit slow degradation of performance rather than catastrophic failure.

This estimate is for contruction costs and therefore assumes that a conceptual design has been completed and that outstanding R&D issues have been resolved. This estimate does, however, include the cost of implementing a prototype version of each subsystem to be implemented. The prototype systems are assumed to compromise a number of channels that is the smaller of 10% of the final subsystem channel count or 1000 channels. Most of the engineering costs are incurred in this phase of the work. The reliability of these estimates will depend on the extent to which the relevant technologies are understood. Systems that require extensive R&D have been assigned higher technical-risk factors in the contingency analysis.

For each system, a straw-man design has been chosen, which is based on available technology, or modest extrapolations thereof, to the extent possible. The final design may be different from that described here. These estimates are best described as top-down, using analogies with existing systems, rather than a full bottom-up approach. The rate of change in electronics technology is rapid enough that a bottom-up estimate based on current technology is inappropriate at this stage of the detector design.

2. Generic development cost used in the cost estimates

These generic items are taken from the EMPACT/TEXAS cost estimate, with some additions and modifications. They have been reviewed here at LeCroy and are still considered to be a reliable guide to development and production costs. The original caveats also still apply, these costs are a guide only in the case of well understood systems, not necessarily correct for systems which are beyond the current state of the art.

The following estimates are based on a labor rate of $74. per hour ($154K per year). This is comparable to the fully burdened rate for an engineer or physicist at one of the national laboratories.

The cost of radiation hard ICs is estimated at twice normal ICs, both for development and production costs. This is supported by discussions with current vendors of radiation hard semiconductors. Note that It may be more difficult to achieve the required performance with radiation hard ICs.

	Engineering/design			EDIA		Prototype	Proc/Fab
Item	Labor my	Rate k$/my	Total k$	Material k$	Proc/Fab k$	Total k$	Material $/each
Simple IC	0.50	154	77.00	30	150	257.00	12
Simple IC, rad hard	1.00	154	154.00	60	300	514.00	24
Complex IC, digital	1.25	154	192.50	40	150	382.50	16
Complex IC, digital, rad hard	2.50	154	385.00	80	300	765.00	32
Complex IC, analog	2.00	154	308.00	40	150	498.00	50
Complex IC, analog, rad hard	4.00	154	616.00	80	300	996.00	100

For the complex analog chips, a special test station is required for production testing. This will be more thorough than normal semiconductor vendor testing. This will test all storage locations in a switched capacitor array, for example.

	Engineering/design			EDIA		Prototype	Proc/Fab
Item	Labor my	Rate k$/my	Total k$	Material k$	Proc/Fab k$	Total k$	Material $/each
Analog tester	1.00	154	154.00	50	50	254.00	16

The pc board production costs include all common parts, but not the special custom integrated circuits. This cost also includes assembly, test and calibration. We note that a standard FASTBUS board has a usable area of approximately 14**2 in**2, yielding a production cost of slightly less than $ 3000. Although GEM has not adopted FASTBUS as a standard, this estimate assumes that most rack-mounted electronics is implemented on boards of this approximate size.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/inch sq.
Simple PC board	0.55	154	84.70	4	16	104.70	8
Complex PC board	1.50	154	231.00	10	20	261.00	15

For the very high density systems in the central detector region, the component density required is similar to that currently found in systems using hybrid or chip-on-board construction techniques. The development effort for this type of construction is similar to a large complex pc board. The estimate of the generic cost is based on LeCroy's experience with a large hybrid TDC for a chamber mounted application. This estimate is an extrapolation to a highly automated production system. Note that the cost of working silicon is in the neighborhood of $500 per sq.in.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/each
Large hybrid chip	1.50	154	231.00	10	20	261.00	100

An alternative method of achieving the very high density required is to design monolithic ICs which incorporate all needed functions on the chip. Very few other components can then be used to achieve the high channel density required. The number of chips required depends on the number of different technologies, probably at least 2, since the preamplifier is expected to use bipolar technology. The analog storage and digital chips can be rad hard CMOS. The expected reliability of an all monolithic system, (with very few connections) is much higher than with hybrid techniques. With this packaging technique, the ICs are more complex, and their development and production costs must reflect this.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/each
High density surface mount PC board	1.50	154	231.0	10	20	261.00	30

3. Support systems in the experimental hall and other common items

a) High voltage for central trackers and muon chambers

The high voltage systems are very similar for several detector systems. We have assumed the use of commercial systems at a cost of $150 per channel, and $50 per channel for cable and connector costs. Since these are commercial systems, we assign little or no development costs.

b) Low voltage power for detector mounted electronics

The low voltage power supplies will be located in the hall, close to the magnet, but in an area where the field is less than 0.1 Tesla. Th transformers and other magnetic components must be shielded from the field, or designed to operate in a 0.1 Tesla field. The cost has been estimated at $4 per watt for the remote operation and monitoring) and $1 per watt for the cable distribution system. These estimates are based on actual costs of existing systems. Only a modest development cost has been assigned, since we expect these systems to be based on commercial offerings.

c) Optical fiber data links

We have used a generic optical data link for the purposes of this estimate. The cost is based on a currently available 80 Meter long link, rated at 125 MHz. We expect that higher performance at a similar price will be available in the SSC/GEM time frame. The production cost is $250 per link. This includes an optical transmitter ($88/each), optical receiver ($88/each), two ST connectors ($12), and 80 meters of multimode graded index fiber ($0.25/ft).

d) Optical fiber receiver and data buffer board

Similarly, the 32 channel receiver buffer board for the optical links is the same for all of the data (non trigger) links. The development cost is charged only once, and is $261k, the cost of developing a complex printed circuit board.

This receiver and buffer is the core of the data acquisition system. All subdetector systems send the data via an optical link to these boards. Most systems send the data after a Level 1 accept. The system is easily modified to accomodate those subdetectors which retain the data until the Level 2 trigger decision. The buffer structure is designed to store all data until transfer to Level 3, which occurs upon receipt of a Level 2 accept.

Each link receiver stores the data received in a FIFO buffer, a separate buffer for each link. The link protocol includes an end of event marker to separate multiple events. The data remains in the FIFO until the Level 2 trigger decision. Any data required by the Level 2 trigger is either copied to an output optical link as it is received, or a duplicate link is provided at the source. The event size at this FIFO is less than 1k bytes, so a 32k buffer will allow a Level 2 trigger delay of 300 microseconds.

At this time the data is either discarded, or transferred to a Level 3 FIFO buffer on the same board. The Level 2 acceptance rate is 3 kHz, or every 333 microseconds. There is only 1 Level 3 FIFO buffer per board. A local event building operation takes place, collecting all data for the accepted event from all Level 2 FIFOs. At the same time, a copy of the complete event is also sent to the Level 3 trigger system via a 32 bit parallel link. Note that the Level 3 trigger is working with a copy and does not need to save the data, nor does it need to use all the data. The maximum event size is 32k at this buffer level. A 1 Mb buffer will allow a 0.01 sec Level 3 trigger delay.

The Level 3 trigger decision causes this event to be either discarded, or read out via the backplane (FASTBUS for example) into a host computer, or directly to long term storage. A FASTBUS system would have more than adequate bandwidth for this task. A full FASTBUS crate will have a maximum event size of 600 kb.

e) Crates with power and controllers

The slot cost for rack mounted boards is based on the typical cost of a FASTBUS crate, with power and controller, $900. per slot. Note that this does not imply the use of FASTBUS, but does produce a more reliable estimate.

For the racks mounted near or on the magnet, this is increased by $600 to include the extra costs associated with liquid cooling and remote or magnetic field tolerant power supplies. The development costs associated with this are common to all crates of this type. This common development cost is charged only once.

f). Signal Cables

Note that cabling in the hall or in the detector is expected to conform to CERN rules for underground areas, i.e. it must be halogen free. The signal cable cost estimates are based on $0.3 / meter, the cost of shielded twisted pair cable.

The resistive plate chamber produces a spark promptly after the particle passage. The combination of the gas and the resistive plate promptly quenches the spark. A large positive charge is left in the gap, producing a large prompt induced signal on a pickup strip electrode. The strip can be designed as a terminated transmission line, requiring only a simple discriminator at the end of the strip to produce a signal with beam crossing timing. There is no drift time to consider. This is modified by the flight time from the vertex, but this can be mitigated by restricting the strip length. The result is a prompt signal that can uniquely identify the beam crossing.

This system satisfies two requirements. It provides a signal for the trigger without waiting for (or correcting for) the drift time. And it provides the z coordinate, as a higher resolution alternate to the time difference from the two ends of a drift wire. A TDC system, similar to the muon barrel system records the time for more precise off line analysis.

The RPC's are arranged in three layers, corresponding to the three superlayers of the barrel muon system. "Azimuthal" strips running parallel to the beam are used for triggering, and strips running perpendicular to the beam are used for z-determination. The non-bend-plane (i.e. z) strips are also placed in coincidence with the bendplane trigger strips to provide added immunity to accidental triggers.

The strips are grouped into 16 azimuthal sectors. The sectors of the first, second, and third superlayers, are subdivided into 111, 187, and 240, azimuthal strips, respectively. To reduce transit-time variations to an acceptable level, the azimuthal strips are divided into eight pieces along z. The z-divisions made in such a way as to be projective from layer to layer.

There are 322 z-strips for each layer of each sector.

The total number of strips is thus

$$N_total = 16 \times [8 \times (111 + 187 + 240) + 3 \times 332] = 84{,}800$$

Each strip provides input to the Level 1 trigger and to a TDC for offline performance monitoring and analysis. Since the TDC system used for the muon drift detectors (see section 5) can be used for the RPC strips, no prototype/development costs have been included. The cost of the Level 1 trigger processing logic for the RPC's is detailed in section 11.

Resistive Plate Chamber, 85k trigger signals

	Engineering/design			EDIA		Prototype	Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total	Material	
Item	my	k$/my	k$	k$	k$	k$	$/chan	$k total
Discriminator IC, 8 str/chip	0.50	154	77	30	150	257	1.5	128
Discriminator PC board, 4ch/sq.in	0.55	154	84.7	4	16	104.7	2	170
Cable to trigger system, 15 meters						20	4.5	383
Total						381.7	8.0	680

Resistive Plate Chamber, 85k TDC channels

Engineering/design	EDIA	Prototype	Proc/Fab

Item	Labor my	Rate k$/my	Total k$	Material k$	Proc/Fab k$	Total k$	Material $/chan	Material $k total
TDC chip 8 channels (same as drift-wire system)							2	170
TDC PC board, 128 TDC/board, 1.5 sq. inch/channel (same as drift-wire system)							22	1870
Crate slot cost, special rack, remote power, 1500/board							12	1020
Total							36	3060
32 readout and comm. links, one for each sector, 80m							250ea	8
Total								8
Low voltage power, less than 100mw/channel, 10 kW total							5/watt	50
High voltage power, 256 channels							150	38.4
Cables							50	12.8
Total								101.2

5. Muon Barrel System

The barrel section will use long drift wires, in either limited streamer or proportional mode. The candidates are limited streamer wires at atmospheric pressure, with an open rectangular cell geometry, and proportional mode wires in pressurized circular drift tubes. In both cases the drift time is the quantity to be measured. The time digitizing resolution (least significant bit, LSB) must be 1 nsec or less. By connecting adjacent (but not overlapping) wires together at the far end, and using one TDC per wire (i.e. two per connected pair) we can use the time difference to determine the Z position with better than 15 cm resolution. The time sum will determine when the avalanche occurred, automatically correcting for the propagation time along the wire.

Task list:

1) preamplifier/ discriminator mounted on the chamber. For the limited streamer mode chambers, the discriminator is mounted directly on the chamber, driving differential wires to the TDC cards. For the proportional mode wire case, It may be necessary to separate the preamplifier and discriminator, at least to the extent of separate cards, though possibly also chamber mounted. This may require a custom integrated circuit design.

2) cables to TDC racks mounted on the magnet pole face. This is a short cable run, less than 15 meters worst case.

3) pipeline tdcs. Currently available commercial TDCs use entirely digital techniques to achieve 1 nanosecond resolution (least count). This is a custom monolithic CMOS chip, which contains the timing and readout logic for 8 channels of multi-hit pipelined TDC. The full scale range is 65,000 counts, with 1 nsec least count. Up to 16 hits per channel are stored, with double hit resolution of 20 nsec. Although the readout properties of the existing chip are not perfectly matched to our requirements, no significant technological extrapolations are required to develop something suitable.

A new chip, with features and performance optimized for the GEM muon system, will be required. The expected improvements in IC processing in the SSC time frame will certainly allow cost, performance and power dissipation to be enhanced compared to the current circuit. This new chip will be designed as a pipeline TDC, with continuous time stamping readout. The pipeline nature of the circuit naturally provides storage of the timing data during the first level trigger delay.

4) crate by crate readout to the upper counting room. This cable run is at least 50 meters.

5) receiver/buffers for 100 optical fibers. Each channel requires a few thousand bytes of fast buffer.

6) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

Muon Barrel System, 133k channels

Item	Engineering/design Labor my	Rate k$/my	Total k$	Material k$	EDIA Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Preamp, 8 wires/chip (proportional mode only)								
	0.50	154	77	30	150	257	1.5	199.5
Discriminator IC, 8 wires/chip								
	0.50	154	77	30	150	257	1.5	199.5

Cable to TDC rack, 15M shielded twisted pair				20		20	4.5	598
Discriminator PC board	0.55	154	84.7	4	16	104.7	2	266
TDC chip 8 channels	1.25	154	192.5	40	150	382.5	2	266
TDC PC board,128 TDC/board, 1.5 sq. inch/channel	1.50	154	231	10	20	261	22	2926
Crate slot cost, special rack, remote power, 1500/board							12	1596
Total (proportional mode)						1552.2	44	6051
Total (limited str. mode)						1295.2	45.5	5851.5
54 readout and comm. links, one for each 2500 signals,80m							250ea	13.5
Receiver/buffer complex boards, 6 sq. inch/link							90	4.9
Rack slot space, $900/board							30	1.6
Total								20
Low voltage power, less than 200mw/channel, 26 kW total (proportional mode)							5/watt	130
Low voltage power, less than 100mw/channel, 13 kW total (limited str. mode)							5/watt	65
High voltage supply, 1000 channels							150	150
Cables						50		50
Total (proportional mode)								330
Total (limited str. mode)								265

6. Muon Endcap

This system consists of closely spaced (2.5 mm) anode wires, as in a standard proportional chamber, but with cathode-strip readout. Four layers are needed to achieve the required spatial resolution. This system is similar to the outer central tracker, but the expected rates are much lower, less than 200 Hz per square centimeter. Thus the pickup strips are bigger, resulting in larger capacitance and correspondingly longer shaping times (about 1 microsecond) for similar noise levels. The induced charge signal must be measured with 1% relative accuracy (channel to channel) to achieve the required resolution. The expected rates are quite low, so some sharing of ADC channels to reduce cost is possible.

A calibration system must be included to ensure the 1% relative accuracy for adjacent channels.

This system will be used in the Level 1 trigger, so that beam crossing resolution is required. It remains to be established whether or not simply using the first hit from the 4 planes of a superlayer will suffice to uniquely determine the beam crossing. If this is not the case, either RPC's or scintillators will be required.

There are three approaches to the readout being considered.

1) Using a variant of the Amplex chip designed at CERN. Either a switched capacitor array or stretcher (a sample hold, with a a self timed clear) is required for the 3 usec trigger delay. if a stretcher is used, a separate digital pipeline is required to record the beam crossing information.

2) Using a switched capacitor array directly as in the outer central tracker. The same system can be used. A prompt trigger output is required, however.

3) Use a time over threshold pulse and pipelined TDC. The analog information is encoded as a pulse width, with both edges recorded in the pipeline TDC.

All three approaches appear viable and the final selection will be based on ease of implementation (cost). For specificity we consider option 1 in what follows.

In principle, the integration time of the front end electronics could be used to provide the Level 1 delay---the slow pulse from the preamp output could be held on a storage capacitor upon receipt of a Level 1 trigger. This approach, however, couples the Level 1 latency time (2 mu-sec in GEM) to the integration time of the preamplifiers, which could lead to undesirable system constraints. Moreover, the long integration times would not permit reliable tagging of the bunch crossing, even in the offline analysis. Both of these problems will be addressed by incorporating digital pipelined logic based on the outputs of discriminators driven by fast-timing pickoffs from the preamplifiers. This logic will operate at the 60 MHz bunch crossing rate and will be used to generate local hold signals that cause the long-shaping-time outputs of the preamplifiers to be retained until the Level 1 trigger decision is available. At that point the analog storage elements can be further held if Level 1 is ''TRUE'' or cleared if Level 1 is ''FALSE''. The digital information will also be stored on a bunch-by-bunch basis for use offline.

Since strip occupancies are low, it is sufficient to combine sixteen of the digital channels into a single chain by ORing the discriminator outputs. Moreover, a single ADC can be used to readout several (here we assume 32) storage capacitors. The pipelined digital data determines which channel provided the analog signal.

Task list:

1) preamplifiers. These are low noise preamplifiers, designed for high input capacitance. The signal to noise ratio, after shaping, must be greater than 100:1. Again, differential outputs are preferred. Test and calibration pulses must be inserted at the preamplifier input, or in the chamber itself. This requires a custom integrated circuit design.

2) cables to racks mounted on the magnet pole face. This is a short run of shielded twisted pairs, the worst case is 15 meters. If all electronics is located on the chamber, these cables are not necessary.

3) shapers, discriminator and sample/hold for each channel

4) digital pipeline with error flags for each channel

5) analog multiplexing and adc system

These 3 items are combined on one large circuit board, with 256 input channels, and 32 ADC channels. Trigger outputs, if required, will be generated by this board. This channel density requires a substantial increase in connector density over the current practice. This requires a custom integrated circuit design.

6) crate by crate readout to the upper counting room. This cable run is at least 50 meters.

7) receiver/buffers for 250 optical fibers. Each channel requires a few thousand bytes of fast buffer.

8) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

Muon endcap system 252k channels mounting nearly all electronics on the chamber using shaping and sample-holds (local dead time) the technical risk is moderate.

Muon Endcap System, 252k CSC pads

	Engineering/design			EDIA		Prototype	Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total	Material	
Item	my	k$/my	k$	k$	k$	k$	$/chan	$k total
Preamp shaper, S&H, 16 PADs/chip, (CERN Amplex)								
	2.00	308	308	40	150	498	3	756
Preamp chip test station								
	1.00	154	154	50	50	254	1	252
ADC 32 PAD's/chip								
	Commercial chip @ $ 100/ea						3	788
Discriminator IC, 16 PADs/chip								
	1.25	154	192.5	40	150	382.5	1	252
Digital logic & hit FIFO, 16 PADs/chip								
	1.25	154	192.5	40	150	382.5	1	252
FIFO chip PC board,normal density, 1 sq in / PAD								
	1.50	154	231	10	20	261	15	3780
Total						1778	24	6079

Muon Endcap System, ???k CSC Anode wires

Item	Engineering/design Labor my	Rate k$/my	Total k$	Material k$	EDIA Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Anode wire preamp, 8 wires/chip	0.50	154	77	30	150	257	1.5	199.5
Digital pipeline, 1 per 8 wires	1.25	154	192.5	40	150	382.5	2	266
PC board, 0.25 sq. inch/ wire	0.55	154	84.7	4	16	104.7	3.75	498
Total						744.2	7.25	963.5
252 readout and comm. links, one for each 1000 signals,80m							250ea	63
Receiver/buffer complex boards, 6 sq. inch/link							90ea	22.7
Rack slot space, $900/board							30ea	7.6
Total								93.3
Low voltage power, less than 100mw/channel, 25 kW total							$5/watt	125
High voltage supply, 1000 channels							150	150
Cables						50		50
Total								325

7. Inner part of the central tracker

This will consist of silicon strips, with the electronics inside, and multiplexed output data on Optical fibers or cables. This is inside the detector, so power and space are at a premium. This part of the detector does participate in 1st level trigger, but will be read in time to provide information for the Level 2 trigger. Storage must be provided for all data during the 1st level trigger delay, and for all successful 1st level triggers during 2nd level trigger delay. The result of the trigger decisions must be sent into the electronics to control the buffering and readout.

This portion of the detector is being designed at Los Alamos. The electronics design and packaging is an integral part of the detector, and will not be further discussed here.

The data will be multiplexed out on 3500 medium speed optical fibers. In this estimate we consider the costs of the drivers, the fiber, and the receiving electronics and data buffering. If rad hard electronics for the fiber system are not available, an intermediate stage will be provided, with copper cables bringing the signals from inside the detector to a location just outside the calorimeter.

Task list:

In the upper counting room the cable run is at least 80 meters.

1) receiver/buffers for 3500 optical fibers. Each channel requires a few thousand bytes of fast buffer.

2) communication of Level 1 & 2 trigger information, as required. This is straightforward, requiring only coordination with the inside electronics. The Level 1 is synchronous, and requires only the presence or absence of a yes signal at the proper time. Level 2 is asynchronous, and requires a specific yes or no answer for each event in the Level 1 buffer.

3) integrating this data into the final data stream to Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

Inner Central Tracker

Item	Engineering/design Labor my	Rate k$/my	Total k$	Material k$	EDIA Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Readout & communication links								
3500 80 meter optical links							250ea	875
Receiver/buffer boards								
complex board, 6 sq. in/link							90ea	315
Rack slot space, $900/board							30ea	105
Total							370ea	1295
High voltage supply, 256 channels							150	38.4
Cables							50	12.8
Total								51.2

8. Outer part of the central tracker

This will be an Interpolating Pad Chamber. All electronics are inside the detector, the data are multiplexed out for successful triggers. This system does not participate in the Level 1 trigger, but may provide selected data for the Level 2 trigger. The charge on each pad is measured with better than 1% accuracy to achieve the required spatial accuracy after interpolation. A switched capacitor array is required for analog storage during the Level 1 trigger delay and for buffering analog samples awaiting digitization after a Level 1 accept. A calibration system is required to maintain the 1% relative accuracy (for adjacent channels).

A reduced set of the anode wires (reduced by ORing) will also be instrumented to determine the Z coordinate with higher precision than the pad size. This will require preamplifiers, discriminators, latches, digital pipelines and buffers. These must also be integrated into the readout, of course. The time resolution need only be good enough to overlap the correct beam crossing. These components must also be Radiation hard. To avoid requiring a high voltage coupling capacitor on each wire, it may be possible to float the entire wire readout at the high voltage. The high voltage capacitors are rather large, and space is at a premium in this system.

Task list:

On the detector

1) preamplifiers on every channel. These are fast shaping and low noise. The input capacitance is modest (bipolar is appropriate). The signal levels are low (100 fC). These preamplifiers must be radhard. This requires a custom integrated circuit design.

2) switched capacitor storage array on every channel. The requirements are modest compared to the calorimeter usage of these devices, but they must be radhard. The ADC can be a simple 8 bit, 2 microsecond Wilkinson type, with one ADC per channel. As many as 3 samples may be required per event. This should be either integrating or peak detecting, not voltage sampling. This requires a custom integrated circuit design.

3) communication of Level 1 trigger information, as required. This is straightforward, requiring only coordination with the inside electronics. The Level 1 is synchronous, and requires only the presence or absence of a yes signal at the proper time. Levels 2 is asynchronous, and require a yes or no answer for each stored event.

4) multiplexing data into output fibers or cables. A multiplexing and sparsifying processor is required. This must be radhard. This requires a custom integrated circuit design.

In the upper counting room the cable run is at least 80 meters.

5) receivers and buffers for 1200 optical fibers. Each channel requires a few thousand bytes of fast buffer.

6) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

7) for the 100k anode wires to be instrumented: preamplifiers, discriminators, digital latch and pipeline, readout.

This is a completely monolithic system, with very few other components. All system functions, including calibration, testing and readout must be incorporated into the integrated circuits. The IC production costs have been doubled to reflect the higher complexity of

the circuits.

Outer Central Tracker, 446k pad channels

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Preamp, 8 channel custom IC, 8 PADs/chip (rad hard)	1.00	154	154	60	300	514	6	2676
Switched capacitor array chip, integrating or peak detecting 16 PADs/chip (rad hard), 8-bit ADC included	4.00	154	616	80	300	996	12.5	5575
Chip test station	1.00	154	154	50	50	254	1	446
MUX and readout chip, 256 PADs/chip (rad hard)	2.50	154	385	80	300	765	.25	112
Dense PC board, 10 PAD/sq.in	1.50	154	231	10	20	261	3	1338
Total (due to the very high level of integration, the technical and cost risks are high)						2790	22.75	10147

1745 readout and comm. links, one for each 256 PADs,80m	250ea	436.3
Receiver/buffer complex boards, 6 sq. inch/link	90	157.1
Rack slot space, $900/board	30	52.4
Total		645.8
Low voltage power, less than 100mw/channel, 45 kW total		225
High voltage supply, 256 channels	150	38.4
Cables	50	12.8
Total		276.2

Outer Central Tracker, 100k anode wires

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Preamp, 8 channel custom IC, 8 wires/chip (rad hard)	1.00	154	154	60	300	514	6	600
Discriminator and digital pipeline, 16 wires/chip (rad hard)	2.50	154	385	80	300	765	4	400
MUX and readout chip, 256 wires/chip (rad hard)	2.50	154	385	80	300	765	0.25	25
Dense PC board, 10 wires/sq.in	1.50	154	231	10	20	261	3	300
Total (due to the very high level of integration, the technical and cost risks are high)						2305	13.25	1325

390 readout and comm. links, one for each 256 wires, 80m	250ea	97.5
Receiver/buffer complex boards, 6 sq. inch/link	90	35.1
Rack slot space, $900/board	30	11.7
Total		144.3
Low voltage power, less than 100mw/channel, 10 kW total		50
Total		50

9. Calorimeter

There are two possible calorimeter systems under consideration. In both cases the calorimeter size is such that a minimum ionizing particle (a muon) deposits about 1 GeV. The maximum expected signal is about 3 TeV, either Hadron jet or electromagnetic shower. In the electromagnetic part of the detector, a muon will deposit only 0.1 GeV, an electron or photon will deposit as much as 2 TeV in a single channel.

The temporary baseline system is a liquid Argon calorimeter, containing both electromagnetic and hadronic sections. The electronic resolution required is 0.1 %, over a 16 bit dynamic range.

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The question of dynamic range and accuracy is under discussion. The above numbers may need to be changed when a firm specification is set.

****

The alternate electromagnetic calorimeter will be Barium Fluoride crystals with photo-triode readout. The hadronic section will be scintillating fibers in matrix of heavy material. With this option, the pre-radiator is not used.

The calorimeter electronics will be outside the magnet, located on the membrane that supports the calorimeter. Only preamplifiers and cable drivers will be in the detector volume.

Liquid Argon:

The liquid Argon calorimeter is used as an ionization chamber, there is no wire gain as with proportional chambers. The absorbing plates are accordian shaped, with the collecting gaps in between. The collecting electrodes are shaped and connected to give the appropriate sampling geometry. Preamplifiers are required to be very close to the collecting electrodes, in the liquid Argon. The detector capacitance is large, so a FET input is required for lowest noise. Pulse shaping results in 40 nsec wide signals. Noise per electronic channel is less than 100 MeV, so the dynamic range (signal/noise) is 16 bits (EM section). There is no gain control, so the ADC dynamic range must be large enough to cover gain variations between channels. To identify the correct beam crossing and reduce the effect of pile up noise, 5 samples (not necessarily contiguous) must be measured for each successful trigger. The switched capacitor analog storage system will sample the signals at the beam crossing rate.

Barium Fluoride electromagnetic section:

This option consists of Barium Fluoride crystals, with vacuumphoto-triode readout. The phototubes are oriented parallel to the magnetic field. A fast preamplifier is required after the phototube. Since the signals are fast and pile up is not expected to be a problem, no more than 3 samples are required, possibly only 1.

Scintillating fiber Hadronic Section:

The fibers are embedded in a matrix of heavy material. The signal is 100 photoelectrons per GeV deposited. Further amplification after the photomultiplier is not required. The channel gains can be equalized by controlling the PMT high voltage. There are about 5000 photomultiplier channels. Noise is less of a problem than with liquid Argon, but photon counting and shower development statistics limit resolution at the low end. The PMTs will not resolve single photoelectrons, so the best case resolution is 2-3 photoelectrons. The

dynamic range requirement is less than 16 bits. The signals are fast, about 10 ns wide.

To determine the longitudinal shower position, leading edge time measurement is required on the signal. The required resolution is 100 psec.

The electronic ADC system:

The ADC system is common to both candidate systems. The requirements are at least 16 bits dynamic range, pipeline delays and trigger outputs. The pipeline delay will be provided by a switched capacitor array sampling the input at the beam crossing rate. These arrays, as developed at LBL, have demonstrated a dynamic range of 12 bits, so both a high and low range channel are required, with x16 gain in the low range channel. This results in a 16 bit dynamic range, with minimum resolution of 8 bits. The LBL chips have been designed as 16 channel devices, so each chip can provide storage for 8 calorimeter channels.

The maximum expected Level 2 input rate of 100 KHz leaves just 10 microseconds to read out all channels. Since for LAR five samples are required, each channel must be instrumented with a 12-bit ADC capable of 500 kHz sampling. Alternatively, a single high-speed ADC can be usedc to service several channels. If, for example, there is one ADC per chip (eight dual-range channels) an 8 MHz ADC would be required. Such an approach will require a significant improvement in the the multiplexer output settling time of the SCA chip.

An electronic test and calibration system is required for the electronic chain, to verify function and stability. The primary energy calibration however, must be via a physics process.

Task list:

Liquid Argon calorimeter

1) preamplifier in the liquid Argon.This is a low noise, FET input preamplifier. It must be designed to operate at liquid Argon temperatures, and dissipate as little power as possible. There is little or no shaping at the preamplifier, the output is differential. This requires a new preamplifier design, either custom monolithic or hybrid.

2) cables to just outside the calorimeter. This cable run is less than 5 meters. The cable should be shielded twisted pair. This is a an unterminated cable, to reduce the power required by the preamplifier.

3) shapers and line drivers. This produces a shaped signal, approximately 40 nsec peaking time, and drives a terminated differential cable. These circuits are mounted in small racks, on the outside of the liquid Argon cryostat or support structure. This requires a custom circuit board.

4) cables to ADC racks located outside the magnet, but inside the hall. This is a 20 meter cable run of shielded twisted pairs.

5) analog pipeline storage, and ADC system. This system is on standard large printed circuit boards, approximately FASTBUS size. The input accepts the differential signal from the shaper, and further shapes, and splits the signal into a high and low range. Each board can contain 64 calorimeter channels, each with a high and low range. This board provides prompt signals for the Level 1 trigger, and receives the trigger decisions. This requires a custom integrated circuit design.

6) crate by crate readout to the upper counting room. This cable run is at least 50 meters.

7) receiver/buffers for 800 optical fibers. Each channel requires a few thousand bytes of fast buffer.

8) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

9) Calibration system. This requires components in the liquid, comparable in complexity to the preamplifier, and some control functions located outside the magnet, near the ADC cards.

The signal processing uses a dual range system to achieve the required dynamic range. Two SCA and two ADC channels are required for each signal channel.

Liquid Argon calorimeter, 80k channels

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Preamp, single monolithic chip, with integrated J-FET	0.50	154	77	30	150	257	6	480
calibration system (this portion on preamp pc board)	0.50	154	77	30	150	257	6	480
Preamp PC board, 4 chan/sq.in	0.55	154	84.7	4	16	104.7	2	160
Cable to outside, 5M sh tw pair				20		20	1.5	120
Intermediate driver PC board	0.55	154	84.7	4	16	104.7	8	640
Cable to ADC racks, 20M				20		20	6	480
Switched capacitor array chip, 8 ch/chip (not radhard)	2.00	154	308	40	150	498	6	480
SCA test station	1.00	154	154	50	50	254	2	160
12-bit high speed ADC, 8 ch/chip(not radhard)	2.00	154	308	40	150	498	6	480
ADC test station	1.00	154	154	50	50	254	2	160
FADC for trigger system							3	240
ADC PC board, 3 sq. inch/channel	1.50	154	231	10	20	261	45	3600
Rack slot cost, special rack, with remote power							25	2000
calibration pc board, 6 sq. in. / cal. ch., 32 signal ch/cal ch	1.50	154	231	10	20	261	3	240
Rack slot cost, special rack, with remote power							.75	60
Total						2343.4	122.25	9780
80 readout and comm. links, one for each 1000 signals,80m							250ea	20

Receiver/buffer complex boards, 6 sq. inch/link	90	7.2
Rack slot space, $900/board	30	2.4
Total		29.6
Low voltage power, less than 200mw/channel, 16 kW total	$5/watt	80
High voltage supply, 1000 channels	150	150
Cables	50	50
Total		280

10. Silicon pre-radiator

This is a silicon strip calorimeter, located just outside the tracker system. It consists of 3 radiation lengths of lead, and 2 layers of 1 mm pitch silicon strips (x & y). This does not participate in the 1st level trigger, but is expected to provide data for the 2nd level trigger. This detector may be embedded in the main calorimeter. The resolution requirements are modest, 6 bits linear, or 4 bits logarithmic. The electronics is inside the detector, the data is multiplexed out after the trigger decision, as the tracker systems. The calibration requirements are quite modest.

Task list:

1) preamplifiers. The input signal levels are modest, about 50 fC/mip (up to 1 pC in a shower). The shaping (peaking time) must be 20 nsec or less. This electronics must be radhard. This requires a custom integrated circuit design.

2) integrating switched capacitor array as developed for the outer tracker. the resolution is sufficient to eliminate the requirement for the special analog channel to measure the energy loss. Two wafers are combined in one readout, since the SCA is expected to be 16 channels.

Alternate readout:

2) logarithmic flash adcs followed by digital pipeline storage. Some combining of channels is possible here. Channels more than 16 strips apart can be resolved by the electromagnetic calorimeter, so can be combined after the preamplifier. This flash ADC must operate at the beam crossing rate, and be low power. This electronics must be radhard. This requires a custom integrated circuit design.

2a) combined analog channel for precision charge measurement. This uses a switched capacitor storage array and adc as in the main calorimeter. This can measure the OR of 64 strips, so only one ADC per silicon wafer is required. This electronics must be radhard. This requires a custom integrated circuit design.

3) multiplexing data onto output fibers or cables. A multiplexing and sparsifying processor is required. This must be radhard. This requires a custom integrated circuit design.

All electronics is mounted very close to the silicon wafer. This puts a high premium on space and power dissipation. The space provided is about 15 square mm of circuit board for each silicon strip.

In the upper counting room the cable run is at least 80 meters.

4) receiver/buffers for 500 optical fibers. Each channel requires a few thousand bytes of fast buffer.

5) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

Pre-Radiator, 14203 signal channels

There are 500k 1 x 64 mm strips in 2 layers. Strips are paired to form 128 mm long strips. Every 8th strip in a pair of wafers is combined into one signal channel. There are only 142203 signal channels. The total cost per signal channel is 16 times the cost per strip.

Note that the IC development cost may not be required, if these are the same ICs developed for the outer central tracker.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Preamp, 8 channel custom IC, 1/16 strips (rad hard)	1.00	154	154	60	300	514	3	42.6
Switched capacitor array chip, integrating or peak detecting 256 strips/chip (rad hard), 8-bit ADC included	4.00	154	616	80	300	996	6	85.3
Chip test station	1.00	154	154	50	50	254	1	14.2
MUX and readout chip, 192 signals/ch (rad hard)	2.50	154	385	80	300	765	0.16	2.3
Complex PC board, one signal/sq.in	1.50	154	231	10	20	261	15	213.1
Total						2790	25.2	357.5
74 readout and comm. links, one for each 192 signals,80m							250ea	18.5
Receiver/buffer complex board, 6 sq. inch/link							90	6.7
Rack slot space, $900/board							30	2.2
Total								27.4
Low voltage power, less than 100mw/channel, 1.5 kW total								7.5
High voltage supply, 900 channels							150	135
Cables							50	45
Total								187.5

11. Trigger Systems

Master trigger crate

This system coordinates the subdetector triggers and combines them into the global trigger. It also orchestrates the multilevel trigger and keeps track of the buffer space available. This system consists of at least one workstation computer and a large quantity of fast logic.

Clock distribution (and other fast signals)

The pipeline storage for the Level 1 trigger delay are synchronous, and must be provided with the 60 MHz clock. The Level 1 accept signal is also synchronous. Both of these signals must be distributed with a timing skew of order 1 nanosecond to all detector signal channels.

The Level 2 trigger, and the data acquisition are asynchronous and do not require precisely timed signals.

Calorimeter trigger system

On each ADC board there will be an Analog sum for each 32 channels, followed by a 3 stage pipelined integrate, sample-hold and logarithmic flash ADC system capable of 16 ns throughput rates. This pipeline is also capable of detecting a local peak to avoid multiple triggering on several adjacent beam crossings when large signals are present. To a first approximation, this peak' detection will also determine the beam crossing. The 8 bit digital signals are converted to serial and leave the ADC board on an optical fiber. Assuming trigger towers of size .16 x .16, there are 1480 fibers for the Ecal and 1480 for the Hcal.

These signals are received on a board in the trigger system in the counting room, and converted to parallel signals, 8 bits every 16 ns are distributed to two systems, the Energy SUM and the Energy ISOLATION systems.

Each Energy Sum board adds 16 signals after converting the signals to a linear 12 bit code. The Sum is converted back to logarithmic before leaving the board. It requires 10 levels of summing and 20 pipeline steps to calculate the sum of 1024 signals. The total number of boards (all identical) is approximately 100.

The Energy ISOLATION board has 25 inputs, and computes the isolation cut for 9 of those inputs. Note that most signals are needed by 2 or more boards. The Electromagnetic calorimeter requires 165 boards, the Hadronic calorimeter requires 165 more.

Task list:

Analog sum on each ADC board. This is included in the ADC board cost estimate, but mentioned here for completness. This has a three stage pipeline for the shaped sum signal which successively integrates, measures with a flash ADC and resets. The ADC is nonlinear, giving 10-12 bits of dynamic range for 8 bits out. The 8 bits are sent to the trigger system via a serial optical link operating at a speed of 2 nsec per bit. (an 8 bit parallel ECL link is also possible). There is one analog sum for each 32 channels, or 2 per ADC board.

The Optical links to the trigger system in the upper counting room. A 32 channel receiver card which converts the data to 8 bits parallel, and fans it out to the trigger cards. Note that some signals have several destinations. The 8 bit signal is non-linear, it is converted to linear only when needed.

The Energy SUM card.

The Energy ISOLATION card.

3000 channels of Analog SUM and flash ADC. These are located on the ADC card, and the cost is included in that card.

Calorimeter trigger system, 2960 channels

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Optical link, 80 m ($250x4)							1000/ea	2960 0
Receiver board, 32 channels, complex digital board	1.50	154	231	10	20	261	94	278
Rack slot space, $900/board							28	83
Total						261		3321
Energy SUM board, 16 8-bit inputs, 100 each for ECAL & HCAL, Complex digital board	1.50	154	231	10	20	261	$/bd 3000	600
*Complex digital chips for summing (15/board)	1.25	154	193	40	150	383	1500	300
Crate slot cost, $900/board							900	180
Total						644		1080
Energy ISOLATION board, 330 boards, 25 8-bit input, Complex digital board	1.50	154	231	10	20	261	3000	990
*Complex digital chips for isolation sum (9/board)	1.25	154	193	40	150	383	900	300
Crate slot cost, $900/board							900	297
Total						644		1587

*Note: we assume chip costs of $ 100/ea since these are large pin count packages.

Muon trigger system

There are two approaches to the muon trigger. The first approach uses simple coincidence circuits and combinatorial logic on a large scale. This can be pipelined (only a few pipeline steps are necessary) at the 60 MHz beam crossing rate and can therefore be completely deadtimeless. The drawback of this approach is that the signals from individual trigger elements (RPC strips in the case of the barrel) must be routed to a common location.

A second approach uses content addressable memories (CAM's) to perform the logic. This approach employs element address information rather than individual element signals, which greatly reduces the number of cables---e.g. hits on a 256-element plane can be encoded as a list of (one or two) eight-bit words. However, since hits are processed in a serial fashion some deadtime is introduced. This deadtime is most likely tolerable since it is local in nature; a candidate track in one sector of the detector needn't deaden the entire array.

In the barrel RPC array the cable density is relatively low, leading one to favor the comparatively simple combinational approach. In the endcap, the trigger elements are much more densely packed, leading one to favor the CAM approach.

Barrel (RPC) Trigger

Since the drift times in the barrel drift tubes are several beam crossings long, resistive plate chambers are planned to provide the trigger information. Pickup strips are arranged to avoid timing ambiguities as described in section 4. The strip segmentation in the bend plane is fine enough to provide sufficient resolution to make the desired momentum cut.

(A backup system that will extract the beam crossing information from the drift wires themselves is under investigation, but that effort is still at an early stage.)

For the barrel, the signals from the RPCs or the wires themselves will be cabled to electronics located on the outside of the magnet. In each of the sixteen phi sectors there are 111, 187, and 240, azimuthal strips for the inner, central, and outer RPC layers, respectively. Since each strip is divided into eight sections along its length (i.e. in z), there are a total of 67K azimuthal strips. Since the requisite logic is comparatively simple, the packing density is limited by the number of signals that can be routed to a single board. This is approximately 192 if double density (20 pairs/inch) flat cable is used. Allowing for edge effects, which will require some signals to go to two modules, we assume 160 signals per board, for a total of 425 complex digital boards. There are 16K z-strips, requiring an additional 100 boards of a different design.

Muon Barrel trigger system, 425 Phi boards

	Engineering/design			EDIA		Prototype	Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total	Material	
Item	my	k$/my	k$	k$	k$	k$	$/board	$k total
Complex digital board	1.50	154	231	10	20	261	3000	1275
*High pin count digital chips for track finding (4/board)	1.25	154	193	40	150	383	400	170
Crate slot cost, special crate $1600/board							1600	680
Total						644		2125

Muon Barrel trigger system, 100 Z-boards

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/board	$k total
Complex digital board	1.50	154	231	10	20	261	3000	300
*High pin count digital chips for track finding (4/board)	1.25	154	193	40	150	383	400	400
Crate slot cost, special crate $1600/board							1600	160
Total						644		800

*Note: we assume chip costs of $ 100/ea since these are large pin count packages.

Combinatorial logic board 160 input, programmable gate array technology, 12 large gate array chips at $80 each, complex digital board	1.50	154	231	10	20	261	3000	856
Crate slot cost, $900/board							900	192.6
Total								1048.6

Endcap System

As mentioned above, the endcap pad system Level 1 trigger is based on content addressable memories (CAM's).

For the endcap chambers, the logical grouping is a box, containing 4 layers of 256 pads each. The complete CAM system will be contained in the box. The CAM logic takes as input latched versions of the pad discriminator outputs, which are driven by the fast trigger-pickoff outputs of the pad preamplifiers (see section 6). When a potential trigger is detected in a group of pads the hit data in that group is latched and a local deadtime signal is asserted. The latched signals are routed to 256-input priority encoders, which produce eight-bit address words for the CAM (each CAM examines quadruplets of eight-bit addresses). The CAM's rapidly (the number of iterations is equal to the maximum number of hits allowed per plane) looking for valid track-segment matches, defined as 3- or 4-fold coincidence among the 4 sub-layers that comprise the box. Track segments (or "match addresses") from the three boxes that comprise a superlayer are routed via optical fiber to the electronics room, where they are linked by a second CAM system into tracks. Since there can be more than one match on a given beam crossing, the system must be prepared to send more than match address to the segment linking CAM. Three optical fibers / box provide the link. The local deadtime induced by the CAM's is approximately 200 ns. f required, it can be largely eliminated by double buffering the latched inputs.

Since the electronics are chamber-mounted the technical risk is high.

Muon Endcap trigger system

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/box	$k total
Latch/buffer/priority encoder chip, $16 each	1.25	154	192.5	40	150	382.5	1024	256

Content addressable memory chip, (large chip @ $100 each)

1.25	154	192.5	40	150	382.5	100	25

1 Gbits/sec optical link to trigger ($250x8) 2500 625

Complex digital PC board, 100 sq. inch, incl. sequencer

1.50	154	231	10	20	261	1500	375

Receiver board, 32 channel, complex digital board, 6 sq. inch/channel

1.50	154	231	10	20	261	270	67.5

Total 1287 1348

Large CAM board for final track finding, 32 required, 1 per sector,
16 CAM chips, 1600 51.2
Complex PC board

1.50	154	231	10	20	261	3000	96

Crate slot cost, $900/board 900 28.8

Total 176

D.R. Marlow
April 22, 1992

Level 2 Trigger and DAQ Costs

PLACEHOLDER COST ESTIMATES

We are currently (4/92), in the process of establishing DAQ and Level 2 trigger groups. At this writing both of these systems are in an embryonic state and credible cost estimates are not available. The following estimates are at best rough guidelines intended to set the scale for planning purposes.

Level 2 Trigger

Some preliminary work has been done on the calorimeter trigger. A few approaches have been investigated, mostly concentrating on designs where "filtered" data from the ADC's are routed to some sort of multiport memory that can be accessed by one or more high-speed microprocessors. The processors make use of Level 1 information to determine where in the memory to search for electron or photon candidates and then perform a detailed shower-shape analysis using the data from individual calorimeter elements. A preliminary analysis carried out by the SSCL DAQ group yields the following conclusions.

---The calorimeter data should be filtered on the ADC cards using low-cost DSP's, each of which services a few (four) channels. This gains an immediate factor of five to ten reduction in the data volume, since the five samples and two ranges can be combined into a single two-byte word.

---Assuming 50 channels per ADC card and fixed block transfers---i.e. all 50 words are transferred without zero suppression---a total of 100 bytes must be transferred to the multiport memory in 10 microseconds. Thus each board should be equipped with an FDDI link. ($ 250/ea)

---The memory will be limited by the number of links that can be handled by each board. The number of such links will be roughly the same as the Level 1 links, or about 3000 for the HCAL and ECAL combined. Assuming 32 links per receiver/memory board, we arrive at a total of 94 boards.

---The Level 2 algorithm requires approximately 100 microseconds on a fast microprocessor. Thus a "farmette" of approximately 10-20 processors is required. We assume one processor per complex digital board.

We thus incur the following costs:

Level 2 Readout Item	Unit	#Req'd	Cost/ea	Total ($K) EDIA	Fab/Proc
Calorimeter-board DSP's (.25/ch)	ea	20K	$ 30		600
Programming Effort for above	MY	1	154K	154	
100 Mbit/sec fiber links	ea	3000	$ 250		750
Receiver/Memory board design	ea	1		261	
Receiver Memory board fab.	ea	94	$ 3000		282
Crate slot charge	ea	94	$ 900		85
Processor boards design	ea	1		261	
Processor boards fab.	ea	20	$ 3000		60
Totals				676	1777

The first two items are actually part of the calorimeter front end and should not be included here. Excluding them yields a total of $ 1700K which with a contingency of 30% yields a total of $ 2.2M for the calorimeter trigger alone. Assuming comparable systems are needed for the central tracker and the muon systems (although the reduced data volumes in the muon system may result in lower costs), one arrives at a total Level 2 cost of $ 6.6M.

Data Acquisition:

Since this has a large software development component, it is particularly difficult to estimate (and will likely remain so for quite some time). Interestingly enough, however, the independent opinions of three "experts"---Botlo, Denes, and DRM (OK, two experts)---on the required level of effort were surprisingly close. Without consulting one another we agreed that to within 20% a team of about ten dedicated DAQ people would be needed at the time the experiment turns on. All also agreed that a level of effort in the two FTE range would be about right in the near term. Starting in FY93 with two FTE's and assuming a linear increase to 10 FTE's in the year 2000, one arrives at a total of 45 FTE-years. At least 50% of these individuals should be full-time residents and are therefore estimated at the SSCL rate of $ 78K/MY, the remainder are visitors, for which we assume the national lab rate of $ 154/MY. This yields $5.2 M plus 30% contingency for a total of $ 6.8 M.

Not included in this estimate is the DAQ hardware and whatever software licenses might be required. Conservatively, these might total to a number that is the same as the manpower costs for a grand total of $ 13.6 M, but this is pure speculation. Indeed, one can hope that most of the DAQ hardware costs have been included in the front end estimates. As mentioned, there is an effort underway aimed at producing a conceptual design that can be more reliably costed.

4/23/92

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
1	Date: April 23,92		Engineering/design			EDIA	Inspection/Administration			Proc/Fab	Installation					Totals				
2			Labor	Rate	Total	Material	Labor	Rate	Total	Material	Labor	Rate	Subtotal	Material	Total	Labor	Material	Subtotal	Contlng	Total
3	WBS number	Item	my	k$/my	k$	k$	my	k$/my	k$	k$	my	k$/my	k$	k$	k$	k$	k$	k$	k$	k$
4																				
5	522.50.5	Electronics																		105081.15
6																				
7	522.50.5.1	Front-end																		84510.56
8																				
9	522.50.5.1.2	Muon																		31018.90
10																				
11	522.50.5.1.2.1	Resistive Plate Chamber (85K)																		5629.97
12	522.50.5.1.2.1.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
13	522.50.5.1.2.1.2	Prototype																		
14	522.50.5.1.2.1.2.1	High voltage																		
15	522.50.5.1.2.1.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
16	522.50.5.1.2.1.2.1.2	Distribution																		
17	522.50.5.1.2.1.2.2	Low voltage in-detector																		
18	522.50.5.1.2.1.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
19	522.50.5.1.2.1.2.2.2	Distribution																		
20	522.50.5.1.2.1.2.3	Signal cables				20										0.00	20.00	20.00	1.40	21.40
21	522.50.5.1.2.1.2.4	Active components																		
22	522.50.5.1.2.1.2.4.1	Preamp/discriminator	0.50	154	77.00	30				150.00				1.50		77.00	181.50	258.50	56.87	315.37
23	522.50.5.1.2.1.2.5	Printed circuit board																		
24	522.50.5.1.2.1.2.5.1	Preamp/discriminator	0.55	154	84.70	4				16.00				2.00		84.70	22.00	106.70	23.47	130.17
25	522.50.5.1.2.1.2.6	On-detector crate completed																		
26	522.50.5.1.2.1.2.7	Control/data links																		
27	522.50.5.1.2.1.2.7.1	Receiver & buffer	0.25	154	38.50											38.50	0.00	38.50	8.47	46.97
28	522.50.5.1.2.1.2.7.2	Optics	0.25	154	38.50											38.50	0.00	38.50	3.47	41.97
29	522.50.5.1.2.1.3	Production																		
30	522.50.5.1.2.1.3.1	High voltage																		
31	522.50.5.1.2.1.3.1.1	Power supply								38.40				3.84		0.00	42.24	42.24	5.07	47.31
32	522.50.5.1.2.1.3.1.2	Distribution	0.50	154	77.00					12.80				1.28		77.00	14.08	91.08	20.95	112.03
33	522.50.5.1.2.1.3.2	Low voltage in-detector																		
34	522.50.5.1.2.1.3.2.1	Power supply								40.00				4.00		0.00	44.00	44.00	7.04	51.04
35	522.50.5.1.2.1.3.2.2	Distribution	0.25	154	38.50					10.00				1.00		38.50	11.00	49.50	11.39	60.89
36	522.50.5.1.2.1.3.3	Signal cables								382.50				4.50		0.00	387.00	387.00	27.09	414.09
37	522.50.5.1.2.1.3.4	Active components																		
38	522.50.5.1.2.1.3.4.1	Preamp/discriminator								127.50				2.00		0.00	129.50	129.50	28.49	157.99
39	522.50.5.1.2.1.3.4.2	TDC chip								170.00				2.00		0.00	172.00	172.00	37.84	209.84
40	522.50.5.1.2.1.3.5	Printed circuit board																		
41	522.50.5.1.2.1.3.5.1	Preamp/discriminator								170.00				2.00		0.00	172.00	172.00	37.84	209.84
42	522.50.5.1.2.1.3.5.2	TDC								1870.00				22.00		0.00	1892.00	1892.00	416.24	2308.24
43	522.50.5.1.2.1.3.6	On-detector crate completed								1020.00				12.00		0.00	1032.00	1032.00	165.12	1197.12
44	522.50.5.1.2.1.3.7	Control/data links (32 links)																		
45	522.50.5.1.2.1.3.7.1	Receiver & buffer								2.88				0.28		0.00	3.16	3.16	0.70	3.86
46	522.50.5.1.2.1.3.7.2	Optics								8.00				0.80		0.00	8.80	8.80	0.79	9.59
47	522.50.5.1.2.1.3.7.3	Rack slot								0.96				0.10		0.00	1.06	1.06	0.17	1.23
48	522.50.5.1.2.1.4	Installation & test																		
49	522.50.5.1.2.1.4.1	Engineer									0.50	78	39.00			39.00	0.00	39.00	8.97	47.97
50	522.50.5.1.2.1.4.2	Sr. technician									0.50	50	25.00			25.00	0.00	25.00	5.75	30.75
51	522.50.5.1.2.1.4.3	Jr. technician									1.50	37	55.50			55.50	0.00	55.50	12.77	68.27
52																				
53	522.50.5.1.2.2	PDT/LSDT (133K channels)																		10305.58
54	522.50.5.1.2.2.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27

$ 1/4M

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
55	522.50.5.1.2.2.2	Prototype																		
56	522.50.5.1.2.2.2.1	High voltage																		
57	522.50.5.1.2.2.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
58	522.50.5.1.2.2.2.1.2	Distribution																		
59	522.50.5.1.2.2.2.2	Low voltage in-detector																		
60	522.50.5.1.2.2.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
61	522.50.5.1.2.2.2.2.2	Distribution																		
62	522.50.5.1.2.2.2.3	Signal cables				20										0.00	20.00	20.00	1.40	21.40
63	522.50.5.1.2.2.2.4	Active components																		
64	522.50.5.1.2.2.2.4.1	Preamp/discriminator	0.50	154	77.00	30				150.00				1.50		77.00	181.50	258.50	56.87	315.37
65	522.50.5.1.2.2.2.4.2	Time digital converter	1.25	154	192.50	40				150.00				2.00		192.50	192.00	384.50	215.32	599.82
66	522.50.5.1.2.2.2.5	Printed circuit board																		
67	522.50.5.1.2.2.2.5.1	Preamp/discriminator	0.55	154	84.70	4				16.00				2.00		84.70	22.00	106.70	23.47	130.17
68	522.50.5.1.2.2.2.5.2	Time digital converter	1.50	154	231.00	10				20.00				22.00		231.00	52.00	283.00	135.84	418.84
69	522.50.5.1.2.2.2.6	On-detector crate completed																		
70	522.50.5.1.2.2.2.7	Control/data links																		
71	522.50.5.1.2.2.2.7.1	Receiver & buffer	0.25	154	38.50											38.50	0.00	38.50	8.47	46.97
72	522.50.5.1.2.2.2.7.2	Optics	0.25	154	38.50											38.50	0.00	38.50	3.47	41.97
73	522.50.5.1.2.2.3	Production																		
74	522.50.5.1.2.2.3.1	High voltage																		
75	522.50.5.1.2.2.3.1.1	Power supply								150.00				15.00		0.00	165.00	165.00	19.80	184.80
76	522.50.5.1.2.2.3.1.2	Distribution	0.50	154	77.00					50.00				5.00		77.00	55.00	132.00	30.36	162.36
77	522.50.5.1.2.2.3.2	Low voltage in-detector																		
78	522.50.5.1.2.2.3.2.1	Power supply								52.00				5.20		0.00	57.20	57.20	9.15	66.35
79	522.50.5.1.2.2.3.2.2	Distribution	0.25	154	38.50					13.00				1.30		38.50	14.30	52.80	12.14	64.94
80	522.50.5.1.2.2.3.3	Signal cables								598.00				4.50		0.00	602.50	602.50	42.18	644.68
81	522.50.5.1.2.2.3.4	Active components																		
82	522.50.5.1.2.2.3.4.1	Preamp/discriminator								199.50				1.50		0.00	201.00	201.00	44.22	245.22
83	522.50.5.1.2.2.3.4.2	Time digital converter								266.00				2.00		0.00	268.00	268.00	150.08	418.08
84	522.50.5.1.2.2.3.5.1	Printed circuit board																		
85	522.50.5.1.2.2.3.5.2	Preamp/discriminator								266.00				2.00		0.00	268.00	268.00	58.96	326.96
86	522.50.5.1.2.2.3.5.3	Time digital converter								2926.00				22.00		0.00	2948.00	2948.00	1415.04	4363.04
87	522.50.5.1.2.2.3.6	On-detector crate completed								1596.00				12.00		0.00	1608.00	1608.00	257.28	1865.28
88	522.50.5.1.2.2.3.7	Control/data links (54 links)																		
89	522.50.5.1.2.2.3.7.1	Receiver & buffer								4.90				0.49		0.00	5.39	5.39	1.19	6.58
90	522.50.5.1.2.2.3.7.2	Optics								13.50				1.35		0.00	14.85	14.85	1.34	16.19
91	522.50.5.1.2.2.3.7.3	Rack slot								1.60				0.16		0.00	1.76	1.76	0.28	2.04
92	522.50.5.1.2.2.4	Installation & test																		
93	522.50.5.1.2.2.4.1	Engineer									0.75	78	58.50			58.50	0.00	58.50	13.46	71.96
94	522.50.5.1.2.2.4.2	Sr. technician									0.75	50	37.50			37.50	0.00	37.50	8.63	46.13
95	522.50.5.1.2.2.4.3	Jr. technician									2.25	37	83.25			83.25	0.00	83.25	19.15	102.40
96																				
97	522.50.5.1.2.3	Endcap																		*15083.351*
98	522.50.5.1.2.3.1	CSC Wire (133K)																		*2700.28*
99	522.50.5.1.2.3.1.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
100	522.50.5.1.2.3.1.2	Prototype																		
101	522.50.5.1.2.3.1.2.1	High voltage																		
102	522.50.5.1.2.3.1.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
103	522.50.5.1.2.3.1.2.1.2	Distribution																		
104	522.50.5.1.2.3.1.2.2	Low voltage in-detector																		
105	522.50.5.1.2.3.1.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
106	522.50.5.1.2.3.1.2.2.2	Distribution																		
107	522.50.5.1.2.3.1.2.3	Signal cables																		
108	522.50.5.1.2.3.1.2.4	Active components																		

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
109	522.50.5.1.2.3.1.2.4.1	Preamp	0.50	154	77.00	30				150.00				1.50		77.00	181.50	258.50	56.87	315.37
110	522.50.5.1.2.3.1.2.4.2	Digital pipeline	1.25	154	192.50	40				150.00				2.00		192.50	192.00	384.50	215.32	599.82
111	522.50.5.1.2.3.1.2.5	Printed circuit board																		
112	522.50.5.1.2.3.1.2.5.1	Pipeline	0.55	154	84.70	4				16.00				1.60		84.70	21.60	106.30	23.39	129.69
113	522.50.5.1.2.3.1.2.6	On-detector crate completed																		
114	522.50.5.1.2.3.1.2.7	Control/data links																		
115	522.50.5.1.2.3.1.2.7.1	Receiver & buffer	0.25	154	38.50											38.50	0.00	38.50	8.47	46.97
116	522.50.5.1.2.3.1.2.7.2	Optics	0.25	154	38.50											38.50	0.00	38.50	3.47	41.97
117	522.50.5.1.2.3.1.2.7.3	Rack slot																		
118	522.50.5.1.2.3.1.3	Production																		
119	522.50.5.1.2.3.1.3.1	High voltage																		
120	522.50.5.1.2.3.1.3.1.1	Power supply																		
121	522.50.5.1.2.3.1.3.1.2	Distribution																		
122	522.50.5.1.2.3.1.3.2	Low voltage in-detector																		
123	522.50.5.1.2.3.1.3.2.1	Power supply																		
124	522.50.5.1.2.3.1.3.2.2	Distribution																		
125	522.50.5.1.2.3.1.3.3	Signal cables																		
126	522.50.5.1.2.3.1.3.4	Active components																		
127	522.50.5.1.2.3.1.3.4.1	Preamp								199.50				1.50		0.00	201.00	201.00	44.22	245.22
128	522.50.5.1.2.3.1.3.4.2	Digital pipeline								266.00				2.00		0.00	268.00	268.00	150.08	418.08
129	522.50.5.1.2.3.1.3.5	Printed circuit board																		
130	522.50.5.1.2.3.1.3.5.2	Pipeline								498.00				3.75		0.00	501.75	501.75	110.39	612.14
131	522.50.5.1.2.3.1.3.6	On-detector crate completed																		
132	522.50.5.1.2.3.1.3.7	Control/data links																		
133	522.50.5.1.2.3.1.3.7.1	Receiver & buffer																		
134	522.50.5.1.2.3.1.3.7.2	Optics																		
135	522.50.5.1.2.3.1.3.7.3	Rack slot																		
136	522.50.5.1.2.3.1.4	Installation & test																		
137	522.50.5.1.2.3.1.4.1	Engineer									0.50	78	39.00			39.00	0.00	39.00	8.97	47.97
138	522.50.5.1.2.3.1.4.2	Sr. technician									0.50	50	25.00			25.00	0.00	25.00	5.75	30.75
139	522.50.5.1.2.3.1.4.3	Jr. technician									1.50	37	55.50			55.50	0.00	55.50	12.77	68.27
140	522.50.5.1.2.3.2	CSC PAD (252K channels)																		*12383.08*
141	522.50.5.1.2.3.2.2	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
142	522.50.5.1.2.3.2.2	Prototype																		
143	522.50.5.1.2.3.2.2.1	High voltage																		
144	522.50.5.1.2.3.2.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
145	522.50.5.1.2.3.2.2.1.2	Distribution																		
146	522.50.5.1.2.3.2.2.2	Low voltage in-detector																		
147	522.50.5.1.2.3.2.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
148	522.50.5.1.2.3.2.2.2.2	Distribution																		
149	522.50.5.1.2.3.2.2.3	Signal cables																		
150	522.50.5.1.2.3.2.2.4	Active components																		
151	522.50.5.1.2.3.2.2.4.1	Preamp	2.00	154	308.00	40				150.00				3.00		308.00	193.00	501.00	110.22	611.22
152	522.50.5.1.2.3.2.2.4.2	Preamp test station	1.00	154	154.00	50				50.00				1.00		154.00	101.00	255.00	56.10	311.10
153	522.50.5.1.2.3.2.2.4.3	Discriminator	1.25	154	192.50	40				150.00				1.00		192.50	191.00	383.50	214.76	598.26
154	522.50.5.1.2.3.2.2.4.4	Digital pipeline	1.25	154	192.50	40				150.00				0.25		192.50	190.25	382.75	214.34	597.09
155	522.50.5.1.2.3.2.2.5	Printed circuit board																		
156	522.50.5.1.2.3.2.2.5.1	RFO	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	126.24	389.24
157	522.50.5.1.2.3.2.2.6	On-detector crate completed																		
158	522.50.5.1.2.3.2.2.7	Control/data links																		
159	522.50.5.1.2.3.2.2.7.1	Receiver & buffer	0.25	154	38.50											38.50	0.00	38.50	8.47	46.97
160	522.50.5.1.2.3.2.2.7.2	Optics	0.25	154	38.50											38.50	0.00	38.50	3.47	41.97
161	522.50.5.1.2.3.2.2.7.3	Rack slot																		
162	522.50.5.1.2.3.2.3	Production																		

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
163	522.50.5.1.2.3.2.3.1	High voltage																		
164	522.50.5.1.2.3.2.3.1.1	Power supply								150.00				15.00		0.00	165.00	165.00	19.80	184.80
165	522.50.5.1.2.3.2.3.1.2	Distribution	0.50	154	77.00					50.00				5.00		77.00	55.00	132.00	30.36	162.36
166	522.50.5.1.2.3.2.3.2	Low voltage in-detector																		
167	522.50.5.1.2.3.2.3.2.1	Power supply								100.00				10.00		0.00	110.00	110.00	17.60	127.60
168	522.50.5.1.2.3.2.3.2.2	Distribution	0.25	154	38.50					25.00				2.50		38.50	27.50	66.00	15.18	81.18
169	522.50.5.1.2.3.2.3.3	Signal cables																		
170	522.50.5.1.2.3.2.3.4	Active components																		
171	522.50.5.1.2.3.2.3.4.1	Preamp								756.00				3.00		0.00	759.00	759.00	166.98	925.98
172	522.50.5.1.2.3.2.3.4.2	Preamp testing								252.00				1.00		0.00	253.00	253.00	55.66	308.66
173	522.50.5.1.2.3.2.3.4.3	Discrimator								252.00				1.00		0.00	253.00	253.00	141.68	394.68
174	522.50.5.1.2.3.2.3.4.4	FIFO								252.00				1.00		0.00	253.00	253.00	141.68	394.68
175	522.50.5.1.2.3.2.3.4.5	ADC								756.00				3.00		0.00	759.00	759.00	425.04	1184.04
176	522.50.5.1.2.3.2.3.5	Printed circuit board																		
177	522.50.5.1.2.3.2.3.5.1	FIFO								3780.00				15.00		0.00	3795.00	3795.00	1821.60	5616.60
178	522.50.5.1.2.3.2.3.6	On-detector crate completed																		
179	522.50.5.1.2.3.2.3.7	Control/data links (252 links)																		
180	522.50.5.1.2.3.2.3.7.1	Receiver & buffer								22.68				2.27		0.00	24.95	24.95	5.49	30.44
181	522.50.5.1.2.3.2.3.7.2	Optics								63.00				6.30		0.00	69.30	69.30	6.24	75.54
182	522.50.5.1.2.3.2.3.7.3	Rack slot								7.56				0.76		0.00	8.32	8.32	1.33	9.65
183	522.50.5.1.2.3.2.4	Installation & test																		
184	522.50.5.1.2.3.2.4.1	Engineer									0.50	78	39.00			39.00	0.00	39.00	8.97	47.97
185	522.50.5.1.2.3.2.4.2	Sr. technician									0.50	50	25.00			25.00	0.00	25.00	5.75	30.75
186	522.50.5.1.2.3.2.4.3	Jr. technician									1.50	37	55.50			55.50	0.00	55.50	12.77	68.27
187																				
188	522.50.5.1.5	Central Tracker																		28462.56
189																				
190	522.50.5.1.5.1	PAD (446K channels)																		*21896.43*
191	522.50.5.1.5.1.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
192	522.50.5.1.5.1.2	Prototype																		
193	522.50.5.1.5.1.2.1	High voltage																		
194	522.50.5.1.5.1.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
195	522.50.5.1.5.1.2.1.2	Distribution																		
196	522.50.5.1.5.1.2.2	Low voltage in-detector																		
197	522.50.5.1.5.1.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
198	522.50.5.1.5.1.2.2.2	Distribution																		
199	522.50.5.1.5.1.2.3	Signal cables																		
200	522.50.5.1.5.1.2.4	Active components																		
201	522.50.5.1.5.1.2.4.1	Preamp	1.00	154	154.00	60				300.00				6.00		154.00	366.00	520.00	291.20	811.20
202	522.50.5.1.5.1.2.4.2	SCA	4.00	154	616.00	80				300.00				12.50		616.00	392.50	1008.50	564.76	1573.26
203	522.50.5.1.5.1.2.4.2	SCA test station	1.00	154	154.00	50				50.00				1.00		154.00	101.00	255.00	56.10	311.10
204	522.50.5.1.5.1.2.4.3	MUX	2.50	154	385.00	80				300.00				0.25		385.00	380.25	765.25	428.54	1193.79
205	522.50.5.1.5.1.2.5	Printed circuit board	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	126.24	389.24
206	522.50.5.1.5.1.2.6	On-detector crate completed																		
207	522.50.5.1.5.1.2.7	Control/data links																		
208	522.50.5.1.5.1.2.7.1	Receiver & buffer	0.25	154	38.50											38.50	0.00	38.50	8.47	46.97
209	522.50.5.1.5.1.2.7.2	Optics	0.25	154	38.50											38.50	0.00	38.50	3.47	41.97
210	522.50.5.1.5.1.3	Production																		
211	522.50.5.1.5.1.3.1	High voltage																		
212	522.50.5.1.5.1.3.1.1	Power supply								38.40				3.84		0.00	42.24	42.24	5.07	47.31
213	522.50.5.1.5.1.3.1.2	Distribution	0.50	154	77.00					12.80				1.28		77.00	14.08	91.08	20.95	112.03
214	522.50.5.1.5.1.3.2	Low voltage in-detector																		
215	522.50.5.1.5.1.3.2.1	Power supply								180.00				18.00		0.00	198.00	198.00	31.68	229.68
216	522.50.5.1.5.1.3.2.2	Distribution	0.25	154	38.50					45.00				4.50		38.50	49.50	88.00	20.24	108.24

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
217	522.50.5.1.5.1.3.3	Signal cables																		
218	522.50.5.1.5.1.3.4	Active components																		
219	522.50.5.1.5.1.3.4.1	Preamp								2676.00				6.00		0.00	2682.00	2682.00	1501.92	4183.92
220	522.50.5.1.5.1.3.4.2	SCA								5575.00				12.50		0.00	5587.50	5587.50	3129.00	8716.50
221	522.50.5.1.5.1.3.4.2	SCA test								446.00				1.00		0.00	447.00	447.00	98.34	545.34
222	522.50.5.1.5.1.3.4.3	MUX								112.00				0.25		0.00	112.25	112.25	62.86	175.11
223	522.50.5.1.5.1.3.5	Printed circuit board								1338.00				3.00		0.00	1341.00	1341.00	643.68	1984.68
224	522.50.5.1.5.1.3.6	On-detector crate completed																		
225	522.50.5.1.5.1.3.7	Control/data links (1745 links)																		
226	522.50.5.1.5.1.3.7.1	Receiver & buffer								157.10				15.71		0.00	172.81	172.81	38.02	210.83
227	522.50.5.1.5.1.3.7.2	Optics								436.30				43.63		0.00	479.93	479.93	43.19	523.12
228	522.50.5.1.5.1.3.7.3	Rack slot								52.40				5.24		0.00	57.64	57.64	9.22	66.86
229	522.50.5.1.5.1.4	Installation & test																		
230	522.50.5.1.5.1.4.1	Engineer									1.25	78	97.50			97.50	0.00	97.50	22.43	119.93
231	522.50.5.1.5.1.4.2	Sr. technician									1.25	50	62.50			62.50	0.00	62.50	14.38	76.88
232	522.50.5.1.5.1.4.3	Jr. technician									6.25	37	231.25			231.25	0.00	231.25	53.19	284.44
233																				
234	522.50.5.1.5.2	Wire (100K channels)																		6566.13
235	522.50.5.1.5.2.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
236	522.50.5.1.5.2.2	Prototype																		
237	522.50.5.1.5.2.2.1	High voltage																		
238	522.50.5.1.5.2.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
239	522.50.5.1.5.2.2.1.2	Distribution																		
240	522.50.5.1.5.2.2.2	Low voltage in-detector																		
241	522.50.5.1.5.2.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
242	522.50.5.1.5.2.2.2.2	Distribution																		
243	522.50.5.1.5.2.2.3	Signal cables																		
244	522.50.5.1.5.2.2.4	Active components																		
245	522.50.5.1.5.2.2.4.1	Preamp	1.00	154	154.00	60				300.00				6.00		154.00	366.00	520.00	291.20	811.20
246	522.50.5.1.5.2.2.4.2	Disc. & pipeline	2.50	154	385.00	80				300.00				4.00		385.00	384.00	769.00	430.64	1199.64
247	522.50.5.1.5.2.2.4.4	MUX	2.50	154	385.00	80				300.00				0.25		385.00	380.25	765.25	428.54	1193.79
248	522.50.5.1.5.2.2.5	Printed circuit board	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	126.24	389.24
249	522.50.5.1.5.2.2.6	On-detector crate completed																		
250	522.50.5.1.5.2.2.7	Control/data links																		
251	522.50.5.1.5.2.2.7.1	Receiver & buffer	0.25	154	38.50											38.50	0.00	38.50	8.47	46.97
252	522.50.5.1.5.2.2.7.2	Optics	0.25	154	38.50											38.50	0.00	38.50	3.47	41.97
253	522.50.5.1.5.2.3	Production																		
254	522.50.5.1.5.2.3.1	High voltage																		
255	522.50.5.1.5.2.3.1.1	Power supply																		
256	522.50.5.1.5.2.3.1.2	Distribution																		
257	522.50.5.1.5.2.3.2	Low voltage in-detector																		
258	522.50.5.1.5.2.3.2.1	Power supply								40.00				4.00		0.00	44.00	44.00	7.04	51.04
259	522.50.5.1.5.2.3.2.2	Distribution	0.25	154	38.50					10.00				1.00		38.50	11.00	49.50	11.39	60.89
260	522.50.5.1.5.2.3.3	Signal cables																		
261	522.50.5.1.5.2.3.4	Active components																		
262	522.50.5.1.5.2.3.4.1	Preamp								600.00				6.00		0.00	606.00	606.00	339.36	945.36
263	522.50.5.1.5.2.3.4.2	Disc. & pipeline								400.00				4.00		0.00	404.00	404.00	226.24	630.24
264	522.50.5.1.5.2.3.4.4	MUX								25.00				0.25		0.00	25.25	25.25	14.14	39.39
265	522.50.5.1.5.2.3.5	Printed circuit board								300.00				3.00		0.00	303.00	303.00	145.44	448.44
266	522.50.5.1.5.2.3.6	On-detector crate completed																		
267	522.50.5.1.5.2.3.7	Control/data links (390 links)																		
268	522.50.5.1.5.2.3.7.1	Receiver & buffer								35.10				3.51		0.00	38.61	38.61	8.49	47.10
269	522.50.5.1.5.2.3.7.2	Optics								97.50				9.75		0.00	107.25	107.25	9.65	116.90
270	522.50.5.1.5.2.3.7.3	Rack slot								11.70				1.17		0.00	12.87	12.87	2.06	14.93

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
271	522.50.5.1.5.2.4	Installation & test																		
272	522.50.5.1.5.2.4.1	Engineer									1.00	78	78.00			78.00	0.00	78.00	17.94	95.94
273	522.50.5.1.5.2.4.2	Sr. technician									1.00	50	50.00			50.00	0.00	50.00	11.50	61.50
274	522.50.5.1.5.2.4.3	Jr. technician									5.00	37	185.00			185.00	0.00	185.00	42.55	227.55
275																				
276	522.50.5.1.6	Generic development																		1049.83
277																				
278	522.50.5.1.6.1	Design/documentation	0.50	154	77.00											77.00	0.00	77.00	16.17	93.17
279	522.50.5.1.6.2	Prototype																		
280	522.50.5.1.6.2.1	Low voltage power supply	1.00	154	154.00											154.00	0.00	154.00	24.64	178.64
281	522.50.5.1.6.2.2	On-detector crate	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	42.08	305.08
282	522.50.5.1.6.2.3	Control/data link	1.00	154	154.00											154.00	0.00	154.00	13.86	167.86
283	522.50.5.1.6.2.4	Receiver & buffer board	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	42.08	305.08
284																				
285	522.50.5.1.8	Calorimeter (80K channels)																		18499.37
286																				
287	522.50.5.1.8.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
288	522.50.5.1.8.2	Prototype																		
289	522.50.5.1.8.2.1	High voltage																		
290	522.50.5.1.8.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
291	522.50.5.1.8.2.1.2	Distribution																		
292	522.50.5.1.8.2.2	Low voltage in-detector																		
293	522.50.5.1.8.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
294	522.50.5.1.8.2.2.2	Distribution																		
295	522.50.5.1.8.2.3	Signal cables				40										0.00	40.00	40.00	2.80	42.80
296	522.50.5.1.8.2.4	Active components																		
297	522.50.5.1.8.2.4.1	Preamp	0.50	154	77.00	30				150.00				16.00		77.00	196.00	273.00	60.06	333.06
298	522.50.5.1.8.2.4.2	Switch capacitor array	2.00	154	308.00	40				150.00				12.00		308.00	202.00	510.00	112.20	622.20
299	522.50.5.1.8.2.4.3	SCA test station	1.00	154	154.00	50				50.00				2.00		154.00	102.00	256.00	56.32	312.32
300	522.50.5.1.8.2.4.4	ADC	2.00	154	308.00	40				150.00				12.00		308.00	202.00	510.00	112.20	622.20
301	522.50.5.1.8.2.4.5	ADC test station	1.00	154	154.00	50				50.00				2.00		154.00	102.00	256.00	56.32	312.32
302	522.50.5.1.8.2.4.6	Calibration system	0.50	154	77.00	30				150.00				2.00		77.00	182.00	259.00	56.98	315.98
303	522.50.5.1.8.2.5	Printed circuit board																		
304	522.50.5.1.8.2.5.1	Shaper & driver	0.55	154	84.70	4				16.00				1.60		84.70	21.60	106.30	23.39	129.69
305	522.50.5.1.8.2.5.2	Preamp	0.55	154	84.70	4				16.00				1.60		84.70	21.60	106.30	23.39	129.69
306	522.50.5.1.8.2.5.3	ADC	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	126.24	389.24
307	522.50.5.1.8.2.5.4	Calibration system	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	126.24	389.24
308	522.50.5.1.8.2.6	On-detector crate completed																		
309	522.50.5.1.8.2.7	Control/data links																		
310	522.50.5.1.8.2.7.1	Receiver & buffer	0.25	154	38.50											38.50	0.00	38.50	8.47	46.97
311	522.50.5.1.8.2.7.2	Optics	0.25	154	38.50											38.50	0.00	38.50	3.47	41.97
312	522.50.5.1.8.3	Production																		
313	522.50.5.1.8.3.1	High voltage																		
314	522.50.5.1.8.3.1.1	Power supply								150.00				15.00		0.00	165.00	165.00	19.80	184.80
315	522.50.5.1.8.3.1.2	Distribution	0.50	154	77.00					50.00				5.00		77.00	55.00	132.00	30.36	162.36
316	522.50.5.1.8.3.2	Low voltage in-detector																		
317	522.50.5.1.8.3.2.1	Power supply								64.00				6.40		0.00	70.40	70.40	11.26	81.66
318	522.50.5.1.8.3.2.2	Distribution	0.25	154	38.50					16.00				1.60		0.00	17.60	17.60	4.05	21.65
319	522.50.5.1.8.3.3	Signal cables								650.00				1.50		38.50	651.50	690.00	48.30	738.30
320	522.50.5.1.8.3.4	Active components																		
321	522.50.5.1.8.3.4.1	Preamp								480.00				6.00		0.00	486.00	486.00	106.92	592.92
322	522.50.5.1.8.3.4.2	SCA								480.00				6.00		0.00	486.00	486.00	106.92	592.92
323	522.50.5.1.8.3.4.3	SCA testing								160.00				2.00		0.00	162.00	162.00	35.64	197.64
324	522.50.5.1.8.3.4.4	ADC/MUX								480.00				6.00		0.00	486.00	486.00	106.92	592.92

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
325	522.50.5.1.8.3.4.5	ADC/MUX tesing								160.00				2.00		0.00	162.00	162.00	35.64	197.64
326	522.50.5.1.8.3.4.6	Trigger FADC								240.00				3.00		0.00	243.00	243.00	53.46	296.46
327	522.50.5.1.8.3.4.7	Calibration system								480.00				6.00		0.00	486.00	486.00	106.92	592.92
328	522.50.5.1.8.3.5	Printed circuit board																		
329	522.50.5.1.8.3.5.1	Shaper/driver								640.00				64.00		0.00	704.00	704.00	154.88	858.88
330	522.50.5.1.8.3.5.2	Preamp								160.00				16.00		0.00	176.00	176.00	38.72	214.72
331	522.50.5.1.8.3.5.3	ADC								3600.00				360.00		0.00	3960.00	3960.00	1900.80	5860.80
332	522.50.5.1.8.3.5.4	Calibration system								240.00				3.00		0.00	243.00	243.00	116.64	359.64
333	522.50.5.1.8.3.6	On-detector crate completed								2060.00				206.00		0.00	2266.00	2266.00	362.56	2628.56
334	522.50.5.1.8.3.7	Control/data links (80 links)																		
335	522.50.5.1.8.3.7.1	Receiver & buffer								7.20				0.72		0.00	7.92	7.92	1.27	9.19
336	522.50.5.1.8.3.7.2	Optics								20.00				2.00		0.00	22.00	22.00	1.98	23.98
337	522.50.5.1.8.3.7.3	Rack slot								2.40				0.24		0.00	2.64	2.64	0.42	3.06
338	522.50.5.1.8.4	Installation & test																		
339	522.50.5.1.8.4.1	Engineer									2.25	78	175.50			175.50	0.00	175.50	40.37	215.87
340	522.50.5.1.8.4.2	Sr. technician									2.25	50	112.50			112.50	0.00	112.50	25.88	138.38
341	522.50.5.1.8.4.3	Jr. technician									2.25	37	83.25			83.25	0.00	83.25	19.15	102.40
342																				
343	522.50.5.1.10	SI. Pre-radiator (14K ch.)																		5479.90
344																				
345	522.50.5.1.10.1	Design/documentation																		
346	522.50.5.1.10.2	Prototype																		
347	522.50.5.1.10.2.1	High voltage																		
348	522.50.5.1.10.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
349	522.50.5.1.10.2.1.2	Distribution																		
350	522.50.5.1.10.2.2	Low voltage in-detector																		
351	522.50.5.1.10.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
352	522.50.5.1.10.2.2.2	Distribution																		
353	522.50.5.1.10.2.3	Signal cables																		
354	522.50.5.1.10.2.4	Active components																		
355	522.50.5.1.10.2.4.1	Preamp	1.00	154	154.00	60				300.00				3.00		154.00	363.00	517.00	289.52	806.52
356	522.50.5.1.10.2.4.2	Switch capacitor array	4.00	154	616.00	80				300.00				6.00		616.00	386.00	1002.00	561.12	1563.12
357	522.50.5.1.10.2.4.3	SCA test station	1.00	154	154.00	50				50.00				1.00		154.00	101.00	255.00	56.10	311.10
358	522.50.5.1.10.2.4.4	MUX	2.50	154	385.00	80				300.00				0.20		385.00	380.20	765.20	428.51	1193.71
359	522.50.5.1.10.2.5	Printed circuit board	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	126.24	389.24
360	522.50.5.1.10.2.6	On-detector crate completed																		
361	522.50.5.1.10.2.7	Control/data links																		
362	522.50.5.1.10.2.7.1	Receiver & buffer	0.25	154	38.50											38.50	0.00	38.50	8.47	46.97
363	522.50.5.1.10.2.7.2	Optics	0.25	154	38.50											38.50	0.00	38.50	3.47	41.97
364	522.50.5.1.10.3	Production																		
365	522.50.5.1.10.3.1	High voltage																		
366	522.50.5.1.10.3.1.1	Power supply								135.00				13.50		0.00	148.50	148.50	17.82	166.32
367	522.50.5.1.10.3.1.2	Distribution	0.50	154	77.00					45.00				4.50		77.00	49.50	126.50	29.10	155.60
368	522.50.5.1.10.3.2	Low voltage in-detector																		
369	522.50.5.1.10.3.2.1	Power supply								6.00				0.60		0.00	6.60	6.60	1.06	7.66
370	522.50.5.1.10.3.2.2	Distribution	0.25	154	38.50					1.50				0.15		38.50	1.65	40.15	9.23	49.38
371	522.50.5.1.10.3.3	Signal cables								45.00				4.50		0.00	49.50	49.50	3.47	52.97
372	522.50.5.1.10.3.4	Active components																		
373	522.50.5.1.10.3.4.1	Preamp								42.60				3.00		0.00	45.60	45.60	25.54	71.14
374	522.50.5.1.10.3.4.2	SCA								85.30				6.00		0.00	91.30	91.30	51.13	142.43
375	522.50.5.1.10.3.4.3	SCA testing								14.20				1.00		0.00	15.20	15.20	3.34	18.54
376	522.50.5.1.10.3.4.4	MUX								2.30				0.20		0.00	2.50	2.50	1.40	3.90
377	522.50.5.1.10.3.5	Printed circuit board								213.10				15.00		0.00	228.10	228.10	109.49	337.59
378	522.50.5.1.10.3.6	On-detector crate completed																		

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
379	522.50.5.1.10.3.7	Control/data links (74 links)																		
380	522.50.5.1.10.3.7.1	Receiver & buffer								6.70				0.67		0.00	7.37	7.37	1.62	8.99
381	522.50.5.1.10.3.7.2	Optics								18.50				1.85		0.00	20.35	20.35	1.83	22.18
382	522.50.5.1.10.3.7.3	Rack slot								2.20				0.22		0.00	2.42	2.42	0.39	2.81
383	522.50.5.1.10.4	Installation & test																		
384	522.50.5.1.10.4.1	Engineer																		
385	522.50.5.1.10.4.2	Sr. technician																		
386	522.50.5.1.10.4.3	Jr. technician																		
387																				
388	522.50.5.2	**Data Acquisition**																		
389																				
390	522.50.5.3	**Trigger**																		20550.59
391																				
392	522.50.5.3.1	**Level 1**																		*17348.22*
393																				
394	522.50.5.3.1.1	Calorimeter (2960 channels)																		9652.35
395	522.50.5.3.1.1.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
396	522.50.5.3.1.1.2	Prototype																		
397	522.50.5.3.1.1.2.1	High voltage																		
398	522.50.5.3.1.1.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
399	522.50.5.3.1.1.2.1.2	Distribution																		
400	522.50.5.3.1.1.2.2	Low voltage in-detector																		
401	522.50.5.3.1.1.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
402	522.50.5.3.1.1.2.2.2	Distribution																		
403	522.50.5.3.1.1.2.3	Signal cables																		
404	522.50.5.3.1.1.2.4	Active components																		
405	522.50.5.3.1.1.2.4.1	SUM chip	1.25	154	192.50	40				150.00				15.00		192.50	205.00	397.50	87.45	484.95
406	522.50.5.3.1.1.2.4.2	ISOLATION chip	1.25	154	192.50	40				150.00				15.00		192.50	205.00	397.50	87.45	484.95
407	522.50.5.3.1.1.2.5	Printed circuit board																		
408	522.50.5.3.1.1.2.5.1	Energy SUM	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
409	522.50.5.3.1.1.2.5.2	Isolation	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
410	522.50.5.3.1.1.2.6	On-detector crate completed																		
411	522.50.5.3.1.1.2.7	Control/data links																		
412	522.50.5.3.1.1.2.7.1	Receiver & buffer	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
413	522.50.5.3.1.1.2.7.2	Optics																		
414	522.50.5.3.1.1.3	Production																		
415	522.50.5.3.1.1.3.1	High voltage																		
416	522.50.5.3.1.1.3.1.1	Power supply																		
417	522.50.5.3.1.1.3.1.2	Distribution																		
418	522.50.5.3.1.1.3.2	Low voltage in-detector																		
419	522.50.5.3.1.1.3.2.1	Power supply																		
420	522.50.5.3.1.1.3.2.2	Distribution																		
421	522.50.5.3.1.1.3.3	Signal cables																		
422	522.50.5.3.1.1.3.4	Active components																		
423	522.50.5.3.1.1.3.4.1	SUM chip								300.00				30.00		0.00	330.00	330.00	72.60	402.60
424	522.50.5.3.1.1.3.4.2	ISOLATION chip								300.00				30.00		0.00	330.00	330.00	72.60	402.60
425	522.50.5.3.1.1.3.5	Printed circuit board																		
426	522.50.5.3.1.1.3.5.1	Energy SUM								600.00				60.00		0.00	660.00	660.00	145.20	805.20
427	522.50.5.3.1.1.3.5.2	Isolation								990.00				99.00		0.00	1089.00	1089.00	239.58	1328.58
428	522.50.5.3.1.1.3.6	On-detector crate completed								477.00				47.70		0.00	524.70	524.70	83.95	608.65
429	522.50.5.3.1.1.3.7	Control/data links																		
430	522.50.5.3.1.1.3.7.1	Receiver & buffer								278.24				27.82		0.00	306.06	306.06	67.33	373.40
431	522.50.5.3.1.1.3.7.2	Optics								2960.00				296.00		0.00	3256.00	3256.00	293.04	3549.04
432	522.50.5.3.1.1.3.7.3	Rack slot								82.88				8.29		0.00	91.17	91.17	14.59	105.75

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
433	522.50.5.3.1.1.4	Installation & test																		
434	522.50.5.3.1.1.4.1	Engineer																		
435	522.50.5.3.1.1.4.2	Sr. technician																		
436	522.50.5.3.1.1.4.3	Jr. technician																		
437																				
438	522.50.5.3.1.2	Muon																		7695.87
439	522.50.5.3.1.2.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
440	522.50.5.3.1.2.2	Prototype																		
441	522.50.5.3.1.2.2.1	High voltage																		
442	522.50.5.3.1.2.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
443	522.50.5.3.1.2.2.1.2	Distribution																		
444	522.50.5.3.1.2.2.2	Low voltage in-detector																		
445	522.50.5.3.1.2.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
446	522.50.5.3.1.2.2.2.2	Distribution																		
447	522.50.5.3.1.2.2.3	Signal cables																		
448	522.50.5.3.1.2.2.4	Active components																		
449	522.50.5.3.1.2.2.4.1	Encoder in Encap	1.25	154	192.50	40				150.00				15.00		192.50	205.00	397.50	87.45	484.95
450	522.50.5.3.1.2.2.4.2	Memory in Encap	1.25	154	192.50	40				150.00				15.00		192.50	205.00	397.50	87.45	484.95
451	522.50.5.3.1.2.2.4.3	Digital chip in Barrel	1.25	154	192.50	40				150.00				15.00		192.50	205.00	397.50	87.45	484.95
452	522.50.5.3.1.2.2.5	Printed circuit board																		
453	522.50.5.3.1.2.2.5.1	Programmable gate array	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
454	522.50.5.3.1.2.2.5.2	Memory	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
455	522.50.5.3.1.2.2.5.3	CAM	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
456	522.50.5.3.1.2.2.5.4	Digital chip in Barrel	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
457	522.50.5.3.1.2.2.6	On-detector crate completed																		
458	522.50.5.3.1.2.2.7	Control/data links																		
459	522.50.5.3.1.2.2.7.1	Receiver & buffer	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
460	522.50.5.3.1.2.2.7.2	Optics																		
461	522.50.5.3.1.2.3	Production																		
462	522.50.5.3.1.2.3.1	High voltage																		
463	522.50.5.3.1.2.3.1.1	Power supply																		
464	522.50.5.3.1.2.3.1.2	Distribution																		
465	522.50.5.3.1.2.3.2	Low voltage in-detector																		
466	522.50.5.3.1.2.3.2.1	Power supply																		
467	522.50.5.3.1.2.3.2.2	Distribution																		
468	522.50.5.3.1.2.3.3	Signal cables																		
469	522.50.5.3.1.2.3.4	Active components																		
470	522.50.5.3.1.2.3.4.1	Encoder in Encap								256.00				25.60		0.00	281.60	281.60	61.95	343.55
471	522.50.5.3.1.2.3.4.2	Memory in Encap								25.00				2.50		0.00	27.50	27.50	6.05	33.55
472	522.50.5.3.1.2.3.4.3	CAM								51.20				5.12		0.00	56.32	56.32	12.39	68.71
473	522.50.5.3.1.2.3.4.4	Digital chip in Barrel								300.00				30.00		0.00	330.00	330.00	72.60	402.60
474	522.50.5.3.1.2.3.5	Printed circuit board																		
475	522.50.5.3.1.2.3.5.1	PGA								856.00				85.60		0.00	941.60	941.60	207.15	1148.75
476	522.50.5.3.1.2.3.5.2	Memory								375.00				37.50		0.00	412.50	412.50	90.75	503.25
477	522.50.5.3.1.2.3.5.3	CAM								96.00				9.60		0.00	105.60	105.60	23.23	128.83
478	522.50.5.3.1.2.3.5.4	Digital chip in Barrel								400.00				40.00		0.00	440.00	440.00	96.80	536.80
479	522.50.5.3.1.2.3.6	On-detector crate completed								381.40				38.14		0.00	419.54	419.54	67.13	486.67
480	522.50.5.3.1.2.3.7	Control/data links																		
481	522.50.5.3.1.2.3.7.1	Receiver & buffer								67.50				6.75		0.00	74.25	74.25	16.34	90.59
482	522.50.5.3.1.2.3.7.2	Optics								625.00				62.50		0.00	687.50	687.50	61.88	749.38
483	522.50.5.3.1.2.3.7.3	Rack slot																		
484	522.50.5.3.1.2.4	Installation & test																		
485	522.50.5.3.1.2.4.1	Engineer																		
486	522.50.5.3.1.2.4.2	Sr. technician																		

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
487	522.50.5.3.1.2.4.3	Jr. technician																		
488																				
489	522.50.5.3.2	Level 2																		3202.37
490																				
491	522.50.5.3.2.1	Design/documentation					0.50	93	46.50							46.50	0.00	46.50	9.77	56.27
492	522.50.5.3.2.2	Prototype																		
493	522.50.5.3.2.2.1	High voltage																		
494	522.50.5.3.2.2.1.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	4.62	43.12
495	522.50.5.3.2.2.1.2	Distribution																		
496	522.50.5.3.2.2.2	Low voltage in-detector																		
497	522.50.5.3.2.2.2.1	Power supply	0.25	154	38.50											38.50	0.00	38.50	6.16	44.66
498	522.50.5.3.2.2.2.2	Distribution																		
499	522.50.5.3.2.2.3	Signal cables																		
500	522.50.5.3.2.2.4	Active components																		
501	522.50.5.3.2.2.4.1	Programming effort	1.00	154	154.00											154.00	0.00	154.00	33.88	187.88
502	522.50.5.3.2.2.5	Printed circuit board																		
503	522.50.5.3.2.2.5.1	Programmable gate array	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
504	522.50.5.3.2.2.5.2	Memory	1.50	154	231.00	10				20.00				2.00		231.00	32.00	263.00	57.86	320.86
505	522.50.5.3.2.2.6	On-detector crate completed																		
506	522.50.5.3.2.2.7	Control/data links																		
507	522.50.5.3.2.2.7.1	Receiver & buffer																		
508	522.50.5.3.2.2.7.2	Optics																		
509	522.50.5.3.2.3	Production																		
510	522.50.5.3.2.3.1	High voltage																		
511	522.50.5.3.2.3.1.1	Power supply																		
512	522.50.5.3.2.3.1.2	Distribution																		
513	522.50.5.3.2.3.2	Low voltage in-detector																		
514	522.50.5.3.2.3.2.1	Power supply																		
515	522.50.5.3.2.3.2.2	Distribution																		
516	522.50.5.3.2.3.3	Signal cables																		
517	522.50.5.3.2.3.4	Active components																		
518	522.50.5.3.2.3.5	Printed circuit board																		
519	522.50.5.3.2.3.5.1	Calorimeter board								600.00				30.00		0.00	630.00	630.00	138.60	768.60
520	522.50.5.3.2.3.5.2	Processor board								60.00				6.00		0.00	66.00	66.00	14.52	80.52
521	522.50.5.3.2.3.6	On-detector crate completed																		
522	522.50.5.3.2.3.7	Control/data links																		
523	522.50.5.3.2.3.7.1	Receiver & buffer								282.00				28.20		0.00	310.20	310.20	68.24	378.44
524	522.50.5.3.2.3.7.2	Optics								750.00				75.00		0.00	825.00	825.00	74.25	899.25
525	522.50.5.3.2.3.7.3	Rack slot								85.00				8.50		0.00	93.50	93.50	8.42	101.92
526	522.50.5.3.2.4	Installation & test																		
527	522.50.5.3.2.4.1	Engineer																		
528	522.50.5.3.2.4.2	Sr. technician																		
529	522.50.5.3.2.4.3	Jr. technician																		
530																				
531																				
532																				
533																				
534																				
535																				
536																				
537																				
538																				
539																				

ELECTRONIC COST SUMMARY

	Channel Count (K)	Prototype k$	Prototype Cont.(%)	Production Cont. (%)	Cost per channel	Total Cost (k$)
Muon						
RPC	85	585.7	19.5	18.9	48.75	5629.97
PDT/LSDT	133	1253.2	37.1	32	48.9	10305.58
CSC Wire	133(?)	949.8	34.5	30.4	8.19	2700.28
CSC PAD	252	1985.7	37.9	42.5	26.85	12383.08
Central Tracker						
Inner						
Outer PAD	446	3012.2	49.7	48.7	26.21	21896.43
Outer Wire	100	2517.7	51.9	43.9	19.03	6566.13
Calorimeter						
LA (no forward cal.)	80	3043.1	25.9	29.3	141.7	18499.37
Pre-radiator	14	2956.2	50.2	32.5	56.0	5479.9

μ trigger not in this

Silicon Tracker Electronics Cost Review

Part II

- Fiber Optic Data Link
- Power Supplies
- Slow Control
- Assemly Test Stations
- Data Acquisition System

Geoff Mills

LANL

Fiber Optic Data Link

- **Component Procurement**

	Number	Cost
Fiber&Connectors	2917	$65
Transmitter &Receiver	"	$60
Total		390k$

- **Labor (FTE)**

	Staff	Technical
Engineering/Design	0.5	0.25
Inspection/Admin.	0.1	0.5
Assembly/Installation	0.1	1.0
Total	0.7	1.75

- **Materials & Supplies for EDIA**

	k$
M&S	50

- **Risk and Contingency**

	Risk Factor	Contingency(%)
Technical	6	12
Cost	4	4
Schedule	4	4
Total		20

- **Total Cost** **730k$**

Power Supplies

- **Component Procurement**

	Number	Cost
Power Supplies	30	2k$
Bias Supplies	200	$150
Total 90k$		

- **Labor (FTE)**

	Staff	Technical
Engineering/Design	0.2	0.5
Inspection/Admin.	0.1	0.1
Assembly/Installation	0.0	0.2
Total	0.3	0.8

- **Materials & Supplies for EDIA**

	k$
M&S	10

- **Risk and Contingency**

	Risk Factor	Contingency(%)
Technical	3	6
Cost	10	10
Schedule	2	2
Total		18

- **Total Cost** **280k$**

Slow Control System

- **Component Procurement**

	Number	Cost
Temperature	1	25k$
Interlock	1	25k$

- **Labor (FTE)**

	Staff	Technical
Engineering/Design	0.25	0.5
Inspection/Admin.	0.0	0.5
Assembly/Installation	0.0	0.0
Total	0.25	1.0

- **Materials & Supplies for EDIA**

	k$
M&S	10

- **Risk and Contingency**

	Risk Factor	Contingency(%)
Technical	3	6
Cost	10	10
Schedule	2	2
Total		18

- **Total Cost** **200k$**

Assembly Test Stations

- **Component Procurement**

	Number	Cost
Ladder Test Station	1	50k$
Shell Test Station	1	50k$
Tracker Test Station	1	50k$
Total		150k$

- **Labor (FTE)**

	Staff	Technical
Engineering/Design	0.5	0.5
Inspection/Admin.	0.2	0.0
Assembly/Installation	0.0	0.0
Total	0.7	0.5

- **Materials & Supplies for EDIA**

	k$
M&S	20

- **Risk and Contingency**

	Risk Factor	Contingency(%)
Technical	6	12
Cost	15	15
Schedule	8	8
Total		35

- **Total Cost** **330k$**

Data Acquisition

- **Component Procurement**

	Number	Cost
Crate & Controller	3	20k$
FastBus Module	57	3k$
Total	231k$	

- **Labor (FTE)**

	Staff	Technical
Engineering/Design	0.5	0.5
Inspection/Admin.	0.2	0.2
Assembly/Installation	0.2	0.2
Total	0.9	0.9

- **Materials & Supplies for EDIA**

	k$
M&S	100

- **Risk and Contingency**

	Risk Factor	Contingency(%)
Technical	6	12
Cost	6	6
Schedule	2	2
Total		20

- **Total Cost** **560k$**

Electronics Cost

Number of MCM	5304
Channels per MCM	640
Total Channel Count	3.39E+06
MCM's per Data Link	2
Number of Data Links	2917

Bipolar VLSI

Cost per Wafer	$3,500
Yield	0.5
Good Area	3142
Die Area	40.96
Good Die per Wafer	76
Cost per Die	$46
Channels per Die	128
Cost Per Channel	$0.36
Total Number of Good Die	26520
Total Bipolar Cost	$1,221,316

CMOS-1 Digital Buffer

Cost per Wafer	$2,800
CMOS Yield	0.35
Good Area	4948
Die Area	76.8
Good Die per Wafer	64
Cost per Die	$44
Channels per Die	128
Cost Per Channel	$0.34
Total Number of Good Die	26520
Total CMOS Cost	$1,160,250

CMOS-2 Controller Chip

Cost per Wafer	$3,500
CMOS Yield	0.40
Good Area	5655
Die Area	64
Good Die per Wafer	88
Cost per Die	$40
Total Number of Good Die	5304
Total CMOS Cost	$210,955

MCM

Area (mm)	1200
Cost per Area	$0.12
Cost Per MCM	$144
Wafer Prep	$110,000
Total MCM Cost	$873,776

Fiber Optic Data Link	
Fiber & Connector Costs	$65
Transmitter/Receiver	$70
Cost per Data Link	$135
Total Data Link Cost	$393,795
Cables	
Number of Cables	192
Cable Cost	$2,500
Total Cable Cost	$480,000
Power Supply System	
Low Voltage Supplies	30
Supply Cost	$2,000
Bias Voltage Channels	200
Channel Cost	$150
Total Supply Cost	$90,000
Slow Control	
Temperature System	$25,000
Interlock System	$25,000
Total Slow Control Cost	$50,000
Assembly Test Stations	
Ladder Assembly	$50,000
Shell Assembly	$50,000
Tracker Assembly	$50,000
Total Test Station Cost	$150,000
Data Acquisition	
Number of modules	57
Cost per Module	$3,000
Total Module Cost	$171,288
Number of Crates	3
Cost per Crate (& controller)	$20,000
Total Crate Cost	$60,000
Total Data Acquisition Cost	$231,288

GEMCT Cost Worksheet

WBS	Item	E/D Labor S	E/D Labor T	E/D A M&S (M$)	I/A Labor S	I/A Labor T	Proc/Fab (M$)	Inst/Assy Labor S	Inst/Assy Labor T	Inst/Assy M&S	Subtotal	Contingency	Total
5.1.3 Detector Electronics													
	5.1.3.1 Bipolar	1.25	1.50	0.41	0.25	1.00	1.22	0.00	0.00	0.00	2.12	32%	2.80
	5.1.3.2 CMOS	1.50	2.00	0.41	0.20	1.00	1.16	0.00	0.00	0.00	2.14	42%	3.04
	5.1.3.3 Controller	1.00	0.50	0.17	0.20	0.50	0.21	0.00	0.00	0.00	0.66	42%	0.94
	5.1.3.4 MCM	0.50	0.25	0.09	0.50	1.00	0.87	0.00	0.00	0.00	1.24	36%	1.69
	5.1.3.5 Fiber Optics	0.50	0.25	0.05	0.10	0.50	0.39	0.10	1.00	0.05	0.73	20%	0.88
	5.1.3.6 Power Supply	0.20	0.50	0.01	0.10	0.10	0.09	0.00	0.20	0.00	0.28	18%	0.33
	5.1.3.7 Cabling	0.25	0.20	0.05	0.10	0.00	0.48	0.10	2.00	0.00	0.83	54%	1.27
	5.1.3.8 Slow Control	0.25	0.50	0.01	0.00	0.50	0.05	0.00	0.00	0.00	0.20	18%	0.24
	5.1.3.9 Test Stations	0.50	0.50	0.02	0.20	0.00	0.15	0.00	0.00	0.00	0.33	35%	0.44
													0.00
5.1.4 Data Acquisition													0.00
	5.1.4.1 DAC	0.50	0.50	0.10	0.20	0.20	0.23	0.20	0.20		0.56	20%	0.68
	Total	6.45	6.70	1.31	1.85	4.80	4.86	0.40	2.40		8.94		12.31
	Total (M$)	0.99	0.69	1.31	0.28	0.49	4.86	0.06	0.25				

Grand Total: 8.94 M$ + 3.36 M$ Contingency

Staff Rate	0.154
Tech Rate	0.103

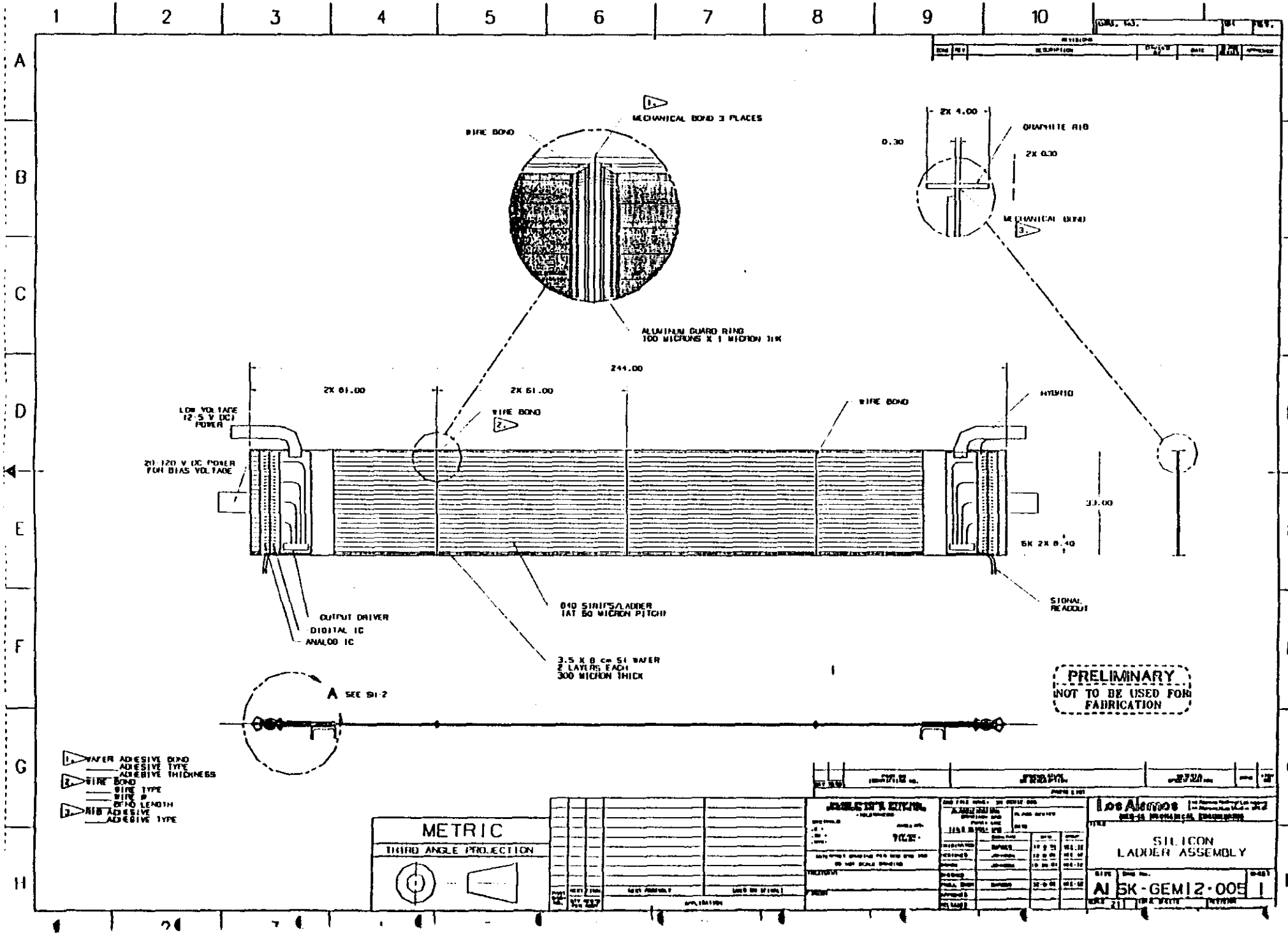
GEM/Silicon Tracker
Front-End Electronics Cost Estimates

(for Micro Circuits, Multi-Chip Modules, Cables)

4-22-92

Sangkoo Hahn
Brad Cooke

Los Alamos National Laboratory


MECHANICAL BOND 3 PLACES
WIRE BOND
ALUMINUM GUARD RING
100 MICRONS X 1 MICRON THK
2X 4.00
0.30
GRAPHITE RIB
2X 0.30
MECHANICAL BOND
244.00
2X 61.00
2X 61.00
WIRE BOND
WIRE BOND
HYBRID
LOW VOLTAGE
12.5 V DC
POWER
20-120 V DC POWER
FOR BIAS VOLTAGE
33.00
5X 2X 0.40
SIGNAL
READOUT
OUTPUT DRIVER
DIGITAL IC
ANALOG IC
040 STRIPS/LADDER
(AT 50 MICRON PITCH)
3.5 X 8 cm SI WAFER
2 LAYERS EACH
300 MICRON THICK
A SEE SH-2
PRELIMINARY
NOT TO BE USED FOR
FABRICATION
WAFER ADHESIVE BOND
ADHESIVE TYPE
ADHESIVE THICKNESS
WIRE BOND
WIRE TYPE
WIRE Ø
BOND LENGTH
RIB ADHESIVE
ADHESIVE TYPE
METRIC
THIRD ANGLE PROJECTION
Los Alamos
SILICON
LADDER ASSEMBLY
A1 5K-GEM12-005 1

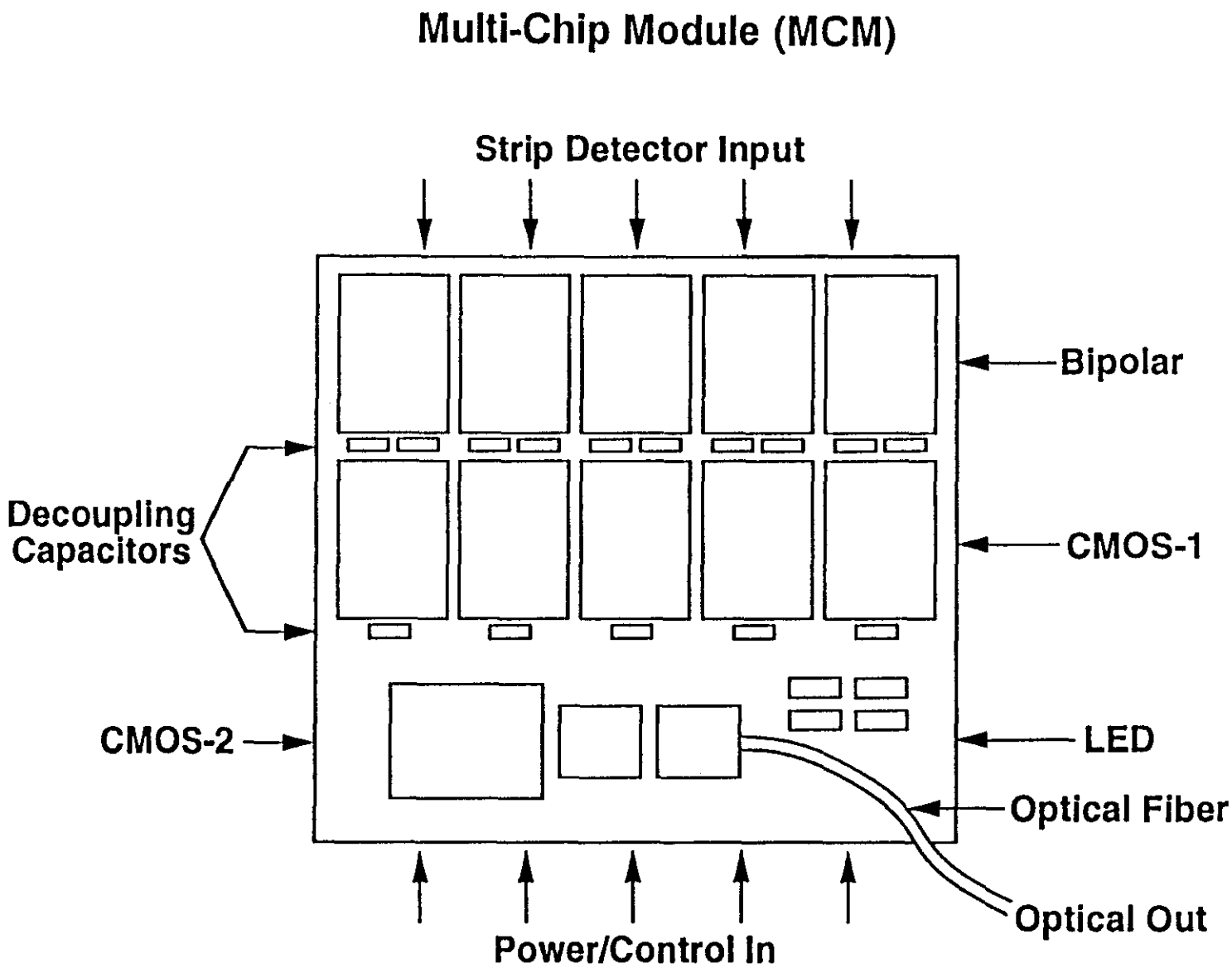


Fig. 1. Conceptual Layout of Si-Tracker MCM

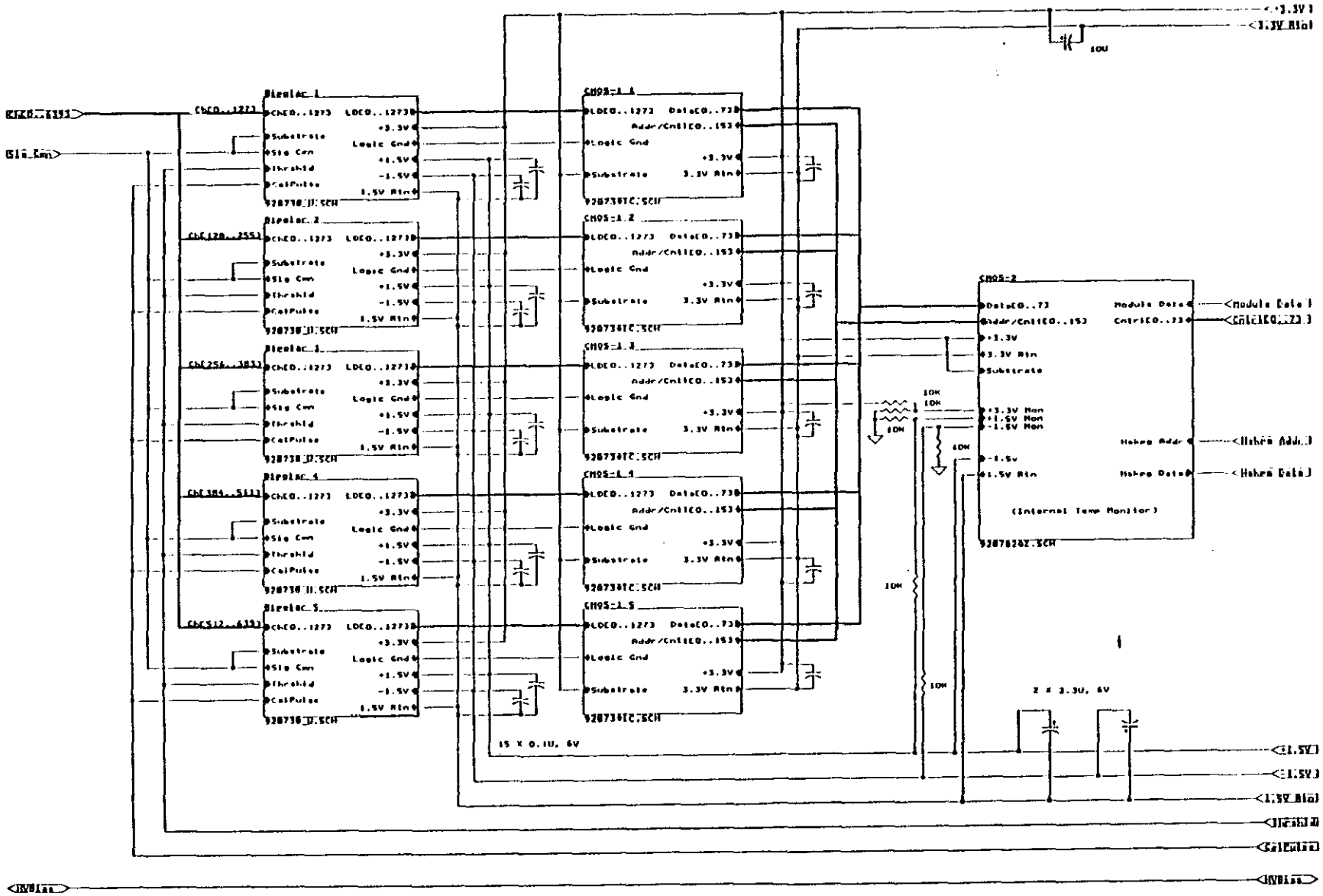


Figure 2. Multi-Chip Module for Si-Tracker

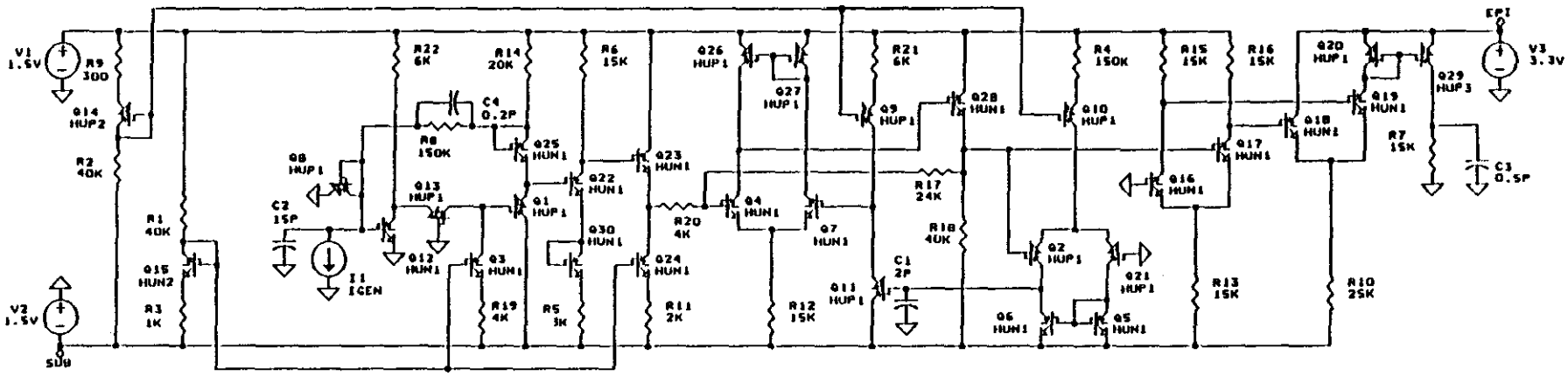
Los Alamos National Laboratory
Title
Si-Tracker Multi-Chip Module
Size Document Number REV
C
Date

Si-Tracker Front-End Electronics Parameters

Total # of MCMs:	5052
# of Channels/MCM:	640
Total # of Channels:	3.2M
# of Bipolar Chips per MCM:	5
Total # of Bipolar Chips:	25260
# of CMOS-1 Chips/MCM:	5
Total # of CMOS-1 Chips:	25260
# of CMOS-2 Chips/MCM:	1
Total # of CMOS-2 Chips:	5052
# of Fiber Optic Link/MCM:	0.5
Total # of Optical Links:	2526
Power Consumption/Channel (Bipolar, CMOS-1, 2, FO):	less than 3mW

Baselines in Cost Estimates

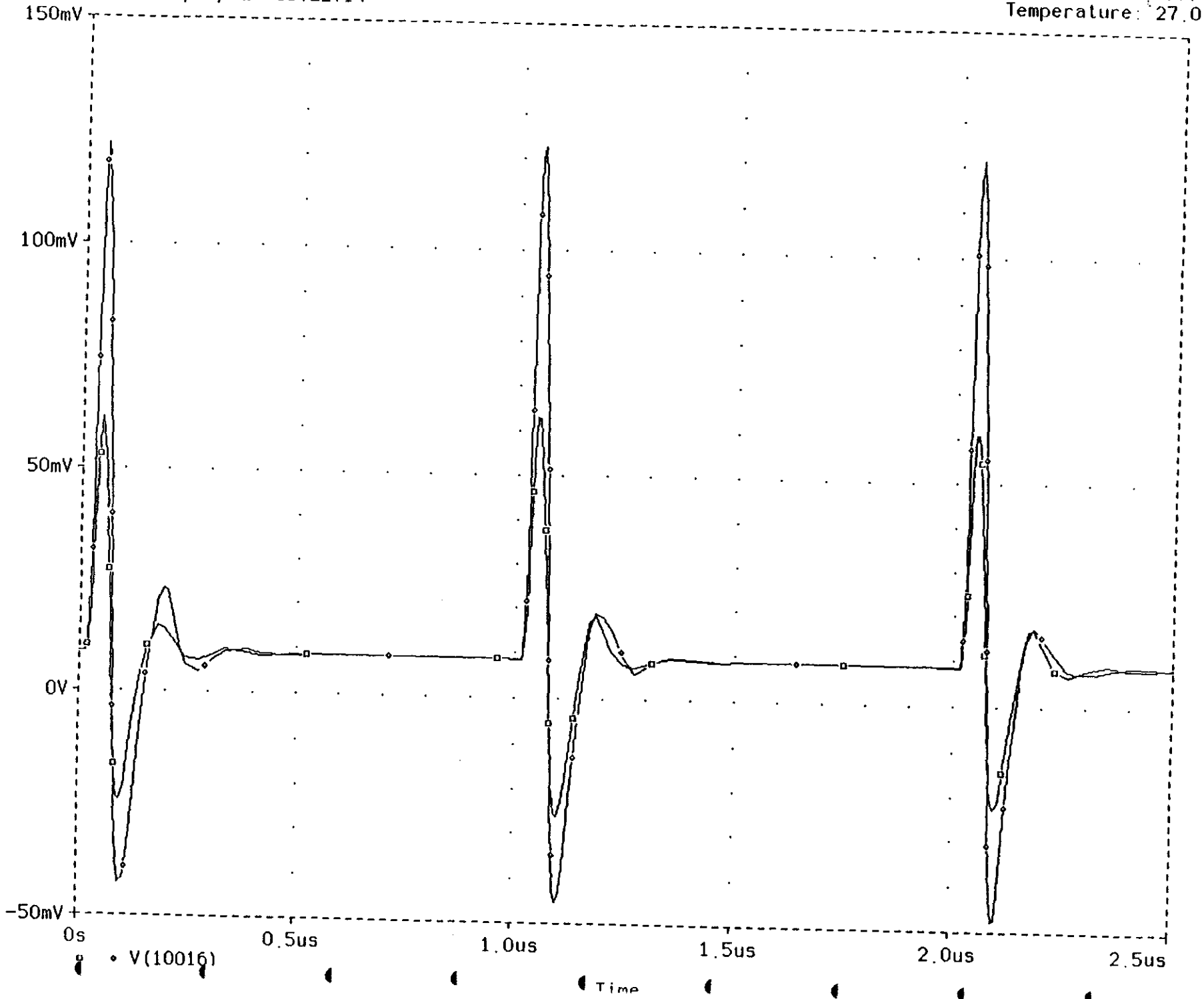
'91 $
5% spare quantity for all chip types, MCMs, cables
Cost of prototyping effort extra
Fabrication starts in the beginning of FY94


V1
1.6V
R9
300
Q14
HUP2
R2
40K
R1
40K
Q15
HUN2
R3
1K
V2
1.5V
SUB
Q8
HUP1
C2
15P
I1
IGEN
R22
6K
R8
150K
C4
0.2P
Q13
HUP1
Q12
HUN1
R14
20K
Q25
HUN1
Q1
HUP1
Q3
HUN1
R19
4K
R6
15K
Q22
HUN1
Q30
HUN1
R5
3K
Q23
HUN1
R20
4K
Q24
HUN1
R11
2K
Q26
HUP1
Q27
HUP1
Q4
HUN1
Q7
HUN1
R12
15K
R21
6K
Q9
HUP1
Q28
HUN1
R17
24K
R18
40K
Q11
HUP1
C1
2P
R4
150K
Q10
HUP1
Q2
HUP1
Q21
HUP1
Q6
HUN1
Q5
HUN1
R15
15K
Q16
HUN1
R13
15K
R16
15K
Q17
HUN1
Q20
HUP1
Q18
HUN1
Q19
HUN1
R10
25K
Q29
HUP3
R7
15K
C3
0.5P
EPI
V3
3.3V

AC7LA.CIR
Date/Time run: 04/16/92 15:22:14

Revised: APRIL 10, 1992, AC7LB.CIR

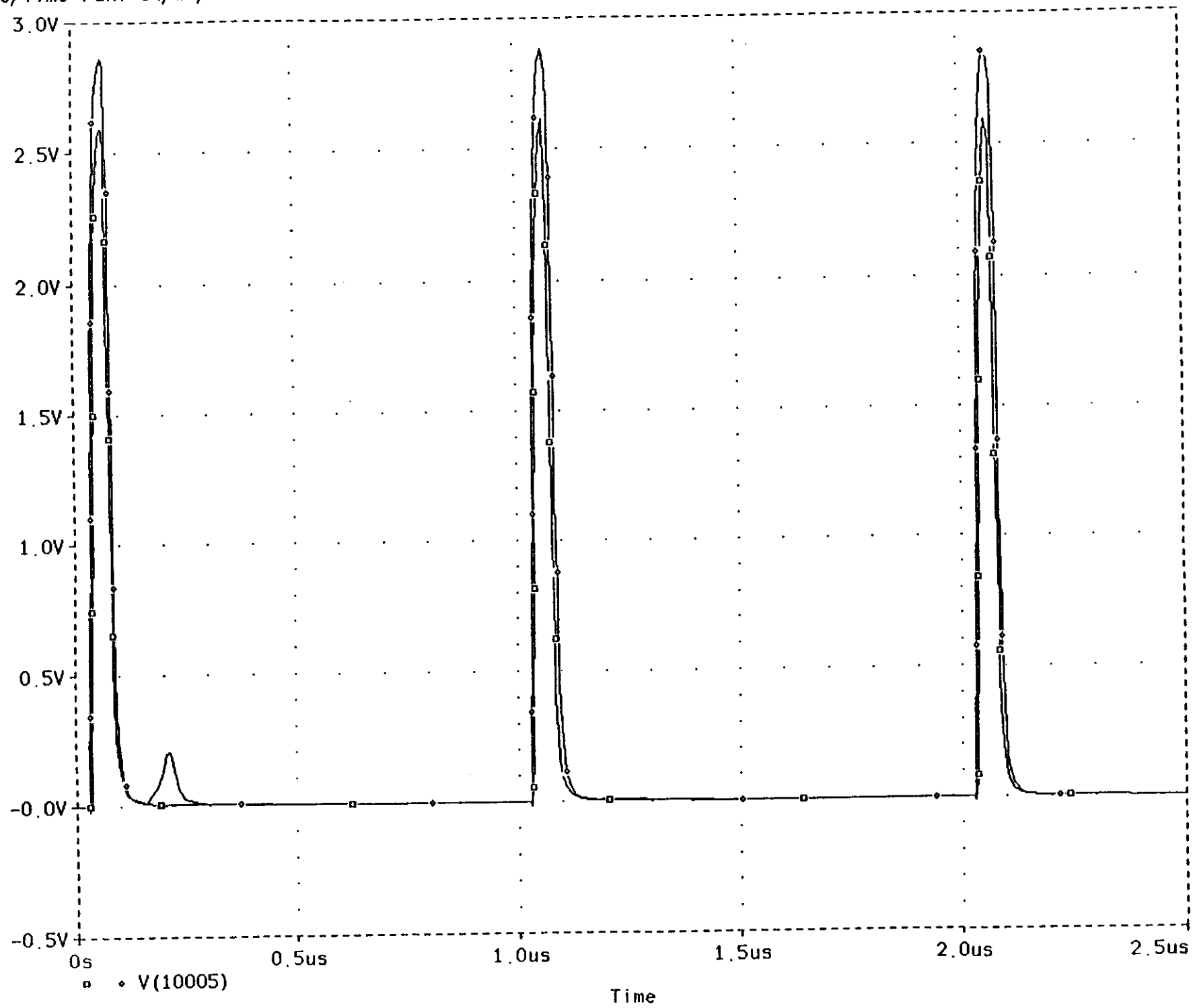
Temperature: 27.0



AC7LA.CIR
Date/Time run: 04/16/92 15:22:14

Revised: APRIL 10, 1992, AC7LB.CIR

Temperature: 27.0



Bipolar Chip

Available Foundries: Harris/AT&T/Tektronix/Motorola
Simulation Results w/ Harris UHF1 Process

- 1.3 mW/Ch
- 1800 electrons RMS noise
- 25ns risetime
- 150ns recovery
- 128 input/output per die

Cost Estimates

E&D (FTE) Staff / Tech	EDIA(M&S) ($Million)	Insp/Adm(FTE) Staff / Tech	Proc/Fab ($Million)	Assy/Inst	Cont'y (%)
1.25/1.5	0.41	0.25/1.0	1.221	0	32

Support Table

a. Wafer Procurement

Cost per Wafer (4"):	$3500
Die Size:	6.4mm x 6.2mm
Yield (incl. dice w/one bad ch.):	50%
# of Good Dice per Wafer:	76
Cost per Die (w/o funct test):	$46
Total Cost (incl. 5% spare)	$1.221M

b. EDIA (Wafer Level Functional Test and Qualification)

Cost per Die:	$15.5
Total Cost	$0.410M

c. Contingency (%)

Tech(12)+Cost (4)+Schedule(16) = 32

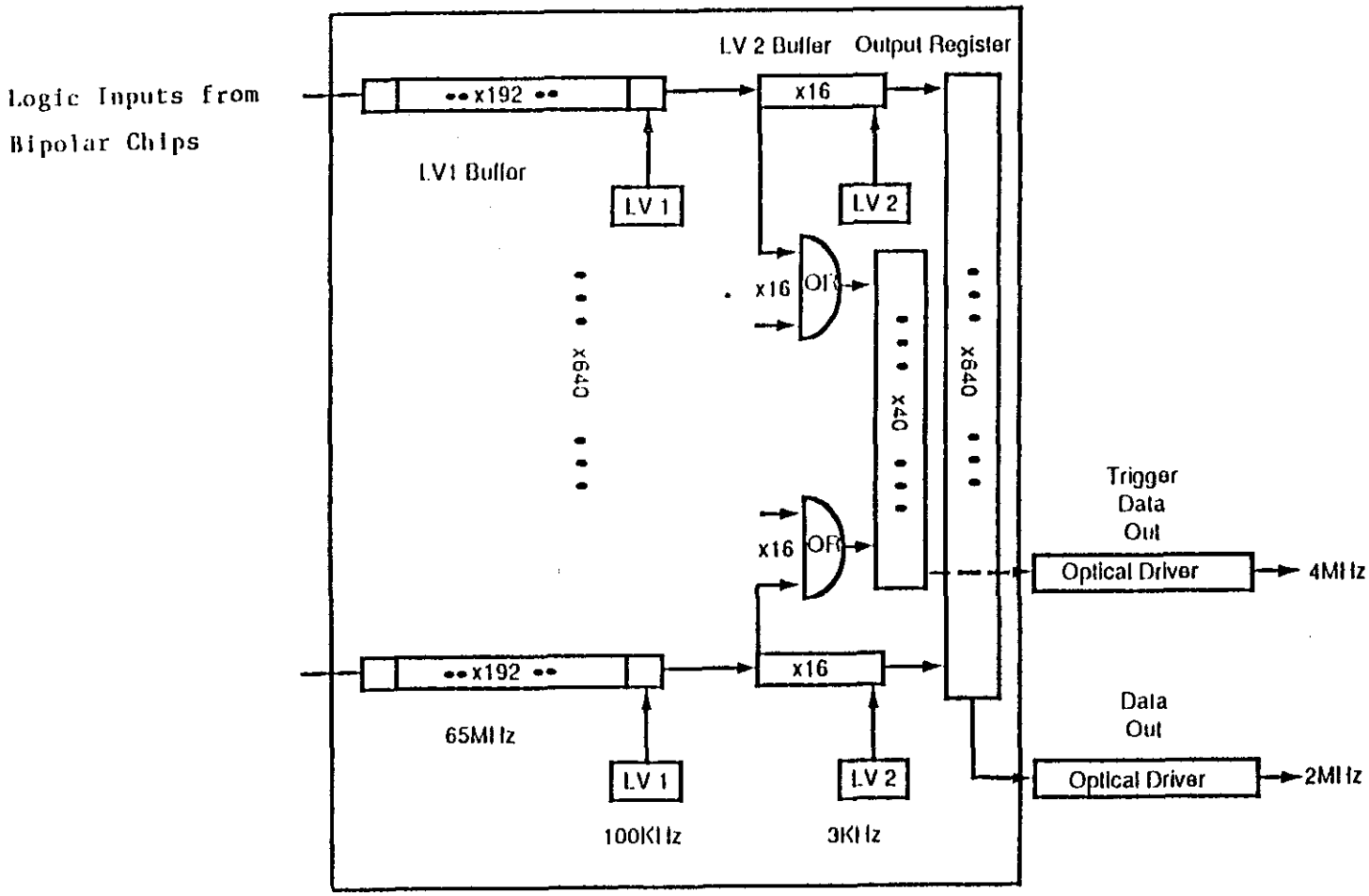


Figure 4. One of the CMOS-1 Architectures

CMOS-1 Chip

128 Inputs / 32 (?) Outputs
Level-1 Trigger Buffer with Data Compression
Currently Under Architectural Study

Cost Estimates

E&D (FTE) Staff / Tech	EDIA(M&S) ($Million)	Insp/Adm(FTE) Staff / Tech	Proc/Fab ($Million)	Ass'y /Inst	Cont'y (%)
1.5/2.0	0.41	0.20/1.0	1.160	0	42

Supprt Table

a. Wafer Fabrication

Cost per Wafer (6"):	$2800
Die Size:	6.4mm x 12mm
Yield:	35%
# of Good Dice/Wafer:	64
Cost per Die :	$44
Total Cost:	$1.160M

b. EDIA (Wafer Level Functional Test and Qualification)

Cost per Die:	$15.5
Total Cost	$0.410M

c. Contingency (%)

Tech(20)+Cost (6)+Schedule(16) = 42

CMOS-2 Chip

32 (?) Logic Inputs + Analog Monitor Lines/ 32 (?) Outputs
Interface between CMOS-1 and Fiber Optics
State-of-Health Monitor
No Detailed Study of This Chip Yet

Cost Estimates

E&D (FTE) Staff / Tech	EDIA(M&S) ($Million)	Insp/Adm(FTE) Staff / Tech	Proc/Fab ($Million)	Ass'y/Inst	Cont'y (%)
1.0/0.5	0.165	0.20/0.5	.212	0	42

Support Table

a. Wafer Fabrication

Cost per Wafer (6"):	$3500
Die Size:	6.4mm x 10mm
Yield:	40%
# of Good Dice/Wafer:	88
Cost per Die:	$40
Total Cost :	$0.212M

b. EDIA (Wafer Level Functional Test and Qualification)

Cost per Die:	$31
Total Cost	$0.165M

c. Contigency (%)

Tech(20)+Cost (6)+Schedule(16) = 42

Multi-Chip Module

Carrier of 11 Custom Chips costing $1000
Reworkability is a must
Flip-chip or Cavity with top layer interconnection
Bump preparation cost included

E&D (FTE) Staff / Tech	EDIA(M&S) ($Million)	Insp/Adm(FTE) Staff / Tech	Proc/Fab ($Million)	Ass'y/Inst	Cont'y (%)
0.5/0.25	0.085	0.5/1.0	0.874	0	36

Support Table

a. MCM Procurement

Cost per cm^2:	$12
MCM Area:	12
Cost per MCM:	$144
Bump Prep:	$0.11M ($100 /wafer x 1100)
Total Cost:	$0.874M

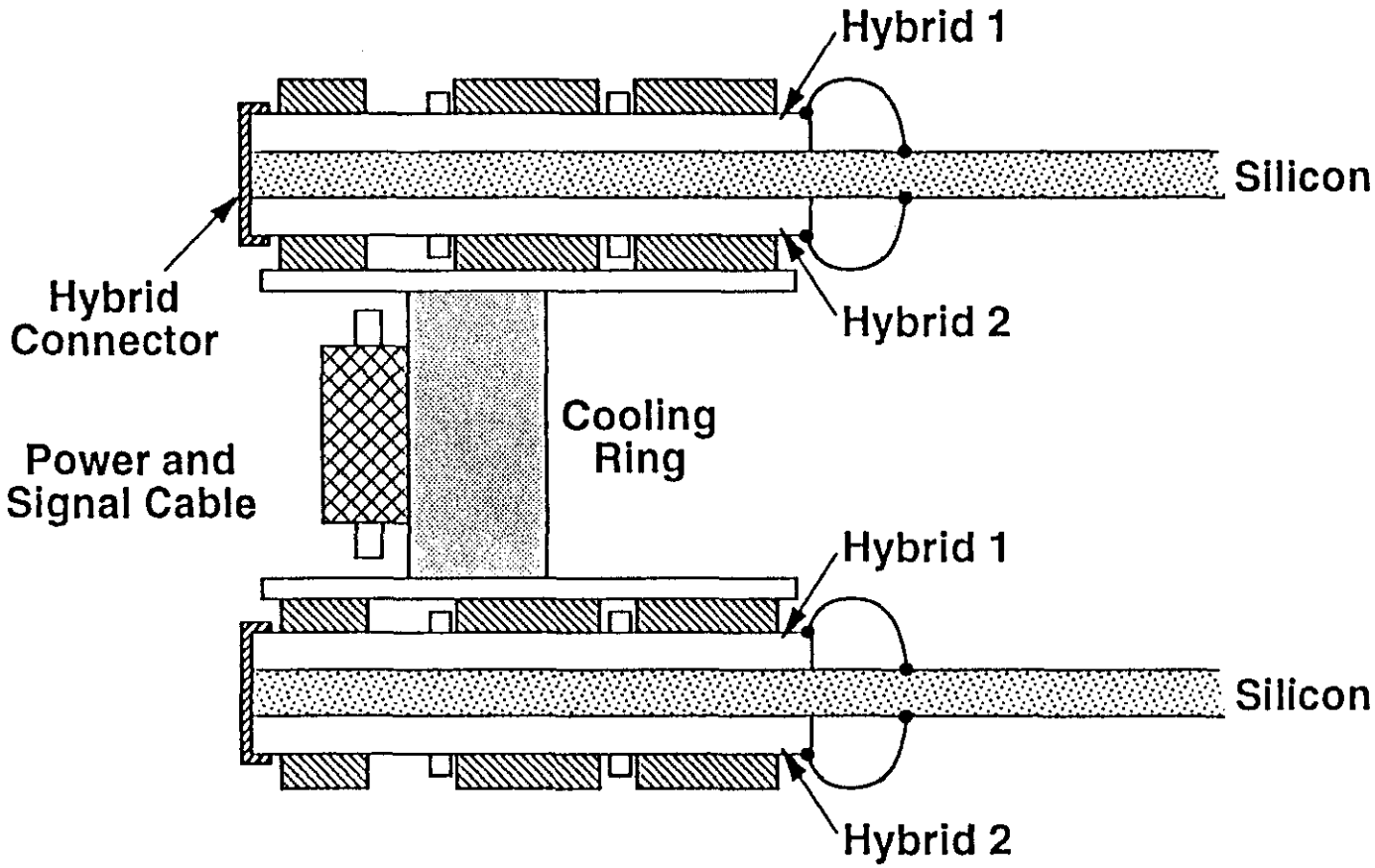
b. EDIA (Functional Test and Qualification)

Cost per MCM:	$16
Total Cost	$0.085M

c. Contigency (%)

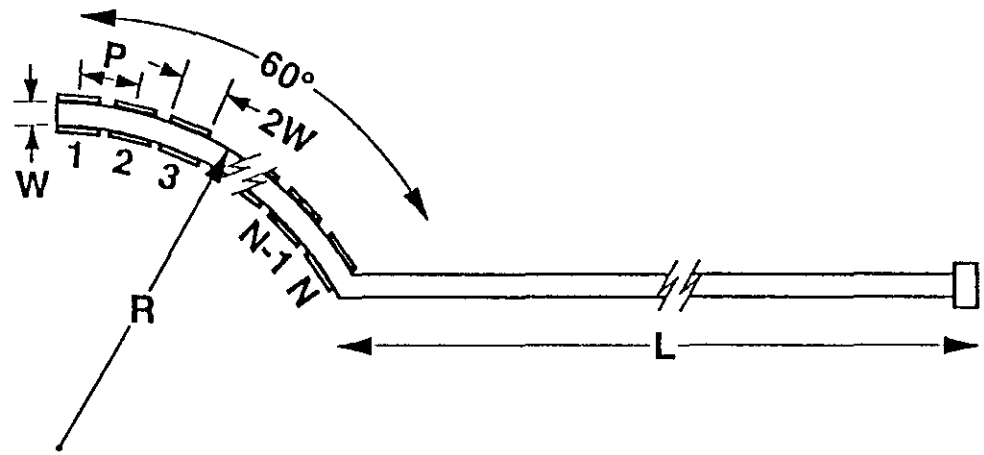
Tech(8)+Cost (12)+Schedule(16) = 36

Double-Sided Silicon Strip Detector with Electronic Assembly

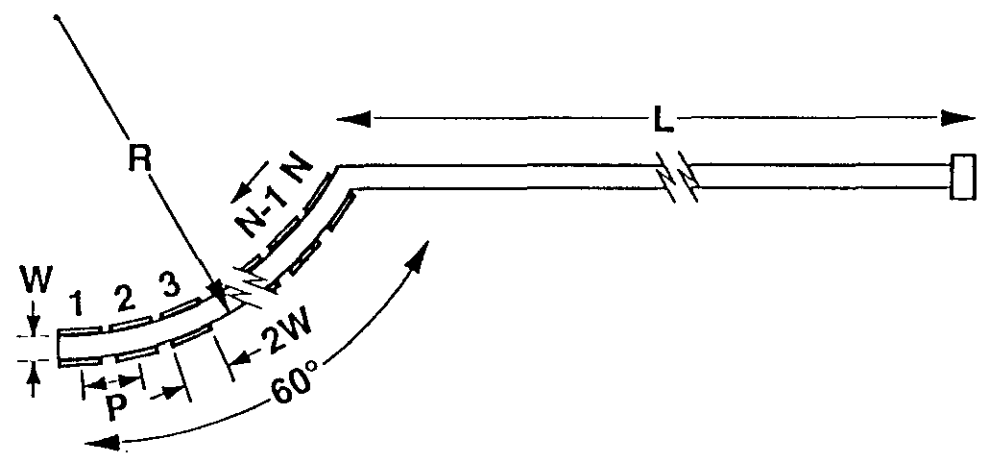


Cable Assembly

Type A

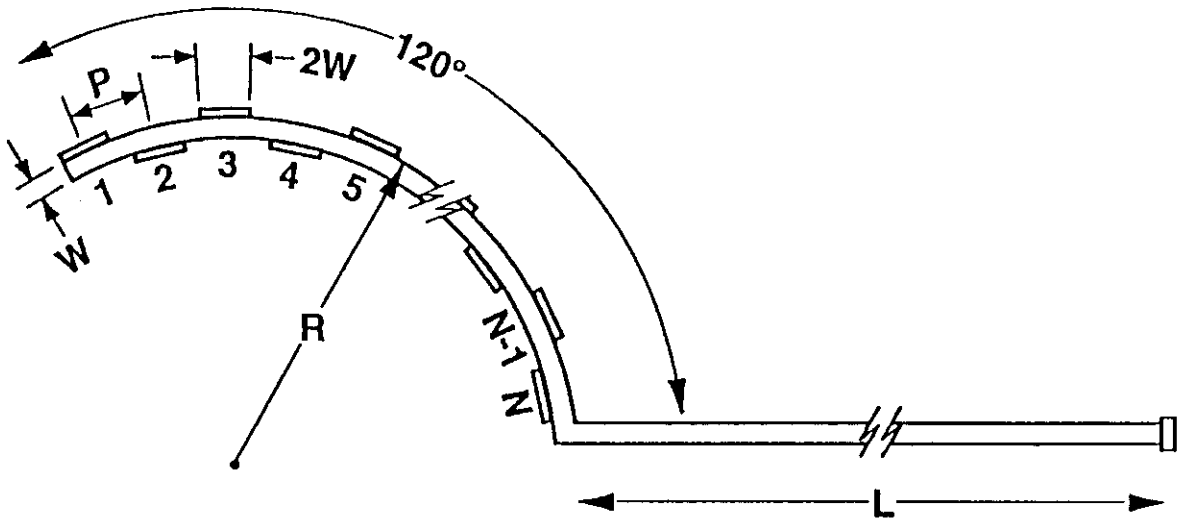


Type B

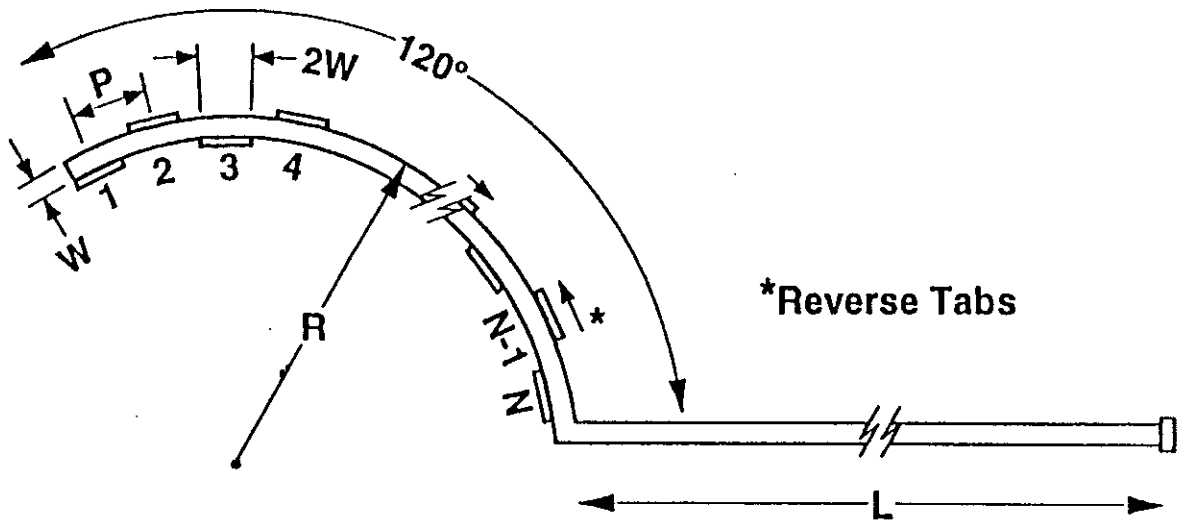


Cable Assembly

Type C (even N)



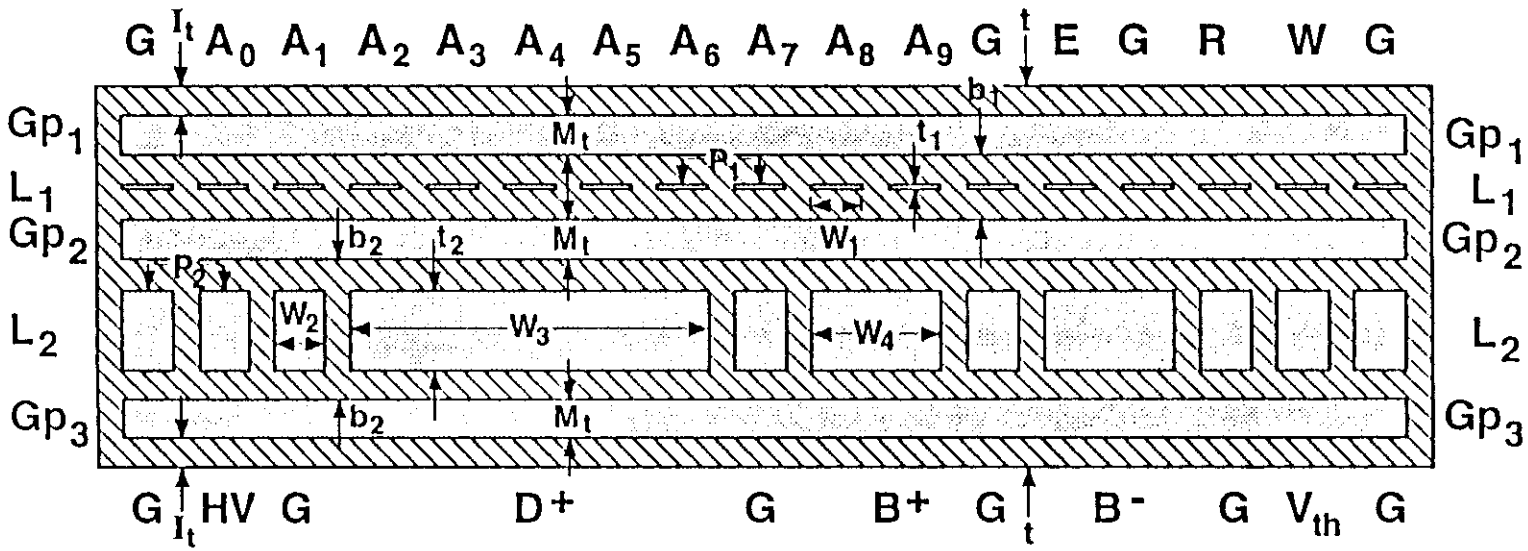
Type D (odd N)



*Reverse Tabs

Power/Signal Cabling

Cross Section



G = Ground
A_0-A_9 = Address/Data Bus
E = Enable
R,W = Read, Write Enable

Gp = Ground Plane
HV = High Voltage
D+ = Digital Voltage
B+,B- = Analog Supply
V_{th} = Analog Threshold

Cables (inside the Si-tracker)

4 Basic Types
16 Different kinds
More than 2 meters long (too long for conventional fab)
Aluminum conductors preferred (fab/maint. problems)

Cost Estimates

E&D (FTE) Staff / Tech	EDIA(M&S) ($Million)	Insp/Adm(FTE) Staff / Tech	Proc/Fab ($Million)	Ass'y/Inst	Cont'y (%)
0.5/0.2	0.05 (?)	0.20	0.386(?)	0	54

Support Table

a. Cable Fabrication (including functional tests)

192 cables x $2000 (?)/cable: $0.386M (?)

b. Contigency (%)

Tech(30)+Cost (16)+Schedule(8) = 54

Summary

	E&D (FTE) Staff / Tech	EDIA(M&S) ($Million)	Insp/Adm(FTE) Staff / Tech	Proc/Fab ($Million)
Bipolar	1.25/1.5	0.41	0.25/1.0	1.221
CMOS-1	1.5/2.0	0.41	0.20/1.0	1.16
CMOS-2	1.0/0.5	0.165	0.20/0.5	0.212
MCM	0.5/0.25	0.085	0.5/1.0	0.874
Cable	0.5/0.2	0.05 (?)	0.20	0.386 (?)
Total	**4.75/4.45**	**1.120**	**1.35/3.5**	**3.853**
$M	.713/.445	1.120	.203/.350	3.853
				$6.684M