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Electronics Cost Estimate

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June 13, 1992

Abstract:

This note was prepared by the authors with the advice and support of the engineering staff of LeCroy Corporation. It represents the first stage of a process that we expect will culminate in bottom up estimates based on detailed designs.

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1. Introduction

This note was prepared by the authors with the advice and support of the engineering staff of LeCroy Corporation. It represents the first stage of a process that we expect will culminate in bottom up estimates based on detailed designs.

All parts of this detector must operate at the SSC beam crossing rate of 60 MHz. The 1st level trigger must be deadtimeless (fully pipelined). The design goal for the Level 1 trigger output rate is 10 KHz. If necessary, an intermediate "Level 1.5" trigger stage will be added to accomplish this. To provide an operating margin, all detectors must be designed to accept Level 1 triggers at an average rate of 100 KHz. The muon system, the calorimeter, and at least part of the central tracker must digitize at this rate, to provide the data required by the Level 2 trigger. A pipelined delay of up to 3 microseconds is required in every signal channel to accommodate the Level 1 trigger delay, and an asynchronous buffer must be provided for the Level 2 delay, where required. All systems which participate in the 1st level trigger decision must identify the beam crossing uniquely. Initially, only the calorimeter and the muon systems will be used in the Level 1 trigger. This beam crossing information determines which of the pipelined signals are digitized and stored.

The 2nd level trigger will be designed to achieve an output rate of 300 Hz or less. To allow for design margin, the readout into Level 3 must be designed to accept events at a rate of 3 kHz. For each accepted 2nd level trigger, any remaining detectors are read out and the entire event is submitted to the Level 3 trigger, which will be a processor farm.

All systems will have test and calibration facilities included as part of the system design. These will allow quick verification of function in all cases and provide a complete calibration for some. This detector must operate reliably for many years. The approach to the electronics design reflects our concern for serviceability of the components. The calorimeter and muon electronics are located where access is possible. Only the minimum electronics is located in the detector, where access time is measured in weeks, not hours or minutes. Those components which must be inaccessible, the calorimeter preamps, and the central tracker, must be designed and tested for reliability. Redundant components and communication paths must be designed in at the system level, to permit slow degradation of performance rather than catastrophic failure.

This estimate is for contruction costs and therefore assumes that a conceptual design has been completed and that outstanding R&D issues

have been resolved. This estimate does, however, include the cost of implementing a prototype version of each subsystem to be implemented.

The prototype systems are assumed to compromise a number of channels that is the smaller of 10% of the final subsystem channel count or 1000 channels. Most of the engineering costs are incurred in this phase of the work. The reliability of these estimates will depend on the extent to which the relevant technologies are understood. Systems that require extensive R&D have been assigned higher technical-risk factors in the contingency analysis.

For each system, a straw-man design has been chosen, which is based on available technology, or modest extrapolations thereof, to the extent possible. The final design may be different from that described here. These estimates are best described as top-down, using analogies with existing systems, rather than a full bottom-up approach. The rate of change in electronics technology is rapid enough that a bottom-up estimate based on current technology is inappropriate at this stage of the detector design.

2. Generic development cost used in the cost estimates

These generic items are taken from the EMPACT/TEXAS cost estimate, with some additions and modifications. They have been reviewed here at LeCroy and are still considered to be a reliable guide to development and production costs. The original caveats also still apply, these costs are a guide only in the case of well understood systems, not necessarily correct for systems which are beyond the current state of the art.

The following estimates are based on a labor rate of $74. per hour ($161K per year). This is comparable to the fully burdened rate for an engineer or physicist at one of the national laboratories. Actual rates for particular institutions have been used where known.

The cost of radiation hard ICs is estimated at twice normal ICs, both for development and production costs. This is supported by discussions with current vendors of radiation hard semiconductors. Note that It may be more difficult to achieve the required performance with radiation hard ICs.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/each
Simple IC	0.50	161	80.5	30	150	260.5	12
Simple IC, rad hard	1.00	161	161.0	60	300	521.0	24
Complex IC, digital	1.25	161	201.3	40	150	391.3	16
Complex IC, digital, rad hard	2.50	161	402.5	80	300	782.5	32
Complex IC, analog	2.00	161	322.0	40	150	512.0	50
Complex IC, analog, rad hard	4.00	161	644.0	80	300	1024.0	100

For the complex analog chips, a special test station is required for production testing. This will be more thorough than normal semiconductor vendor testing. This will test all storage locations in a switched capacitor array, for example.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/each
Analog tester	1.00	161	161.0	50	50	261.0	16

The pc board production costs include all common parts, but not the special custom integrated circuits. This cost also includes assembly, test and calibration. We note that a standard FASTBUS board has a usable area of approximately 14**2 in**2, yielding a production cost of slightly less than $ 1600. Although GEM has not adopted FASTBUS as a standard, this estimate assumes that most rack-mounted electronics is implemented on boards of this approximate size.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/sq in
Simple PC board	0.55	161	88.6	4	16	108.6	8
Complex PC board	1.50	161	241.5	10	20	271.5	8

For the very high density systems in the central detector region, the component density required is similar to that currently found in systems using hybrid or chip-on-board construction techniques. The development effort for this type of construction is similar to a large complex pc board. The estimate of the generic cost is based on LeCroy's experience with a large hybrid TDC for a chamber mounted application. This estimate is an extrapolation to a highly automated production system. Note that the cost of working silicon is in the neighborhood of $500 per sq.in.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/sq in
Large hybrid chip	1.50	161	241.5	10	20	271.5	100

An alternative method of achieving the very high density required is to design monolithic ICs which incorporate all needed functions on the chip. Very few other components can then be used to achieve the high channel density required. The number of chips required depends on the number of different technologies, probably at least 2, since the preamplifier is expected to use bipolar technology. The analog storage and digital chips can be rad hard CMOS. The expected reliability of an all monolithic system, (with very few connections) is much higher than with hybrid techniques. With this packaging technique, the ICs are more complex, and their development and production costs must reflect this.

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/sq in
High density surface mount PC board	1.50	161	241.5	10	20	271.5	30

3. Support systems in the experimental hall and other common items

a) High voltage for central trackers and muon chambers

The high voltage systems are very similar for several detector systems. We have assumed the use of commercial systems at a cost of $150 per channel, and $50 per channel for cable and connector costs. Since these are commercial systems, we assign little or no development costs.

b) Low voltage power for detector mounted electronics

The low voltage power supplies will be located in the hall, close to the magnet, but in an area where the field is less than 0.1 Tesla. Th transformers and other magnetic components must be shielded from the field, or designed to operate in a 0.1 Tesla field. The cost has been estimated at $4 per watt for the remote operation and monitoring) and $1 per watt for the cable distribution system. These estimates are based on actual costs of existing systems. Only a modest development cost has been assigned, since we expect these systems to be based on commercial offerings.

c) Optical fiber data links

We have used a generic optical data link for the purposes of this estimate. The cost is based on a currently available 80 Meter long link, rated at 125 MHz. We expect that higher performance at a similar price will be available in the SSC/GEM time frame. The production cost is $250 per link. This includes an optical transmitter ($88/each), optical receiver ($88/each), two ST connectors ($12), and 80 meters of multimode graded index fiber ($0.25/ft). The total cost per link becomes $ 370. when the cost of the receiver/buffer board and its associated slot charge ($ 90. and $ 30./channel, respectively) are added.

d) Optical fiber receiver and data buffer board

Similarly, the 32 channel receiver buffer board for the optical links is the same for all of the data (non trigger) links. The development cost is charged only once, and is $271.5k, the cost of developing a complex printed circuit board.

This receiver and buffer is the core of the data acquisition system. All subdetector systems send the data via an optical link to these boards. Most systems send the data after a Level 1 accept. The system is easily modified to accomodate those subdetectors which retain the data until the Level 2 trigger decision. The buffer structure is

designed to store all data until transfer to Level 3, which occurs upon receipt of a Level 2 accept.

Each link receiver stores the data received in a FIFO buffer, a separate buffer for each link. The link protocol includes an end of event marker to separate multiple events. The data remains in the FIFO until the Level 2 trigger decision. Any data required by the Level 2 trigger is either copied to an output optical link as it is received, or a duplicate link is provided at the source. The event size at this FIFO is less than 1k bytes, so a 32k buffer will allow a Level 2 trigger delay of 300 microseconds.

At this time the data is either discarded, or transferred to a Level 3 FIFO buffer on the same board. The Level 2 acceptance rate is 3 kHz, or every 333 microseconds. There is only 1 Level 3 FIFO buffer per board. A local event building operation takes place, collecting all data for the accepted event from all Level 2 FIFOs. At the same time, a copy of the complete event is also sent to the Level 3 trigger system via a 32 bit parallel link. Note that the Level 3 trigger is working with a copy and does not need to save the data, nor does it need to use all the data. The maximum event size is 32k at this buffer level. A 1 Mb buffer will allow a 0.01 sec Level 3 trigger delay.

The Level 3 trigger decision causes this event to be either discarded, or read out via the backplane (FASTBUS for example) into a host computer, or directly to long term storage. A FASTBUS system would have more than adequate bandwidth for this task. A full FASTBUS crate will have a maximum event size of 600 kb.

e) Crates with Power

The slot cost for rack mounted boards is based on the typical cost of a powered FASTBUS crate, about $600. per slot. Note that this does not imply the use of FASTBUS, but does produce a more reliable estimate.

For the racks mounted near or on the magnet, this is increased by $300 to include the extra costs associated with liquid cooling and remote or magnetic field tolerant power supplies. The development costs associated with this are common to all crates of this type. This common development cost is charged only once.

f). Signal Cables

Note that cabling in the hall or in the detector is expected to conform to CERN rules for underground areas, i.e. it must be halogen free. The signal cable cost estimates are based on $0.3 / meter, the cost of shielded twisted pair cable.

4. Resistive plate chambers

The resistive plate chamber produces a spark promptly after the particle passage. The combination of the gas and the resistive plate promptly quenches the spark. A large positive charge is left in the gap, producing a large prompt induced signal on a pickup strip electrode. The strip can be designed as a terminated transmission line, requiring only a simple discriminator at the end of the strip to produce a signal with beam crossing timing. There is no drift time to consider. This is modified by the flight time from the vertex, but this can be mitigated by restricting the strip length or by applying suitable realtime corrections. The result is a prompt signal that can uniquely identify the beam crossing.

This system satisfies two requirements. It provides a signal for the trigger without waiting for (or correcting for) the drift time. And it provides the z coordinate, as a higher resolution alternate to the time difference from the two ends of a drift wire. A TDC system, similar to the muon barrel system records the time for more precise off line analysis.

The RPC's are arranged in three layers, corresponding to the three superlayers of the barrel muon system. "Azimuthal" strips running parallel to the beam are used for triggering, and strips running perpendicular to the beam are used for z-determination. The non-bend-plane (i.e. z) strips are also placed in coincidence with the bendplane trigger strips to provide added immunity to accidental triggers.

The strips are grouped into 16 azimuthal sectors and segmented into two lengths along the z direction. The sectors of the first, second, and third superlayers, are subdivided into 111, 187, and 240, azimuthal strips, respectively. To reduce transit-time variations to an acceptable the bend-plane strips are read from both ends. Each pair of outputs from a strip is routed to a discriminator/chronotron card that shapes the pulses and provides a single output pulse whose leading-edge time is independent of the position of incidence.

There are 322 z-strips for each layer of each sector.

The total number of strips is thus

$$N = 16 \times 2 \times (111 + 187 + 240) = 17{,}216 \text{ bend-plane}$$

$$N = 16 \times 2 \times (3 \times 166) = 15{,}936 \text{ non-bend-plane (z)}$$

$$= 33{,}152 \text{ total}$$

Each strip provides an input to the Level 1 trigger and to a TDC for offline performance monitoring and analysis. Since the TDC system used for the muon drift detectors (see section 5) can be used for the RPC strips, no prototype/development costs have been included. The cost of the Level 1 trigger processing logic for the RPC's is detailed in section 11.

Resistive Plate Chamber, 33k trigger signals

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab $/chan	Material $k total
Bend-plane discriminator/chronotron boards (two input signals per strip): 17.2K strips								
Cable to far-end discriminator 15 m						20.0	4.80	82.6
Discriminator IC, 4 strip/chip (no engineering, same as drift-wire)							3.00	51.6
Chronotron semi-custom IC for Time-Deskewing (8 str/chip)	0.25	161	40.3	5	50	95.2	12.50	215.2
Discriminator PC board, 2ch/sq.in	0.55	90	49.5	4	16	69.5	4.00	69.0
Cable to trigger system, 15 meters						20.0	4.50	77.5
Non-bend-plane discriminator boards: 15.9K strips								
Discriminator IC, 8 strip/chip (no engineering, same as drift-wire)							1.50	23.9
Discriminator PC board, 4ch/sq.in	0.55	90	49.5	4	16	69.5	2.00	31.8
Cable to trigger system, 15 meters						20.0	4.50	71.6
TDC boards (same for all 33.2K strips)								
TDC chip 8 channels (same as drift-wire system)							2.00	66.4

TDC PC board, 96 TDC/board, 2.0 sq. inch/channel (same as drift-wire system)	16.00	531.2
Crate slot cost, special rack, remote power, $900/board	7.03	233.5
Readout and comm. links, one/sector, @ $ 370./ea (One/sector + One/2500 TDC Channels = 32 + 34 = 66 links)	.74	24.2
LVPS 100mw/channel, 3.3 kW total @ $5/watt	.50	16.5
HVPS & Cables 256 chan. @ $ 200/ea	1.54	51.0
Total	<46.5>	1546

5. Muon Barrel System

The barrel section will use long drift wires, in either limited streamer or proportional mode. The candidates are limited streamer wires at atmospheric pressure, with an open rectangular cell geometry, and proportional mode wires in pressurized circular drift tubes. In both cases the drift time is the quantity to be measured. The time digitizing resolution (least significant bit, LSB) must be 1 nsec or less. By connecting adjacent (but not overlapping) wires together at the far end, and using one TDC per wire (i.e. two per connected pair) we can use the time difference to determine the Z position with better than 15 cm resolution. The time sum will determine when the avalanche occurred, automatically correcting for the propagation time along the wire.

Task list:

1) preamplifier/ discriminator mounted on the chamber. For the limited streamer mode chambers, the discriminator is mounted directly on the chamber, driving differential wires to the TDC cards. For the proportional mode wire case, It may be necessary to separate the preamplifier and discriminator, at least to the extent of separate cards, though possibly also chamber mounted. This may require a custom integrated circuit design.

2) cables to TDC racks mounted on the magnet pole face. This is a short cable run, less than 15 meters worst case.

3) pipeline tdcs. Currently available commercial TDCs use entirely digital techniques to achieve 1 nanosecond resolution (least count). This is a custom monolithic CMOS chip, which contains the timing and readout logic for 8 channels of multi-hit pipelined TDC. The full scale

range is 65,000 counts, with 1 nsec least count. Up to 16 hits per channel are stored, with double hit resolution of 20 nsec. Although the readout properties of the existing chip are not perfectly matched to our requirements, no significant technological extrapolations are required to develop something suitable.

A new chip, with features and performance optimized for the GEM muon system, will be required. The expected improvements in IC processing in the SSC time frame will certainly allow cost, performance and power dissipation to be enhanced compared to the current circuit. This new chip will be designed as a pipeline TDC, with continuous time stamping readout. The pipeline nature of the circuit naturally provides storage of the timing data during the first level trigger delay.

4) crate by crate readout to the upper counting room. This cable run is at least 50 meters.

5) receiver/buffers for 100 optical fibers. Each channel requires a few thousand bytes of fast buffer.

6) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

Muon Barrel System, LSDT Option 110K channels

	Engineering/design			EDIA		Prototype	Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total		Material
Item	my	k$/my	k$	k$	k$	k$	$/chan	$k total
Discriminator IC, 8 wires/chip	0.50	161	80.5	30	150	260.5	1.50	165
Cable to TDC rack, 15M shielded twisted pair					20.0	4.50	495	
Discriminator PC board	0.55	161	88.6	4	16	108.6	2.00	220
TDC chip 8 channels	1.25	161	201.3	40	150	391.3	2.00	220
TDC PC board, 96 TDC/board, 2.0 sq. inch/channel	1.50	161	241.5	10	20	271.5	16.00	1760
Crate slot cost, special rack, remote power, $900/board							7.20	792

Readout & comm. links, one/2500 signals,80m 44@ $ 370/ea								.19	21
LVPS, 100mw/channel, 11 kW total @ $5/watt								.50	55
HVPS & Cables 1000 channels @ $ 200./ea								1.81	200
LSDT Total			1052		35.70	3927			

Muon Barrel System, PDT Option 90K channels

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab $/chan	Material $k total
Preamp, 8 wires/chip (proportional mode only)	0.50	161	80.5	30	150	260.5	1.50	135
Discriminator IC, 8 wires/chip	0.50	161	80.5	30	150	260.5	1.50	135
Cable to TDC rack, 15M shielded twisted pair						20.0	4.50	405
Discriminator PC board	0.55	161	88.6	4	16	108.6	2.00	180
TDC chip 8 channels	1.25	161	201.3	40	150	391.3	2.00	180
TDC PC board, 96 TDC/board, 1.5 sq. inch/channel	1.50	161	241.5	10	20	271.5	16.00	1440
Crate slot cost, spec. rack, remote pwr, $900/board								7.20	648
Readout & comm. links, one/2500 signals: 36@ $ 370/ea								.15	13
LVPS, 200mw/channel, 18 kW total @ $ 5/W								1.00	90
HVPS & Cable 1000 channels @ $ 200./ch								2.22	200
PDT Total							1312.4	38.07	3426

6. Muon Endcap

This system consists of closely spaced (2.5 mm) anode wires, as in a standard proportional chamber, but with cathode-strip readout. Four layers are needed to achieve the required spatial resolution. This system is similar to the outer central tracker, but the expected rates are much lower, less than 200 Hz per square centimeter. Thus the pickup strips are bigger, resulting in larger capacitance and correspondingly longer shaping times (about 1 microsecond) for similar noise levels. The induced charge signal must be measured with 1% relative accuracy (channel to channel) to achieve the required resolution. The expected rates are quite low, so some sharing of ADC channels to reduce cost is possible.

A calibration system must be included to ensure the 1% relative accuracy for adjacent channels.

This system will be used in the Level 1 trigger, so that beam crossing resolution is required. It remains to be established whether or not simply using the first hit from the 4 planes of a superlayer will suffice to uniquely determine the beam crossing. If this is not the case, either RPC's or scintillators will be required.

There are three approaches to the readout being considered.

1) Using a variant of the Amplex chip designed at CERN. Either a switched capacitor array or stretcher (a sample hold, with a a self timed clear) is required for the 3 usec trigger delay. if a stretcher is used, a separate digital pipeline is required to record the beam crossing information.

2) Using a switched capacitor array directly as in the outer central tracker. The same system can be used. A prompt trigger output is required, however.

3) Use a time over threshold pulse and pipelined TDC. The analog information is encoded as a pulse width, with both edges recorded in the pipeline TDC.

All three approaches appear viable and the final selection will be based on ease of implementation (cost). For specificity we consider option 1 in what follows.

In principle, the integration time of the front end electronics could be used to provide the Level 1 delay---the slow pulse from the preamp output could be held on a storage capacitor upon receipt of a Level 1 trigger. This approach, however, couples the Level 1 latency

time (2 mu-sec in GEM) to the integration time of the preamplifiers, which could lead to undesirable system constraints. Moreover, the long integration times would not permit reliable tagging of the bunch crossing, even in the offline analysis. Both of these problems will be addressed by incorporating digital pipelined logic based on the outputs of discriminators driven by fast-timing pickoffs from the preamplifiers. This logic will operate at the 60 MHz bunch crossing rate and will be used to generate local hold signals that cause the long-shaping-time outputs of the preamplifiers to be retained until the Level 1 trigger decision is available. At that point the analog storage elements can be further held if Level 1 is ``TRUE" or cleared if Level 1 is ``FALSE". The digital information will also be stored on a bunch-by-bunch basis for use offline.

Since strip occupancies are low, it is sufficient to combine sixteen of the digital channels into a single chain by ORing the discriminator outputs. Moreover, a single ADC can be used to readout several (here we assume 32) storage capacitors. The pipelined digital data determines which channel provided the analog signal.

Task list:

1) preamplifiers. These are low noise preamplifiers, designed for high input capacitance. The signal to noise ratio, after shaping, must be greater than 100:1. Again, differential outputs are preferred. Test and calibration pulses must be inserted at the preamplifier input, or in the chamber itself. This requires a custom integrated circuit design.

2) cables to racks mounted on the magnet pole face. This is a short run of shielded twisted pairs, the worst case is 15 meters. If all electronics is located on the chamber, these cables are not necessary.

3) shapers, discriminator and sample/hold for each channel

4) digital pipeline with error flags for each channel

5) analog multiplexing and adc system

These 3 items are combined on one large circuit board, with 256 input channels, and 32 ADC channels. Trigger outputs, if required, will be generated by this board. This channel density requires a substantial increase in connector density over the current practice. This requires a custom integrated circuit design.

6) crate by crate readout to the upper counting room. This cable run is at least 50 meters.

7) receiver/buffers for 250 optical fibers. Each channel requires a few thousand bytes of fast buffer.

8) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

Muon endcap system 252k channels mounting nearly all electronics on the chamber using shaping and sample-holds (local dead time) the technical risk is moderate.

Muon Endcap System, 242k CSC pads

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab $/chan	Material $k total
Preamp shaper, S&H, 16 PADs/chip	2.00	161	322.0	40	150	512.0	3.00	726
Preamp chip test station	1.00	161	161.0	50	50	261.0	1.00	242
ADC 32 PAD's/chip Commercial chip @ $ 100/ea							3.00	726
Discriminator IC, 16 PADs/chip	1.25	161	201.3	40	150	391.3	1.00	242
Digital logic & hit FIFO, 16 PADs/chip	1.25	161	201.3	40	150	391.3	1.00	242
FIFO chip PC board,normal density, 1 sq in / PAD	1.50	161	241.5	10	20	271.5	8.00	1936
Readout & Comm. Links, one/1000 signals @ $ 370/ea							.37	90
LVPS, 100mw/channel, 24 kW total @ $ 5/W							.50	121
HVPS & Cable 1000 channels @ $ 200/chan							.83	200
CSC Pad Total						1827.1	18.70	4525

Muon Endcap System, 29k CSC Anode wires
(same readout as barrel drift-wires)

Item	Engineering/design Labor my	Rate k$/my	Total k$	EDIA Material k$	Proc/Fab k$	Prototype Total k$	Proc/Fab Material $/chan	$k total
Preamp, 8 wires/chip (proportional mode only) (same as barrel drift-wire)							1.50	43.5
Discriminator IC, 8 wires/chip (same as barrel drift-wire)							1.50	43.5
Cable to TDC rack, 15M shielded twisted pair						20.0	4.50	130.0
Discriminator PC board	0.55	161	88.6	4	16	108.6	2.00	58.0
TDC chip 8 channels (same as barrel drift-wire)							2.00	58.0
TDC PC board, 96 TDC/board, 2.0 sq. inch/channel (same as barrel drift-wire)							12.00	348.0
Crate slot cost, spec. rack, remote pwr, $900/board							7.20	208.8
Readout & comm. links, one/2500 signals: 12@ $ 370/ea							.15	4.3
LVPS, 200mw/channel, 6 kW total @ $ 5/W							1.00	29.0
Total						128.6	31.85	923.7

(HVPS included as part of Cathode Pads)

7. Inner part of the central tracker

This will consist of silicon strips, with the electronics inside, and multiplexed output data on Optical fibers or cables. This is inside the detector, so power and space are at a premium. This part of the detector does participate in 1st level trigger, but will be read in time to provide information for the Level 2 trigger. Storage must be provided for all data during the 1st level trigger delay, and for all successful 1st level triggers during 2nd level trigger delay.

The result of the trigger decisions must be sent into the electronics to control the buffering and readout.

This portion of the detector is being designed at Los Alamos. The electronics design and packaging is an integral part of the detector, and will not be further discussed here.

The data will be multiplexed out on 3500 medium speed optical fibers. In this estimate we consider the costs of the drivers, the fiber, and the receiving electronics and data buffering. If rad hard electronics for the fiber system are not available, an intermediate stage will be provided, with copper cables bringing the signals from inside the detector to a location just outside the calorimeter.

Task list:

In the upper counting room the cable run is at least 80 meters.

1) receiver/buffers for 3500 optical fibers. Each channel requires a few thousand bytes of fast buffer.

2) communication of Level 1 & 2 trigger information, as required. This is straightforward, requiring only coordination with the inside electronics. The Level 1 is synchronous, and requires only the presence or absence of a yes signal at the proper time. Level 2 is asynchronous, and requires a specific yes or no answer for each event in the Level 1 buffer.

3) integrating this data into the final data stream to Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

8. Outer part of the central tracker

This will be an Interpolating Pad Chamber. All electronics are inside the detector, the data are multiplexed out for successful triggers. This system does not participate in the Level 1 trigger, but may provide selected data for the Level 2 trigger. The charge on each pad is measured with better than 1% accuracy to achieve the required spatial accuracy after interpolation. A switched capacitor array is required for analog storage during the Level 1 trigger delay and for buffering analog samples awaiting digitization after a Level 1 accept. A calibration system is required to maintain the 1% relative accuracy (for adjacent channels). The z coordinate will be determined by small-angle stereo pads.

Task list:

On the detector

1) preamplifiers on every channel. These are fast shaping and low noise. The input capacitance is modest (bipolar is appropriate). The signal levels are low (100 fC). These preamplifiers must be radhard. This requires a custom integrated circuit design.

2) switched capacitor storage array on every channel. The requirements are modest compared to the calorimeter usage of these devices, but they must be radhard. The ADC can be a simple 8 bit, 2 microsecond Wilkinson type, with one ADC per channel. As many as 3 samples may be required per event. This should be either integrating or peak detecting, not voltage sampling. This requires a custom integrated circuit design.

3) communication of Level 1 trigger information, as required. This is straightforward, requiring only coordination with the inside electronics. The Level 1 is synchronous, and requires only the presence or absence of a yes signal at the proper time. Levels 2 is asynchronous, and require a yes or no answer for each stored event.

4) multiplexing data into output fibers or cables. A multiplexing and sparsifying processor is required. This must be radhard. This requires a custom integrated circuit design.

In the upper counting room the cable run is at least 80 meters.

5) receivers and buffers for 1200 optical fibers. Each channel requires a few thousand bytes of fast buffer.

6) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

7) for the 100k anode wires to be instrumented: preamplifiers, discriminators, digital latch and pipeline, readout.

This is a completely monolithic system, with very few other components. All system functions, including calibration, testing and readout must be incorporated into the integrated circuits. Due to the very high level of integration, technical and cost risks are high.

Outer Central Tracker, 400k pad channels

Item	Engineering/design Labor my	Rate k$/my	Total k$	Material k$	EDIA Proc/Fab k$	Prototype Total k$	Proc/Fab $/chan	Material $k total
Preamp, 8 channel custom IC, 8 PADs/chip (rad hard)								
EE	.50	120	60					
Tech/Des	.50	70	35					
				60	300	455.0	3.00	1200
SCA 16 PADs/chip (rad hard), 8-bit ADC included								
EE	2.00	140	280					
Tech/Des	2.00	90	180					
				80	300	840.0	6.25	2500
Chip test station								
EE	.50	80	40					
Tech	.50	50	20					
				50	50	160.0	1.00	400
Readout/Controller Chip, 128 PADs/chip (rad hard)								
EE	1.25	80	100					
Tech/Des	1.25	50	62.5					
				80	300	542.5	.25	100
Dense SM PC board, 10 PAD/sq.in								
EE	1.00	80	80					
Tech/Des	2.00	50	100					
				10	20	210.0	3.00	1200
Readout & Comm Links, one/256 Pads @ $ 370./ea							1.45	578
LVPS 100mw/channel, 40 kW total @ $ 5/W							50	200
HVPS & Cable 256 channels @ $ 200/chan							.13	51
Total						2207.0	15.58	6229

9. Calorimeter

There are two possible calorimeter systems under consideration. In both cases the calorimeter size is such that a minimum ionizing particle (a muon) deposits about 1 GeV. The maximum expected signal is about 3

TeV, either Hadron jet or electromagnetic shower. In the electromagnetic part of the detector, a muon will deposit only 0.1 GeV, an electron or photon will deposit as much as 2 TeV in a single channel.

The baseline system is a liquid-Krypton/Argon EM calorimeter, backed up by a SPACAL hadronic section. The required electronic resolution in the EM section is 0.1 %, over a 16 bit dynamic range.

The alternate electromagnetic calorimeter will be Barium Fluoride crystals with photo-triode readout. The hadronic section will be scintillating fibers in matrix of heavy material. With this option, the pre-radiator is not used.

The calorimeter electronics will be outside the magnet, located on the membrane that supports the calorimeter. Only preamplifiers and cable drivers will be in the detector volume.

Liquid Argon/Krypton:

The liquid Argon/Krypton calorimeter is used as an unity-gain ionization chamber. The absorbing plates are accordian shaped, with the collecting gaps in between. The collecting electrodes are shaped and connected to give the appropriate sampling geometry. Preamplifiers are required to be very close to the collecting electrodes, in the liquid argon/krypton. The detector capacitance is large, so a FET input is required for lowest noise. Pulse shaping results in 40 ns wide signals. Noise per electronic channel is less than 100 MeV, so the dynamic range (signal/noise) is 16 bits (EM section). There is no gain control, so the ADC dynamic range must be large enough to cover gain variations between channels. To identify the correct beam crossing and reduce the effect of pile up noise, 5 samples (not necessarily contiguous) must be measured for each successful trigger. The switched capacitor analog storage system will sample the signals at the beam crossing rate.

Barium Fluoride electromagnetic section:

This option consists of Barium Fluoride crystals, with vacuumphoto-triode readout. The phototubes are oriented parallel to the magnetic field. A fast preamplifier is required after the phototube. Since the signals are fast and pile up is not expected to be a problem, no more than 3 samples are required, possibly only 1.

Scintillating fiber Hadronic Section:

The fibers are embedded in a matrix of heavy material. The signal is 100 photoelectrons per GeV deposited. Further amplification after

the photomultiplier is not required. The channel gains can be equalized by controlling the PMT high voltage. There are about 5000 photomultiplier channels. Noise is less of a problem than with liquid Argon, but photon counting and shower development statistics limit resolution at the low end. The PMTs will not resolve single photoelectrons, so the best case resolution is 2-3 photoelectrons. The dynamic range requirement is less than 16 bits. The signals are fast, about 10 ns wide.

To determine the longitudinal shower position, leading edge time measurement is required on the signal. The required resolution is 100 psec.

The electronic ADC system:

The ADC system is common to both candidate systems. The requirements are at least 16 bits dynamic range, pipeline delays and trigger outputs. The pipeline delay will be provided by a switched capacitor array sampling the input at the beam crossing rate. These arrays, as developed at LBL, have demonstrated a dynamic range of 12 bits, so both a high and low range channel are required, with x16 gain in the low range channel. This results in a 16 bit dynamic range, with minimum resolution of 8 bits. The LBL chips have been designed as 16 channel devices, so each chip can provide storage for 8 calorimeter channels.

The maximum expected Level 2 input rate of 100 KHz leaves just 10 microseconds to read out all channels. Since for LAR five samples are required, each channel must be instrumented with a 12-bit ADC capable of 500 kHz sampling. Alternatively, a single high-speed ADC can be usedc to service several channels. If, for example, there is one ADC per chip (eight dual-range channels) an 8 MHz ADC would be required. Such an approach will require a significant improvement in the the multiplexer output settling time of the SCA chip.

An electronic test and calibration system is required for the electronic chain, to verify function and stability. The primary energy calibration however, must be via a physics process.

Task list:

Liquid Argon calorimeter

1) preamplifier in the liquid Argon.This is a low noise, FET input preamplifier. It must be designed to operate at liquid Argon temperatures, and dissipate as little power as possible. There is little or no shaping at the preamplifier, the output is differential. This

requires a new preamplifier design, either custom monolithic or hybrid.

2) cables to just outside the calorimeter. This cable run is less than 5 meters. The cable should be shielded twisted pair. This is a an unterminated cable, to reduce the power required by the preamplifier.

3) shapers and line drivers. This produces a shaped signal, approximately 40 nsec peaking time, and drives a terminated differential cable. These circuits are mounted in small racks, on the outside of the liquid Argon cryostat or support structure. This requires a custom circuit board.

4) cables to ADC racks located outside the magnet, but inside the hall. This is a 20 meter cable run of shielded twisted pairs.

5) analog pipeline storage, and ADC system. This system is on standard large printed circuit boards, approximately FASTBUS size. The input accepts the differential signal from the shaper, and further shapes, and splits the signal into a high and low range. Each board can contain 64 calorimeter channels, each with a high and low range. This board provides prompt signals for the Level 1 trigger, and receives the trigger decisions. This requires a custom integrated circuit design.

6) crate by crate readout to the upper counting room. This cable run is at least 50 meters.

7) receiver/buffers for 800 optical fibers. Each channel requires a few thousand bytes of fast buffer.

8) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

9) Calibration system. This requires components in the liquid, comparable in complexity to the preamplifier, and some control functions located outside the magnet, near the ADC cards.

The signal processing uses a dual range system to achieve the required dynamic range. Two SCA and two ADC channels are required for each signal channel.

Liquid Argon/Krypton EM Calorimeter, 64k* channels

(*64K channels includes EM & Forward calorimeter)

Item	Engineering/design Labor my	Rate k$/my	Total k$	Material k$	EDIA Proc/Fab k$	Prototype Total k$	Proc/Fab $/chan	Material $k total
Preamp, 4 ch/monolithic chip, with integrated J-FET	0.50	161	80.5	30	150	260.5	6.00	384.0
Calibration system (this portion on preamp pc board)	0.50	161	80.5	30	150	260.5	6.00	384.0
Preamp PC board, 4 chan/sq.in	0.55	161	88.6	4	16	108.6	2.00	128.0
Cable to outside, 5m sh tw pair					20	20.0	1.50	96.0
Intermediate driver PC board	0.55	161	88.6	4	16	108.6	8.00	512.0
Cable to ADC racks, 20m					20	20.0	6.00	384.0
SCA chip, 8 ch/chip (not radhard)	2.00	161	322.0	40	150	512.0	6.00	384.0
SCA test station	1.00	161	161.0	50	50	261.0	2.00	128.0
12-bit high speed ADC, 8 ch/chip(not radhard)	2.00	161	322.0	40	150	512.0	6.00	384.0
ADC test station	1.00	161	161.0	50	50	261.0	2.00	128.0
FADC for trigger system							3.00	192.0
ADC PC board, 32 channel/board ==> 6. sq. inch/channel	1.50	161	241.0	10	20	271.5	48.00	3072.0
Rack slot cost $ 900./board							28.13	1800.3
Calibration pc board, 6 sq. in. / cal. ch., 32 signal ch/cal ch	1.50	161	241.0	10	20	271.5	3.00	192.0
DSP for on-board processing (+ 1 MY software engineer)	1.00	161	161	10	50	221.0	7.50	480.0
Rack slot cost, special rack, with remote power							1.50	96.0

Readout & comm. links, one/32 channels @ $ 370/ea		11.56	739.8
LVPS, 200mW/chan. 17.2 kW total @ $5/W		1.00	64.0
HVPS & Cable 1000 channels @ $ 200/ea		2.32	148.5
LAr/LKR Calorimeter Total	2827.0	144.01	9216.6

SPACAL Hadronic Calorimeter, 5.5k* channels

	Engineering/design			EDIA	Prototype		Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total		Material
Item	my	k$/my	k$	k$	k$	k$	$/chan	$k total
Calibration system	0.50	161	80.5	30	150	260.5	6.00	33.0
Cable to outside, 25m sh coax					20	20.0	20.00	110.0
SCA chip, 8 ch/chip (not radhard) (same as EM)							6.00	33.0
SCA test station (same as EM)							2.00	11.0
12-bit high speed ADC, 8 ch/chip(not radhard) (same as EM)							6.00	33.0
ADC test station (same as EM)							2.00	11.0
FADC for trigger system							3.00	16.5
ADC PC board, 32 channel/board ==> 6. sq. inch/channel (same as EM)							48.00	264.0
Rack slot cost $ 900./board							28.13	154.7
Calibration pc board, 6 sq. in. / cal. ch., 32 signal ch/cal ch	1.50	161	241.0	10	20	271.0	3.00	16.5
DSP for on-board processing (+ 1 MY software engineer) (same as EM)						7.50	41.3	

Rack slot cost, special rack, with remote power		1.50	8.3
Readout & comm. links, one/32 channels @ $ 370/ea		11.56	63.5
LVPS, 200mW/chan. 1.1 kW total @ $5/W		1.00	5.5
HVPS & Cable 1/chan @ $ 200/ea		200.00	1100.0
Calorimeter Total	551.5	345.69	1901.3

10. Silicon pre-radiator

*Note: This system is no longer in the GEM baseline and therefore its electronics costs have not been included in the WBS. The following is for reference only.

This is a silicon strip calorimeter, located just outside the tracker system. It consists of 3 radiation lengths of lead, and 2 layers of 1 mm pitch silicon strips (x & y). This does not participate in the 1st level trigger, but is expected to provide data for the 2nd level trigger. This detector may be embedded in the main calorimeter. The resolution requirements are modest, 6 bits linear, or 4 bits logarithmic. The electronics is inside the detector, the data is multiplexed out after the trigger decision, as the tracker systems. The calibration requirements are quite modest.

Task list:

1) preamplifiers. The input signal levels are modest, about 50 fC/mip (up to 1 pC in a shower). The shaping (peaking time) must be 20 nsec or less. This electronics must be radhard. This requires a custom integrated circuit design.

2) integrating switched capacitor array as developed for the outer tracker. the resolution is sufficient to eliminate the requirement for the special analog channel to measure the energy loss. Two wafers are combined in one readout, since the SCA is expected to be 16 channels.

Alternate readout:

2) logarithmic flash adcs followed by digital pipeline storage. Some combining of channels is possible here. Channels more than 16 strips apart can be resolved by the electromagnetic calorimeter, so can be combined after the preamplifier. This flash ADC must operate at the

beam crossing rate, and be low power. This electronics must be radhard. This requires a custom integrated circuit design.

2a) combined analog channel for precision charge measurement. This uses a switched capacitor storage array and adc as in the main calorimeter. This can measure the OR of 64 strips, so only one ADC per silicon wafer is required. This electronics must be radhard. This requires a custom integrated circuit design.

3) multiplexing data onto output fibers or cables. A multiplexing and sparsifying processor is required. This must be radhard. This requires a custom integrated circuit design.

All electronics is mounted very close to the silicon wafer. This puts a high premium on space and power dissipation. The space provided is about 15 square mm of circuit board for each silicon strip.

In the upper counting room the cable run is at least 80 meters.

4) receiver/buffers for 500 optical fibers. Each channel requires a few thousand bytes of fast buffer.

5) integration into the Level 2 trigger, and into the final data stream for Level 3. This is accomplished by sufficient buffer space on the receiver boards, and integration into the event builder.

Pre-Radiator, 14203 signal channels

There are 500k 1 x 64 mm strips in 2 layers. Strips are paired to form 128 mm long strips. Every 8th strip in a pair of wafers is combined into one signal channel. There are only 142203 signal channels. The total cost per signal channel is 16 times the cost per strip.

Note that the IC development cost may not be required, if these are the same ICs developed for the outer central tracker.

	Engineering/design			EDIA	Prototype		Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total		Material
Item	my	k$/my	k$	k$	k$	k$	$/chan	$k total
Preamp, 8 channel custom IC, 1/16 strips (rad hard)								
	1.00	161	161	60	300	521	3	42.6
Switched capacitor array chip, integrating or peak detecting 256 strips/chip (rad hard), 8-bit ADC included								
	4.00	161	616	80	300	1024	6	85.3

Chip test station	1.00	161	161	50	50	261	1	14.2
MUX and readout chip, 192 signals/ch (rad hard)	2.50	161	391	80	300	783	0.16	2.3
Complex PC board, one signal/sq.in	1.50	161	231	10	20	271.5	15	213.1
Total						2790	25.2	357.5

74 readout and comm. links, one for each 192 signals,80m		250ea	18.5
Receiver/buffer complex board, 6 sq. inch/link	90	6.7	
Rack slot space, $900/board	30	2.2	
Total		27.4	
Low voltage power, less than 100mw/channel, 1.5 kW total			7.5
High voltage supply, 900 channels	150	135	
Cables	50	45	
Total		187.5	

11. Trigger Systems

Master trigger crate

This system coordinates the subdetector triggers and combines them into the global trigger. It also orchestrates the multilevel trigger and keeps track of the buffer space available. This system consists of at least one workstation computer and a large quantity of fast logic.

Clock distribution (and other fast signals)

The pipeline storage for the Level 1 trigger delay are synchronous, and must be provided with the 60 MHz clock. The Level 1 accept signal is also synchronous. Both of these signals must be distributed with a timing skew of order 1 nanosecond to all detector signal channels.

The Level 2 trigger, and the data acquisition are asynchronous and do not require precisely timed signals.

Calorimeter trigger system

On each ADC board there will be an Analog sum for each 32 channels, followed by a 3 stage pipelined integrate, sample-hold and logarithmic flash ADC system capable of 16 ns throughput rates. This pipeline is also capable of detecting a local peak to avoid multiple triggering on several adjacent beam crossings when large signals are present. To a first approximation, this peak' detection will also determine the beam crossing. The 8 bit digital signals are converted to serial and leave the ADC board on an optical fiber. Assuming trigger towers of size .16 x .16, there are 1480 fibers for the Ecal and 1480 for the Hcal.

These signals are received on a board in the trigger system in the counting room, and converted to parallel signals, 8 bits every 16 ns are distributed to two systems, the Energy SUM and the Energy ISOLATION systems.

Each Energy Sum board adds 16 signals after converting the signals to a linear 12 bit code. The Sum is converted back to logarithmic before leaving the board. It requires 10 levels of summing and 20 pipeline steps to calculate the sum of 1024 signals. The total number of boards (all identical) is approximately 100.

The Energy ISOLATION board has 25 inputs, and computes the isolation cut for 9 of those inputs. Note that most signals are needed by 2 or more boards. The Electromagnetic calorimeter requires 165 boards, the Hadronic calorimeter requires 165 more.

Task list:

Analog sum on each ADC board. This is included in the ADC board cost estimate, but mentioned here for completness. This has a three stage pipeline for the shaped sum signal which successively integrates, measures with a flash ADC and resets. The ADC is nonlinear, giving 10-12 bits of dynamic range for 8 bits out. The 8 bits are sent to the trigger system via a serial optical link operating at a speed of 2 nsec per bit. (an 8 bit parallel ECL link is also possible). There is one analog sum for each 32 channels, or 2 per ADC board.

The Optical links to the trigger system in the upper counting room. A 32 channel receiver card which converts the data to 8 bits parallel, and fans it out to the trigger cards. Note that some signals have several destinations. The 8 bit signal is non-linear, it is converted to linear only when needed.

The Energy SUM card.

The Energy ISOLATION card.

3000 channels of Analog SUM and flash ADC. These are located on the ADC card, and the cost is included in that card.

Calorimeter trigger system, 2960 channels

Item	Engineering/design Labor my	Rate k$/my	Total k$	Material k$	EDIA Proc/Fab k$	Prototype Total k$	Proc/Fab $/chan	Material $k total
Optical link, 80 m ($ 250x4)							1000.00	2960.0
Receiver board, 8 channels, complex digital board								
	.50	120	60.0					
	1.00	60	60.0					
				10	20	150.0	192.00	568.3
Rack slot space, $600/board							75.00	222.0
Trigger Links Total						150.0		3750.3

Energy SUM Board, 16 Eight-bit inputs, 100 each for ECAL & HCAL

	Engineering/design Labor	Rate	Total	Material	EDIA Proc/Fab	Prototype Total		Proc/Fab Material
						$/board	$k total	
Complex digital board								
	.50	120	60.0					
	1.00	60	60.0	10	20	150.0	1600.	320.0
*Complex digital chips for summing (15/board)								
	1.25	120	150.0	40	150	340.0	1500.	300.0
Crate slot cost, $600/board							600.	120.0
Total						490.0	3700.	740.0

Energy ISOLATION Board, 330 boards, 25 Eight-bit Inputs

	Engineering/design			EDIA	Prototype		Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total		Material
					$/board	$k total		
Complex digital board								
	.50	120	60.0					
	1.00	60	60.0	10	20	150.0	1600.	560.0
*Complex digital chips for isolation sum (9/board)								
	1.25	120	150.0	40	150	340.0	900.	297.0
Crate slot cost, $600/board							600.	198.0
Total						490.0	3100.	1055.0

*Note: we assume chip costs of $ 100/ea since these are large pin count packages.

Muon trigger system

There are two approaches to the muon trigger. The first approach uses simple coincidence circuits and combinatorial logic on a large scale. This can be pipelined (only a few pipeline steps are necessary) at the 60 MHz beam crossing rate and can therefore be completely deadtimeless. The drawback of this approach is that the signals from individual trigger elements (RPC strips in the case of the barrel) must be routed to a common location.

A second approach uses content addressable memories (CAM's) to perform the logic. This approach employs element address information rather than individual element signals, which greatly reduces the number of cables---e.g. hits on a 256-element plane can be encoded as a list of (one or two) eight-bit words. However, since hits are processed in a serial fashion some deadtime is introduced. This deadtime is most likely tolerable since it is local in nature; a candidate track in one sector of the detector needn't deaden the entire array.

In the barrel RPC array the cable density is relatively low, leading one to favor the comparatively simple combinational approach. In the endcap, the trigger elements are much more densely packed, leading one to favor the CAM approach.

Barrel (RPC) Trigger

Since the drift times in the barrel drift tubes are several beam crossings long, resistive plate chambers are planned to provide the trigger information. The strip segmentation in the bend plane is fine enough to provide sufficient resolution to make the desired momentum cut.

(A backup system that will extract the beam crossing information from the drift wires themselves is under investigation, but that effort is still at an early stage.)

For the barrel, the signals from the RPCs or the wires themselves will be cabled to electronics located on the outside of the magnet. In each of the sixteen phi sectors there are 111, 187, and 240, azimuthal strips for the inner, central, and outer RPC layers, respectively. Since each strip is divided into two sections (+/- z) along its length there are a total of 17K azimuthal strips. Since the requisite logic is comparatively simple, the packing density is limited by the number of signals that can be routed to a single board. This is approximately 192 if double density (20 pairs/inch) flat cable is used. Allowing for edge effects, which will require some signals to go to two modules, we assume 160 signals per board, for a total of 108 complex digital boards. There are 16K z-strips, requiring an additional 100 boards of a different design.

Muon Barrel trigger system, 108 Phi boards

	Engineering/design			EDIA	Prototype		Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total		Material
Item	my	k$/my	k$	k$	k$	k$	$/board	$k total
Complex digital board								
	.50	120	60.0					
	1.00	60	60.0	10	20	150.0	1600.	172.8
*High pin count digital chips for track finding (4/board)								
	1.25	120	150.0	40	150	340.0	400.	43.2
Crate slot cost, special crate $ 900/board							900.	97.2
Total						490.0	2900.	313.2

Muon Barrel trigger system, 100 Z-boards

Item	Engineering/design Labor my	Rate k$/my	Total k$	Material k$	EDIA Proc/Fab k$	Prototype Total k$	Proc/Fab $/board	Material $k total
Complex digital board								
	.50	120	60.0					
	1.00	60	60.0	10	20	150.0	1600.	160.0
*High pin count digital chips for track finding (4/board)								
	1.25	120	150.0	40	150	340.0	400.	43.2
Crate slot cost, $900/board							900.	90.0
Total								293.2

Muon Barrel Trigger System Combiner Boards

Four Complex digital board designs, each replicated only a few times, total of 25 boards.
(details of these boards remain to be determined)

2.00	120	240.0					
4.00	60	240.0	40	80	600.0	1600.	40.0

Endcap System

As mentioned above, the endcap pad system Level 1 trigger is based on content addressable memories (CAM's).

For the endcap chambers, the logical grouping is a box, containing 4 layers of 256 pads each. The complete CAM system will be contained in the box. The CAM logic takes as input latched versions of the pad discriminator outputs, which are driven by the fast trigger-pickoff outputs of the pad preamplifiers (see section 6). When a potential trigger is detected in a group of pads the hit data in that group is latched and a local deadtime signal is asserted. The latched signals are routed to 256-input priority encoders, which produce eight-bit address words for the CAM (each CAM examines quadruplets of eight-bit addresses). The CAM's rapidly (the number of iterations is equal to the maximum number of hits allowed per plane) looking for valid track-segment matches, defined

as 3- or 4-fold coincidence among the 4 sub-layers that comprise the box. Track segments (or "match addresses") from the three boxes that comprise a superlayer are routed via optical fiber to the electronics room, where they are linked by a second CAM system into tracks. Since there can be more than one match on a given beam crossing, the system must be prepared to send more than match address to the segment linking CAM. Three optical fibers / box provide the link. The local deadtime induced by the CAM's is approximately 200 ns. if required, it can be largely eliminated by double buffering the latched inputs.

Since the electronics are chamber-mounted the technical risk is high.

Muon Endcap trigger system (250 boxes)

	Engineering/design			EDIA		Prototype	Proc/Fab	
	Labor	Rate	Total	Material	Proc/Fab	Total		Material
Item	my	k$/my	k$	k$	k$	k$	$/box	$k total
Latch/buffer/priority encoder chip, $16 each								
	1.25	161	201.3	40	150	391.3	1024	256
Content addressable memory chip, (large chip @ $100 each)								
	1.25	161	201.3	40	150	391.3	100	25
1 Gbits/sec optical link to trigger ($250x8)							2500	625
Complex digital PC board, 100 sq. inch, incl. sequencer								
	1.50	161	241.5	10	20	271.5	1500	375
Receiver board, 32 channel, complex digital board, 6 sq. inch/channel								
	1.50	161	241.5	10	20	271.5	270	67
Total						1325.6	5394	1348
Large CAM board for final track finding, 32 required, 1 per sector,								
16 CAM chips,						1600	51.2	
Complex PC board								
	1.50	161	231	10	20	271.5	3000	96
Crate slot cost, $900/board							900	28.8
Total						176		

12. Level 2 Trigger and DAQ

At this writing (6/12/92) designs do not exist for the data acquisition or the clock and control system of the experiment.

Very rough "placeholder estimates" and their supporting arguments follow. These estimates will clearly need to be replaced by considerably more detailed estimates before the time of the GEM TDR. Work on this is in progress.

The clock and control system is estimated to comprise the equivalent of ten high-complexity PC designs, replicated an average of 10 times each for a total of 100 boards. We assume that this work will be done by the SSCL DAQ group. Although much of the clock and control logic will be replicated only a small number of times and will therefore be implemented in field-programmable gate array or similar devices, it is estimated that three custom IC designs will be needed for use as variable delay elements along critical timing paths throughout the system. We assume 1000 units of each IC will be needed. In addition, it is estimated that 1000 fiber links will be needed for the distribution of clock and control signals.

Clock and Control System

	Engineering/design Labor			EDIA Mat'l	Proc/Fab	No# Designs	Prototype Total		Proc/Fab Material
Item	my	k$/my	k$	k$	k$		k$	$/bd	$k total
System Design									
	5.	69			345.				
(10 equivalent complex PC designs, 100 boards)									
	.5	69	34.5						
	1.0	50	50.0	10	20	10	1145	1600.	160
(3 equivalent complex digital IC designs)									
	1.25	69	86.3	40	150	3	828	--	---
Rack Slot charge (100 boards)								600.	60
1000 Fiber links @ $ 250./ea								250.	250
Total Clock and Control							2218		470

Level 2 Trigger

We are currently (4/92), in the process of establishing DAQ and Level 2 trigger groups. At this writing both of these systems are in an embryonic state and detailed cost estimates are not available. The following estimates are at best rough guidelines intended to set the scale for planning purposes.

Some preliminary work has been done on the calorimeter trigger. A few approaches have been investigated, mostly concentrating on designs where "filtered" data from the ADC's are routed to some sort of multiport memory that can be accessed by one or more high-speed microprocessors. The processors make use of Level 1 information to determine where in the memory to search for electron or photon candidates and then perform a detailed shower-shape analysis using the data from individual calorimeter elements. A preliminary analysis carried out by the SSCL DAQ group yields the following conclusions.

---The calorimeter data should be filtered on the ADC cards using low-cost DSP's, each of which services a few (four) channels. This gains an immediate factor of five to ten reduction in the data volume, since the five samples and two ranges can be combined into a single two-byte word.

---Assuming 50 channels per ADC card and fixed block transfers---i.e. all 50 words are transferred without zero suppression---a total of 100 bytes must be transferred to the multiport memory in 10 microseconds. Thus each board should be equipped with an FDDI link. ($ 250/ea)

---The memory will be limited by the number of links that can be handled by each board. The number of such links will be roughly the same as the Level 1 links, or about 3000 for the HCAL and ECAL combined. Assuming 32 links per receiver/memory board, we arrive at a total of 94 boards.

---The Level 2 algorithm requires approximately 100 microseconds on a fast microprocessor. Thus a "farmette" of approximately 10-20 processors is required. We assume one processor per complex digital board.

We thus incur the following costs:

Level 2 Readout				Total ($K)	
Item	Unit	#Req'd	Cost/ea	EDIA	Fab/Proc
Calorimeter-board DSP's (.25/ch)	ea	20K	$ 30		(600)
Programming Effort for above	MY	1	161K	(221)	

100 Mbit/sec fiber links	ea	3000	$ 370		(994)
Receiver/Memory board design	MY	2	120K	240	
Receiver Memory board fab.	ea	94	$ 1600		150.0
Crate slot charge	ea	94	$ 600	56.4	
Processor boards design	ea	2.5	120K	300	
Processor boards fab.	ea	20	$ 1600		32.0
Total for Level 2 Part			540	238.4	

The first three items (in parentheses) are part of the calorimeter front end and have been included there. Excluding them from the Level 2 costs yields a total of $ 780K which with a contingency of 40% yields a total of $ 1.09 M for the calorimeter trigger alone. Assuming comparable systems are needed for the central tracker and the muon systems (although the reduced data volumes in the muon system may result in lower costs), one arrives at a total Level 2 cost of $ 3.27 M.

Data Acquisition:

Since this has a large software development component, it is particularly difficult to estimate (and will likely remain so for quite some time). Based on previous projects of a similar scale (UA1, L3) it is estimated that a team of about ten dedicated DAQ people would be needed at the time the experiment turns on. This effort would start in the very near term at the two FTE level and increase steadily to full strength at turn-on. Starting in FY93 with two FTE's and assuming a linear increase to 10 FTE's in the year 2000, one arrives at a total of 45 FTE-years. At least 50% of these individuals should be full-time residents and are therefore estimated at the SSCL rate of $ 69K/MY, the remainder are visitors, for which we assume the national lab rate of $ 161/MY. This yields a total of $ 5.2M, to which a 30% contingency should be added.

Not included in this estimate is the DAQ hardware and whatever software licenses might be required. Note that the Level 3 ranch is part of the computing costs and therefore not included here. Moreover the first level of data collection has been included in the board costs of the front end systems. Conservatively, the hardware and software costs might total to a figure that is the same as the manpower costs for a grand total of $ 13.6 M. Although this is borne out by rough independent estimates, much work is clearly needed in this area. As mentioned, there is an effort underway aimed at producing a conceptual for the DAQ system, which will soon facilitate significantly reliable costing.