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SDC
SOLENOIDAL DETECTOR NOTES

SDC TRIGGER EMULATION MODULE (TEM): OPERATIONS MANUAL

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Part A: TEM Installation, Testing and Trouble Shooting Instructions
Part B: SDC Trigger Emulation Module Performance Specification

Part A : TEM Installation, Testing and Trouble Shooting Instructions

1 Introduction

This part of the TEM document provides instructions to install, test and trouble shoot the SDC Trigger Emulation Module (TEM). The TEM is designed to emulate much of the clock and control functionality anticipated for the final SDC Global Trigger System. See Part B of this manual for detailed description of TEM functionality.

2 Hardware Requirements

- TEM Module
- Power Adaptor Card to draw -2V and -5V (Included with TEM)
- Loop back cable (Included with TEM)
- 6U VME Crate. TEM draws +5V from Standard J1 and J2 VME backplane pins. (However, TEM can get by without J2 Backplane)
- VME Bus Master e.g. MVME147 / MVME167
- -2V (1.5Amps) and -5V (3Amps) Power supplies

3 Installation

- Unplug all power supplies.
- Connect -2V, and -5V power leads to the Power Adaptor Card.
- -2V and -5V power supplies must be grounded on the Power Adaptor Card or on the backplane.
- Select VME base address for the module using VME Address select jumpers A14 - A23. These jumpers select the decoding for the top 10 bits in 24 bit VME Address space. The bits are OFF when the pins are shorted. e.g. If the jumper A23 is NOT shorted and all others are shorted the 24 bit address for the module is 0x800000. On a MVME147 it maps directly to VME address 0x00800000. On a MVME167 it maps to 0xF0800000.
- VME Interrupt level is chosen using the interrupt request (VME IRQ) and acknowledge (VME IACK) jumbers near U32 and U11 parts on TEM. Note that these two switches SHOULD be set identically. Short one of the pins 1-7 to select VME interrupt level 1-7.
- Seat the TEM in one of the VME Crate slots. Plug in the Power Adaptor Card to the "wire wrap pins" on the back of the J2 backplane. If you do not have all three rows of "wire wrap pins" you are out of luck. If you do not have J2 backplane you can plug in

the Power Adaptor card directly on to the TEM J2 connector. However, in this case you should ground the -2V and -5V power supplies directly on the Power Adaptor card (See Warning below). TEM module is slightly thicker (84 mils) than standard VME modules. In case it does not fit in your card guides please get wider card guide. We had to mill our card guides a little. Two sample card guides are provided.

- Switch the power on for the crate including -2V and -5V supplies.
- Check that the bottom three LEDs on the TEM front panel are ON, indicating that the power is properly configured.

WARNING: When TEM modules are unplugged make sure that you also remove the Power Adaptor Cards from the J2 backplane. It is recommended that the TEM slot in the crate be keyed, such that only the TEM module with its small notch in the middle fits into that slot with Power Adaptor Card.

4 Software Requirements

- About 1MB disk space and RAM.
- ANSI Standard C Compiler
- Functions to turn off VME Address Security (If such security exists). OS9 functions are supplied.

5 Test Software Instructions

- The TEM TEST software is stored on the fnsg01.fnal.gov computer at Fermilab in the directory */usr/files/lv15/sdc_trig/TEM/tem_test* There is an account called sdc_trig available on that machine for SDC trigger group use. Contact S. Dasu or J. Butler for password. Refer to the README file in that directory for uptodate information.
- Edit the file "tem.h" and change the TEMBASEADDRESS definition to the base address that you selected. If you have a default base address different from your selected address, you will have to enter the BASE ADDRESS every time you run the test program.
- Edit main_menu.c and search for the word "permit". Change or delete the function call so that structure pointer "tem" is read/writeable. You might have to run the program in super user mode to achieve that.
- Edit Makefile and make sure it is suitable for your purpose.
- Compile and link software supplied.

- Connect Cntl-In and Cntl-Out ports on the front of the TEM using the Loop back cable supplied.
- Run TEM_TEST program. The menu is self explanatory. The test consists of running several "modules" that test various functions of the TEM. The modules are organized such that simple tests are done first. The test aborts as soon as an error is detected. You can turn off the offending modules and try the test again to check if rest of the modules work.
- If you want to run the test program with external clock selected you need a special loop back cable with clock inputs patched in along with the loop back cable. You also need to select external clock for the test explicitly.

6 TEM Interrupt Test Software

The interrupt test software is written in ANSI standard C but it does use OS9 specific functions. ULTRA-C is required to compile and run the programs. However, one can replace the OS9 specific calls with some other operating system specific calls. This program is available on fnsg01.fnal.gov computer in */usr/files/lv15/sdc_trig/TEM/intrpt* directory. The main functions in the program are:

icnt The program **icnt** establishes an interrupt handler and creates an OS9 global data module which contains counters. The interrupt handler wakes up on interrupts from the TEM and increments the counters in the data module.

igen The program **igen** talks the TEM to make it generate requested number of L1ACCEPT, L2ACCEPT or L2REJECT triggers, with sleep times between interrupts if needed. This program is not OS9 specific.

timeo The program **timeo** talks to the TEM to make it generate requested number of busy time out triggers. This program is not OS9 specific either.

dmpicnt The program **dmpicnt** dumps the contents of the OS9 data module containing interrupt counters.

zeroicnt The program **zeroicnt** zeroes the contents of the OS9 data module containing interrupt counters.

Remember to set the IACK lines on the VME crate appropriately before running the interrupt test software. You might crash the computer otherwise. To establish the interrupt handler one needs to be super user. The **icnt** program needs to be owned by the super user in OS9.

7 TEM Programming Utility

The program **pgen** available in the directory */usr/files/lv15/sdc_trig/TEM/pgen*, serves as a programming example and as a utility. This program reads a data file with simple instructions to specify a pattern. The pattern specification and instructions are described in the README file. **pgen** parses the instructions, loads the TEM FIFO, and spews out the programmed pattern. The pattern can be as long as 2046 words long. One can add simple looping control to repeatedly load the FIFO and spew out the programmed pattern. However, the process of loading the FIFO produces intermittant clock ticks. One may have to put in an explicit reset pulse and some nulls, at the beginning of the pattern to initialize the receiving electronics board.

pgen program uses ANSI standard C, and it does not have any operating system specific code. It should compile and run on any machine. If there is any VME memory address protection on your machine you should insert a call in the main function pgen.c to disable the protection.

8 Trouble Shooting

- Check the power LEDs on the TEM front panel. If any of those are OFF check the fuses:
  - Check fuses F1-F9. F1,F2 and F3 are for +5V, and are 4A slow blow type. F4, F8 and F9 are for -5V, and are also 4A slow blow type. F5, F6 and F7 are for -2V, and are 2A fast blow type.
  - Check fuses on Power Adaptor Card. These fuses are 10 A fast blow type.
  - The replacement part number for 4A slow blow type fuse is:
    Manufacturer: Littlefuse
    Part number: PICO III 473004 (4A - Slow Blow)
  - The replacement part number for 2A fast blow type fuse is:
    Manufacturer: Littlefuse
    Part number: PICO II 251002 (2A - Fast Blow)
  - The replacement part number for 10 fast blow type fuse is:
    Manufacturer: Littlefuse
    Part number: PICO II 251010 (10A - Fast Blow)
- Run the TEM_TEST program with logging turned on. Read the verbose output in the file. If it is not an obvious problem with your setup, contact T. Gorski (gorski @ wisssc.physics.wisc.edu) or S. Dasu (dasu @ wisssc.physics.wisc.edu), with an explanation of your setup and a copy of program output.

Part B : SDC Trigger Emulation Module Performance Specification

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1 Introduction

This document outlines the specifications of the SDC Trigger Emulation Module (TEM). The TEM is designed to emulate much of the clock and control functionality anticipated for the final SDC Global Trigger System. Its purpose is to aid in the test bench debugging of Subsystem front end electronics, DAQ and trigger circuits, and to serve the basic functions of a trigger module for test beam experiments. The TEM is designed to operate as part of a bench test of front end electronics, where it provides patterns of Level 1 and 2 Trigger and clock signals that can be fed in from either pulsers, an external Pattern Generation Module (see below) or a DAQ processor. The TEM is also designed to operate in a test beam, where the clock is externally provided by the accelerator RF signal and the triggers are produced by beam hodoscopes. The TEM provides the gating logic necessary to handle the interface to the DAQ processor, providing interrupts when triggers occur, and holding off triggers while the processor is busy, as well as monitoring this deadtime. The goal of the TEM development is to provide a module to which front end electronics and DAQ systems can interface that resembles the final interface to the trigger clock and control system. The TEM is designed so that a subsystem that operates with it should find minimal difference when the TEM is replaced with the final interface to the trigger clock and control system. This should ease eventual integration of detector electronics subsystems into the global SDC trigger clock and control system.

The TEM provides the Level 1 Accept/Reject, Level 2 Accept, Level 2 Reject, Level 1 Synch, Level 1 Reset, and Bunch Crossing 0 signals. It provides a test trigger output that can be used as an empty bunch indicator. It also carries a bit that is used to stop the clocks. The bits that indicate the state of these signals can either be filled up in a FIFO memory by the DAQ processor and played back at 16 nsec speed for 32 μsec, or be brought in on an external connector and delayed by a time programmable up to the 32 μsec depth of the FIFO. The 60 MHz clock can be generated internally or by an external RF clock. If the DAQ processor can only read one event at a time, then for each Level 1 Accept or Level 2 Accept, the TEM checks if the DAQ processor is busy. If not, it issues the trigger, and raises the busy until the DAQ processor reads out the event and lowers the busy. If the DAQ system is buffered, the TEM does not raise a busy and wait for the DAQ to clear it. Instead, the TEM issues Level 1 Accepts or Level 2 Accepts/Rejects until the DAQ raises the busy. It then stops Accepts/Rejects until the busy is cleared. The busy is brought in and out on external connectors so the busy can be chained with other modules. The TEM counts the number of Level 1 Accepts that should be issued and the number that are actually able to be issued when the DAQ processor is not busy. The TEM counts the time when the DAQ processor is busy and produces an interrupt if this time exceeds a preset value. The TEM can be reset via the DAQ processor or a frontpanel button.

In addition to the TEM, two other modules are planned for support of tests of front end electronics and test beam experiments. The first is a Clock and Control Fanout Module, which will provide a one-to-four fanout of the Clock and Control output from the TEM to the front end electronics. The second module is a Pattern Generation Module, which will use programmable memory lookup tables and state machines to generate long and

potentially complicated sequences of Clock and Control input data to drive the TEM. These sequences will run at the full 60 MHz clock speed and provide detailed tests of the interface between trigger, DAQ and front end electronics. The general functionality implemented by these modules is described in [1].

2 General Overview

The TEM is a 6U high, 160mm long, .084" thick (as opposed to the standard .062" thickness) VME card. The card contains a standard A24:D16 VME slave interface, with the ability to generate bus interrupts.

The card uses a mixture of ECL and TTL logic. For power, the card uses +5V, -5V, and -2V, which it receives from the crate via the backplane connectors P1 and P2. The -5V and -2V ECL voltages are applied to the card on P2 from a power adaptor card which plugs onto the other side of the backplane. This card is described later in the document.

Figure 1 shows a block diagram of the six major sections of the TEM. The VME Slave Interface provides the link between the other sections of the DAQ Processor in the crate. The slave is implemented for standard A24:D16 bus operation. The Slave Interface supports a local data bus which is active and controlled by the DAQ Processor during VME bus cycles to the card. The Slave Interface also decodes the VME address and read/write lines into individual read or write data strobes for the addressable locations on the card.

The Bus Interrupter/Status Register section contains the status register for the card and the logic to generate a VME bus interrupt request. Interrupt requests can be made in response to multiple events, including Level 1 or Level 2 Accepts, and a busy timeout condition. The status register and interrupt sources are described in greater detail below.

The Clock Generator/Select/Fanout Logic provides the high-speed accelerator clock source for the card. The card permits either an on-board 60 MHz oscillator or external clock from the frontpanel to be used as the clock source, as selected by DAQ Processor. This logic also has the capability to shut off and restart the clock to and from a low state, without generation of any spurious clock edges or partial-width clock pulses. This section also includes an 8-bit phase counter, which simply keeps a modulo-256 count of the number of high-speed clock cycles which have occurred. This counter can be used in conjunction with similiar counters on front end electronics components to verify the integrity of the high-speed clock distribution from the TEM.

The Reset/Configuration Register Logic distributes reset signals throughout the card. This section contains the 16-bit configuration register for the card, as well as the reset circuitry. The TEM supports three general types of resets which are stacked in a hierarchy: a "power-on" reset, which resets the board, including the VME-programmable configuration register to a known state, a "pushbutton" reset, which resets the board without modifying any of the VME-programmed registers, and a "counter clear" reset, which specifically targets the Busy Timer and Level 1 Accept Counters, which are explained

TRIGGER EMULATOR MODULE (TEM) BLOCK DIAGRAM

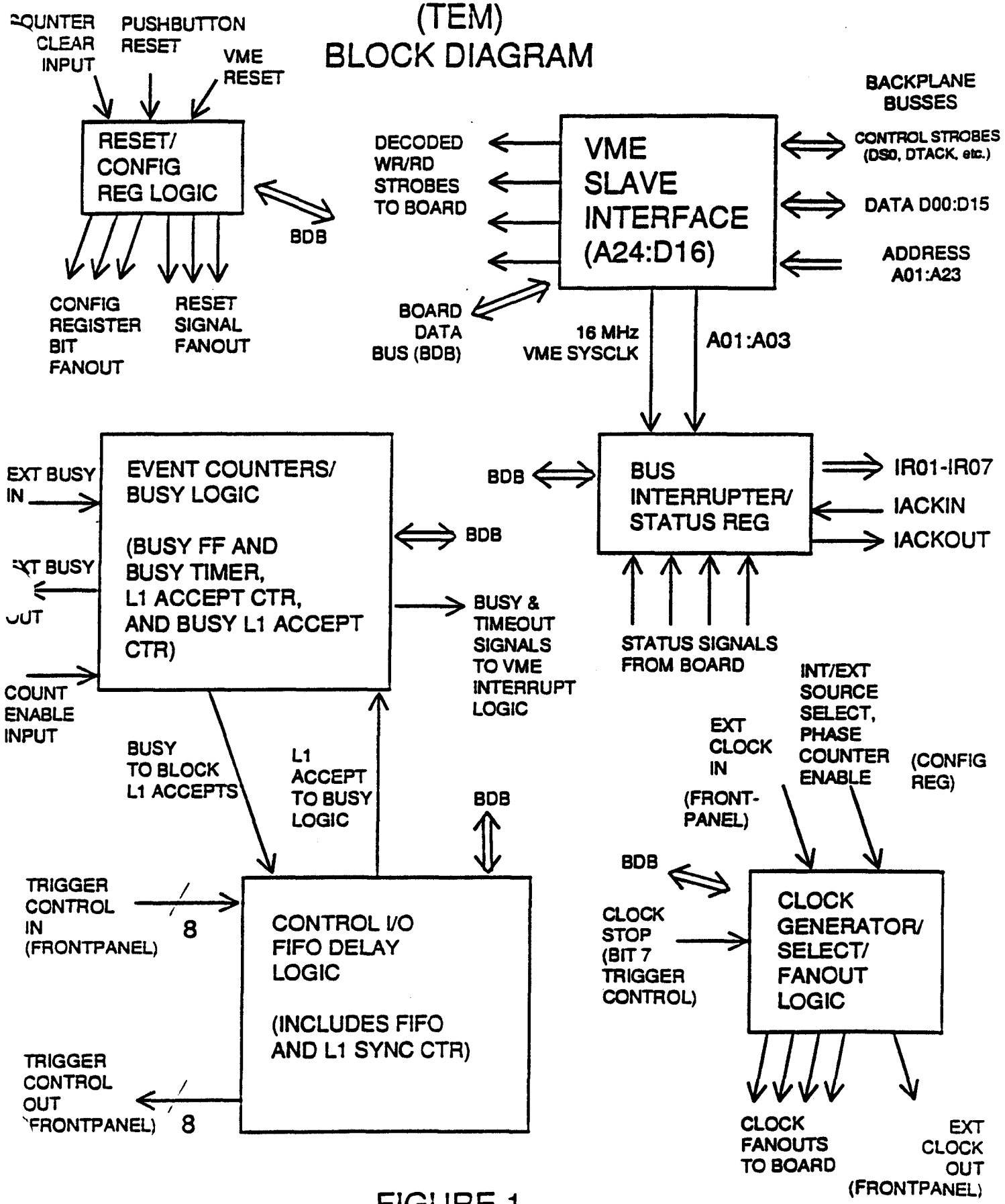


FIGURE 1

below.

The Event Counter/Busy Logic contains two event counters, a Busy Timer, and the Busy flip flop logic. The event counters are each 16 bits wide. One is used to count the overall number of Level 1 Accepts received by the card, while the second counts the number of Level 1 Accepts actually issued by the card while Busy is inactive. These counts are used to perform dead-time calculations. The Busy Timer consists of a programmable 16-bit prescaler to generate a slow timebase, called the "slow clock," from the high-speed clock, and a 16-bit down counter. This slow clock is used only to drive the down counter. The down counter is used to measure the real dead time caused by the DAQ processor, as well as provide a timeout signal which triggers a VME bus interrupt when the DAQ processor does not complete servicing of the Level 1 Accept within the preloaded time limit. If the DAQ processor has set the enable busy flip-flop bit, then the Busy flip flop activates the Busy when either a Level 1 or Level 2 Accept, as selected by the user is transmitted, and keeps it busy until it is serviced by the DAQ processor or reset. If the flip flop is not enabled, then the card will have a Busy status only when asserted by the DAQ Processor or the external Busy Input. The operation of the Busy flip flop is described in greater detail later in the document.

The Trigger Control I/O and FIFO Delay Logic receives the Trigger Control input from the frontpanel, passes it through a FIFO which introduces a programmable number of between 5 and 2K 16-nsec pipelined delay cycles, and delivers the Trigger Control stream back to the frontpanel as an output. Trigger Control input can also be supplied by the DAQ Processor via a VME access. Data from the DAQ Processor is bitwise ORed with the Trigger Control input from the frontpanel at the input to the FIFO. This section also contains a counter which automatically generates a Level 1 Sync pulse for every 256th Level 1 Accept transmitted, as part of the Trigger Control stream.

3 Trigger Control Bit Definitions

The TEM supports an 8-bit Trigger Control stream. As mentioned above, this stream enters the card through the Trigger Control inputs, is delayed for some number of high-speed clock cycles in a FIFO, and then delivered as output to the frontpanel. The stream to the Trigger Control inputs can come from the Pattern Generation Module or from other user-provided external circuitry.

Additionally, the DAQ Processor can supply words for the Trigger Control stream using two general methods. First, with the high-speed clock stopped, the DAQ Processor can fill the FIFO with contiguous Trigger Control words through VME bus cycles. When the FIFO is full, the high-speed clock can be restarted, and the contents of the FIFO will be transmitted to the Trigger Control output at the full clock rate. This method is useful for generating short determinate bursts of Trigger Control traffic at the end of which the clock can again be shut off. The FIFO has a capacity of 2047 words, which allows for approximately 32 μsec of storage at a 60 MHz clock rate.

In the second method, the DAQ processor simply writes Trigger Control words while

Bit Number	Definition
0	Level 1 Accept
1	Level 2 Accept
2	Level 2 Reject
3	Level 1 Sync
4	Level 1 Reset
5	Bunch Crossing 0/Spare
6	Empty Bunch/Test Trigger
7	Clock Stop

Table 1: Trigger Control Word Bit Definitions

the high-speed clock is active, using the same simple VME write bus cycle. The logic will grab the word and 1-shot it so that it appears in the Trigger Control stream for one high-speed clock cycle. This method is useful for generating longer streams of traffic which do not need have their timing aligned with a specific high-speed clock cycle.

Included in the 8-bit Trigger Control word is a bit for stopping the high speed clock, and a test trigger output bit, a copy of which goes to a separate frontpanel connector. The clock stopping bit, bit 7 of the definition below, permits the the high-speed clock distributed to the front end electronics to be shut off at a controlled interval with respect to the other bits in the Trigger Control stream. The test trigger output bit, bit 6, can serve as a start sync to an external pulser in test bench configurations, to commence a test sequence. This bit can also be used to fire charge injectors, which are used to calibrate front end electronics in test beam configurations. In this application, the test trigger signal must be generated a specific number of high-speed clock cycles before a Level 1 Accept, as determined from the inherent pipeline delay of the front end electronics.

Table 1 shows the bit name definitions of the Trigger Control word. The function of each of these bits is briefly described as follows.

Bit 0: Level 1 Accept. This bit is active for those crossings for which a Level 1 Accept is issued. It may be driven onto the TEM from the DAQ Processor via the VME bus or from an external counter via the Trigger Control input. The TEM blocks transmission of Level 1 Accepts to the Trigger Control output while the card is Busy. A pair of event counters on the card count the overall number of Level 1 Accepts received by the card, as well as those actually issued when the card is not busy. Separate Level 1 Accepts may not be issued on adjacent cycles, but a single Level 1 Accept may cover multiple clock cycles.

Bit 1: Level 2 Accept. This bit is active for one cycle to indicate a Level 2 Accept should be performed on the oldest Level 1 Accept pending in the buffers in the front end electronics. The Level 2 Accept pulse may be generated by the DAQ Processor via the VME bus or through external circuitry via the Trigger Control frontpanel input.

Bit 2: Level 2 Reject. This bit is active for one cycle to indicate a Level 2 Reject should be performed on the oldest Level 1 Accept pending in the buffers. The Level 2 Reject pulse may be generated by the DAQ Processor via the VME bus or through external circuitry via the Trigger Control frontpanel input.

Bit 3: Level 1 Sync. This bit is active for one cycle, accompanying every 256th Level 1 Accept issued by the TEM. This sync is generated by an 8-bit counter on the TEM, which is automatically reset by a Level 1 Reset signal or a Counter Clear pulse. This bit does not need to be externally driven from either the Trigger Control input or VME bus. Any additional pulses on this line would interfere with the operation of the on-board sync counter. However, the counter may be disabled by the DAQ processor, thus permitting this bit to be driven externally for other applications.

Bit 4: Level 1 Reset. This bit is active to indicate a Level 1 Reset operation. A Level 1 Reset can be initiated either by the DAQ Processor via the VME bus or by external control circuitry through the Trigger Control frontpanel input. The Level 1 Reset has no effect on the TEM other than to reset the Level 1 Sync counter. It does not function as a reset to the TEM card.

Bit 5: Bunch Crossing 0/Spare. This bit is defined as Bunch Crossing 0. It can be used in test beam operation to indicate the beginning of a sequence of RF buckets or can be used to synchronize counters when sent as a start pulse after a reset operation or can have other applications as a spare bit. As Bunch Crossing 0, it can be driven into the Trigger Control input from an external counter. This counter would generate a Bunch 0 pulse at a regular, predetermined interval of RF high-speed clock cycles.

Bit 6: Empty Bunch/Test Trigger. This bit is active on those crossings which contain an empty bunch. This bit is also driven to a Test Trigger Out connector on the frontpanel, where it may alternately be used in a variety of applications, such as providing a start sync for a pulser in a test bench environment, or triggering an oscilloscope during electronics debugging. It is anticipated that the most likely crossings to be used for test trggers will be empty bunches. The Test Trigger pulse will likely originate from the DAQ Processor, either as part of a FIFO fill-up with the clock stopped, or "on-the-fly", with the high-speed clock running. The Test Trigger Pulse can also originate from external control circuitry through the Trigger Control frontpanel input

Bit 7: Clock Stop. This bit is used by the TEM to stop the high-speed clock used and transmitted by the board. When this bit is active at the Trigger Control output, the TEM stops the clock after the next *falling edge*, and the clock remains in a low state. Once stopped, the clock can only be restarted either by the Clock Start VME strobe asserted by the DAQ Processor, or by a board reset, which is asserted either by the frontpanel pushbutton, or by clearing the TEM Enable bit in the board configuration register. The Clock Stop bit can be inserted into the Trigger Control data stream to provide a clock stop a fixed number of steps after a particular control sequence. The Clock Stop pulse can originate from the DAQ Processor, either as

part of a FIFO fill-up or with the high-speed clock running to catch the status "at random". The Clock Stop pulse can also originate from external control circuitry through the Trigger Control frontpanel input.

4 TEM Frontpanel

Figure 2 shows the frontpanel of the TEM card. The frontpanel has numerous LEDs to indicate card status, a pushbutton reset, TTL inputs for Busy and a Counter Clear signal, TTL outputs for Busy and a Test Trigger, and finally the differential ECL Clock and Control inputs and outputs. Each frontpanel item in Figure 2 is described in general below.

Pushbutton Reset. This reset switch provides a convenient means of resetting the TEM during use. This reset clears a Busy status due to pending service of a Level 1 Accept, as well as the Level 1 Accept counters. It causes the Busy Timer to reinitialize to its preloaded value, and clears/resets the FIFO and its associated pipeline delay logic. It also resets any latched Status Register bits (described below), and clears any pending VME interrupt requests. Finally, the reset also restarts the high-speed board clock if it was in the stopped state, although it does not change the clock source selection. It does not, however, affect the state of the configuration or interrupt vector registers.

RESET LED. This red LED illuminates while any counter clear, pushbutton or power-up reset is active, and also when the TEM is disabled via the TEM Enable bit (bit 0) of the configuration register.

VME I/O LED. This green LED flashes momentarily each time the TEM services a VME bus cycle initiated by the DAQ Processor.

BUSY LED. This red LED is lit for the duration of time which the card Busy status is true. The Busy status is true when the DAQ Processor is servicing a Level 1 Accept (if the Busy Flip Flop is set), the DAQ Processor is busy for other reasons, not ready, or when the Busy Input is active.

When Busy is true, the card will block the transmission of any Level 1 Accept signals from the Clock and Control Output described below.

INT CLK SEL LED. This red LED is lit if the on-board 60 MHz oscillator is selected as a high-speed timebase for the card. Alternately, the high-speed clock is received externally at the Clock and Control Input header. Clock source selection is controlled by the DAQ Processor through a configuration register on the card. The card defaults to the internal source on power-up.

CLK ON LED. This green LED is lit while transitions are regularly detected on the selected high-speed clock source, either the internal 60 MHz or an external RF clock. This LED goes out when the clock is shut off by the on-board clock stopping circuitry, or if the selected external RF clock is shut off or disconnected.

TEM FRONTPANEL

Pushbutton Reset. Clears Busy, Counters, FIFO, Status Register, Interrupts, and Restarts Clock

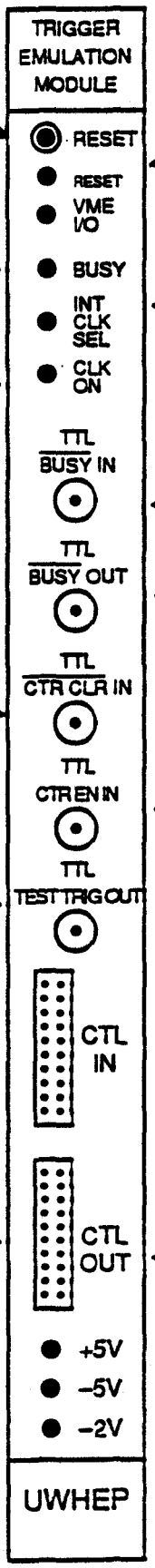
Busy LED. Lit when card status is Busy due to External Busy Input, DAQ Servicing of L1 Accept, or DAQ not online.

CLK ON LED. Lit when detecting active transitions on selected clock source.

Counter Clear Input. For reset of Event Counters in "burst mode" operation. Uses TTL levels and Lemo 00 Connector.

Test Trigger Output. Bit 6 of Control Output as TTL logic level to Lemo 00 Connector.

Clock and Control Outputs. Includes FIFO pipeline delay of programmed length, and L1 Sync on every 256th A1 Accept. Uses differential ECL logic levels.



RESET LED. On during reset or when TEM disabled by DAQ processor

VME I/O LED. Blinks for each VME bus cycle serviced by card

INT CLK SEL LED. Lit to indicate internal 60 MHz timebase selected as clock source.

Busy Input and Output. For external control and daisy chaining. Uses TTL logic levels and Lemo 00 Connectors

Counter Enable Input. Enables Event Counters and Busy Timer for use with external "Beam On" signals. Uses TTL Logic Levels and Lemo 00 Connectors.

Clock and Control Inputs. Includes L1 Accept, L1 Reset, L2 Accept, Clock Stop and other control signals. Uses differential ECL logic levels.

Internal Programmable FIFO Delay

Voltage Source LEDs. Indicate blown fuse on card for respective voltage when not illuminated.

FIGURE 2

Busy Input and Output. These are TTL logic, Lemo 00-type inputs and outputs. A logic-low level on the Busy input causes the TEM to register a Busy status. The Busy output is an active-low level reflecting the Busy status of the card. The TEM can be held in a Busy state by either the Busy input, a static bit in a configuration register, controlled by the DAQ processor via the VME bus, or (if enabled) by the Busy flip flop logic, which is activated by a transmitted Level 1 Accept and cleared by the DAQ Processor, Counter Clear input, or a reset.

If the Busy input is not connected, it automatically pulls up to a high, inactive state.

Counter Clear Input. This is a TTL logic, Lemo 00-type input. A logic-low level on this input clears the Level 1 Accept Counters and any Busy status *due to the pending servicing of a Level 1 Accept*. It does not clear a Busy status due to an active Busy Input or the DAQ Processor offline status.

The Counter Clear input can be used to reset the counters automatically from external logic, in a "burst mode" of operation. If this input is not connected, it automatically pulls up to a high, inactive state.

Counter Enable Input. This is a TTL logic, Lemo 00-type input. A logic-high level on this input enables the Level 1 Accept Counters and the Busy Timer. This signal may be tied to a spill gate output in order to limit the measurement of dead time to only those intervals in which beam is actually on.

If this input is not connected, it automatically pulls up to a high, active state, in which the counters are enabled.

Test Trigger Output. This is a TTL logic, Lemo 00-type output. Test Trigger Output is defined as bit 6 (out of bits 0–7) of the 8-bit Trigger Control stream. This output duplicates what is transmitted for this bit on the Clock and Control output connector. This bit is provided in TTL/Lemo format to conveniently serve as a general-purpose scope sync or startup sync to the DAQ subsystem.

Clock and Control Inputs. The Clock and Control inputs are received as ECL differential pairs on a 44-pin, high-density, subminiature-D header. The card receives one clock pair and 8 pairs which make up the Trigger Control input stream. The DAQ processor can select either this clock input or the on-board 60 MHz oscillator to provide the high-speed timebase source for the TEM card and DAQ system. In bench test configurations, the internal 60 MHz clock could be used, while in Test Beam configurations, an external RF clock source would be selected, with a maximum allowed frequency of 60 MHz, and no minimum frequency.

On the 8 Trigger Control input signals, the TEM receives the patterns of Level 1 Accepts and other previously-described signals which it turns around back out to the Clock and Control outputs, after passing them through a FIFO delay of programmable length between 6 and 2050 clock cycles, including latency due to inherent card pipeline stages.

These inputs may come either from hardware associated with the Test Beam or bench environments, or from a Pattern Generation Module (PGM) in an adjacent

VME slot. The PGM has the capability to generate Trigger Control sequences from pattern memories, and link together simple sequences to form more complex Trigger Control input streams.

Clock and Control Outputs. The Clock and Control outputs are delivered as ECL differential pairs on a 44-pin, high-density, subminiature-D header. A single copy of the high-speed board clock, from the selected source, either external or the internal 60 MHz oscillator, is delivered as the clock output.

Regardless of which clock source is selected, distribution of the high-speed clock to the DAQ subsystem from this header permits the clock stopping capability of the TEM to be used throughout the DAQ configuration.

The Trigger Control output is driven by the 8 bits of data received from the pipeline delay FIFO. Between the FIFO and the outputs is some additional logic which blocks the transmission of Level 1 Accepts if the card is Busy, and which also sends a Level 1 Sync pulse with every 256th transmitted Level 1 Accept. The Level 1 Sync may be used by DAQ subsystems to verify proper synchronization with the TEM.

Voltage Source LEDs. These are green LEDs which when lit indicate the presence of the specified voltages on the card. Each of these voltages is fused on the TEM. Should a fault occur which causes any fuses to open, then the LEDs for the affected voltages will go out.

5 Functional Descriptions

Figure 3 shows an actual-size view of the Assembly Drawing for the TEM. It features the frontpanel reset switch, LEDs and connectors, as well as the backplane DIN connectors. The circuitry on the card is divided up into seven main functional blocks, which are described in the following subsections.

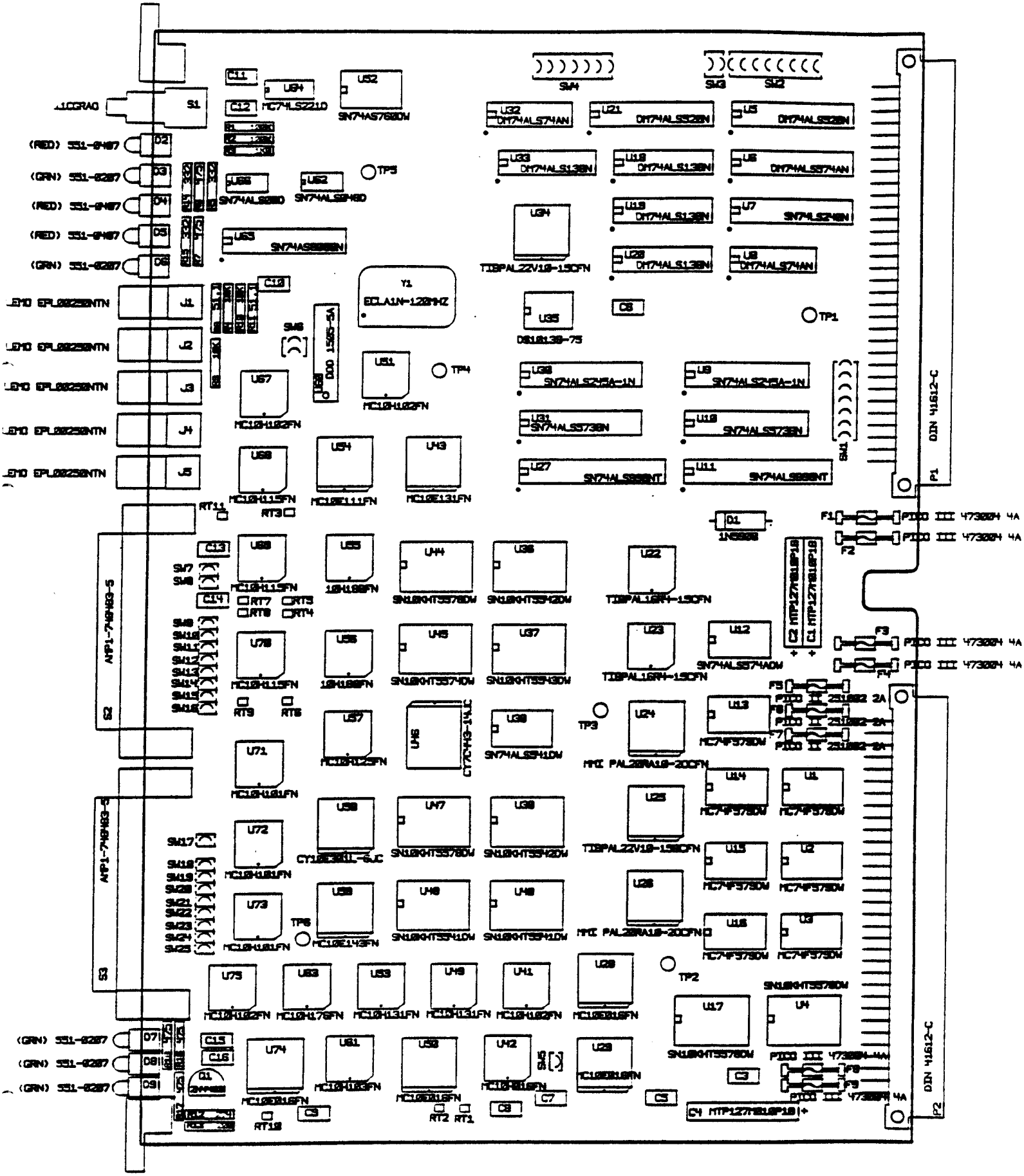
5.1 VME Slave Interface

The TEM is equipped with a VME slave interface which is compatible with standard IEEE 1014-1987.

The card acts as an A24:D16 slave. The card supports Address-Only cycles[2], but *does not* support block transfers. It does support read-modify-write cycles.

5.1.1 Address Modifiers

All I/O addressable space on the card is accessable in Standard Address Space, for Data Access. Thus, the card supports bus data transfer cycles only using Address Modifier Codes 39 hex (Standard Non-Priviliged Data Access), and 3D hex (Standard Supervisory Data Access). Address Modifier Codes are driven on lines AM0–AM5 of the VME Bus.


S1
U52
SN74AS760DW
U34
MC74LS221D
U32
DM74ALS74AN
U21
DM74ALS528N
U5
DM74ALS528N
U33
DM74ALS138N
U18
DM74ALS138N
U6
DM74ALS574AN
U19
DM74ALS138N
U7
SN74LS245N
U28
DM74ALS138N
U8
DM74ALS74AN
U34
TIBPAL22V10-15CFN
U35
DS1813B-75
Y1
ECLA1N-120MHZ
TP1
U38
SN74ALS245A-1N
U9
SN74ALS245A-1N
U31
SN74ALS573BN
U10
SN74ALS573BN
U27
SN74ALS888NT
U11
SN74ALS888NT
U51
MC10H102FN
U67
MC10H102FN
U68
MC10H115FN
U54
MC10E111FN
U43
MC10E131FN
U69
MC10H115FN
U55
10H188FN
U44
SN10KHT5578DW
U36
SN10KHT5542DW
U22
TIBPAL16R4-15CFN
U70
MC10H115FN
U56
10H188FN
U45
SN10KHT5574DW
U37
SN10KHT5543DW
U23
TIBPAL16R4-15CFN
U12
SN74ALS574ADW
U57
MC10H125FN
U46
CY2C443-14JC
U38
SN74ALS541DW
U24
MMI PAL20RA10-20CFN
U13
MC74F579DW
U71
MC10H181FN
U14
MC74F579DW
U1
MC74F579DW
U58
CY10E301L-6JC
U47
SN10KHT5578DW
U39
SN10KHT5542DW
U25
TIBPAL22V10-15CFN
U72
MC10H181FN
U15
MC74F579DW
U2
MC74F579DW
U59
MC10E143FN
U48
SN10KHT5541DW
U40
SN10KHT5541DW
U26
MMI PAL20RA10-20CFN
U16
MC74F579DW
U3
MC74F579DW
U73
MC10H181FN
U75
MC10H102FN
U63
MC10H176FN
U53
MC10H131FN
U49
MC10H131FN
U41
MC10H102FN
U29
MC10E016FN
U17
SN10KHT5578DW
U4
SN10KHT5578DW
U74
MC10E016FN
U61
MC10H103FN
U50
MC10E016FN
U42
MC10E016FN
U28
MC10E016FN
C4 MTP127N10P18
C2 MTP127N10P18
C1 MTP127N10P18
D1
1N5908
F1
F2
F3
F4
F5
F6
F7
F8
F9
PICO III 47300H 4A
PICO II 251002 2A
DIN 41612-C
P1
P2
S2
S3
AMP1-749483-5
AMP1-749483-1
(RED) 551-8487
(GRN) 551-8287
J1
J2
J3
J4
J5
D2
D3
D4
D5
D6
D7
D8
D9
Q1
2N4403
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
RT1
RT2
RT3
RT4
RT5
RT6
RT7
RT8
RT9
RT10
RT11
RT12
TP2
TP3
TP4
TP5
TP6
SW1
SW2
SW3
SW4
SW5
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SW15
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SW17
SW18
SW19
SW20
SW21
SW22
SW23
SW24
SW25

Figure 3

The card will ignore bus requests associated with any other Address Modifier codes.

5.1.2 Slot Address Decoding

The upper 10 bits of the 24-bit address space are interpreted by the card as the *slot address*. The TEM is configured by the user for operation at a particular slot address through on-board jumpers. The card will service a data bus transfer request by the master only when the card detects both a match in the slot address, and a recognized Address Modifier Code on the bus.

Of the remaining 14 bits of address space, only the bottom six, A01–A06, are referenced by the TEM.

5.1.3 On-Board Busses

The card has an on-board 16-bit data bus to support VME accesses. This bus is implemented in TTL, and is only active during VME bus cycles.

5.2 VME Bus Interrupter/Status Register

This block contains the circuitry for generating VME bus interrupt requests. It supports generating interrupt requests at any of the 7 priority levels. The priority level to be used for interrupt request and acknowledge cycles is selected via jumpers on the card.

The card has an 8-bit vector number register which provides an interrupt vector number during the interrupt acknowledge cycle. This register must be programmed with a valid user-defined vector number by the DAQ Processor during card setup, if VME interrupts are to be used.

The four possible sources for interrupts on the card are as follows: Level 1 Accept, Level 2 Accept, Level 2 Reject, and Busy Timeout. Each of these events is maskable as an interrupt source through bits 8–11 of the configuration register. Each of these four sources has an associated flag bit in the status register, as described below. During the interrupt service routine, the DAQ Processor interrogates the status register to determine the source of the interrupt.

The TEM card has a 16-bit status register which is readable by the DAQ Processor via the VME interface. Table 2 contains the bit definitions for this register.

The Board Busy status (bit 1) is active whenever the External Busy Input or Busy Flip Flop (bit 0) are active, or if the DAQ Busy bit (bit 3 of the configuration register) is set. Bits 3-7 are latched status bits. Of these bits, 3-6 can serve as interrupt source bits. Each of these bits can initiate a VME bus interrupt, as permitted by their corresponding mask bits in the configuration register. Each bit is set by a particular event, and once set, remains so until explicitly cleared. Bits 3-5 are cleared by a VME write to a "status

Bit Number	Definition
0	Busy Flip Flop Status (0 = not busy, 1 = busy)
1	Board Busy Status–logical OR of DAQ Busy (Config reg bit 3), Ext. Busy Input, and Busy FF (0 = not busy, 1 = busy)
2	Clock Stop Status (0 = clock enabled, 1 = clock stopped)
3	Level 1 Accept Transmitted (Maskable Interrupt Source)
4	Level 2 Accept Transmitted (Maskable Interrupt Source)
5	Level 2 Reject Transmitted (Maskable Interrupt Source)
6	Busy Timeout (Maskable Interrupt Source)
7	L1 Accept Counter Overflow
8	Busy Frontpanel Input (0 = busy inactive, 1 = busy active)
9	Counters/Timer Enabled (0 = disabled, 1 = enabled)
10	Prescaler Jumper Position (0 = jumper not installed, 2^{17} slow clock timebase, 1 = jumper installed, 2^{13} slow clock timebase)
11	Reset Flag (0 = no reset to card since last status read, 1 = reset occurred since last status read)
12–15	Spare (Zero)

Table 2: Status Register Bit Definitions

clear" mask explained later in the document. Bits 6 and 7 are cleared by a counter clear reset, either via the frontpanel LEMO connector, or a VME strobe. The persistence of latched status bits allow the DAQ Processor to identify even a transient event such as a Level 1 Accept pulse as the source of an interrupt request, long after the event occurred. Bit 8 shows the instantaneous status of the frontpanel Busy Input, latched at the time of the status register read. This bit is at a logic one to indicate that the Busy Input is active. Bit 9 shows whether or not the Event Counters and Busy Timer are currently enabled. When they are enabled, this bit is a logic one. The enable signal is the result of a logic AND between the frontpanel Count Enable Input and configuration register bit 1, the Event/Busy Count Disable bit. Bit 10 shows the position of the jumper which controls the Busy Timer slow clock prescaler rate. If the bit is a logic zero, then the jumper is not installed, and the slow clock prescaled rate is 2^{17}. If the bit is a logic one, then the jumper is installed, and the slow clock prescaled rate is 2^{13}. Bit 11 is set whenever the card receives a Counter Clear, "pushbutton", or "power-up" reset, and is automatically cleared by a status register read. It allows the DAQ Processor to determine that a reset of some kind has occured on the card.

The TEM uses the Release on Acknowledge (ROAK) method to drop the interrupt line. In this method, the active request signal on the backplane bus is automatically deasserted by the TEM during the acknowledge cycle for that interrupt.

As noted above, latched status bits are used by the TEM as the source for interrupt requests, with each bit logically ANDed with a corresponding mask bit in the configuration

register. For each enabled bit, and interrupt request is generated only when the status bit goes active. This means that subsequent events associated with a status bit, such as a Level 1 Accept pulse for example, will not cause interrupt requests, if they occur while the Level 1 Accept status bit (bit 3) is still latched from a previous event. Each status bit must be explicitly cleared by the DAQ Processor by writing the status clear mask described in section B.3, before another interrupt request associated with that event can be generated.

5.3 Reset Logic/Configuration Register

As stated previously, the TEM has 3 classes of resets, which are stacked in a hierarchy. The broadest in scope is the power-on reset, which resets the entire board, including the VME-programmable configuration register, to a known state. Next is the pushbutton reset, which resets the board without modifying any of the VME-programmed registers. Finally, there is the counter clear reset, which specifically clears the Level 1 Accept counters, Busy Timer, and the Busy status if it is due to waiting for the DAQ Processor to service a Level 1 Accept.

Each reset type can originate from two different sources. The power-on reset activates either during a VME access to the "Power-Up" Reset Strobe, described in section B.4, or when the backplane VME signal SYSRESET goes active, typically during a crate powerup or DAQ Processor reset. The pushbutton reset, as its name implies, is activated by pressing the pushbutton switch on the frontpanel, but is also active if the TEM Enable bit (bit 0) in the configuration register is at a zero state. Finally, the counter clear reset is activated by the application of a TTL logic low signal to the frontpanel Counter Clear LEMO connector, or during a VME access to the Counter Clear Strobe, described in section B.5.

This logic block also contains the configuration register for the card. This register is written by the DAQ Processor to control operation of the TEM card. Table 3 describes the bit definitions for this register. On powerup, this register is reset to an all-zero state.

5.4 Clock Generator/Select/Fanout Logic

This block provides the TEM with a high-speed clock. It contains a 60 MHz, 50% duty cycle source, a 2-input clock source select multiplexer, the clock stopping logic, a fanout buffer for driving the clock throughout the board, and finally a driver for shipping the clock out the frontpanel on the Clock and Control Output connecter.

The 60 MHz source is made using an on-board 120 MHz ECL oscillator source, which is divided by 2 to get the 50% duty cycle. This signal is sent to one input of the source select multiplexer, with the other input coming from the Clock and Control Input connector by way of a differential receiver. Source selection is controlled by the High Speed Clock Source Select bit (bit 4) in the configuration register, written by the DAQ Processer.

Bit Number	Definition
0	TEM Enable (0 = disabled, held in in "pushbutton" reset state, 1 = enabled).
1	Event/Busy Counter Disable (0 = counters disabled, 1 = counters enabled/controlled by frontpanel input)
2	Busy Flip Flop Enable (0 = disabled, 1 = enabled)
3	DAQ Busy (0 = DAQ Busy, 1 = DAQ not busy)
4	High-Speed Clock Source Select (0 = internal oscillator, 1 = external clock source)
5	Clock Phase Counter Reset/Enable (0 = reset, 1 = enabled)
6	Enable External Clock Output (0 = disable, 1 = enable)
7	Level 1/Level 2 Busy Select (0 = Level 1, 1 = Level 2)
8	L1 Accept Interrupt Mask (0 = no interrupt on status bit 8, 1 = enable interrupt on status bit 8 set)
9	L2 Accept Interrupt Mask (0 = no interrupt on status bit 9, 1 = enable interrupt on status bit 9 set)
10	L2 Reject Interrupt Mask (0 = no interrupt on status bit 10, 1 = enable interrupt on status bit 10 set)
11	Timeout Interrupt Mask (0 = no interrupt on status bit 13, 1 = enable interrupt on status bits 13 set)
12	VME-to-FIFO 1-Shot Disable (0 = enable 1-shot on VME data
	injection, 1 = disable 1-shot)
13	Control Input Enable (0 = frontpanel Trigger Control word input path disabled, 1 = path enabled)
14	Level 1 Sync Counter Enable (0 = disabled, 1 = enabled)
15	FIFO Enable (0 = FIFO disabled, 1 = FIFO enabled)

Table 3: Configuration Register Bit Definitions

The clock stopping logic blocks propagation of clock edges from the selected source to the board and external output. The logic is designed so that no spurious clock edges or partial-width pulses are generated on the clock, independent of the duty cycle of the selected clock source. The logic is activated by a rising edge on the Stop Clock bit (bit 7) of the output Trigger Control stream, or by the DAQ Processor. Once stopped, the clock is left in a logic low state, and can only be restarted by the DAQ Processor via the High-Speed Clock Start strobe, or by a pushbutton reset.

A form of "single stepping" of the clock can be performed by the DAQ Processor. With the high-speed clock stopped, the DAQ Processor can inject single clock pulses generated by VME bus cycles onto the clock using an OR gate. These single-step pulses are produced directly from the activated High-Speed Clock Single-Pulse strobe, and are approximately 75 nsec wide.

This section also includes an 8-bit Phase Counter, which is readable and resettable by the DAQ Processor. This TTL counter simply counts the number of high-speed clock cycles generated by the TEM, wrapping around every 256 cycles. When the high-speed clock is started, run for an interval and then stopped, the value on this counter can be read out by the DAQ Processor, and compared with the values on similiar counters in the DAQ front end electronics to verify the integrity of the clock distribution system. The Phase Counter is controlled by the Clock Phase Counter Reset/Enable bit (bit 5) in the configuration register. If this bit is low, the counter is held in a zeroed, reset state. If this bit is high, then the counter is enabled, and will count once for each high-speed clock. The Phase Counter should only be read out via VME while the high-speed clock is stopped, and before the counter is reset.

5.5 Event Counters/Busy Logic

This block contains the two Level 1 Accept counters, the Busy Timer, the Busy flip flop, and their associated control logic.

The Level 1 Accept counters are 16-bit counters readable by the DAQ Processer through the VME interface. They are reset to zero by a power-up, pushbutton, or counter clear reset. One counter tallies the total number of Level 1 Accepts received by the card, while the other only counts the number of Level 1 Accepts actually issued by the card while not Busy. If an overflow condition occurs, a status register bit is set, and the counters automatically wraparound.

The Busy Timer actually consists of two parts: a 16-bit prescaler to generate a slow clock, and a 16-bit up counter. The prescaler is a free-running counter which operates on the board high-speed clock. It divides the high speed clock down by a choice of two predefined factors, selected by an on-board jumper. When the jumper is installed, a prescale factor of 2^{13} is used. When the jumper is open, a factor of 2^{17} applies.

The up counter is used to both measure the duration of the interval in which the board Busy signal is active, and to set a timeout flag if a maximum duration is exceeded. The default duration limit is 65535 slow clock ticks, but this value can be changed by writing

a non-zero preload value to the Busy Timer address from the DAQ Processor.

The frontpanel Counter Enable input controls when the Event Counters and Busy Timer can operate. While this input is low, or disabled by the Event/Busy Counter Disable bit (bit 1) of the configuration register, these counters hold their current value and ignore all Level 1 Accept events and Busy status intervals. This frontpanel input permits the user to define those windows in which actual dead time calculations using these counters are to be performed.

Under normal operation, the Busy Timer automatically resets itself to the default value of zero when the Busy clears, and waits for the next Busy interval to begin the countdown again. However, if the Busy timer is allowed to count up to FFFF hex zero before the Busy clears, then it stops counting, sets the Busy Timeout bit in the status register, and generates a VME bus interrupt if enabled.

While the Busy Timeout bit is set in the status register, counting is disabled on both Level 1 Accept counters. Also, the Busy Timer will not restart until the Busy Timeout status bit is cleared by a counter clear reset.

The Busy flip flop and its associated logic, when enabled, automatically generate a Busy condition upon transmission of a Level 1 or Level 2 Accept. Bit 4 of the configuration register enables the Busy flip flop, and bit 7 of that register is the Level 1/Level 2 select. Once set in this manner, the board busy remains active until the flip flop is cleared by the DAQ Processor, counter clear, or other reset. In addition to the flip flop, a Busy status can also be asserted from the TTL Busy Input on the frontpanel, or by the DAQ Busy bit (bit 3) in the configuration register. While active, the Busy will block transmission of any additional Level 1 Accepts if Level 1 mode is selected or any Level 2 Accepts/Rejects if Level 2 operation is selected.

5.6 Control I/O/FIFO Delay Logic

This block consists of a loopback path from the Trigger Control input to the Trigger Control output on the frontpanel, with the path going through a programmable FIFO delay.

Between the Trigger Control input and FIFO sits the input gating logic. When enabled at bit 12 of the config register, this logic allows Trigger Control words from the frontpanel to pass to the FIFO input. When disabled, this logic blocks the passage of input data from the connector to the FIFO. This gating logic should be disabled when the frontpanel connector is not used, and Trigger Control words are sent to the FIFO only from the DAQ Processor via the VME Interface.

The FIFO can hold up to 2046 high-speed clock cycles worth of Trigger Control words at any time. At a high-speed clock rate of 60 MHz, this totals to approximately 32 μsec. As mentioned, Trigger Control words come either from the Trigger Control input, or from the DAQ Processor. The effective depth of the FIFO is determined by the DAQ Processor, using a preloadable delay counter. During normal operation with the high-speed clock,

a simultaneous read and write normally occurs on the FIFO on each clock cycle. In order to space the pointers within the FIFO to the proper distance, a counter delays the predetermined number of clock cycles after a reset before enabling reading. Thus, write operations which put data into the FIFO are permitted to get a particular number of cycles ahead of read operations which remove the same data from the FIFO. Each Trigger Control word thus spends the selected number of clock cycles inside the FIFO, between the time it is written, until it is subsequently read out. In this sense, the FIFO is able to emulate a pipeline delay.

On the output side of the FIFO, the TEM has gating logic which can inhibit the transmission of Level 1 Accepts or Level 2 Accepts/Rejects if the card is Busy, and a counter which transmits a Level 1 Sync along with every 256th Level 1 Accept transmitted. This counter is automatically reset by a Level 1 Reset signal.

5.7 LED Drivers

This block contains the LEDs and the circuitry to drive them. The RESET LED is on whenever the TEM is disabled (bit 0 of the configuration register), or when any of the three reset signals is active on the card.

The VME I/O LED uses a one-shot to generate an easily visible pulse on the LED each time the TEM services a VME bus request from the DAQ Processor.

The CLK ON LED also uses a one-shot to generate a visible pulse. This one-shot is triggered by logic which monitors the high-frequency When the clock is running, the LED appears to be on continuously. When the clock is stopped or disconnected, the LED turns off.

The BUSY and INT CLK SEL LEDs are driven from their respective sources with no one-shot pulse generation circuitry used.

The -5V and +5V LEDs are driven directly from these voltages on the board. The -2V LED is driven by making use of the -5V supply and a simple transistor switch.

6 Using the TEM

The TEM is designed to be used in both the test bench and test beam environments. A description of a typical setup in each environment is provided in the subsections below.

6.1 Typical Bench Test Configuration

In the "bench test" configuration, external pulse generators. counters, fanouts, and other modules can serve to emulate the beam and detector. Typically, the 60 MHz oscillator on the TEM is selected as the clock source for the setup, and is fanned out externally to

the card by a Clock and Control fanout module or equivalent circuitry.

Level 1 Accepts, and other signals in the Trigger Control word can be generated through two general methods. In the first method, with the high-speed clock stopped, the DAQ Processor fills the FIFO on the TEM with a Trigger Control sequence up to 32 μsec in duration. This sequence typically includes a Test Trigger pulse at the start to fire an external pulser, one or more Level 1 Accepts some cycles later, and finally a Clock Stop pulse at the appropriate time. When the system is ready, the DAQ Processor will restart the high-speed clock, and the Trigger Control stream will flow from the FIFO to the DAQ electronics.

In the second method, Trigger Control signals are transmitted to the TEM Trigger Control input from an external patch panel dynamically, with the high-speed clock continuously running. Signals such as Level 1 Accept, Bunch 0 Indicator, and Test Trigger are driven to the card by external counters which run off of the high-speed clock. These signals are driven at regular intervals, with a particular phase relationship to each other. For example, the Test Trigger signal could be used to fire an a pulser which generates a test pulse for the DAQ electronics. After the appropriate number of clock cycles have passed, the Level 1 Accept would be fired to instruct the DAQ electronics to capture that test pulse. The clock could then be stopped by firing a Stop Clock pulse from an external delay counter the appropriate number of cycles after the Test Trigger or Level 1 Accept. Signals such as the Level 2 Accept and Reject, and Level 1 Reset could be dynamically injected into the Trigger Control stream by the DAQ Processor without disrupting the high-speed clock.

6.2 Typical Test Beam Configuration

From the viewpoint of the TEM, the "test beam" configuration differs in only a few aspects from the bench test configuration.

First, the beam RF clock is selected by the TEM as the high-speed clock source, as opposed to the internal 60 MHz oscillator. Even with this change, it still makes sense to distribute the high-speed clock to the remaining components in the system from the TEM, in order to continue to take advantage of its clock-stopping circuitry.

Next, the external test pulse generation circuitry, which was driven by the Test Trigger signal, is replaced by the actual test beam and the associated detector. External trigger counters and circuitry would then generate the Level 1 Accept input to the card.

Another difference in the two configurations might be the use of external gating logic in the test beam environment to drive the Counter Enable Input on the card. This connection would cause the TEM to only measure Level 1 Accept events and busy time during intervals when the Test Beam "spill gate" was actually open and delivering beam to the DAQ front end electronics.

6.3 DAQ Processor Servicing of Level 1 Accepts

Independent of the installed configuration (test beam or bench test), and the means by which the Level 1 Accept was generated (canned sequence in FIFO, external bench test counter, or test beam trigger), the steps performed by the DAQ Processor to service a Level 1 Accept are basically the same.

When it receives a Level 1 Accept pulse, and it is currently not Busy, the TEM transmits that Level 1 Accept via its Trigger Control output to the DAQ electronics. At the same time, it sets bit 3 of the status register, and if the Level 1 Accept interrupt is enabled, generates a VME interrupt to the DAQ Processor. Also at this time, if the Busy flip flop is enabled and Level 1 mode selected, the Busy flip flop is set by the Level 1 Accept, thereby generating a Busy status which blocks any additional Level 1 Accepts from being transmitted, and starts the countdown of the Busy Timer.

Upon receiving the interrupt, the DAQ Processor reads the status register of the TEM and observes that a Level 1 Accept has been transmitted. The DAQ Processor then performs a readout of the DAQ electronics for this Level 1 Accept. When the readout is complete, the DAQ Processor then accesses the TEM again. First it reads the Busy Timer to determine the real time required to perform the readout, and then it clears the Busy flip flop if it was set.

By automatically asserting Busy as a result of each transmitted Level 1 Accept, the Busy flip flop automatically prevents the pileup of issued Level 1 Accepts. Once set, the flip flop keeps Busy active, thereby blocking any successive Level 1 Accepts, until the DAQ Processor has completed the readout and is ready for another.

When the Busy flip flop is not enabled, Busy is not automatically asserted, and multiple Level 1 Accepts can be issued by the card, and are stored in the system buffers. In this situation, Busy must be asserted by other means to prevent an overrun of the front end Level 1 Buffers. This is accomplished as follows. When the DAQ Processor senses that it is "falling behind" in the readout, it can cause a Busy on the TEM by zeroing the active-low DAQ Busy bit (bit 3) in the configuration register. This causes the TEM Board Busy status to go active, and thereby block further transmission of Level 1 Accepts by the TEM. Once the DAQ Processor has caught up, it deasserts the DAQ Busy, and transmission of Level 1 Accepts from the TEM can resume.

6.4 Level 2 Triggers

In both test configurations described above, the DAQ Processor has the responsibility to generate Level 2 Accepts and Rejects. and to send them to the TEM (via the VME bus) for subsequent retransmission to the DAQ electronics.

All housekeeping of Level 2 Accept and Reject counts must be performed by the DAQ Processor.

The Busy logic can be used for optionally blocking Level 2 triggers in a manner similiar

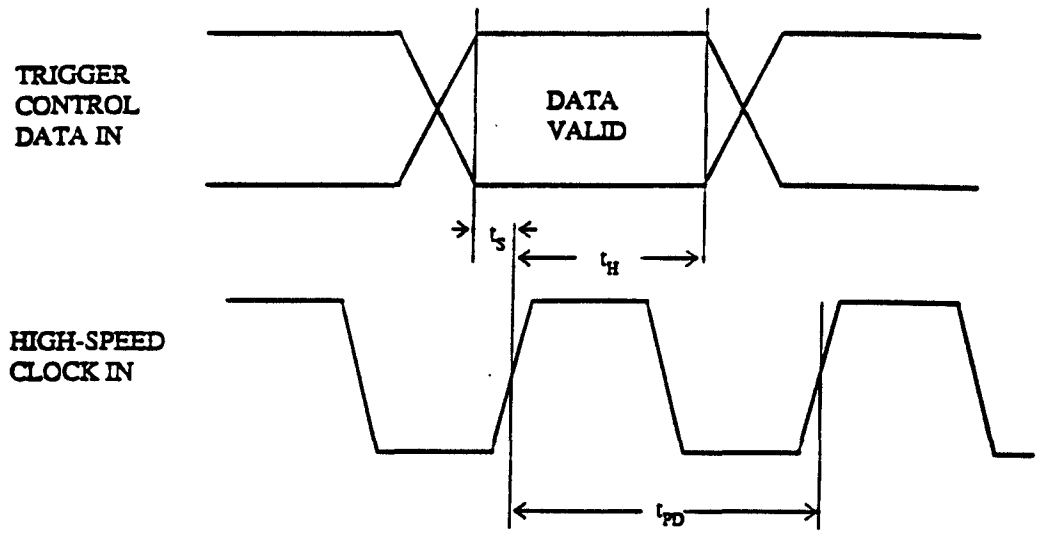

Figure 4: Clock and Control Input Timing Diagram

to that described in the previous section for Level 1 Triggers, by selecting Level 2 mode for the Busy logic on the Level 1/Level2 Busy Select bit (bit 7) in the configuration register.

7 Example Diagrams

This section provides example diagrams which illustrate certain aspects of TEM operation. In particular, the timing relationship between the high-speed clock and Trigger Control I/O on the frontpanel, and two types of Busy intervals are shown.

7.1 Clock and Control Input Timing

Figure 4 shows the timing requirements at the Trigger Control Input connector on the frontpanel for the receipt of both external clock and external data by the TEM. A well-defined phase relationship between the incoming clock and data is necessary, as this clock is used internally on the TEM to synchronously capture the Trigger Input data by the board's input register. Both the clock and data are received as differential 10K ECL signals.

The figure references five different timing parameters: t_S, t_H, and t_{PD}. Each of these parameters is described in Table 4. Note that these parameters by definition apply at the TEM input connector.

Table 4: Parameter Definitions for Clock and Control Input Timing

Parameter	Min	Max	Description
t_S	2 ns		Setup Time, Data Valid before Clock
t_H	3 ns		Hold Time, Data Valid after Clock
t_{PD}	16.6 ns		Clock Period

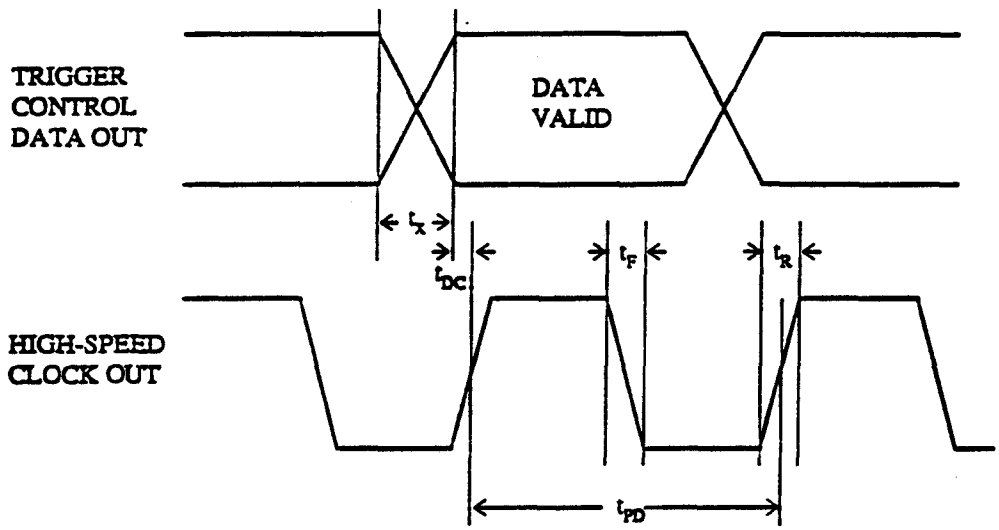

Figure 5: Clock and Control Output Timing Diagram

7.2 Clock and Control Output Timing

Figure 5 shows the timing at the Trigger Control Output connector on the frontpanel. At this connector the 8-bit Trigger Control word and a copy of the high-speed clock are driven out as differential 10K ECL signals.

The figure references five different timing parameters: t_X, t_{DC}, t_{PD}, t_R, and t_F. Each of these parameters is described in Table 5. Note that these parameters apply at the TEM output connector. The parameters as observed at the receiver will vary, depending on factors such as cable losses, capacitance, and length.

7.3 Busy Flip Flop Interval

Figure 6 shows an example Busy interval using the TEM Busy Flip Flop. Enabled by the DAQ Processor, this flip flop is set by the transmission of a Level 1 Accept at the Trigger Control frontpanel output. Once the flip flop is set, the board maintains a Busy status until the flip flop is cleared by the DAQ Processor. The duration of this Busy interval is

Table 5: Parameter Definitions for Clock and Control Output Timing

Parameter	Min	Max	Description
t_X		4 ns	Data Transition Time (includes skew and 80%/20% rise/fall)
t_{DC}	3 ns	6 ns	Data Valid to associated Clock rising edge
t_{PD}	16.6 ns		Clock Period
t_R/t_F		2.5 ns	Clock Rise/Fall Time

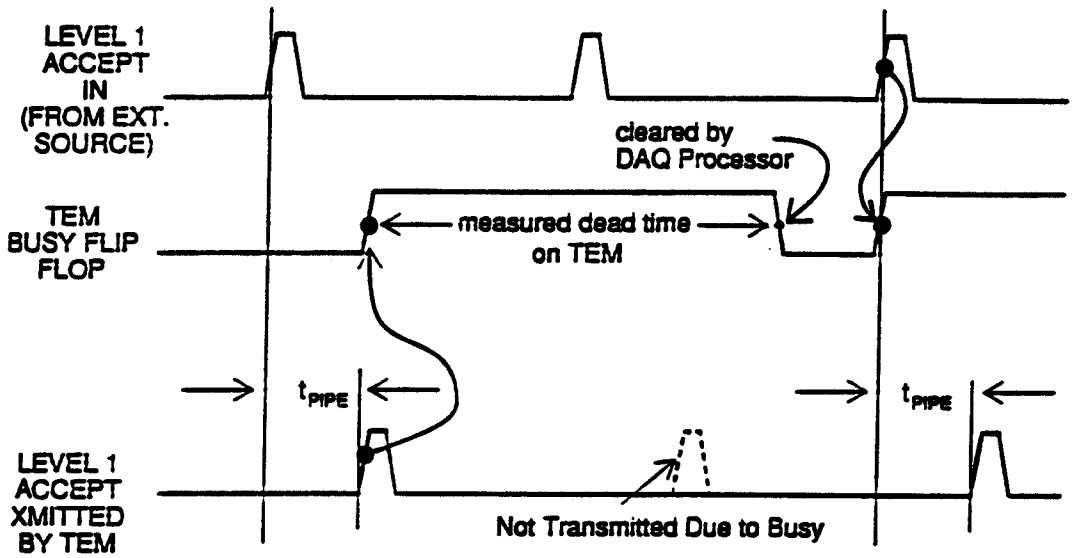

Figure 6: Busy Flip Flop Interval Timing Example

measured as dead time by the Busy Timer on the TEM.

While the Busy status is active, the TEM blocks the transmission of any additional incoming Level 1 Accepts, as shown in the figure. These events are not included in the count kept by the TEM of transmitted Level 1 Accepts. However, such Level 1 Accepts which are blocked from transmission are still counted by the card as part of the total Level 1 Accepts received count.

Figure 6 also shows a timing parameter t_{PIPE} separating the input and transmitted Level 1 Accepts. This parameter reflects the pipeline delay which is programmed into the TEM FIFO. As stated prevoiusly in the document, this parameter can be set by the user within the range of 5 to 2051 crossing clocks in length.

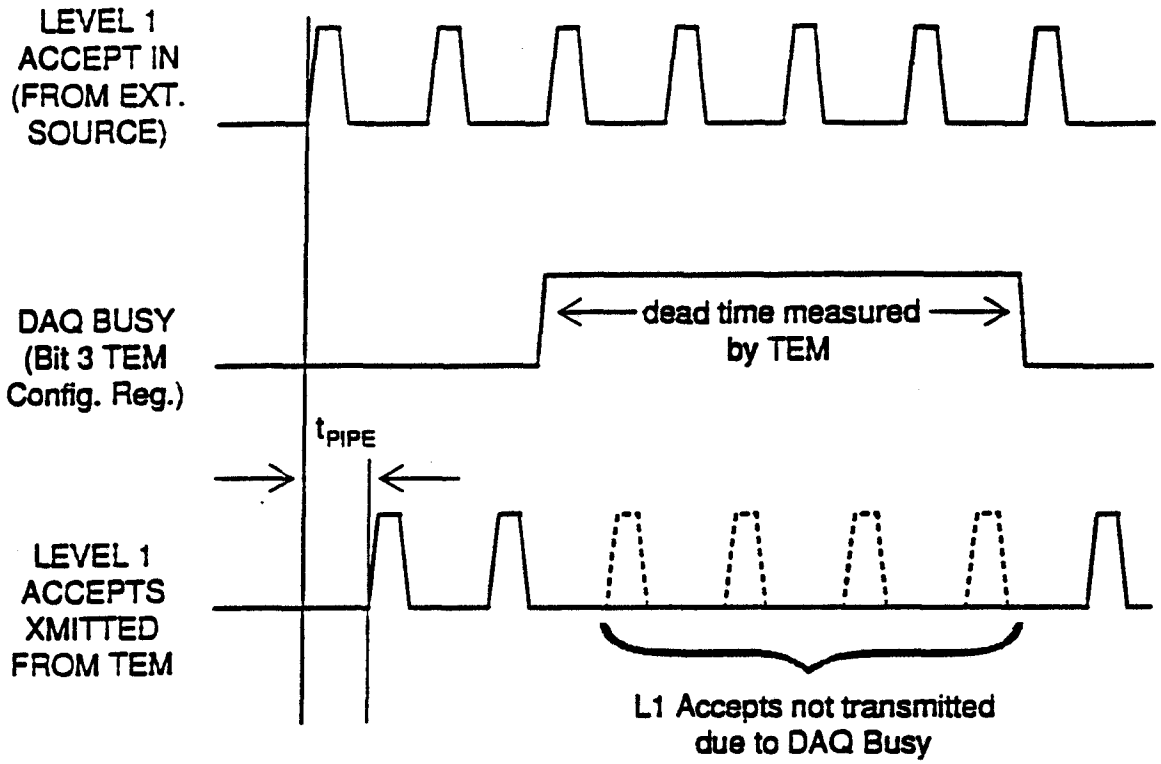

Figure 7: DAQ Busy Interval Timing Example

7.4 DAQ Busy Interval

Figure 7 shows an example Busy interval initiated by the DAQ Processor by asserting the active-low DAQ Busy bit (bit 3) in the configuration register. The DAQ Processor asserts this busy bit whenever it is unable to handle additional Level 1 Accepts. The duration of this Busy interval is measured as dead time by the Busy Timer on the TEM.

As in the previous example, while the Busy status is active, the TEM blocks the transmission of any additional incoming Level 1 Accepts, as shown in the figure. These events are not included in the count kept by the TEM of transmitted Level 1 Accepts, but are included in the total Level 1 Accepts received count also kept by the TEM.

This example also shows the pipeline delay parameter t_{PIPE}, which can be set by the user within the range of 5 to 516 high-speed clock cycles.

References

[1] W. H. Smith, T. Gorski, J. Lackey, *SDC Global Level 1 Processor: Clock & Control*, U. Wisconsin SDC Note SDC-91-00090, 1991.

[2] *The VMEbus Specification*, Revision C.1, 1985.

A Backplane Signal Definitions

Tables 6 and 7 show the backplane DIN 41612 connector pin assignments for TEM connectors P1 and P2. The pin assignments on P1 are per the standard VME definition. Only those signals with an actual electrical connection on the TEM are shown.

P2 is used by the TEM only for power and ground connections. The pin assignments on this connector follow the VXI standard for connector P2, with additional -5V, -2V, and ground assignments on rows A and C to support the ECL power requirements of the TEM, Fanout, or Pattern Generation Modules

Table 6: TEM P1 Pin Assignments

Pin Number	Row a Signal Mnemonic	Row b Signal Mnemonic	Row c Signal Mnemonic
1	D00		D08
2	D01		D09
3	D02		D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	
11	GND	BG3OUT*	BERR*
12	DS1*		SYSRESET*
13	DS0*		LWORD*
14	WRITE*		AM5
15	GND		A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20		GND	
21	IACKIN*		
22	IACKOUT*		
23	AM4	GND	
24		IRQ7*	
25	A06	IRQ6*	
26	A05	IRQ5*	
27	A04	IRQ4*	
28	A03	IRQ3*	
29	A02	IRQ2*	
30	A01	IRQ1*	
31			
32	+5V	+5V	+5V

Note: "*" denotes active-low signal.

Table 7: TEM P2 Pin Assignments

Pin Number	Row a Signal Mnemonic	Row b Signal Mnemonic	Row c Signal Mnemonic
1	-2V	+5V	
2	-2V	GND	
3	-2V		GND
4	GND		-5V
5			-5V
6			-5V
7	-5V		GND
8			
9			
10	GND		GND
11			-2V
12		GND	-2V
13	-5V	+5V	-2V
14			-2V
15			-2V
16	GND		GND
17			
18			
19	-5V		-5V
20			-5V
21			-5V
22	GND	GND	GND
23			
24			
25			GND
26			
27			
28	GND		GND
29			
30			GND
31	GND	GND	
32		+5V	

A.1 Power Adaptor Card

The Power Adaptor Card is a small printed circuit card which distributes ECL power from the crate supplies to the P2 connector, to supply power to the TEM or other module using the same pinout. A Power Adaptor Card is provided with each TEM module. The card is designed to mount on the long-tail, "wire-wrap" posts of the P2 connector in the same slot as the TEM, but on the back side of the backplane.

Physically, the card is 3U high by 1.8" long. It connects to the backplane via a right-angle, 96-pin female reverse-DIN connector. To connect to the power supplies, it has 2 .250" male tabs each for both the -2V and -5V supplies, and 2 .250" male tabs each for the ground return path to these supplies. It is recommended that in order to keep voltage-drop losses sufficiently low, AWG 12 or larger wire be used to make the connections between the card and the power supplies. Each voltage is fused on the card to 20A with fast-blow picofuses. For our DIN connector, we use Harting 09 73 196 6801 connectors, which are rated for current-carrying capacity at greater than 5 amps per pin at 60 degrees C, and 3 amps per pin at 100 degrees C.

B VME I/O Address Map

This section describes the VME addressable range of the TEM. It lists the addressable objects defined within that range, and describes their function. Table 8 shows the VME I/O Address Map. Each item in this table includes a board-relative byte address, an access type, and a general item description. Defined access types for the card include 8-bit or 16-bit reads and writes, plus "address only" (AO) accesses, which are performed simply as 16-bit write operations, where the write data is not used, and is considered a "don't care." AO accesses are simply used to generate control strobes on the board.

The board address space covers 24 distinct locations, which are decoded as shown in the table within the range of board-relative byte addressess 00 to 2F hex. The topmost 10 bits of the 24-bit address range are decoded by the card as the slot address. The card uses a on-board jumpers to select this address.

B.1 Configuration Register

Shown in Table 3, the configuration register is a 16-bit register which contains the various static signals required to control the TEM. It resets to an all-zero state when the crate is powered-up or reset, or due to a power-up reset issued by the DAQ Processor. This register supports both write and read accesses, with write access at board address 00 hex, and read access at board address 20 hex. (The fact that read and write access occurs at different addresses is the result of the desire to keep the address decoding circuitry on the card as simple as possible.)

Table 8: TEM VME I/O Address Map

Hex Address	Access	Description
XXX000	W16	Configuration Register (Write Access)
XXX003	W8	VME Interrupt ID Register (Write Access)
XXX005	W16	Status Bit Clear Mask
XXX006	AO	"Power-Up" Reset Strobe
XXX008	AO	Counter Clear Strobe
XXX00B	W8	FIFO Write Port
XXX00C	W16	FIFO Depth Select Register
XXX00E	W16	Busy Timer Preload Port
XXX010	AO	High-Speed Clock Stop Strobe
XXX012	AO	High-Speed Clock Start Strobe
XXX014	AO	High-Speed Clock Single-Pulse Strobe
XXX016	AO	Busy Flip Flop Clear Strobe
XXX018		(Spare Write/AO Address)
XXX01A		(Spare Write/AO Address)
XXX01C		(Spare Write/AO Address)
XXX01E		(Spare Write/AO Address)
XXX020	R16	Configuration Register (Read Access)
XXX022	R16	Status Register
XXX024	R16	Total Level 1 Accept Counter
XXX026	R16	Non-Busy Level 1 Accept Counter
XXX028	R16	Busy Timer
XXX02B	R8	FIFO Read Port
XXX02D	R8	Clock Phase Counter
XXX02F	R8	VME Interrupt ID Register (Read Access)

Note: "XXX" denotes the upper 12 address bits, the lower 2 of which must be zero, with the upper 10 determined by the Card Address jumpers on the TEM.

B.2 VME Interrupt ID Register

This is an 8-bit register that contains a user-defined interrupt vector number, which is used to identify the TEM to the DAQ processor as the requestor on VME Interrupts. The vector written to this register is system dependent, and must be determined by the user.

This register is written using a VME byte access to byte address 03 hex on the TEM. It is read using a VME byte access to byte address 2F hex on the card. It is not initialized to any state by a power-up reset, and must be initialized prior to use of VME interrupts by the TEM.

B.3 Status Bit Clear Mask

The Status Bit Clear Byte is a 16-bit location at byte address 04 hex on the card which is written to clear the latched Level 1 Accept, Level 2 Accept, and Level 2 Reject bits (bits 3–5) in the Status Register. Referring to Table 2, these bits are "latched"–that is, once set, they remain so until the card receives a pushbutton reset, or until the bits are explicitly cleared by a write to the Status Bit Clear Byte.

A given status bit is cleared through a VME write to the Status Bit Clear Mask, in which the bit is set corresponding to the status bit to be cleared. Thus, bit 3 set clears the Level 1 Accept status bit, bit 4 set clears the Level 2 Accept status, and bit 5 set clears the Level 2 Reject status. These 3 bits in the status clear byte operate independently of each other, and may operate simultaneously. All other bits in this byte are ignored.

B.4 "Power-Up" Reset Strobe

This strobe is generated through an AO access (16-bit write data transfer on VME bus, where the data is a "don't care") to byte address 06 hex on the card. This strobe is equivalent on the TEM to the actions of VME SYSRST, which goes active at crate power-up or reset.

On the TEM, this reset has the greatest breadth possible. It resets most programmable registers, such as the Configuration, FIFO Depth and Prescaler Registers to their programmed defaults, as well as causing pushbutton and counter clear resets to occur.

B.5 Counter Clear Strobe

This strobe is generated through an AO access to byte address 08 hex. It is functionally equivalent to the Counter Clear Input signal input through the frontpanel connector, and is in fact OR'ed with that signal to produce the Counter Clear signal used by the card.

The Counter Clear signal asynchronously resets both Level 1 Event Counters and the

Busy Timer to zero. It also clears the Level 1 Counter Overflow and Busy Timerout status bits. When reset in this manner, the Busy Timer will commence counting again on the next transition of the card from the non-Busy to the Busy state.

B.6 FIFO Write Port

The FIFO Write Port is an 8-bit location at board address 0B hex written by the DAQ Processor in order to load a Trigger Control word into the FIFO. It is written using a VME byte access to address 0B hex on the card.

Through this port, Trigger Control words can be OR'ed onto the path from the Trigger Control frontpanel input to the input of the FIFO. Words written through this port are automatically "1-shotted" so that they are written to the FIFO only one time on one high-speed clock cycle, even though approximately one half-dozen high-speed clock cycles actually occur during the interval of time that the VME write takes place.

This port can also be used to prefill the FIFO from the VME interface. In this mode, the High-Speed clock is stopped, and the FIFO is written by alternating writes to the port with High-Speed Clock Single Pulse strobes, generating single pulse on the High-Speed clock for each VME access. If desired, the single clock pulses can be blocked from being transmitted outside of the card by clearing the External Clock Output Enable bit (bit 6) in the Configuration Register. Each write to the port will set up a new Trigger Control word to be written to the FIFO, and each single pulse will write it.

B.7 FIFO Depth Select Register

The FIFO Depth Select Register is a 16-bit register at board address 0C hex written to set the desired depth of the FIFO. The FIFO depth determines the number of high-speed clock cycles of pipeline delay seen by the Trigger Control words on the TEM. The register can be programmed to select 1 to 2047 cycles of FIFO delay. When added to the 4 clock cycles of I/O register overhead in the TEM circuitry, the result is a sum total of 5 to 2051 high-speed clock cycles of pipeline delay.

After a power-up or pushbutton reset, writes automatically commence to the FIFO on each high-speed clock cycle. At the same time, a depth counter generates the specified number of cycles of delay. During this delay period, no reads are performed on the FIFO, and it fills up to the specified depth. Once the delay expires, reads are enabled, and thereafter, both a write and read are performed on the FIFO on each high-speed clock cycle. The FIFO will then maintain this phase offset between its internal write and read pointers, and thus an effective pipeline delay, until the next reset.

On a power-up reset, the register automatically defaults to a total pipeline depth of 2051 cycles.

B.8 Busy Timer Preload Port

The Busy Timer Preload Port is a 16-bit write location at board address 0E hex written to set a non-default timeout limit value for the Busy Timer. The Busy Timer is used to both measure the real busy time observed by the TEM, as well as to generate a VME interrupt request if a specified Busy time limit is exceeded. The Busy Timer is driven by a free-running slow clock source, which is a prescaled version of the high-speed clock.

After it is read out or reset, the Busy Timer has a default preload value of 0, which corresponds to a timeout interval of 65535 slow clock ticks. Prior to clearing the Busy, the DAQ Processor may write a new preload value to the Busy Timer through this preload port. By writing a non-zero preload value, the DAQ Processor reduces the number of slow clock ticks it will take for the Busy Timer to count up to its timeout value of FFFF hex, and thereby shorten the duration of time between the onset of a Busy and a timeout interrupt.

B.9 High-Speed Clock Stop Strobe

This strobe is generated through an AO access to byte address 10 hex. Like the Clock Stop bit (bit 7) in the Trigger Control word, this strobe causes the high-speed clock to be shut off to the zero state. Although the strobe occurs asynchronously to the high-speed clock, the clock stop circuitry is designed so that no spurious edges or partial-width clock pulses are generated. On the first normally-occuring falling edge after the clock stop strobe is generated, the clock remains in zero state.

Once stopped, the clock will remain at a zero state until restarted, either by a High-Speed Clock Start strobe, or by a pushbutton reset.

B.10 High-Speed Clock Start Strobe

This strobe is generated through an AO access to byte address 12 hex. It causes the high-speed clock to be turned once again after it has been stopped. As is the case with the Clock Stop strobe, this strobe will not cause any spurious edges or partial-width clock pulses to be generated. Upon receipt of this strobe, high-speed clock pulses will again be generated starting with the next *normally scheduled* rising edge of the clock.

The start/stop status of the high-speed clock can be interrogated at bit 2 of the Status Register. The default state after a reset is to have the high-speed clock turned on.

B.11 High-Speed Clock Single-Pulse Strobe

This strobe is generated through an AO access to byte address 14 hex. It provides a simple single-pulse capability on the high-speed clock, which can be both useful for system debug,

as well as necessary for certain aspects of TEM setup, such as prefilling the FIFO from the the DAQ Processor.

This strobe is intended to be used *only* when the high-speed clock is turned off. It produces a high-going pulse approximately 75 nsec in duration, which is OR'ed onto the high-speed clock path after the clock stopping logic, at a point prior to the fanout circuitry which distributes the clock throughout the TEM and to the External Clock Output on the frontpanel.

This strobe has a number of general uses. First of all, it is used to verify proper operation of the TEM itself, as part of a software-controlled test of the various components of the board. The card is set up into a predefined state, and a metered quantity of pulses are applied. The card state is then interrogated, and compared against what would be expected given the number of clock cycles.

The pulse can also be used to single-step the test beam hardware configuration, specifically including those electronic components which receive their high-speed clock from the TEM.

Additionally, the Single-Pulse strobe must be used by the DAQ Processor to load the FIFO, either for FIFO-testing purposes or for actual Test Beam use. As the FIFO writes data on every high-speed clock cycle, in order for the DAQ Processor to successfully write a series of Trigger Control words into contiguous locations in FIFO memory, it must first stop the normal high-speed clock through the Clock Stop strobe described above. Then, it can alternate writes to the FIFO Write Port with Single-Pulse strobes to fill the FIFO. Once the FIFO is filled and the test is ready, the DAQ Processor restarts the high-speed clock and the pre-programmed Trigger Control words will be delivered to the Trigger Control Output on the frontpanel at the full data rate.

B.12 Busy Flip Flop Clear Strobe

This strobe is generated through an AO access to byte address 16 hex. It clears the Busy Flip Flop, which, when enabled, is set by the transmission of a Level 1 or Level 2 Accept at the Trigger Control Output on the frontpanel.

This flip flop is enabled to automatically generate a Busy status each time a selected Level 1 or Level 2 Accept is transmitted. This Busy status automatically blocks the further transmission of Accepts for the Level 1 Trigger, or Accepts and Rejects for the Level 2 Trigger, while the DAQ Processor performs the readout of the front end electronics. Bit 7 of the configuration register selects whether the flip flop will operate on the Level 1 or Level 2 Trigger. When the DAQ Processor is ready to process further Accepts, it clears the Busy Flip Flop using this strobe.

B.13 Status Register

Shown in Table 2, the Status Register is a 16-bit read-only register whose individual bits are defined to show the current state of operation of the TEM. The register is accessed at board byte address 22 hex.

Bits 0–2 and 8–10 of the Status Register are "instantaneous"status signals which are only latched for VME reads. Bits 3-7 of the Status Register are "latched", which means that once set, the must be cleared either by a board reset or by accessing the Status Bit Clear Mask. Bit 11, the reset flag, is automatically cleared by the status register read. See Section 5.2 for a description of the status register and its bit definitions.

B.14 Total Level 1 Accept Counter

Board address 24 hex is the VME read address for the 16-bit Total Level 1 Accept Counter. As its name implies, this counter totals the number of Level 1 Accepts, including those while the card was Busy, which were seen by the TEM when the counter enable signal was active.

This counter is reset to zero by either a counter clear signal or by a board reset. It can count up to 65535 Level 1 Accepts. If an attempt is made to count beyond that limit, the L1 Accept Counter Overflow bit (bit 7) in the Status Register is set, and the counter wraps around automatically.

B.15 Non-Busy Level 1 Accept Counter

Board address 26 hex is the VME read address for the 16-bit Non-Busy Level 1 Accept Counter. This counter operates in a manner identical to the Total Level 1 Accept Counter, with the additional constraint that it only counts those Level 1 Accepts which occurred while the TEM status was not Busy, or put another way, only those Level 1 Accepts which were actually transmitted by the TEM.

B.16 Busy Timer

Board address 28 hex is the VME read address for the Busy Timer. As described previously, the Busy Timer monitors the total real time that the TEM has a Busy status.

The DAQ Processor reads the Busy Timer to obtain the duration of the most recent Busy interval. The length of this interval is calculated by first reading the Busy Timer immediately prior to clearing the Busy, and then taking the difference between the read value and the preloaded value (either the default value of zero or the value written by the DAQ Processor through the Busy Timer Preload Port). This difference gives the length of the Busy interval in slow clock cycles. The Busy Timer can count up to 65535 slow clock cycles. For an example slow clock rate of 2^{17} high-speed clocks, and a high-speed

clock rate of 60 MHz, this would mean that the Busy Timer could measure an interval of up to approximately 143 seconds before timing out.

As stated previously, the Busy Timer performs the twin tasks of measuring this real busy time, as well as generating a timeout interrupt if the busy interval exceeds the limit set in the Busy Timer Preload Port. See Sections 5.5 and B.8 for a further discussion of the operation of the Busy Timer.

B.17 FIFO Read Port

Board address 2B hex is the read address for the 8-bit FIFO Read Port. This port is used when testing the TEM to verify proper logical operation of the FIFO circuitry. It is designed to be used when the high-speed clock is stopped, and pulses on this clock are instead provided using the High-Speed Clock Single-Pulse strobe.

As actual writes and reads on the FIFO are tied to the high-speed clock cycles, accesses to this address do not actually cause new data to be read out of the FIFO. Rather, the FIFO Read Port is simply a buffer that gates the *data currently at the FIFO output* onto the bus so it can be read by the DAQ Processor.

To read adjacent locations in the FIFO memory, it is necessary to alternate accesses to the FIFO Read Port with High-Speed Clock Single-Pulse strobes.

B.18 Clock Phase Counter

Board address 2D hex is the read address for the 8-bit Clock Phase Counter. This TTL counter counts the number of high-speed clock cycles generated by the TEM, wrapping around every 256 cycles. This counter provides a modulo-256 sum of the number of clock cycles generated by the TEM over a particular interval, to be compared with similiar sums on other DAQ components, to verify the integrity of clock distribution.

The current contents of the counter are delivered to the DAQ Processor by a read access at the address above. In order to guarantee that a stable value is present on the counter during the read, the counter should only be read while the high-speed clock is inactive. Bit 5 of the Configuration Register enables the Phase Counter. While this bit is low, the counter is held in a reset state. When the bit is high, the counter automatically counts on each high-speed clock cycle.

C Cable Interconnections

This section describes various electrical and mechanical aspects of making cable interconnections to the TEM in the Test Beam environment, including termination schemes, pinouts for Clock and Control frontpanel I/O, and some special cabling configurations.

C.1 Cable Termination

As mentioned previously, the TEM has both ECL and TTL I/O interfaces on the front-panel. These interfaces have been designed to drive or be driven by a particular impedance of cable and termination scheme, depending on the logic family.

The card has a total of 3 TTL inputs and 2 TTL outputs which are connected using LEMO 00-type ("NIM") connectors. When driving the inputs it is recommended that 50-ohm coaxial cable, such as RG-58 or RG-174 be used, and that the cable be "back-terminated" at the driving end with a 50 ohm series resistor. The guidelines for interfacing to the TTL outputs are identical, taking note that integral 50-ohm output series resistors are included on the TEM.

The TEM also has approximately nine 10K ECL inputs and outputs each, which are received and driven as differential pairs. Motorola MC10H115 integrated circuits are used for the differential input receivers, and MC10H101 integrated circuits for the differential output drivers.

On the TEM, the differential inputs are terminated by connecting each end to -2V via a 50 ohm resistor. Additionally, the active-low side of each differential pair has a connection to board ground via a 1.62K ohm resistor. This additional connection results in an approximately 60 mV difference voltage across the inputs of the Motorola 10H115 ECL receiver when no driver is connected. This 60 mV difference at the receiver input is sufficient to guarantee that the receivers will not oscillate when the receiver is left open (with no driver). This scheme gives a net termination impedance across the pair of approximately 98.5 ohms, and for this reason, it is recommended that the ECL inputs to the TEM be driven with 100-ohm twisted-pair cable. As for the ECL outputs on the TEM, it is recommended that same this termination scheme be used by the circuitry which receives the TEM output.

In any case, note that the output drivers on the TEM are *not* biased on-board to any reference voltage (such as the commonly-used connection to -5V via 330 ohms), and therefore *must* be biased on the receiver in order to obtain proper DC logic levels. The above described scheme of terminating each end of the pair to -2V via 50 ohms does both jobs, terminating the cable at the proper impedance, as well as providing a DC bias current path for the output driver emitter-followers back on the TEM.

In the next section, which shows the ECL signal pinouts on the frontpanel connectors, a pin is assigned to each pair for a drain wire. This pin assignment allows for the used of individually-shielded, twisted-pair cables. Immediately behind the two ECL frontpanel connectors on the TEM are a series of jumper positions. These jumpers allow for optional connection of each drain wire to the board ground plane on a per drain wire basis. The purpose of these jumpers is to allow for maximum flexibility in the management of ground paths and possible ground loops in the uncertain grounding environment of the many possible Test Beam configurations. TEMs are shipped with all jumper connections made with soldered AWG 20 wire.

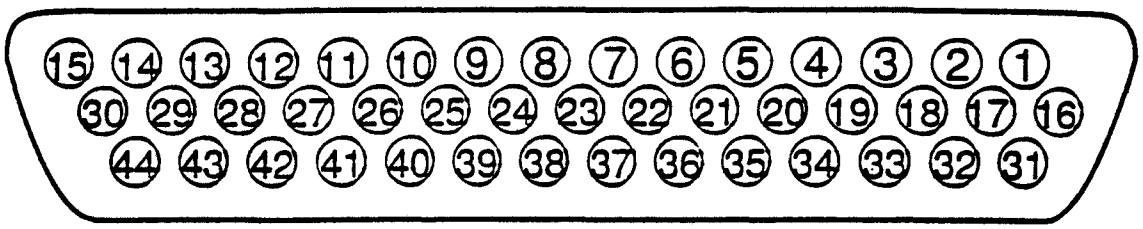

Figure 8: 44-pin High-Density Connector Pinout

C.2 Clock and Control I/O Pinouts

Figure 8 shows the basic pinout on the connector used for the frontpanel Clock and Control Inputs and Outputs. This connector is a female receptacle, with shell dimensions indentical to those of the standard, 25-pin subminiature-D connector. This high-density, 44-pin version is made by at least two manufacturers, specifically AMP and Amphenol. On the TEM, we use an AMP version of the connector, part #1-748482-5. A similiar part from Amphenol has part #17BH-044-S-AM-2-10.

Table 9 gives the pin assignments for the Clock and Control Input connector. Note that all inputs are differential ECL pairs, and that a drain wire pin is assigned to each pair. Also note that some pins are marked as "Reserved". This status applies to pins which are assigned an incompatible signal definition on the Clock and Control output connector. By taking advantage of the relative abundance of pins on the 44-pin connectors, which allow for the mapping of signals incompatible between the two connectors to separate pins, a single Trigger Control Cable type can be fabricated to connect to either the Clock and Control Input or Output at the TEM. Finally, of special note is the signal group "PGMCOUT...." This signal has been allocated for future expansion on connects to the Pattern Generation Module mentioned previously in this document.

Table 10 gives the pin assignments for the Clock and Control Output connector. Like the input connector, all signals are differential pairs, with a drain wire pin assigned to each pair. previously in this document. Note that the Trigger Control output data pin assignements correspond exactly to those on the input connector, while the PGMCOUT assignments are deleted, and the output clock moved. The output clock is assigned different pins than the input clock in order to avoid an accidental and invalid feedback loop for the clock in the data loopback configuration, described below.

Table 11 shows the resulting pin definitions for a single Trigger Control Cable type, which is produced by combining the pin definitions for the input and output connectors above.

Table 9: Clock and Control Input Pin Assignments

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	L1A IN+	16	Spare	31	Spare
2	L1A IN-	17	L1A IN drain	32	L2A IN+
3	L2R IN+	18	L2A IN drain	33	L2A IN-
4	L2R IN-	19	L2R IN drain	34	L1SYNC IN+
5	L1RST IN+	20	L1SYNC IN drain	35	L1SYNC IN-
6	L1RST IN-	21	L1RST IN drain	36	BC0 IN+
7	EBTT IN+	22	BC0 IN drain	37	BC0 IN-
8	EBTT IN-	23	EBTT IN drain	38	CSTOP IN+
9	Spare	24	CSTOP IN drain	39	CSTOP IN-
10	Spare	25	Spare	40	Spare
11	PGMCOUT+	26	Spare	41	Spare
12	PGMCOUT-	27	PGMCOUT drain	42	Reserved
13	CLK IN+	28	Reserved	43	Reserved
14	CLK IN-	29	CLK IN drain	44	Spare
15	Spare	30	Spare		

Table 10: Clock and Control Output Pin Assignments

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	L1A OUT+	16	Spare	31	Spare
2	L1A OUT-	17	L1A OUT drain	32	L2A OUT+
3	L2R OUT+	18	L2A OUT drain	33	L2A OUT-
4	L2R OUT-	19	L2R OUT drain	34	L1SYNC OUT+
5	L1RST OUT+	20	L1SYNC OUT drain	35	L1SYNC OUT-
6	L1RST OUT-	21	L1RST OUT drain	36	BC0 OUT+
7	EBTT OUT+	22	BC0 OUT drain	37	BC0 OUT-
8	EBTT OUT-	23	EBTT OUT drain	38	CSTOP OUT+
9	Spare	24	CSTOP OUT drain	39	CSTOP OUT-
10	Spare	25	Spare	40	Spare
11	Reserved	26	Spare	41	Spare
12	Reserved	27	PGMCOUT drain	42	CLK OUT+
13	Reserved	28	CLK OUT drain	43	CLK OUT-
14	Reserved	29	Reserved	44	Spare
15	Spare	30	Spare		

Table 11: Single Clock and Control Cable Type Pin Assignments

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	L1A I/O+	16	Spare	31	Spare
2	L1A I/O-	17	L1A I/O drain	32	L2A I/O+
3	L2R I/O+	18	L2A I/O drain	33	L2A I/O-
4	L2R I/O-	19	L2R I/O drain	34	L1SYNC I/O+
5	L1RST I/O+	20	L1SYNC I/O drain	35	L1SYNC I/O-
6	L1RST I/O-	21	L1RST I/O drain	36	BC0 I/O+
7	EBTT I/O+	22	BC0 I/O drain	37	BC0 I/O-
8	EBTT I/O-	23	EBTT I/O drain	38	CSTOP I/O+
9	Spare	24	CSTOP I/O drain	39	CSTOP I/O-
10	Spare	25	Spare	40	Spare
11	PGMCOUT+	26	Spare	41	Spare
12	PGMCOUT-	27	PGMCOUT drain	42	CLK OUT+
13	CLK IN+	28	CLK OUT drain	43	CLK OUT-
14	CLK IN-	29	CLK IN drain	44	Spare
15	Spare	30	Spare		

C.3 Cable Suggestions

In this section, some cable types are given which should be generally suitable for use with the TEM.

For the 50-ohm TTL cable connections, standard RG-58 or RG-174 cable is perfectly suitable.

For the Clock and Control Cable, individually-shielded, 100 ohm twisted-pair cable is available from manufacturers such as Belden and Carol. Specifically, both of these manufacturers make a cable which has 11 total pairs in an overall PVC jacket, and which easily gives good performance in lengths up to 10 meters, with 100 ohms nominal impedance, 0.78c velocity of propagation, and 12.5 pF/ft nominal capacitance. The Carol number for this cable is C0915, while the Belden number is 9733.

C.4 Special Cabling Configurations

In this section, two special cabling configurations for the TEM will be described. Specifically, they are a Clock and Control loopback connection on a single TEM, and a Clock and Control "master/slave" connection from the Clock and Control output of one TEM to the input of a second. These configurations are primarly intended for testing and initial checkout of TEMs, but a description of them may be of interest to the general user of the TEM as well.

The loopback connection allows Trigger Control output data from the TEM to be immediately fed back into the input on the next high-speed clock cycle. A length of Trigger Control Cable between 2 and 6 feet in length, connected between the two frontpanel connectors, will make the loop. These length parameters are specified in order to keep the loopback data within the proper timing window with respect to the on-board high-speed TEM clock. Note that the input and output clocks have different pin assignements on the cable. This is to prevent the accidental closing of an invalid loopback path when the data loopback connection is made.

The second special cabling configuration is from the Clock and Control output of one TEM to the input of another. In this configuration, both clock and data would be driven from the first TEM, the "master," to the second the "slave." Given the different pin definitions for the input and output clocks on the headers, this requires a modification to the standard Clock and Control cable format. In order to drive the clock out from pins 42 and 43 and receive it on pins 13 and 14 of the cable, it is necessary to "cross over" these signals on the cable. Thus, at each end of the cable, the pair that connected to pins 42 and 43 at the *far end* should be connected to pins 13 and 14 of the *local end.*