

SDC
SOLENOIDAL DETECTOR NOTES

**3D-FLOW PROCESSOR PRELIMINARY
TECHNICAL SPECIFICATIONS**

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Abstract

In High Energy Physics experiments it is necessary to identify objects (particles such as electrons, jets, muons, *etc.*) with programmable algorithms at 60 million frames-per-second. In commercial applications, on the other hand, objects are typically recognized at 30–120 frames-per-second. The above requirements have led to the design of a special “3D-Flow” processor that, together with a special pipelined parallel-processing architecture, allows a sustained input data rate of 60 million frames-per-second. The 3D-Flow is a data flow processor that can be used in one-, two-, or three-dimensional array for high-speed signal-processing applications such as identification of objects on a matrix in a programmable form. This report describes the main characteristics of the 3D-Flow cell processor and the interconnection scheme of several 3D-Flow cells in a chip.

1.0 3D-FLOW PROCESSOR ARCHITECTURE DESCRIPTION

The architecture of the 3D-Flow processor cell is shown in Figure 1.

The core of the cell of the 3D-Flow processor is identical for the entire 3D-Flow array processor system. In the 3D-Flow cells assembled as a pipelined system within a chip, the first 3D-Flow cell of the pipeline that is receiving data from the calorimeter must have a look-up table to correct and linearize the received data.

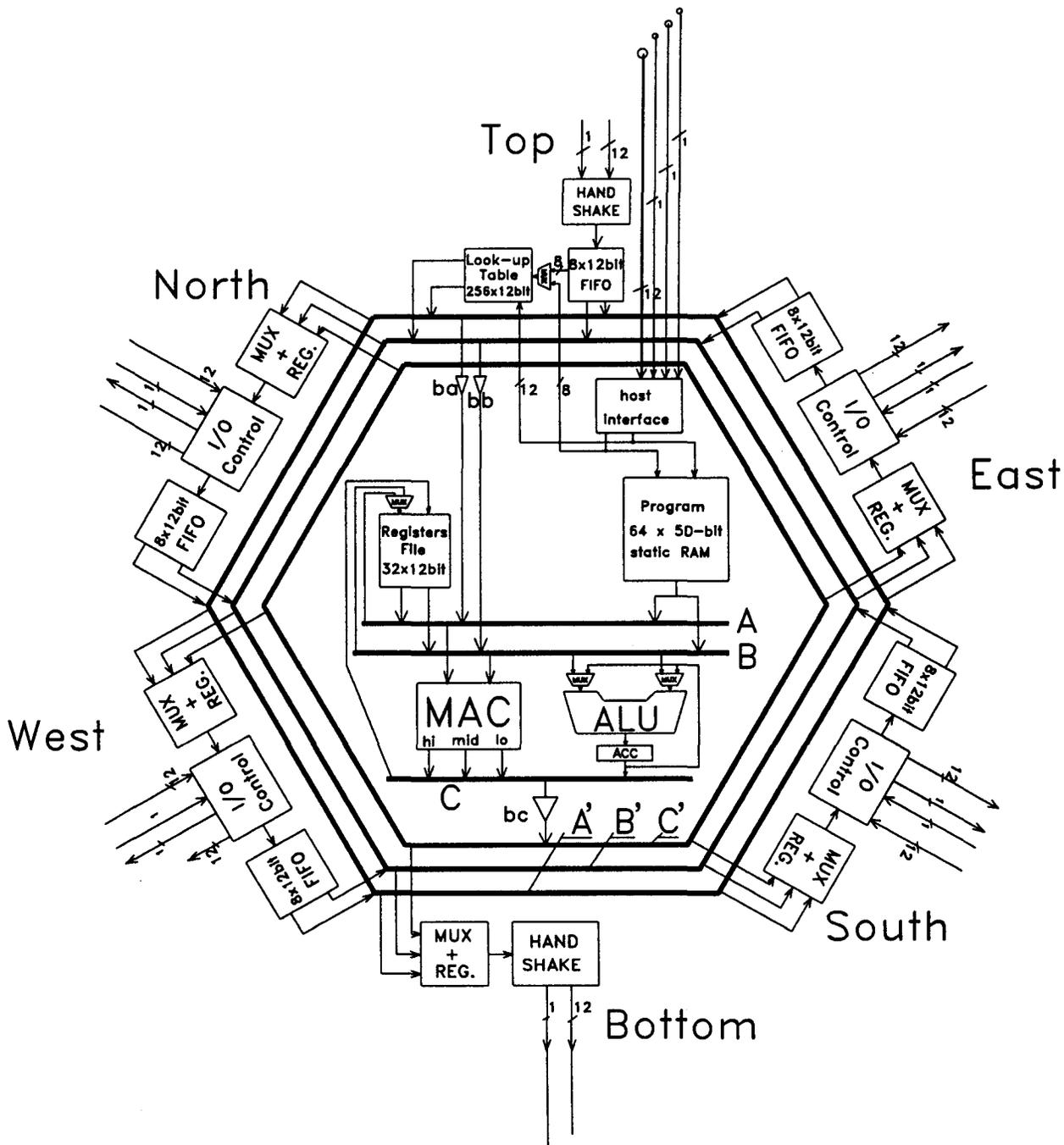


Figure 1. 3D-Flow Cell Architecture.

The 3D-Flow operates on a data-driven principle. Program execution is controlled by the presence of the data at the five ports (North, East, West, South, and Top) according to the instruction being executed.

A clock running at a frequency of 60 (or 120) MHz synchronizes the operation of the cells. Each cell consists of program memory, a multiply accumulate (MAC) unit; an arithmetic and logic unit (ALU); a register file; an interface to the Universal Asynchronous Receiver and Transmitter (UART), which is used to load programs, debug, and monitor during execution; and program storage surrounded by a system of three-ring buses. An example of the use of the 3D-Flow in a parallel processing system for calorimeter triggers is described in Reference 1.

North, East, West, and South ports are bidirectional on separate lines for input and output; the Top port is input only, and the Bottom port is output only.

The top input port has an 8×12-bit FIFO buffer to derandomize data from external devices (such as a calorimeter). The North, East, West, and South ports have a 4×12-bit FIFO that, together with an asynchronous handshake control, allows the exchange of data between adjacent 3D-Flow cells at the minimum time.

At each clock, a three-ring bus system allows input of data from a maximum of two ports and output to a maximum of five ports. During the same cycle, results from the internal units (ALU, *etc.*) may be sent through the internal ring bus to a maximum of five ports. Each 3D-Flow cell may execute different 64-line code programs. When it is issued an input instruction from a 3D-Flow cell and the data is not present, that particular 3D-Flow cell waits until the data becomes available before resuming execution.

The program is loaded into each individual cell program RAM through the UART serial I/O. During execution time, the UART interface should have access to a status register of each 3D-Flow cell in order to allow the monitoring of the activity of the program execution. The UART should also allow single-step execution of programs at each 3D-Flow cell during debugging of the system.

2.0 3D-FLOW INSTRUCTIONS

The instruction cycle is determined by the clock speed, which may be 16.6 or 8.3 ns. All instructions should be executed in one cycle.

The instruction set is reduced and consists of the following operations: addition; subtraction; accumulation; shift; logical; conditional and unconditional branch; a no operation; a single cycle comparison of one register with eight registers, with a 1-bit result of each of the eight comparisons in the accumulator; and a port I/O as described previously. A programmable timer at each input port linked to the trigger by the watchdog signal should allow generation of error flow.

It should be possible to implement the code listed in Tables 22 and 29 of Reference 1, including the multiple operations per cycle (all operations listed in a single line code).

3.0 CONSTANTS LOADED IN THE LOOK-UP TABLE OF THE FIRST STAGE

Figure 2 shows the layout of the 3D-Flow chip with four cells. Raw data coming from the calorimeter are corrected and linearized from 8-bit to 12-bit in the look-up table before flowing to one of the rings to a destination unit. As indicated in Figure 2, it should be possible to send the raw data from the calorimeter directly on the bus ring to the destination. Precalculated constants should be loaded into the look-up table at power on through the UART serial I/O interface.

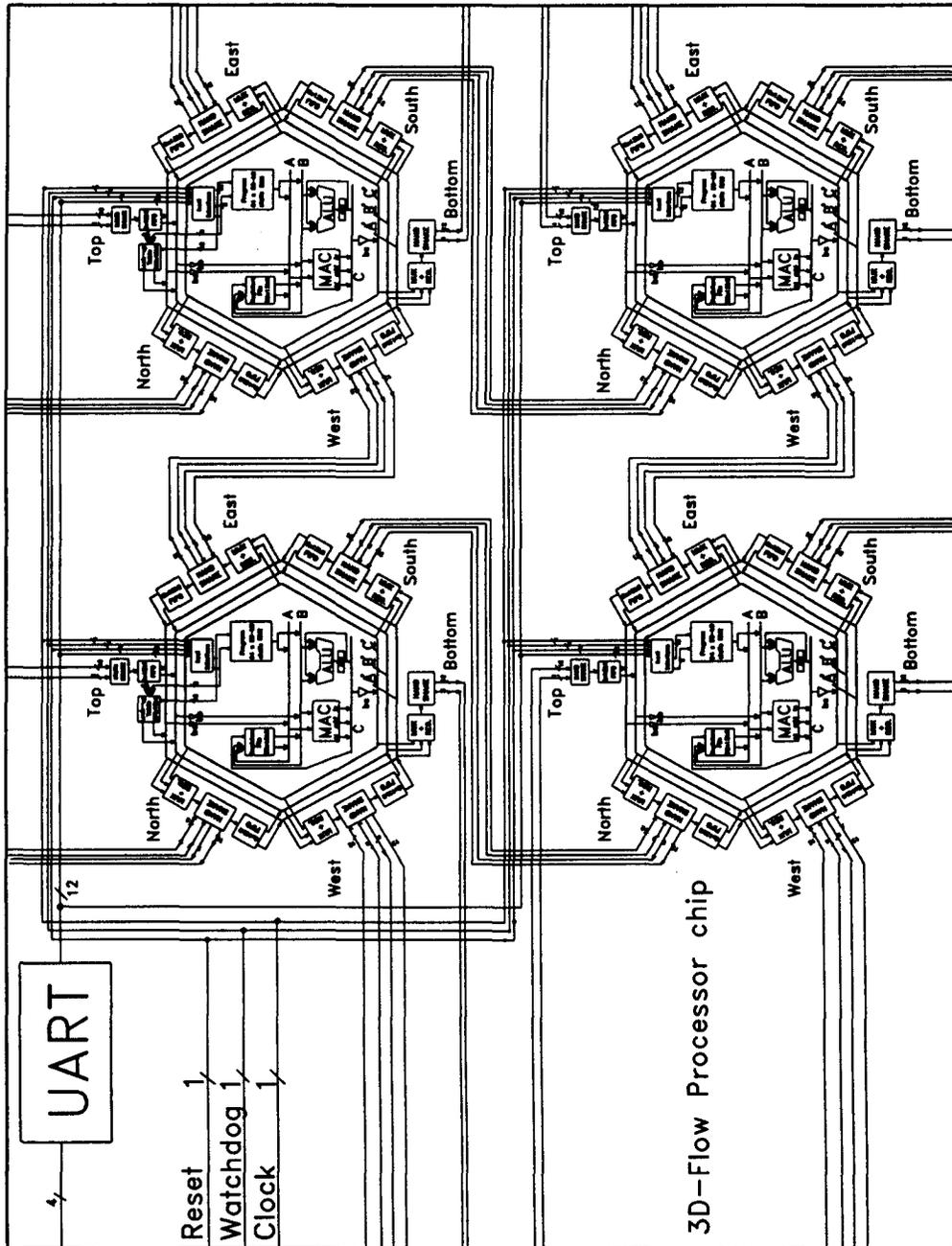


Figure 2. 3D-Flow Chip Assembly of 4 Cells.

4.0 CONCLUSIONS

With a processor running at 120 MHz, an algorithm for “em” + front-to-back could be implemented in eight stages (to sustain the rate of 16.6 ns), resulting in a total of 10,000 processors for the GEM experiment and 28,672 for the SDC. (For the “em” + front-to-back + isolation + jet-finding, the processor speed or the number of processors should be double.)

The flexibility of this solution can be demonstrated by the ease of programming a 3D-Flow cell. Any physicist can change the algorithms of the 3D-Flow by coding a simple program, consisting of fewer than 64 lines of operations, and by using an instruction set of only a few instructions. Because of this simplified instruction set, the effort required to learn to program the 3D-Flow is minimal.

Experience shows that trigger algorithm tuning usually begins after acquisition of a few full events. The possibility of a flexible, programmable system at an affordable cost (compared with cabled logic) makes exploring this solution beneficial not only to the GEM and SDC experiments but to other experiments as well.

REFERENCE

1. D. Crosetto and L. Love, "Fully Pipelined and Programmable Level 1 Trigger," SSCL-576, July 1992.