The ShowerMax Detector Front End & Read-out Electronics

Edited by Patrick Le Dû for the Saclay Group - August 1992

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1. Introduction

This document presents the R & D work done by the Saclay group to develop a compact and cost effective front end electronics optimized for the SDC ShowerMax Detector (SMD). The idea adopted is to combine in a realistic manner the detector performance with the less-risky technology choices.

2. Requirements and constraints

The Shower Maximum Detector [Ref. 1] provides fine segmentation within the EM calorimeter. The 8 Phi-strips and 8 Eta-strips per tower are used to measure the position and the shape of the EM showers. In besides data being readout through the DAQ system, information is also generated for use by the level 1 and level 2 triggers. This electronics will also be used to instrument the Massless Gap at the front of the barrel calorimeter.

2.1. Channel count

The SMD electronics process 47,104 electronics channels (94,208 after upgrade) plus 10,368 Massless Gap electronic channels.

2.2. Dynamic range

The SMD should measure EM showers from transverse energies from 10 Gev to about 1 Tev. The factors determining the required dynamic ranges of the electronics are listed in the table below. this range just fits onto a 12 bit ADC, with a minimal separation between the pedestal and the useful signal .

Consideration	Factor
Energy range 10 Gev to 1 Tev	33
Downward fluctuation at 10 Gev	2
Upward fluctuation at 1 Tev	1.5
Shaping and center of gravity	10
Pedestal separation	4
Total range	4000

2.3. Input signal

A 10 Gev electron will leave on the average an 80 mip-equivalent signal in each of the SMD layers. The largest signal in a single strip will be about 40 mips. The least count will correspond to half a mip. It is expected to get 2 photoelectrons per mip with 4 mm thick scintillator or one photoelectron per count. It is not clear what is the real shape of the input signal which depend of the shifting fiber characteristics. First observations of these signals show a rise time of 10 ns and a fall time of 20 ns. The present study is based of a more optimistic 5 ns rise time and 10 ns fall time.

2.4. Level 1 trigger

At level 1, it is difficult, complex and too costly to use the full granularity of the SMD to match the tracker detectors. In addition barrel cracks in the calorimeter mechanics could provide some inefficiency at the first stage of the event selection. However, some limited information at the level 1 can be useful for certain category of calorimeter trigger particularly to reject photo tube sparks or unexpected electronics noise. The logical OR of 16 discriminated signals above a programmable threshold would be adequate.

2.5. Level 2 trigger

At level 2 more information is available from the tracker (including the inner silicon tracker) and from the SMD. Photon conversion can be found using the silicon tracker. Fake electron can be eliminated by using the momentum-energy match and the track-shower match using the full SMD granularity. Monte-Carlo results shows that the SMD can be useful to reduce the level 2 rate.
The fine segmentation of the ShowerMax detector allows to refine the granularity of the electromagnetic shower detector and give the basic level 2 grid of 1024 phi x 30 eta. Theoretically, an electromagnetic shower hits more than 3 adjacent strips. A simple logic should be able to give the position of strip "centroid" including a rough estimate of the energy deposition. However, cracks in the detector and possible inefficiencies' dues to radiation damage should be incorporated and may complicate this simple hardware-oriented algorithm . Utilization of the second "eta" layer of strips should minimize these effects.
This requirement imposes to access and extract full or part of the digitized information directly after each level 1 trigger. Extraction of this information for the level 2 trigger is not yet clearly understood. In the worse case 8 bit of data per strip should be send out.

2.6. Photo detectors

2.6.1. Multichannel Photomultiplier (MCPMT)

MCPMT have traditionally been used as the photo detector element of the baseline choice (TDR) for the SMD, in particular the Philips XP1722 64-channels. This device is based on an established and reliable technology with a gain of 5 x 10**5 . On the other hand, the quantum efficiency is low (7-10%), its linearity, uniformity and cross-talk (~ 5%) characteristics are marginal. Improved devices with lower cross-talk and with green-enhanced photo cathodes are being developed with Philips and Hamamatsu. From the technical point of view they may be a viable solution for the system, however the cost of ~ 4000 $ or more per tube is a major disadvantage., and one of the main reasons why an alternative is being sought.

2.6.2. Avalanche Photo Diode (APD)

Avalanche Photo diode (APD) arrays operated in a linear mode are potential candidates to replace MCPMTs. They offer a much simpler mechanical design, large quantum efficiency (60-80%) and dynamic range, good uniformity and low cross-talk. The drawbacks are lower gain (100-500) and temperature stability requirements. Therefore low-noise, moderate gain, fast preamplifiers are required. However the low cost of 600-800 $ per array makes them very attractive.
Commercial APD's produced by EG&G (Vaudreuil, Canada) gave very encouraging results in the beam test of the SMD prototype. Recent API 3x3 array pixel looks also very promising.

2.6.3. Hybrid APD-PMT

APD-PMT would use an APD array mounted in a proximity-focused image tube with a conventional or extended photo cathode. The gain is high because the photoelectrons are accelerated in a strong electric field before impinging on the APD. The APD array under development at Advanced Photonix (API) is being incorporated in this hybrid device by Litton Electron Device. This new device should have in principle good qualities such as improved quantum efficiency, low cross talk and large dynamic range. However a full study of their behavior in beam tests including lifetime and rate performance has to be done.

The table below give a summary of technical characteristics [Ref. 2] of the 3 different photo detector types. Taking into account the uncertainty about the final choice of the photo detector technology, the SMD front end electronics will be designed to be compatible as much as possible with any one of the final decision.

	MCPMT	APD	APD-PMT	IDEAL
• Gain	~ 5. 10**5	100-500	10**5-10**6	≥ 10**5
• Quantum efficiency @ 550 nm	7-12 %	60-80 %	up to 35%?	100%
• Linearity	10**3	≥ 10**7	≥ 10**5	≥ 10**4
• Noise , dark current	5 nA	~ 10 nA	~ 10 nA	≤ 5 nA
• Crosstalk	3-5 %	≤ 1%	low?	0
• Uniformity	5:1	10-20%	good	≤ 10%
• Temperature stabilization	No	Yes	?	No
• Magnetic sensitivity	70 Gauss?	No	No?	No
• HV or Vbias	≤ 2 kV	200V-2kV	10 kV	≤ 2 kV
• Radiation hard	OK	under test ?	?	Yes
• Status	Established	Tested for SMD	Prototype	-
• Availability	64 Ch.	9 to 32 pixels		-
• Technical complexity	None	Preampli	?	None
• Main concern	Quantum Efficiency	Signal/Noise	Lifetime ?	-
• Cost per channel	≥ 50 $	~ 10$	16 $	≤ 20 $
• Manufacturer	Philips,Hamamatsu	EGG,API,Hughes?	Litton & API	-

2.7. Calibration aspects

Additional features, including a possible current integration capability for source calibration and a variable- amplitude charge injection test signal, should be provided. The technical specification for the design that depend on the photo detector choice is not yet completely studied.

3. Read Out scheme

3.1. Conceptual choice

Two schemes are being developed for the calorimeter read-out [Ref. 3]. If that choice of technology will be the same for the calorimeter and the ShowerMax, this is a short comparison of the two concepts.

For the SMD a dynamic range of 12 bit is required as opposed to 17 bits for the calorimeter and the outputs from the photo detector are arranged in groups of 64 channels.

3.1.1.Analog scheme

The analog read-out is a conventional approach (charge integrator, shaper, pipeline and A/D converter) using well-understood techniques and cost relatively predictable. Large systems have already been built and are operational.

The disadvantages of an analog system are essentially timing considerations that are however not critical for the SMD:

- a signal shaping of 5 ns rise-time and 10 ns fall-time is assumed. Due to the long decay times of the fluors in the WLS fiber, some part of the signal will be lost after the shaper. This lost is estimated to be approximately 20%.
- some time response variations due to the signal jitters with respect to the SSC reference clock.
- transport of analog signals between the different parts of the processing chain should be optimized to be insentitive as much as possible to the signal degradation, environmemt noise and crosstalk.

3.1.2.Digital scheme

In this implementation, every SMD channel is connected to a single ASIC that performs all functionality's from the digitization to the storage directly after the photo detector. This ASIC consists of a current splitter, a gated integrator array, a 5 bit Flash ADC and associated data storage. This modern and elegant scheme is simple in its principle and looks very attractive.

Advantages of the digital system are:

- all the signal (if less than 16 ns) is collected.
- once digitized the system is effectively noise immune.

It seems difficult at the early stage of the study to estimate the possible unknown or hidden complexity and drawbacks of integrating all the functionality's including crosstalk, analog-digital coupling, chip to chip performance spread (current splitter...), etc... .
Coupling this one channel ASIC to a 64 channels photodetector array can be a delicate and complex problem to keep the crosstalk low. Advantage of an "all in one" ASIC becomes a disadvantage when the photodetector choice and parameters are not yet optimized. The "variable gain" function may also add some complexity.
In addition, the "system issue" in a realistic environment (noise, temperature behavior...) has not yet been demonstrated in any large system.
Cost is another major issue, which however should be comparable to the analog one, even if there are four times more ASICs.

Taking into account these considerations, the choice made was to develop a readout chain around the conservative SCA analog pipeline developed at LBL. As it is emphasized above, the SMD read-out requirements are much less severe than that of the calorimeters in dynamic range and timing accuracy and our concern is to design a low cost read-out that will meet our requirement's first. Effort in the design and optimization in the cost and high level of packaging of each element is then the key issue of our study.

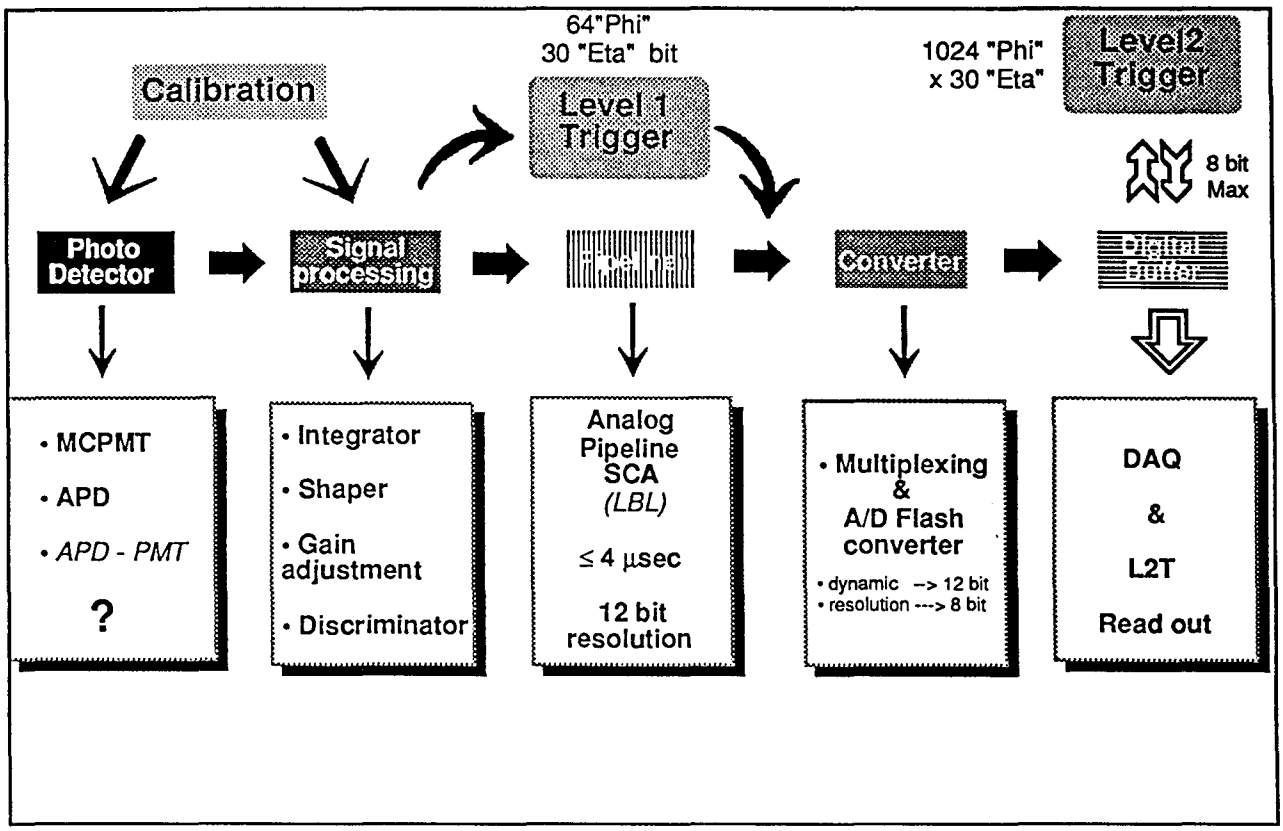
3.2. Read out components

The output signal from each photo detector channel will be coupled to an analog signal processing chain consisting of a charge integrator, a shaper, a gain adjustment amplifier and discriminator, the analog pipeline and finally an A/D converter. This scheme is basically the same as the calorimeter analog readout chain.

However there are two substantial differences:

- The photo detector is an array of 64 pixels with only one common HV (MCPMT) or Vbias (APD). Therefore some gain adjustment between individual channels is required in the readout chain. In addition a relatively high degree of integration should be done. Since the SCA is already packaged into 16 channels ASIC, it is foreseen to keep this basic number for all other functions

- Digitization should be achieved directly after a level 1 trigger to be able to extract information toward the level 2 trigger. Independent of this specific requirement, this classical 2 step's approach is certainly the more flexible in a long term view in case of trigger upgrade for example and should be strongly considered for the calorimeter scheme itself. At that level some multiplexing can be introduced in order to use only one fast digitizer per 16 channels.

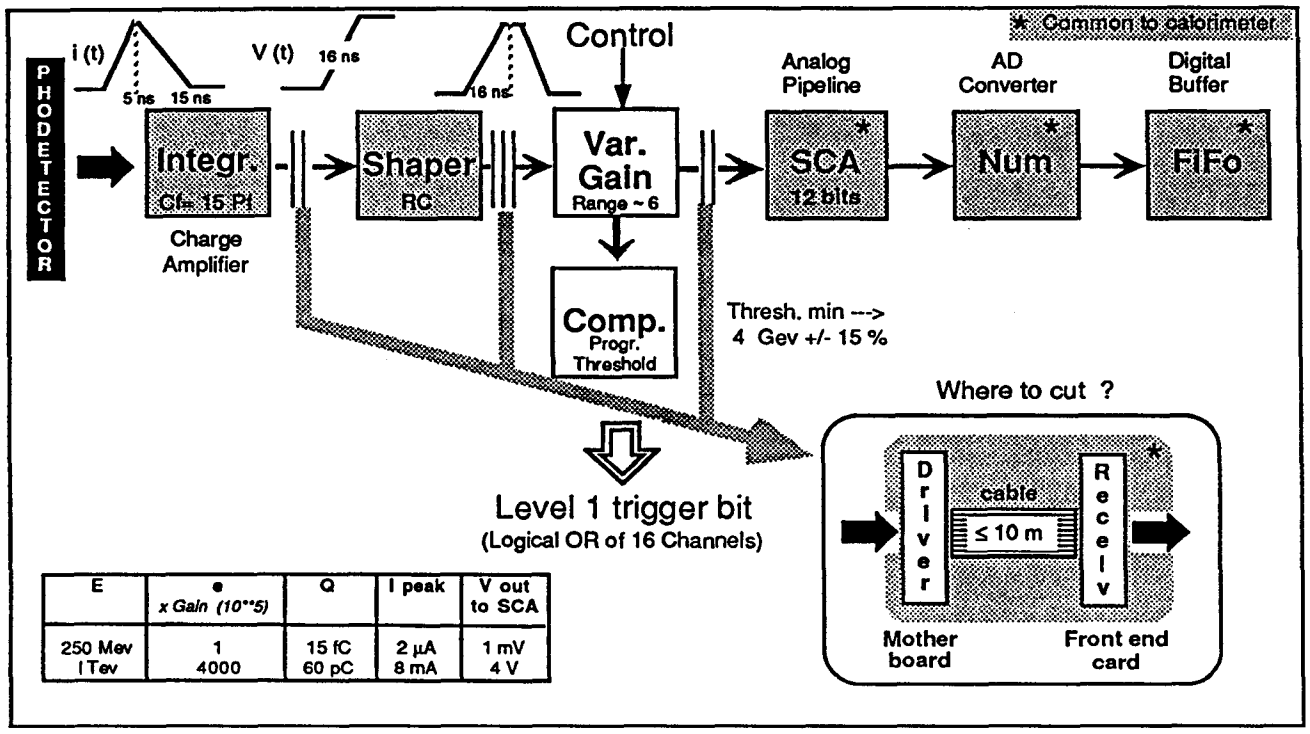


3.3.Functionalities

The signal processing part has been optimized for the Philips MCPMT photo detector. Modification for the other photo detectors will be discussed in the paragraph 5.2 (New developments).

The required characteristics are:

- Charge integrator with a rise time less than 5 ns.
- Occupancy ≤ 5%
- Peaking time less than 16 ns.
- Gain and sensitivity optimized for a MCPMT output signal between 15 fC and 60 pC. (Dynamic range 4000 compatible with the range 1mV- 4 V of the SCA)
- Gain adjustment from 3 to 16 (range ~ 6) between channels.
- Programmable discriminator threshold with a range of a factor 10 and a logical "OR" of the outputs for use in the Level 1 trigger with a minimum threshold of 4 Gev +/- 15%.



E	• x Gain (10**5)	Q	I peak	V out to SCA
250 Mev 1 Tev	1 4000	15 fC 60 pC	2 µA 8 mA	1 mV 4 V

This readout chain will be topologically implemented in two physical parts connected through few meters of cable (5 to 10 meters):

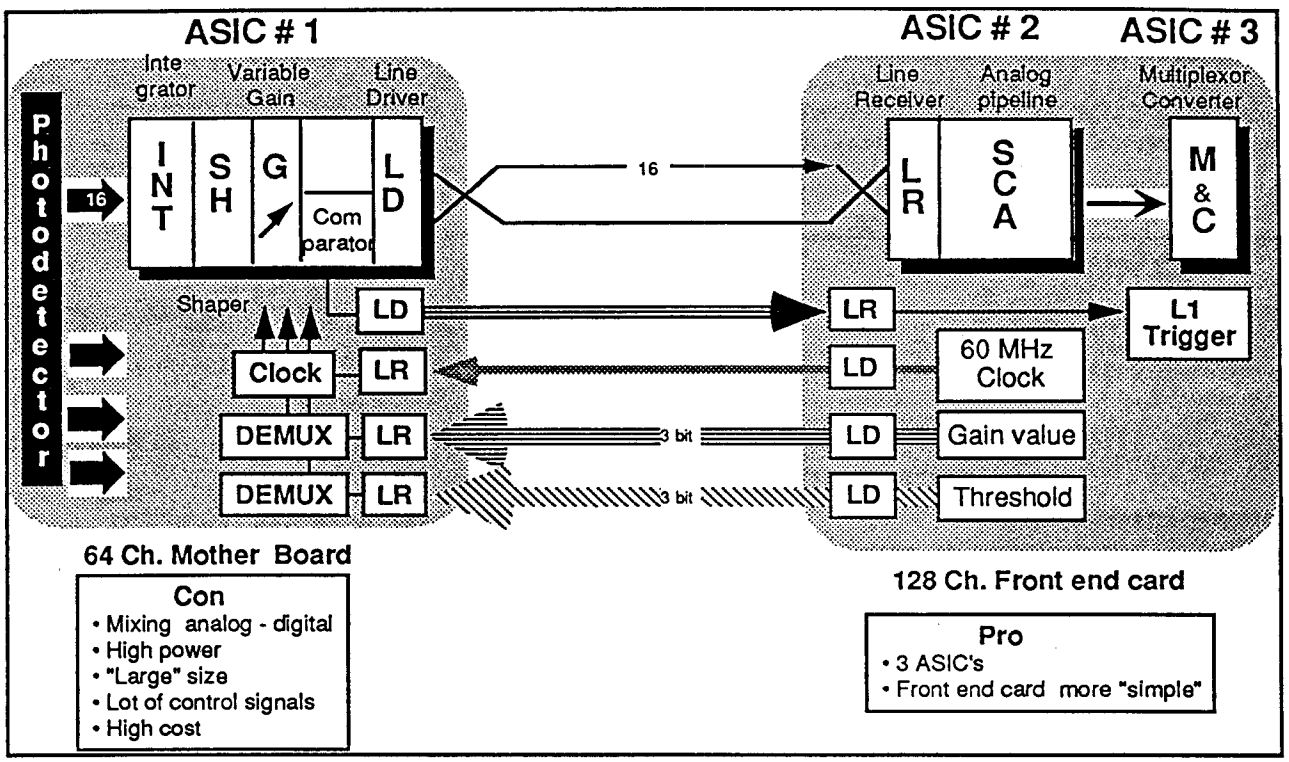
- The "Mother Board" directly connected to the photo detector in the back side of the calorimeter .
- The "Front End Card" installed in the "Front End readout Crate".

The choice of the function to be implemented in each board and the consequences for the inter-connection system (line driver and receiver, signal levels, clock distribution ...etc) is discussed in the next section.

3.4. Choice of configuration

3.4.1.Technical Report (TDR) configuration

In the TDR [Ref. 1] all the signal processing functions are grouped in the same ASIC. In addition to the complexity of designing such ASIC and its associated "Mother Board", there is a mixing between the analog (comparator input) and digital (60 MHz clock) signal processing functions. To avoid coupling between these 2 functions, it should be safe to separate them. There are also a large number of connections and fast signal distribution that is always very costly.

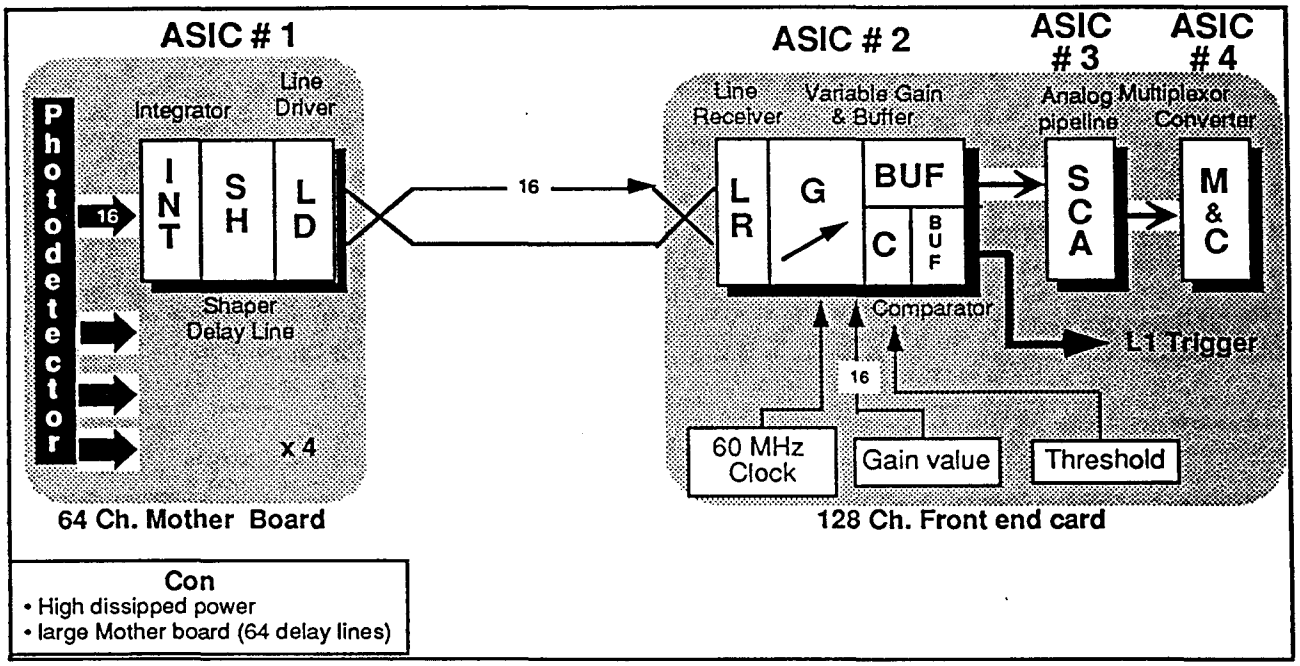


3.4.2.Calorimeter type configuration

In this scheme, the pure analog function is separated from the rest of the signal processing. The shaping is made using individual delay lines like for the calorimeter. These delay lines are placed just after the charge integrator. This is certainly the best technical and clean solution with many advantages like:

- Recovery time << RC filter circuit.
- Timing reproducibility (dependent on the signal shape)
  ---> insensitivity to the jitters between the physical PMT output signal and the SCA clock, minimization of the "walk" at the comparator input.
- No signal attenuation.

This solution that is certainly very desirable for the calorimeter is not compatible with a low cost, low power consumption and a high integration.



3.4.3.New proposed configuration

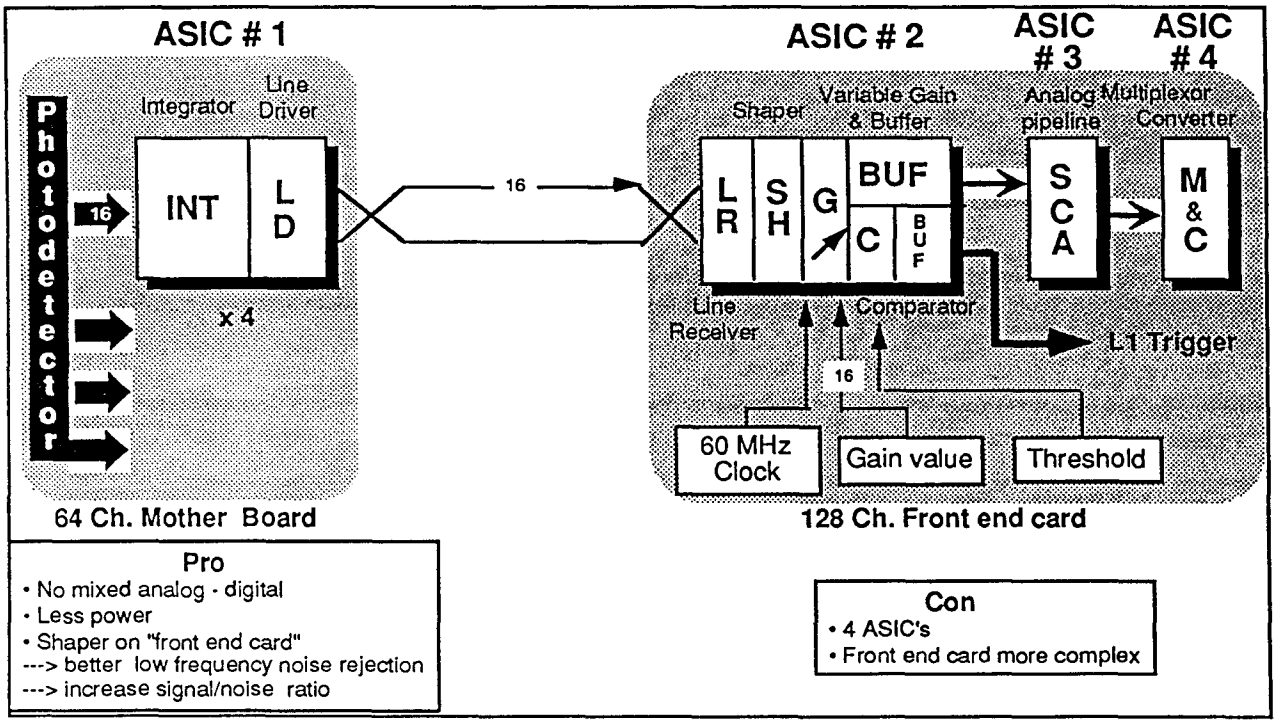
This scheme is a modified version of the previous one that isolates in a nice way the pure "high sensitivity" analog part from the rest of the digital functionality's. The shaping part is made using RC circuit implemented in the front end card which looks a good compromise in our case. This is also the best configuration to minimize noise problems.

In addition, there is a one important advantage keeping the system very flexible:

- The "Mother Board" contains only the part that is specific to a particular device (MCPMT or APD) without changing the rest of the readout chain. This board drive signals across a cable to the next stage.
- The "Front End Card" located in a crate filled with other MD or calorimeter card is approximately "general" where common calorimeter and SMD functions can be implemented.

In this solution the readout is achieved using four different 16 channel ASICs. These are:

- The CHARGE INTEGRATOR (ASIC# 1).
- The SHAPER , gain adjustment & level 1 signal extraction (ASIC # 2).
- The ANALOG PIPELINE (ASIC # 3).
- The MULTIPLEXING ADC (ASIC # 4).



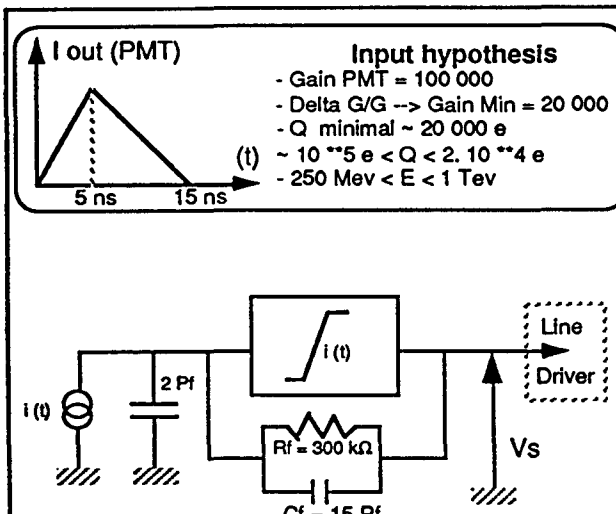
3.5. Integrated circuits

Three ASICs are currently developed by the Saclay Microelectronics Group.

3.5.1.Charge Integrator

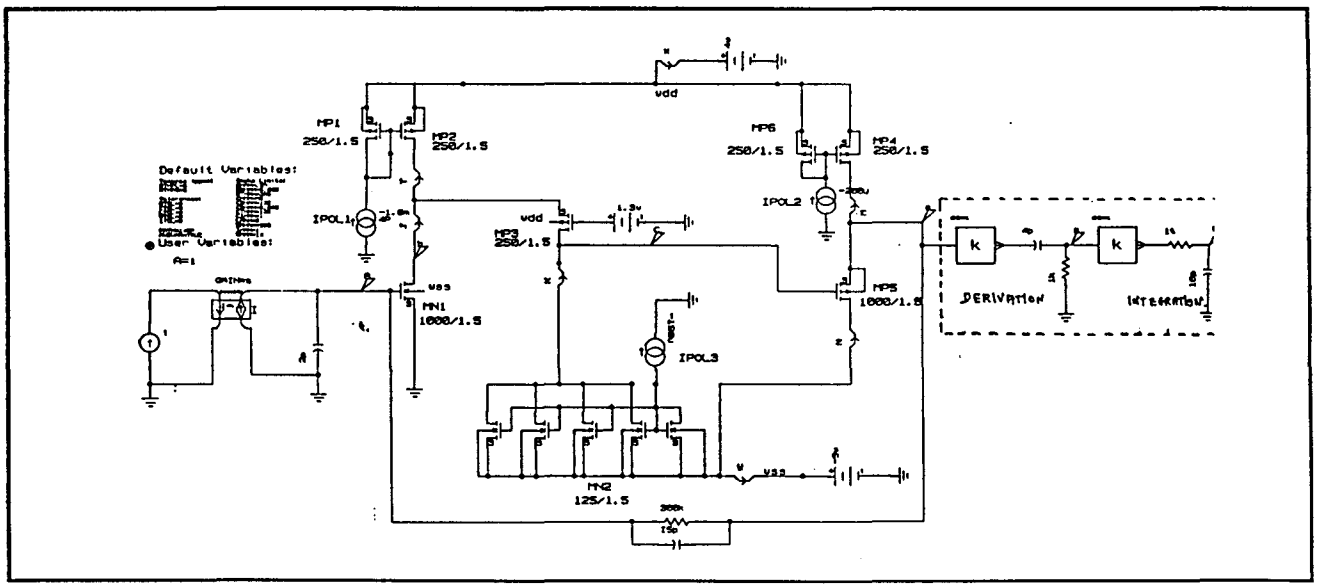
The first stage of the signal processing has been optimized for the Philips MAPMT XP1722 with a positive anode current output and a typical capacitance of 2pF, dark current of 4 nA, rise time of 5 ns, transit time spread of 2 ns, and maximum current amplifacation of 10**5.

The characteristics of this CMOS ASIC are presented in the following diagram:
(The line driver function will not be implemented in the first version of the chip. This is a problem which is common for both calorimeter and SMD) .



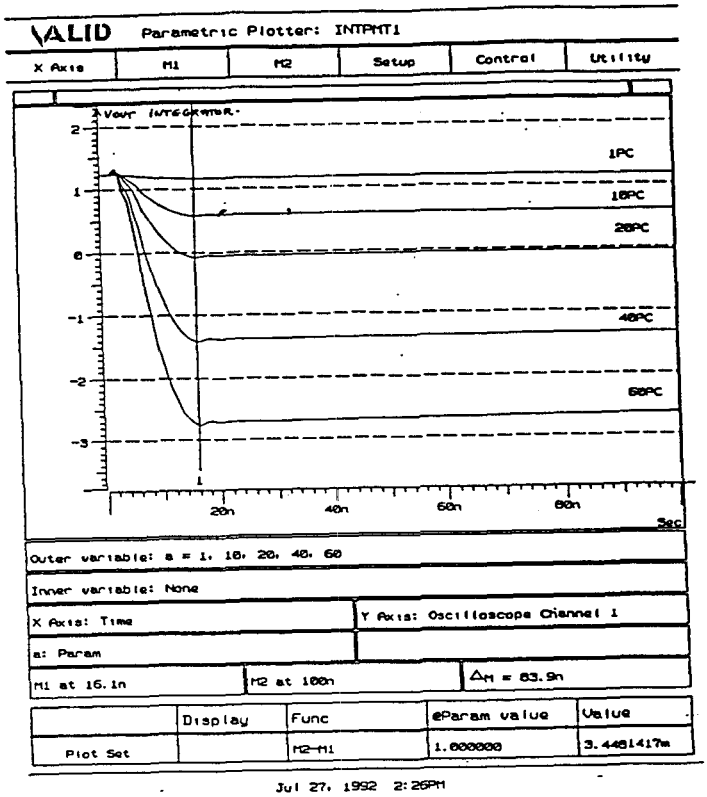
• Function	Integrator
• Technology	1.5 µm CMOS
• Number of channels/ ASIC	16
• Bandwidth	60 MHz
• Dynamic range	4000
• Time constant (300 KΩ*15pF)	4.5 µsec
• Transfer function	67 mV/pC
• Settling time (= 5%)	< 16 ns
• Power dissipation/Ch.	25 mW
• Input noise (expected ENC)	2000 e rms
• Output range	1mV- 4 V
• Non-linearity	< 1%
• Crosstalk (expected)	< 2%
• Output impedance	5Ω

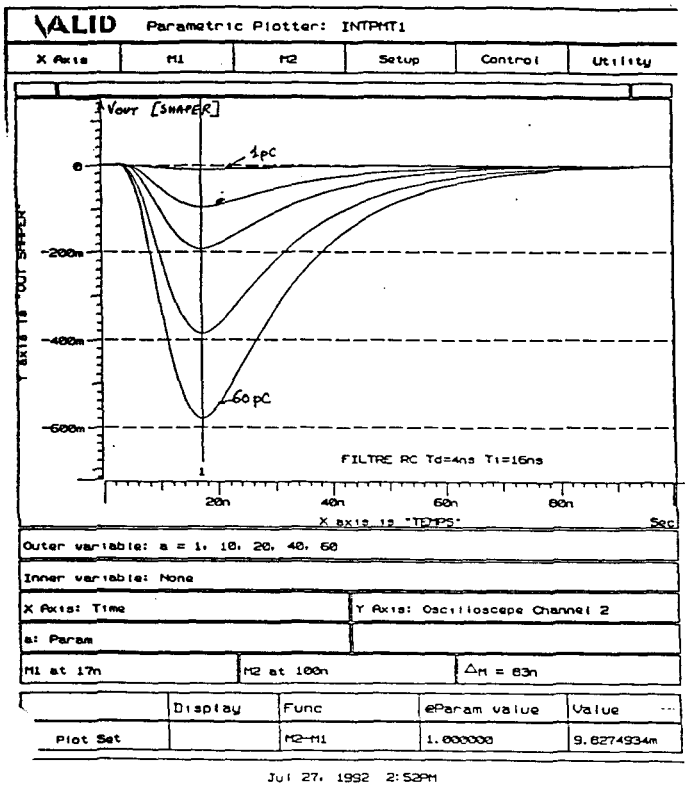
The circuit schematic for the charge sensitive preamplifier is presented below. The topology is a classical cascode preamplifier and source follower with a low output impedance and low power dissipation.

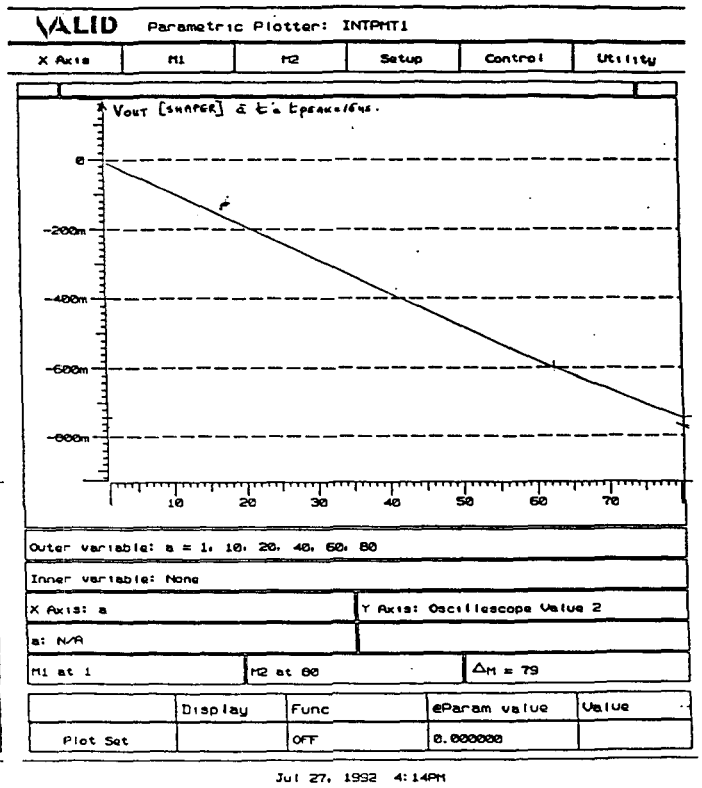


Three simulations are shown, the photomultiplier being modeled by a 2pF capacitor in parallel with the current source.

- Normalized time response of the integrator to a simulated charge stimulus of 10 to 60 pC.
- Time response after an RC filter.
- Linearity of the output of the RC shaper. The 80 pC value is there to show the non-linearity part.



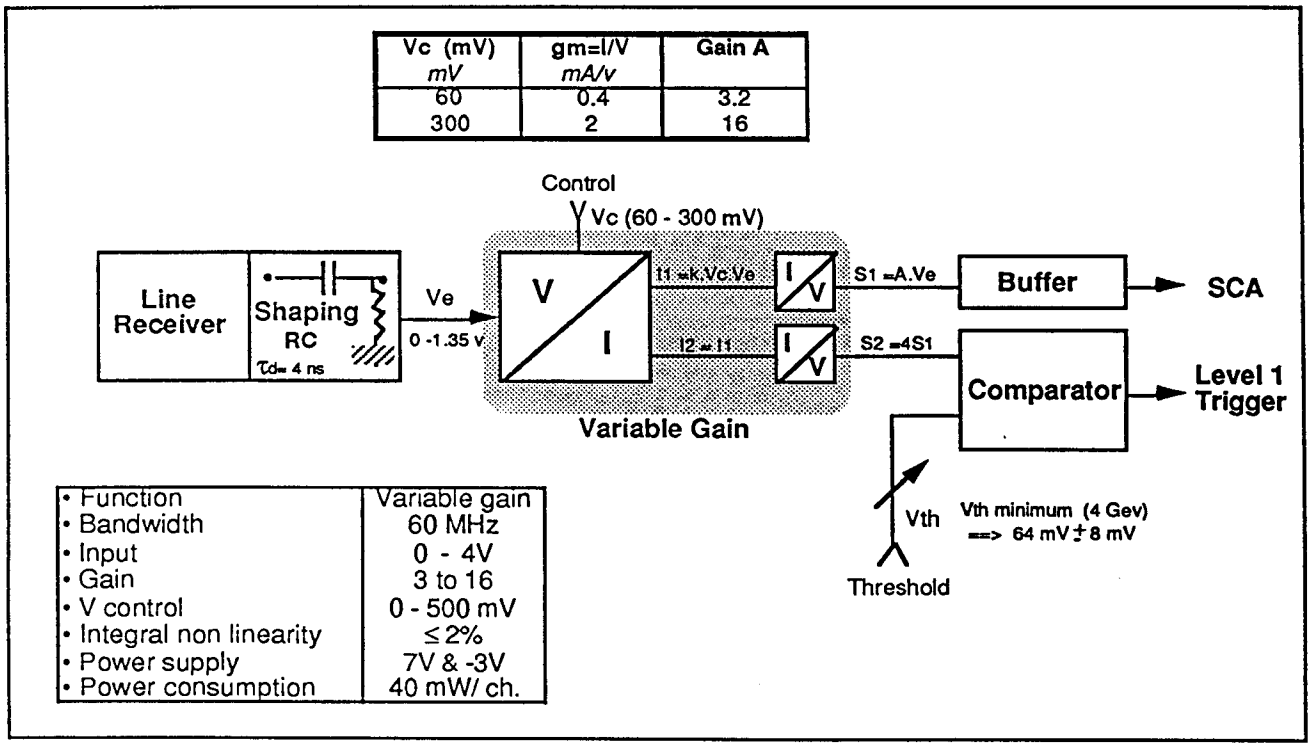




3.5.2. Shaper - Gain adjustment and Comparator

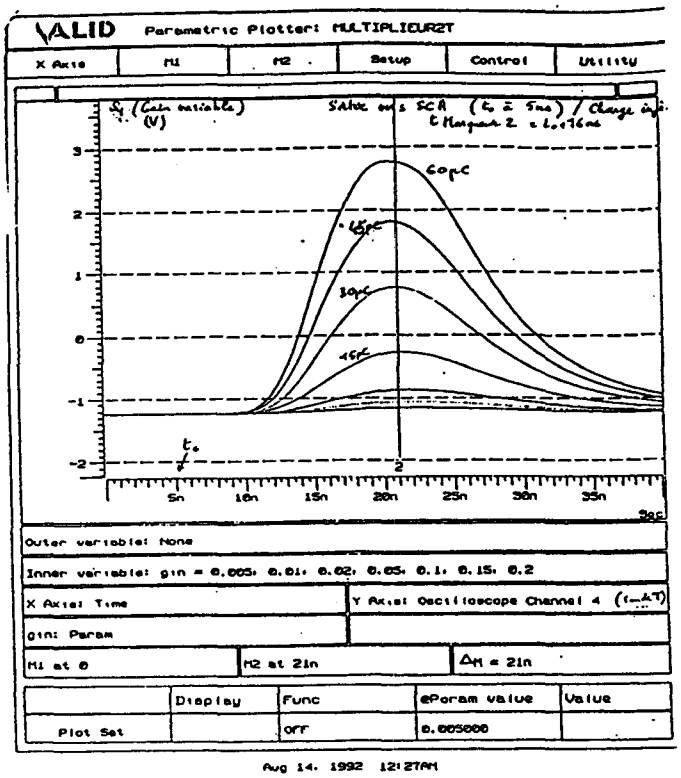
The functions of this 16 channel CMOS ASIC 1.5 µm technology (MIETEC) are the following:

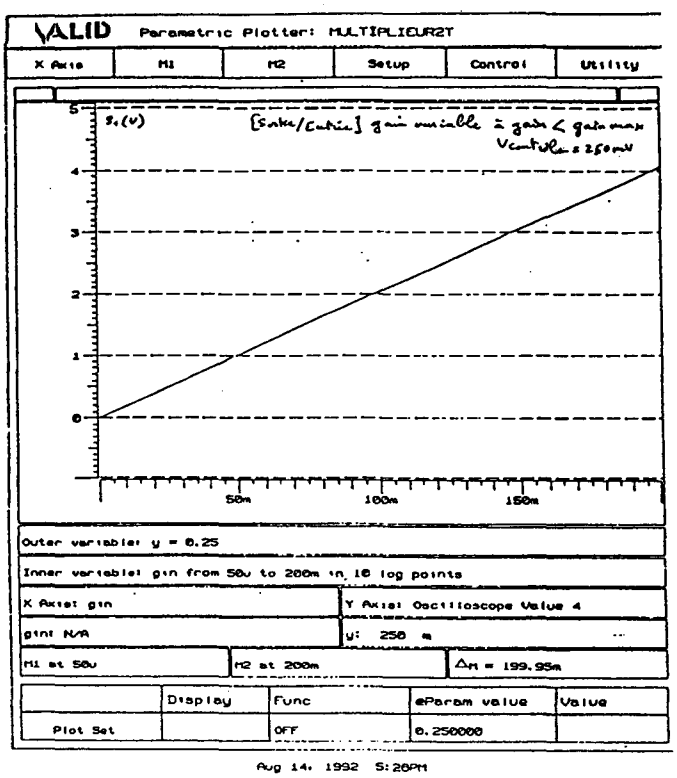
- Line receiver (not implemented in the first version).
- Shaper. Filtering is provided by a simple RC circuit with a time constant of 4 ns. The choice of this cheap and low consumption technique instead of a delay line was explained in the previous section. The single main advantage of the delay line being to be insensitive to the signal amplitude and then to minimize timing fluctuation in the recovery time. But this is not a strong argument if we compare to the 1% expected occupancy. There is an attenuation of the signal by a factor of 3 (range 0-1.35v) which should be recovered by and additional gain adjustment.
- Variable gain with both separate adjustment for the SCA input buffer and the level 1 comparator.
- Fast comparator. The basic requirements of this function are:
  - Bandwidth 60 MHz
  - Sample during one SSC period (16 ns).
  - Insensitive to the "walk".
  - Threshold range ~ 50 (6 bit)
  - threshold dispersion ~ 15%

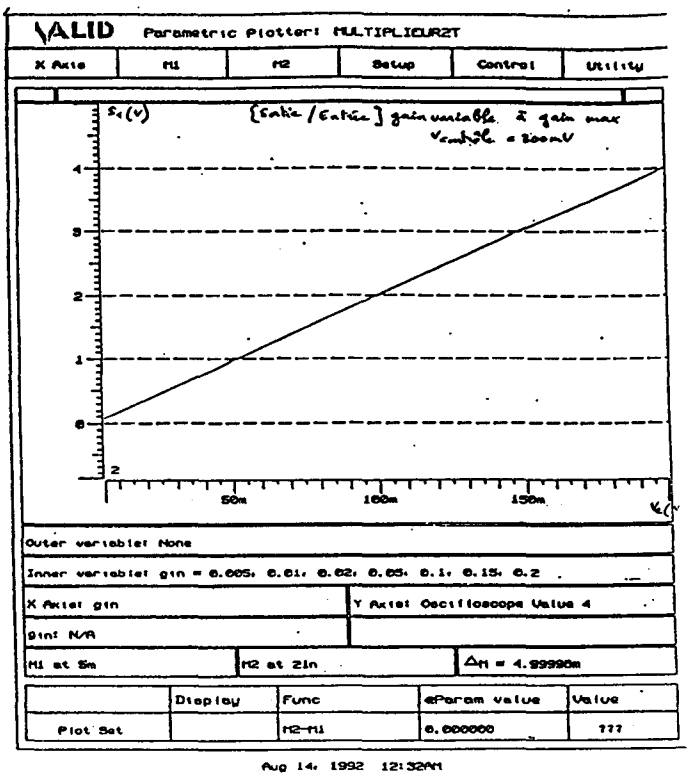


The simulation of the "variable gain "function shows:

- the output signal to the SCA at maximum gain for different input coming from the integrator.
- tranfer curves for 2 values (intermediate and maximum) of the "varable gain" , inter

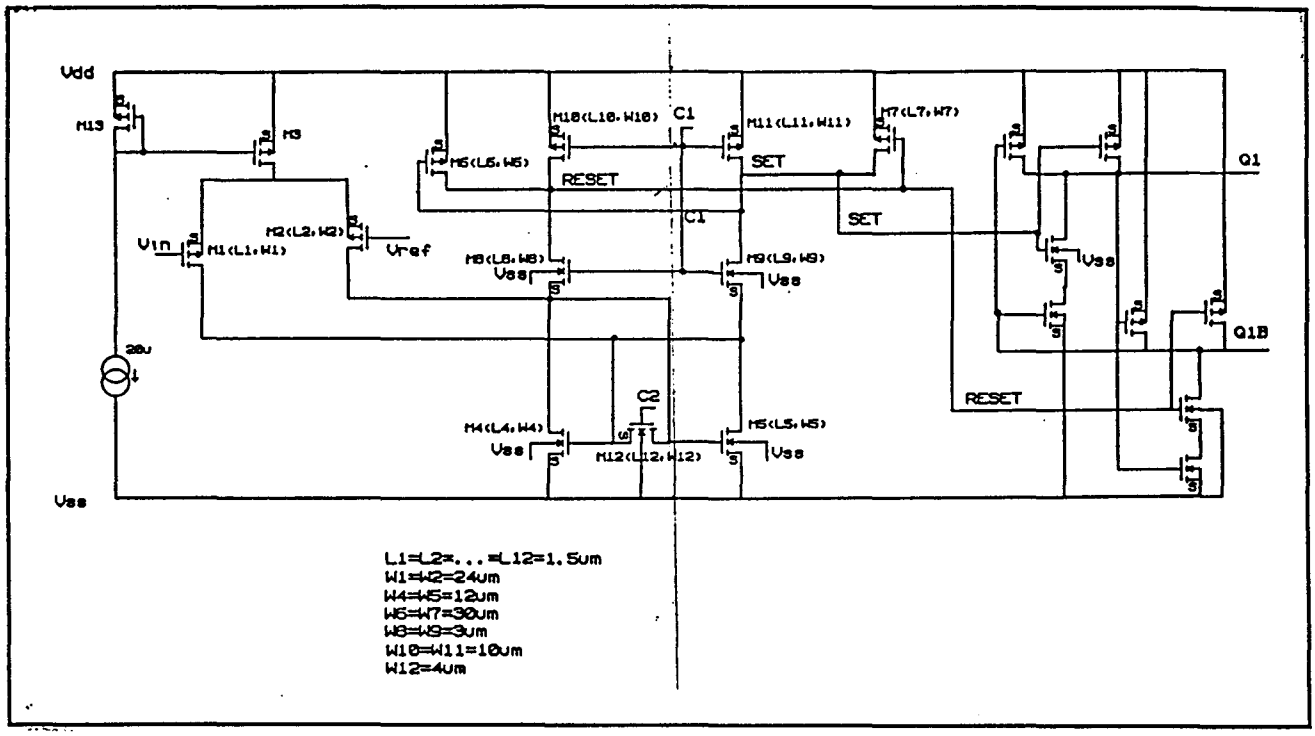




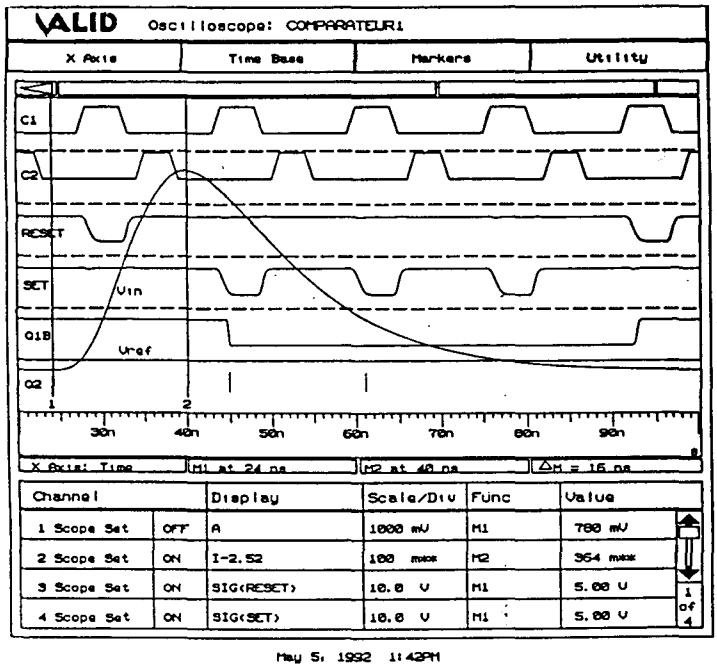


The comparator for the level 1 trigger is the most sensitive function and may be the most technically interesting. The minimum threshold has been set to 4 Gev with 15% accuracy. This is a realistic compromise between the physics requirement and the technical difficulty. The solution investigated is based on the Ref. [4] .

This is a very low power, very small area and high speed (>60 MHz) CMOS comparator. This circuit performs directly by mean of regeneration without extra offset cancellation circuit. The low offset voltage of the comparator is obtained through carrying out the comparison in two steps of regeneration with the use of two non overlapping clocks.



In order to be as much as possible independent of the "walk" and timing difference between channels, the sampling is made around the peaking time. To be sure that the comparator output is "true" only during one SSC period, the "time over threshold" is chosen greater than 16 ns. Reducing the threshold dispersion should involve a careful knowledge and optimization of the "offset" problem.



3.5.3. Analog pipeline

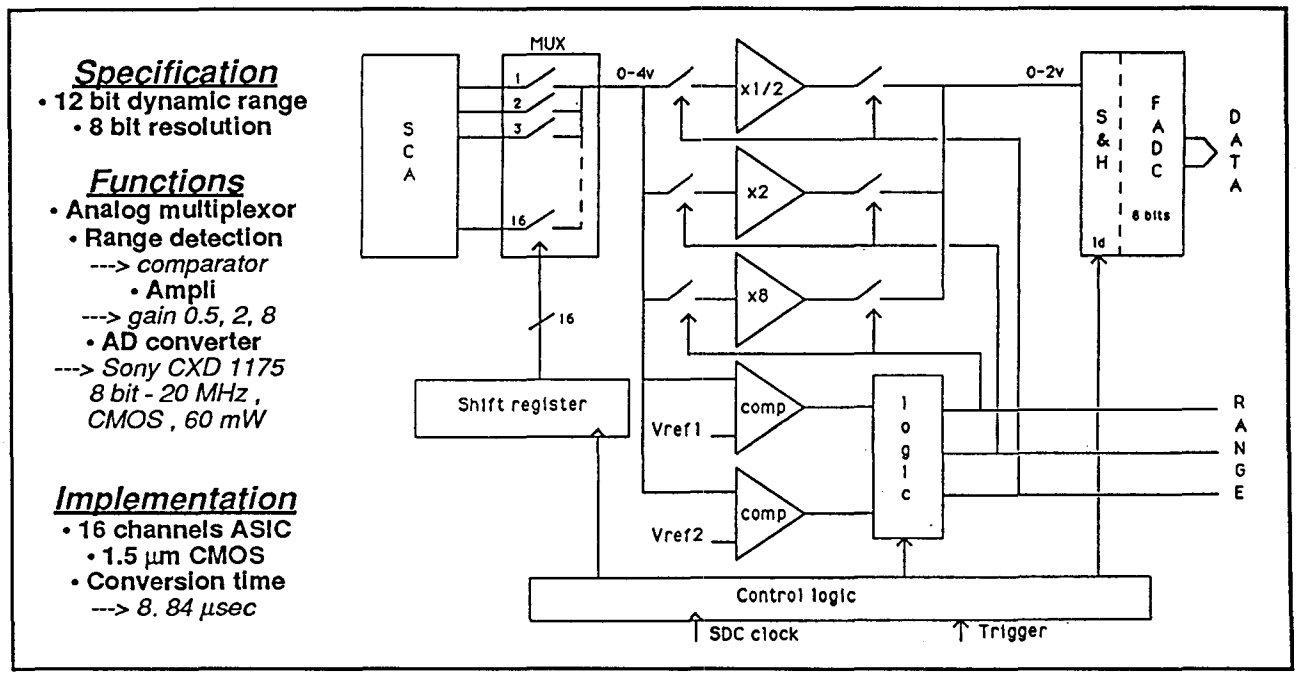
Switched Capacitor Arrays (SCA) will be used to store the analog data until digitization. The SCA is a 4K addressable sample-and-hold analog memory, divided into 16 channels of 256 cells each as described in Ref.[3]. It samples and stores, in parallel, 16 analog inputs at the SSC crossing rate of 60 MHz. It can simultaneously store a 12-bit analog sample in one cell and retrieve another such analog sample from a different cell. The analog memory is controlled by a specialized integrated circuit, the Address List Processor (ALP), which manipulates stored data addresses (pointers) through a series of bookeeping lists.

This ASIC is currently available at LBL. Improved version less sensitive to the environment with ECL logic inputs and 3 separate power lines is under development.

3.5.4. Digitization

The Level 1 accepts occur in average every 10 µsec. This time interval is sufficiently long to allow the use of a single ADC. The 16 channels are multiplexed to a common analog bus connected to a single inexpensive 8-bit 20 MHz Flash digital converter (FADC). In order to preserve the full 12 bit dynamic range, a range detection system composed of two comparators and four amplifiers (gain 0.5, 2, 4, 8) is placed in the front of the FADC. The result of the conversion is a 12-bit number, which is stored in a digital FIFO buffer. An alternative solution will be to use a commercial monolithic or hybrid 12-bit 20 MHz Flash converter when it becomes available at reasonable price.

The diagram of the principle of this converter is presented below.



The functions integrated in this CMOS ASIC 1.5 µm technology (ES2) are the following:

- 16 channels analog multiplexor.
- 2 comparators for the range detection.
- 4 amplifiers to adapt the 0-4 volts SCA output to the 0-2 volts input range of the commercial digital converter.
- Control logic.

Simulation results using a scheme that combines comparators with hysteresis and operational amplifiers give a conversion time of 400 ns per channel and a power consumption of 40 mW for the analog part. The surface of the chip will be 15 mm2. The total conversion time is expected to be 8.84 µsec.

The converter selected is a CMOS 8-bit 20 MHz SONY CXD1175. The power consumption is 60 mW and its cost is ~ 6 $ in large quantity (3000).

• Function	Digitizer with range selection
• Mode	Multiplexor + FADC
• Input range	0 - 4V
• Output range	12 bits
• Resolution	8 bits
• LSB (0 ---> 62.5 Gev)	0.25 Gev/cx
• LSB (62.5 ---> 250 Gev)	1 Gev/cx
• LSB (250 ---> 1 Tev)	4 Gev/cx
• Technology	1.5 µm CMOS
• Number of channels	16
• Conversion time / Ch.	400 ns
• Total conversion time (16 Ch. + SCA settling time)	9 µsec.
• Cross talk (expected)	< 2%
• Power dissipation	30 mW
• Cost per chip (15 mm2)	10$

3.6. Cables & Drivers

Connection between the 2 parts (ASIC # 1 ---> ASIC # 2) should be achieved through a multiconductor cable (which is not the case for the single PMT calorimeter scheme). Among the possible solutions as "coaxial" or "twisted pairs" cables, the DIFFERENTIAL TWP approach has some advantages:

- TWP are known to be cheaper than coaxial cables, not only the material itself but also for the connector part.
- TWP have small crosstalk and have good behavior in a noisy environment.
- Differential TWP are very well adapted to signal polarity change, since the final decision for the ASIC # 1 is not yet done.

However differential TWP needs more complex line driver/receiver design with also more power consumption. Integration of such function in the CMOS ASIC # 1 (Line driver) and ASIC # 2 (Line receiver) will be studied in collaboration with the calorimeter group.

4. System aspects

This section describes how the overall system could be organized. This is a draft version. More details will be available in the next few weeks.

4.1. Mother board

Each front end analog module will handle 64 channels from a single photo detector MCPMT or APD array (32 phi strips and 32 eta strips). This corresponds to one 0.1 x 0.1 hadron tower cell. The design depends strongly of the choice of the photo detector (MCPMT vs. APD). There will be 784 of such boards mounted around the back of the calorimeter. This is a simple printed circuit board of 5 x 15 cm2 maximum size with no particular technical difficulty that will contain the 4 ASIC # 1 and the necessary control and calibration logic. A prototype of such board will be done in 93.

4.2. Front end card

Implementation of this card is strongly connected to the concept and the design of the Level 2 trigger and DAQ systems. In addition, the design of this card should be closed as much as possible to the calorimeter one. These elements are not yet very well understood today. The ideas presented here are personal inputs for later discussion in the trigger/DAQ group.

In a classical approach "a la VME" (Option 1-TDR), characteristics of this card could be the following:

- 9 U "Jumbo EURO" card with 3 rear connectors .
- a "Control bus" access which is typically today the VME bus (20 Mbytes per second) which can be replaced if there is the necessity by another commercial BUS (Futurebus)
- an "Extension bus" connector (like the VSB) which can be used for the connection to the level 2 trigger if the "control bus " bandwidth is not sufficient.
- a "Dedicated bus" access for synchronization signal distribution (Clock, Trigger Accept & Reject...).
- the I/O functions to the DAQ that contains the various "general purpose" interfaces to the "standard" Control bus (VME..), a DRAM , up to internal resources including a "local processor " kernel (a DSP or a RISC).
- one or more specific "piggy back" multilayer PC board containing:
  - the analog/digital conversion chain (ASICs 2 + 3 + 4 + FADC).
  - the level 1 trigger logic including timing and clock synchronization.
  - the level 2 "extraction feature" logic.
- A card with 128 channels (4 x 16 channels chain) is a realistic goal .

This card was used to get a cost estimate of the "option 1" readout chain.

A more modern, versatile and attractive concept is under study to optimize the reliability and minimize the cost and maintenance and upgrade aspects without loosing any performance. This is based on 12 years "good and bad" experiences in LEP experiments where the maintenance cost and system upgrade were rarely considered! In this scheme, the "front end card" has the following characteristics:

- 9 U "Jumbo EURO dumb" card with no intelligence at all and no connection to any data bus.

- a simple "fiber channel" interface with "minimum" protocol, which is a point to point optical fiber link to "push" data to an external "data collector card" located in the surface control room.

- the minimum functionality's described above as "specific piggy-back board" for 128 channels.

The cost of such a card is obviously cheaper than the previous one since there is no interface and connector to any bus. It should be noticed also an important simplification in the specification for the Front End Crate which does not requires any "standard" bus. Distribution of Clock and Synchronization signals could be done in a very simple and cost effective manner. Power supply can be carried out using a simple dedicated back plane. "Local slow controls" can be done using either the "local back plane" or remotely through the fiber link.

This scheme was used to get a cost estimate of the "option 2" readout chain.

4.3. Level 2 trigger data extraction

Clearly, a dedicated data extraction feature is a very heavy and costly solution. Effort is underway to understand what is the best way to achieved the integration of the SMD in the Level 2 Trigger. It is also clear as presented in the next section that this technical problem depends strongly on the DAQ readout scheme.

4.4. Data Collection (DAQ)

4.4.1.Input parameters and Data throughput

The read out of the 47104 SMD channels is achieved using a modular tree structured organization from the front end "Mother Board" level to the "Data Collector" crate. The table below review the different physical components:

Component	Contains	Barrel	End Cap	Total
• Channels number	—	28672	18432	47104
• Mother board	64 Ch.	448	320	768
• Front End Board	128 Ch.	224	160	384
• Front End Crate	16 Cards	14	10	24
• Data Collector Board	1024 Ch.	28	20	48
• Data Collector Crate	≤ 14 Cards	2	2	4

Event size and data throughput at each level can be estimated using the following assumptions:

- 5% maximum occupancy.

- Sparsified data syse of 8 bytes per "cluster" (2 bytes address and 2 x 3 bytes data strips).

- Trigger rates : Level 1 = 100 KHz and level 2 = 1 KHz.

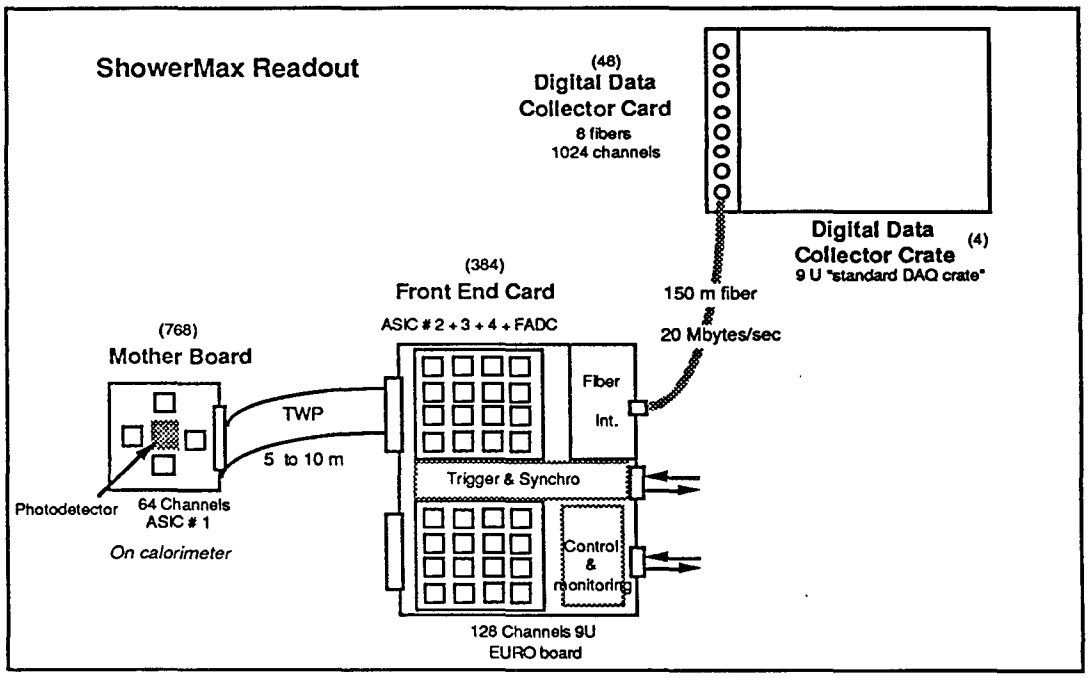
	Raw	Sparse
• Unit	Strip	Cluster
• Data size	12 bits	8 bytes
• Front End Card read-out	128 Ch.	6 clusters
• Event size @ the Front End Card (FEC) level	192 bytes	48 bytes
• Data throughput/ FEC @ level 1 trigger rate	19.2 Mbytes/sec	4.8 Mbytes/sec
• Event size @ Data Collector Card level	...	384 bytes
• Data througput / Data Collector Board @ Level 2 rate	...	384 Kbytes/sec
• Maximum Data Troughput / Data Collector Crate		5.3 Mbytes/sec
• Data Througput total SMD		20 Mbytes/sec
• SMD maximum event size		20 Kbytes

4.4.2.Front End read-out topology

In both options described in the section 4.2, the first step of the data collection is achieved by front end digitizer cards placed in each "Front End Crate". Each crate contains 16 front end cards. The full SMD DAQ readout is carried out using 24 crates. Then, the read out of the front end digitized data is carried out by "Data Collector Cards" placed in an external "Digital Read out Crate".

There are 2 topological arrangements for the front end readout:

- along the azimuth "phi" sector segmentation that fits perfectly the 32 physical "wedges".
- along "eta" slices. For example each one of the 24 crates can collect all the 1024 contiguous azimuth PHI and their associated ETA strips. The advantage is to minimize the complexity of the "feature extraction for the level 2 trigger data". Disadvantage is the increase of the cable length between the crate and the "Mother Boards". In addition this scheme introduces a difference in the data throughput between "end cap" and "barrel" readout crates.



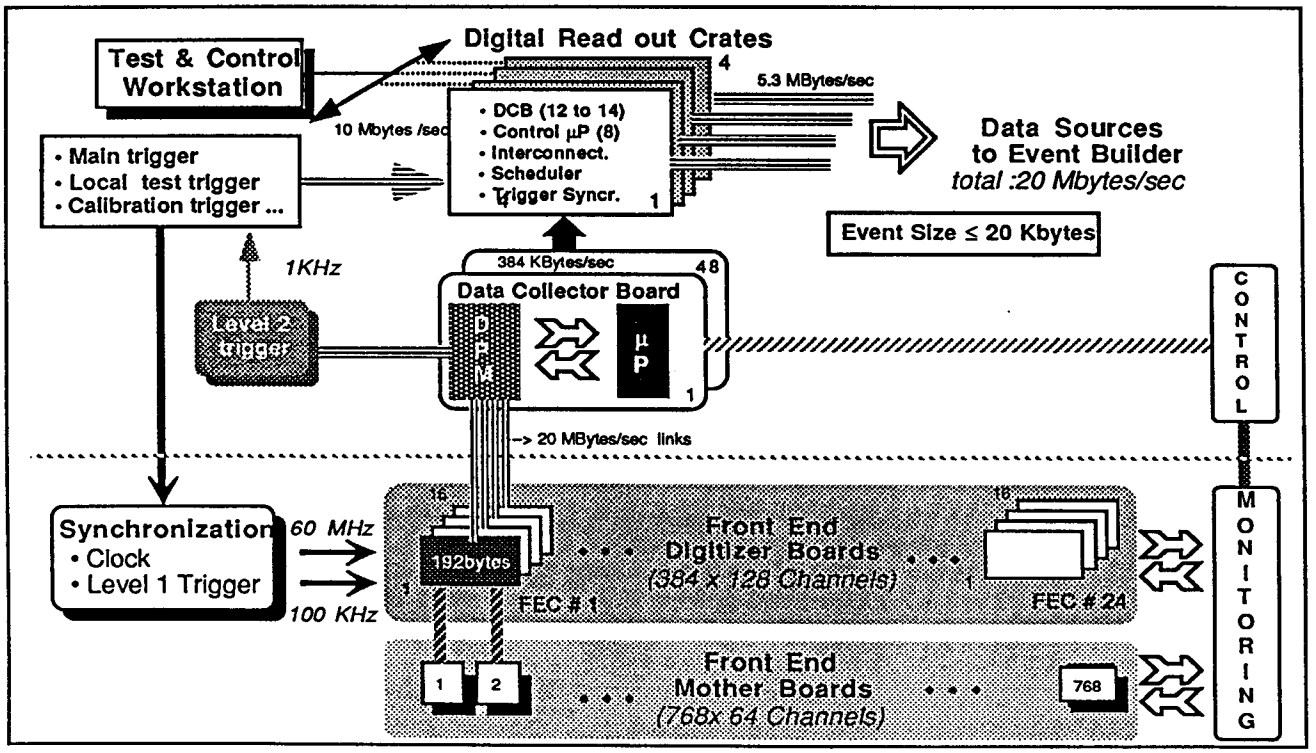
4.4.3.Data Collector Board

As described in the previous section, the data collection is achieved externally by the "Data Collector Board " through a "fiber point to point link". A maximum throughput of 20 Mbytes/sec is necessary to "push" every digitized raw information out of each front end card.

Preliminary specifications of this Data Collector Board are the following:

- able to read and monitor up to 1024 front end channels.
- 8 fiber inputs (one per Front End Board) with its internal resources (LAN...)
- a RISC microprocessor kemel
- Dual port DRAM buffer memory.
- Control or DAQ bus interface
- interface "feature extraction" for the level 2 data including a possible "local level 2 data processing" performing a cluster finding algorithm .

With this scheme, he full SMD DAQ readout can be done using 384 fibers connected to 48 "Data Collector Boards" (each card being the image of 8 Front End Digitizer Cards). They fill up 4 Digital Readout Crates (2 for the end caps and 2 for the barrel). This is a flexible manner to solve the "topological "readout problem and the level 2 data extraction. There is another advantage that the Front End Crate can contain indifferently any Front End Card belonging either to the calorimeter or the SMD.



5. Prototypes

Series of tests are planned for 1993 in order to implement such configuration in a realistic environment. This will be mainly focused on photo detector comparison and performance of each ASIC and little on the system aspect.

5.1. 1993 tests

It is foreseen to equip up to 256 channels of the SMD electronics in 93 . Two calorimeter-SMD test-beam prototypes have been selected. Three successive steps have been identified. They are compatible with the production of each ASIC in order to systematically test each function in the best realistic environment :

- Step #1 : the end cap monolithic prototype (LBL design) with up to 64 channels (BNL ~ June 93). Photo detectors (MCPMTs & APDs) associated with the ASIC#1 (charge integrator) could be implemented at that time.

- Step # 2 : the Barrel "Full Scale Prototype" with up to 256 channels of the SMD (FNAL ≥ July 93) where the first activity will be to test the system environment and the combined calorimeter/SMD performance. Test of the read out front electronics (ASICs # 1 + 3 + 4) should be possible but with a limited time.

- Step # 3 : Test of the full chain (> September 93) using a prototype of the "Mother Board" (ASIC # 1) and a versatile 6U VME front board equipped with the ASIC 2 + 3 + 4, including the connection (line driver and receiver).

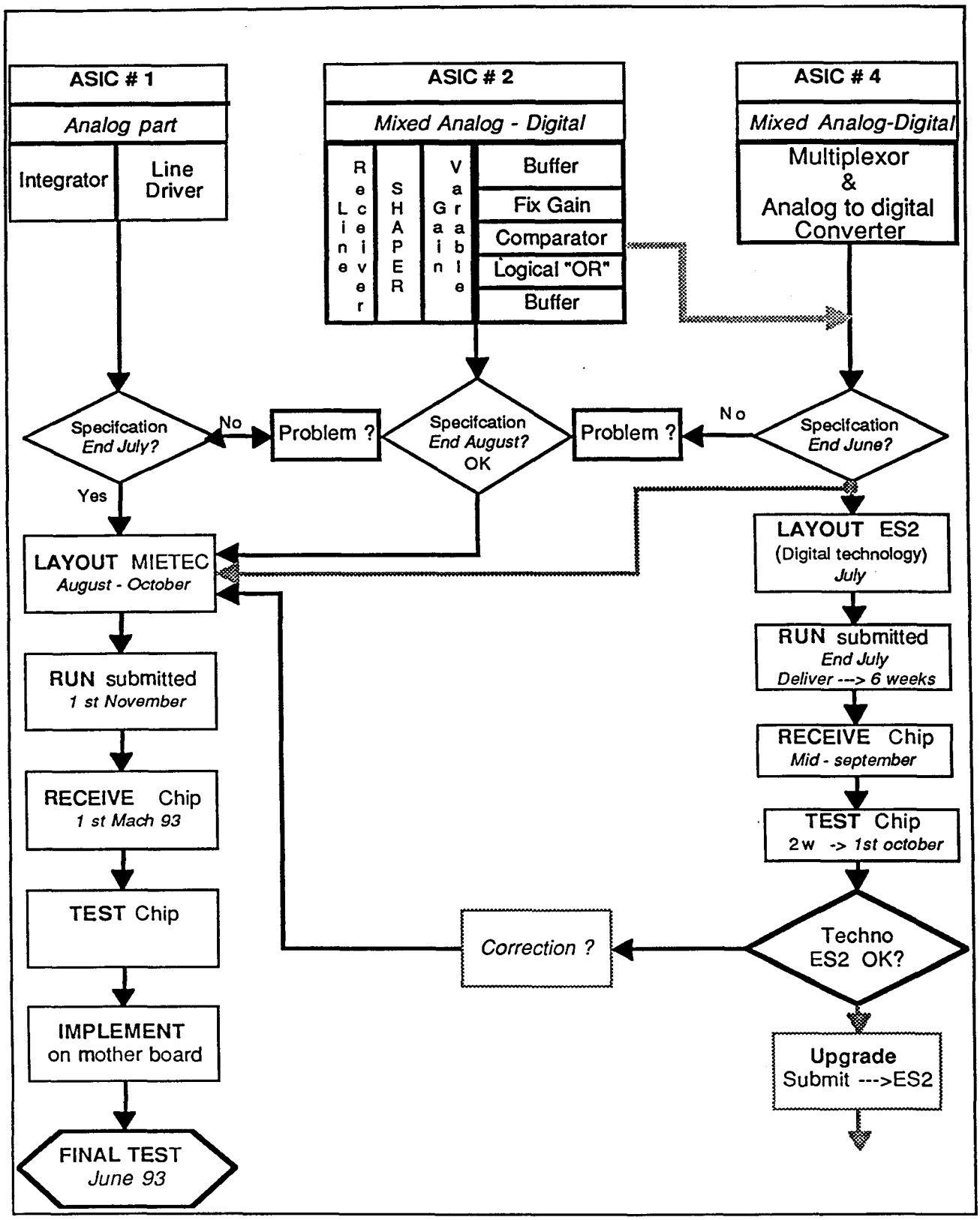
5.2. Status of the various components

The status (august 92) of each ASIC necessary for the 93 test is presented below. A summary of the different operations is presented in the flow chart diagram. Until now, analog CMOS 1.5 µm technology is only available in Europe in the MIETEC company with only 2 runs per year (November and April). Another company ES2 has a better running time (6 weeks) but has no experience in analog CMOS technology. A 20 chip's wafer for each ASIC (320 channels) will be produced for next year:

- ASIC # 1 (integrator): optimization and simulation of the design is completed. This is a 10 mm2 CMOS chip. The layout in underway which will be submitted the 1st of November 92 at MIETEC .

- ASIC # 2 (Shaper, Variable Gain & Fast Comparator): optimization of the variable gain function is not yet totally completed. Global simulation is underway. This is also a 10 mm2 CMOS chip. Submission will be made in November to MIETEC in the same time as the ASIC #1.

- ASIC # 4 (analog multiplexor, amplifier and comparator) : design and simulation are completed since July 92 and a first layout was submitted to ES2 as a "test bed" for analog technology. This is a 15 mm2 CMOS chip. A first wafer of 20 chips will be expected to be delivered in September 92. Submission for a second run will be possible to MIETEC or/and ES2. This depends on the test results (end September 92).


ASIC # 1
Analog part
Integrator
Line Driver
ASIC # 2
Mixed Analog - Digital
Line Receiver
SHAPER
Gain
Variable
Buffer
Fix Gain
Comparator
Logical "OR"
Buffer
ASIC # 4
Mixed Analog-Digital
Multiplexor & Analog to digital Converter
Specifcation End July?
No
Problem ?
Specifcation End August? OK
Problem ?
No
Specifcation End June?
Yes
LAYOUT MIETEC August - October
LAYOUT ES2 (Digital technology) July
RUN submitted End July Deliver ---> 6 weeks
RUN submitted 1 st November
RECEIVE Chip 1 st Mach 93
RECEIVE Chip Mid - september
TEST Chip 2w -> 1st october
TEST Chip
Correction ?
Techno ES2 OK?
IMPLEMENT on mother board
Upgrade Submit --->ES2
FINAL TEST June 93

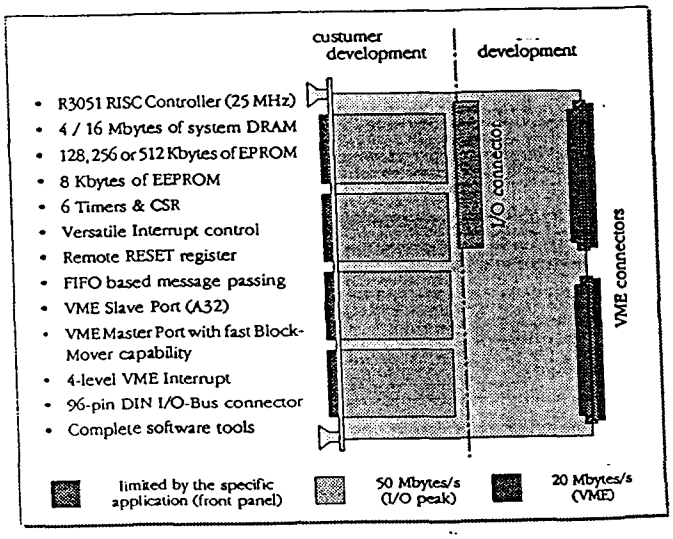
The design of the system aspect i.e. mounting these ASICs on simple printed circuit board will start soon (September 92) :

- The 64 channels "Mother Board" should be defined in close connection with the photo detector. A dedicated meeting is planned in October at Rockfeller University to define its specification. The first prototype should be ready by march 93 when the ASIC# 1 will be delivered.

- The "Front End Card" that contain the pipeline and the digitizer is under study. A first VME card containing 48 channels (3 SCAs) is under design at LBL. This card can be used for the combined barrel FSP calorimeter /SMD test at FNAL. However, it is foreseen to implement our digitization scheme in a very simple and economic manner. The idea is to avoid to spend time and money to design a standard 6U VME board with its DAQ interface. We intend to use for example the CES MIO board [Ref. 5]. The architecture of this module is based on five major blocks:
  - the microprocessor kernel
  - the system DRAM
  - the internal resources
  - the VME bus interface
  - the I/O specific hardware which is tailored for each application. The I/O functions are designed on separate piggy-back modules. Up to 4 piggybacks can be attached to a standard MIO board with 96 pins I/O connector.

  A first idea is to implement the digitization chain (ASIC 2+3+4) and its control logic on one or two piggy-back boards . Minimum of 32 channels could then be implemented in such a way. Further modification or evolution will be very easy to design an another piggy-back without changing anything in the readout part. In addition, optimization of noise problem could be achieved in such layout by a physical separation between the front end analog/digital conversion chain and the VME logic. A first piggy-back with one SCA followed by the ASIC # 4 can be implemented soon.

- Connection of the 2 parts (line driver, cable and line receiver) in a typical calorimeter/ SMD common problem and should be solved in the same manner. Discussion with LBL about this subject will take place in a meeting in September at Saclay.



5.3. New developments

The flexibility of this design is that we should be able to investigate others photo detector devices by adapting and optimizing only the first function (charge integrator) . Two developments are under discussion:

5.3.1.Negative current input for the ASIC # 1

A new 64 channels MCPMT fabricated by Hamamatsu is being tested at UCLA. This device has a negative output current.

- A modified version of the ASIC #1 (integrator) is under study.

5.3.2.Avalanche Photo Diodes

APDs array of 8 x 8 pixels are being developed for the SDC SMD detector. Prototypes of these array currently exist, are tested and are exhibiting good gain uniformity, with room temperature dark currents low enough to make direct detectionof few photons minimum signal feasible. These devices are operated in a linear mode, with gain of 100 to 500.

A particular charge integrator (ASIC # 1) is under discussion between LBL and Saclay. This ASIC is derived from erxisting study of similar circuitry. For a device with a pixel capacitance of 1 pF and 5 nA dark current, preliminary specification and simulations results are:

- 16 channels 1.2 μm CMOS.
- Gain 1000.
- Equivalent Noise Charge (ENC) 200 electrons rms (for a 16 ns RC-CR shaper).
- Signal/Noise ≥4.
- Power consumption 10 mW/Ch.

6. Logistic

This chapter presents for the first time the situation of the electronics seen from the "Saclay point of view". It should be emphasised that until now the Saclay group has the responsibility to design the readout chain and to build a large part the SMD electronics. It is not yet clear if we can afford 50, 75 or even 100% of these channels? It's depends strongly of the way to define the balance between the " cash money" and internal engineering labor. The cost was evaluated using European criteria and our past experience in large experiments at LEP (Aleph, Delphi, Opal) and HERA (H1) in the design and fabrication of front end electronics systems. It could be slightly different from the previous TDR WBS that currently couples together the calorimeter and SMD may be not the optimum realistic solution. As it is presented above the "Mother Board" will be anyway different, but it likely that the connection (Line Driver and Receiver) and the "Front End Board" can use identical blocks as much as possible and even be the same. This chapter is not yet completed and there will be a revised version for the September revue. However, our first goal is to give a realistic evaluation of the cost of one channel of this electronics chain as described in this document.

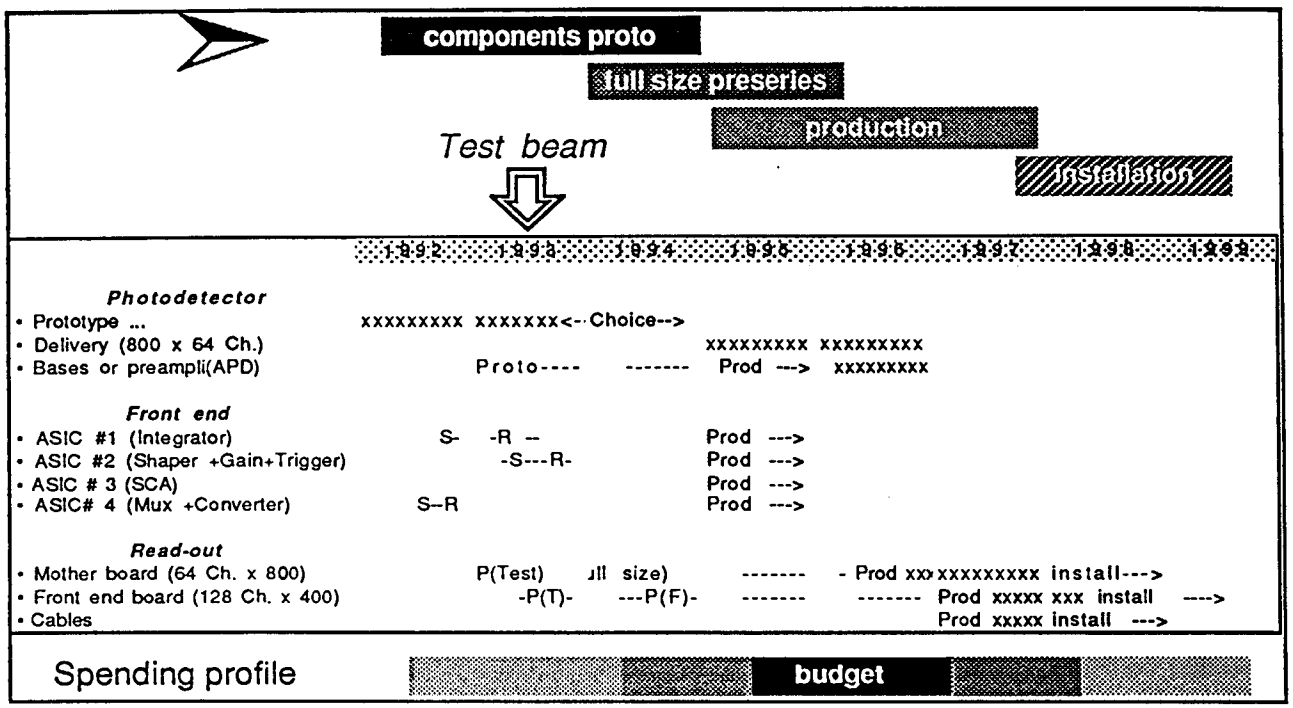
6.1.Cost

The following table presents the production cost including assembly and test of each component (for a large quantity) based on a realistic and known European price list and a dollar currency exchange at 5 FF. Prototypes, development costs and calibration stuff are not yet included due to the lack of time. In particular, it should be noted that the grater part of the cost is coming from the "Front End Card" which was estimated using a recent "conservative" commercial example. Optimization and refinement can to be achieved by the end of 92. It is also clear that the readout option 2 is already 30% cheaper. It should be notice that there is a very strong interconnection between the Front readout Card and the DAQ system and these 2 items are difficult to be estimated independently.

Component	Cost est.	# ch.	Cost ($)	cost per channel	Quantity	Cost(K$)
Option 1						total
• ASIC# 1 (Charge Integrator)	MIETEC	16	20	1.25	3000	60
• ASIC # 2 (RC + Gv+ Comp)	MIETEC	16	20	1.25	3000	60
• ASIC # 3 (SCA)	"LBL"	16	20	1.25	3000	60
• ASIC # 4 (MUX+ range det.)	ES2	16	50	3.15	3000	150
• FADC 8 bit-20 MHz	SONY	1	30	1.88	3000	90
• Mother Board	Saclay	64	200	3.13	800	160
• Cables and connectors	CERN	32	40	1.25	1600	64
• Front End Board*	CES...	128	2500	19.53	400	1000
Total (option 1)				32.65		1644
Option 2						
• "Dumb" Front end board *	Saclay	128	1000	7.81	400	400
Total (option 2)				20.93		1044
Level 2 Trigger						
• "Data Collector Board"	CES	1024	2500	2.44	48	120
• Fiber Channel 1 Gb connection	UWS	128	300	2.34	400	120
Total (Level Trigger 2 part)				4.78		240

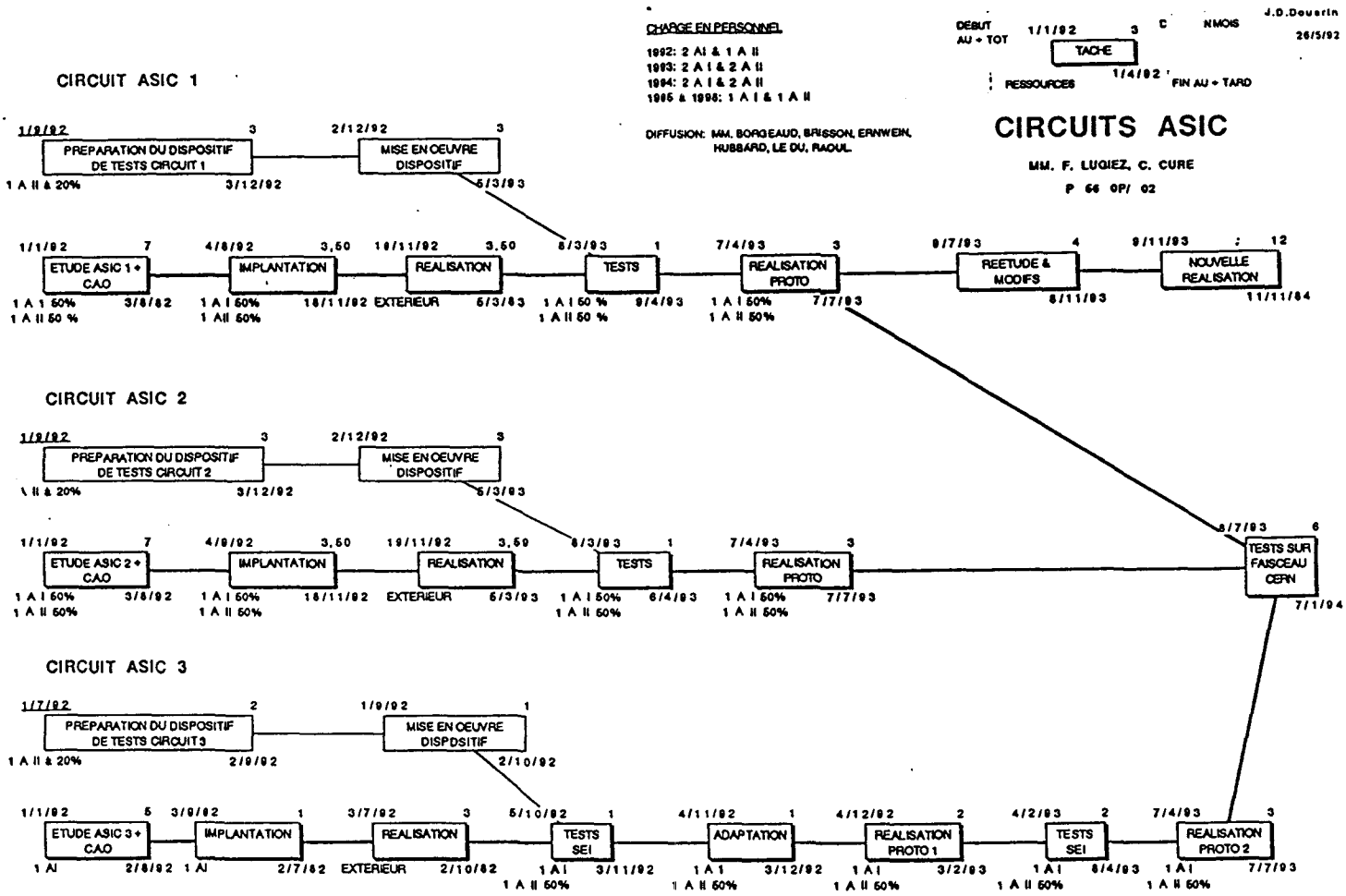
6.2.Schedule

A realistic and coherent time scale and a description of the different phases of activities including critical choices are presented below. Taking in account uncertainties of the SSC schedule, it would be very unrealistic to take decision too early since some developments to reduce the costs are underway (photo detectors for example!). This schedule is however compatible with an SSC setting-up in late 99 where all decision should be made by the beginning of 95. Production is spread over the next 3 years (95 to 98).



6.3.Manpower

Presently, there are 4 persons working almost full time (FTE) on this project. Most of the work has to be done on the ASIC part and the definition of the 2 PC boards. Prototype's production is not yet well estimated due to the lack of time. In the next 2 years, it is foreseen to have 3 FTE (2 engineers and 1 technician). Since the production will be done outside our institution, this number should decrease to 2 (one "project engineer " and one technician). The following diagram shows the first part of our planning (92 to 94) up to the production phase.



7. Conclusions & Summary

This document intends to present a coherent, realistic plan to build a reliable and cost effective front end electronics chain for the ShowerMax Detector using the available manpower.

The main characteristics of such an electronics chain are:

- COMPACT : using a series of 4 "functional CMOS Application Specific Integrated Circuits (ASICs) allowing a high density electronics design, fabrication and packaging.

- FLEXIBLE with a logical implementation in 2 parts :
  - a 64 channels pure analog "Mother Board" optimized for the selected photo detector (MCPMT or APD).
  - A "simple" 128 channels "Front End Board" that contains essentially the pipeline and the analog to digital converter part.

- MODULAR approach that allow a cost effective repair, maintenance and performance upgrades as better quality photodetectors (MCPMTs or APDs) becomes available.

- CHEAP : a minimal production cost ~ of 20 $ per channel can be achieved.

It is also demonstrated what are the technical advantages but also the limitations of a common calorimeter & SMD "global readout concept". Finally, study of the cost shows that there is a very strong connection between the design of front end and the DAQ readout scheme. In particular in term of system upgrade, reliability and maintenance over a long period. Minimizing the front end card functions to a simple "dumb" board should allow to save not only much money but also maintenance cost.

8. References

[1] The SDC ShowerMax detector - SDC report in preparation.
[2] From P. Cushman & R. Rusack (private communication)
[3] SDC TDR chaper 8 (Electronics & DAQ)
[4] "A high speed CMOS comparator with 8 bit resolution". W. Sausen - IEEE Journal of solid state circuits. Vol. 27 No. Feb.. 92.
[5] Creative Electronics System MOI 8261 Multi I/O VME board specifications.