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DIGITAL READOUT OF THE SHOWER-MAXIMUM DETECTOR OF THE SDC CALORIMETER

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INTRODUCTION

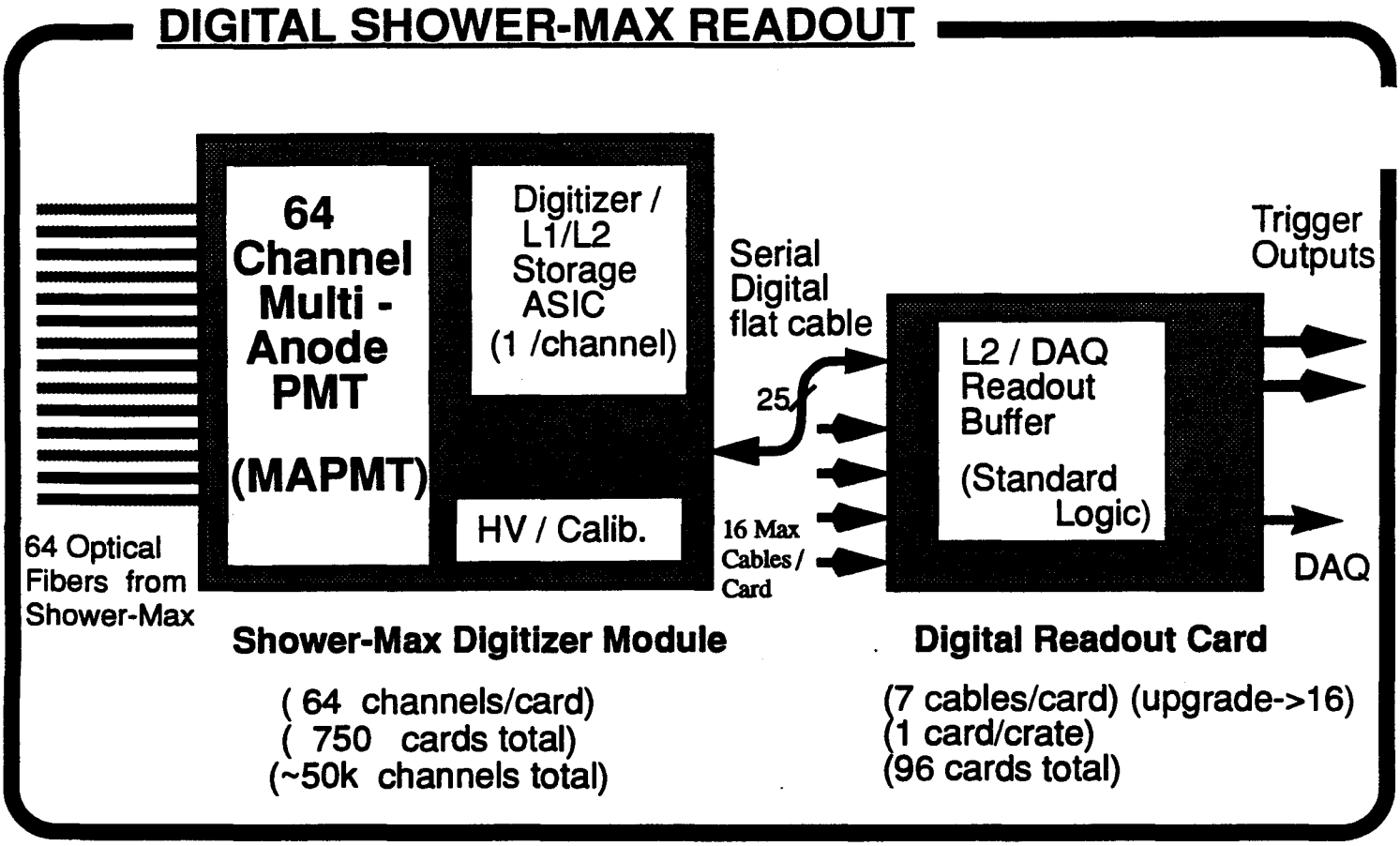
This document describes the Digital Phototube readout for the Shower-Maximum "Strip" detectors of the SDC calorimeter [1] [2] . It is closely related to the Digital Readout System [3] for the main photomultiplier tubes (PMTs) of the calorimeter. The main differences in the Shower-Max version are the reduced dynamic range and accuracy requirements and the reduced capabilities of the Level 1 trigger outputs. These are reflected in a lower power dissipation and cost per channel. This is achieved through a higher level of integration than in the Digital PMTs of the main calorimeter readout.

In this system, the phototube signals are digitized immediately at the base of each photodetector. The digitized information is stored locally (on the same IC which performs the digitization) during the trigger decision time. In the baseline design, only a single bit from each channel is output to the Level 1 trigger system. The full digitized information is transmitted to the Trigger/DAQ system following a L1/L2 trigger accept.

The photodetector in the SDC baseline design is a 64-channel multi-anode PM tube (MAPMT). This document describes a system in which a single mechanical package contains a MAPMT and 64 channels of digitizer. The Digital readout system will work equally well with other photodetectors (such as APDs).

The Shower-Max system is essentially a repackaging of the subcircuits of the Digital Phototube System into ways which are economical and convenient for Shower-Max. Only a single custom Application Specific Integrated Circuit (ASIC) is required. It contains subcircuits which have been successfully tested for the Digital Readout of the main PMTs. The layout of this ASIC is now underway.

The main strengths of this system are it's simplicity, and the fact that all analog operations take place in the interior of a metal can containing the MAPMT, base, and digitizers. All external signal processing is done digitally. It thereby avoids the system-level analog noise and crosstalk problems which are the traditional bane of detector commissioning. It also benefits from the flexibility, modularity, and upgrade capabilities offered by rapidly advancing digital technology.



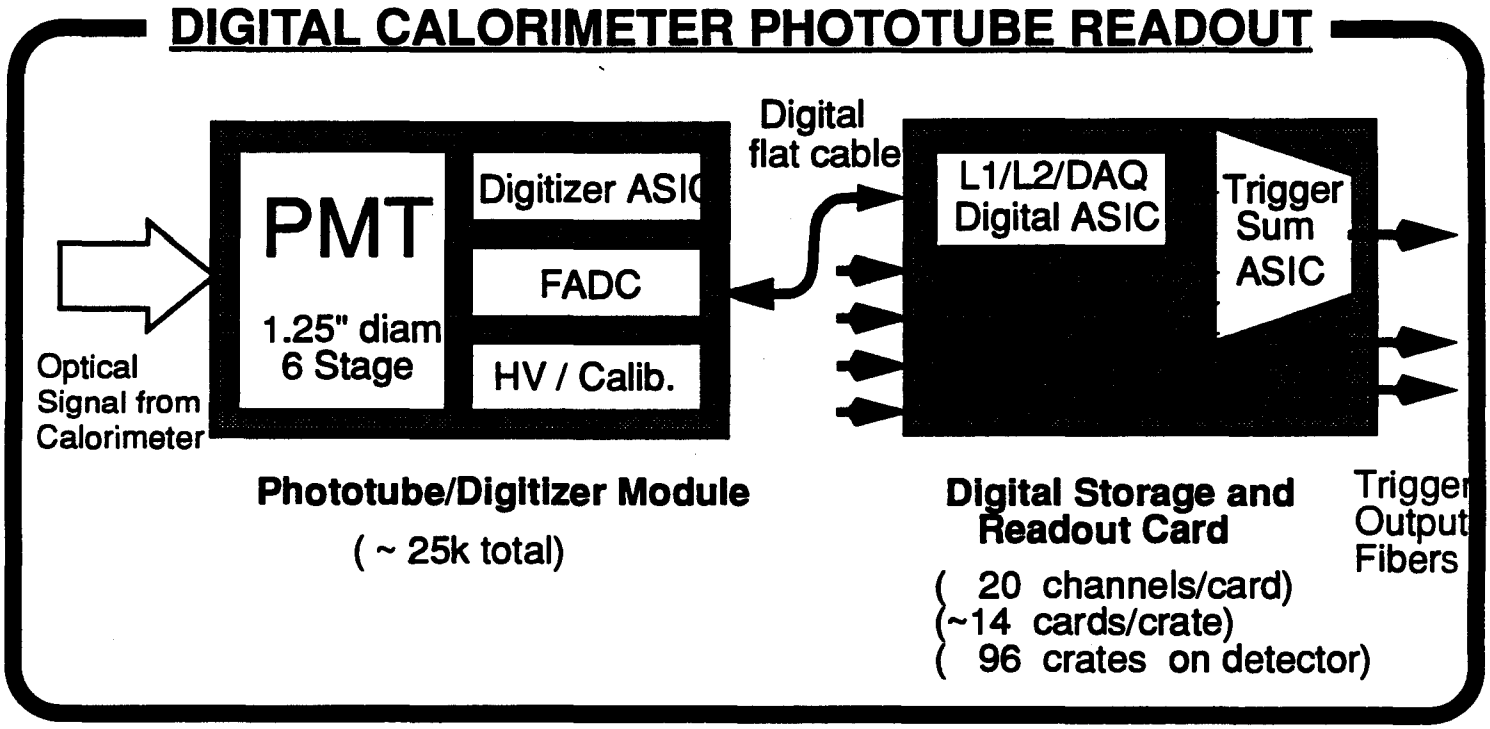


Fig. 1. Block Diagrams of the Digital Shower-Maximum Readout System and the Digital Phototube Readout System for the SDC calorimeter.

Table 1: Specifications for Shower-Max Digital Readout

Channel Count	47,000 (upgrade to 100k)
Photodetector	64-Channel Multi-Anode PMT (or 64-channel APD + Preamp Assy)
Digitizer Location	64 Channels on base of Photodetector
L1/L2 Storage	on Digitizer ASIC
DAQ Interface	Serial Digital Flat Cable to Readout Card
Readout Card	Single Card in Crate on Detector. Each Card handles 7 Modules/Wedge, (Upgrade to 14)
Time Resolution	16ns
Dynamic Range	12 bits (greater if desired)
Least Count	250 MeV (15 fC)
Full Scale	1 TeV (60 pC)
Output Format	Digital Floating Point 3 bit Exponent (8 Scale Ranges) 5+1 bit Mantissa
Accuracy	Signals Digitized to accuracy which varies between 1/64 and1/32 of itself. Digitization Sigma averages 0.6%
Peak Current from PMT	8ma x 15ns triangular pulse
Signal Rise Time	5-8ns
Crosstalk	<0.5% electronic crosstalk.
Level 1 Trigger Output (option; staged at present)	1-bit Digitally Programmable Energy Threshold
Clock / Gate Timing	+/- 0.5ns Programmable, Adjustment Individually Per Channel
Phototube DC Current Measurement	Individual Per Channel Built into Digitizer ASIC Dynamic Range 0.01nA --> 10uA
Charge Injection Calibration Circuit	Two ranges, built into Digitizer ASIC. Computer enable for each range.
High Voltage Supply	Cockroft-Walton on Base
Power/Channel	~ 100 mW

SHOWER-MAX BASE / DIGITIZER MODULE

The system has two components. The first (fig.2) is a Multi-Anode PMT HV Base/Digitizer module. Seven of these reside on the back of each "wedge" of calorimetry, with provision for another seven as an upgrade option. Each module processes the optical signals from 64 tile/fiber "strips" and contains a 64-channel PM tube. It contains digitization and local storage of data during the L1/L2 trigger decision time. It outputs the full digitized signal to L2/DAQ as floating-point numbers on a multiplexed (serial) flat cable. A single flat cable is required for clock, control, serial data, calibration and power supply to each module. The design also provides for individual Level 1 trigger bits for each channel. (At present these are "staged" in the SDC baseline design. If implemented, these will require a second flat cable from each module to carry the L1 trigger signals). The module provides the PMT high voltage via a Cockroft-Walton "charge pump"[15] [16] , so that no exposed HV cabling occurs anywhere in the system.

DIGITAL READOUT CARD

The second component is a digital readout card which is located in crates mounted on the detector. A single card accommodates the seven (as an upgrade, eventually 14) modules on each wedge. It performs low-bandwidth Data Acquisition (DAQ), Calibration, and HV control functions. It also fans out clock, power, and trigger/control signals on the flat cable to each Base/Digitizer module.

In the SDC "baseline" design, this card simply receives the serial digitized data from each module and stores it for DAQ readout. It is a 9U VME card containing "standard" logic (no custom ICs). As possible upgrade paths, this card transmits the L1 and/or L2 signals over fiber optics to the (upstairs) trigger system, or uses the L1/L2 trigger signals for local electron identification logic. (See Trigger discussion below).

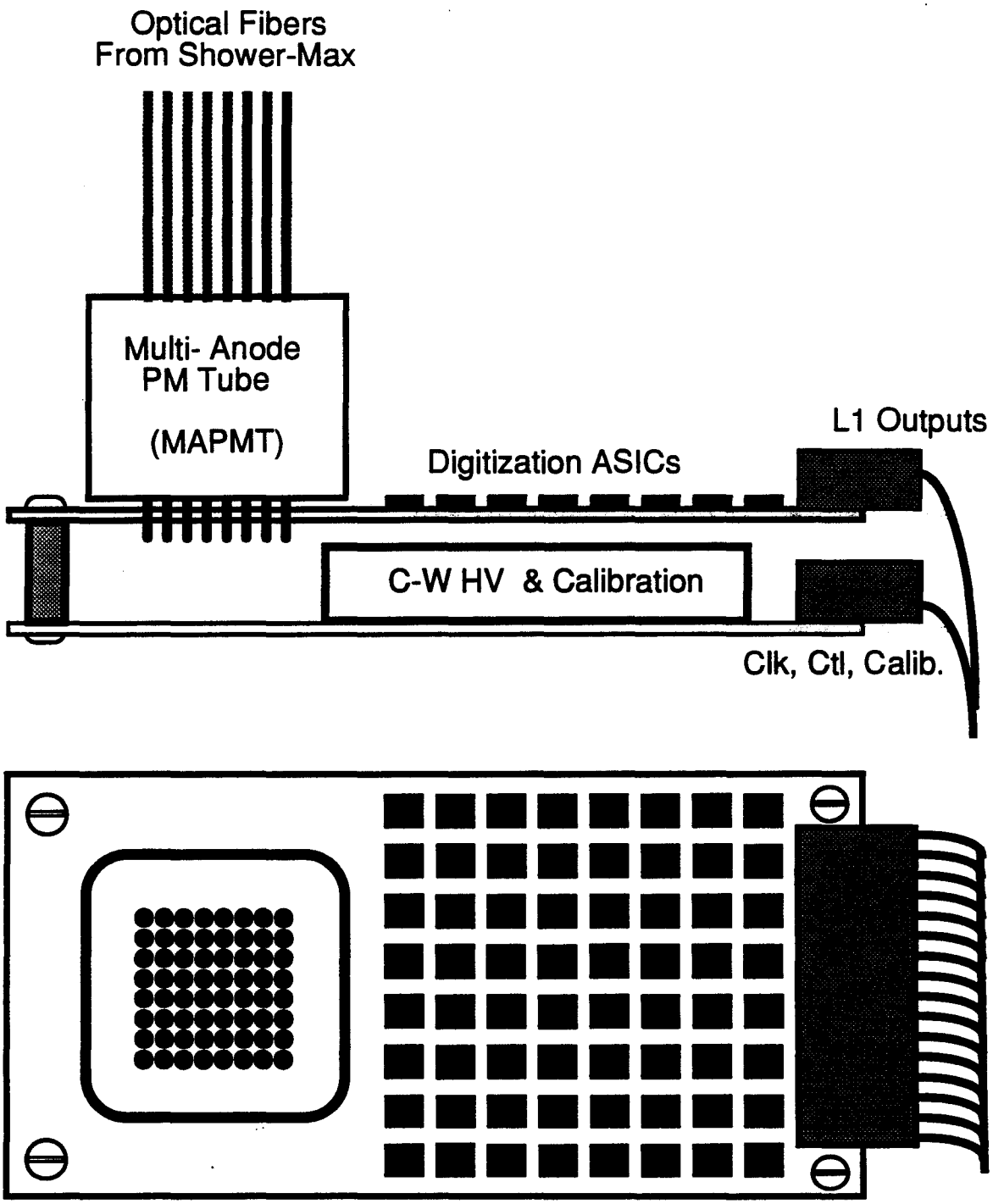


Fig 2. Multi-Anode PMT Base-Digitizer Module. 64 Digitizer ASICs are connected to individual anodes on the MAPMT. Clock, control, calibration, power and serial data signals connect through a single flat cable. A second flat cable transmits "Discriminator Bits" for each channel to the Level 1 trigger.

DIGITAL SHOWER-MAX READOUT BOARD

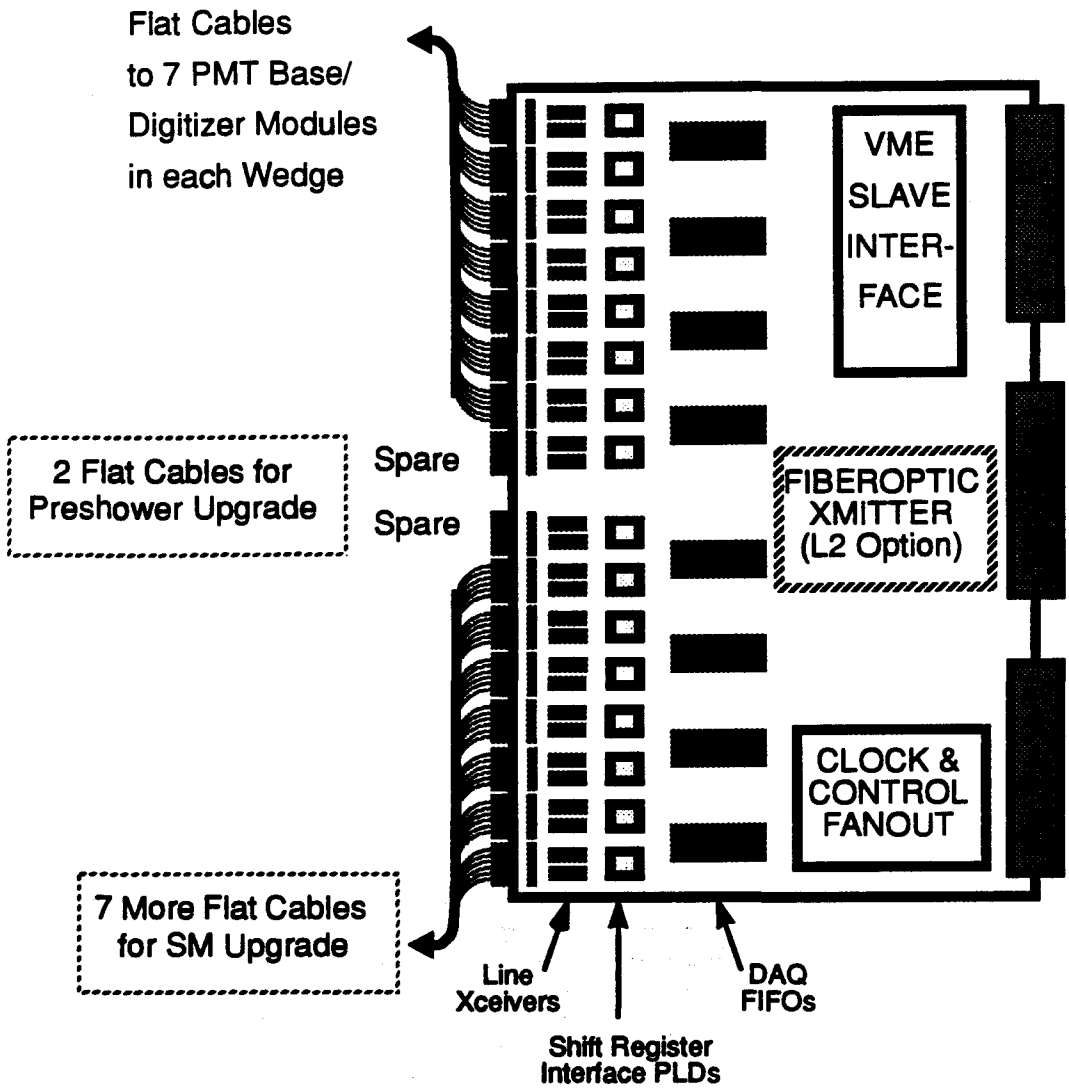


Fig 3. VME Readout Board for Digital Shower-Maximum System. The readout board fans out Clock, Trigger, Control and DC Power via flat cables to the digitizer modules. It also controls the serial (JTAG-type shift register) linkages on the flat cables which are used for diagnostics, downloading, and DAQ. The incoming data is stored in FIFOs for DAQ readout over the crate backplane, and (optionally) transmitted to Level 2 following a L1 accept.

Table 2: Shower-Max Digital Readout Card Specifications

Mechanical	9U Eurocard
Inputs	16 cables from Digitizer Modules. 7 channels Used in Baseline; 7 more for Upgrade. (Barrel)
Cable Type	0.025" pitch flat cable with ground plane.
Signals Levels on Cable	See Table 3
Serial Links	JTAG-type shift register interface on flat cable to each module. Used for diagnostics, downloading, and DAQ. PLD on each channel to handle serial shift-register protocol.
Calibration Voltage (charge injection)	Generated by 12-bit DACs on Readout Card. One per Digitizer module.
Clock & Control Fanout	Input to board on P3 backplane. Fanned out (0.5V differential) on flat cables. Timing Slew <3ns. Clock Jitter <0.1ns RMS.
VME Interface	Block Transfer Slave
Event Record Size	64 Bytes per digitizer module from each live crossing. 512 bytes maximum if all 16 inputs connected.
Readout Time	12.8 usec at 40MB/sec (all 16 channels) 13% bus utilization at 10,000 events/sec
Level 2 Outputs (optional)	One 1GB/sec fiber optic output per card. Transmits Event data (512-bytes) in 5usec following L1 Accept. Buffered by Level 2 FIFOs on Digitizer ASICs to allow multiple Level 1 triggers pending.
Power Dissipation	15W on card 100W on Digitizer modules connected to card (all 16 connected).

DIGITIZATION ASIC

The key component in this system is a custom CMOS IC (fig. 4) which integrates and digitizes the PMT charge in 16ns intervals.

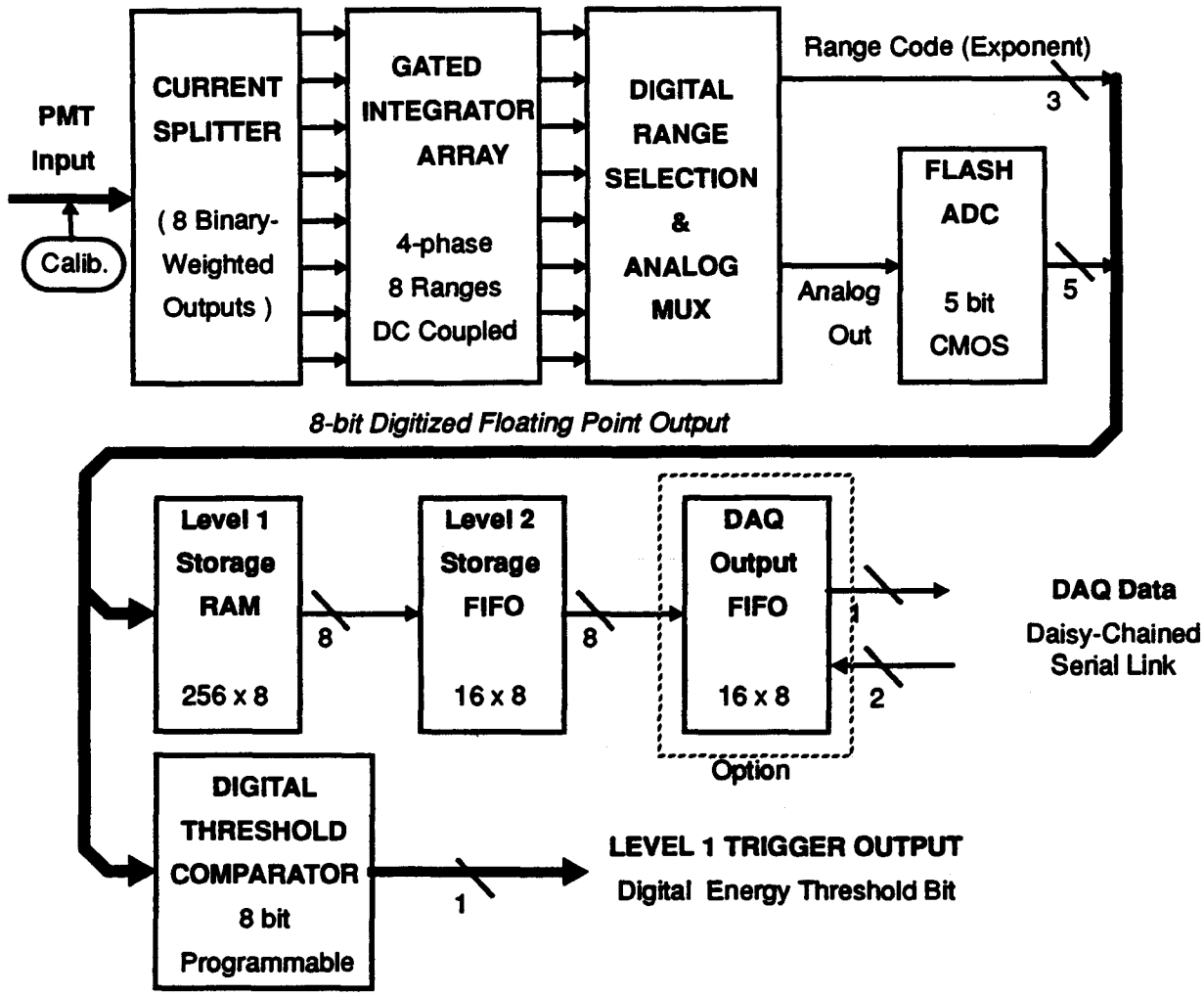


Fig. 4 SHOWER-MAX DIGITIZER IC BLOCK DIAGRAM. Main circuit elements are: (i) Current Splitter, which splits the Phototube current into 8 binary weighted scales; (ii) Gated Integrator Array, which integrates the charge from each scale on one of four capacitors in a pipelined "round-robin" manner; (iii) Autoranging logic, which determines which capacitor contains an "interesting" voltage (between 1/2 and full scale) and outputs this voltage to the Flash ADC; (iv) a 5-bit FADC using the design developed and tested in our Version 3 ASIC; (v) Level 1 digital storage RAM; (vii) Level 2 digital FIFO storage; (viii) Digital FIFO storage and serial output to DAQ (or optionally data is sent directly to Level 2), and (ix) digital threshold comparator for Level 1 trigger outputs. Calibration circuitry including Charge Injection and DC current monitoring is built into the front-end ASIC as described in [4] .

The Digitization ASIC contains a current splitter, gated integrator array, autoranging logic, flash ADC, digital L1/L2 DAQ storage, charge-injection calibration, a PMT current measurement circuit, and a serial interface for DAQ readout and diagnostics. The serial interfaces are daisy-chained (in groups of 8-16) to reduce the connector count on the readout flat cable. Low-level differential signals are used for digital I/O. A listing of the signals on the Digitization ASIC and Digitizer Flat Cable is given in Table 3.

Table 3: Digitizer Signals and their Function

Signal Name	Level	Description
PMT Input	0-10ma (analog)	Bare Anode from multi-anode PMT Current sensitive; held at virtual ground by splitter / integrator input.
Clock	0.5V Differential	60 MHz clock. Digital delay on ASIC allows phase adjustment of PMT integration gate individually for each channel.
Level 1 Accept, Level 2 Accept Level 2 Reject	0.5V Differential	Trigger signals which control Level 1 /Level 2 digital storage. Sampled synchronously on leading edge of clock.
Serial Data In Serial Data Out Serial Control	0.5V Differential	Serial Data Link (JTAG Shift Register) for diagnostics, downloading, and DAQ functions. Serial links are daisy-chained between ASICs on a digitizer module.
Level 1 Output	0.5V Differential	Level 1 output "discriminator" bit. 60 MHz Synchronous digital output. Output is high whenever digitized energy exceeds a programmable threshold.
V_{CALIB}	+/-5V (analog)	Calibration Voltage used for Charge Injection
T_{CALIB}	0.5V Differential	Calibration pulse timing signal used for Charge Injection.
V+, V-, Analog Ground Digital Ground	DC	Power supplies and ground signals.

The Digitization ASIC is packaged in a 28-pin PQFP (surface-mount package) (fig.5).

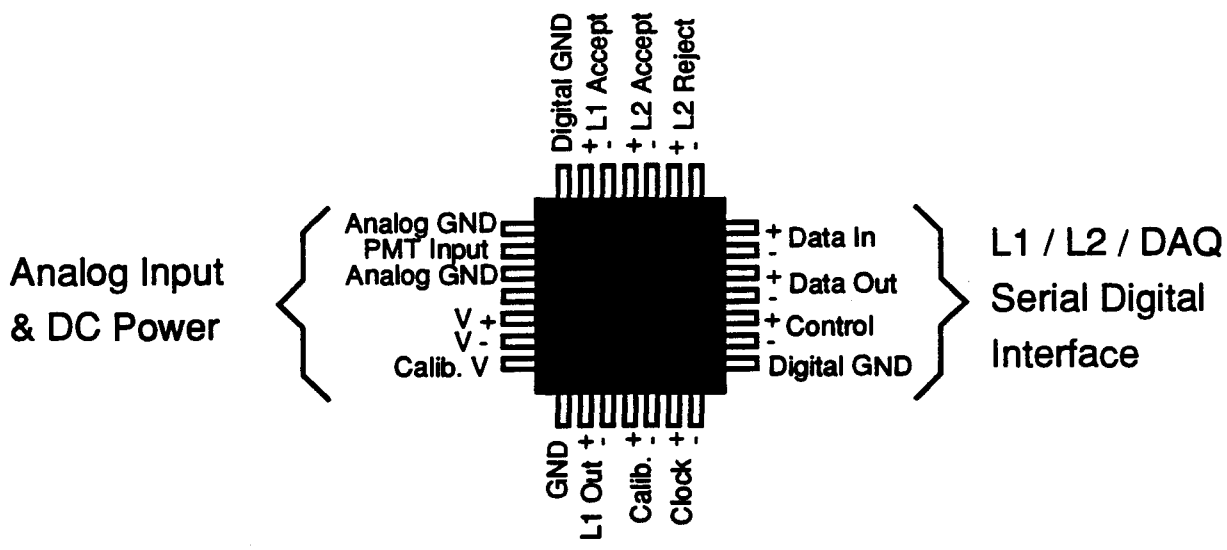


Fig. 5. Input/Output connections for Shower-Max Digitizer ASIC.

Additional details on the operation of the digitization ASIC are given in a subsequent section.

DYNAMIC RANGE AND ACCURACY

The floating-point output covers a 12-bit dynamic range (80 MeV to 320 GeV) with 5-6 bit accuracy. The dynamic range requirement matches the range over which the SDC intends to analyze electrons. The accuracy requirement comes from the desire to fit the centroid of an electron shower to ~1mm or ~1/10th of a strip width. Tests [7] [8] [9] for the Digital Photomultiplier readout system for the SDC calorimeter indicate that larger dynamic range (17-20 bits) can be obtained with this approach if this is deemed useful.

The Floating-point output is encoded as a 3-bit exponent (8 range scales) and a 5+1 bit mantissa. Thus, signals are digitized to an accuracy which varies between 1/32 and 1/64th of themselves. This is more than sufficient given the large intrinsic fluctuations due to electromagnetic shower development in the signals from shower-maximum detector.

TRIGGER OUTPUTS

The SDC does not yet understand the trigger capabilities that will be required from the Shower Max strips at various trigger levels. The trigger design described here[13] assumes that Level 1 receives a single bit from each channel, and that the fully digitized information is passed to the L2 trigger as well as DAQ. This results in a single flat cable for control and data, and a second flat cable for the Level 1 trigger outputs. Thus, the bandwidth and number of interconnections required for these signals are small. This results in a substantial improvement in the packaging density and cable layout as compared to the main PMTs.

The fully digital nature of the readout allows a number of trigger design options. The Shower-Max information passed to the L1 trigger can be a single bit per channel, several bits, a fraction of a bit (strips can be 'OR'ed in Eta or Phi), or no bits at all. The fully digitized information can be passed to the Level 2 trigger following a Level 1 accept, or passed to the L3/DAQ system following a Level 2 accept. In all cases, the trigger outputs will be derived from the fully digitized data. *The trigger will be operating on exactly the same information as the offline processing, so that the performance of the trigger will be completely deterministic.* The absence of a second trigger digitization path is a main operational advantage of the Digital PMT readout.

The digital readout boards can be easily replaced over the lifetime of the detector. This allows upgrades such as improved trigger algorithms,

trigger segmentation, DAQ bandwidth, etc. as machine luminosity and digital technology evolve.

DC COUPLING FOR HIGH RATE OPERATION.

The DC coupling provides immunity to rate effects and will allow the system to operate comfortably at a luminosity of $10^{34}cm^2/sec$.

COMPUTER CONTROLLED DE-SKEWING OF CLOCK, GATE, AND TEST PULSES.

The Shower-Maximum output pulses from the same beam crossing will not arrive at the same time. There will be differences of a few nsec arising from differences in the length of optical fibers from different shower-maximum strips. Routing of the optical fibers to the multi-anode PMTs is a highly nontrivial engineering problem, and it is difficult to guarantee that the fiber lengths in all channels will be matched. Additional time slewing will arise between different channels of the Multi-anode Photomultiplier Tubes and in the front-end electronics.

It is, however, essential that all PMT pulses be accurately positioned with respect to the integrator gate [12] . Trimming of optical fibers or delay cables is a very painful way to ensure this. Therefore, the Digital readout system allows computer controlled adjustment of the gate position **on individual channels.** This is accomplished with a digital delay selector on the clock input buffer of each digitization ASIC. This system permits automated correction for cable lengths, time-of-flight, and propagation delays in the shower-max fiber optics, phototubes and electronics. Cable and fiber lengths can be set by convenience rather than necessity, and all hand-trimming is avoided. This ability to trim the gate timings of individual channels is another major operational advantage of the digital Shower-Max readout system.

CALIBRATION FEATURES.

The digital readout system has a conventional electronic charge-injection system built into the Digitization ASICs. This system is described fully in [4] . The charge injection system has two scales which are capable of exercising the full dynamic range of the digitizers. Pulse height is set by a 12-bit calibration DAC on each module. Timing is set by a digital calibration

timing pulse from the control card. Individual channels can be enabled and disabled via commands from the DAQ interface of the Digitization ASIC.

The DC current from each anode of the MAPMTs can be monitored by circuitry built into the front-end ASIC. This circuitry is also described in [4]. The anode currents from radioactive sources which move throughout the detector [14] are used to calibrate and monitor the performance of the shower-maximum system.

DIAGNOSTIC FEATURES.

The Digital SM system has a complete set of pipeline diagnostics. Test patterns can be loaded into the front-end RAMs of the Shower-Max Digitizers and "played back" through the Trigger and DAQ. This performs a complete, full speed, end-to-end check of entire system. In fact, long sequences of *Monte Carlo* events can be stored in the front end digital RAMs and "played back" (in concert with the digital readout for the main Calorimeter PMTs) to verify trigger and DAQ performance. Since there are no stochastic analog components in the system, the entire Trigger/DAQ system is deterministic and performance can be absolutely verified, on an event-by-event basis, without beam.

ACCOMODATION OF LONG PIPELINE LENGTHS

In the digital Shower Max readout system there is no inherent technological limit to the trigger Level 1 pipeline length, as occur in analog storage schemes. For digital storage, the cost of adding another crossing's delay is 8 RAM cells per chip (very small), and the power dissipation increase is negligible. If some future upgrade, or some unforeseen contingency, requires a longer pipeline length it can be easily accommodated in the Digital PMT Readout system.

MORE DETAILS OF THE SHOWER-MAX DIGITIZATION ASIC

The shower-max digitization ASIC is a repackaged version of circuit components which have been developed for the Digital readout system for the "main" Calorimeter PMTs. The current-splitting and digitization in this system is described in detail elsewhere [3] [5]. The main differences for the Shower-Max readout are:

1) The current splitter for the Shower-Max readout is an all-CMOS design rather than the bipolar-CMOS design for the main PMTs. Bipolar performance is not needed because of the small (8ma) peak current from the multi-anode PMT compared to 100ma for the Calorimeter PMTs. The modest dynamic range and accuracy specifications for the Shower-Max readout are also satisfied by a CMOS current splitter (see fig.7). The advantages of a CMOS design are that a fine-lined CMOS process allows a compact L1/L2 storage RAM, and that all-CMOS designs are easier to fabricate for our foreign collaborators.

2) The Shower-Max digitizer contains an integral 5-bit Flash ADC. This consists of a block of 32 comparators and encoding logic to produce a 5-bit binary result. Our "Version 3" ASIC [10] contained comparators and encoding logic for a 4-bit FADC. Test results indicated that the comparator performance (10mv offset, 1mw power dissipation, 8ns worst-case response time) was more than adequate for a 5-bit Flash. This design has been expanded to 5 bits and is being included in the layout of the Shower-Maximum ASIC. The comparator layout for the Shower-max FADC is also being scaled from 2u to 1.2u design rules, which should result in improvements in both speed and power dissipation. Power dissipation calculations for the 5-bit FADC are based on measurements of the 2u test chip. Since the final design is being executed in a 1.2u process, these are probably pessimistic.

3) The digital storage elements for Level 1, Level 2, and DAQ are included on the front-end chip. The digitized information is transmitted to Level 2 and/or DAQ only following a trigger accept. The design for these elements is similar to digital storage ASICs [11] which we have fabricated, tested, and successfully incorporated in board-level designs.

4) The relatively low bandwidth of the L2/DAQ readout allows this data transmission to occur on a serial JTAG-type shift register readout. This readout is daisy-chained across the digitization ASICs, and a small number of serial links (~4) is required on the flat cable from each digitizer module. This approach avoids most of the of the cost and power dissipation associated with driving the parallel pipelined flat cable for the Calorimeter PMTs. The time taken to transfer one crossing's data from a Shower-Max module is: (64 Channels) x (8 bits) x (16ns) / (4 links) = 2usec. This is adequate for a worst-case assumption that all digitized data is to be transferred to Level 2 processors every ~10 usec.

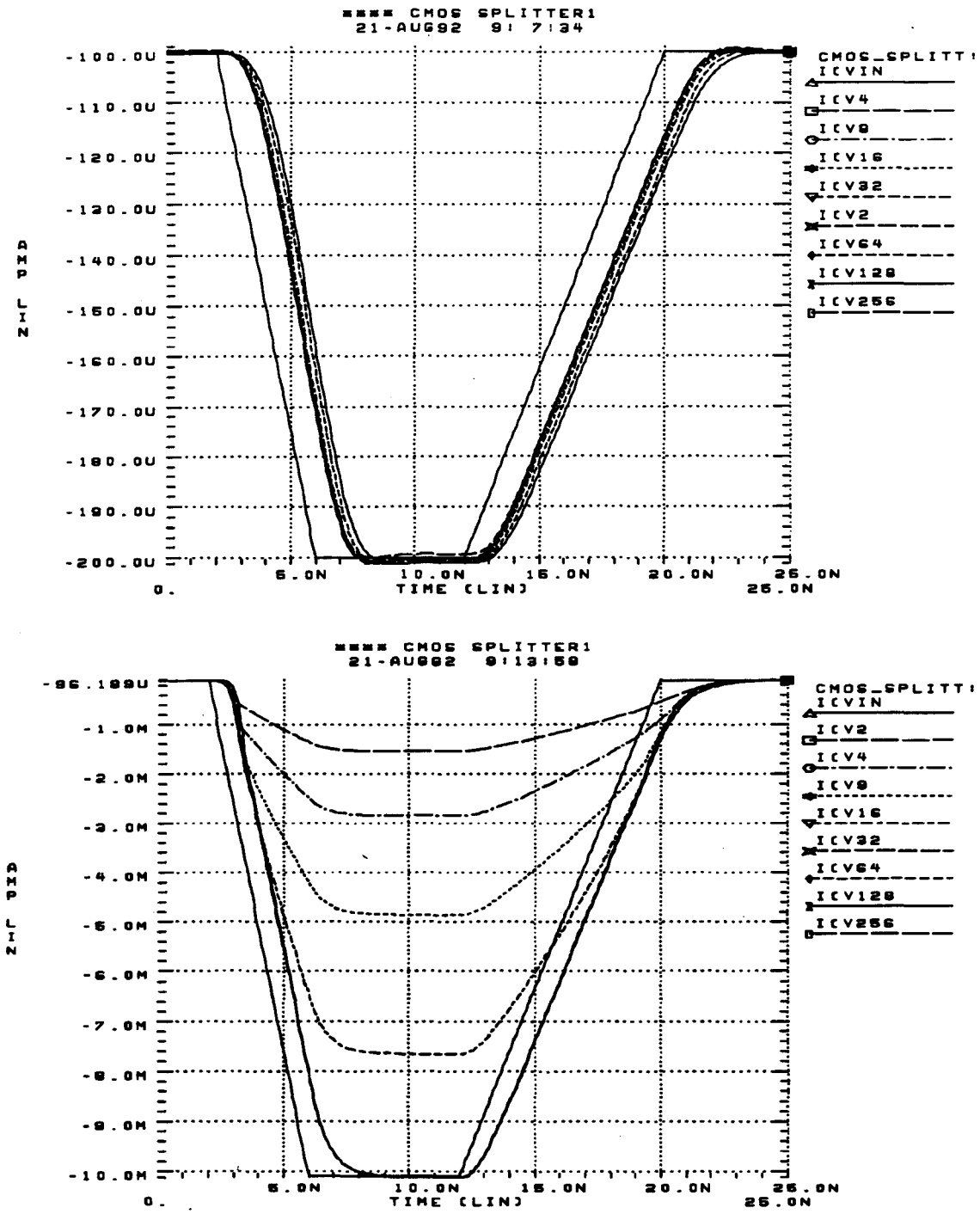


Fig 7. HSpice Simulation of CMOS Current-Splitter Design. TOP: 100uA current pulse from photodetector, with outputs from the current splitter. The 8 binary weighted outputs have been scaled appropriately and overlaid. BOTTOM: Full scale (10ma) current pulse from splitter. Current limiting is observed on the I/2, I/4, I/8, and I/16 scales -- this feature prevents overloading of the gated integrators on sensitive scales during large pulses. Current split accuracy is preserved on the I/32 through I/256 scales which are relevant for large pulses.

CABLE TESTS

The digital shower-max system uses the same type of cable as the Digital Calorimeter PMT readout. The cable must be able to carry 60 MHz digital signals for several meters, carry a modest amount of DC power, and conform to appropriate safety codes (i.e. be nonhalogenated). Tests have been performed[17] to determine a suitable readout cable and digital signal levels. The system cost estimates are based on a 0.025" pitch flat cable [6] with integral ground plane which meets our requirements. This is a nonhalogenated version of a cable that we have used in previous experiments. It is available in mass-terminated, factory tested assemblies in the lengths required.

SHOWER-MAX READOUT OPTION USING APDs.

Avalanche photodiodes (APDs) are being considered as an alternative photodetector to the Multi-Anode Photomultiplier tube. The changes required in the Digital Readout system to conform to this option are as follows:

1) A preamplifier with a current gain of roughly 200 and an input noise of ~500 electrons in a 16ns gate time would be required. The digitizer module would be divided into two sections: a low-level Analog section containing APDs and preamplifiers, and the digitizer section. See fig. 8.

2) The PMT HV supply would be gone, replaced by a 100-2kV supply for the APDs. It is unclear as to whether the APDs will require individually adjustable supplies.

3) The APDs will require some form of thermal management. In any case the temperature must be regulated to within ~1 degree C in order to maintain adequate gain stability. If the APDs and preamps must be cooled to provide adequate noise performance, then the Preamp section would be physically separated from the digitizer ASICs.

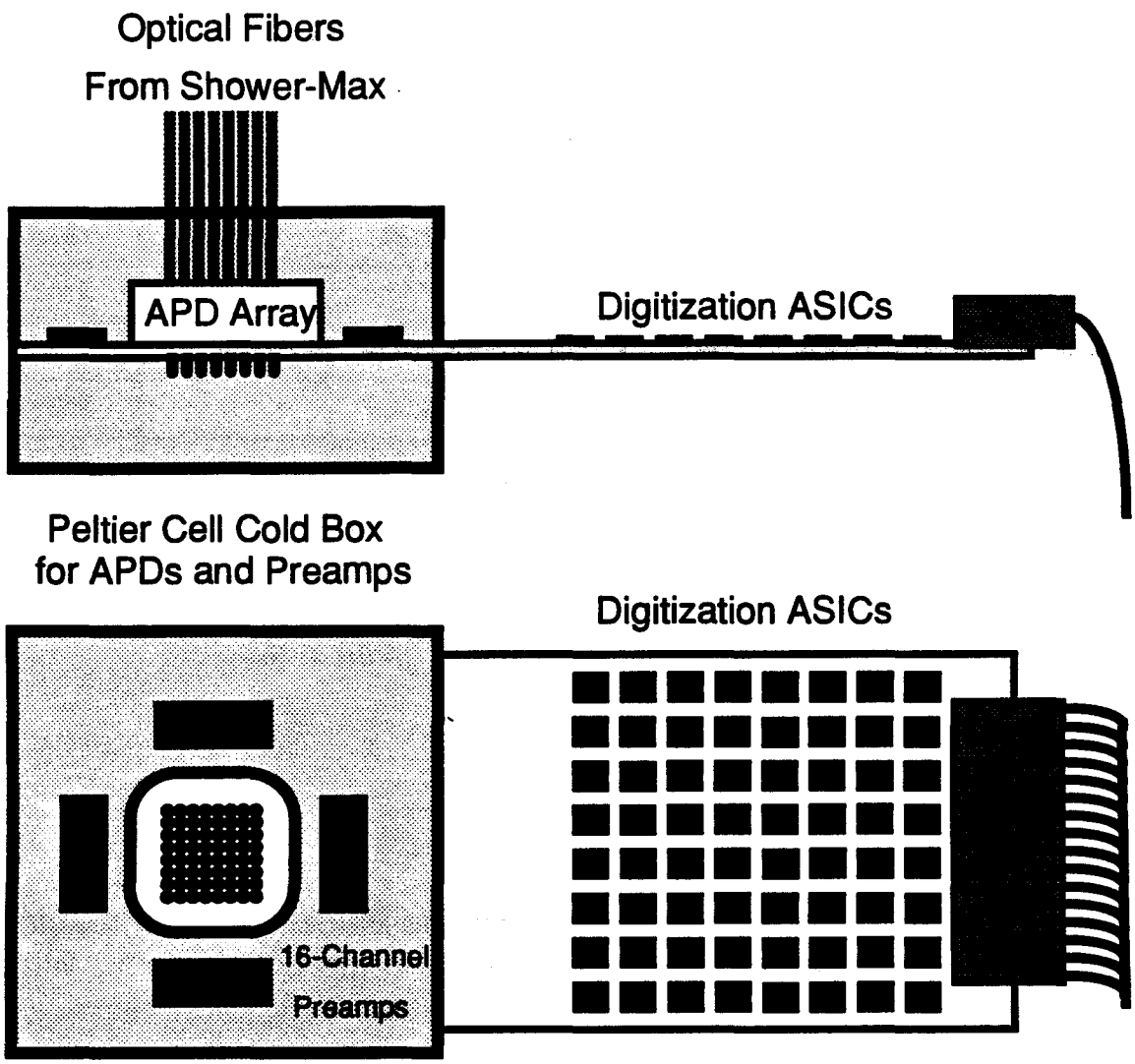


Fig 8. Shower Max Digitizer Module for Avalanche Photodiode (APD) Option. The module is separated into a low-temperature (~0 deg C) section containing a 64-channel APD array and FET preamps, and a room-temperature section containing Digitizer ASICs identical to those for the Multi-Anode PMT option.

SUMMARY COST ESTIMATE.

Fig. 10 gives a summary of production costs, and Table 4 gives a summary cost estimate for the system.

Table 4: Cost Estimate for Digital Shower-Maximum System

Item	Cost ea.	Qty.	Total
Digitizer Modules: (production, test, and all parts except Digitizer ASICs and MAPMT / HV)	$124	750	$93,750
Digitizer ASICs (production Cost)	$5.96	48,000	$286,080
Flat Cable Assemblies (production + test)	$27.20	750	$20,400
Digital Readout Board (Production + test)	$1546	96	$148,416
Production Engineering and Documentation	$147,000	1	$147,000
Pre-production Electronics and Engineering	$624,000	1	$624,000
Management and System Documentation	$124,300	1	$124,300
TOTAL (w/o contingency)			$1,455,600

A complete WBS based cost estimate is given in [6] .

Acknowledgments.

We would like to thank Roger Rusack and Patrick LeDu for reading an early draft of this document and checking it for consistency with the requirements of the ADC Shower-Maximum system.

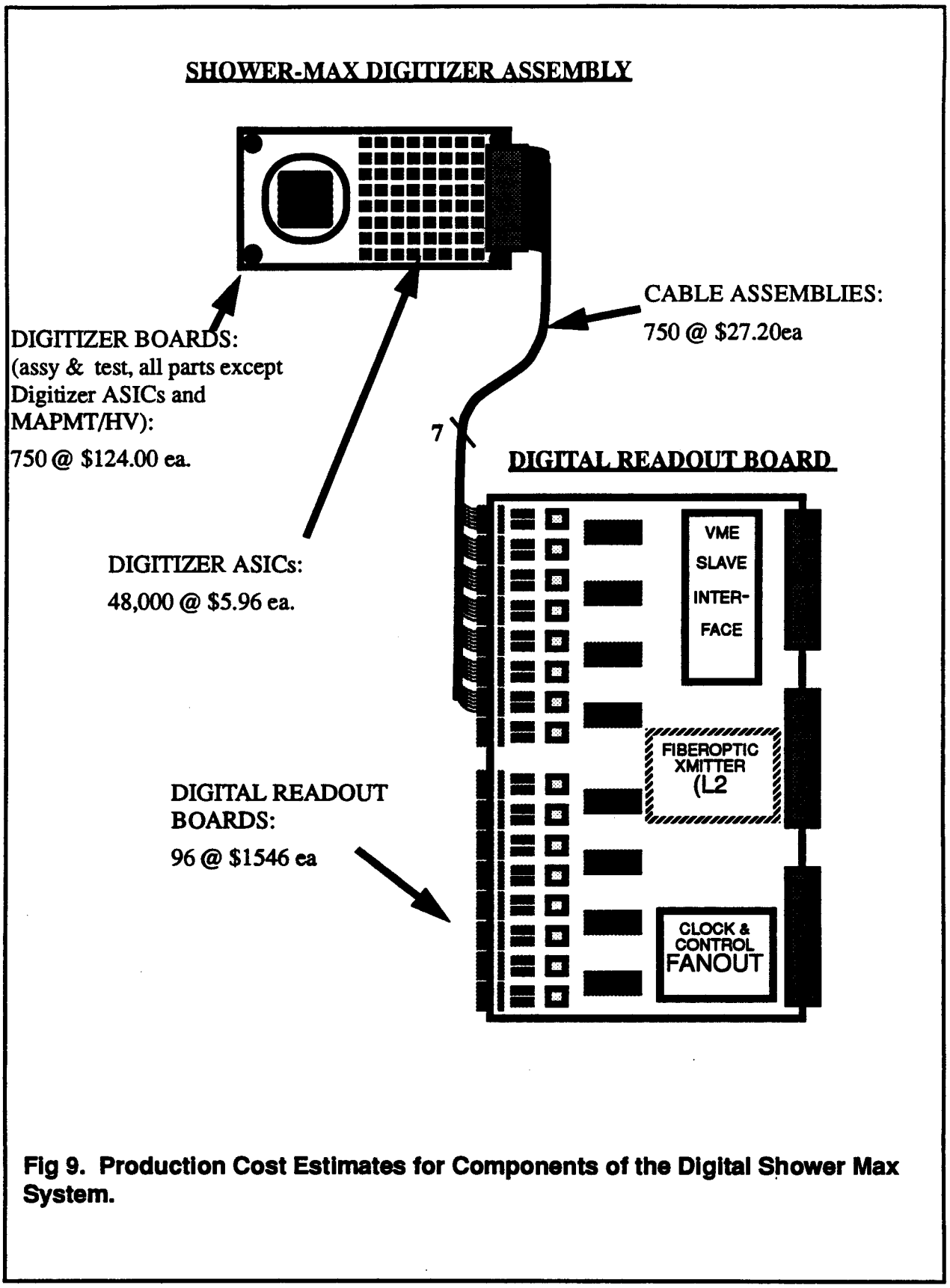


Fig 9. Production Cost Estimates for Components of the Digital Shower Max System.

REFERENCES

[1] "SDC TECHNICAL DESIGN REPORT", SDC-92-201, Solenoidal Detector Collaboration, 1 April 1992.

[2] " CALORIMETER CONCEPTUAL DESIGN: TILE/FIBER SCINTILLATOR OPTION", SDC Tile/fiber Calorimeter Group, Sept 3,1991.

[3] "BASELINE IMPLEMENTATION OF THE DIGITAL PHOTOTUBE READOUT SYSTEM FOR THE SDC CALORIMETER", SDC note SDC-92-306, Sept 15, 1991, Revised 27 Aug 1992.

[4] "CALIBRATION OF THE DIGITAL READOUT SYSTEM FOR THE SDC CALORIMETER", W. Foster, J. Hoff, M. Sarraj, R.J. Yarema, T.Zimmerman, SDC note SDC-92-307, 27 Aug 1992.

[5] "A PIPELINED MULTIRANGING INTEGRATOR AND ENCODER ASIC FOR FAST DIGITIZATION OF PHOTOMULTIPLIER SIGNALS", R.J. Yarema, W. Foster, J. Hoff, M. Sarraj,T.Zimmerman, Proc. 2nd Annual Conference on Electronics for Future Colliders, Chestnut Ridge, NY May19-21 1992.

[6] "WBS DICTIONARY AND COST/SCHEDULE BREAKDOWN FOR DIGITAL CALORIMETRY READOUT OPTION FOR THE SDC", Ray Yarema, Feb 14 1992; updated Aug 1992.

[7] "BEAM TESTS OF THE DIGITAL PMT READOUT SYSTEM", G.W. Foster and R. Tschirhart, (in preparation).

[8] "PMT DIGITIZER CURRENT SPLITTER VERSION 1 TEST RESULTS", FNAL technical note, T. Zimmerman, Jan 14,1992.

[9] "PMT DIGITIZER CURRENT SPLITTER VERSION 2 TEST RESULTS", FNAL technical note, T. Zimmerman, March 31,1992.

[10] "PMT RANGE ENCODER AND INTGRATOR CONTROL [Version 3] TEST CHIP", M. Sarraj, FNAL technical note, 17 July1992.

[11] "THE SIRO CHIP", Jim Hoff, FNAL Technical Note, Dec. 1990; "SIRO TESTS", J.Hoff, (undated).

[12] C. Blocker, presentation at the SDC Calorimetry Group meeting, Aug 3 1992.

[13] "THE CONCEPTUAL DESIGN OF THE SDC TRIGGER", the SDC Trigger Group, Aug. 27, 1991; THE SDC GLOBAL LEVEL 1 PROCESSOR, Preliminary Draft, Wesley H. Smith, March 14, 1991.

[14] V. Barnes, Ft. Worth SSC Symposium, 1990.

[15] Cockroft-Walton Phototube HV Supply, L. Mo et. al.

[16] "A HV RESONANT CONVERTER FOR PHOTOMULTIPLIER TUBE BASES", G. W. Foster, S.Hansen,C.Rivetta June 1992.

[17] "TEST OF DIGITAL TRANSMISSION CHARACTERISTICS OF 0.025" PITCH FLAT CABLES", M. Haldeman, R. Yarema, FNAL Technical Note, Jan 23,1989.