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CALIBRATION OF THE DIGITAL READOUT SYSTEM FOR THE SDC CALORIMETER

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INTRODUCTION

This document describes the circuitry and procedures for calibration of the Digital Phototube Readout System[2] [4] for the SDC Calorimeter and Digital Readout of the Shower-Maximum detectors [3] . Some test results from Digitizer ASICs which are relevant to calibration issues are discussed.

In this system, the phototube signals are digitized immediately at the base of each photodetector. The digitized information is transmitted to the trigger and stored locally during the trigger decision time. The analog components associated with all calibration functions are contained in the single assembly containing the Photomultiplier, Base, and Digitization ICs. Most calibration components are built into the front-end ASICs.

Both the Shower-Maximum detectors and the main Photomultiplier tubes of the calorimeter share the same calibration procedures, although the accuracy requirements of the Shower-Max detectors are considerably relaxed. In the Shower-Maximum detector of the SDC baseline design, the phototransducer is a 64-channel multi-anode PM tube (MAPMT). A readout based on Avalanche Photodiodes (APDs) is also under consideration. The Digital readout system will work equally well with APDs. This document assumes MAPMT readout for the Shower Maximum detector.

CALIBRATION STRATEGY

The calibration strategy for the SDC calorimeter is outlined in section 6.8 of the SDC Technical Design Proposal [1] . The main components are as follows:

1) A ***Source Calibration*** using the DC Phototube current from radioactive sources which move throughout the calorimeter. This will be used to set the initial energy scale (phototube gains) to an accuracy of ~2%. It will also be used for quality assurance during manufacturing to ensure longitudinal uniformity of response, as well as to monitor the depth profile of radiation damage in the calorimeter. The main electronics requirement for the source calibration circuit is that the DC currents from the PMTs can be

accurately correlated with the charge gains of the fast pulse digitization. In the Digital Readout system, the source current measurement circuitry is built into the front end ASICs.

2) An ***In Situ Calibration*** which uses colliding-beam data to set the energy scale of the calorimeter to an accuracy of a fraction of 1%. For the main calorimeter PMTs, this uses electron tracks measured in the tracking chambers as well as constraints from the Z^0 mass, etc. For the Shower-Maximum Detector, the final calibration will be obtained by comparison of the shower-max "strip" energies with those of the calorimeter towers containing the strip hits. These *in situ* calibrations consist primarily of fine-tuning the energy scales of individual towers. They are "offline" techniques which require only a linearized response, and a reasonable first estimate of the energy scale.

3) An ***Optical Flasher Calibration*** system is the major tool for establishing the linearity of the overall system. It is capable of measuring photomultiplier space-charge saturation which is expected to be the dominant nonlinearity in the system. This system is not useful for establishing the energy scale of calorimeter channels due to the difficulty in ensuring a precise optical coupling to individual phototubes.

4) An internal ***Charge Injection System*** is included to provide a convenient way of testing and calibrating the electronics. This capability is partially redundant with the optical flasher system. It provides a low-noise means of injecting test pulses into the DAQ and trigger system, a convenient way to establish scale overlaps, check for missing codes in ADCs, etc. in a way which does not depend on PMTs and HV. In the Digital Readout system, the charge injection circuitry is almost entirely built into the front end ASICs.

5) A ***Trigger Calibration System*** is not needed in the Digital PMT readout system. Normally, this consists of a series of analog components which inject (a series of) test pulses into the trigger digitization path. Instead, the Digital Readout System provides the ability to download digital test patterns (and Monte Carlo events if desired) directly to the digitizer ASICs. These test patterns allow exhaustive, full-speed testing of the trigger/DAQ system, measurement of the bit-error rates on the optical fibers of the trigger outputs, etc.

6) ***Gate Timing Calibration Procedures*** are essential to obtaining desired resolution from the SDC calorimeter. The Digital Readout System has the ability to adjust the gate positions on individual channels to an accuracy of +/- 0.5ns. Test Beam data using the Digital Readout ASICs (with a realistic tile/fiber calorimeter module and six-stage phototube) indicate that the time structure of the signal from a single minimum-ionizing muon is clearly resolved in this system. This allows cosmic-ray muons to be used to

establish the initial gate timings to an accuracy of <1nsec prior to the start of colliding beams.

RADIOACTIVE SOURCE CALIBRATION SYSTEM

The goal of this system is to relate the DC current observed from a moving radioactive source [14] to the charge gain for calorimeter pulses. The overall accuracy goal for this measurement is 2% RMS [1] . The desired accuracy of the electronics component of this measurement should be 1% or better.

The magnitude of the source current to be measured is ~10nA, assuming a 1mCurie source, a PMT gain of $5x10^3$, and a calorimeter light yield of 200 PE/GeV. These currents are a factor of ~20 below those measured by CDF and Zeus, so the problem is nontrivial. The measured dark currents for an "SDC Spec" phototube (Hamamatsu R5329) operated at this gain are in the range of 0.01-0.02nA [15] .

The conventional solution to this problem (Fig. 1) is to measure the DC current by developing a voltage across a high-valued resistor, and separately measure the AC gain of the pulse integrator/shaper/digitization path by charge injection with a known capacitance. In the SDC application, several problems arise with this conventional approach:

(i) The smallness of the source currents to be measured yield very large resistor values: e.g. a gain of 1V/nA requires $R_{FB} = 10^9$ Ohms +/- 0.5%. Such resistors tend to be unwieldy, expensive, unstable, sensitive to handling, etc.

(ii) At the fast shaping times required at the SSC, the effective gain of the AC shaping network is very pulse-shape dependent. Care must be taken to ensure that the charge-injection pulse accurately reflects the signal characteristics of the PMT input pulse.

(iii) There is considerable difficulty in obtaining 0.5% accuracy in the small capacitors (10-100pf) required for charge injection and integrator feedback. The absolute accuracy (not just the matching) of these capacitances is important, since the DC currents are being measured by a separate resistor.

(iv) The separate digitization path for the "slow" measurement of DC currents introduces potential measurement errors due to mismatching of the ADC gains for "slow" and "fast" digitization.

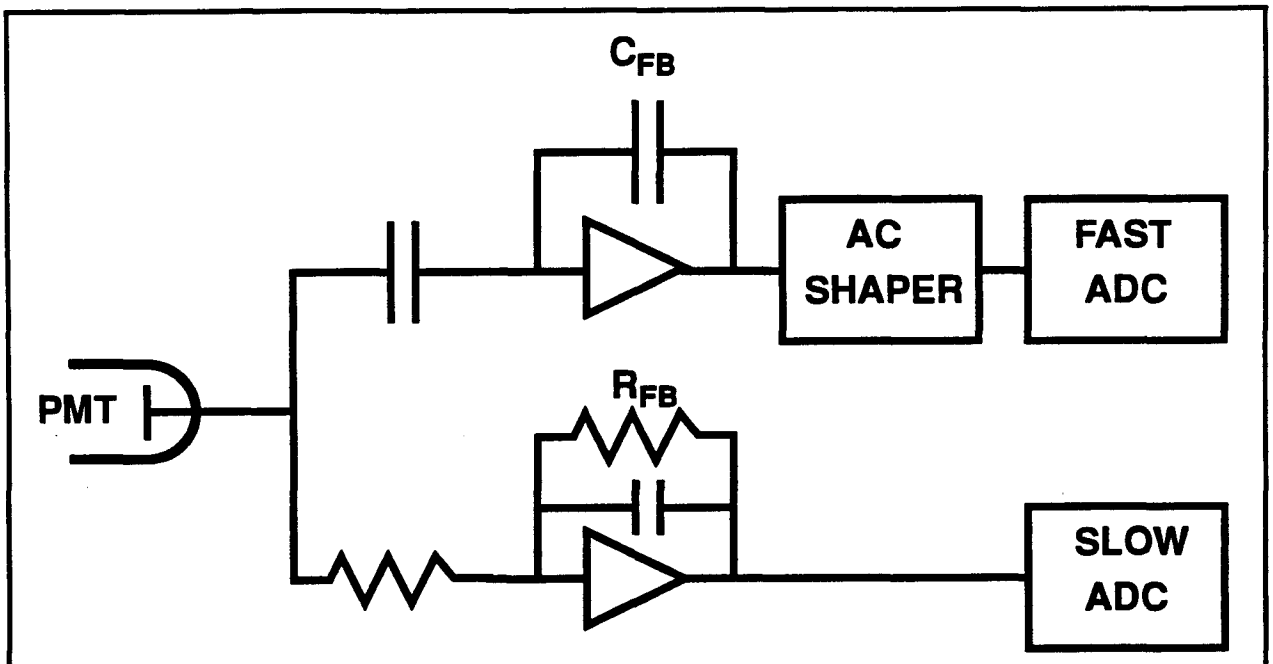

Fig. 1. The conventional solution to DC current measurements. Accuracy depends on high-valued resistors, low-valued capacitors, and the AC gain of the shaper circuit.

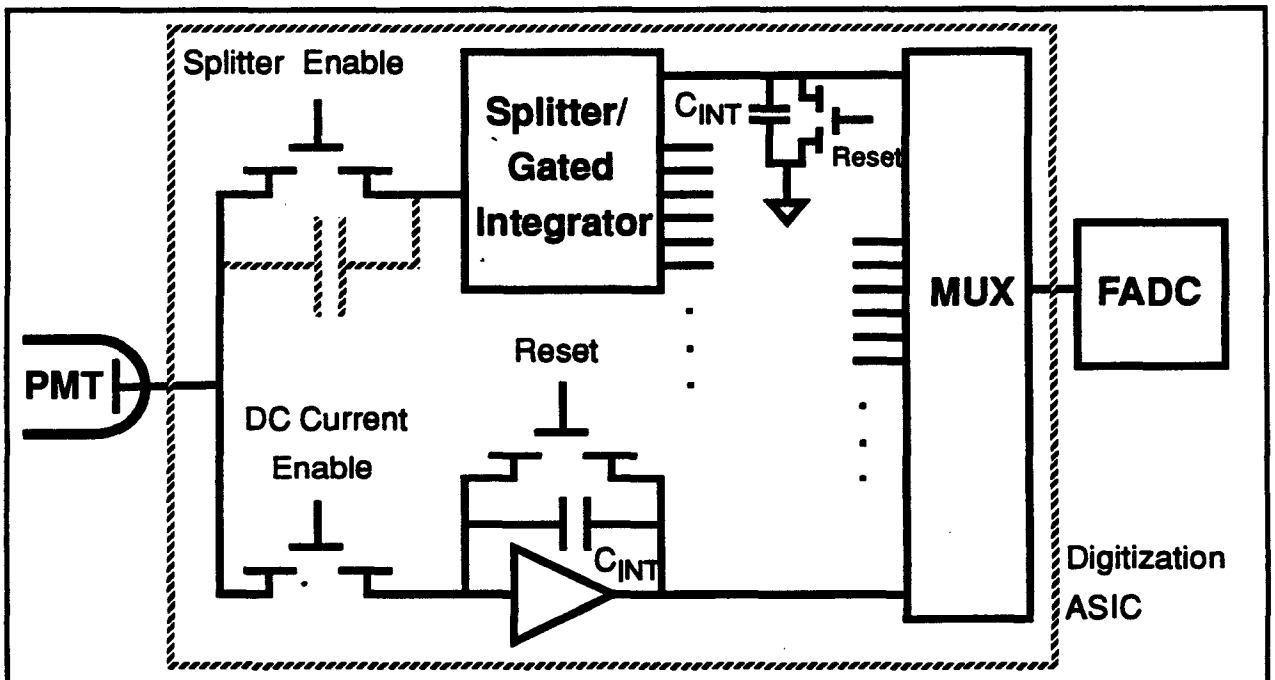

Fig. 2. DC current measurements in the Digital PMT System. Both DC and pulse current measurements are made with DC-coupled, resetable integrators. On-chip capacitors ensure <0.5% matching between functions.

DC Current Measurement in the Digital Readout System (fig. 2) avoids these problems by performing the current measurement using on-chip capacitors matched to those of the gated integrators. Both the gated integrator and the source current measurement are DC-coupled, resetable integrators. An FET switch at the input commutates between the two operating modes. No precision external high-valued resistors or low-valued capacitors are required. The ON resistance of the FET switch is noncritical since the switch which passes the fast PMT pulses is capacitively bypassed (see fig.2) to ensure good dynamic response.

The DC current measurements are performed by measuring the slew rate of the integrator by repeatedly digitizing it with the FADC. By varying the rate at which the integrator output is sampled (and reset), a very wide dynamic range (~10pa to 10uA) can be achieved.

Almost all sources of error cancel in the measurement of (DC Source current) / (Pulsed Beam current). The absolute values of the on-chip capacitors are not critical, and only the matching is important. Matching of on-chip capacitors is in the range +/-0.1-0.2%, and the absolute accuracy and temperature stability of the current splitter has been measured to be ~0.7% over the operating temperature range [7]. Integrator offsets are irrelevant since only the charging rate of the integrator is used to determine the DC current. Finally, the same ADC is used for both digitizations, so that ADC gain variations cancel. We therefore expect that the accuracy of the DC/Pulse current comparison will be in the range of 0.5% RMS or better.

The accuracy of the DC/Pulse gain calibration can be verified by using the charge injection system (described below) to inject identical test pulses into both the DC current integrator and the gated integrator array. This provides a capability for improving the DC vs. Pulsed current calibration that does not exist in the conventional approach to current monitoring.

The incorporation of the source current measurement circuitry onto the front-end ASIC has other advantages. On-chip leakage currents are typically smaller than for equivalent circuits made with discrete components. (We have measured typical leakage currents of 0.1pA for a node with a few FETs and a ~1pf capacitor [10]). Finally, an integrated approach has fewer components and is simpler and cheaper than one based on discrete components [5].

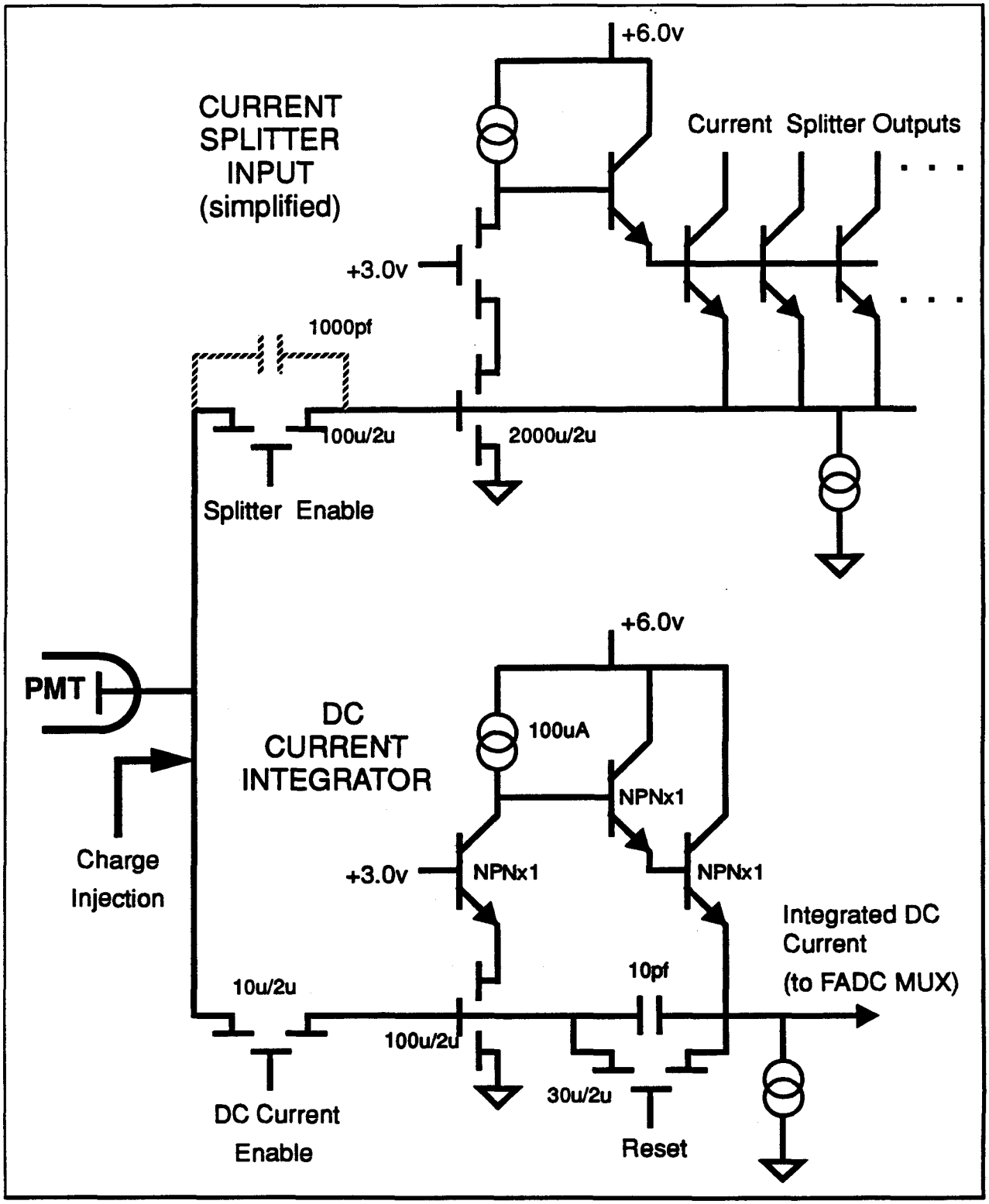

Fig 3. Device-level circuit diagram for DC source-current measurement. The 1000pf cap is off-chip.

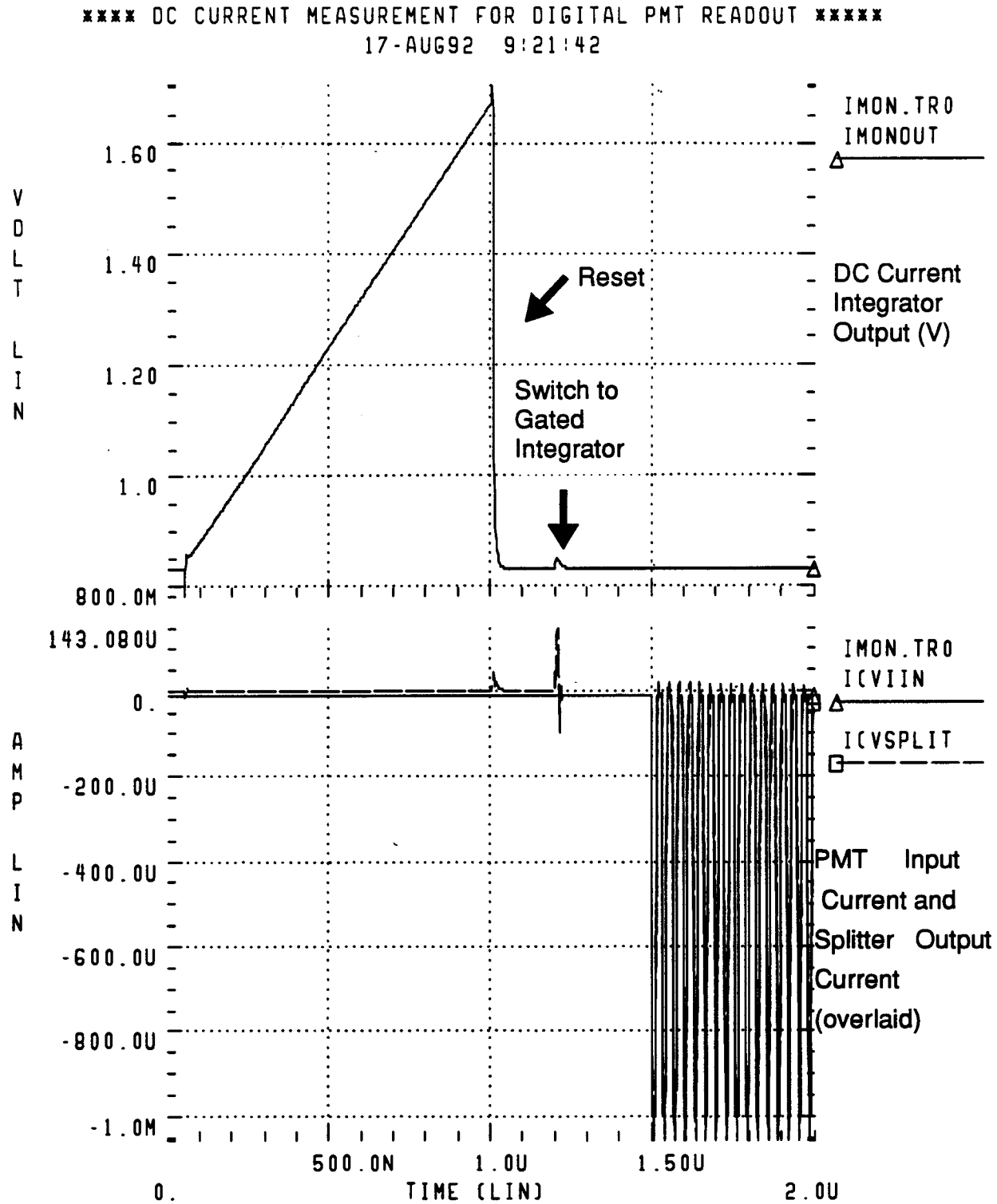

Fig. 4. HSpice simulation of the charge measurement circuit shown in fig. 3. The simulation shows correct operation of the DC current integrator, the commutation of the FET switches to change the circuit into pulse mode, and correct operation of the current splitter for a train of 100 GeV pulses every 32ns. The PMT output and the current splitter output current are overlaid in the bottom trace. No degradation of the splitter's accuracy or DC coupling is observed.

OPTICAL FLASHER CALIBRATION SYSTEM

The SDC will have an optical flasher calibration system similar to systems used by CDF, Zeus, and other large PMT-based experiments. These systems deliver an optical pulse to each PMT, with controlled characteristics and pulse shape similar to that of the calorimeter. The optical pulse is typically produced by N_2 laser illumination of a sample of scintillator/ waveshifter of the same type used in the calorimeter. The pulse is fanned out and delivered to the PMTs via optical fibers. The pulse height can be controlled over many orders of magnitude by suitable optical attenuators. Pulse height is monitored on a pulse-by-pulse basis by a PIN diode which remains linear over >6 decades.

Fig. 5 represents data taken with the Digital PMT Readout ASICs using the flasher calibration system at the Fermilab Photomultiplier Test Facility [12] . It is a scatterplot of the pulse height observed on a single scale of the PMT Digitizer ASIC, against the pulse height observed with the PIN diode used to monitor the optical pulse. The pulse height correlation is 1-2%, so that a few hundred triggers will be necessary to measure PMT + Digitizer nonlinearities to the required (8-9 bit) accuracy on each scale. The maximum output pulse rates for N_2 lasers are typically 100-500Hz, so we expect that the entire dynamic range of the digitizer can be calibrated in 1-2 minutes.

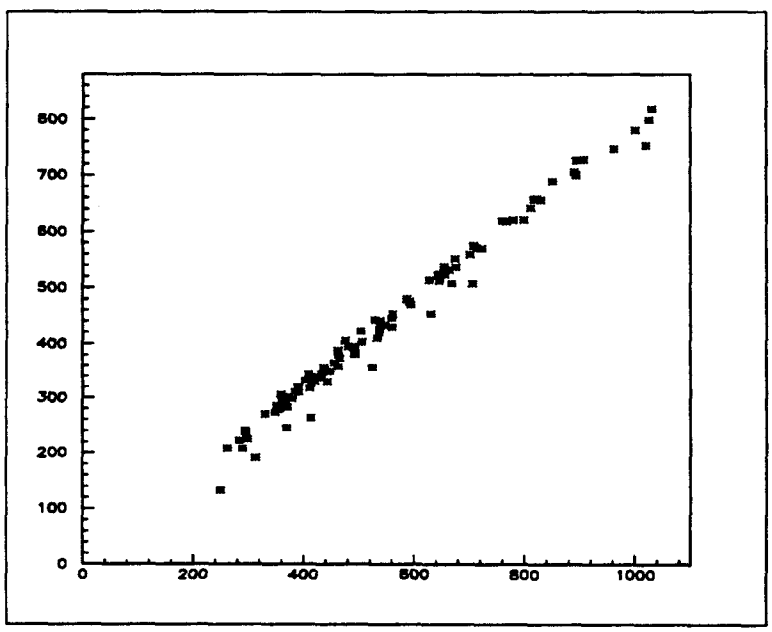

Fig. 5. Laser Flasher data taken with the Digital PMT Readout ASIC test board at the Fermilab Photomultiplier Test Facility [12]. X-axis: PIN photodiode monitor of laser output; Y-axis: charge measured by PMT/Digitizer.

CHARGE-INJECTION CALIBRATION SYSTEM

This system (fig. 7) provides the capability of injecting a known amount of charge into the front-end of the digitizer ASIC. It does so by charging a known capacitor to a known voltage, then using an FET switch to discharge it into the input node of the PMT Digitizer ASIC.

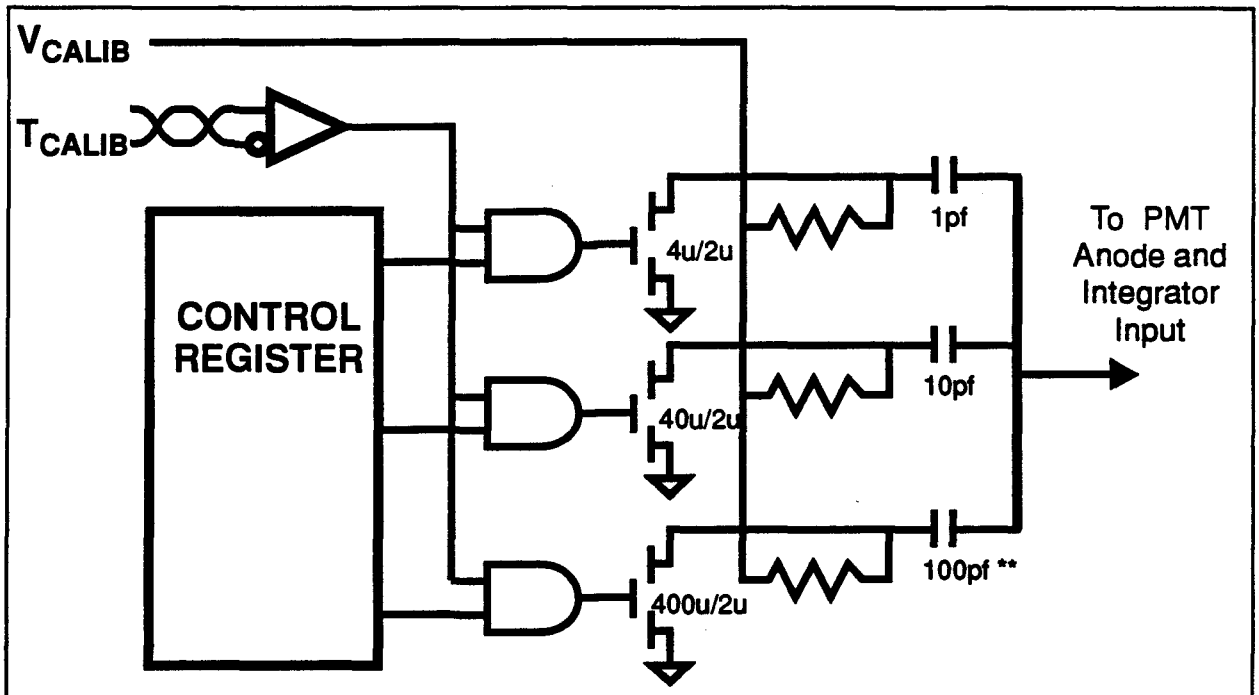

Fig. 7. Charge injection circuitry on the front-end digitizer ASIC. Pulse height is determined by an external DC voltage V_{CALIB} which determines the initial voltage on the charge-injection capacitors. Timing of the injected pulse comes from a low-level differential logic signal T_{CALIB} which is fanned out from the Readout Crate. A programmable register on the ASIC selects one of three charge injection ranges to pulse. *The 100pf injection capacitor is not needed on the Shower-Maximum system.

The pulse height of the charge injection is determined by a computer-controlled DC voltage which is generated on the readout card and distributed to the PMT/Digitizer modules.

The timing of the injected pulse is determined by a low-level differential logic signal (~0.7v P-P and ~2ns rise time) which is fanned out from the "VME" Digital readout cards to the flat cables to each digitizer module. We have successfully used these signaling levels for clock distribution in our ASIC test module, which achieved noise levels of 2fC in a test beam environment. We therefore do not anticipate noise problems from the digital calibration timing signals. The differential line receiver subcircuit [4] [9]

which receives the calibration pulse has a 2ns propagation delay and was also used successfully in the Digitizer ASIC in the test beam.

Three charge injection scales are needed to cover the full dynamic range of the gated integrator. The DC voltage is distributed as a +/- 5v signal with a least count of 1mv. The coupling capacitors on the scales are 100pf, 10pf, and 1pf. The largest pulse which can be injected is 100pf x 10V =1nC, and the smallest resolvable charge increment is 1pf x 1mV = 1fC. This matches the 20-bit dynamic range of the gated integrator ASIC.

The FETs which produce the calibration pulse, as well as the control logic which determines which of the charge-injection scales to fire, are located on the Digitization ASIC. The capacitors used for charge injection can be either inside or outside of the Digitizer ASIC. External capacitors have the advantage of more accurate absolute calibration. Internal capacitors have the advantage of lower complexity and cost, as well as better matching relative the Gated Integrator capacitors. At present, we plan an external capacitor for the 100pf scale, and internal capacitors on the 10pf and 1pf scales. For the Shower-max version of the Digitizer ASIC, full scale is only 60pC and the 100pf capacitor is absent.

A nontrivial problem which must be addressed in the charge injection circuit is to avoid loading down the input node with excess capacitance from the charge-injection circuit. Without the charge injection circuit, the PMT anode, base, digitizer ASIC and board assembly have ~10pf total input capacitance. Degradation in circuit performance becomes noticeable above ~30pf. This potentially complicates the design of the 100pf charge-injection scale. Fortunately, the off-state capacitance of the FET switch appears in series with the 100pf capacitor. The FET size (400u/2u) is chosen to give a discharge time constant of ~3ns on the 100pf capacitor. The effective off-state capacitance of this FET is ~0.2pf, so that the calibration circuit does not appreciably contribute to the input capacitance.

CALIBRATION OF THE RANGES OF THE DIGITIZATION ASIC

The PMT Digitization ASIC performs charge measurement on ~10 binary-weighted scales. As will be described below, a piecewise-linear calibration of the device (one slope and one offset constant for each scale) is sufficient over the entire dynamic range of the system. Measurements of the Gated Integrator/ Current Splitter ASICs indicate that the uncorrected accuracy of the device will be in the range of 1%. This uncorrected accuracy is adequate for the Shower-maximum detector, which will then require only

overall phototube gain and pedestal constants for each channel.

Gated Integrator Linearity

Figs. 8a-c. (from refs. [4] and [8]) show the measured nonlinearity of a single scale on the Current Splitter/Gated Integrator ASIC. The RMS residual to the best fit line is 80 parts per million -- adequate for 13-bit linearity. The AC accuracy is not yet measured. However, since we require only 8-9 bit accuracy on each scale, it is likely that no nonlinear correction from the gated integrator will be required on any scale.

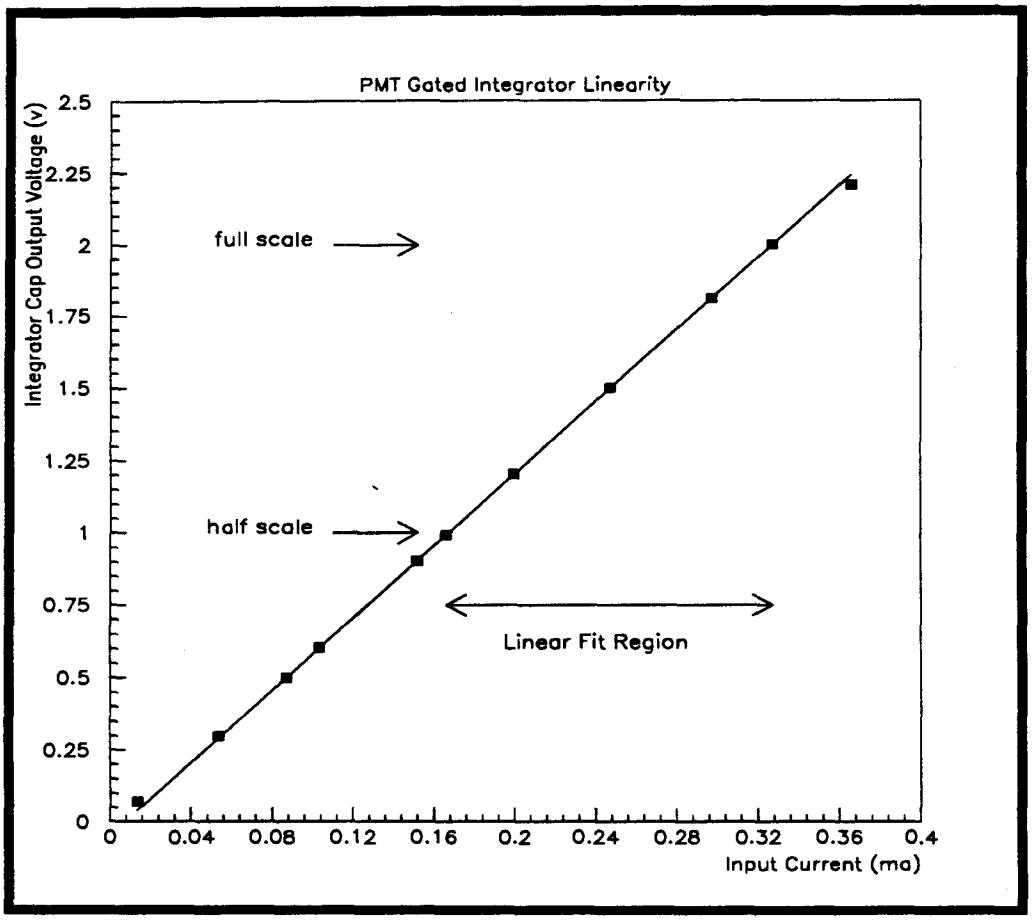

Fig. 8a. Linearity measurements of the I/2 scale of the Current Splitter / Gated Integrator test chip. The final capacitor voltage is plotted as a function of the DC current injected into the input, for a fixed 16ns gate time. Linearity is relevant in the output range between 1/2 and full scale, since it is only over this range that the integrator output is sent to the FADC.

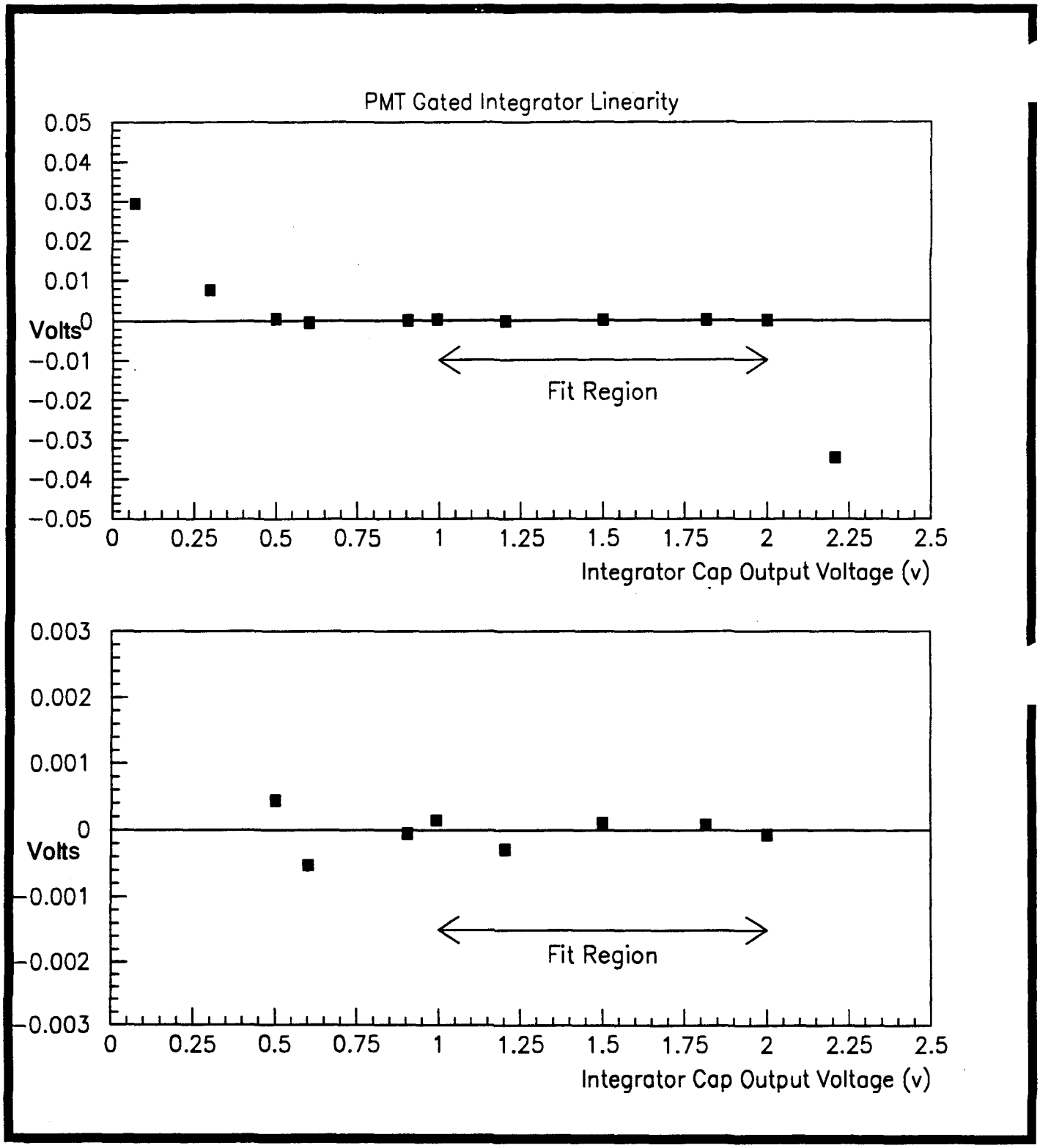

Fig. 8b,8c. Measured nonlinearity (fit residuals) for the Current Splitter / Gated Integrator test ASIC, on two different scales. In the region between 1/2 and Full scale where the integrator output is digitized and the linearity is important, the RMS deviation from the best fit line was 83 parts per million of the 2v full scale of the Gated Integrator. This accuracy exceeds that required for a desir based on either an 8 or 10 bit FADC.

Accuracy and Temperature Stability of the Current Splitter

The absolute accuracy of the current split into each of the binary-weighted scales is not critical since each scale is independently calibrated. The major concern is that large differences in the slopes and offsets of individual scales might necessitate increasing the voltage range on the FADC ladder, which would result in a slightly less efficient use of the FADC dynamic range.

Measurements of the accuracy of the current splitter are described in [7] and [8] . The overall accuracy was within <1% in all cases tested. This exceeds our requirements.

Temperature stability is important. Measurements on the splitter ASIC described in [7] indicate that the ratios of the binary current split are stable +/-0.5% over a temperature swing of 35 degrees C. Over a realistic range of operating temperature the splitter can be expected to maintain better than 0.1% stability.

Other Possible Sources of Nonlinearities and Offsets

Nonlinear corrections of order 1-2% may arise due to nonuniformity in depth in the sampling of a calorimeter tower, or from space-charge current limiting in the PMT dynode chain. These are not associated with readout electronics and will occur in either Analog or Digital readout. For the PMTs under consideration (Hamamatsu R5329, Phillips XP1911, or similar), the nonlinearities occur primarily above 25ma output current (2.5 TeV). These nonlinearities [if they are significant] will have a soft enough energy dependence that they can be incorporated in the piecewise-linear calibration of the range scales of the Digitizer ASIC.

Typical FADCs have integral nonlinearity specifications of 0.5-1 LSBs, worst-case deviation over the entire FADC range. Our design uses an 8-bit FADC to measure gated integrator voltages between 1/2 and Full scale, so that each signal is digitized to an accuracy which varies between 1/256 and 1/512 of itself. Thus the effect of this (absolute worst-case) FADC nonlinearity varies between 0.5% and 0.25% of itself, and we anticipate a RMS nonlinearity below 0.1%. We are in the process of making these measurements.

Computer Time Required for Offline Calibration of the Digital PMT Data

One possible consideration is the amount of time taken to calibrate the data from the digital PMT readout. The Digital Readout data has 10 scales and a piecewise-linear calibration.

In order to evaluate this, a simple program loop was written which performs the

required calibration on an array of PMT energies in the format that they are generated by the Digitizer ASIC: a 4-bit range scale or "exponent" and an (8+1)bit "mantissa" from the FADC. The algorithm represents a worst-case situation in which all PMT data are fully calibrated before any zero-suppression takes place.

```
DO I = 1, 25000                    !loop over array of 25,000 PMT energies
  IDAT = PMTDAT(I)                 !get word containing PMT data
  ISCALE = ISHFT(IDAT,-8)          !get scale range bits for this word
  FADC  = IAND(IDAT, 255)          !get FADC data (mantissa) for this word
  ECAL(I) = FADC*SLOPE(ISCALE,I) + OFFSET(ISCALE,I)
ENDDO
```

This loop compiles into ~12 Vax instructions and would execute in ~400msec on a Vax-780 if we still had one around. This is negligible in relation to the CPU time budget for event processing in Level 3 of 100 Vax-seconds [1] .

Calibration Data Storage Requirements

Another consideration might be the offline storage requirements for calibration constants. The function of the offline calibration is to bring the accuracy of an uncalibrated PMT/Digitizer/calorimeter channel (with a full spread of ~2% in the uncalibrated nonlinearity) to a calibrated accuracy of sigma <0.2%. To obtain a concrete estimate of the calibration storage requirements, we assume the following procedures:

(1) The slope and offset information for each scale is stored as two 4-bit fields. Each field represents the deviation of the best-fit line from nominal linearity, evaluated at the scale endpoints and in units of 0.5 FADC counts. Thus, one byte is sufficient to hold the calibration/linearization information for a single scale.

(2) Each channel has an overall channel gain constant stored as a 16-bit integer.

The total storage required for calibration of each channel is then: (10 scales) x (1 byte/scale) + (2 byte gain constant) = 12 bytes/PMT. The shower-maximum system would not need item (1) since the uncorrected linearity will be more than adequate given the ~15% constant term in the

shower-max resolution. In addition, a single-byte gain constant will be adequate. Thus, the total storage required for calibration constants is:

	(47k Shower-max channels) x (1 byte / channel)
+	(27k Digital PMT channels) x (12 bytes/channel)
=	371 kbytes.

Thus, the hard disk on a desktop computer could store the constants from 5,000 calibration runs.

CALIBRATION OF GATE TIMING

Most people who have set up high rate experiments and/or tightly timed triggers have experienced the joy of hand-trimming cables from individual phototubes. The SDC Calorimeter and Shower-Maximum detectors will have channel-to-channel time slewing of several nsec due to time-of flight, scintillator tile size variation and waveshifting fiber length, photomultiplier transit times, cable lengths, electronics propagation delays, and time skewing in the gate/clock fanout.

For the shower-maximum detector the problem is exceptionally severe. There will be differences of a few nsec arising from differences in the length of optical fibers from different shower-maximum strips. Routing of the optical fibers to the multi-anode PMTs is a highly nontrivial engineering problem, and it is difficult to guarantee that the fiber lengths in all channels will be matched. Additional time slewing will arise in different channels of the Multi-anode Photomultiplier Tubes.

The Digital Readout System has the ability to adjust the gate positions on individual channels to an accuracy of +/- 0.5ns.This is accomplished with a digital delay selector on the clock. For the Shower-Maximum detector, the delay selector is located on the input buffer of each digitization ASIC. For the Digital PMT readout, it is located on the digital ASIC on the Readout Board. This system permits automated correction for cable lengths, time-of-flight, and propagation delays in the shower-max fiber optics, phototubes and electronics. Cable and fiber lengths can be set by convenience rather than necessity, and all hand-trimming is avoided. This ability to trim the gate timings of individual channels is another major operational advantage of the digital readout system.

Gate timing calibration procedures are essential to obtaining desired

resolution from the SDC calorimeter [13] . Ideally these procedures should be executable in beam-off conditions, e.g. using cosmic-ray muons. This requires that the time structure of the signal from a single minimum-ionizing muon be clearly resolved.

Fig 9a is a test-beam muon signal [6] taken with the Digital PMT Readout ASICs, using a realistic Tile/Fiber EM calorimeter module and six-stage phototube. The muon signal is clearly resolved above noise. Figure 9b gives the energy sharing between buckets, as a function of the beam particle timing with respect to the clock phase. An accuracy of <1nsec seems easily achievable. This measurement allows cosmic-ray muons to be used to establish the initial gate timings to an accuracy of <1nsec prior to the start of colliding beams.

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Fig. 9a. Test-beam muon signal [6] taken with the Digital PMT ASICs, using a realistic Tile/Fiber EM calorimeter module and six-stage phototube. Vertical scale is 2fc/count, horizontal resolution is 18ns/sample. The muon signal is clearly resolved above noise.

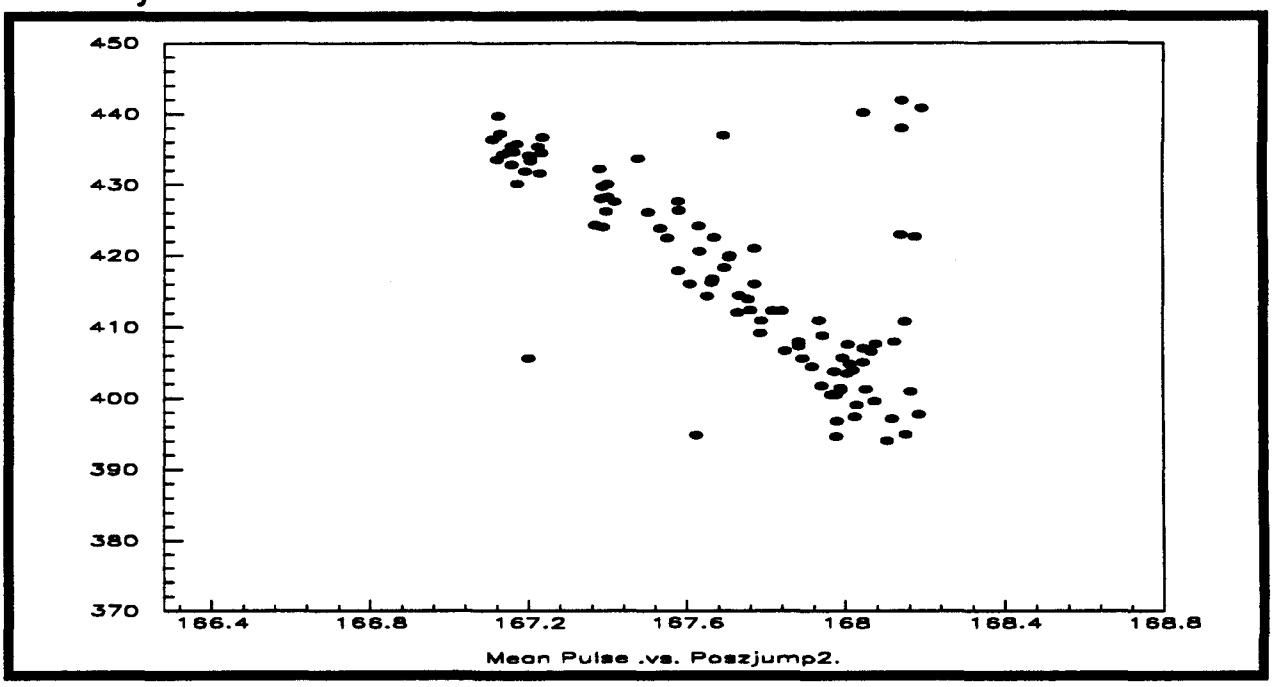

Fig. 9b. Time centroid of energy deposition in 18ns RF buckets, as a function of the test beam particle timing with respect to the clock phase. The correlation has a width of about 3ns. This distribution can be used to determine the relative T-zeros of individual channels to an accuracy of <1nsec.

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