SDC-92-306

SDC
SOLENOIDAL DETECTOR NOTES

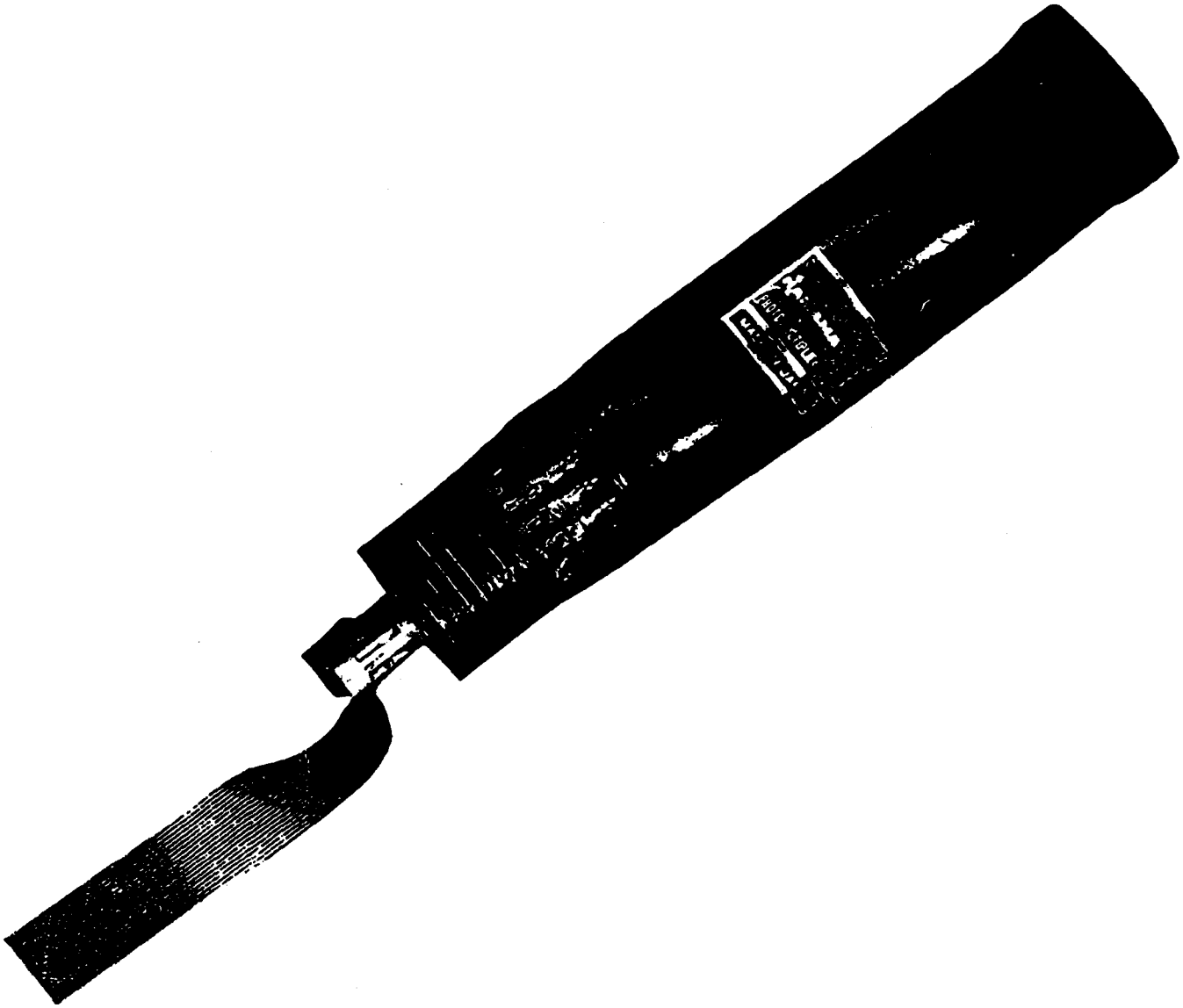
BASELINE IMPLEMENTATION OF THE DIGITAL PHOTOTUBE READOUT SYSTEM FOR THE SDC CALORIMETER

September 1991, Revised August 1992

Al Baumbaugh, G. William Foster, Sten Hansen, Jim Hoff,
Mark Larwill, Catherine Newman-Holmes, Claudio Rivetta,
Ray Yarema and Tom Zimmerman
Fermi National Accelerator Laboratory

BASELINE IMPLEMENTATION OF THE DIGITAL PHOTOTUBE READOUT SYSTEM FOR THE SDC CALORIMETER

Sept. 1991, revised August 1992



Al Baumbaugh, G. William Foster, Sten Hansen, Jim Hoff, Mark Larwill, Catherine Newman-Holmes, Claudio Rivetta, Ray Yarema, Tom Zimmerman

Fermi National Accelerator Laboratory

1. INTRODUCTION

This describes the system features and specifications for the "all-digital" photomultiplier (PMT) readout system for the SDC calorimeter [1] [2]. Related documents describe the Digital Readout of the Shower-Maximum Detector [3], the Calibration Procedures for the Digital Readout System [4], and test-beam results [7] using the Digital PMT readout system. A detailed description of the Digitization IC can be found in [5]. A complete WBS cost/ schedule for the system is given in [6]; this has only a summary of system costs.

The system has two components. See fig. 1.1. The first is a PMT HV Base/Digitizer module (fig. 1.2) which resides on the back of each tube. It provides the PMT high voltage via a Cockroft-Walton "charge pump". It also digitizes the PMT current in each 16ns interval, and outputs the digitized signal as a 12-bit floating-point number on a flat cable. The key component in this is a custom biCMOS IC which integrates and digitizes the PMT charge in conjunction with a commercial Flash ADC. This ASIC also contains calibration circuitry for charge-injection and measurement of DC currents from the phototubes.

The second component (fig. 1.3) is a digital readout/trigger card, located in crates mounted on the detector. In the SDC "baseline" design, it receives flat cables from 8 towers (18 PM tubes) and performs the necessary Trigger, Data Acquisition (DAQ), Calibration, and HV control functions. The same digitized data stream is used for both Trigger and DAQ purposes. This component is presently specified and cost-estimated as a 9U VME Slave card (fig 1.4) in an "SDC standard" crate located on the detector.

2. SYSTEM FEATURES

Digitization at the Phototube. Photomultiplier signals are fully digitized each crossing by a circuit mounted directly on the PMT base. All external signal processing is done digitally, and system noise problems associated with 60 MHz millivolt-level analog signal transmission are avoided.

All Digital Trigger and DAQ. No analog summations or thresholds are performed at any point. This permits complete full-speed testing of Trigger and DAQ systems prior to detector turn-on. The clock can be single-stepped to isolate and reproduce faults in the trigger and readout logic.

High Dynamic Range. The 12-bit floating-point output of the digitizer

COVER PHOTO: Mechanical model of PMT Base/digitizer used to test the manufacturing technique described in Section 5.

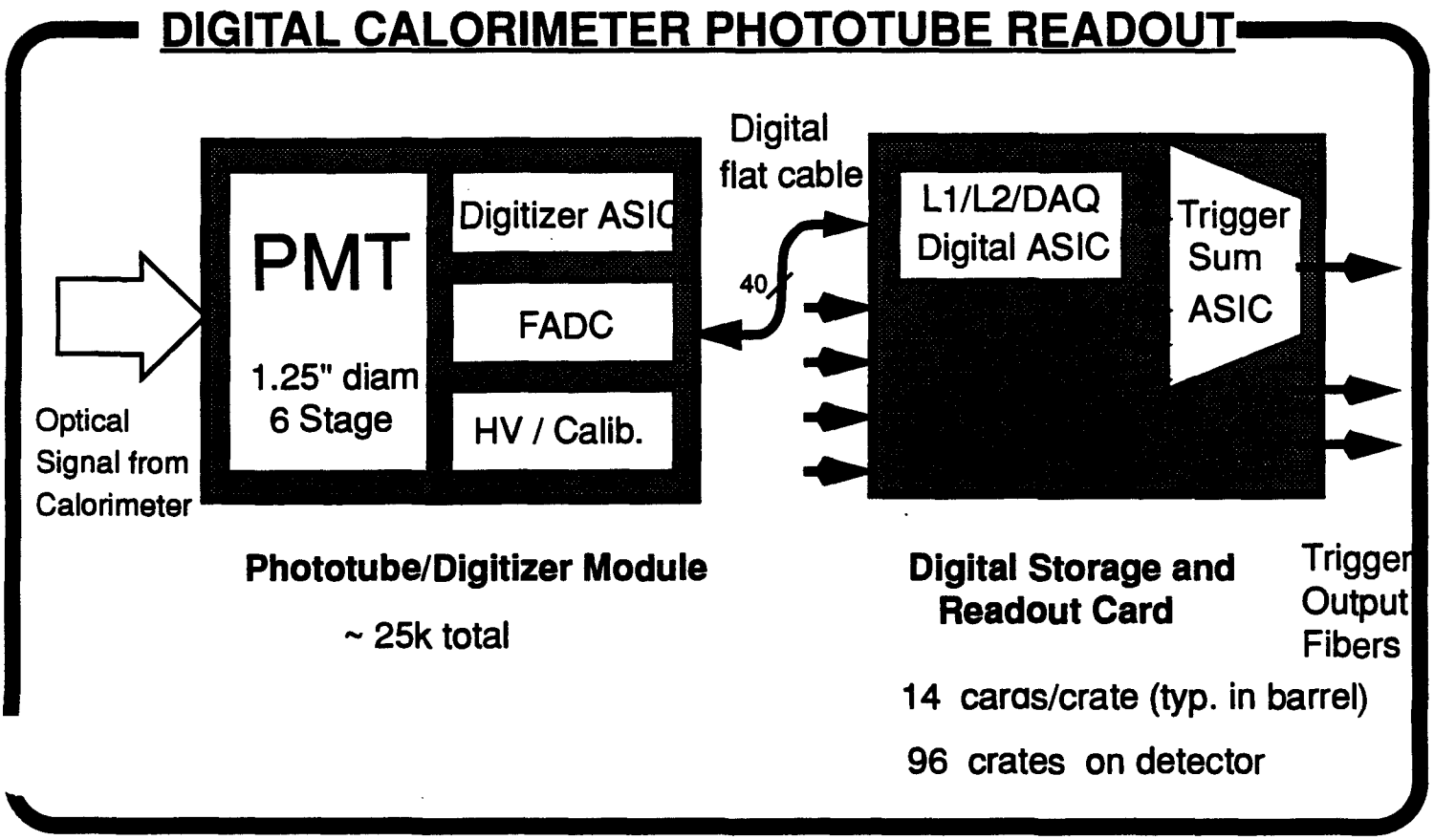


Fig. 1.1 - **SYSTEM BLOCK DIAGRAM.** There are two components in the system. The first component is the PMT Base/Digitizer assembly which contains the Phototube HV, Digitization, Current Monitoring and Calibration circuitry. These are connected via a flat cable to the second component, a card which contains the digital ICs which perform DAQ, Trigger, and calibration/monitoring functions. In the baseline trigger design [1] this card accepts flat cables from 8 towers of calorimetry and transmits energy sums for two "trigger towers" onto optical fibers to the trigger.

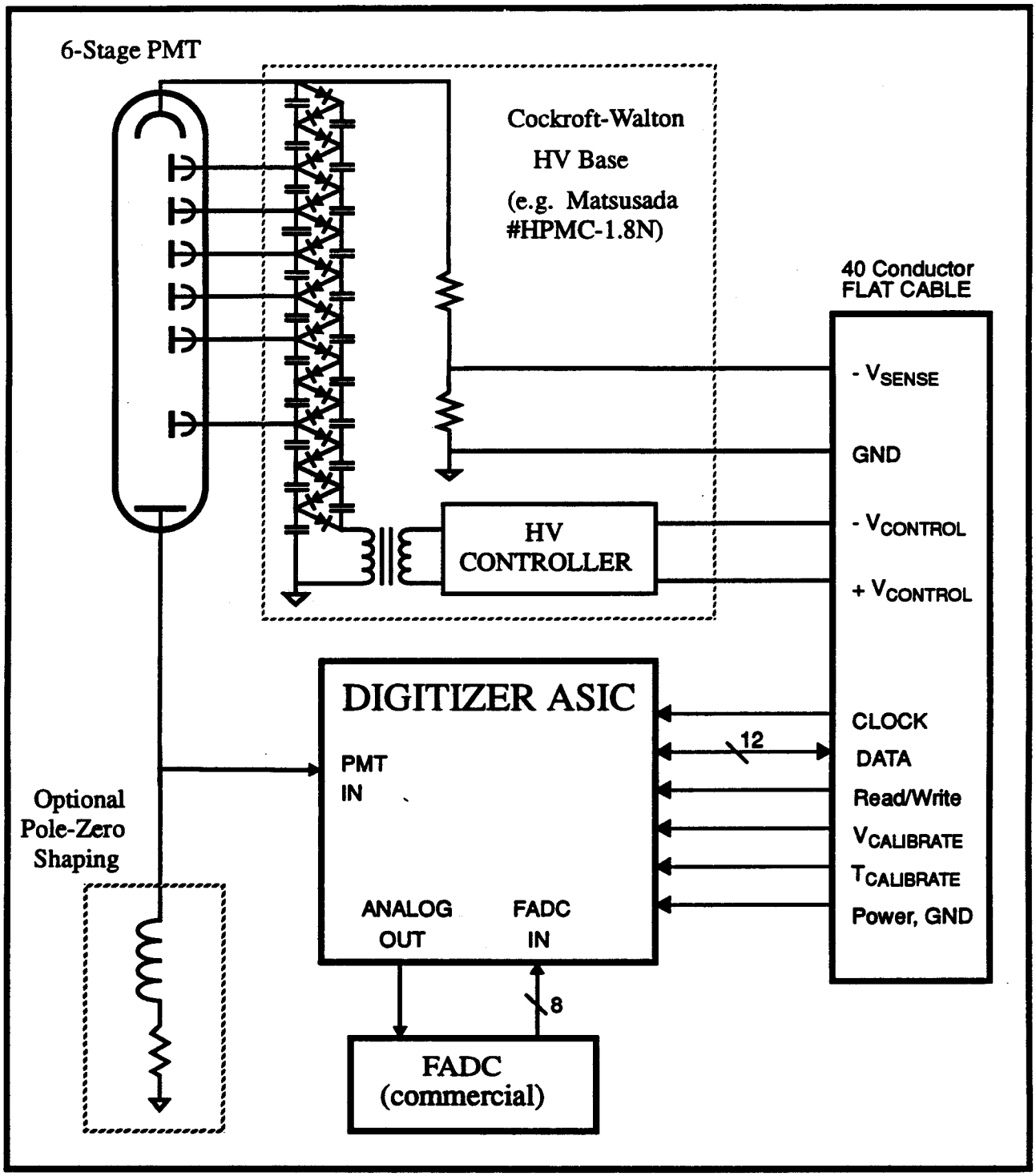


Fig. 1.2 **PMT BASE/DIGITIZER MODULE** circuit diagram. It contains the Phototube, Cockroft-Walton "charge pump" HV supply, HV monitor, PMT Digitizer ASIC, and 8-bit FADC. The PMT current monitor and Charge-Injection circuitry is built into the ASIC. A single flat cable connects to the readout board.

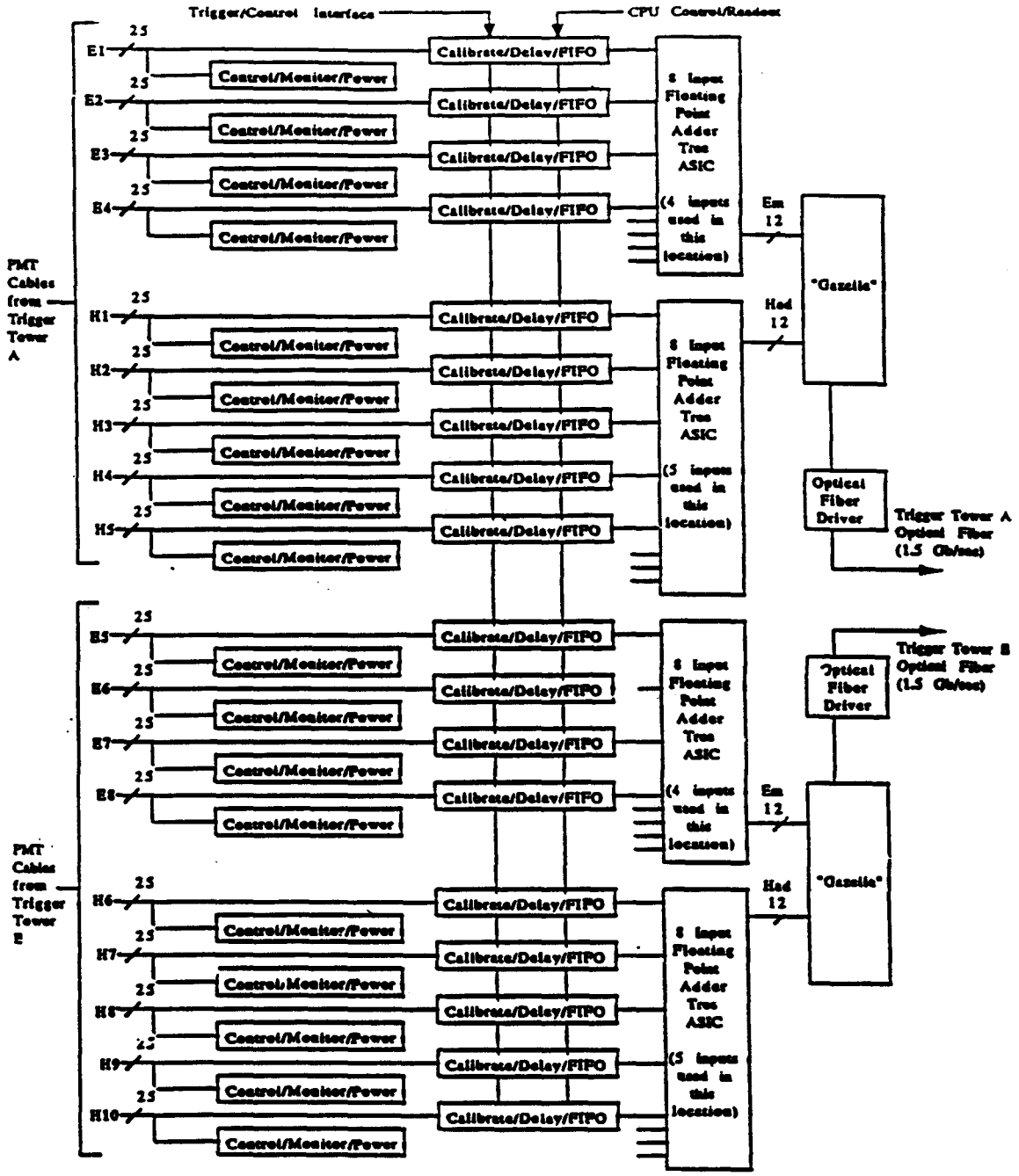


Fig. 1.3 READOUT BOARD BLOCK DIAGRAM. (Barrel Calorimeter Version). Each board has connects to eight calorimeter towers (18 Phototubes). HV Control, Monitor, Power, Calibration and DAQ functions are performed on a per-channel basis identically for all PM tubes. Trigger signals from 4 towers of calorimetry are summed into EM and HAD sums for two trigger towers. Trigger sums are formed digitally using the floating-point adder described in[12], and transmitted to the trigger by optical fibers.

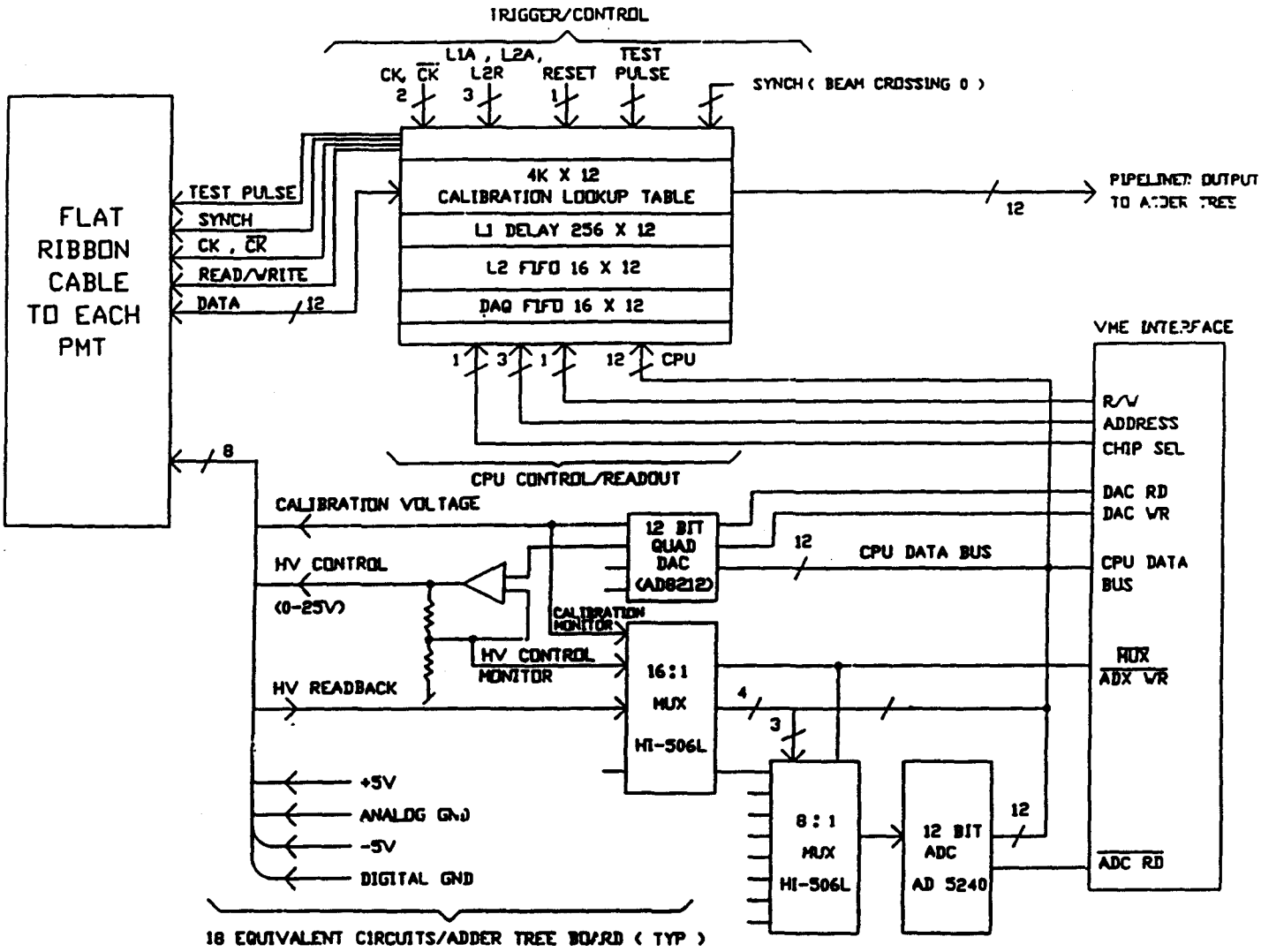


Fig. 1.3.1 CIRCUIT-PER-CHANNEL on Digital Readout Board.

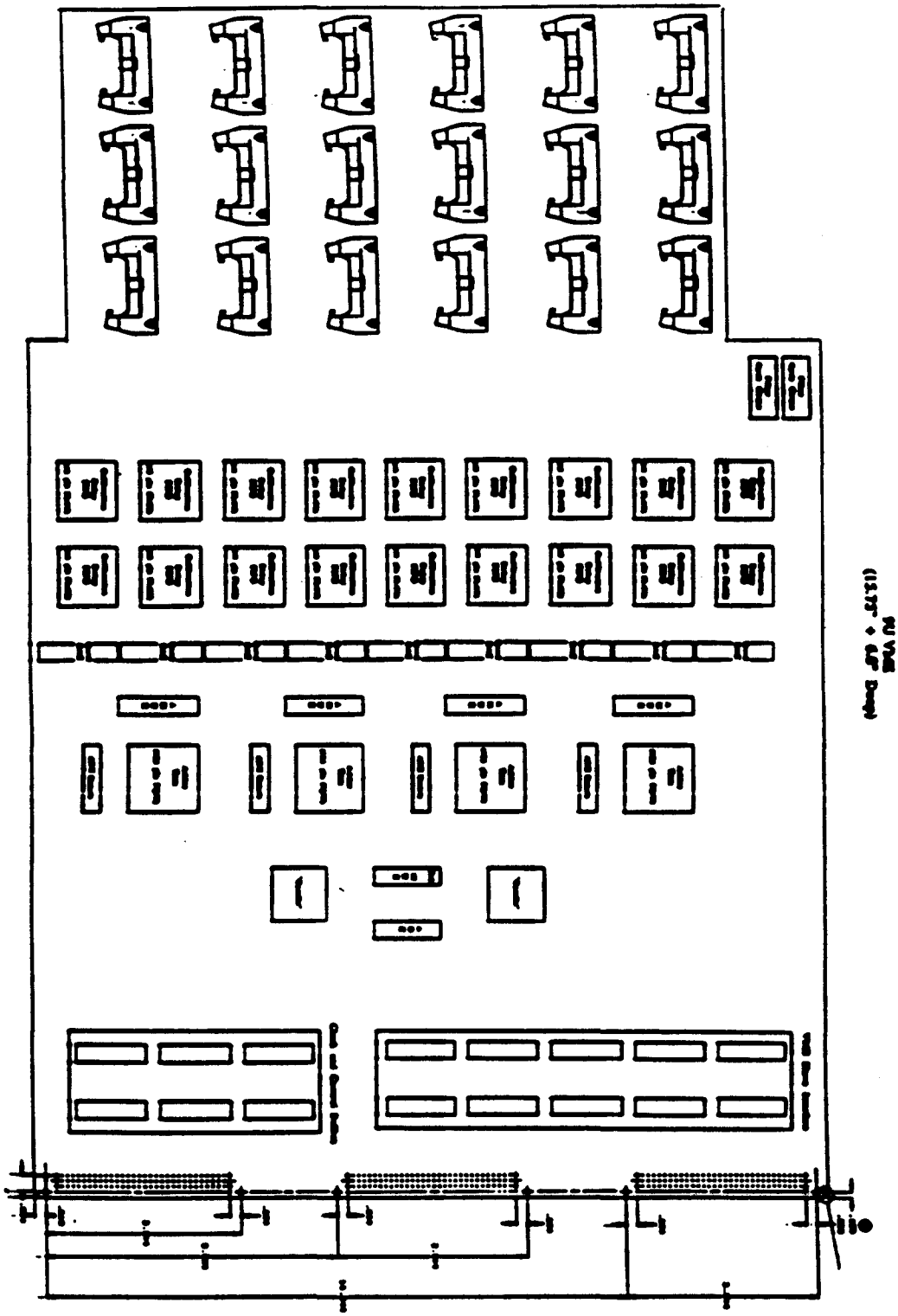


Fig. 1.4 READOUT BOARD PHYSICAL LAYOUT. In the baseline design these are "SDC Standard 9U VME" cards which communicate with the "Standard SDC Trigger Interface Board" on the P3 connector.

records the PMT charge with 8-9 bit accuracy over a nominal 20-bit dynamic range. This corresponds to a least count of 10 MeV (sufficient to put a muon signal in channel ~15) and a full scale of 10 TeV (a 1 TeV E_T deposition at the corner of the endcap calorimeter).

Integral PMT High Voltage System. The PMT Base/Digitizer assembly contains a Cockroft-Walton "charge-pump" HV supply for each tube. No exposed HV cabling occurs anywhere in the system.

Low Power. The power dissipation target for the PMT Base/Digitizer is 1w or less, including the HV supply and cable drivers. The power dissipation on the Digital Readout board is expected to be < 500mw/channel.

DC Coupling for High Rate Operation. The Photomultiplier is a DC-coupled device, and high-rate experiments are best off using DC-coupled systems. For this reason, our digitizer is implemented as a (set of) DC coupled "gated integrators" which directly integrate the PMT current for one crossing on a sampling capacitor. These capacitors are then digitized and reset in a pipelined manner during subsequent crossings. This results in a DC-coupled system with little or no memory of the energy depositions from previous crossings, no problems with saturation of input integrating amplifiers, etc.

Full Pipeline Diagnostics. Thousands of events stored in the front-end digital RAMs can be "played back" at full clock speed to verify trigger and DAQ performance. Additionally, the BiCMOS ASICs in the PMT digitizer allow a smaller number of events to be downloaded *directly into the PMT base*, allowing a full speed end-to-end check of the cabling, trigger, and DAQ.

Digital Storage for L1, L2, & DAQ. Information storage required during trigger decision latencies uses standard digital building blocks: RAMs, registers, FIFOs, and programmable logic. Test beam prototypes of these have been made using standard ICs, as well as VME boards using custom ICs. Custom ASICs for the final system can easily incorporate these as pre-assembled and debugged standard logic blocks, using design tools available from a variety of sources. Thus, the engineering costs and technical risk associated with these functions is much less than for analog schemes.

Long Pipeline Lengths Easily Accommodated. In the digital PMT readout system there are no inherent technological limits to the trigger Level 1 pipeline length, as occur in analog storage schemes. For digital storage, the cost of adding another crossing's delay is 12 RAM cells per chip (very small), and the power dissipation increase is negligible. If some future upgrade, or some unforeseen contingency, requires a longer pipeline length it can be easily accommodated in the Digital PMT Readout system.

Table 1: Specifications for the Digital Calorimeter Readout

Channel Count	20,736 (upgrade to ~30,000)
Photodetector	6-stage Photomultiplier tube (gain ~6000)
Digitizer Location	on base of Phototube
Cable from PMT	40 conductor flat cable, 0.025" pitch, integral ground shield, nonhalogenated. Carries signal, power, and HV control.
L1/L2 Storage Location	Readout Cards in Crates on Detector.
Readout Cards	14 Cards per Crate (typical for wedge in barrel)
DAQ Interface	"VME" block transfer slave on backplane
Time Resolution	16ns
Dynamic Range	20 bits
Least Count	10 MeV (1 fC)
Full Scale	10 TeV (1 nC)
Output Format	Digital Floating Point 4 bit Exponent 8+1 bit Mantissa
Accuracy	Signals Digitized to accuracy which varies between 1/256 and1/512 of itself. Digitization Sigma averages 0.1%
Peak Current from PMT	100ma x 10ns pulse (1nC)
Signal Rise Time	5-8ns
Crosstalk	< 1 LSB (10MeV) disturbance for full-scale hit in other PMTs in crate
Level 1 Trigger Output	12-bit Digital Floating Point Sums of PMT energies in 0.1 x 0.1 towers. Separate sums for EM and HAD energies.
Clock Gate Timing	+/- 0.5ns Programmable, Adjustment Individually Per Channel
High Voltage Supply	Cockroft-Walton on Base
Power/Channel	~ 1W on base + 0.5W on readout card

Trigger Energy Sum Outputs on Optical Fibers. In the SDC Baseline Trigger design, energies from 0.05 x 0.05 calorimeter towers are summed into "Trigger Towers" with 0.1x0.1 eta-phi granularity. The Electromagnetic (EM) and Hadronic (HAD) energies are summed separately. These are then transmitted to the global L1 trigger on optical fibers. In order to perform these energy sums, we have built and tested custom CMOS ICs which perform pipelined floating-point additions. These use the same floating point format (8+1 bit mantissa, 4-bit exponent) that is output by the PMT digitizer. In the baseline design, these circuits are used to form an 8:1 floating point adder tree to sum the energies from up to 8 PMTs in a "trigger tower". Other, more powerful, local digital triggers are possible.

Trigger Decision Based on the Same Information as Offline. Digitized PMT signals are passed through a pipelined calibration-lookup RAM table before being used in the Trigger and DAQ. This provides for arbitrary corrections for PMT gain, linearity, digitizer scale overlaps, E_T weighting, etc. It also allows the trigger decision to be based on the best set of calibrations known at the time the data is taken. All trigger sums are formed as 12-bit floating-point numbers, with the full precision (10 MeV least count, 10 TeV full scale) obtained from the PMT digitization. In the Digital PMT readout there is no separate source for low-precision "trigger data", hence no "trigger efficiency curves" to complicate offline analysis. The performance of the trigger can be exactly modeled in the Monte Carlo detector simulations. The trigger performance can be exactly verified, on an event by event basis, from the energies observed offline.

Built-in Phototube Current Monitor & Source Calibration System. The SDC scintillator calorimeter design [1] [2] provides a remote-controlled radioactive source which visits each tile in the calorimeter [25]. This current is measured by integrating amplifiers [4] in the digitizer ASICs, digitized by the same ADC which does the pulse digitization, and monitored by the CPU in the readout crate. This CPU also controls the source position via a commercial VME stepping-motor control board. This provides each wedge of calorimetry with a completely self-contained source calibration system.

Electronic (Charge-Injection) Calibration System. Each front-end ASIC has the ability to inject a calibration pulse [4] with an individually controlled amplitude and time of arrival. This charge injection system can exercise the full dynamic range of the digitizer. This system will be used to check for missing codes, establish scale overlaps, perform cabling checks, etc.

Optical Pulser Calibration System. The linearity check of the (PMT+Digitizer) system will be performed using a flasher system similar to that used by CDF [32], Zeus[33], KTEV [34] and many other experiments. The optical attenuation of flashers are controllable over many orders of magnitude.

System linearity can be verified at the percent level by the usual trick of: (flash A alone, flash B alone, flash A & B together), or by monitoring the output with a PIN diode. The results of these and other calibrations will be downloaded into the calibration lookup RAM table in the Digital Readout board. Thus, any residual nonlinearity in the PMT, calorimeter, or digitizer will have been removed by the time the Trigger & DAQ see the calorimeter data.

Computer Controlled De-Skewing of Clock, Gate, and Test Pulse Signals. Programmable gate positioning allows automated correction for cable lengths, time-of-flight, and propagation delays in the phototubes and electronics. This feature allows PMT cable lengths to be set by convenience rather than propagation delay, and considerably eases the problems of signal routing on the detector. Once signals have entered the digital pipeline, programmable clock phases allow automatic testing of timing margins and correction for unanticipated propagation delays and/or cable lengths. We have fabricated ASIC subcircuits to demonstrate programmable phase control of multi-channel 60 Mhz clock and gate fanouts.

Simple Cabling. A single flat cable carries DC levels for power, HV control, current monitoring and calibration as well as the digital readout. This greatly simplifies the layout of cables on the detector. Multiple cables and their associated ground loops are avoided.

Simple Troubleshooting. If a channel malfunctions, the only candidates for replacement are the PMT Assembly, the relevant channel of the Readout Board, and the cable between them.

Incorporation of Shower-Max Strips in Digital Readout. A similar style of readout is planned for the Multi-Anode PMTs for the Shower-Max detector. The major differences are the reduced dynamic range (12 bits instead of 20), the reduced precision (5+1 bit mantissa and 3-bit exponent are sufficient), and the reduced trigger capability (only a single-bit output from each strip is used in the baseline design). Power dissipation per channel will be substantially lower, since i) the Cockroft-Walton gets shared among 128 channels in a multi-anode PMT, ii) only a 5-bit flash ADC is required, and iii) there is only a single line driver output from each channel. The ICs involved are essentially scaled-down versions of those used in the main calorimeter readout, so that R&D costs will be minimal.

Low Cost. The major cost drivers in the system are the engineering costs, and the per-piece price of the PMT base/digitizer assembly. This first cost is attacked by minimizing the number of items to be designed. In this system there are only two custom components, and three custom ICs. Moreover, only one of the ICs contains any analog circuitry. The second cost

driver is attacked by optimizing the Digitizer module for manufacturability using automated assembly equipment. Traditional PMT base designs are quite labor intensive. To reduce this we have developed a method for producing the PMT base/digitizer assemblies literally a hundred at a time, using pick-and-place equipment and a minimum of hand labor. (See sect 5).

3. KEY SPECIFICATIONS

This section discusses in some detail the key specifications which drive the design.

Packaging

Photomultiplier tubes occur in a variety of configurations in the calorimeter. Fig. 3.1 is a conceptual drawing of what one might hope the phototube layout to look like in the barrel, and fig. 3.2 is a realistic drawing from an engineering design. PMTs in the barrel are laid on their sides along the surface of the detector. Phototubes reading out towers cut by the "vertical readout crack" will be piled up along a bulkhead. Special arrangements must be made for PMTs obstructed by the arms of the calorimeter support cradle. Phototubes in the endcaps will require entirely different arrangements. The number of PMTs/tower changes as a function of Eta, and changes for towers which get split by the readout crack. Finally, phototubes occur in cramped quarters in the access space around the calorimeter. Here a quick, easy, modular means of replacement for both the PMT and electronics is a necessity.

Anticipating these difficulties, and asking ourselves the question "What do we really want for a Phototube readout for the SSC?", we settled on the packaging scheme shown in fig. 3.3 and on the cover of this document. The housing looks rather like a conventional PMT housing. A bundle containing 20-50 optical fibers from a depth segment of a tile/fiber calorimeter tower [2] enters at one end. A single flat cable containing digitized signals, power, clocks, and HV control connects at the other end. A bayonet disconnect allows quick replacement of the PMT/base/digitizer assembly.

This packaging solves a number of engineering problems. Mechanically, it provides a flexible module which can be deployed and cabled in a variety of convenient ways on the calorimeter. Electrically, we have isolated the problems of High Voltage and analog crosstalk to the interior of individual metal cans for each phototube.

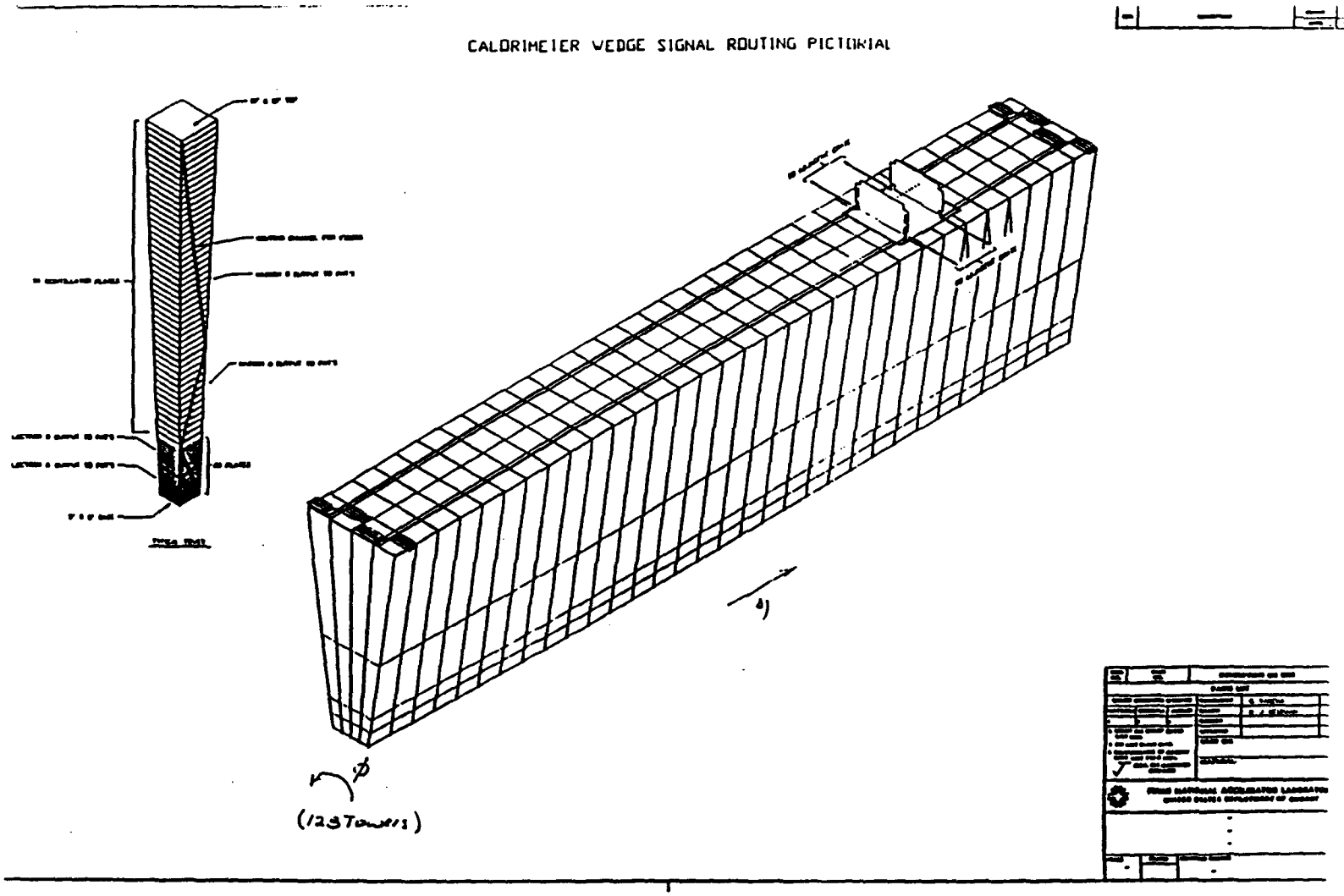


Fig. 3.1 PMT CABLING CONCEPTUAL LAYOUT for tile/fiber calorimetry. Each "Wedge" of calorimetry in the barrel contains an array of 4x26 towers with PMTs for each depth segment.

SEVERAL VIEWS OF A TYPICAL BARREL CALORIMETER WEDGE, SHOWING PMTS, FIBER ROUTING GROOVES, AND EM "PIANO WIRES"

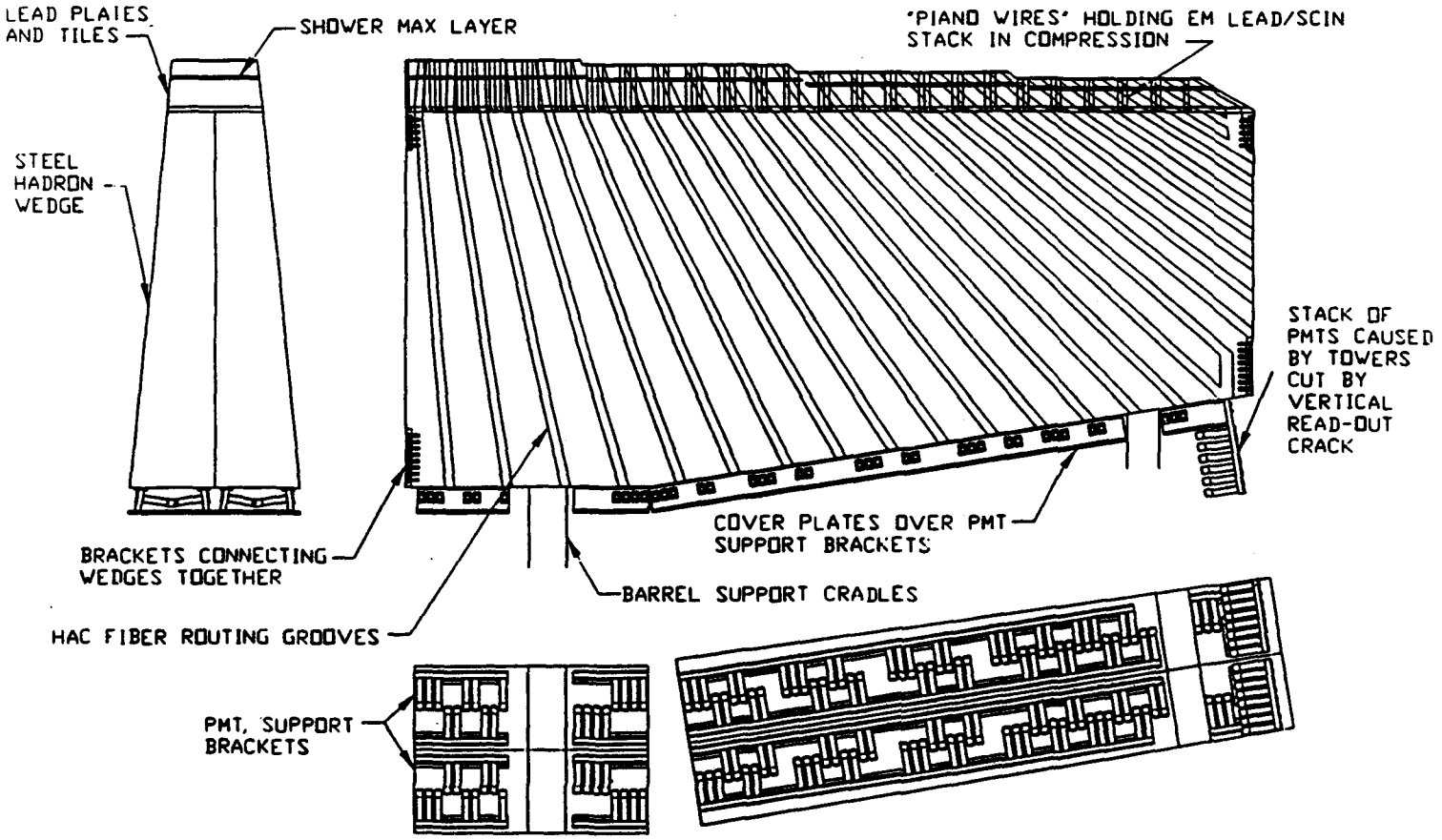


Fig. 3.2 PMT REALISTIC LAYOUT (from "Iron" engineering design option for tile/fiber calorimetry.) A realistic design places PMTs in many configurations and demands a flexible packaging scheme.

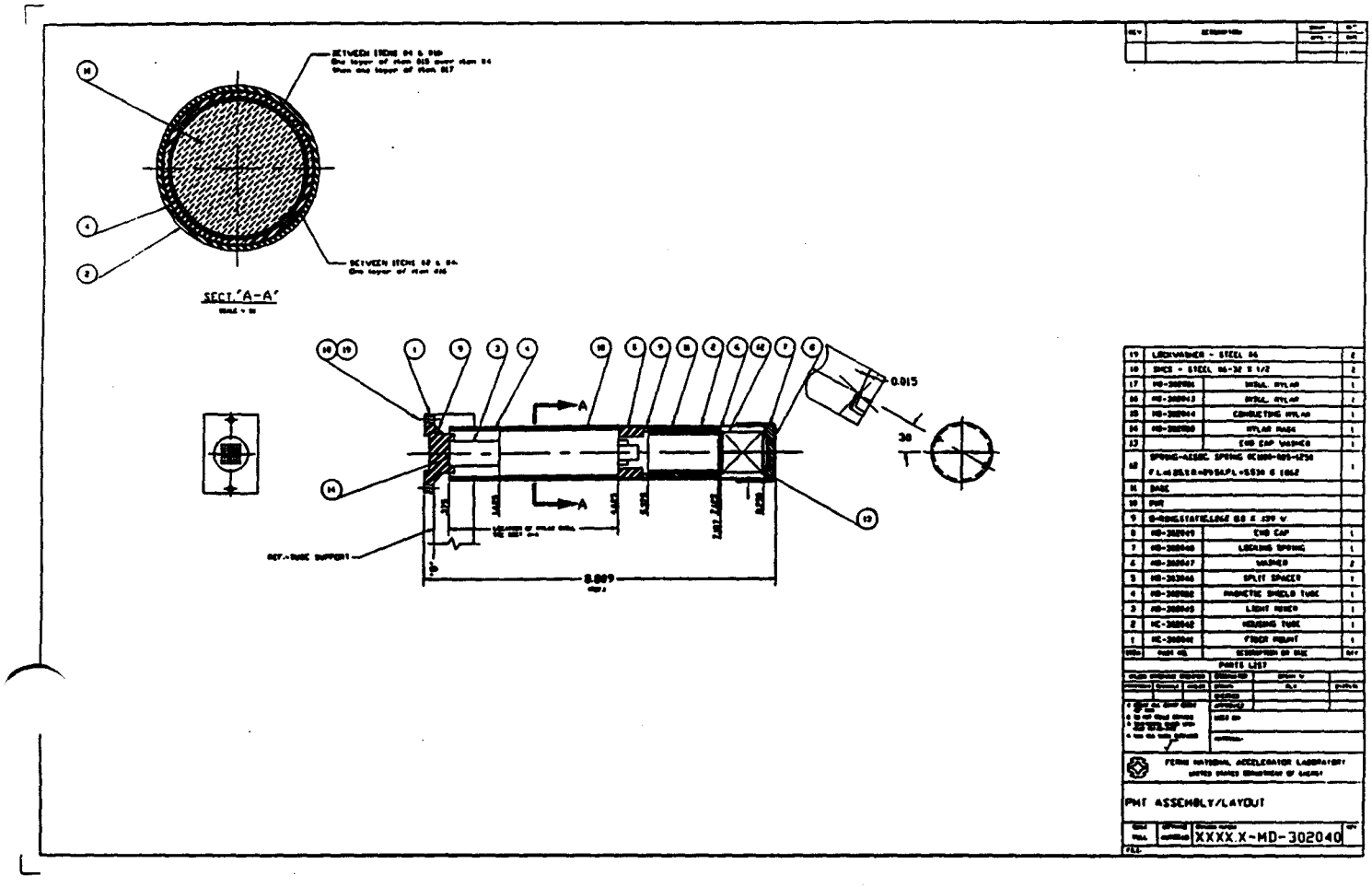


Fig. 3.3 DETAIL OF PMT MOUNTING SCHEME, including cookie, light mixer, phototube, base/digitizer assembly, cable, and bayonet quick-disconnect.

In the beam tests of the Digitizer ASIC we discovered that it was not necessary to go to extremes of shielding and grounding in order to attain adequate noise levels. (The 2fC noise level achieved in the BNL test beam was within a factor of two of the noise level needed for our 20-bit dynamic range spec described below). For example, a small 3" cable stub between the PMT base and the Digitizer card did not adversely affect the noise. A standard circuit board (multilayer with ground and power planes) did not need any additional shielding (foil, metal boxes, etc.) in order to achieve good noise performance. The phototube had to be well shielded, however, and its shield well connected to the ground of the Digitizer board.

Dynamic Range

The dynamic range is set by Physics requirements on the calorimetry, and by PMT and scintillator characteristics. The 20 TeV beam energy requires that the system be able to record a 1 Tev E_T deposition at 5.7 degrees in the endcap calorimeter (10 TeV E_{TOTAL}). Calorimeter resolution requires 100-200 Photoelectrons/GeV. To optimize the dynamic range, one normally matches the maximum linear pulsed current from a PMT to maximum energy deposition in the detector. Thus, the upper limit of the dynamic range is set by the charge (~1nc) which can be delivered in a 10ns pulse by a reasonably good PM tube. These numbers fix the PMT gain at ~ 6000.

The lower limit of the dynamic range is set by the desire to see a clean muon signal in each depth segment of the calorimeter. This is a capability of a phototube calorimeter which has proven very useful at CDF and which should not be compromised by the electronics. The MIP energy depositions in the EM1, EM2, HAD1 and HAD2 depth segments are 100 MeV, 100 MeV, 1.3 GeV and 1.5 GeV respectively. We therefore choose 10MeV as the least count resolution for our system. This choice puts the muon peak in channel ~10 in each of the EM compartments. It corresponds to 3 Photoelectrons/ count for a calorimeter with 300 PEs/GeV. It also corresponds to a least count sensitivity of 6000 electrons/count.

The test beam module clearly resolved the signal from muons (and/or punch-through pions) [7].

Table 2: Dynamic Range Summary

Least Count Sensitivity	= 1 fC = 6000 electrons = 0.1 uA x 10ns current pulse from PMT = 1mV on a 1 pf integrating capacitor = 10 MeV for a calorimeter with 100 PE/GeV and a Phototube gain of 6000 = 1/10 MIP in EM1 & EM2 Sections of Calorimeter
Full Scale Sensitivity	= 1 nC = 2 volts on 1pf after 1/512 current attenuation = 100ma x 10 nsec current pulse from phototube = 10 TeV for a calorimeter with 100 PE/GeV and a Phototube gain of 6000 = 10^6 least counts

Digitizer Resolution

The inherent resolution of the scintillator/phototube calorimeter should not be degraded by the electronics digitization error at any energy. Rather than attempting to cover the 20-bit dynamic range with one or two high precision scales, we have chosen an approach in which internal signal processing takes place on a large number of binary-weighted scales. Only an honest 8-9 bit analog signal processing accuracy is required on each scale, which may actually be possible at 60MHz. Thus we have chosen a 12-bit floating-point digitized output which spans the 20-bit dynamic range of the system. The floating point output has a 4-bit exponent and an 8+1 bit mantissa. (Here the "+1" refers to the so-called "hidden bit" in floating point notation, see. It is related to the fact that the FADC ladder is set up to digitize only the last 1/2 of the output range of any given integrator, so that the 256 counts of the FADC correspond to what would be the *last* 256 counts of a 512-count range). Thus, except at the low end of the range, every signal is digitized to a least-count accuracy which varies between 1/256 and 1/511 of itself.

A plot of the Digitization Error vs. Energy is given in Fig. 3.4. Here the digitization error is sigma = (least count) / sqrt(12). Also shown is a nominal calorimeter energy resolution of 10% / sqrt(E) in quadrature with a 0.5% constant term. The floating point digitization accuracy is more than sufficient

over the entire dynamic range.

The floating point output can be thought of as a 12-bit approximation to a 20-bit number in which each count represents 10MeV. See section 4 and ref. [12] for details.

DC Coupling

The hit rate in the calorimeter approaches 50% / channel / crossing at the corner of the endcap at a luminosity of $10^{34}/cm^2/sec$. There will be large stochastic fluctuations in this energy deposition. Moreover, the luminosity will have systematic on/off fluctuations on the time scale of microseconds due to the RF structure of the machine: booster batches, abort gaps, etc. Under these conditions, any kind of AC coupling or bipolar shaping creates problems with baseline shifts and pileup which are detrimental to signal quality and trigger performance. These problems have traditionally been avoided in high-rate experiments by DC coupled systems, and unipolar shaping which clips the PMT pulse back to baseline as quickly as possible. Thus our digitizer is implemented as a (set of) DC coupled "gated integrators" which directly integrate the PMT current for one crossing on a sampling capacitor. In this topology the current passes directly from the PMT anode to the sampling capacitors. The capacitors voltages are digitized and the capacitors are fully reset before being used during subsequent crossings. The system is completely DC-coupled and hence has no memory of the energy depositions from previous RF buckets.

Noise

The required dynamic range (10 MeV least count, 10 TeV full scale) is a factor of 10^6 or 20 bits. Realizing the low end of this dynamic range requires a digitizer with a least count sensitivity of 6000 electrons/count. This is obviously a great technical challenge in a 60 MHz system. This is not a problem from an electronics noise point of view; given the small ~10pf anode capacitance of a PMT with base, input charge noise levels of 1000-1500 electrons are possible in a 16ns gate. The authors have several experiments taking data today using custom ICs with 1000-1200 electrons equivalent noise charge with ~ 20ns shaping times.

Noise pickup from digital clocking represents a much more serious problem for the project. The digitization circuits reside in individual metal cans at the base of each PM tube. Only high-speed digital links and low-

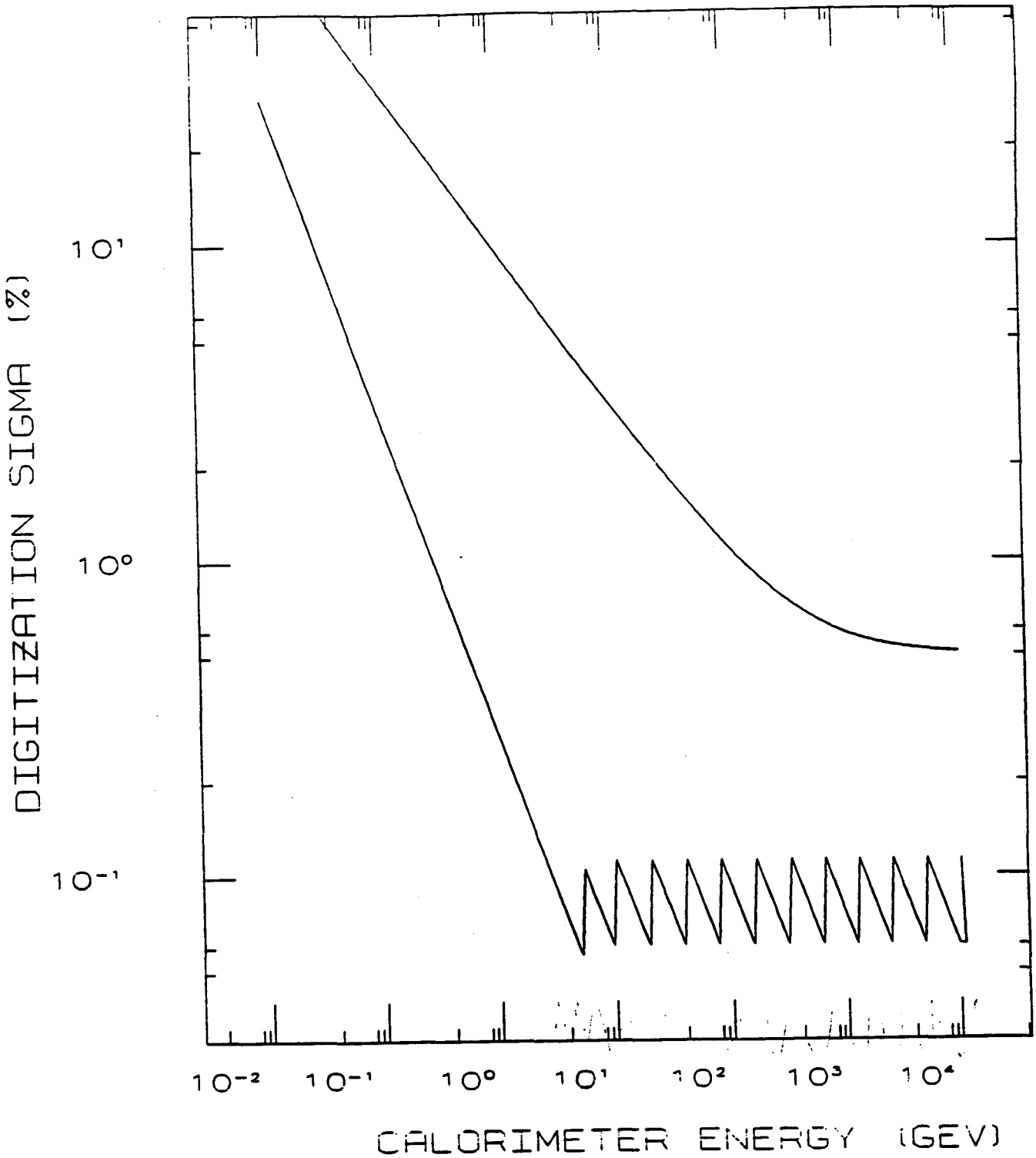


Fig.3.4 DIGITIZATION ERROR and ENERGY RESOLUTION OF CALORIMETER as a function of energy. The bottom curve gives the digitization sigma = (least count) / sqrt(12) for the floating-point output of the digitizer. Except at the low end of the scale, a signal is digitized to a least-count accuracy which varies between 1/256 and 1/512 of itself. Also shown is a (rather optimistic) calorimeter energy resolution of 10%/sqrt(E) with a 0.5% constant term.

bandwidth analog monitoring signals travel on the connecting flat cable, so that system-level crosstalk problems should be minimal. This leaves two possible additional sources of digital noise: board-level noise pickup and on-chip pickup (e.g. substrate coupling). These are art. The current state of our art is the 2fC pedestal noise in the Test Beam ASIC / Digitizer module [7]. The ASIC in this module brings out only the 2nd most sensitive scale to the FADC. We expect that our next (Version 4) ASIC, which brings out all scales, will reach the 1fC needed for 20-bit dynamic range.

Crosstalk and Coherent System Noise

The physics crosstalk from an EM energy deposition in a nearby tower is 10^{-2}, 10^{-4}, and 10^{-6} for signals 1, 2, and 3 towers away. This physics crosstalk signal comes from low-energy gamma's and albedo. Our general design philosophy is to not let the electronics limit the performance of a scintillator/phototube calorimeter. Therefore, the design goal is that any (or all) of the PMTs in a crate should be able to absorb simultaneous full-scale hits while disturbing a non-struck PM tube in the same crate by less than one count (10 MeV). We feel that this specification is achievable in the context of individual digitizers in metal cans on each PM tube. While this specification is arguably overkill from a physics perspective, it is a worthwhile exercise to ensure of the robustness of the overall system.

Data-dependent digital crosstalk may present a serious system noise issue. The input to the metal can containing the PMT is optically isolated, but it is possible that noise coming down the flat cable from the digital crates could get into the digitizer circuit. The worry is that this could give rise to the classic trigger problem of coherent, data dependent noise or oscillations which become visible only when large numbers of signals are added together. In principle low-level noise pickup can be suppressed by digital thresholding in the trigger pipeline; however is it clearly desirable to have these thresholds as low as possible. Our test-beam module used differential current-mode signals on the flat cable. The PMT base/digitizer will be carefully tested for rejection of noise transients coming down the cable at it. At present, the target spec is that a worst-case switching transient on all digital trigger and DAQ lines produces a disturbance of less than 1 count (10 MeV) in the digitized value in each PMT.

In order to define an achievable specification for coherent system noise, we are producing a demonstration system containing several of the test beam ASIC/ FADC digitizer boards [7], VME based "pipelined adder tree" boards [21], and VME based pipelined readout boards [20]. By

repetitive triggering and digital averaging on this prototype system, we hope to be able to measure a coherent disturbance of a small fraction of a count. If possible, we may move to a more aggressive specification than the 10MeV/ Channel worst case coherent noise specification.

Radiated Noise

A possible concern with this system might be the noise radiated from the cables causing problems in the low-level analog signals of other systems. Presumably crate-level noise associated with simultaneous clocking of large numbers of channels occurs in any readout scheme. This is a concern, but will not differentiate between Analog and Digital readout systems.

We do not expect cable radiation to be a serious problem. Firstly, the fiber bundle inputs to the PM tubes provide optical isolation, and a single flat cable connects between the PMTs and the Readout Crate. Therefore, no ground loops can be developed.

Secondly, the flat cable that we've tested and are using in our cost estimate contains an integral ground plane. In a bundle of these cables, the signal conductors are effectively shielded on both sides by these ground planes. If necessary, the cable bundles can themselves be shielded by wrapping with a foil conductor.

Finally, the PMTs and cable runs are behind protective covers [2] which will likely be aluminum and could easily be RF-shielded.

Out of necessity, each of the other subsystems has to deal with their own digital noise from clocking, trigger, DAQ, and calibration pulsers. Subsystems which might be affected are, in order of increasing distance from the readout crates:

1) The Shower-Max subsystem, which shares crates with the Digital Readout system. If the Digital Readout system is used, the topology is the same as for the Digital PMTs: optically isolated input, a metal can around the photodetector, and a single (digital) flat cable going to the crate. If the Analog readout system is used for shower-max readout, problems with noise pickup in the analog cables could be severe -- from the calorimeter readout and from other systems.

2) The muon system is within earshot of many of the PMT assemblies. The current design has wire gains of ~10^5 and unpreamplified cable runs to "mini-crates" a couple of meters away [1]. There are also high-speed digital signals from several thousand muon trigger counter discriminators nearby, which will be a much more immediate problem for the muon system.

3) The fiber tracking readout is a big digital pipeline, which has been tested in coexistance with us (we shared readout crates) in the BNL test beam with no problems. The straw tracking design[1] has digital trigger and data collection logic on the tracker endplate a few centimeters away from the low-level amps. The digital noise from calorimeter readout electronics which are separated by 2m of iron should be the least of their problems.

4) The silicon system claims to be optically isolated except for their power feeds...their main worries will be internal clocking noise and radiation from oscillating straw tube amps.

Power Dissipation

The power dissipation target is < 1w per channel at the Phototube. Individual targets are 100 mw for the analog ASIC and 750 mw for the commercially-purchased Flash ADC (the Analog Devices AD9002 used in the cost estimate meets this spec). On the Digital Readout Board, the targets are 300mw for the L2/L2/Calib digital ASIC, and 250mw/input for the floating-point adder tree. (A power dissipation of ~265mw/input was measured in tests of the Adder Tree ASIC by the SSCL electronics group[15]). For an SSC calorimeter with 21,000 PM tubes, this is 32kw. Since all of this power is dissipated on the outside of the detector, this poses no particular problem.

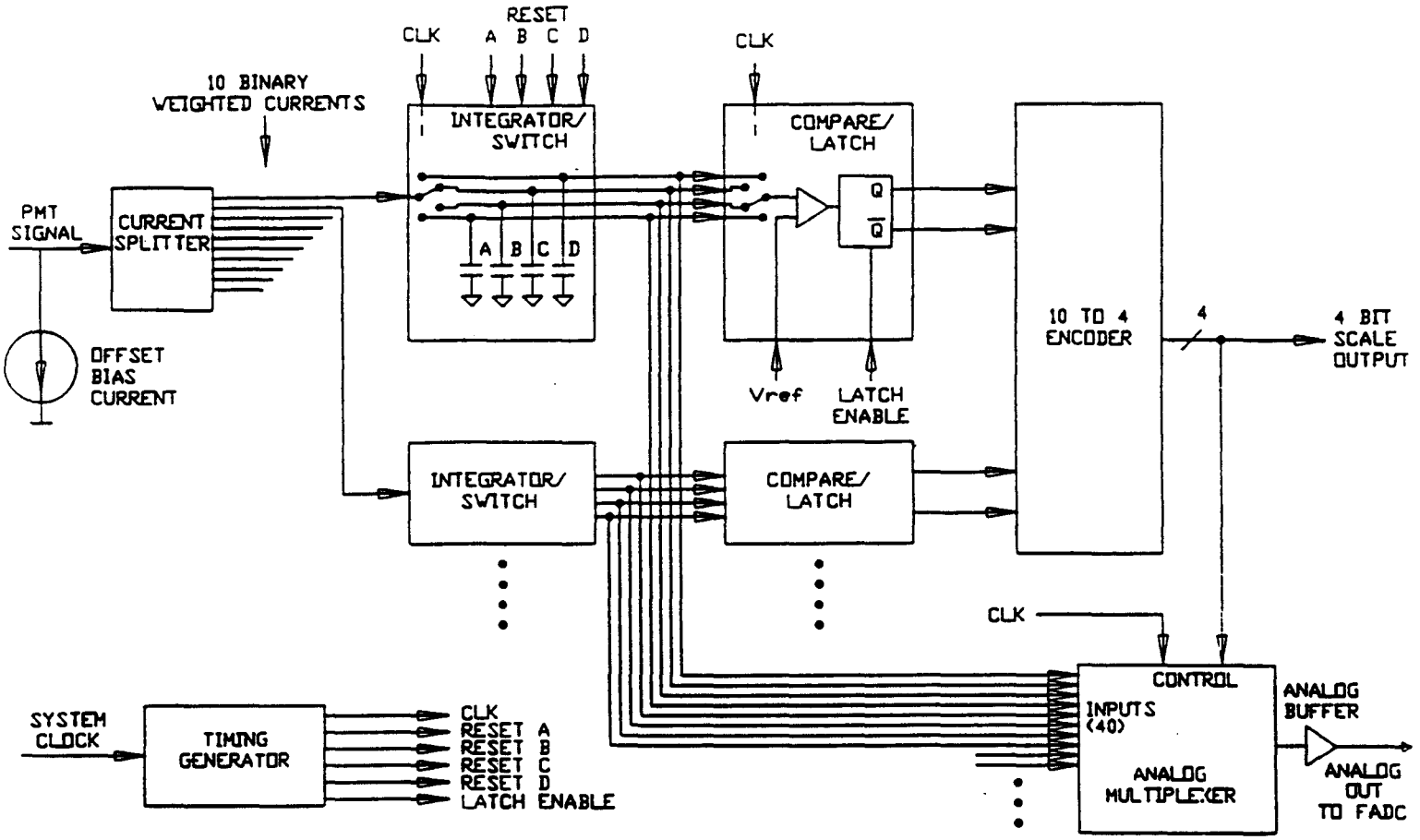
4. PHOTOTUBE DIGITIZATION

The cornerstone of the Digital PMT Readout is the circuit which provides high dynamic range digitization of the PMT charge in each 16ns bucket. It produces a floating-point output with 8-9 bit accuracy and 20-bit dynamic range. A complete description of the circuit is given in [5]; this is a brief overview.

The Basic Idea. A block diagram of the circuit is shown in fig. 4.1. It has five major sections.

The first (Current Splitter) section, the PMT current is split into ~10 binary-weighted current outputs. These generate the binary scales corresponding to the exponent of the floating point output.

In the second (Gated Integrator/Switch) section, each of the split phototube currents is sent through a four-way current switch to one of four integrating capacitors. Each of these four capacitors goes through a four-clock sequence in which it integrates, settles, is (sometimes) digitized, and is



PHOTOMULTIPLIER TUBE GATED INTEGRATOR/DIGITIZER CHIP

Fig 4.1 PMT DIGITIZER BLOCK DIAGRAM. Main circuit elements are: (i) Current Splitter, which splits the Phototube current into ~10 binary weighted scales; (ii) Integrator/Switch, which integrates the charge from each scale on one of four capacitors in a pipelined "round-robin" manner; (iii) Comparator/Latch, which determines if the capacitor contans an "interesting" voltage (between 1/2 and full scale), (iv) Encoder, which uses the comparator outputs to generate the 4-bit scale code ("mantissa"), and (v) Analog Multiplexor/Buffer, which selects the "interesting" capacitor voltage and outputs it the FADC on each cycle.

reset. The sequence proceeds in round-robin manner so that one capacitor is always integrating, i.e. the circuit is deadtimeless.

The third (Compare/Latch) section is responsible for determining which of the capacitors to digitize. There are ~10 binary-weighted gated integrators to chose from each cycle, but only one of them is "interesting", i.e. between half scale and full scale. A single comparator on each capacitor makes this determination. The comparator outputs are latched and allowed to settle.

The fourth (Encoder) section turns the comparator bits into a 4-bit binary-encoded output. These 4 bits form the binary scale range (exponent) of the floating-point output.

The fifth (Analog Multiplexor) section uses the encoder output to select the voltage from the "interesting" capacitor on each crossing, and buffers that voltage off-chip to the 8-bit FADC. This FADC produces the 8-bit "mantissa" of the floating-point output. The FADC function may be integrated onto the IC in the final design if this is economically justified.

Additional details of the digitization

1. Since the FADC is only called upon to digitize capacitor voltages between 1/2 and full scale, the FADC ladder can be set up to cover only the top half of the range. Thus, the circuit digitizes signals to a least-count accuracy which varies between 1/256 and 1/511 of itself, even though the ADC is only 8 bits.

2. In order to produce a nonzero digitized signal on the lowest range scale when zero charge is deposited from the phototube, a bias current $I_{PEDESTAL}$ is injected into the input. Thus the digitized output is:

$$\text{Charge (in fC)} = (\text{FADC Mantissa} + 256) \times 2^{\text{EXPONENT}} - I_{PEDESTAL}$$

This bias current $I_{PEDESTAL}$ is "subtracted out" in the calibration lookup RAM.

Table 3: Time Sequence for 4-Clock Sampling and Digitization

Cycle	Time	Operation
1	16ns	Integration on Sampling Capacitor
2	4ns 12ns	Capacitor, Follower, and Comparator Settling Latch Decision Time (resolve metastability)
3	16ns	Output Multiplexing and Buffering to FADC
4	16ns	Reset of Sampling Capacitor

Input Characteristics and Pulse Clipping

The analog ASIC is optimized for placement in close proximity to the Phototube (i.e. no cable). The input stage (basically a common-base NPN transistor with feedback) must have a low enough input impedance to drain off the charge from the anode (~ 10 pf) with an RC time constant of 2ns or less. This requires an input impedance of 200 Ohms or less, which is easily met by our splitter design (Z_{IN} ~ 40 Ohms).

The input is compatible with a passive phototube pulse-clipping network, either delay-line, R-C, or R-L. Such clipping techniques (which effectively subtract off the exponential tail of the scintillation light pulse) have been used to bring the pulse from PM tubes back to baseline within ~2 signal rise times.

Another important feature of pulse clipping, if it can be achieved without sacrificing calorimeter energy resolution, is that it allows the PM signals to be at baseline at either edge of the sampling gate. This makes the digitized charge insensitive to the exact position of the pulse inside the gate. A pulse which fits comfortably inside the ADC gate considerably eases the timing requirements on the timing of the gate fanout.

5. MASS PRODUCTION TECHNIQUE FOR PMT BASE / DIGITIZER ASSEMBLIES

We have been investigating a technique of assembling phototube bases which lends itself to easy, automated manufacture. Traditional PMT

base assemblies are very labor intensive, and contain many hand-soldered joints which can limit reliability. This is a scheme which allows one to capture the economic advantages of surface mounted components and automated "pick and place" machines, while producing a finished assembly which has the right size, shape, and shielding characteristics to be used as a phototube base.

The basic idea is that of a three dimensional printed circuit board with buried components. A cylindrical "plug" of G10 or ceramic is built up out of a series of "disks and washers" which contain circuit board traces, components, and vias. Each disc in the assembly may have surface mount components on both sides. They are first assembled in the usual way using pick-and-place machines. These components are soldered in place as if this were the final product. This layer has not only components but special pads which are used to make connections to the next layer which has holes to allow for the components on the other layers and pads and traces to make connections vertically through the stack of boards. Many layers can be built up in this fashion, with each new layer being added using conductive epoxy or a lower temperature solder.

The use of surface-mount components in the PMT base is important if we to minimize the cost of the Cockroft-Walton charge pump circuitry. The installed, tested cost is ~$0.05 ea. for discrete components using this technique.

When this technique is applied to some thing as small as a PMT base, each PC board may contain many copies of the same circuit. Thus as the assembly is manufactured, a large number of bases are made at once. If the bases were laid out on a 10 by 10 grid, 100 bases would be manufactured at the same time. These bases would then be cut apart and tested before final assembly into the base canister. The other feature of this technique is that the base would be mechanically robust.

The specific example we have been working with has 3 distinct circuit layers, which are round, with SMT components on both sides and 2 sets of "Rings" which make the electrical connections between the component layers. The size we chose was a 1 inch diameter circle, the final base electronics assembly would then be a cylinder 1 inch in diameter by about 1 inch high. We have used both solder and conductive epoxy to make the inter- layer connections and both techniques seem to work although we are still experimenting. The "rings" which make the connections between layers have an 8 inch hole in them which allows for the vertical size of the SMT components. This hole is plated through so that the effect is that of a metal canister buried inside the PMT, this would be used to shield the voltage

multiplier circuit from the other sensitive electronics. These rings and the component discs also have aligned .031" plated through holes which are connected to ground, these holes, after assembly, create a grounded tube through which one can run a small wire, creating a shielded coaxial path through the device so that sensitive signals can be passed thought noisier sections of the base without degradation.

We believe that this technique can be used to mass produce PMT bases at a very low cost, and that the ability to include within the base coaxial signal paths and shielded regions containing components will be useful in optimizing the performance of the base/digitizer.

6. SUMMARY COST ESTIMATE FOR DIGITAL PMT READOUT

Table 4 gives a summary cost estimate for the system. A complete WBS based cost estimate is given in [6]. The production quantities assumed here are 26,000 whereas the current channel count for the system is 20,736.

Table 4: Cost Estimate for Digital PMT System

Item	Cost ea.	Qty.	Total
Digitizer Modules: (production, test, and all parts except Digitizer ASICs, FADCs, PMTs & PMT mechanics.	$41.00	26000	$1,066,000.
Digitizer ASICs (production Cost)	$6.13	26,000	$159,080
FADC (8 bit, Analog Devices AD9002)	$30.00	26,000	$780,000
Flat Cable Assemblies (production + test)	$23.68	26,000	$615,000
Digital Readout Board (Production + test)	$1356	1408	$1,910,000
Crates (shared w/showermax)	$4900	64	$313,000
Misc. Production costs	$630,000	1	$630,000
Production Engineering and Documentation	$368,000	1	$368,000
Pre-production Electronics and Engineering	$1,772,000	1	$1,772,000
Management and System Documentation	$169,000	1	$169,000
TOTAL (w/o contingency)			$7,782,000

REFERENCES

[1] "SDC TECHNICAL DESIGN REPORT", SDC-92-201, Solenoidal Detector Collaboration, 1 April 1992.

[2] " CALORIMETER CONCEPTUAL DESIGN: TILE/FIBER SCINTILLATOR OPTION", SDC Tile/fiber Calorimeter Group, 3 Sept 1991.

[3] "DIGITAL READOUT OF THE SHOWER-MAXIMUM DETECTOR FOR THE SDC CALORIMETER", W. Foster, J. Hoff, M. Sarraj, R.J. Yarema, T.Zimmerman, SDC note SDC-92-308, 27 Aug 1992.

[4] "CALIBRATION OF THE DIGITAL READOUT SYSTEM FOR THE SDC CALORIMETER", W. Foster, J. Hoff, M. Sarraj, R.J. Yarema, T.Zimmerman, SDC note SDC-92-307, 27 Aug 1992.

[5] "A PIPELINED MULTIRANGING INTEGRATOR AND ENCODER ASIC FOR FAST DIGITIZATION OF PHOTOMULTIPLIER SIGNALS", R.J. Yarema, W. Foster, J. Hoff, M. Sarraj,T.Zimmerman, Proc. 2nd Annual Conference on Electronics for Future Colliders, Chestnut Ridge, NY May 19-21 1992.

[6] "WBS DICTIONARY AND COST/SCHEDULE BREAKDOWN FOR DIGITAL CALORIMETRY READOUT OPTION FOR THE SDC", Ray Yarema, Feb 14 1992; updated Aug 1992.

[7] "BEAM TESTS OF THE DIGITAL PMT READOUT SYSTEM", G.W. Foster and R. Tschirhart, SDC note SDC-92-0310 (in preparation).

[8] "A PROOF-OF-PRINCIPLE FADC TEST BOARD FOR THE DIGITAL PHOTOTUBE READOUT SYSTEM FOR THE SDC CALORIMETER", C. Rivetta, S. Hansen, G.W.Foster, FNAL tech note Sept 1991, revised Aug 1992.

[9] "PMT DIGITIZER CURRENT SPLITTER VERSION 1 TEST RESULTS", FNAL technical note, T. Zimmerman, Jan 14,1992.

[10] "PMT DIGITIZER CURRENT SPLITTER VERSION 2 TEST RESULTS", FNAL technical note, T. Zimmerman, March 31,1992.

[11] "PMT RANGE ENCODER AND INTGRATOR CONTROL [Version 3] TEST CHIP", M. Sarraj, FNAL technical note, 17 July 1992.

[12] "A FULL CUSTOM, HIGH SPEED FLOATING POINT ADDER", Jim Hoff and Bill Foster, FNAL Technical Note #TM-1779, Nov. 1991.

[13] "ADDER CHIP", Jim Hoff, FNAL Technical Note, July 1991.

[14] "ADDER TESTS", M.Larwill,J.Hoff,C.Needles, Feb 17,1992, revised April 1 1992.

[15] "ADDER TESTS", SSCL Physics Research Division Technical Note, Srinivas Karuturi, Paschal Kibuule, Jheroen Dorenbosch, June 9 1992.

[16] "AN APPROXIMATE HSPICE MODEL FOR ORBIT LOW-NOISE ANALOG BIPOLAR NPN TRANSISTORS", Fermilab TM-1748, July 1991.

[17] "THE SIRO CHIP", Jim Hoff, FNAL Technical Note, Dec. 1990; "SIRO TESTS", J.Hoff, (undated).

[18] "THE AD CHIP", Jim Hoff, FNAL Technical Note, Aug 1. 1990; "AD CHIP TEST RESULTS",FNAL Technical Note, T. Zimmerman, Oct 12 1990.

[19] "RADIATION EFFECTS ON THE SVX SILICON READOUT CHIP", Ray Yarema et. al., FNAL technical note, 1990.

[20] "SDC FIFO STORAGE AND SEGMENT FINDER MODULE PRELIMINARY SPECIFICATIONS",FNAL technical note, Al Baumbaugh and Andy Romero, March 1992.

[21] "SDC ADDER TREE VME MODULE VERSION 1",FNAL Technical note, Hector Gonzalez, Nov 1991.

[22] For more information on the Fermilab PMT Test Facility contact Steve Pordes or Mike Crisler, Fermi National Accelerator Lab, P.O. Box 500, Batavia IL 60510.

[23] C. Blocker, presentation at the SDC Calorimetry Group meeting, Aug 3 1992.

[24] "THE CONCEPTUAL DESIGN OF THE SDC TRIGGER", the SDC Trigger Group, Aug. 27, 1991; THE SDC GLOBAL LEVEL 1 PROCESSOR, Preliminary Draft, Wesley H. Smith, March 14, 1991.

[25] V. Barnes, Ft. Worth SSC Symposium, 1990.

[26] Cockroft-Walton Phototube HV Supply, L. Mo et. al.

[27] "A HV RESONANT CONVERTER FOR PHOTOMULTIPLIER TUBE BASES", G. W. Foster, S.Hansen,C.Rivetta, SDC note SDC-92-309 (in preparation).

[28] "TEST OF DIGITAL TRANSMISSION CHARACTERISTICS OF 0.025" PITCH FLAT CABLES", M. Haldeman, R. Yarema, FNAL Technical Note, Jan 23,1989.

[29] HAMAMATSU R5329 SAMPLE TEST SHEET, obtained from Don Lowell, Hamamatsu Photonics, dated May 28 1992.

[30] AMES Laboratory's FADC test facility is supported through SSC funding; contact Eli Rosenberg for details.

[31] The gated integrators used in by the D-Zero collaboration (13 or 14 bits) are at least one example.

[32] "THE CDF CENTRAL AND ENDWALL HADRON CALORIMETER", NIM A267 (1988) 301-314.

[33] ZEUS collaboration, Detector Status Report, 1989.

[34] KTEV Design Proposal, Nov 1991.