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FRONT END BUFFERS FOR A STRAW TUBE DCC SYSTEM

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Abstract

In this note we present the results of calculations of the buffer occupancies at the front end card and compare options that make it possible to impose a minimal time between L2 accepts to allow the FMUX to be read out completely for one event. For the L2 buffer 10-15 storage locations per channel would be sufficient. One can impose a minimal distance between two L2 trigger accepts and with only little additional burden to the L2 buffer, get time ordered events.

1 Introduction

We develop in the following chapters one after the other the requirements of the buffers at the various stages, which lead to the understanding of the final system. The reader who is not interested in the details might want to go directly to chapter 6 where the parameters of the model system are presented and its performance discussed.

The model is a simplified version of the front end simulation model of Sinervo et al. [1]. The model uses the beam clock as the minimal time step and starts generating events for any L1 accept. The L1 triggers are generated with an $L1$ rate between 62MHz*(0.001-0.005). For L1 trigger accepts, hits are generated with a probability/crossing, occup=0.05-0.1. For each trigger 3 beam crossings are read out. These hits then enter the L2 pipeline. The L2 delay ($L2lat$) is parametrized by a gaussian with mean 24 μs and same width (a) or a flat uniform distribution between 10 and 100 μs (b) or 10 and 50 μs (c). L2 trigger accept signals are generated with the probability $L2$. We further require a minimum time $L2min$ between two L2 triggers. This time is the same for L2 accepts or L2 rejects. For all L2 trigger accepts the hits are moved to the FMUX. If one allows for some time t_{FMUX} between 2 L2 trigger

accepts of between 30 and 60 μs one would have enough time to read out the FMUX for one event before before the next one enters the FMUX and get time ordered events. The additional burdens of this additional latency are discussed in chapter 5 and 6.

2 L1 buffer occupancy

The L1 buffer occupancy depends only on the delay of the L1 trigger decision, which we take to be 240 crossings, and the occupancy of one channel per crossing. It follows a binomial distribution:

$$prob(n) = \frac{240!}{(240-n)! * n!} * occup^n * (1 - occup)^{240-n}$$

From this we calculate that for a buffer length of 32 that $2 * 10^{-7}$ of the hits would be lost for an occupancy of 5 %. For an occupancy of 10%, 3.8% of the hits would not be collected by a storage buffer of length 32 and 0.05% of the hits would be lost with a buffer of length 40.

3 L2 buffer occupancy

We test the required L2 buffer size in a simplified version of the front end simulation model of Sinervo et al. [1] We note the following parameters for the huffer: the maximal occupancy $nmax$ of the L2 buffer, the average occupancy n (averaging excludes empty buffer conditions) and the variance of the occupancy distribution σ. Table 1 gives the results for various parameters.

From this table one can infer that the variables n, σ and nmax scale approximately with the square root of L1, occup and L2lat.

$$\mathrm{n}, \sigma, \mathrm{nmax} \propto \sqrt{\mathrm{occup}} * \sqrt{\mathrm{L1}} * \sqrt{< \mathrm{L2lat} >}$$

The introduction of minimal distance between L2 triggers of 250 Xings=4μs does not have a big influence on the performance of the system. This parameter however, starts to have a large influence as soon as this distance comes close to the mean time between L1 trigger accepts (60 MHz*L1=10-20 μs). Conservatively a buffer length of 10-15 storage locations per channel should be sufficient with little losses. Figure 1 shows the maximal occupancy of the L2 buffer, nmax, as the function of the L1 trigger rate for occupancy/crossing of 0.1 and 0.05.

L1	occup	L2lat	L2min(Xing)	n	σ	nmax
0.002	0.1	a	250	2.5	1.6	11
0.002	0.1	a	10	2.3	1.4	10
0.002	0.1	a	600	14	7	>24
0.002	0.05	a	250	1.6	0.9	6
0.002	0.05	b	10	1.9	1.1	7
0.002	0.1	b	10	3.1	1.9	11
0.001	0.05	b	250	1.4	0.7	4
0.001	0.1	b	250	1.9	1.1	6
0.001	0.1	c	10	1.5	0.8	5
0.005	0.1	c	10	3.9	2.1	15

Table 1: L2 buffer occupancies.

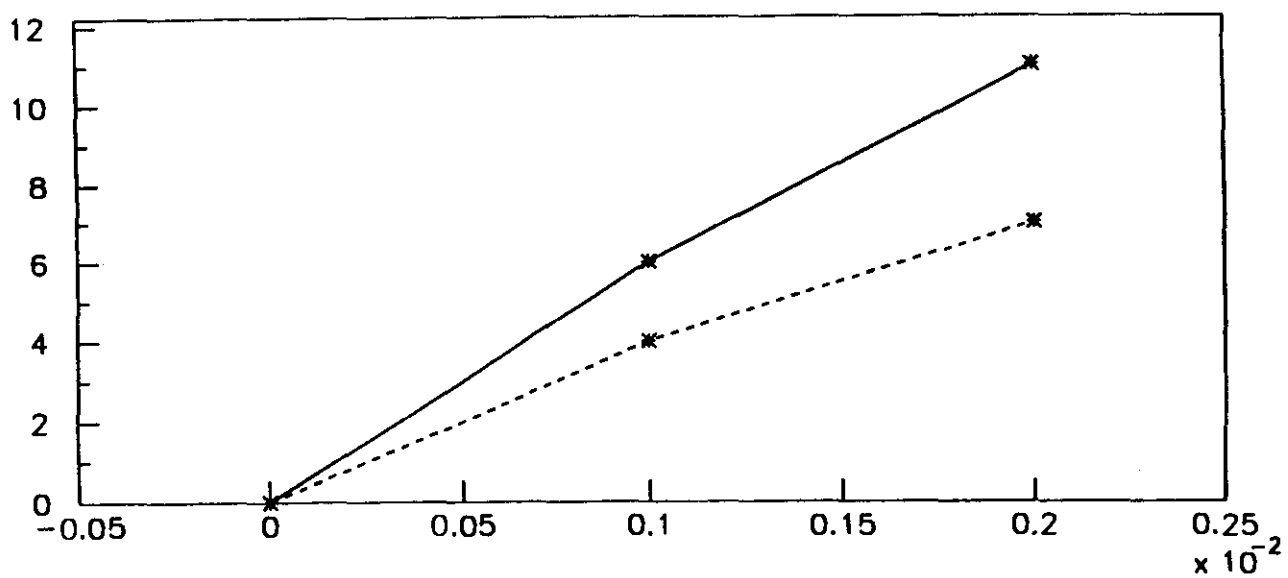

Figure 1: nmax as a function of the L1 trigger accept rate for an occupancy/crossing of 0.1 (upper curve) and 0.05 (lower curve).

4 FMUX occupancy

After each L2 accept the hits are digitized (which happens on a timescale of 3-5 μs) and shipped to a buffer on the FMUX. In this design one FMUX is connected to 32 different data channels. The FMUX itself is read out by the next stage in the readout chain. We now consider the storage needed for this stage.

4.1 A simple calculation

Assume we have an L2 accept rate at crossing number 0. The distance to the next L2 trigger then follows an exponential distribution with the mean L2 trigger rate λ as a parameter. Let t_{FMUX} be the time for the FMUX to be read out, then the probability to have in this time another L2 accept is given by:

$$\text{Prob} = \int_0^{t_{\text{FMUX}}} \lambda * \exp(-\lambda * t)\, dt$$

To be more precise, Prob is now the probability, that during the readout of one event in one FMUX, a second L2 trigger arrives and possibly mixes with the first event.
The present design architecture [2] connects the FMUX to 8 TVC/AMU's each with 4 channels. The time t_{FMUX} is then related to the bandwidth with which the FMUX is read out

$$t_{\text{FMUX}} = \frac{32 * 4 * (0.10 - 0.20)}{\text{bandwidth}} = \frac{(10 - 20)\ \mu s}{\text{bandwidth[Mbyte/s]}}$$

where we assume 4 byte as the length of the data for each hit and (0.10-0.20) as the occupancy per trigger.
The probability that during the time t_{FMUX} two L2 trigger accepts arrive is consequently given by:

$$\text{Prob}_2 = \int_0^{t_{\text{FMUX}}} \lambda * \exp(-\lambda * t)dt \int_t^{t_1} \lambda * \exp(-\lambda * t2)dt2 =$$

$$(\frac{1}{2} - exp(-\lambda * t_{FMUX}) + \frac{1}{2} * exp(-2\lambda * t_{FMUX}))$$

Table 2 gives the results for various parameters.

4.2 Results of simulations

A detailed analysis can be done by using a stochastic simulation. The simulation used to model the L2 buffer occupancy was extended to include the FMUX. After the L2latency

λ(kHz)	$t_{FMUX}(\mu s)$	Prob(%)	$Prob_2$ (%)
1	10	1	0.005
1	50	5	0.1
1	100	9.5	0.5
5	10	5	0.1
5	50	22	
5	100	39	7.7
10	10	9.5	0.5
10	50	39	7.7
10	100	63	20

Table 2: FMUX occupancies (calculation).

time the events are moved to the FMUX where they are read out after a time t_{FMUX}. Now we are interested in the maximal occupancies of the FMUX, n_{hits}, and in the maximal number of different events in one FMUX buffer, n_{evt}. This last number is larger than the number of hits since not every event contains a hit for a particular channel. However since in the present design 32 channels are read out by one FMUX, this number is the important one for making statements about event mixing etc. Table 3 gives the numbers for various parameters:

L1	L2	t_{FMUX} (μs)	n_{hits}	n_{evt}
0.001	0.02	16	1	2
0.001	0.02	32	1	2
0.001	0.02	64	2	2
0.003	0.05	16	2	2
0.003	0.05	32	3	3
0.003	0.05	64	5	9

Table 3: FMUX opccupancies (simulation).

For the last two parameters sets, the probabilities for having 2, 3 or 4 events in the buffer are: 13 %,1% and 0% and 30 %, 12% and 6%, respectively showing that our simple calculations above were reasonably accurate. (the values have to be compared with the second last entry in that table).

The number of different events in the FMUX is very small unless the FMUX readout time

comes close to the L2 trigger accept rate. This is the case for the last parameter set where the L2 trigger accept rate is 11 kHz, which is only a factor 2 larger than the FMUX readout rate.

5 Event ordering

In the above design, one unattractive feature is that different events get intermixed when the FMUX is read out. Since the FMUX occupancies are low, one might want to impose an artifical minimal distance τ between two *L2 trigger accepts* in order to leave enough time to read out the FMUX for one event. τ therefore has to be larger than t_{FMUX}. For simplicity we will assume that $\tau = t_{FMUX}$. This additional latency would require the L2 buffer to take the burden of this additional buffering. The time needed for the additional buffering depends on the time one needs to clear the FMUX.

L1	L2	L2rate(kHz)	$t_{FMUX}(\mu s)$	n	σ	nmax	(%)
0.002	0.02	2.4	1	2.5	1.5	11	0
0.002	0.02	2.4	32	2.5	1.5	11	11
0.002	0.02	2.4	64	2.6	1.6	11	22
0.003	0.05	9	1	4.1	2.3	15	
0.003	0.05	9	32	4.2	2.5	15	
0.003	0.05	9	64	6.9	4.3	> 24	

Table 4: L2 buffer occupancies with an minimal L2 trigger accept distance.

The last column in the table gives the percentage of L2 trigger accepts that had to be buffered so that the minimal distance criterion was satisfied.
For the L2 latency time we used a uniform distribution between 10 and 100 μs, so that the typical latency was usually much larger, than the additional latency caused by the minimal distance requirement.
The increase in required L2 buffer space on the L2 buffer side seems to be modest, if noticable at all for the assumed parameters. However, as soon as the FMUX readout speed approches the L2 accept rate, the required buffer size increases dramatically. The small increase in buffer requirement can be understood in the following way: The minimum L2 accept requirement introduces *on the average* a latency of L2 * t_{FMUX} for each event, which is quite small compared to the L2 decision latency, since L2 is small. This effect however becomes very important when the probability that during this latency another L2

taccept trigger occurs becomes important. At this point the L2 buffer queue is not emptied any more.

This method of event ordering also requires a buffer space on the FMUX of only 3 storage locations per data channel (since 3 crossings are read out per trigger). Figure 2 compares the L2 buffer occupancy distribution for L1=0.003 and L2=0.05 before (a) and after (b) imposing the L2 accept delay of 32 μs. One sees only a slight increase in buffer space needed.

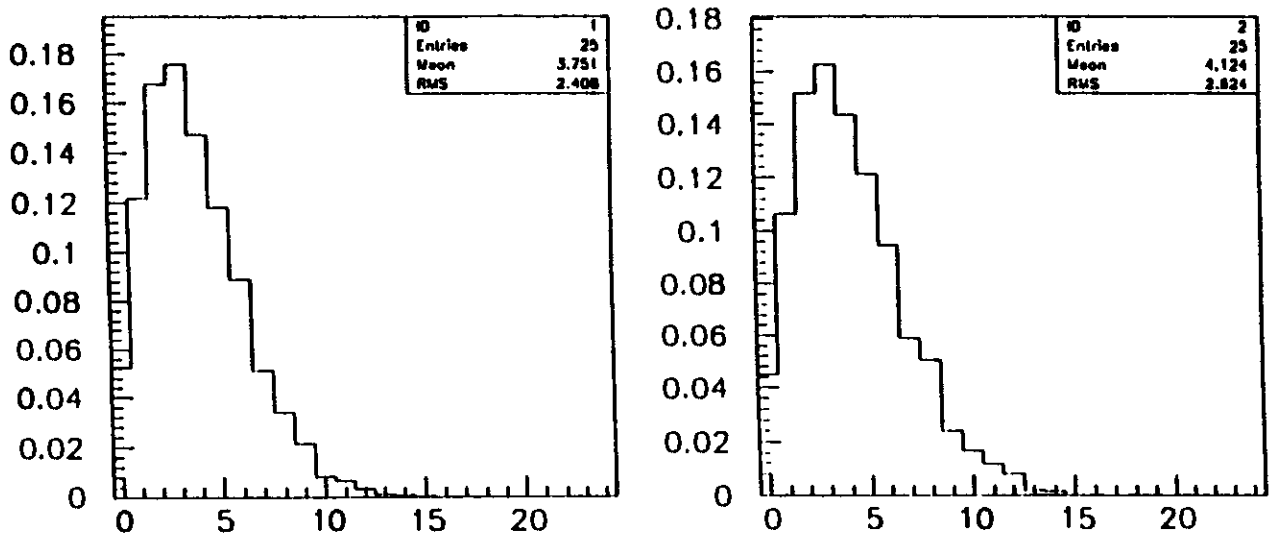

Figure 2: L2 buffer occupancy without (left) and with (right) the minimal L2 trigger accept requirement, for L1=0.003 and L2 =0.05.

6 Toy Model of a Front End System

We evaluate a front end system as it is described in the introduction with the following parameters

- L1 : 0.001 - 0.005
- L2 : 0.02 - 0.05
- L2 latency: 10-100 μs uniform distribution
- single crossing occupancy : 0.05 - 0.1
- t_{FMUX}: minimum distance between two L2 accept triggers 0-64 μs

- L2buffer length: 10-15

and study the performance under various changes of the parameters. The introduction of a minimal latency time between two L2 accept triggers allows the FMUX to be read out completely for one event before the next event is acquired. This way we naturally get ordered events.

	L1	L2	L2rate(kHz)	L2 buffer	occup	$t_{FMUX}(\mu s)$	hits-lost(%)	wait(%)
1)	0.001	0.02	1.2	10	0.05	32	0	1
2)	0.001	0.02	1.2	10	0.1	32	0	1
3)	0.001	0.02	1.2	10	0.05	64	0	2
4)	0.001	0.02	1.2	10	0.1	64	0	2
5)	0.002	0.03	3.6	10	0.05	32	0	9
6)	0.002	0.03	3.6	10	0.1	32	0.3	9
7)	0.002	0.03	3.6	10	0.05	64	0	23
8)	0.002	0.03	3.6	10	0.1	64	0.3	23
9)	0.003	0.05	9.0	10	0.05	1	0.05	0
10)	0.003	0.05	9.0	10	0.1	1	3	0
11)	0.003	0.05	9.0	10	0.05	32	0.1	26
12)	0.003	0.05	9.0	10	0.1	32	4	26
13)	0.003	0.05	9.0	10	0.05	64	14	50
14)	0.003	0.05	9.0	10	0.1	64	24	50
15)	0.003	0.05	9.0	15	0.05	64	7	50
16)	0.003	0.05	9.0	15	0.1	64	12	50
17)	0.003	0.05	9.0(c)	10	0.05	64	3	50
18)	0.003	0.05	9.0(c)	10	0.1	64	14	50

Table 5: Performance of a model system.

The last column gives the percentage of L2 accepts were the minimal distance condition had to be imposed. The last two rows were made with an L2 latency distribution, between 10 and 50 μs.
Figure 3 shows the dependence of the fraction of hits lost on the trigger rate for FMUX readout times t_{FMUX} of 1, 32 and 64 μs. Except for a rate of 9 kHz the losses are very small for 32 as well as 64 μs. The values were taken for the case with an occupancy of 0.1. For an occupancy of 0.05 the losses are much smaller.

As long as the FMUX can be cleared much faster than the average time difference between two L2 trigger accepts, the system does not show any degradation in the throughput

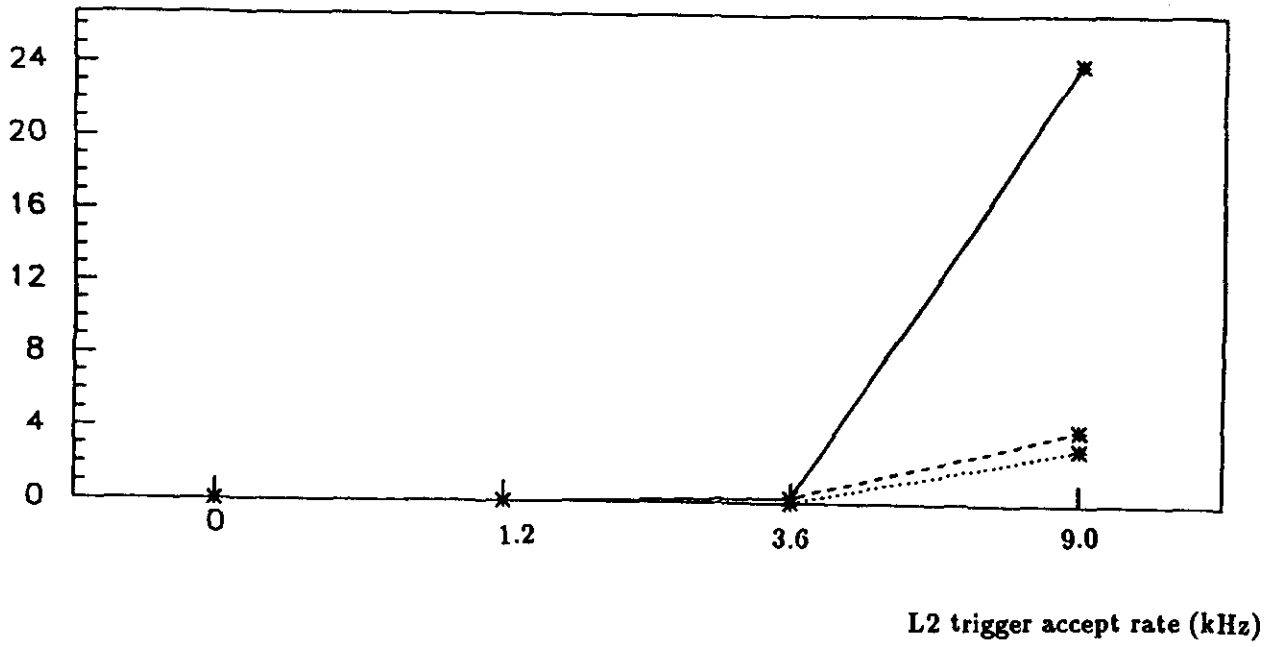

Figure 3: % lost hits in the model front end system for an FMUX readout time of 1 (lower), 32 (middle) and 64 (upper curve) μs.

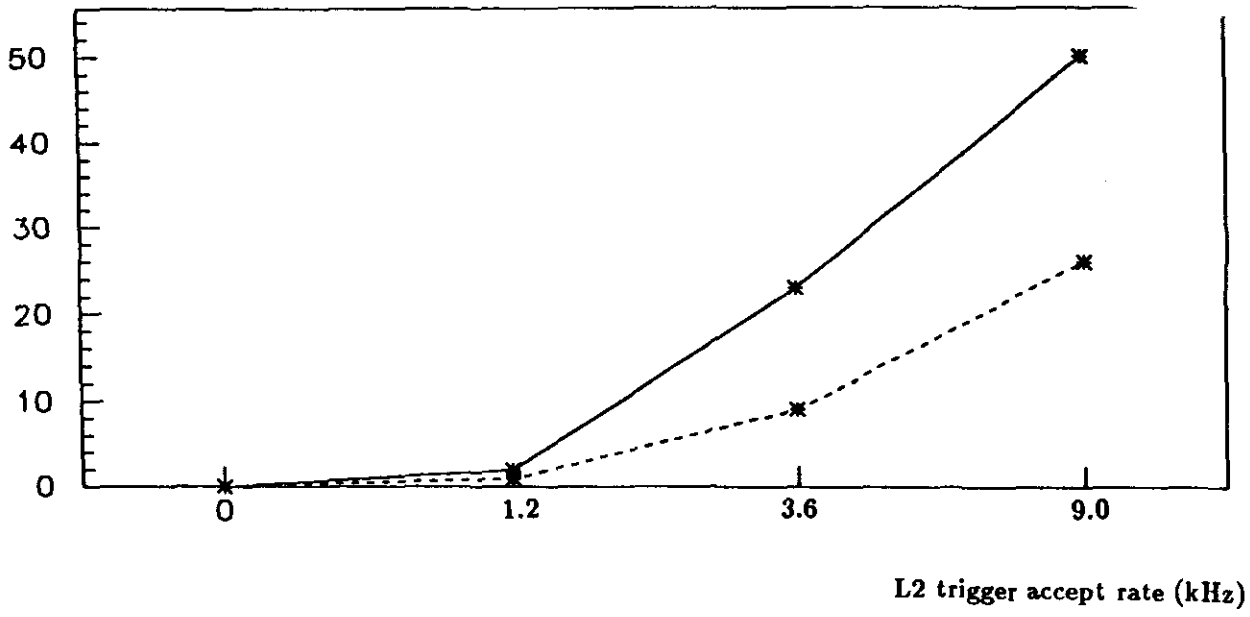

Figure 4: % of L2 trigger accepts which have to wait in order to enforce the minimal distance condition, for the FMUX readout times of 32 and 64 μs.

rate and the additional latency between L2 trigger accepts allows the events to be read out of the Front end in an ordered way. For high rates, however, the t_{FMUX} introduces more deadtime (compare 9)-14)). However, these high rates are probably prohibitive.
The L2 trigger delay has to be done in a local trigger distribution box unless other detector parts have similar requirements and this becomes a general requirement for the trigger logic. Figure 4 shows the percentage of L2 accept triggers which had to be delayed, to enforce the FMUX readout time distribution.

If ones requires that the system should be capable of sustaining a L2 triggger accept rate of 10 kHz with less than 10% losses, one can deduce that the FMUX's have to be read out in about 50 μs. On each Front end card there are up to 6 FMUX's, which have to be connected to the Crate Interface Card (CIC), which is located outside the calorimeter. In the present design studies there are two options to read out the FMUX's. Firstly one connects each of the up to 6 FMUX's on one Front seperately to the CIC. This translates with the formula given in chapter 4.1 to a bandwidth for the link from one of the FMUX's of

$$\text{bandwidth}(\text{FMUX} \rightarrow \text{CIC}) = 0.2 - 0.4 \text{ Mbyte/s}$$

Secondly one would read out the FMUX's over one Front end transmitter (FETX), which sends the data over one cable to the CICs. This would imply a six times larger bandwidth for the connection of the FMUX's to the FETX and the FETX's to the CIC of

$$\text{bandwidth}(\text{FMUX} \rightarrow \text{FETX} \rightarrow \text{CIC}) = 1.2 - 2.4 \text{ Mbyte/s}$$

7 Conclusions

In this note we have evaluated the buffer requirements at various stages of the front end system. We also have shown that without much additional burden a minimal distance of 30-60 μs between 2 L2 accept triggers can be imposed. This would leave enough time to read out the FMUX's for one event and get naturally event ordered datasets. The performance of the system degrades rapidly as soon as the rates come close to the final throughput.
The L1 buffer pipeline requires 24 storage locations for an occupancy of 0.05 per crossing and 32 storage locations for an occupancy of 0.1. The L2 buffer should be conservatively dimensioned to 10 storage locations per channel, including the additional burden due to the FMUX readout latency. In this scheme the FMUX buffer requirement is minimal.

References

[1] P. Sinervo et al., *SSC Front End Simulations* Forth Worth Symposium 1990.

[2] G.Stairs et al., *Front end Collector Bus Design Description*, UofT-DCC-03, Jan. 1992 (unpublished).