SDC-92-242

SDC
SOLENOIDAL DETECTOR NOTES

DIVISION OF DCC FUNCTIONALITY BETWEEN FE INTERFACE AND DAQ INTERFACE

January 20, 1992

A. Holscher, G. Stairs and P.K. Sinervo
University of Toronto

UOFT-DCC-04

Division of DCC Functionality Between FE Interface and DAQ Interface

A. Hölscher, G. Stairs and P. K. Sinervo
University of Toronto
Toronto, Canada

January 20, 1992

Abstract

We present arguments for how to divide the functionality of the DCC system for the SDC straw tube tracker between the part of the system near the detector and the part which forms the interface to the DAQ system.

1 Introduction

In a previous note [1], we described an architecture for the data collection system for the SDC straw tube tracker that consists of 1) a Front End Readout Controller (FERC) located on the board carrying the front end readout circuits (*e.g.*, the TVC/AMU or TMC chips) and 2) a Data Collector (DC) located some distance off the detector that provides the interface to the SDC DAQ system. We outlined what we believed to be the most effective way to share the functionality of the entire DCC system between the FERC and DC. In this note, we wish to elaborate in more detail on this point.

2 Summary of DCC Functionality

The DCC system was assumed to have the following functionality:

- collection of data from a group of FE chips after receipt of a L2 trigger accept, with the data for a given trigger being presented to the DAQ system in a single packet,
- monitoring and error detection of the basic operation of the FE chips,

- the data collection would be essentially data-driven, with each FE chip generating data asynchronously, and
- the distribution of the high-speed control signals required by each FE chip, as well as the slow control signals used for any downloading of information, control or monitoring tasks.

3 FERC Versus DC Functionality

The FERC can be viewed as being either a simple multiplexor that acts as a data-driven pipeline funnelling the digital information from a collection of FE chips to a buffer in the DC, or as a more complex device that first packages the information from the FE chips into "packets,", where each packet contains data from all the channels on the FE readout card for a specific trigger. Other scenarios are possible, but these appear to be the most practical.

The advantage of the simple multiplexor is that it makes the FERC a less complex device in principle, since many functions are effectively off-loaded onto the DC. However, this architecture places the greatest data management load on the DC, which is required to have a throughput that could be up to $\sim$ 100 Mb/s (assume 200 channels per FE chip, an occupancy per trigger of 0.3 hits/channel, 6 bytes of information per hit, each DC module reads out 32 FERC's and a maximum L2 trigger rate of 10 kHz). In addition, the actual savings in complexity of the FERC may not be that large, as the FERC will be required to do a modest amount of monitoring and error detection.

On the other hand, the disadvantage of the more complex FERC is that the greater complexity may create an electronic noise problem when placed in proximity to the very sensitive FE readout. This issue can only be resolved by detailed prototyping in order to determine what limitations noise generation places on the digital activity on the FE card.

4 Overlapping Hits

One problem that has been discussed at some length is what to do with hits that may be associated with two or more interactions. The overlap probabilities have been calculated by A. Hölscher [2], and the conclusion is that this aspect may cause a problem only in the case of very high occupancy systems and/or detector readout times that are quite long relative to the SSC bunch crossing frequency.

Detailed consideration of how one can handle this problem indicate that it is very difficult to resolve once one has packaged the data into event packets (where all the data is supposed to come from one interaction). The computing required to sort out this ambiguity is also non-trivial. Initial estimates indicate that this load could be handled at the FERC level by currently available DSP's, making such devices obvious candidates for the FERC computing engine.

We thus believe that the most appropriate level to resolve this ambiguity is at the FERC level and not to postpone it to the level of the DC, where the large bandwidth capability forces any computation to take place in parallel. A specific scheme to perform this task has been outlined by G. Stairs [3]. Since the FERC already will have to be a computing engine of some sort (to do the error detection and monitoring task), it seems most expedient to add this parallel processing at this point rather than a separate device in the DC (or the datapath between the FERC and DC).

5 Conclusion

We helieve that the most cost-effective division of functionality between the FERC and DC is to have the FERC do a modest amount of data manipulation and produce packets of data, where each packet contains all the data for a given trigger. Further prototyping will allows us to evaluate whether such a solution is consistent with the noise limitations imposed by the FE chips.

References

[1] G. Stairs and P. K. Sinervo, *Design Options for an SSC Wire Chamber Data Collection System*, UOFT-DCC-01, Oct. 1991 (unpublished).

[2] A. Hölscher, *Overlap Probabilities*, UOFT-DCC-02, Jan. 1992 (unpublished).

[3] G. Stairs, *Front End Collector Bus Design Description*, UOFT-DCC-03, Jan. 1992 (unpublished).