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A NEW APPROACH IN DEVICE TESTING

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Abstract. **The note shows results of tests of a TDC chip using the traditional test method that give global performance as well as a new visualization technique. 200 million tests have been performed (1.3 Gbyte of data acquired). Each TMC cell has been tested under several conditions and several times for each condition, with supply voltage ranging from 2 Volt to 3.5 Volt and frequency ranging from 20 MHz to 75.75 MHZ. This visualization technichue relates a deviation from expected results to a specific area of silicon on the chip and at the same time shows its global performance. In addition, by using animation, one can observe behavior as a function of an additional variable (such as power supply voltage or clock speed). Animation gives the point where performance degrades, and one can locate a specific area of silicon which is failing, from a particular slice in the animation sequence. Results of the test of a TDC chip TMC1004 are then summarized. The tools used can quickly detemine its properties as well as spotting problems and exploring the dynamic range of operation. The technique is general and permits more in-depth study. As a result of fairly extensive testing, the TDC chip does erform as specified.**

I. INTRODUCTION

The present technique involves:

1) acquisition of several Mbytes of data from the Device Under Test (DUT).

2) representation of the acquired data in graphical form in such a way that the main characteristics such as lineaity, integral linearity, differential linearity, time resolution and accuracy can be visualized much like a small experiment.

A complete test of a chip involves not only characterization of a new chip derived from R&D, but also a system reliability check involving single failure rates over millions of measurements, and appropriate production tests (real time compare test, pass/fail)

Once the data is acquired, powerful graphical analysis can be performed off-line whic otherwise would not be possible. (For example, animation can help one to visualize four dimensional relations and give immediate recognition of an anomaly).

This technique can be applied to the testing of several types of components. As an example, the chip TMC1004, designed by Y. Arai of KEK (Japan) [1,2], has been tested and evaluated. The TDC chip may be used in the readout system for the straw tubes of the SDC outer tracking system. Tests have been conducted using a digital testing station, HP 82000.

Fig1 shows the logical function of the chip consisting of 32 rows, each one with 32 TMC (Time Memory Cells). The leading edge signal that must be measured with respect to the clock leading edge is presented to all TMC.

One row at a time is enabled by the write/read pointers from an external clock with a 32-ns period. A delay on the clock is provided between TMC of the same row. Since the last TMC on the right will geneate a longer clock input delay, one would expect a less accurate measurement as compared to the TMC at the left end of the row. The timing relation of the signals is shown at the top of Fig. 1.

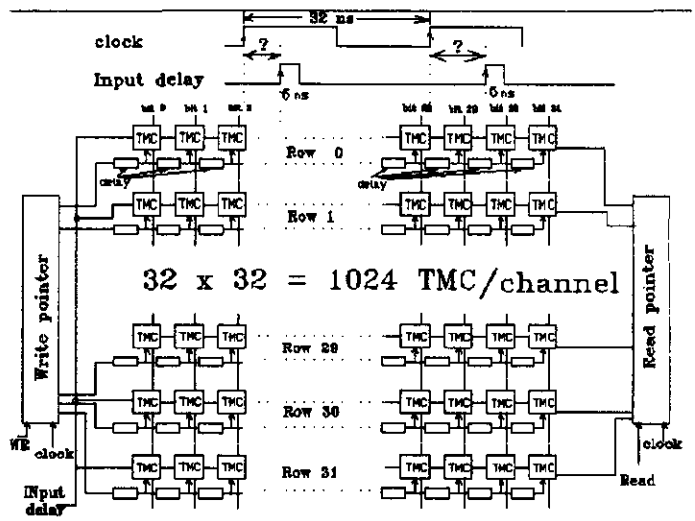

FIGURE 1. TMC1004 Block diagram.

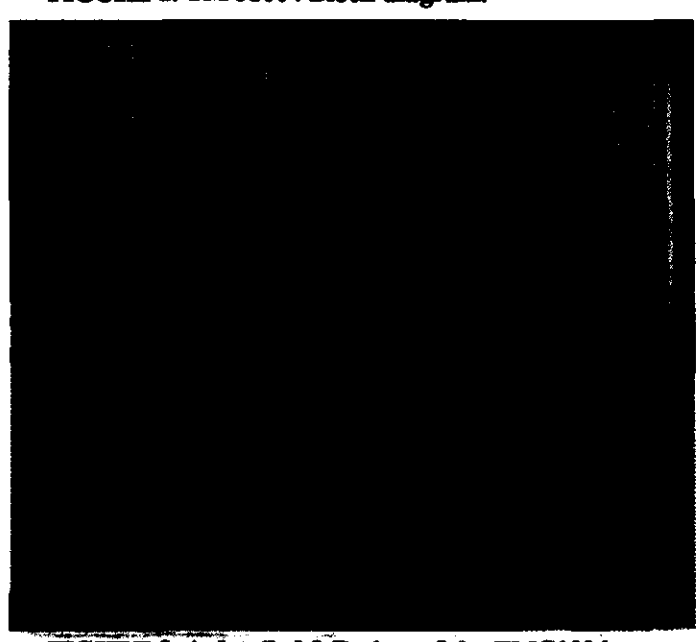

FIGURE 2. A detailed 3-D view of the TMC1004 tests.

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The features of the new visualization technique are shown in Fig. 2 and Fig. 3. The figure shows results of several tests executed under the following conditions: power supply = 3 Volts, temperature = 25 C, input delay varying from 0 to 40 ns with steps of 50 ps and clock frequency = 31.25 MHz. If a unique relation between input and output (1 ns = 1 LSC) exists, one would see no spread (nored would appear). But as shown in Figure 2, spread of output for given input is observed.

The yellow part represents the ideal response of the Time to Digital (TDC) chip TMC1004. Distance betweenyellow bars represents digital output values. The thin slices within theyellow bar represent 20 different tests. Ideally, the TDC should always give the same digital output within a given 1 ns range (=20 steps of 50 ps), but in reality the response of the chip is described by the sliced planes (each corresponding to 50 ps test). Only with some input values, we have as result of the test the same digital output value (see long red bars), for the remaining, different output are detected.

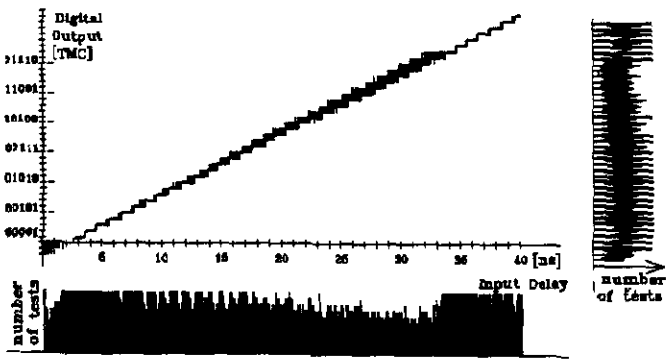

FIGURE 3. Linearity response characteristic of the TMC1004. 8000 measurements were taken (40ns/50ps x 10 times).

The bottom portion of theFig. 2 is the view of the 3-D picture the projected onto the input delay axis "x" and shows the maximum number of tests passed for a given input delay that gives the same output value. On the right is the projection along digital output axis "y". (This view is a superimposition of all input delay slices).

II. Acquire data to characterize the chip.

Tests of the TDC chip have been aquired by means of an HP82000 as follows:

1) input channels of the TDC have been pulsed with 5 ns pulse width. The leading edge of this pulse has been changed from 0 to 40 ns (with step increment of 50 ps.) delayed respect to the leading edge of the clock (see Fig 1).

2) the clock frequency to the TDC has been set to 31.25 MHz.

3) all outputs have been sampled by the HP82000 41 ns after the leading edge of the clock.

4) each input delay value has been tested ten times.

5) a check that the present setup is working properly is then performed by usiag, the built-in functions of HP82000 (state list and timing diagram).

6) a simple data acquisition program has been written wherein the functionality determined in step 5 is automated and raw data is file-stored.

III. Offline data manipulation

The acquired data can be manipulated and displayed on a graphic terminal by displaying a sequence of pictures that shows symptoms of failure of the chip as the animation sequence variable, such as: the clock frequency or the voltage is varied.

One expects the new technique (making use of different display packages) to give more precise information than the previous method (Hplot/Hbook). This is the case since the raw data is not "binned", and it is not necessary to use a graphic terminal to "Query" the data points for recovering the corresponding coordinate. Measured data and ideal data are displayed with precision in 3-D. The ideal response of the TMC1004 is generated from the relation 1 ns = 1 LSC using a C program. All above described precise data can be extracted directly from the picture (see Fig. 2).

Simple checks are made by using already existing graphical tools (such as CERNLIB Hbook/Hplot, done with the help of E. Wang).

IV. Global performance measurements.

A. Linearity

In an ideal linear TDC, equal increments in the TIN delay inputs values should produce equal increments in the digital output. Linearity is a measure of deviation from this expected relationship: 1 ns = 1 LSC.

The graphic information obtained from the binned scattered plot of Fig. 4 (generated using Hbook/Hplot) has less precise informations than the graphical representation of Fig. 3.

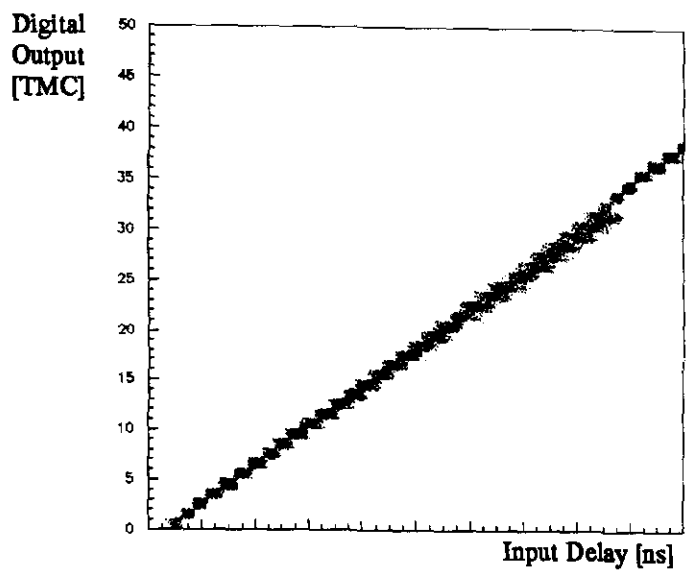

FIGURE 4. Binned scattered plot of input delay versus digital output.

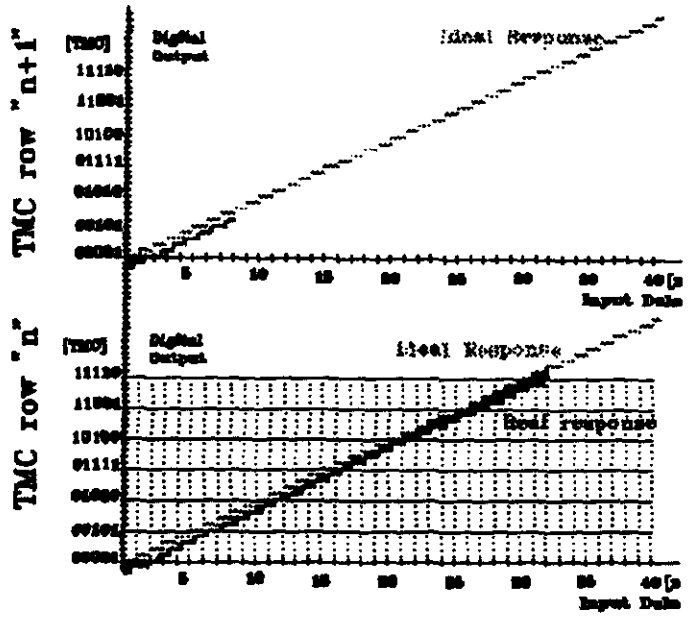

FIGURE 11. No missing code, output channels continuity across the boundary of adjacent rows.

F. Stability.

Figure 12 shows the slope change for a variation of the power supply Vdd and fix frequency (31.25MHz).

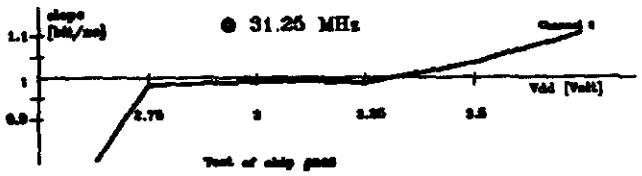

FIGURE 12. Slope variation at different Vdd

G. Cross-talk measurement.

Several million tests have been performed by applying a signal to 3 inputs out of four available and then sampling the four output channels. Zero noise cross talk has been detected. Fig. 11 shows the zero output value for channel 1 (which did not have input applied).

H. Slope measurement of all rows and all channels.

Figures 14 and 15 show the slope response of the different rows (32x4 channels) in the respective chip N. 60, N.211 at the frequency of 31.25 MHz and Vdd = 3 Volt. For each data point displaying the slope (Fig. 14, 15), 8000 measurements have been made. Only the central part of the response (2-30 ns) has been considered for the slope calculation. Weights related to different output response of several measurements at the same condition have been included to obtain greater precision.

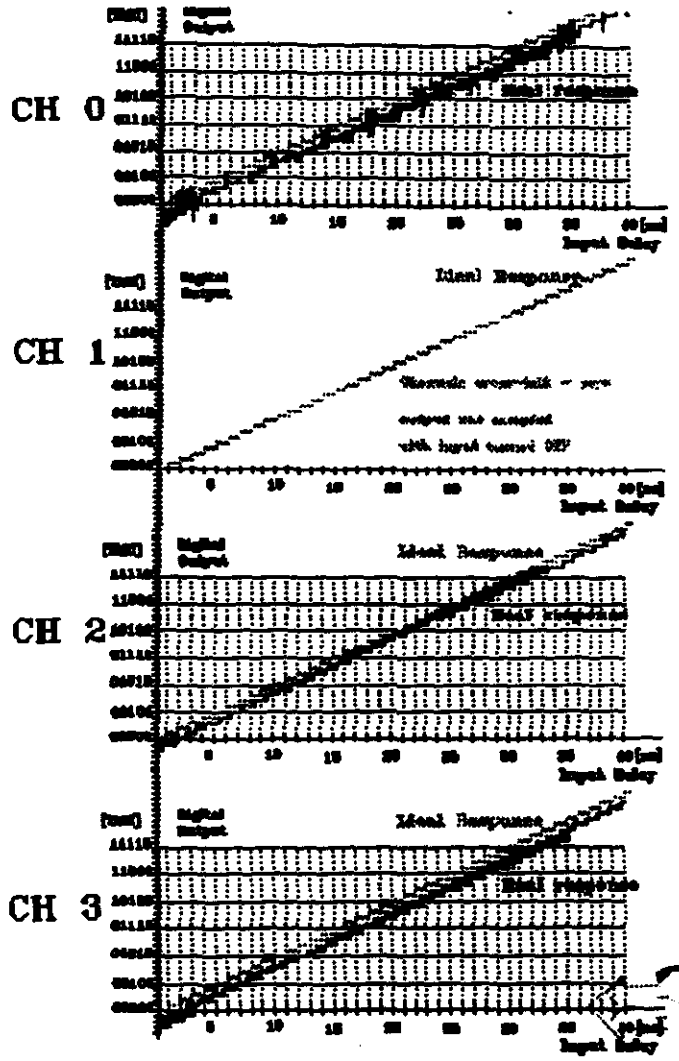

FIGURE 13. Zero cross-talk

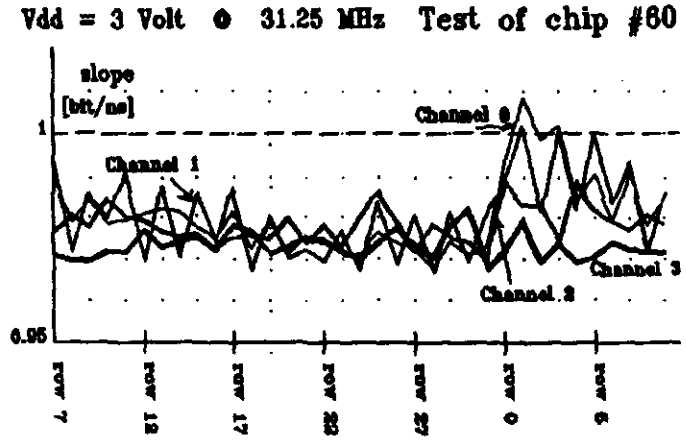

FIGURE 14. Slope measurement of 128 rows (32 x 4 channels) of chip N. 60.

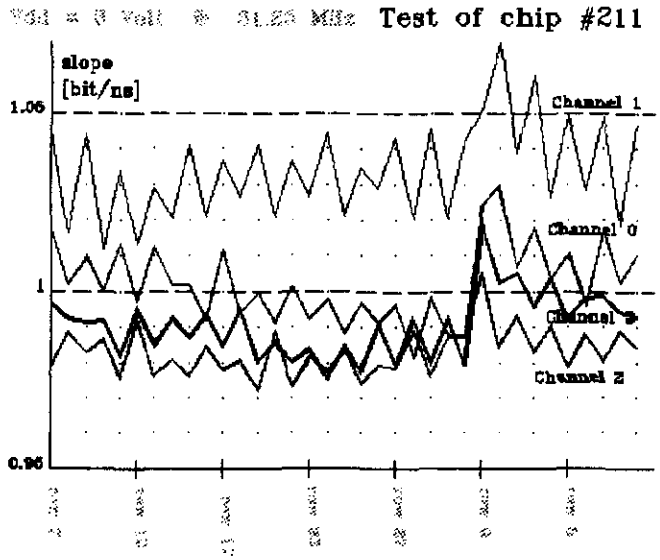

FIGURE 15. Slope measurement of 128 rows (32 x 4 channels) of chip N. 211.

L. Slope response at different frequency.

Fig. 16 shows a the slope change by varying the frequency and wdith Vdd = 3Voll.

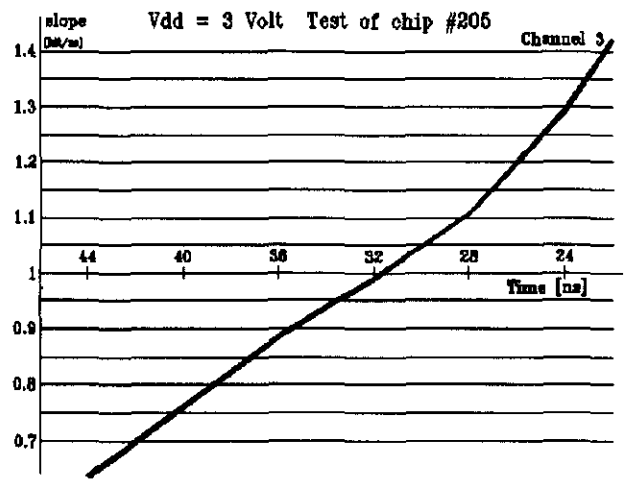

FIGURE 16. Slope response at different frequency.

M. Frequency and voltage operating range.

When the TMC1004 Time-to-Digital converter is tested at conditions different from the typical ones, the chip behaves as one would expect.

Two types of measurements have been performed:

1) a complete scan from the lowest frequency and voltage to the highest, in order to find out the operating range of the chip. Also, in order to see which type and which area of chip caused the first failures.

TABLE 1. Measured Performance

No. Channel	4
Least Time Count	1 ns/bit
Time Range	1024 µs (4 channels)
	2048 µs (2 channels)
	4096 µs (1 channel)
Clock Frequency	31.25 MHz
Time Resolution	$\sigma = 0.50$ ns
Integral Linearity Error	< 1.3 bit
Differential Linearity error in a row	< 0.2 bit
Row-to-row Discontinuity	< 0.5 bit
TMC Array-to-array Discontinuity	< 1 bit
Variation of Slope	< 0.1 % (2.75 - 3.25 Volt
(time-to-digital conversion factor)	< 0.1 % (chip to chip)
Data Output	32 ns cycle
Supply Voltage	3 Volt

2) a more refined measurement of the slope, sigma,etc. at the typical frequency and voltage has also been performed in order to check its functionality.

Figure 17 shows a good response of the TDC at 55.55 MHz. (there is no single failure in a complete row.

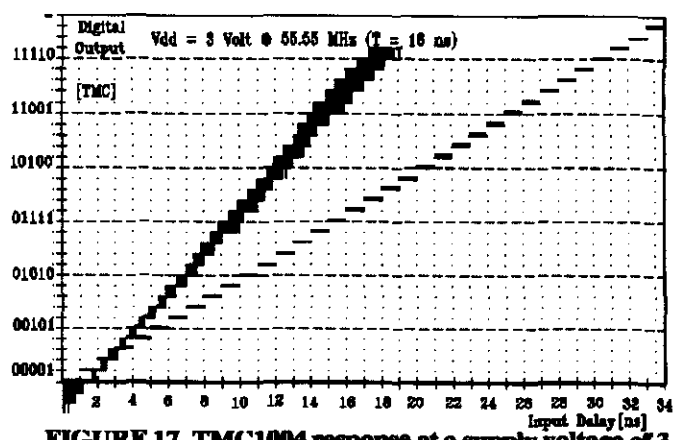

FIGURE 17. TMC1004 response at a supply voltage of 3 Volts and at the frequency of 55.55 MHz.

The data acquired permits visualizing the behavior of any TMC cell. Starting from frequency of 20.83 MHz to 75.75 MHz, the Least Time Count is decreased from >1 ns/bit to <1 ns/bit. The typical value of 1 ns/bit is given at 31.250 MHz (see Fig.3).

For clarity, only part of the data related to a few rows has been displayed in order to show when the TMC1004 begins failing and which part of the silicon is failing first.

For lower frequency and lower power supply voltages, the spread of output significantly increases. On the other hand, by increasing the frequency and voltage, the chip fails only at frequencies higher than twice the typical one (see Fig. 18).The first area of silicon that fails is the one related to the TMCs for short measurements. This area is the one related to the right part of TMC block scheme of Figure 3.

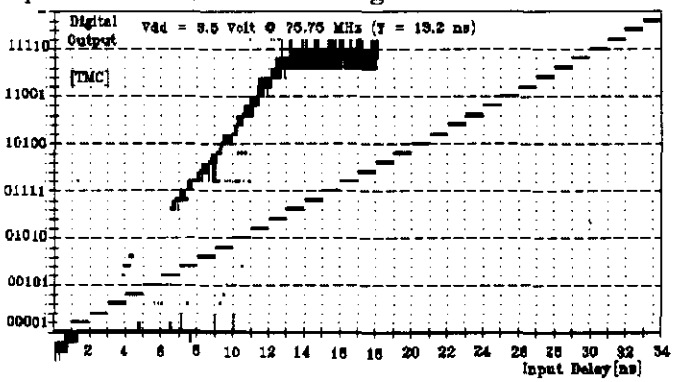

FIGURE 18. TMC1004 response at a supply voltage of 3.5 Volt and at the frequency of 75.75 MHz.

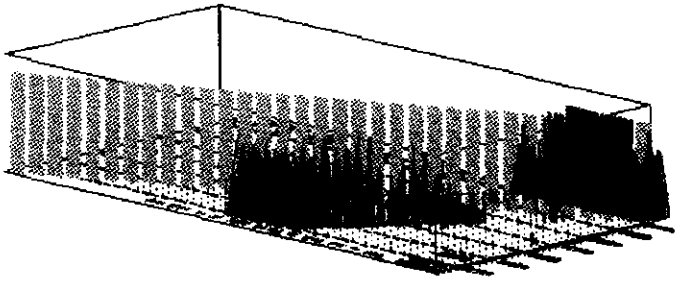

FIGURE 19. A 3-D view of Fig. 18.

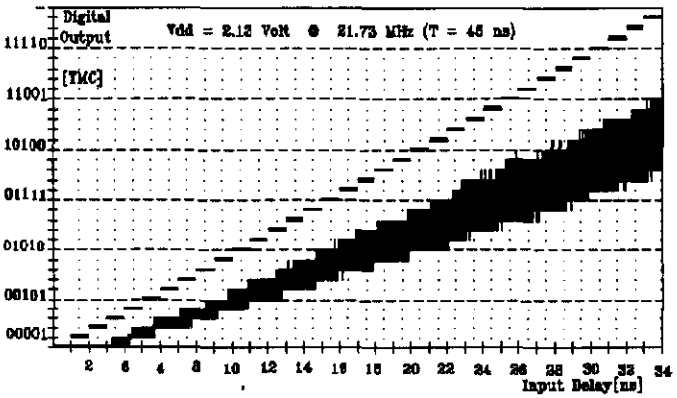

FIGURE 20. TMC1004 response at supply voltage of 2.13 Volt and at the frequency of 21.73 MHz.

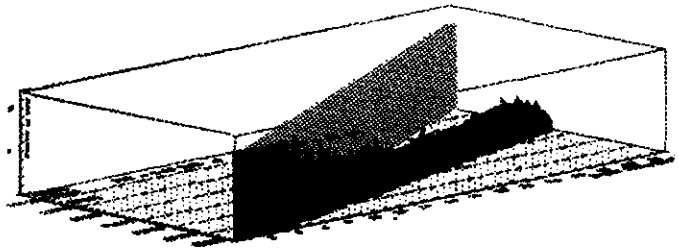

FIGURE 21. A 3-D view of Fig. 20

The animation associated with this test (delivered on MSDOS floppy disk) plays in one real-time minute, and is the result of 100 million measurementsaccumulated for seve days. The user immediately recognizes anomalies in the c cuits when voltage and frequency are applied out of the operating range.

Futhermore the user can see with the animation the relationship between five variables. For examples, the following assignments have been made:

- axis "x" = input delay
- axis "y" = output value
- axis "z" = number of tests
- color = power supply voltage
- animation = clock frequency

The problem of a single output data failure is clearly evident.

VI. CONCLUSION

The overall performance of the chip is satisfactory. It has low power consumption. It operates with good response for supply voltage ranging from 2.75 to 3.25 Volt (see Fig. 12). The linearity within a row is good. within 4% (see Fig.14 The frequency is proportional to the LSC step (see Fig. 16).

The TMC1004 has a wide tolerance to variation of parameters such as voltage, clock speed, etc. It has been designed to measure 1 ns step and output 1 digit for each ns delay increment at the input.

The linearity is good and the offset shown in the figures c be corrected by external digital logic (DSP) during pedes subtraction.

The extensive tests on the three different chips agree with the results described in reference [1,2], but limits obtained for this report are wider. The best performance was seen in chip N. 60 (see Fig 14).

The present testing methodology visualization tectnique [3] and the facility used for this test (hardware and software) are modular and can partly be used for tests of other chips such as ADC, DAC, etc.

Acknowledgements

I would like to acknowledge E. Wang and J. Lonon for their help on the data analysis.

References

[1] Y. Arai, M. Ikeno and T. Matsumura: "Development of a CMOS Time Memory Cell VLSI and CAMAC Module with 0.5 ns Resolution," Submitted to the 1991 IEEE Nuclear Science Symposium, Santa Fe, Nov. 1991 KEK Preprint 91-202.

[2] Y. Arai, T. Matsmura and K. Endo; "A CMOS 4 ch x 1 k Time Memory LSI with 1 ns/bit Resolution", IEEE Jour of Solid-state Circuits, Vol. 27. No. 3, March 1992.

[3] D. Crosetto, SSCL Physics Research Div., Technical Note N. 9, February 25th, 1992.