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SDC
SOLENOIDAL DETECTOR NOTES

A PIPELINED DOMINO LOGIC 4 x 12 BIT ADDER

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A PIPELINED DOMINO LOGIC 4 X 12 BIT ADDER

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I. Introduction

The purpose of this project is the fabrication of a 4 12-bit numbers adder using CMOS 1.2 μm technology. It is proposed for computing the pipelined energy sums in the SDC level 1 trigger system. The adder is designed to work at a minimum 28 ns latency, and 14 ns throughput. The design of choice uses domino logic, and the circuit is conceived as a two stage pipeline.

II. Specifications

Inputs: - 4 - 12 bit operands;
- mode ("1" – the shift registers send out their content at the serial clock rate; "0" – the output of the pipeline first stage is loaded in parallel into the shift registers);
- serial clock (gives the timing for shifting out the content of the shift registers);
- phi (the circuit clock: period > 28 ns and 50 % duty cycle) – 1 pin;
- dly1 and dly2: signals coming from the 4– and 10– ns delay lines to from the internal phases phi1 and phi2 required by the domino logic implementation;
- TOTAL INPUT PIN COUNT: 53

Output: - 12 bits, the result of the addition;
- carry out (cout);
- tst0 and tst1 (the outputs of the shift registers);
- phi1 and phi2: outputs provided to trim and to test the internal phases phi1 and phi2;
- TOTAL OUTPUT PIN COUNT: 17

Power supplies: - +5V (Vdd) – 3 pins
- GND – 3 pins

TOTAL PIN COUNT: 76

III. Circuit description

The circuit is a four 12-bit numbers adder. Is built using domino logic design and it has a two–stage pipeline structure. Fig. 1 shows the block diagram of the circuit.

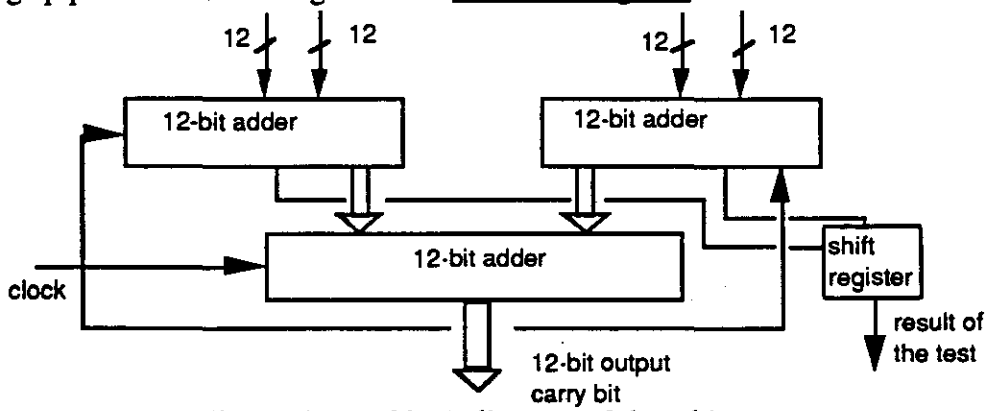


Figure 1. The block diagram of the adder

Since the computation of the carries can slow down the computation we decided to use carry lookahead technique for the basic cell, which is a 4-bit adder, and carry select technique for the overall adder. We motivate this decision based on the fact that the computation time for carry lookahead addition is proportional to $O(\log_2 n)$ while the time for carry select addition is proportional to $O(\sqrt{n})$, thus for $n = 12$ the carry select provides a better execution time.

The first stage of the pipeline performs 2 12-bit additions in parallel and buffers all the 4 12-bit numbers.

The second stage of the pipeline adds the results coming from the first stage and also computes the carry out.

To test the first stage of the pipeline we used 2 shift registers which, when mode = 1, send out the output of the first stage of the pipeline. We used this simple testing procedure to maximize the speed of the circuit.

The floor plan for the circuit is given in fig. 2.

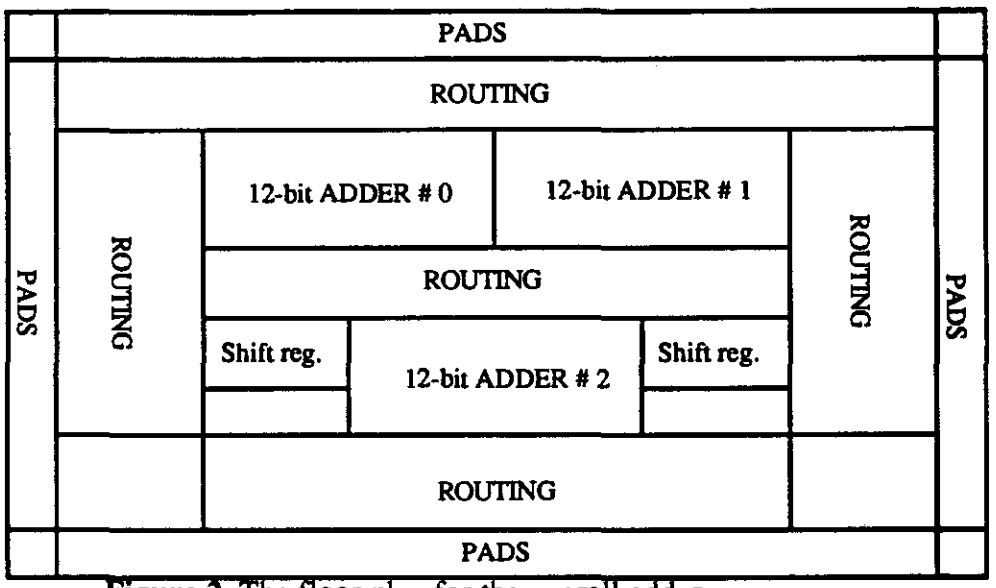


Figure 2. The floor plan for the overall adder

The power is fed from the top and the GND is brought at the bottom. 3 pins are used for each of the Vdd and GND connections. The area of the circuit is 1425 X 5510 (μm^2) and the transistor count is 6639.

The basic cell of the circuit is the 12-bit adder. Its floor plan is given in Fig. 3 (a).

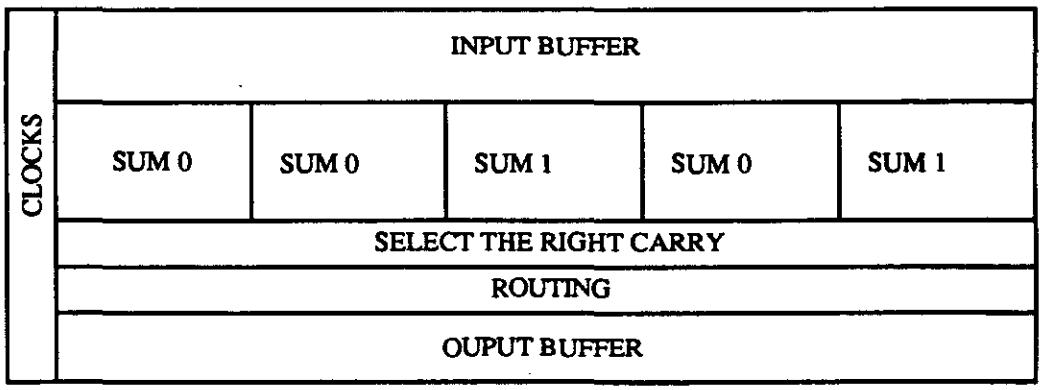


Figure 3 *(a)* The floor plan for the 2 X 12-bit adder cell

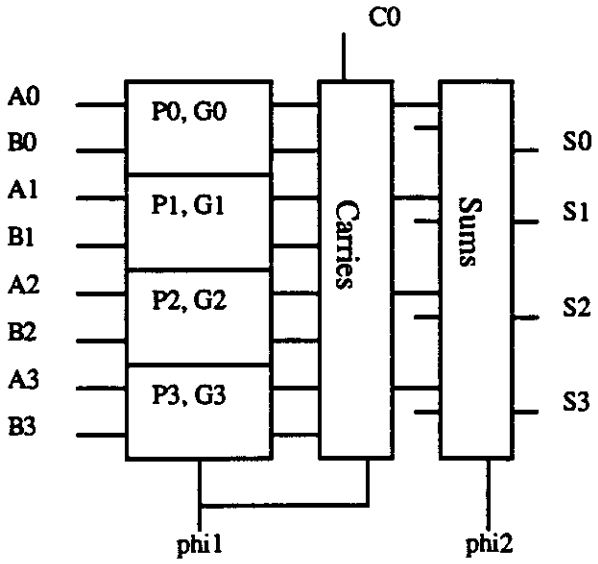
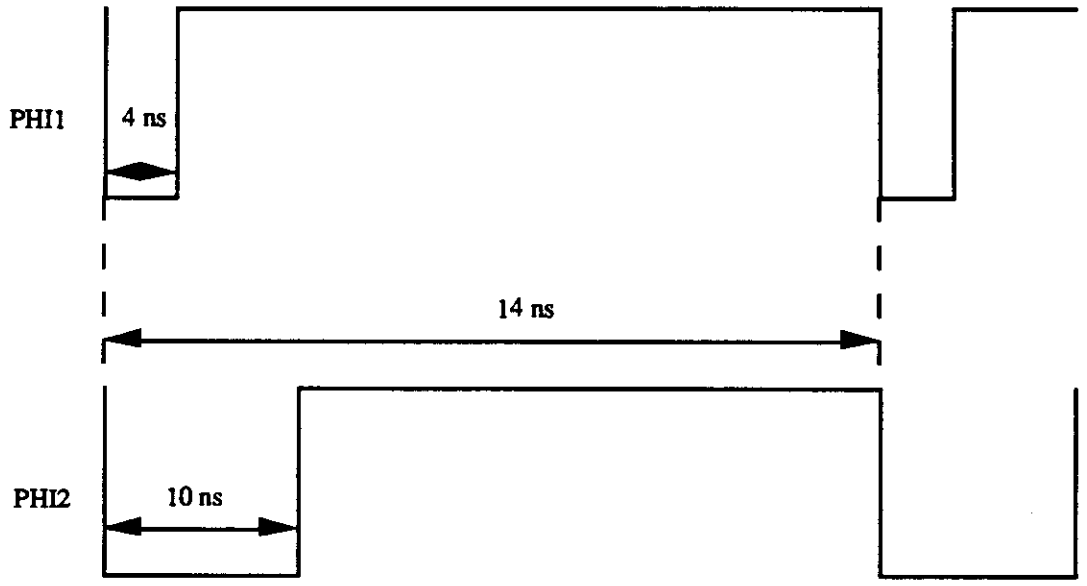


Figure 3 *(b)* The structure of the 2 X 4 bit adder

To obtain the 4-bit adder we generated p0 - p3 and g0 - g3, then we computed the carries c1 - c4, and, using c0 - c3, the sums s0 - s3. The carry out bit, c4, was used to select the correct result of the next stage. Figure 3 (b) presents the block diagram of the 4-bit adder. The adder SUM 0 was obtained by connecting c0 to 0 and c0_bar to 1. The adder SUM 1 was obtained by connecting c0 to 1 and c0_bar to 0. The two phases that clock the adder are generated in accordance to the timing diagram given below:



IV. Layouts

Figure 4 shows the layout of the adder (the topmost cell is represented). Adder.1 and adder.2 form the first stage of the pipeline. The second stage contains only adder.3. The shift

registers used for testing are on the sides of the adders. The 6 clock drivers (the small rectangles) are represented as well.

Figure 5 shows a view of the 132 ceramic PGA used to encapsulate the circuit. We used a 132 PGA, although the circuit has only 76 pads, to minimize the cost of the fabrication, making sure that in this way we did not compromise the expected performance of the chip (the remaining pins, up to 132, are not connected).

Figure 6 presents the layout of the shift register used for testing.

Figure 7 shows the layout of the clock driver.

Figure 8 shows the layout of the 2 X 12 bit adder.

Figure 9 shows the layout of the main cell used to create the 2 X 12 bit adder, this is the 2 X 4 bit adder.

Figure 10 shows the layout of an input pad. The output pad are similar except that the Enable signal (internal signal) is connected to allow the outward transfer of the signals.

V. Simulations

We simulated all the subcircuits in the adder by SPICE and IRSIM. Adding up the individuals times obtained from the SPICE simulations we obtained 13.5 ns minimum throughput for the overall circuit, using 1 kΩ and 10 pf load on the output pads. However problems might appear since we could not account for the effects of the internal heating which is likely to occur. From these simulations we estimate that the dissipated power, at a 14–ns clock, is around 1.5 W.

VI. Testing

The performance test has to be done for worst case which is given by the following combination (which was used in the IRSIM simulation of the circuit):

FIRST CLOCK PERIOD	NEXT CLOCK PERIOD
#1: 1111 1111 1111	#1: 0101 0101 0101
#2: 1111 1111 1111	#2: 1010 1010 1010
#3: 1111 1111 1111	#3: 0101 0101 0101
#4: 1111 1111 1111	#4: 1010 1010 1010

To test the circuit we use a customized tester connected to a VAX through a VME interface.

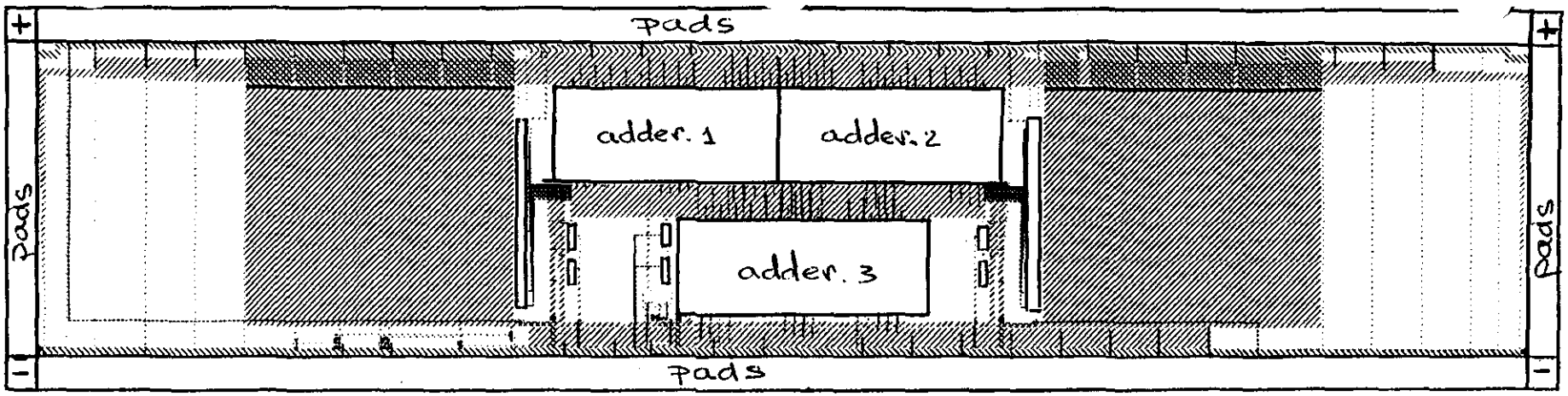


Figure 4. The layout of the circuit (topmost cell). Adder. 1 and adder. 2 form the first stage of the pipeline. Adder. 3 forms the second stage. The shift registers for testing are on the sides of the adders. There are 6 clock drivers.

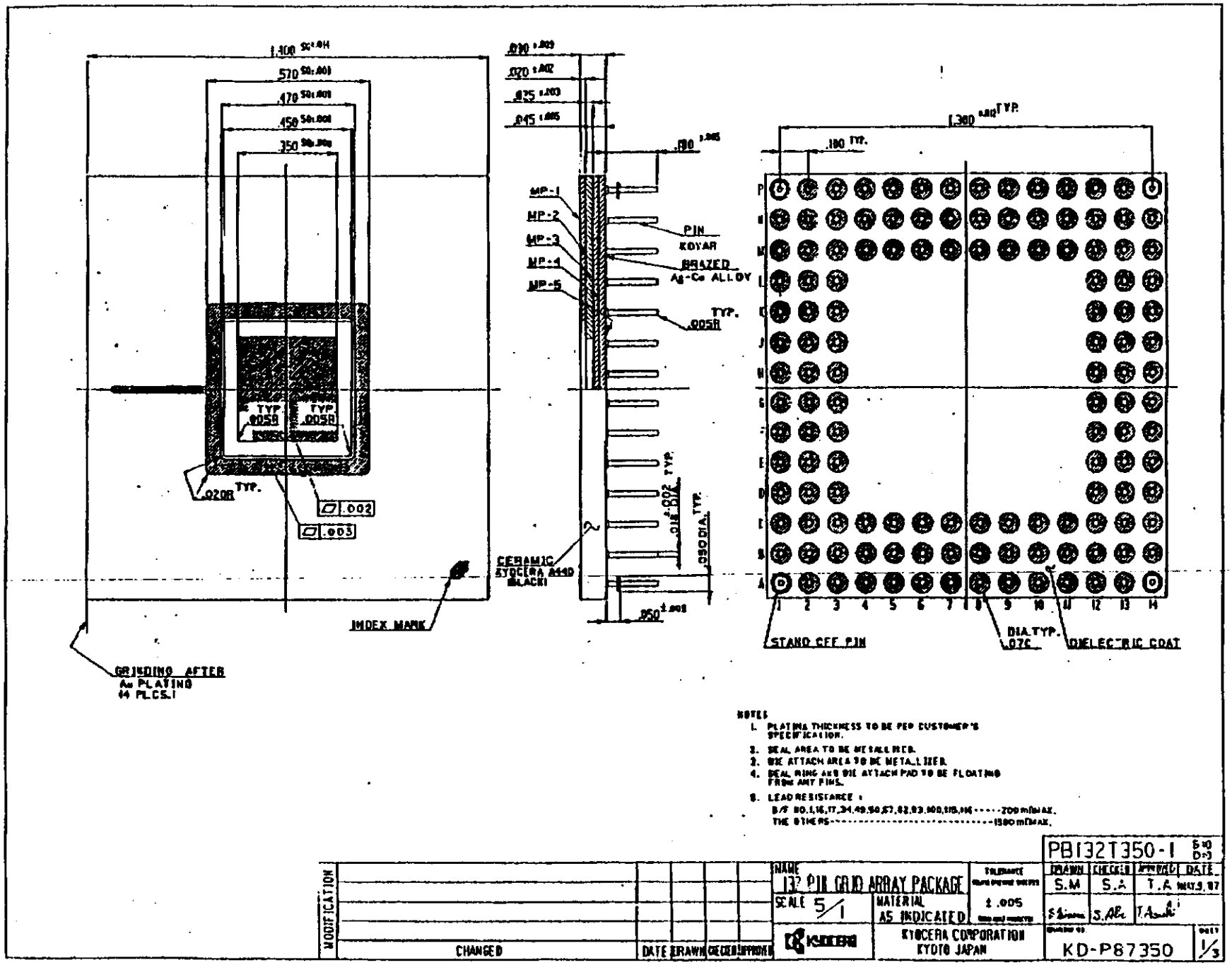


Figure 5. View of the PGA used for encapsulation

Figure 6. The layout of the shift register used for testing

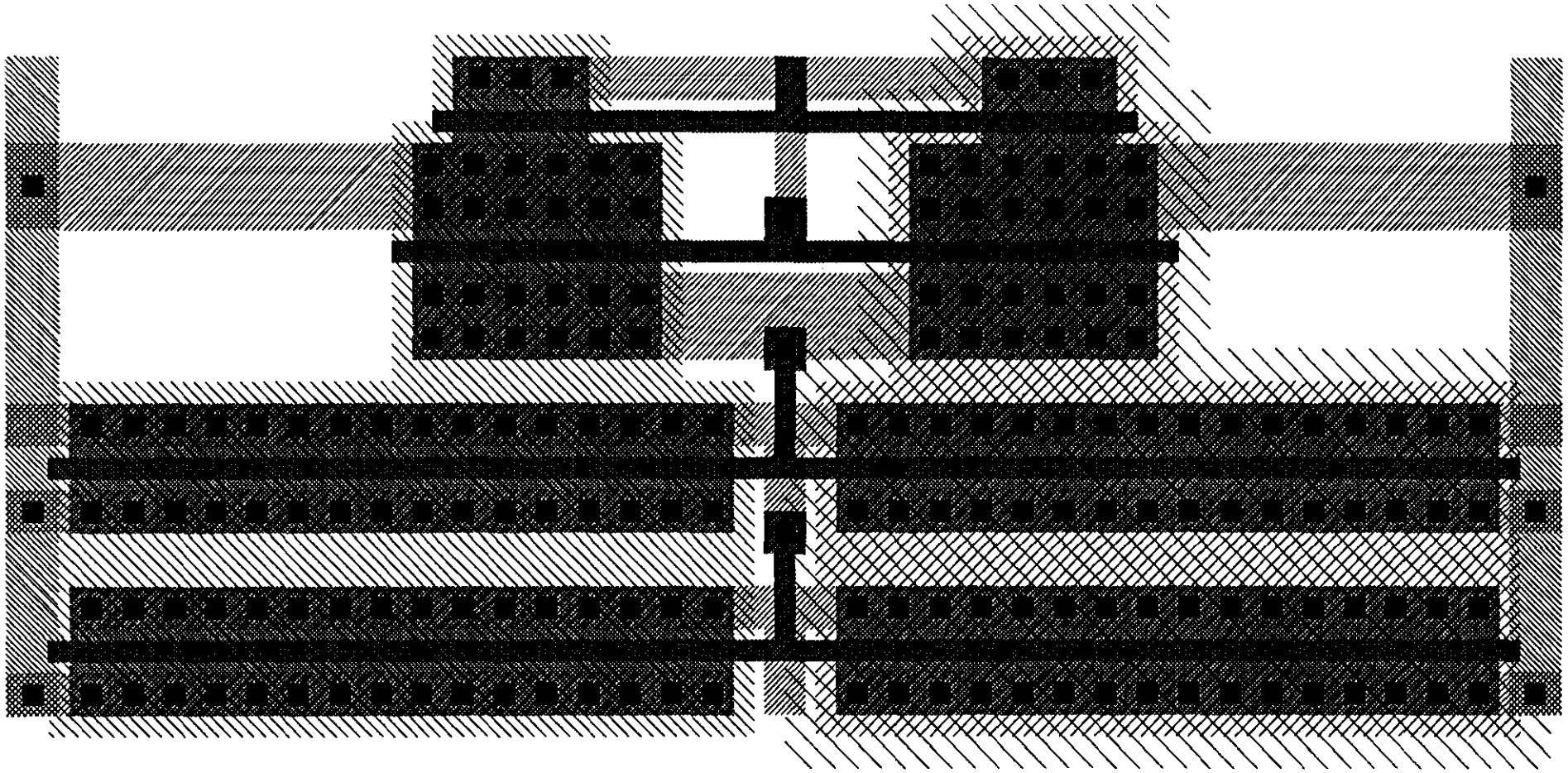


Figure 7. The layout of the clock driver.

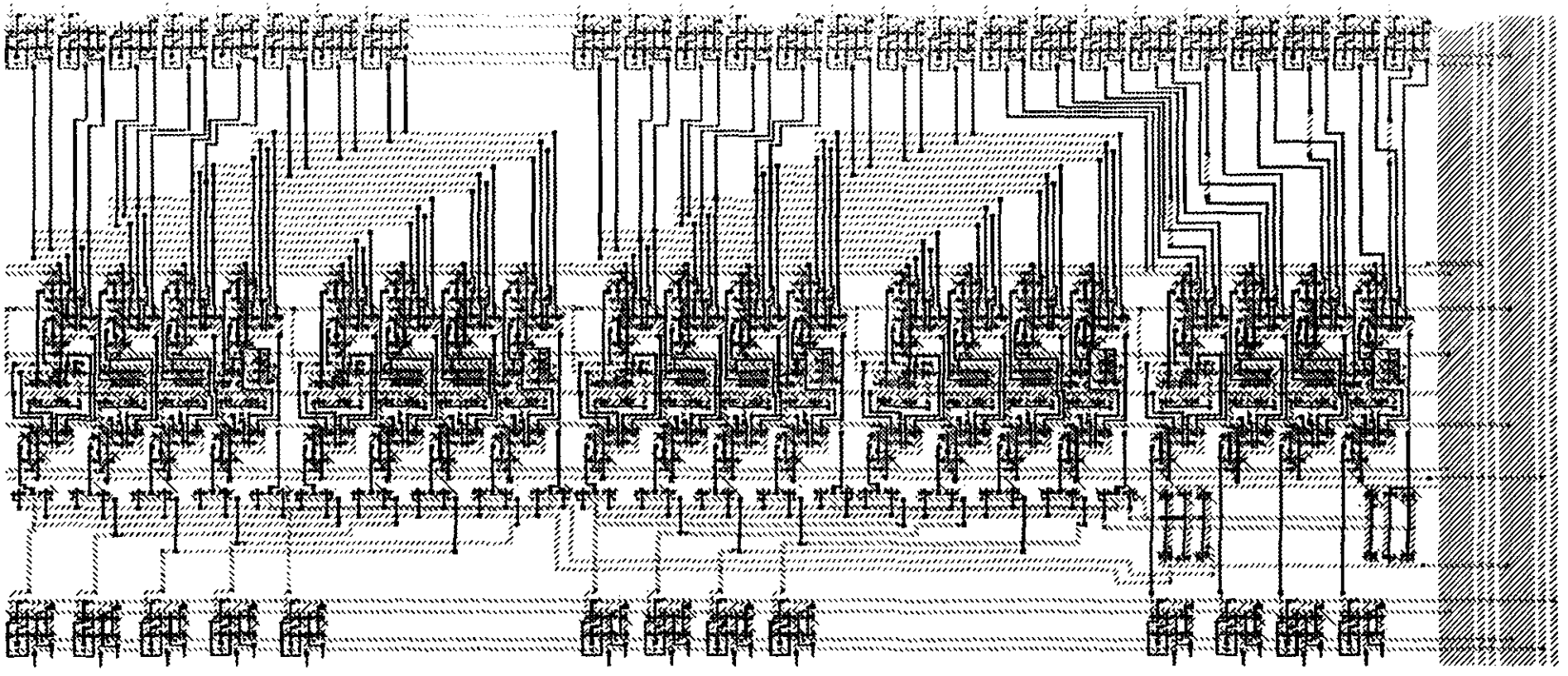


Figure 8. The layout of the 2x12 bit adder

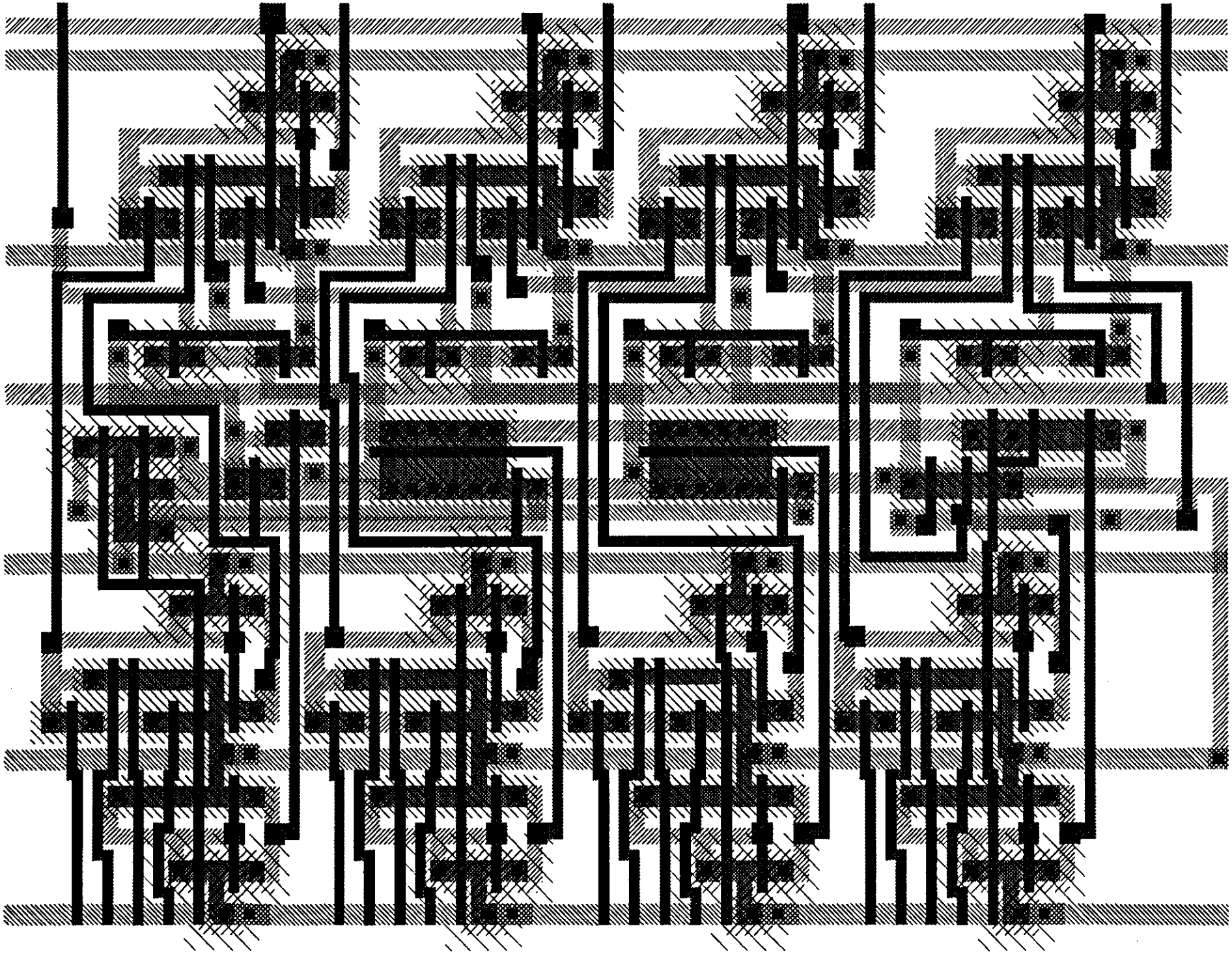


Figure 9. The layout, the 2×4 bit adder.

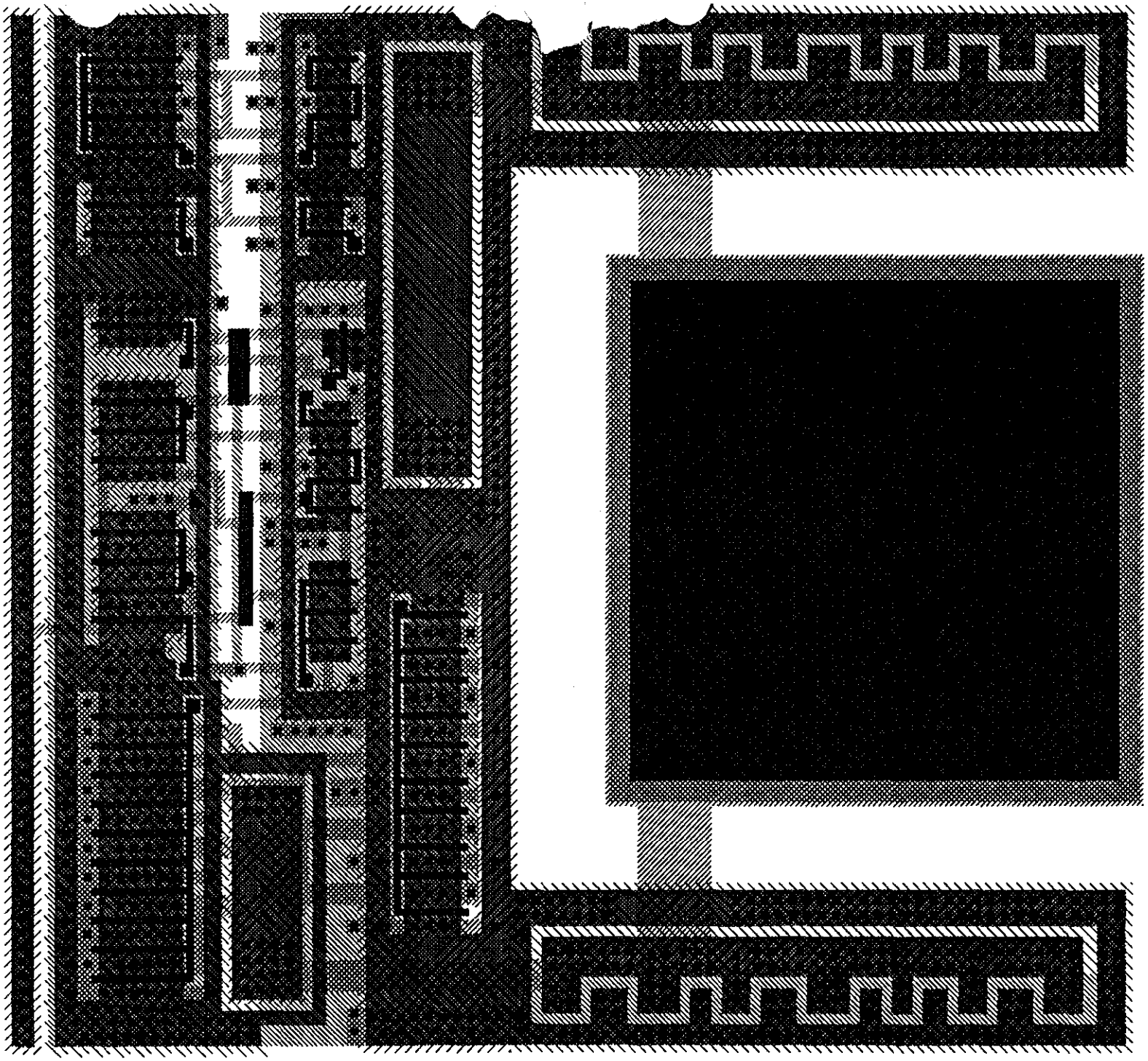


Figure 10 The layout of an input pad.