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SOLENOIDAL DETECTOR NOTES

L1 MUON TRIGGER ELECTRONICS

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CMOS field programmable gate array (FPGA) is gaining popularity very rapidly. The key features of FPGA are its flexibility, large size, extremely fast speed and low power consumption. These features make it very attractive for trigger applications in high energy experiments. Compared to custom ASIC's, FPGA does not need expensive and time consuming chip design process and good design software support is available. In many cases, FPGA can be more cost effective than the custom ASIC.

We have implemented several trigger circuits into XILINX FPGA chips. The design of these circuits are based on a completely digital trigger scheme proposed by J. Oliver and T. Zhao during the last Berkeley meeting. The first circuit discussed in this node is a digital vresion of the CDF muon trigger circuit. The second one is very similar to that proposed by J. Chapman. A working prototype which runs up to 60 MHz was demonstrated in Madison trigger meeting last September. We have also built a CAMAC trigger module which can be operated at 90 MHz.

1 Basic Requirements for Trigger Electronics

1.1 Time Required for L1 Trigger Generation

Due to the long signal collection time inside drift cells, the time required to generate L1 muon trigger is the determine factor for the total pipe line length of the entire SDC detector readout electronics. Our group have proposed a drift chamber system based on cylindrical drift cells with 3.7 cm maximum drift distance. Without field shaping, the maximum drift time can be limited to within 1 μs using P10 or some other gas mixtures. With proper field shaping, the maximum drift time is 780 ns for conventional gas mixtures and is less than 500 ns for some fast gas mixtures containing small amount of CF_4. It is also extremely important to minimize the processing time of the L1 electronics.

1.2 ΔT Coverage

The basic trigger element of the L1 muon trigger system is a pair of drift tubes which are separated by about 16cm/sinθ in our design. The maximum time difference which the trigger circuit has to cover occurs at the lowest P_t and at the smallest θ in the central detector. At $\theta = 40^o$ and for 10 GeV/c P_t muon, the time difference

which the trigger circuit has to cover is $\Delta T = T_1 - T_2 \sim 500ns$ or about 30 clock cycles for a digital trigger running at 60 MHz.

1.3 Time Resolution

The fastest XILINX FPGA is rated at 125 MHz which limits the trigger time resolution to 8 ns, corresponding to 0.4 mm in terms of drift distance using conventional gas. In terms of angular measurements, the maximum error given by trigger electronics is 2.5 mr. For comparison, the angular smearing due to multiple scattering in the calorimeter and iron toroid is $\sigma_\theta \sim 4$ mr for a 40 GeV/c muon. The limitation of the trigger angular resolution due to the 5 cm interaction region size is $\sigma_\theta = 6$ mr at r = 8.5 meters. Therefore, a digital trigger system operating at 60 MHz is already sufficient. Results of computer simulation about this issue is summarized in another note (PHY-154).

1.4 Programmability

The trigger logic should be field programmable in order to accommodate unexpected problems and changes in trigger strategies during the experiment's many year life time.

P_t thresold of our proposed chamber system has a $1/\sin\theta$ dependence. For a fixed P_t threshold, the Δt cut of the trigger electronics has to be different at different θ. It is not necessary to design a circuit such that this θ correction can be made continuously. The entire barrel muon detector can be divided into three regions, 90°-60°, 60°-45° and 45°-35°. Trigger circuits have to be programmed differently in different regions.

2 Circuit Designs

2.1 Circuit 1

Fig. 1 shows the block diagram of a simple trigger circuit. The major component of this circuit is a 24 bit shift register. The clock of this shift register is started by the OR of the two wire hits and stopped by the AND of the two wire hits. The location of the first arrival hit in the shift register is directly related to the P_t of the muon track. Output switches selects the desired P_t thresholds and the trigger output is stored in registers for further processing. A complete logic diagram is shown in fig. 2.

This circuit is sensitive only to the first arrival signals in each drift tube. Because of this, a high P_t muon can be lost if soft electrons accompanying it create a hit earlier than the real muon hit. Also, Low P_t muons can generate false triggers due to soft electrons. In a minimum trigger system which consists only 2 layers of chambers,

these problems would be very serious. However, in a trigger system using all 8 θ layers of BW2 and BW3, these two problems are minimized due to the redundancy of the system. We expect this simple circuit to give satisfactory performance.

2.2 Circuit 2

The circuit shown in fig. 3 is very similar to the circuit suggested by Jay Chapman. In this case, signals propagate to opposite directions in two shift registers. Properly arranged coincidence gates among the shift register outputs determine the P_t of the muon track. This circuit has multihit capability. In the example given in fig. 3, there are four different trigger thresholds available for further processing.

3 Implemeting into Xilinx FPGA

We have implemented the two circuits discussed above into a 3020 chip mounted on a Xilinx prototype development box. The Xilinx 3020 chip we used is rated at 100 MHz. But the development system box limits our clock speed. As a general testing device, it has switches and headers, long printed circuit traces and wire connections. Even with these bad features, we are still able to operate the system at 60 MHz.

In order to evaluation the performance of our proposed trigger system, a CAMAC module which contains two 3020 chips has been constructed. The logic diagram of this CAMAC module is shown in fig. 4. Discriminated outputs from a cosmic ray test station which consists four drift tubes are fed into this CAMAC module and also into a LeCroy 2277 multihits TDC module. This system simulates our proposed L1 muon trigger system. It is now operational and the evaluation is in progress.

The circuits in the CAMAC module can be operated at maximum speed of 90 MHz. We expect that the operating speed can still be improved by using a better disigned printed circuit board.

4 Trigger System Design

In the barrel region, we will need roughly 12,000 channels of trigger circuits. It requires 12,000 chips Xilinx 3020 chip. The total number of chips will be reduced if we use bigger chips. These chips will be divided into boards and crates according to the the geometric arrangement of drift chamber modules. The obvious location for the L1 trigger crates is the space in between BW2 and BW3.

As proposed by the Michigan group, it is necessary to use all 8 θ layers in BW2 and BW3 in order to minimize the fake trigger rate due to low P_t muons. The basic trigger requirement is $(T_1 \times T_2) \cdot (T_3 \times T_4)$. T_1 is the trigger signal generated by a

pair of tubes in chamber layer 1 and 3 of BW1. T_2 is the or of two neighboring cells from layer 2 and 4 of BW2. T_3 is from layer 1 and 3 in BW3 and T_4 is from layer 2 and 4 in BW3.

We have to interconnect the trigger signals between BW2 and BW3. A 10 GeV/c P_t muon be deflected from the projective line by about $\pm$ 30 cm. Therefore, both T_3 and T_4 have to be the OR's of at least eight pairs of drift tubes. It requires rather complicated Interconnections in order to form a complete trigger tower.

5 Future Plans

We expect to complete the evaluation of our CAMAC trigger prototype based on 3000 serial chips in the next few months. With the new Xilinx 4000 serial devices, we expect that 120 MHz clock speed can be achieved. The availability of chips are still limited and the design software are evolving. We plan to upgrade our system to the Xilinx 4000 in 1992.

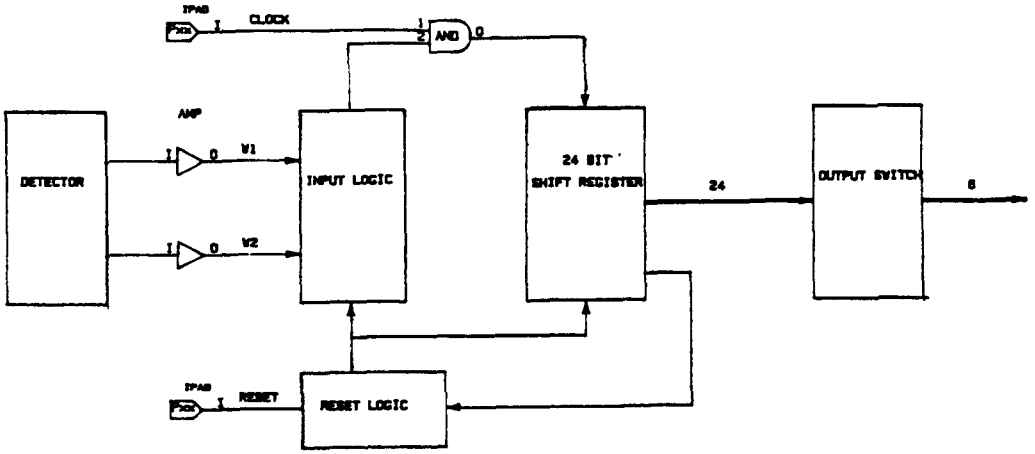

Fig. 1. Block diagram of trigger circuits

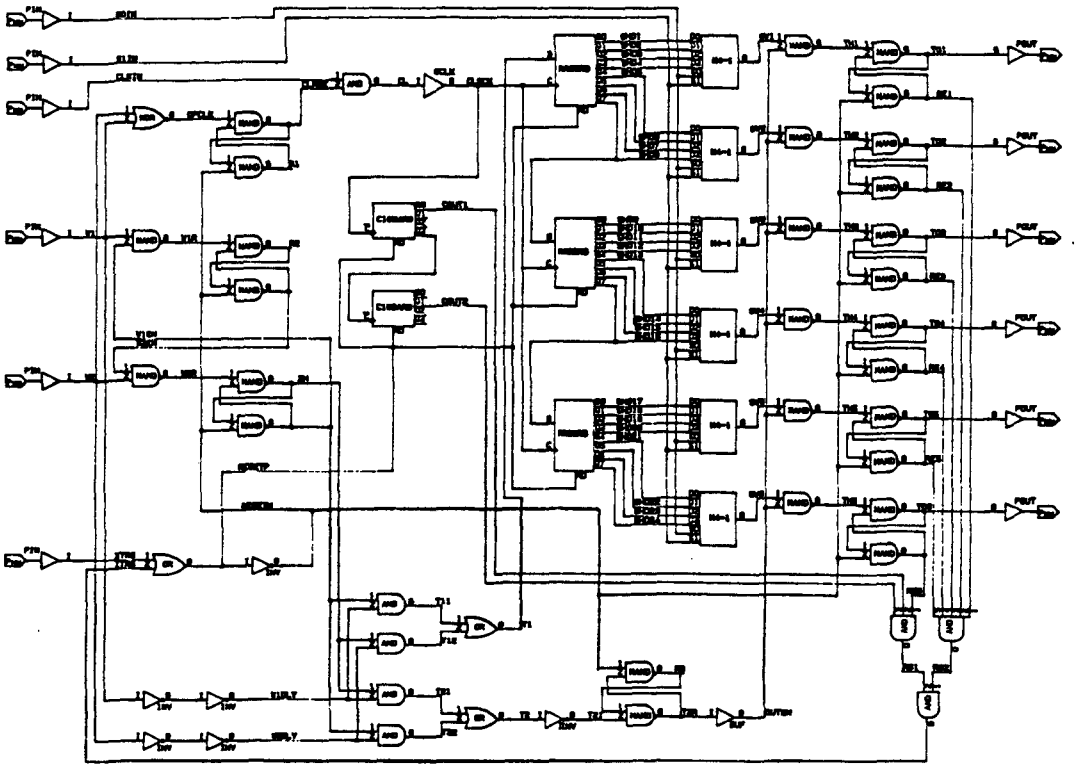

Fig. 2. Logic diagram of circuit 1

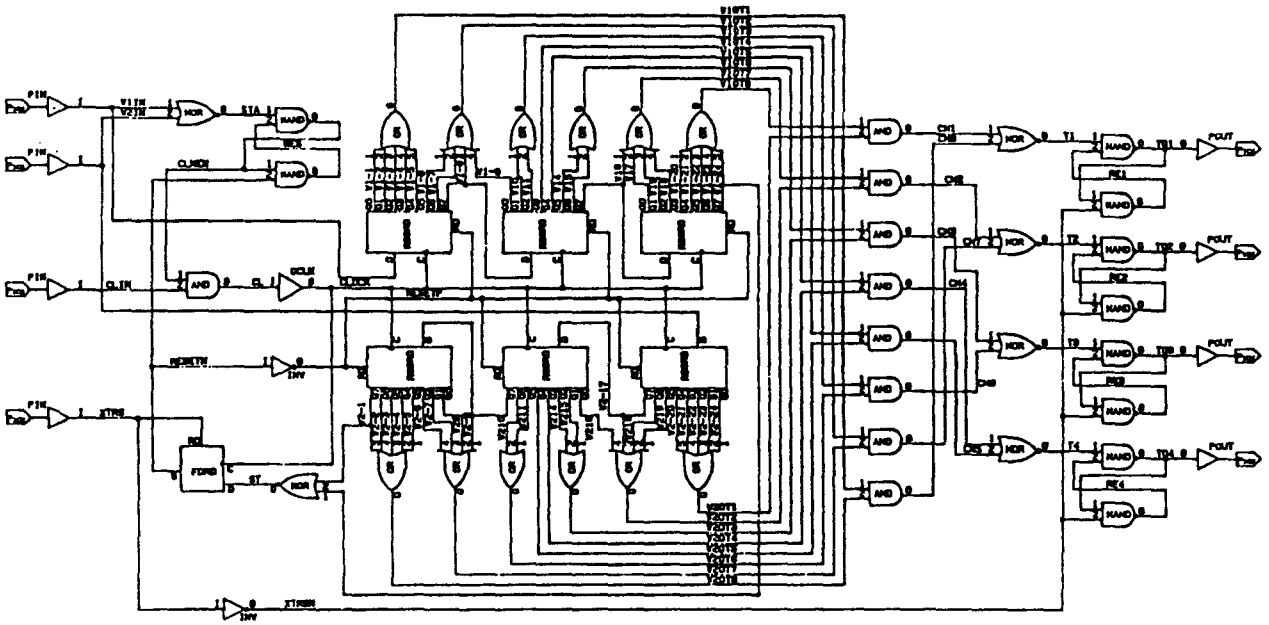

Fig. 3. Logic diagram of circuit 2

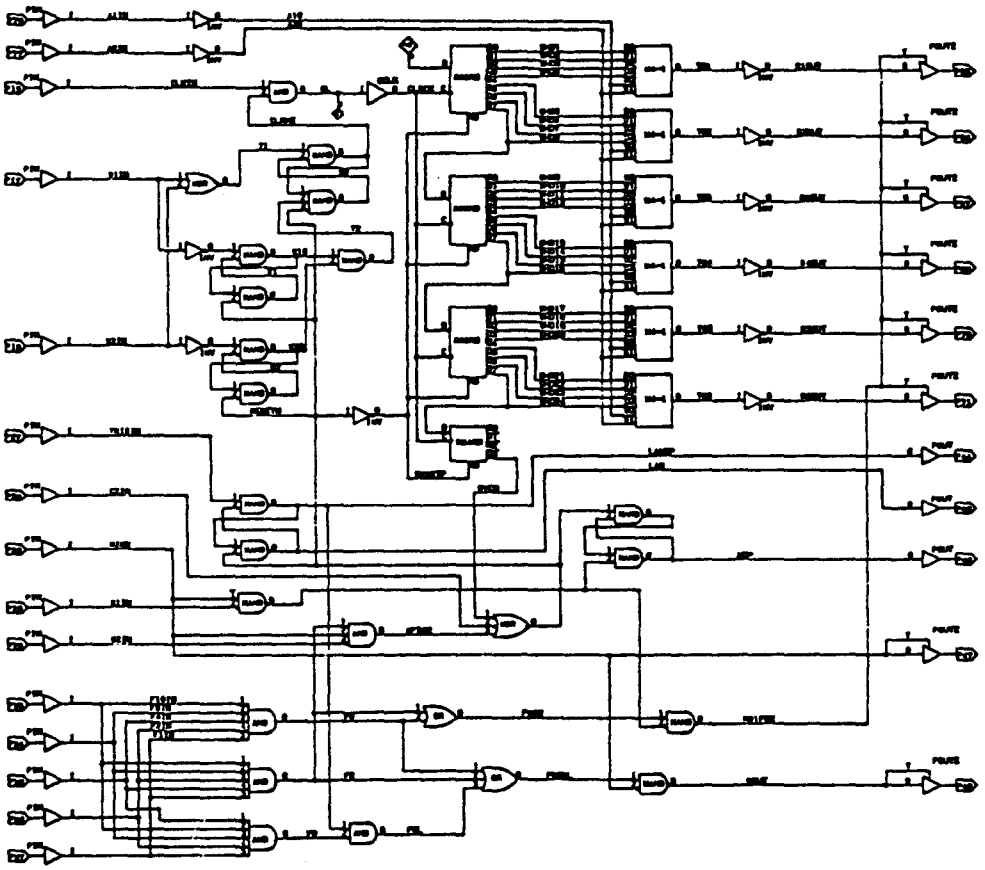

Fig. 4. Logic diagram of the CAMAC trigger module