SDC-92-175

SDC
SOLENOIDAL DETECTOR NOTES

CERENKOV SYSTEM COST

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University of Colorado

December 16, 1991

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1 Introduction

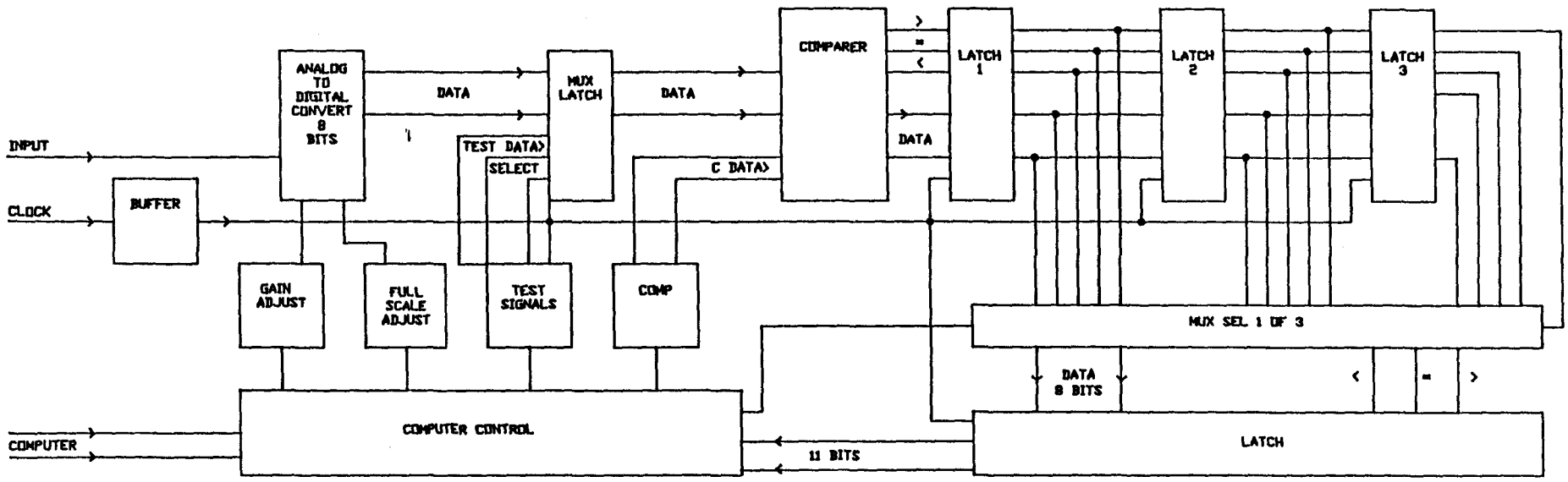
This document describes the Work Breakdown Structure (WBS) cost estimate and circuit description for the SDC Cerenkov Electronic System (WBS 5.3). Pricing of the SDC Cerenkov electronic system is based on a particular implementation and does not include system and fiber optic cabling to the computer system. A block diagram and design concept is discussed in Section 2. Each card is connected with optical fibers to the trigger system. The host computer system will command the Cerenkov electronics to perform Built In Test (BIT), threshold settings, and calibration. There are no manual adjustments.

2 Electronic Description

Figure 1 is the Block diagram of a single electronic channel. The input signal is received by a buffer amplifier and then terminated into the characteristic impedance of the transmission line. The output of the buffer amplifier goes to the Analog to Digital Converter. The eight bit Analog to Digital Converter makes its conversion from a command signal coming from the sensor system. A discriminator can be substituted for the eight bit analog to digital converter thus reducing resolution of the experiment. This change would considerably reduce the hardware cost of the system. This data is then clocked to a storage register. The output of the storage register goes to a digital comparator. The other input to the digital comparator is a level controlled by the host computer. This level is latched and can be changed dynamically by the host computer. The comparator information and the data information for each channel is then stored in the electronics for further processing. The 25 channels are then multiplexed and sent to a fiber optic channel with the appropriate overhead and error detection coding expanded on.

Each channel has its own digital comparator setting and computer controlled analog to digital calibration. In conjunction with the host computer Built In Test can be performed indicating the defective channel and parts that have to be replaced.

CERENKOV SINGLE CHANNEL ELECTRONICS



3. Cost Estimate

3.1 Methodology

The cost for the Cerenkov Electronic System was calculated by determining the number of boards needed to construct the system. The electronics was partitioned to equal the sensor partition taking advantage of testing and building a complete integrated section. The Cerenkov Counter construction has two identical sides with each side having eight wedges and each wedge having 25 Cerenkov cells. Thus each Cerenkov electronic board contains 25 complete channels. Thus costing is based on 16 boards plus two spares with each board having 25 channels. The cost of each board was calculated with the following components: Analog to Digital Converter electronics, controller electronics, optical fiber electronics, an ASIC, glue logic, and printed circuit board. Each electronics board was costed with contingency at 7.50 k$ with .360 k$ for the printed circuit board, 7.02 K$ for parts and .120 k$ for assembly and test. This cost is based on vendor quotes, past experience and estimates from the SDC trigger system.

The design of Cerenkov Electronics is considered to be of moderate complexity. The design is estimated to take 2 man-year(MY) of engineering time. In addition, each MY of engineering time was assumed to also use a MY of technician time as well expenses for travel and supplies and computing (i.E. CAD).

3.2 Prototype

A prototype system consisting of two cards using FPLGA instead of ASICS will be designed first. This design will be proof of concept. The FPLGA design will then be converted to ASICS. The advantage of this technique is faster development for the FPLGA and less cost for engineering changes. The disadvantage is that the FPLGA lower gate density per package resulting in more area and higher cost per channel. This will result in fewer channels per board than the completed set of 25. Since each set is identical there is no real need to have a complete set of 25 channels.

3.3 Contingency

The cost listed in the budget estimate are the base costs of producing each item correctly the first time. There are also explicit costs listed for prototyping where required. The cost contingency is the cost required beyond the base cost to ensure successful completion. The calculation of contingency has been the base cost to ensure successful completion. The calculation of contingency has been done for each WBS item. Each item has been

assigned a technical risk factor, a cost risk factor and a schedule risk factor. Table 1 is the criteria used in estimating the **RISK FACTORS**. Table 2 is the **WEIGHING FACTORS** for each type of risk. Table 3 represents the calculation of each risk factor. Each risk was multiplied by its weighing factor and the total of these products was used as the total contingency for each item.
These contingency calculations are for each WBS and is summarized in Table 3 **CONTINGENCY CALCULATION CHART**.

TABLE 1– TECHNICAL, COST & SCHEDULE RISK FACTORS

RISK FACTOR	TECHNICAL	COST	SCHEDULE
1	EXISTING DESIGN AND OFF THE SHELF H/W	OFF THE SHELF OR CATALOG ITEM	
2	MINOR MODIFICATION TO EXISTING DESIGN	VENDOR QUOTE FROM ESTABLISHED DRAWINGS	NO SCHEDULE IMPACT TO ANY OTHER ITEM
3	EXTENSIVE MODIFICATION TO AN EXISTING DESIGN	VENDOR QUOTE WITH SOME DESIGN SKETCHES	
4	NEW DESIGN, NOTHING EXOTIC	IN-HOUSE ESTIMATE BASED ON PREVIOUS SIMILAR EXPERIENCE	DELAYS COMPLETION ON NONCRITICAL PATH SUBSYSTEM
6	NEW DESIGN, DIFFERENT FROM ESTABLISHED DESIGNS EXISTING TECHNOLOGY	IN-HOUSE ESTIMATE FOR ITEM WITH MINIMAL EXPERIENCE BUT RELATED TO EXISTING CAPABILITY	
8	NEW DESIGN, REQUIRES SOME R&D BUT DOES NOT ADVANCE THE STATE-OF-THE ART	IN-HOUSE ESTIMATE FOR ITEM WITH MINIMAL EXPERIENCE AND MINIMAL IN-HOUSE CAPABILITY	DELAYS COMPLETION OF CRITICAL PATH SUBSYSTEM ITEM
10	NEW DESIGN, DEVELOPMENT OF NEW TECHNOLOGY WHICH ADVANCE THE STATE-OF-THE ART	TOP-DOWN ESTIMATE FORM ANALOGOUS PROGRAMS	
12	NEW DESIGN, WAY BEYOND THE CURRENT STATE-OF-THE ART	ENGINEERING JUDGMENT	

TABLE 2 - TECHNICAL, COST & SCHEDULE WEIGHTING FACTORS

WEIGHTING FACTOR	RISK
TECHNICAL WEIGHTS	
2%	DESIGN OR MANUFACTURING
4%	DESIGN AND MANUFACTURING
COST WEIGHTS	
1%	MATERIAL COST OR LABOR RATE
2%	MATERIAL COST AND LABOR RATE
SCHEDULE WEIGHT	
1%	(SAME FOR ALL)

CONTINGENCY CALCULATION CHART

WBS	ELEMENT DESCRIPTION	TECH RISK	COST RISK	SCHEDULE RISK	TECH WEIGHT	COST WEIGHT	SCHEDULE WEIGHT	COMPOSITE CONTINGENCY %
5.1.4.3.	Cerenkov Counter Electronics							
5.1.4.3.1	A to D Evaluation	1	1	4	2	2	1	8
5.1.4.3.2	Design FPLGA	4	1	4	4	1	1	21
5.1.4.3.3	Prototype Design PC Card	4	2	4	4	2	1	24
5.1.4.3.4	Design Computer Interface	4	3	4	2	2	1	18
5.1.4.3.6	Design Power Distribution	4	3	4	2	1	1	15
5.1.4.3.7	Design Interconnect for Prototype	4	2	4	2	1	1	14
5.1.4.3.5	Build and Test Prototype	4	4	4	4	2	1	28
5.1.4.3.8	Build and Test Prototype System	4	4	4	4	2	1	28
5.1.4.3.9	Finalize Design	1	1	4	2	1	1	7
5.1.4.3.10	Design ASICS	4	4	4	4	2	1	28
5.1.4.3.11	Finalize Printed Circuit Design	4	4	4	2	2	1	20
5.1.4.3.12	Finalize Power Design	2	4	4	4	1	1	16
5.1.4.3.13	Buy Build and Test Power Electronics	2	4	4	4	2	1	20
5.1.4.3.14	Finalize Electronic Interconnections	2	4	4	2	1	1	12
5.1.4.3.15	Buy Build and Test Final Version of Electronics	2	4	4	4	2	1	20
5.1.4.3.16	Photo Tube Base	1	1	2	1	2	1	5
5.1.4.3.17	Buy Interconnect Power and Signal Cables	1	1	2	1	2	1	5
5.1.4.3.18	Buy Interconnecting Connectors	1	1	2	2	2	1	6
5.1.4.3.19	Buy Power Supply for sensors	1	1	2	2	2	1	6

4. RESERVED FOR FUTURE USE

5. WBS Dictionary

5.1.4.3	This is the WBS for the level 1 trigger for the Cerenkov Counter Electronics.
5.1.4.3.1	Test and evaluation of analog to digital converter.
5.1.4.3.2	Design of digital logic and FPLGA.
5.1.4.3.3	Design of the prototype type printed circuit card.
5.1.4.3.4	Design of the computer interface for the Cerenkov Counter Electronic.
5.1.4.3.5	Design and test power distribution for the Cerenkov Electronics.
5.1.4.3.6	Design interconnection for the Cerenkov Counter Electronics and computer interface for prototype system.
5.1.4.3.7	Build and test the prototype type printed circuit card assemblies.
5.1.4.3.8	Build and test the prototype type System.
5.1.4.3.9	Finalize design.
5.1.4.3.10	Design ASICS from FPLGA
5.1.4.3.11	Finalize printed circuit card and make any changes needed.
5.1.4.3.12	Finalize power distribution for the Cerenkov Electronics.
5.1.4.3.13	Buy build and test final version of Cerenkov Counter Electronics power distribution.
5.1.4.3.14	Design finalize Cerenkov Counter Electronics interconnections.
5.1.4.3.15	Buy and build and test final version of Cerenkov Counter Electronics cards.
5.1.4.3.16	Photo tube Base

5.1.4.3.17 Evaluate and buy high frequency cables interconnecting to the sensors with the Cerenkov Counter Electronics

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5.1.4.3.18 Evaluate and buy high voltage and coaxial connectors interconnecting the sensors with the Cerenkov Counter Electronics.

5.1.4.3.19 Evaluate and buy the power supplies for the sensors

6. Card Usage in the Cerenkov System.

6.1 Card Summary

There are 16 identical cards used in the system.
Each card consist of 25 channels

6. Cost Breakdown

Appendix A give the detailed cost breakdown for the SDC Cerenkov System. The WBS numbers follow the description given in the WBS section above. The total cost of the electronics is $320,700 plus $69,204 contingency, giving a total project cost of total project cost, 389,904. The total cost of the cerenkov system including the electronics is $598,752 plus 83,377 contingency, giving a total project cost of total project cost, $682,129.

The cost can be reduce by sacrificing resolution. A discriminator can be substituted for the Analog to Digital converter. This would give one bit resolution with a variable threshold. If this option is chosen it is highly recommended that the design and prototyping is still the full A to D converter and the handles to upgrade the production boards to a full A to D system be kept. If the approach is taken the total project cost can be reduced by $36,450

APPENDIX A

SDC CERENKOV SYSTEM WBS 5.1.4.3

WBS STANDARD FORMAT SHEET 1 0F 3

	A	B	C	D	E	F	G	H	I	J	K	L
1	WBS NUMBE	WBS OR ACTIVITY DESCRIPTION	UNIT	QTY	COST EA(K$)	EN M/D	ENM M/D	EA M/D	EAM M/D	DR M/D	DRM /MD	AD M/D
3	5.1.4.3.	Cerenkov Counter Electronics										
4	5.1.4.3.1	A to D Evaluation		1	5.08							
5	5.1.4.3.2	Design FPLGA		1	12.10	67						
6	5.1.4.3.3	Prototype Design PC Card		1	3.10	10						
7	5.1.4.3.4	Design Computer Interface		1	0.47							
8	5.1.4.3.5	Design Power Distribution		1	0.23							
9	5.1.4.3.6	Design Interconnect for Prototype		1	0.23							
10	5.1.4.3.7	Build and Test Prototype		2	11.14							
11	5.1.4.3.8	Build and Test Prototype System		1	0.26	2						
12	5.1.4.3.9	Finalize Design										
13	5.1.4.3.10	Design ASICS				516						
14	5.1.4.3.11	Finalize Printed Circuit Design				13						
15	5.1.4.3.12	Finalize Power Design										
16	5.1.4.3.13	Buy Build and Test Power Electronics		1	2.40							
17	5.1.4.3.14	Finalize Electronic Interconnections										
18	5.1.4.3.15	Buy Build and Test Final Version of Electronics		18	7.51							
19	5.1.4.3.16	Photo Tube Base		420	0.079	17						
20	5.1.4.3.17	Buy Interconnect Power and Signal Cables		70000	0.0002							
21	5.1.4.3.18	Buy Interconnecting Connectors		1600	0.006							
22	5.1.4.3.19	Buy Power Supply for sensors		117	1.15							
23												
24												
25												
26												
27	TOTAL											
28												
29												
30												
31												
32												
33												
34												
35												
36												
37												
38												

WBS STANDARD FORMAT SHEET 2 0F 3

M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
ADM M/D	TE M/D	TEM M/D	LA M/D	LAM M/D	$EXP(K$)	$MINOR(K$)	$MAJOR(K$)	WBS M/D	WBS MAT(K$)	WBSBASE(K$)	CONTING %	CONTING(K$)	WBS TOTAL(K$)
						5.08		X	X	X	X	X	5.08
					2	30.25		X	X	X	X	X	32.25
	45					11.78		X	X	X	X	X	11.78
						0.47		X	X	X	X	X	0.47
						0.23		X	X	X	X	X	0.23
						0.23		X	X	X	X	X	0.23
						22.27		X	X	X	X	X	22.27
	10					0.26		X	X	X	X	X	2.18
					15			X	X	X	X	X	15.00
					10		140.80	X	X	X	X	X	150.80
	62					12.00		X	X	X	X	X	12.00
								X	X	X	X	X	
					1	2.40		X	X	X	X	X	2.40
								X	X	X	X	X	
							135.12	X	X	X	X	X	135.12
	81	821.3333			20		116.03	X	X	X	X	X	136.03
						11.03		X	X	X	X	X	11.03
						10.18		X	X	X	X	X	10.18
							135.10	X	X	X	X	X	135.10
													682.13

WBS STANDARD FORMAT SHEET 3 0F 3

CODE	DESCRIPTION	MAN YEAR COST IN $	WORKING DAYS IN MAN YEAR	RATE IN $ PER DAY
EN M/D	ENGINEERING MAN DAYS	60000	220	273
ENM MD	ENGINEERING MANUFACTURING MAN DAYS			
EA M/D	ENGINEERING ASSOCIATE MAN DAYS			
EAM M/D	ENGINEERING ASSOCIATE MANUFACTURING MAN DAYS			
DR M/D	DRAFTSMAN MAN DAYS			
DRM M/D	DRAFTSMAN MANUFACTURING MAN DAYS			
AD M/D	ADMINISTRATION MAN DAYS			
ADM M/D	ADMINISTRATION MANUFACTURING MAN DAYS			
TE M/D	TECHNICIAN MAN DAYS	30000	220	136
TEM M/D	TECHNICIAN MANUFACTURING MAN DAYS	18000	220	82
LA M/D	LABORER MAN DAYS			
LAM M/D	LABORER MANUFACTURING MAN DAYS			
$EXP(K$)	EX: TRAVEL, PUBLISHING, ETC			
$MINOR(K$)	MINOR PROCUREMENT	NOT ADDITIONAL COST		
$MAJOR(K$)	MAJOR PROCUREMENT	NOT ADDITIONAL COST		

WBS COSTING

		WITHOUT CONTINGENCY						WITH CONTINGENCY					
WBS	ELEMENT DESCRIPTION	MATERIAL	MISC	LABOR	ENGINEERING	EXPENS	SUM	MATERIAL	MISC	LABOR	ENGINEERING	EXPENS	SUM
5.1.4.3.	Cerenkov Counter Electronics												
5.1.4.3.1	A to D Evaluation		$4,700				$4,700		$5,076				$5,076
5.1.4.3.2	Design FPLGA		$10,000		$15,000	$2,000	$27,000		$12,100		$18,150	$2,000	$32,250
5.1.4.3.3	Prototype Design PC Card		$2,500		$7,000		$9,500		$3,100		$8,680		$11,780
5.1.4.3.4	Design Computer Interface		$400				$400		$472				$472
5.1.4.3.5	Design Power Distribution		$200				$200		$230				$230
5.1.4.3.6	Design Interconnect for Prototype		$200				$200		$228				$228
5.1.4.3.7	Build and Test Prototype	$17,400					$17,400	$22,272					$22,272
5.1.4.3.8	Build and Test Prototype System		$200		$1,500		$1,700		$256		$1,920		$2,176
5.1.4.3.9	Finalize Design					$15,000	$15,000					$15,000	$15,000
5.1.4.3.10	Design ASICS				$110,000	$10,000	$120,000				$140,800	$10,000	$150,800
5.1.4.3.11	Finalize Printed Circuit Design				$10,000		$10,000				$12,000		$12,000
5.1.4.3.12	Finalize Power Design												
5.1.4.3.13	Buy Build and Test Power Electronics		$2,000				$2,000		$2,400				$2,400
5.1.4.3.14	Finalize Electronic Interconnections												
5.1.4.3.15	Buy Build and Test Final Version of Electronics	$111,600	$1,000				$112,600	$133,920	$1,200				$135,120
5.1.4.3.16	Photo Tube Base	$31,500		$64,000	$15,000	$20,000	$130,500	$33,075		$67,200	$15,750	$20,000	$136,025
5.1.4.3.17	Buy Interconnect Power and Signal Cables	$10,500					$10,500	$11,025					$11,025
5.1.4.3.18	Buy Interconnecting Connectors	$9,600					$9,600	$10,176					$10,176
5.1.4.3.19	Buy Power Supply for sensors	$127,452					$127,452	$135,099					$135,099
	TOTAL OF EACH ITEM	$308,052	$21,200		$158,500	$47,000	$598,752	$345,567	$25,062		$197,300	$47,000	$682,129

ECTRONIC COST FOR CERENKOV SYSTEM

DESCRIPTION	PART NUMBER	COST/UNI	UNIT	TOTAL COST	
A TO D CONVERTER 8 BITS	AD9012AP	81	25	2025	
WIDE BANDWIDTH BUFFER AMPLIFIER	AD9611B	90	25	2258	
COMPARATOR	AD96685B	6	25	150	
+REF FOR A-D	AD741CH	1	25	28	
-REF FOR A-D	AD741	1	25	28	
REF VOLTAGE	AD1403N	2	25	50	
REF VOLTAGE		2	25	50	
REF VOLTAGE		2	25	50	
DIGITAL OFF SET ADJUST		2	50	100	
D - A CONVERTER FOR CAL AND TEST		40	1	40	
BUFFER AMP	AD741	1	5	6	
ECL T0 CMOS TRANSLATOR		4	3	12	
BUFFER CHIPS		10	2	20	
GATE ARRAY		125	1	125	ESTIMATE FROM PASSED EXPERIENCE
CONTROLLER CHIP		40	1	40	
GLUE LOGIC		4	25	100	
FIBER OPTIC LINKS		300	1	300	REFERENCE QUOTE FROM TRACKING SYSTEM
RESISTORS		0.1	1050	105	
CAPACITORS		0.2	250	50	
DE-COUPLING CAPS LIGHT		1	75	38	
DECOUPLING CAPS HEAVY		1	3	3	
POWER CONNECTOR		12	1	12	
CONTROL CONNECTOR		12	1	12	
CONNECTORS SMA		8	25	200	
PC BOARD		300	1	300	
CARD ASSY		75	1	75	
TEST		25	1	25	
TOTAL COST				6200	
TOTAL COST PER CHANNEL					248

TOTAL MATERIAL 16 CARDS (EARCH CARD 25 CHANNELS) PLUS TWO SPARE CARDS	111591
TWO PROTOTYPE	17400
TOTAL MATERIAL 16 CHANNELS PLUS SPARES AND PROTOTYPE	128991

CERENKOV COST OF INTERCONNECT CABLE AND POWER SUPPLIES

DESCRIPTION	UNIT COST	QUANTITY	COST
PHOTOTUBE BASE	75	400	30000
PHOTOTUBE BASE (SPARE	75	20	1500
SUB TOTAL PHOTOTUBE BASE			31500
CABLE HIGH VOLTAGE PER FT	0.16	35000	5600
RG58 COAXIAL CABLE PER FT	0.14	35000	4900
SUB TOTAL CABLE			10500
CONNECTORS SHV	10	800	8000
CONNECTORS BNC	2	800	1600
SUB TOTAL CONNECTOR			9600
LE CROY HV4032A/M/HV (32 CH/UNIT)	4628	13	60164
4 CHANNEL HV4032IN (3.3 KV MAX)	647	104	67288
SUB TOTAL HIGH VOLTAGE POWER SUPPLY			127452