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SOLENOIDAL DETECTOR NOTES

SILICON TRACKING
CONCEPTUAL DESIGN REPORT

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Conceptual Design Report – 1992

I. Introduction and Goals

This paper is the conceptual design report for the SDC silicon tracking detector. Together with outer tracking superlayers within the solenoidal field volume and chambers at large radius outside the calorimeter for tracking muons, it forms the SDC charged particle tracking system. The silicon array, presented below, will provide charged particle detection at radii smaller than 50 cm, while the outer tracking superlayers cover the region beyond this, out to a radius of 170 cm. The outer tracker, like the silicon, has layers configured in a barrel and forward planar geometry.

The goals for the tracking system of the SDC are summarized concisely and quantitatively in Table 1. For the magnet dimensions and field strength of the SDC, it would be extremely difficult to meet the SDC goals for momentum resolution at large or small rapidities, for vertexing, or for rapidity acceptance using detection elements restricted to radii > 50 cm. Thus the silicon forms a critical element in the tracking system.

In addition, it will play a critical role in pattern recognition and provide high luminosity capability because of the very low occupancy of each detector element. These will considerably enhance the SDC capabilities for surprise discoveries.

A quarter section of the silicon system is shown in Fig. 1. The subassembly dimensions are given in Table 2. Detailed justification for this design will be given in the next section. The detector has cylindrical layers covering the region at small rapidity, and planar disk layers covering the large rapidity region. The silicon area is about 17 m^2 and number of electronics channels about 6×10^6. An option for the detector would be to have the layers inside of 15 cm (first two barrel layers) made of pixel detectors. The mechanical design effort for pixels is focussed on ladder structures and cooling schemes which will allow such an option without necessitating mechanical system changes. The mechanical design allows for replacement of the innermost layers in the case of upgrades or after performance degradation after several megarads of radiation dosage.

Table 1. Summary of Requirements for Tracking System

1) Acceptance and $P_\perp$ resolution:
   (a) $|\eta|$ coverage at least out to $|\eta| = 2.5$ ($H^0 \to 4$ charged lepton geometrical efficiency $\gtrsim 60\%$ for $m_H \geq 200$ GeV/c^2).
   (b) Reconstructed (as opposed to parametric) vertex constrained momentum resolution for isolated charged tracks of $\sigma_{P_\perp}/p_\perp^2 < 20\%$ TeV/$^{-1}$ for $|\eta| \leq 1.8$, allowed to rise to $\sigma_{P_\perp}/p_\perp^2 \to 100\%$ TeV/$^{-1}$ as $|\eta| \to 2.5$.
2) Reconstruction efficiency within this acceptance $\geq 97\%$ for isolated tracks having $P_\perp \geq 10$ GeV, with ≤ 0.1 false tracks of $P_\perp \geq 10$ per trigger. (Efficiency greater than 90% for detecting all four leptons from $H^0 \to 4$ charged leptons, exclusive of lepton identification— E/p and η, ϕ matching—and trigger cuts.) This requirement is specified for design luminosity, but with occupancy assumed twice that calculated by Monte Carlo for $pp \to X$.
3) Reconstruction efficiency for same as in (2) $\geq 90\%$ at 10 $\times$ design luminosity.
4) b tagging efficiency for top studies with 125 GeV$^2 \leq M_{\text{top}} \leq 250$ GeV^2:
   (a) Reconstruction efficiency $\geq 80\%$ for tracks of $P_\perp > 5$, with less than 10% fakes, within jets of $P_\perp$ up to 100 for b tagging using leptons.
   (b) b tagging efficiency $\geq 25\%$ with $\geq 90\%$ purity using detached vertices. Implies impact parameter resolution ≤ 20 μm for stiff tracks, ≤ 100 μm for $P_\perp = 1$, and $\geq 85\%$ efficiency for finding tracks with $P_\perp > 1$ within jets of $P_\perp$ up to 100.
5) Material $\lesssim 15\% X_0$, $\lesssim 7\% X_0$ inside 50 cm (average over $|\eta| \leq 2.5$). For efficiency of electron ID (E/p cut).
6) Position resolution at the calorimeter shower maximum detector of ≤ 5 mm in $r\phi$ (where bremsstrahlung smearing occurs) and ≤ 2.5 mm in z.
7) Alignment relative to the muon system of 100 μm in $r\phi$ and 2 mm in z.
8) Jet charged multiplicity measurement within 15% for jets up to $P_\perp = 500$ (to distinguish isolated W's, and to study fragmentation for QCD studies and background modelling).
9) Resolution for measurement of the z component of the vertex of 2 mm, to separate pileup interactions.
10) First level trigger with momentum resolution $\sigma_{P_\perp}/p_\perp^2 \sim 10$ TeV/$^{-1}$—implies a 10% error for a 10 GeV lepton.
11) First level trigger efficiency $\geq 96\%$ per track, with ≤ 0.05 false triggers per calorimeter trigger ϕ bin per crossing, over the range $|\eta| \leq 2.5$.
12) Second-level trigger with momentum resolution $\sigma_{P_\perp}/p_\perp^2 = 5$ TeV/$^{-1}$. Gives a 20% error for a 40 GeV lepton for triggering on $Z \to \ell^+\ell^-$, $W \to \ell\nu$.
13) Discovery potential—hard to quantify. In general want maximum capabilities from detector. Based on history, highest priority (other than isolated lepton of Higgs case above) would be reconstruction and impact parameter measurement of leptons within jets up to the largest jet $P_\perp$ possible (at least ≥ 500 GeV). Desired reconstruction efficiency $\geq 50\%$.
14) Survivability at standard $\mathcal{L}$ for ≥ 10 years.
15) Allows a natural path for upgrading to a system with survivability of ≥ 10 years at 10$\times$ standard $\mathcal{L}$ with emphasis (*e.g.* momentum resolution, pattern recognition, isolated track efficiency) to be decided based on what is learned during initial running.

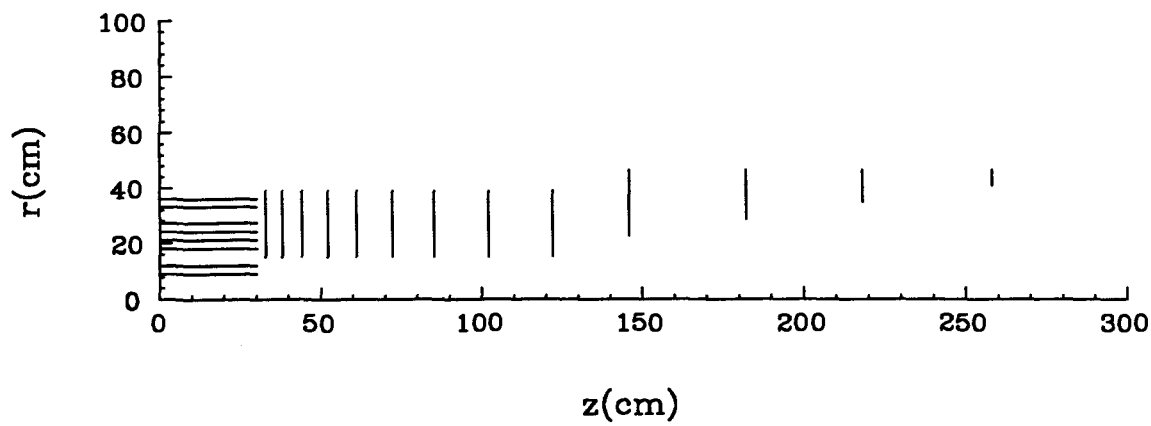


Fig. 1. Silicon tracker design.

Table 2. Dimensions for tracker

Barrel	r	z		
(1)	9 cm	30 cm		
(2)	12 cm	30 cm		
(3)	18 cm	30 cm	6.78 m^2 for Barrel.	
(4)	21 cm	30 cm		
(5)	24 cm	30 cm		
(6)	27 cm	30 cm		
(7)	33 cm	30 cm		
(8)	36 cm	30 cm		
Disks	r_{in}	r_{out}	z	
(1)	15 cm	39 cm	33 cm	
(2)	15 cm	39 cm	38 cm	
(3)	15 cm	39 cm	44 cm	10.16 m^2 for Disks
(4)	15 cm	39 cm	52 cm	(both sides)
(5)	15 cm	39 cm	61 cm	
(6)	15 cm	39 cm	72 cm	
(7)	15 cm	39 cm	85 cm	
(8)	15 cm	39 cm	102 cm	
(9)	15 cm	39 cm	122 cm	
(10)	22.5 cm	46.5 cm	146 cm	
(11)	28.5 cm	46.5 cm	182 cm	
(12)	34.5 cm	46.5 cm	218 cm	
(13)	40.5 cm	46.5 cm	258 cm	
		Total Area = 16.94 m^2		

II. Design of Silicon System

A. Parametric Performance Considerations

In this section the overall design parameters of the silicon tracker are explained in terms of parametric calculations. More detailed results are presented in the next section, II.B.

The parameters of the system are determined by several general considerations. The pattern recognition role dictates a minimum number of detector layers. This issue is discussed in the next section on simulation studies, which indicate that seven layers averaged over rapidity is a good choice. The vertexing requirement dictates a ratio between inner and outer radii of about four in order for the vertexing accuracy to be comparable to the individual detector measuring accuracy. To allow extrapolation to the outer tracker with an accuracy comparable to the size of an outer tracker measuring element (2 mm) requires about 25 cm of silicon tracking length. In the very forward direction, the silicon is the main element determining the momentum measuring accuracy and thus should have the largest lever arm affordable.

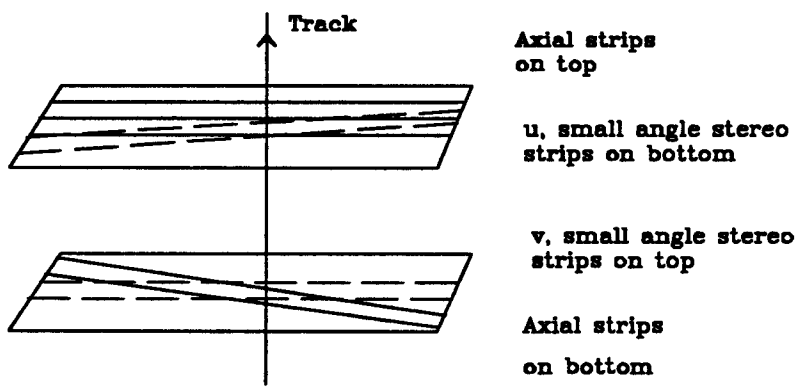


Fig. 2. Orientation of double-sided strips on radially adjacent detector pairs.

The strips on the detectors out of which the tracker is made are chosen to have 50 μm pitch. This will allow all bonding and circuitry to be located on one end, minimizing material and cost. Figure 2 shows an arrangement of adjacent strip layers for the barrel. The primary coordinate readout is the ϕ coordinate in cylindrical coordinates for both barrel and forward planar detectors. This is the coordinate exhibiting bending in a solenoidal field. A small stereo angle for the backside of the strip detectors provides a coarser measurement of the second coordinate which is the z coordinate in the barrel section and the r coordinate in the forward detectors. This allows a maximum contribution of the measurements on both sides of a given detector to the momentum determination. A choice of

resolution of about 1.5 mm (stereo angles of 10 mrads) for the coarsely measured coordinate is sufficient to avoid broadening the multiparticle mass resolution due to the angle determination in this coordinate.

In the discussion in this report, we will assume 12 μm measuring accuracy per double-sided silicon detector and 80 μm for each outer multiple-element superlayer of straws or fibers. With these numbers we can compare various alternatives. For example, taking as a goal a momentum error of 20% at 1 TeV for the non-vertex constrained momentum measurement, we find that a system with 11 equally spaced silicon layers or 11 outer detector superlayers would require an active tracking length of 80 cm and 2 m, respectively, plus the appropriate radiation stay clear areas for each technology. The mixed system chosen by SDC requires about 140 cm and therefore represents a compromise between limiting the radial extent and limiting the amount of silicon.

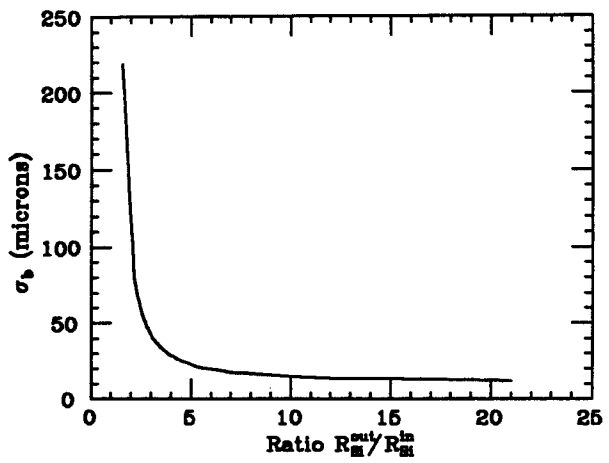


Fig. 3. Impact parameter error vs. detector geometry for high momentum.

1. Vertexing

We want the silicon to provide an impact parameter measurement with an error small enough for B and τ tagging, using reasonably high $P_\perp$ tracks. Assuming n equally spaced silicon layers with fixed measuring accuracy σ_m, the error on the impact parameter b, σ_b, is just a function of the ratio of the outer to the inner radius of the silicon detector for high $P_\perp$ tracks such that we can ignore multiple scattering. That is, $\sigma_b = \sigma_m f(R_{\rm Si}^{\rm Out}/R_{\rm Si}^{\rm In})$. Taking for definiteness, $n = 8$, Fig. 3 shows σ_b vs. the ratio of radii for $\sigma_m = 12$ μm. To get down to $\sigma_b = 25$ μm we need a ratio of radii $\gtrsim 4$. To minimize the effects of multiple scattering we need to minimize $R_{\rm Si}^{\rm In}$ as well as the material associated with the innermost layers. A

reasonable choice, given the severe radiation environment at small radii, is $R_{\rm Si}^{\rm In} \simeq 9$ cm and $R_{\rm Si}^{\rm Out} \simeq 36$ cm.

The desire to get sufficiently good vertex resolution from the silicon alone stems from two reasons. It allows good vertexing even in complicated events where the outer tracker may have difficulty in providing hit information and also, for the case of electrons, radiation makes the outer hits less usable for vertex reconstruction. Figure 4a–f shows the distribution of the displacement of the impact parameter from its true position using the silicon alone, or a full tracker with 5 outer straw superlayers, for 5, 10, and 50 GeV electrons. The calculations include measurement errors and multiple scattering as well as bremsstrahlung. The material in the silicon system at $\eta = 0$ was 6.5% X_0, including the beampipe. Table 3 lists the fraction of electrons lost if a cut at 2 σ_b, calculated for muons, were imposed on the electron sample.

2. Matching of Isolated Tracks

The main long term vulnerability of the above design is from radiation damage to the innermost silicon layers. In fact, as the machine goes up in luminosity the innermost layers of both the silicon and the outer tracker may lose functionality. However, we expect both the bulk of the silicon and the outer layers of the outer detector to function for many years at $\mathcal{L} = 3\text{–}5\times10^{33}\,\mathrm{cm}^{-2}\mathrm{sec}^{-1}$. If the information from both detector types can be linked, they will provide excellent momentum measurement for matching with electron and muon detectors since the momentum improvement due to the outer tracking elements is gotten almost entirely from the outermost layer. The linkage can be based on a track found in the silicon and a stiff hit pattern in the appropriate outer tracking superlayer. The linkage should work well if the occupancy in the outermost layer is not too great and the silicon measurement is good enough to predict the position at the outer detector with an accuracy approximately the size of an outer measuring element, which we assume to be about 2 mm [1]. For n equally spaced silicon layers, the curvature error for the track measured by the silicon alone can be written as

$$\sigma_K = \frac{\sigma_m \times \text{ constant}}{(R_{\rm Si}^{\rm Out} - R_{\rm Si}^{\rm In})^2}.$$

The error in extrapolation is dominated by the error σ_K for large radial extrapolations, so that the predicted circumferential position at the outer tracker radius R has an error

$$\sigma_{\rm extrap} = \sigma_m \times \text{ constant} \left[R/(R_{\rm Si}^{\rm Out} - R_{\rm Si}^{\rm In})\right]^2.$$

Taking $n = 8$ layers, $R = 1.6$ m, $\sigma_m = 12$ μm, Fig. 5 shows the error, $\sigma_{\rm extrap}$,

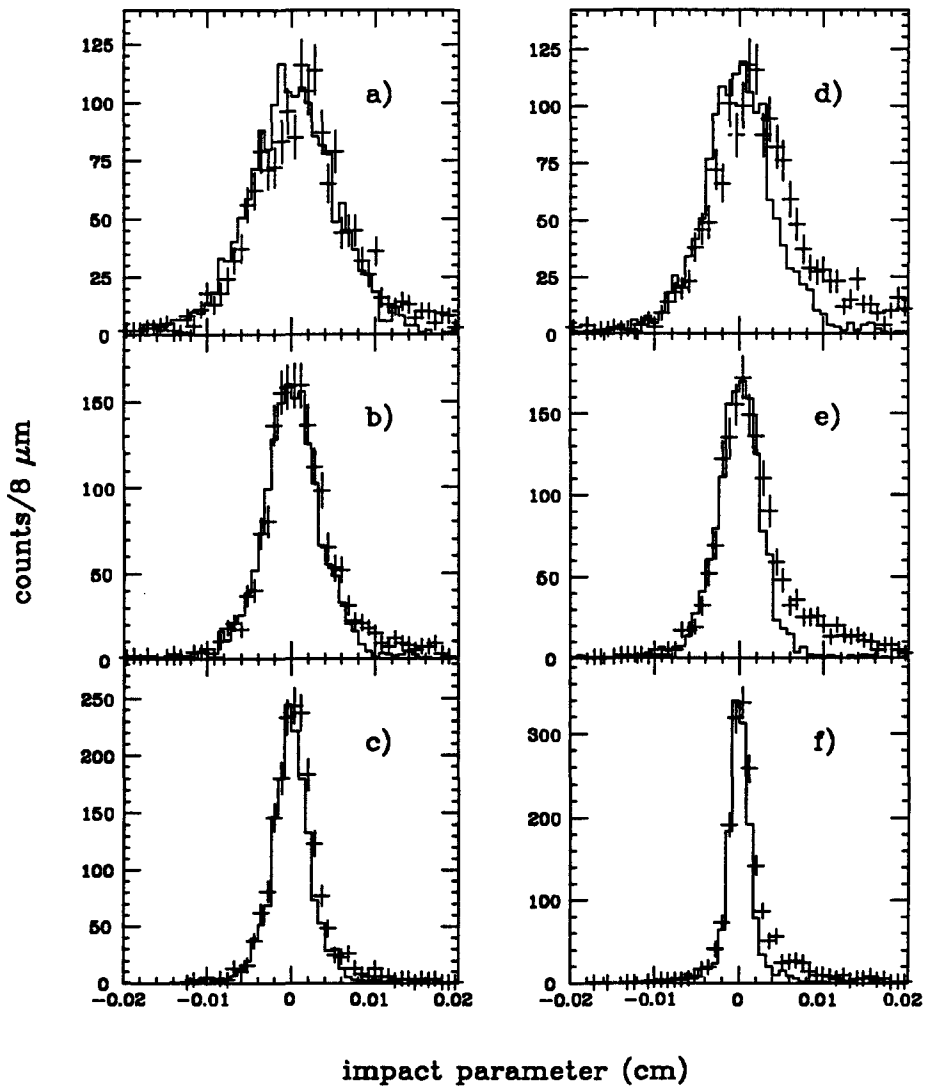


Fig. 4. Impact parameter distributions for e^- (crosses) and μ^- (histograms) single track events generated from $z = 0$ at fixed $P_\perp$ and uniformly in η over the range $|\eta| < 2.5$. Impact parameter determined from the silicon system alone for $P_\perp = 5, 10$ and 50 GeV tracks [a)–c), respectively] and for the combined silicon and straw tube system [d)–f)].

Table 3. Fractional Losses in %

Fraction of Events Lost	5 GeV	10 GeV	50 GeV
2 σ_b cut with Silicon Alone for e^-	15.2	12.3	11.2
for μ^-	4.4	3.2	4.9
2 σ_b cut with Full System for e^-	24.1	25.4	25.8
for μ^-	5.5	5.3	8.3

as a function of radial coverage of the silicon, $R_{\rm Si}^{\rm Out} - R_{\rm Si}^{\rm In}$. For 24 cm coverage, $\sigma_{\rm extrap} = 2$ mm. A radial coverage of 20–25 cm for high $\mathcal{L}$ should be adequate for linking, provided enough silicon layers are available for robust pattern recognition of stiff tracks. The baseline design has $R_{\rm Si}^{\rm Out} - R_{\rm Si}^{\rm In}$ typically 27 cm.

3. Rapidity Coverage of the Detector

The silicon tracker in Fig. 1 has elements spaced over a large distance in z, in order to cover a large range in rapidity. This complicates the mechanical support, but is necessary at a hadron collider where particles of interest often emerge at small angles to the beam. Figure 6 shows the expected efficiency to contain all four leptons from the "Standard Model" Higgs boson decay for several possible Higgs masses. A detector covering rapidities up to $|\eta| \leq 2.5$ (10° to the beam) is a practical compromise, giving acceptance > 50% without having to cover impractically small production angles.

4. Geometric Characteristics of Design

The previous sections have specified for the measured points on a track that the silicon detector provide an average of seven hit detector layers averaged over rapidity, 27 cm of radial extent, and a ratio of 4 between the outer and inner radii. Figures 7a), b), and c) show the number of hits, the radial extent and ratio of radii, vs. rapidity after averaging over a $\sigma = 5$ cm beam–beam interaction region in z. Contributions are separately shown for the barrel and disk detectors. These are seen to mesh together rather well. The ratio of radii is, however, only reasonably well maintained near 4 for $|\eta| < 2$.

B. Pattern Recognition and Physics Studies

The silicon detector simulation allows for a flexible description of the detector, in order to investigate a wide variety of designs. In the GEANT framework, detectors and inert material are described by a hierarchical volume structure. For the silicon system, the lowest level volumes are the detector wafers, which are positioned within layer volumes that simulate the support material. Each wafer has axial (or radial) strips on one side and stereo strips on the other, and an inactive region (default 500 μm) at the edges. The detector configurations involve wafers which are bonded together into larger "readout units" and which are "shingled" to avoid excess dead space. This is shown more graphically for the barrel detector in Fig. 7a. Fig. 7b shows a typical forward planar detector array.

The GEANT routines transport particles through the apparatus and generate decays and interactions with material, including conversions, bremsstrahlung, and delta rays. When a charged particle crosses a silicon wafer, the amount of dE/dx

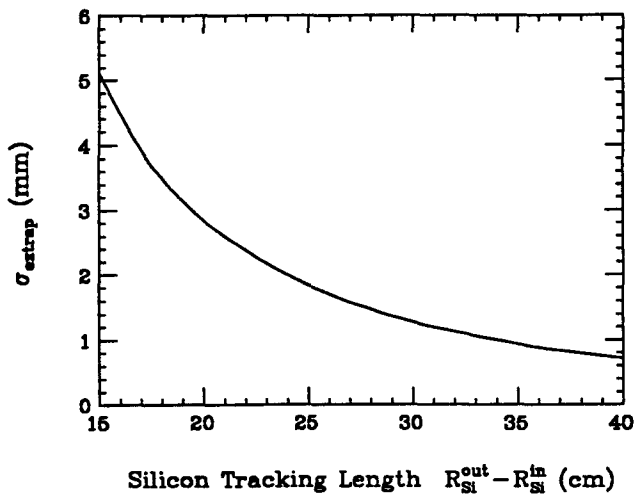


Fig. 5. Position error at 1.6 m radius vs. silicon tracking length.

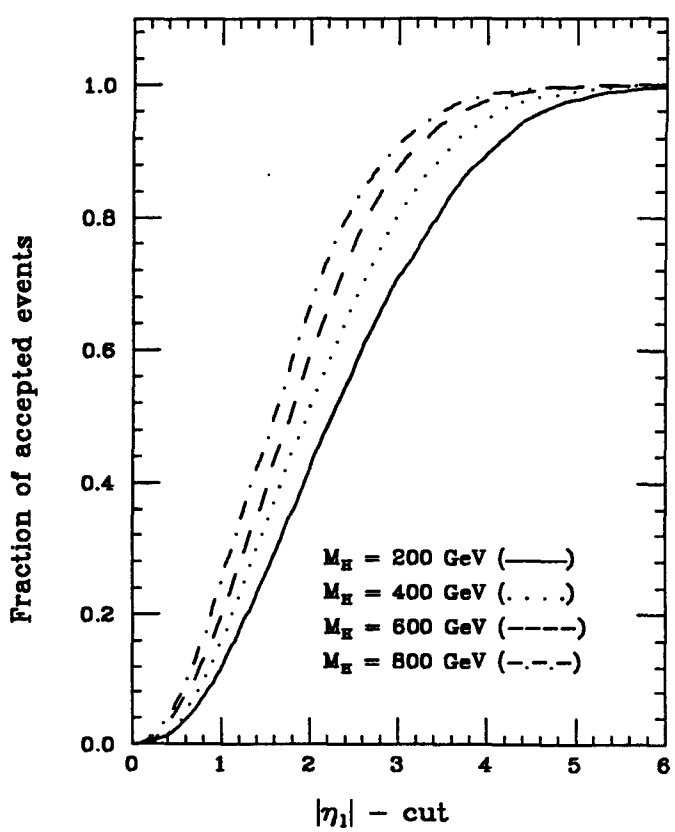


Fig. 6. Acceptance for all four leptons from $H^0 \to Z^0 Z^0$ decay vs. rapidity coverage.

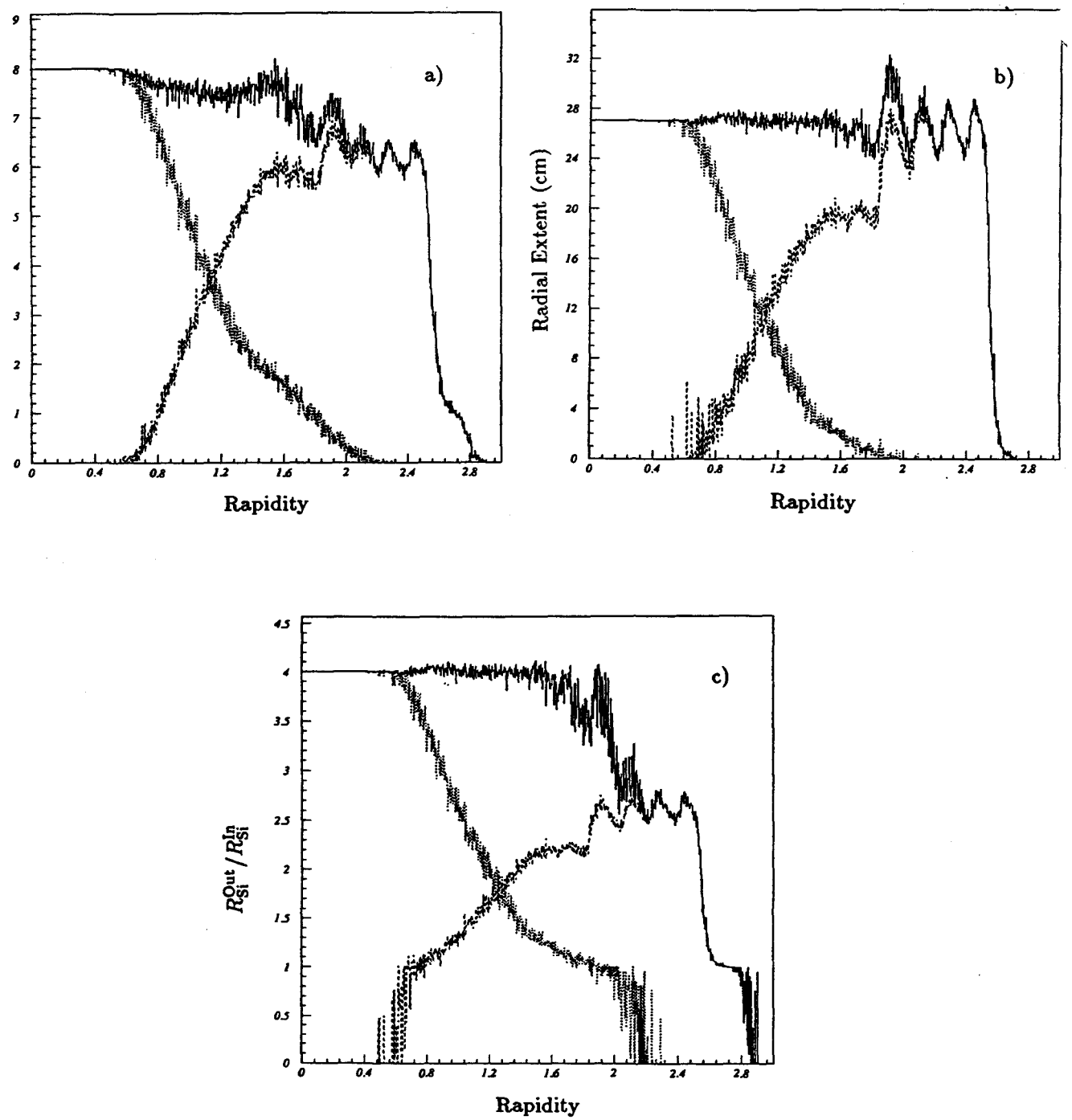


Fig. 7. a) Number of silicon detectors crossed vs. rapidity. Contributions from barrel and disks shown separately. b) Radial extent of silicon detectors vs. rapidity. Contributions from barrel and disks shown separately. c) Ratio of outermost to innermost radius for silicon detectors hit, vs. rapidity.

energy deposited in each strip is recorded and compared with a threshold. Clusters of strips with energies above the threshold are recorded in the raw data banks, with no analog information kept. At present, the effects of noise and charge sharing from the magnetic field and diffusion are not included.

Figure 8 shows the number of axial hits on tracks vs. rapidity for the detector configuration in Fig. 1. This calculation includes smearing of the vertex along the beam direction with a standard deviation of 5 cm. The design provides typically 8 hits below a unit of rapidity, 7–8 from 1–2 units of rapidity, and 6 or 7 from 2–2.5 units.

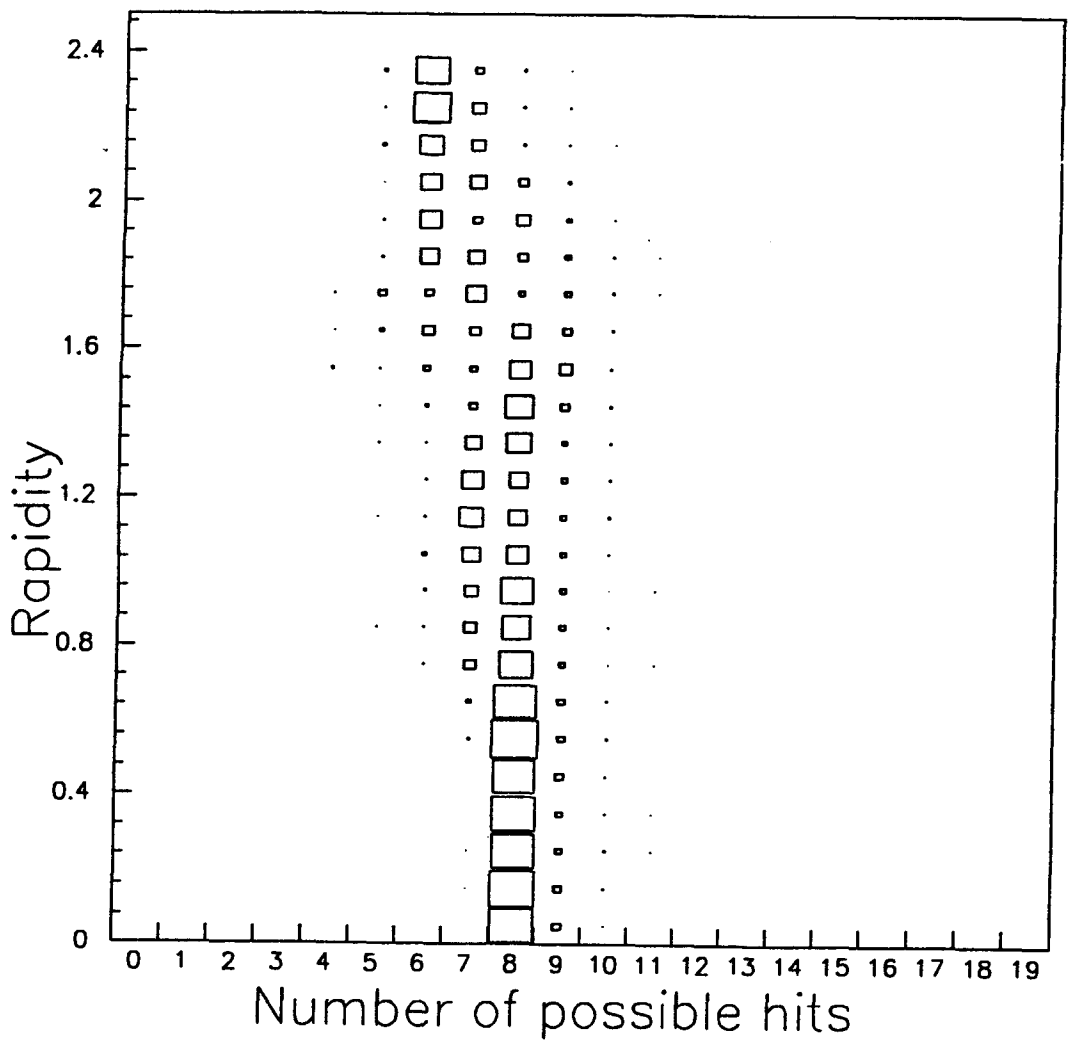


Fig. 8. Number of detectors hit for design in Fig. 1. Calculation includes vertex smearing. Box width is proportional to number of tracks.

The raw data are reconstructed using the algorithm described in Ref. 2, briefly summarized here. The coordinate reconstruction matches an axial strip with a stereo strip (if possible) within a wafer and the results are expressed in the cylindrical coordinates r, ϕ and z. Segments are formed between 2 adjacent layers, connecting coordinates that are close in ϕ, and requiring the extrapolated z_0 to be within the range $|z_0| < 25$ cm. At this point the segment parameters ϕ_0, ρ (curvature), z_0 and $s = \tan\lambda$ (λ = dip angle) are determined with respect to the distance of closest approach to the origin. For the forward disks, the segment parameters are combinations of the above parameters which are more appropriate for the geometry [3].

The track reconstruction program used for this report has several steps. The first is to take the segments from the silicon system and make clusters from segments that have close values of ϕ_0, ρ and z_0, s. The association is a χ^2 match based on the estimated error in the parameters and an estimate of multiple scattering. The barrel and forward segments are clustered separately as they have different parameter sets. Candidate tracks are clusters with at least 2 segments.

The second step is to take the list of hits in the candidate tracks and perform an iterative 5 parameter fit (the parameters ϕ_0, ρ, z_0, s and the impact parameter b_0). The fit includes multiple scattering in the silicon layers. Next, the algorithm tries to delete points that contribute the most to the χ^2 if the result from the first fit has a large χ^2. A road technique is then used to pick up hits that were missed in the silicon as well as add information from other systems and also to join tracks which cross both the silicon barrel and forward regions. Hits near the track are picked up individually and then the track is refit, to guarantee the best possible estimate when extrapolating.

In the following sections, the silicon system (as described in section I) and an outer system of straw tubes was used. The straw tube system consisted of 3 axial superlayers and 2 superlayers with 3° stereo angle.

1. Higgs Boson

The decay of a neutral Higgs boson (mass = 300 GeV) $H^0 \rightarrow Z^0 Z^0 \rightarrow e^+e^-\mu^+\mu^-$ has been studied with the combined silicon and straw system. The ISAJET generator was used to produce the Higgs event and PYTHIA minimum bias events were added as background. The design luminosity was simulated by a Poisson-distributed mean of 1.6 background events for each bunch crossing, with a total of 7 crossings (−4 to +2 from the crossing with the Higgs) used to account for loopers and long drift times in the straw system.

Figure 9 shows the reconstructed efficiency vs η for all tracks with transverse

momenta above 1 GeV for 200 Higgs events at design luminosity. (A beam constraint of 10 μm was used for tracks with small impact parameters after the initial set of iterations.) Tracks were required to have at least 4 axial silicon hits or 3 axial silicon hits and 1 straw segment. For tracks with $P_\perp > 20$ GeV, the efficiency (averaged over all η) is 99%. The number of fake tracks (tracks which have more than 2 hits from another Monte Carlo track) with $P_\perp > 5$ GeV is found to be 0.03 ± 0.01 per event.

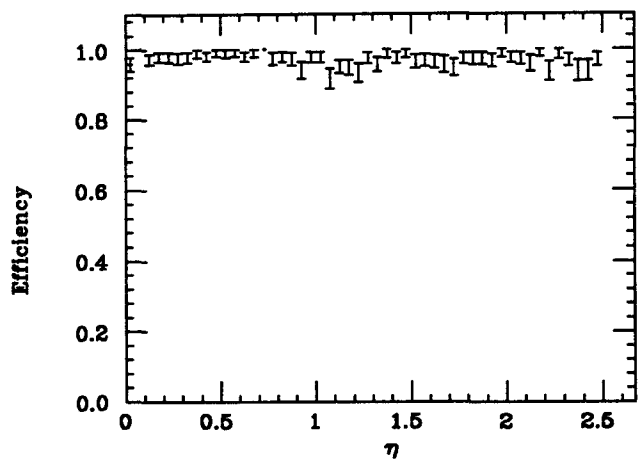


Fig. 9. Efficiency of single tracks with $P_\perp > 1$ GeV as a function of pseudorapidity.

To identify the gauge boson decay products, tracks are assumed to be identified as either an electron or a muon, using the Monte Carlo information in place of the calorimeter or muon system. Leptons are required to have $P_\perp > 10$ GeV and electrons to have $P_{\rm gen}/P_{\rm fit}$ within the range 0.7 to 1.4 to simulate the calorimeter energy and track momentum matching cut. In the case of electrons, the tracking momentum for these cuts is based on a refitted value using only the silicon information in order to minimize the effects of bremsstrahlung. Note that all leptons passing the above cuts were used in the analysis; therefore such leptons from b decays and conversions were considered.

To pair the leptons in order to make Z^0 candidates, the following algorithm was used. All pairs of same type, opposite sign leptons were made and the invariant mass was calculated. The invariant mass of the electrons was formed using the direction information from tracking but smearing the generated energies by the calorimeter resolution, since this typically provides the most accurate value of the electron energies. The muon invariant mass was calculated using the reconstructed momentum from the central tracking system only. The list of Z^0 candidates was made by ordering the pairs by their closeness to the Z^0 mass and then accepting

pairs so that each lepton was used only once. The invariant mass of the electron pairs is shown in Fig. 10a, and the muon pairs in Fig. 10b. A cut requiring the invariant mass to be within 10 GeV of the Z^0 mass was then used to further restrict the list before the Higgs was reconstructed.

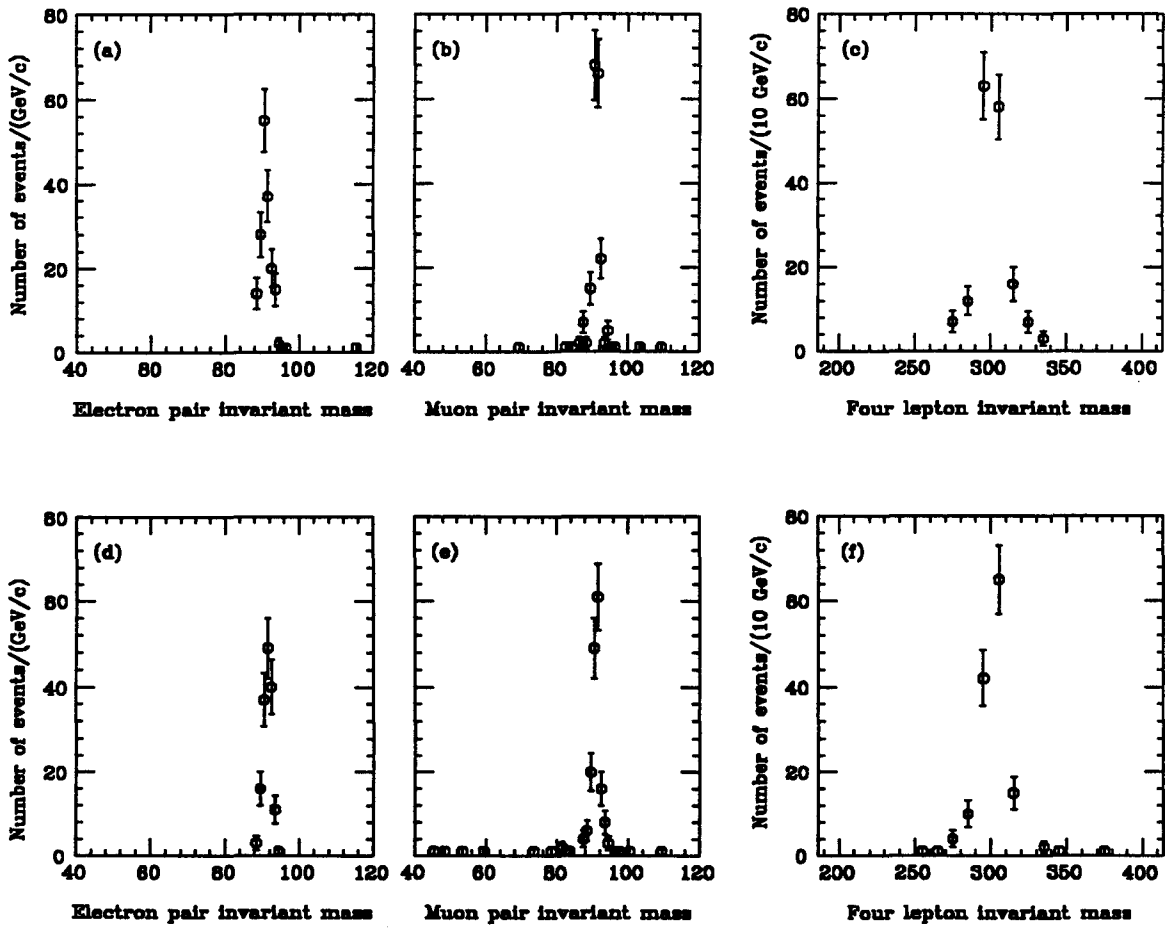


Fig. 10. a) Dilepton invariant mass distribution for electrons that have passed the P_{gen}/P_{fit} cut. b) Dilepton invariant mass distribution for muons. c) Reconstructed (solid) and generated (dashed) four-lepton invariant mass distribution for a 300 GeV Higgs. (d)–(f) similarly for 6×10^{33} cm^{-2}s^{-1}.

The four lepton invariant mass is plotted in Fig. 10c for events with two Z^0 candidates. Figures 10a–c are for the design luminosity of 10^{33} for which the efficiency for reconstructing the Higgs is 84%. This includes a small loss for events where the leptons did not all pass the 10 GeV $P_\perp$ cut. Table 4 summarizes the

detector performance for this decay mode. In addition, the analysis was performed at luminosities of 3×10^{33} and 6×10^{33} with smaller event samples. All results are shown in Table 4 and the invariant mass plots for the 6×10^{33} luminosity case are in Figs. 10d–f.

It is seen that the tracking detector should allow excellent performance for Higgs reconstruction well beyond the design luminosity. This is the single most important design goal for the detector. The track reconstruction was also performed without using information from silicon barrel layers 1 and 2 (at r=9 and 12 cm respectively) to check that the design is robust against some inefficiency. Note that occupancy in the silicon system is not a problem even at six times design luminosity and thus does not impair high luminosity performance.

Table 4. Summary of efficiencies and number of fake tracks for $H^0 \rightarrow e^+e^-\mu^+\mu^-$ events for various configurations.

Luminosity/ Configuration	Fakes per event with $P_\perp$ >5GeV	Track Efficiency $P_\perp$ >20GeV	Electron E/p Efficiency 0.7<E/p<1.4	M_Z cut Efficiency e	M_Z cut Efficiency μ	Higgs Reconstruction Efficiency
1×10^{33} 8 layer STS + straws	0.03 ± 0.01	0.991	0.96 ± 0.01	0.99 ± 0.01	0.99 ± 0.01	0.84 ± 0.04
1×10^{33} 6 layer STS + straws	0.02 ± 0.01	0.963	0.93 ± 0.01	0.99 ± 0.01	0.97 ± 0.01	0.71 ± 0.04
3×10^{33} 8 layer STS + straws	0.04 ± 0.02	0.983	0.96 ± 0.01	1.00 ± 0.01	0.97 ± 0.02	0.83 ± 0.04
6×10^{33} 8 layer STS + straws	0.18 ± 0.03	0.972	0.93 ± 0.01	1.00 ± 0.01	0.93 ± 0.02	0.75 ± 0.04
6×10^{33} 6 layer STS + straws	0.06 ± 0.02	0.956	0.93 ± 0.01	1.00 ± 0.01	0.90 ± 0.02	0.65 ± 0.04

2. Jets

Tracking particles inside jets will be an important task for the SDC tracking system for a number of reasons, including finding leptons from semileptonic decays, secondary vertexing for recognizing b-jets, and studying jet properties in detail. The efficiency for reconstructing tracks within jets has also been studied with the simulation and track reconstruction program described above. The method and results are similar to a previous study [2]. However, the GEANT simulation used

here is more realistic both for particle interactions with material and the detector geometry, which includes dead area, wafer tilt and staggering. Also, the design presently starts at 9 cm radius rather than the 18 cm used in the previous study.

Two-jet events were generated at several $P_\perp$ thresholds (50, 100, 200 and 500 GeV). For this work, no background minimum bias events were added, justified by the expectation that in jets, the loss of efficiency will be due to local track density from the jet itself. Tracks were reconstructed with the same algorithm parameters used in the Higgs study, using data from the silicon system only. (Further work will add data from the outer systems).

The jet momenta were reconstructed by summing the momenta of Monte-Carlo final state particles clustered within a cone of opening angle $R \equiv \sqrt{\Delta\eta^2 + \Delta\phi^2} <$ 0.5 units. The jets were required to have $P_\perp > 20$ GeV and $|\eta| < 2.0$.

Charged tracks were considered if they had $P_\perp > 1$ GeV, $|\eta| < 2.5$, impact parameter $|b_0| < 1$ cm, and $\Delta R < 0.5$ units to a jet axis. Figure 11 shows the efficiency for reconstructing these tracks within the jets as a function of the jet transverse momentum. Two sets of data points compare this efficiency for 10 and 20 milliradian stereo angle. The larger stereo angle shows slightly lower efficiency, due to two things:

- increased dead area on the stereo side of the wafer, typically 2% for 20 milliradians compared to 1% for 10 milliradians.
- increased ambiguity for matching axial and stereo hits for closely spaced tracks, leading to larger combinatorics during segment clustering.

The primary loss of efficiency is due to tracks being merged together during segment clustering. The efficiency within jets is above 90% for jet $P_\perp < 200$ GeV and is somewhat lower than that determined in the previous study with a less realistic simulation and more detector layers [2]. In Fig. 12 the efficiency is shown as a function of the fragmentation variable z (the momentum fraction carried by a single particle) for two jet $P_\perp$ intervals. For the higher $P_\perp$ interval ($200 < P_\perp < 400$ GeV), the efficiency decreases to about 60% for high $P_\perp$ tracks ($z \sim 0.2$). We expect these numbers to improve as we improve our track finding algorithms.

3. Top

The ability to recognize B jets is expected to be an important tool for studying the $t\bar{t}$ system by reducing the non-$t\bar{t}$ background by orders of magnitude, and also reducing combinatoric background for measuring the mass of the t quark. Assuming a standard model top with mass well above that of the W, it will decay, in general, into a W and a b quark jet with typical $P_\perp$ of 50 GeV. The $t\bar{t}$ production

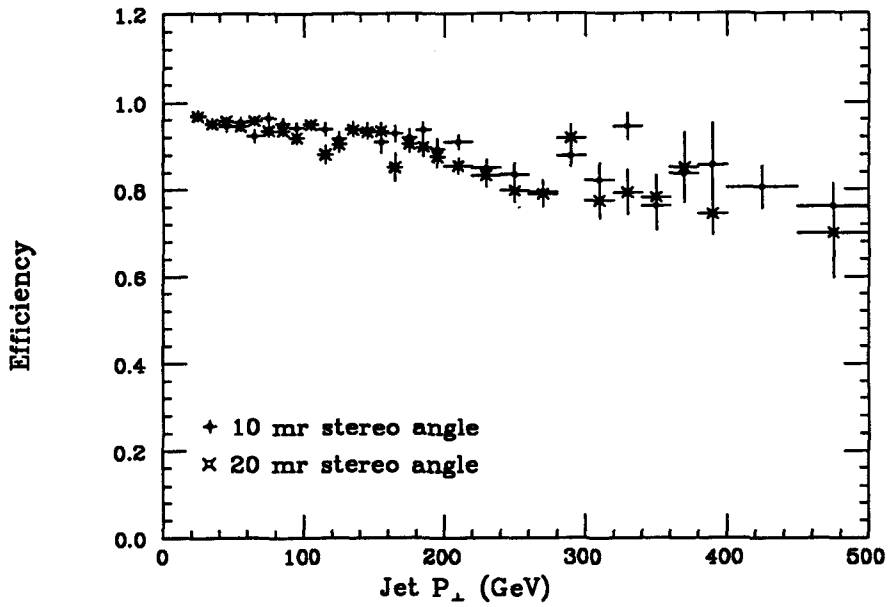


Fig. 11. Efficiency for reconstructing tracks with $P_\perp > 1$ GeV inside jets as a function of the jet transverse momentum, for two values of the stereo angle.

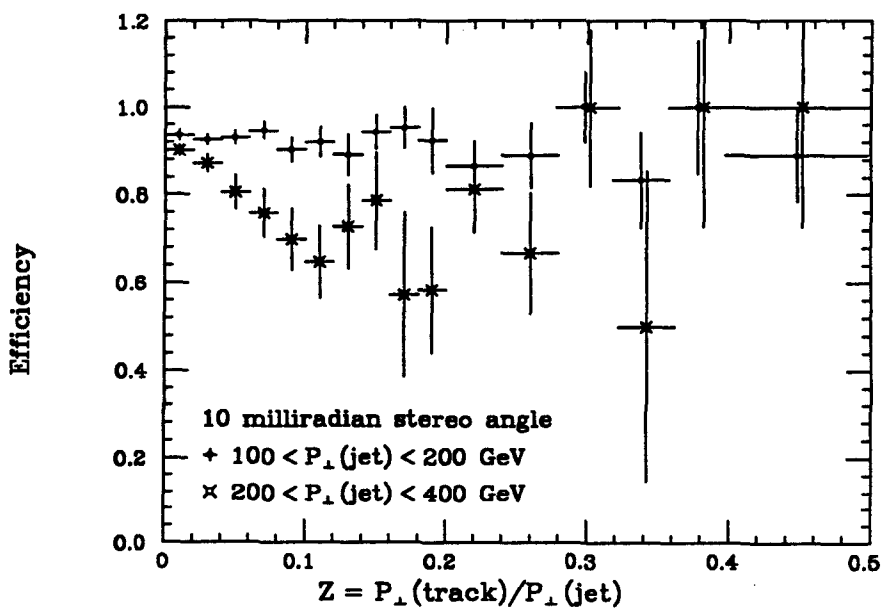


Fig. 12. Track reconstruction efficiency as a function of the fragmentation variable z (for two intervals of jet $P_\perp$). The stereo angle used was 10 milliradians.

cross section is reasonably high, so it may be studied during the early running period, at luminosities well below the design.

The efficiency for identifying the B jets through secondary vertices has been investigated with the GEANT simulation and full event reconstruction. A simple algorithm was used, which was to count the number of reconstructed tracks with significant impact parameter inside a jet. Assuming the calorimeter provides the jet direction with precision better than ≈ 0.1 in η and ϕ, tracks were considered within the cone $\Delta R < 0.5$ to the jet axis. Only tracks with measured $P_\perp > 0.8$ GeV and $b_0 < 1$ cm were considered (the latter cut to discriminate against other secondaries) and the impact parameter was required to have the correct sign to be consistent with originating from the decay of a particle moving in the jet direction.

ISAJET was used to generate B and "generic" jets in separate jobs, and tracks were reconstructed with the combined silicon and straw system. As shown in Figure 13, using both the silicon and outer tracking system improves the impact parameter measurement over the silicon alone, particularly at large momenta. Requiring 3 or more tracks with impact parameter greater than 3σ, Figure 14 shows the efficiency for tagging B jets compared to light quark jets. For B jets with $P_\perp > 40$ GeV, the efficiency is approximately 30%, and the rejection of the non-B jets is very high. With a looser requirement of 3 tracks with $\geq 2\sigma$, the efficiency is typically 40% for the B.

The efficiency for single- and double-B tagging in $t\bar{t}$ events was evaluated previously at the Monte Carlo generator level, without detailed simulation [4]. That study estimated the efficiency for identifying one or both B jets in a $t\bar{t}$ event to be approximately 70% for M_{top}=150 GeV, assuming an efficiency of 50% for B jets with $P_\perp > 30$ GeV. Using the B tagging result from the GEANT simulation, the efficiency for tagging one or both B jets from $t\bar{t}$ decay is estimated to be around 50%, assuming only secondary vertices are used.

C. Material and Electron Identification

The SDC tracking system differs in at least two significant ways from previous tracking systems in collider experiments: the tracking technologies that are matched to SSC physics have intrinsically more mass, and the desire to provide tracking over the rapidity interval $|\eta| < 2.5$ means that much of the mechanical support material for the tracking system is inside the tracker. As a result the SDC tracking system will have more material than previous collider experiments. In this section we review the results of the recent "Impact of Material in the SDC Tracking System" study [5] as they relate to the design and optimization of the silicon tracking subsystem. Although the systems that were considered are not

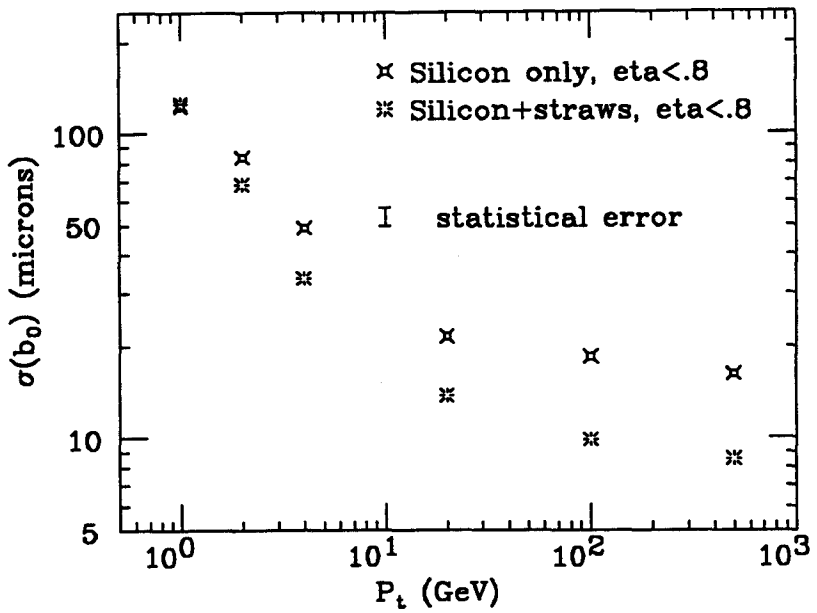


Fig. 13. Impact parameter resolution for single muons as a function of $P_\perp$ over different η ranges. Note that the resolution of the combined system is ~ 9 μm, compared to 18 μm for the silicon system alone.

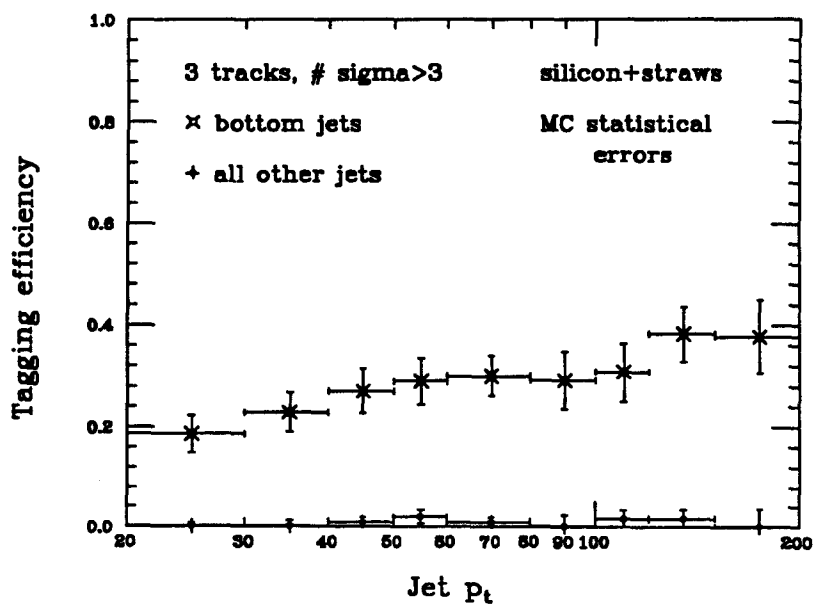


Fig. 14. b tagging efficiency vs. jet $P_\perp$ for the combined system using the method described in the text.

identical to the one is this report, they are close enough that the conclusions can provide guidance for our design.

The material in the silicon tracking subsystem impacts the SDC trigger, and the reconstruction and identification of electrons (and photons) as follows:

a. *Triggering:* Electron bremsstrahlung and photon conversions will occur in the material in the SDC tracking system. Electron bremsstrahlung will put some high $P_\perp$ electrons below the Level 1 tracking trigger threshold resulting in a smearing of the $P_\perp$ threshold. Photon conversions will result in a number of high $P_\perp$ electrons that will pass the Level 1 trigger, and may result in a loss of prompt high $P_\perp$ photons at the trigger level.

b. *Momentum resolution:* Bremsstrahlung in the material in the silicon tracking subsystem will lead to degraded momentum resolution for electrons.

c. *EM Calorimetry:* Electromagnetic showers are identified by requiring that Had/EM is small, and that transverse shower profiles are consistent with an EM shower. Bremsstrahlung in the silicon tracking subsystem results in several energy deposits in the EM calorimeter rather than one from the electron shower. This results in altered transverse shower profiles, as measured in EM towers and in the strip detectors at shower maximum. As a result EM clusters may be reconstructed with reduced efficiency.

d. *e/γ ID:* e/γ separation is achieved by identifying a charged track pointing at the EM shower and $e/\pi^{\pm}\pi^0$ separation is achieved by track–shower matching using the strip detectors at shower maximum, and by requiring a selection on E/p near 1. Degradation of the electron momentum resolution and the EM calorimeter cluster position resolution will result in reduced efficiency for e/γ identification.

The conclusions of Ref. 5 are that the most significant impact of the SDC tracking material is through e bremsstrahlung. As noted above, bremsstrahlung smears the e trigger threshold(s), and reduces the efficiency for identifying electrons cleanly. The limitation of the material is most stringent for the tracking elements closest to the beam. Thus it is recommended that the material in the silicon tracker is not more than 5–6% X_0 at $\eta = 0$.

The remaining tracking material before the Level 1 tracking trigger should also be minimized. As an example, $\sim$ 10% X_0 of material (exclusive of internal bremsstrahlung) before the Level 1 tracking trigger elements results in a significant "softening" of the e high $P_\perp$ trigger. Efforts should be made to keep below this amount of material. With this level of material before the Level 1 tracking trigger elements, the rates for isolated electrons from the conversion of QCD prompt

photons are tolerable relative to the physics backgrounds: W$\rightarrow e^{+-}$, Top$\rightarrow e^{+-}$, etc.

Unlike previous collider tracking systems, the silicon tracking system in SDC is sufficient for track reconstruction and is sufficient to make a determination of the track momentum and direction. This is important for the identification of electrons in SDC. Bremsstrahlung affects the measurement of the momentum of electrons. Simulations suggest that uniformly spaced material in the tracking region is approximately equivalent to 1/2 as much (inert radiator) material before the tracking system in terms of its effect on the error in momentum. Thus the material in the SDC tracker, using the silicon system to measure the momentum and direction of electrons, is equivalent to 1/4 to 1/3 the effective material in the entire tracking system (assuming approximately equal material in X_0 in the inner silicon and outer tracking subsystems). Consequently an SDC tracker with 10–12% X_0 at $\eta = 0$, which averages to 18–19% X_0 for $|\eta| < 2.5$ including internal bremsstrahlung, the beam pipe, and air, corresponds to an average value of 4-5% X_0 (excluding internal bremsstrahlung) radiator before the tracking system. For comparison, the average amount of material inside the CDF central tracker is 3–4% at present, and will increase to 5–7% with the addition of the new SVX vertex detector.

Simulations utilizing the power of the silicon system indicate that electron tracks can be identified with efficiencies comparable to those in CDF [6] reported in Table 5. The observations and conclusions relevant to the silicon tracking subsystem include:

a. *Track Reconstruction:* Using only the silicon tracking subsystem, with $\sim 6.8\%$ X_0 at $\eta = 0$, the efficiency for reconstructing (isolated) single tracks was 98–99% for electrons and for muons.

b. *E/p:* With material distributed throughout the SDC tracking volume, highest E/p efficiencies are obtained using only the inner (silicon) tracking system for the momentum measurement. E/p efficiencies $\sim$ 95% for $E/p < 1.5$ were obtained for a silicon system with 6.8% X_0 at $\eta = 0$.

c. *EM isolation:* The e efficiency is reduced at low $P_\perp \sim 10$ GeV as a result of e Bremsstrahlung occurring at or near the beam (i.e., far from the EM calorimeter). Scaling the $\sim 3\%$ X_0 from internal bremsstrahlung and from material in the beam pipe to the mean radius of the silicon tracking system, suggests that the material in the silicon tracker should not be greater than $\sim 5\%$ X_0.

d. *Track–Shower Match:* For a silicon plus outer tracking system with $\sim 11.5\%$ X_0 at $\eta = 0$, approximately 94% of the electrons pass a "tight" track–shower maximum $r\phi - z$ match with a rectangular window of 10 mm in the bend plane and 5 mm in the non-bend plane.

Table 5. CDF selection cuts and efficiencies for electrons from $Z \rightarrow e^+e^-$ with $E_T > 20$ GeV in the $|\eta| < 1$ region of the calorimeter.

Cut Type	Cut Value	Efficiency (%)
Hadron/EM	< 0.05	96.8 ± 1.3
LSHR	< 0.2	97.8 ± 1.1
$r\phi$ match	< 1.5 cm	98.9 ± 0.8
Z match	< 2.0 cm	99.5 ± 0.5
Wire χ^2	< 10	86.5 ± 2.5
Strip χ^2	< 10	96.6 ± 1.7
E/p	< 1.5	92.5 ± 1.9
Total		77.4 ± 3.1

A study using $Z \rightarrow e^+e^-$ events to calibrate the EM calorimeter found that the amount of material preceding each calorimeter tower must be known to within 5% X_0 to establish the correct peak value of E/p. The number of electrons required increases exponentially with the amount of material. The calibration time was estimated to be $\sim$ 1 month at SSC design luminosity for an average value of $\sim$ 16% X_0 in the tracking system. This material corresponds to $\sim$ 11% X_0 at $\eta = 0$.

Based on the above, we have chosen as a goal for the silicon tracker, including the beam pipe, a total number of radiation lengths $\leq 6\%$ at normal incidence and $\leq 7\%$ averaged over $|\eta| \leq 2.5$. Figure 15 shows the material as a function of η, in radiation lengths, for the detector arrays shown in Fig. 1. The value at $\eta = 0$ is 2.6% and the rapidity averaged value is 2.9%. The beampipe, main support elements (cylinders, spaceframe, outer enclosure) and power cables contribute about 1.2% X_0 at $\eta = 0$. This allows about 0.25 X_0 averaged over a layer for the electronics and its cables, and the cooling structures.

D. Alignment Goals

A quantitative study of the effect of systematic errors and alignment has been presented in Ref. 7. We summarize the main conclusions here. The related mechanical issues are discussed below in the section on support structures and cooling. In addition, we plan on using X-rays to map out individual wafer locations on detector subassemblies as well as in the final assembly. An example of how this can be done is given in Ref. 8. We note that if we can meet our alignment goals for the silicon system then the use of extrapolated tracks into the outer tracking device should allow for a good check of the positioning of these devices.

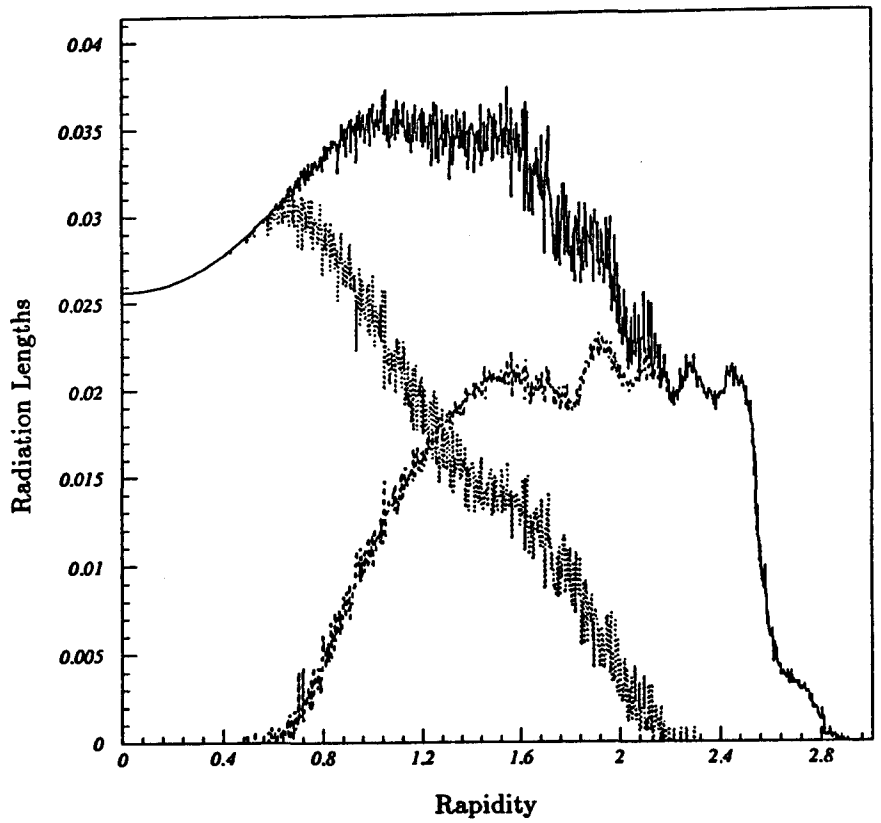


Fig. 15. Average material in silicon detectors for array in Fig. 1. Smearing due to the beam length in z has been included and contributions from barrel and disks are separately shown.

Our physics goals are: A degradation of the momentum resolution $\leq 10\%$ due to random placement errors and $\leq 33\%$ for correlated errors. These lead to the following goals for the detector stability relative to a data base of positions:

Circumferential position error	≤ 5 μm.
Radial location error	≤ 80 μm
Longitudinal location error	≤ 250 μm

The transverse momentum is measured using the circumferential position at given radii and hence the greatest stability is needed for this coordinate. The radial error produces a circumferential error for a detector of fixed width, giving the limit above on the radial location. The tolerable longitudinal error is largest since we measure this coordinate with the largest statistical error.

The alignment plan is to place detectors within subassemblies (cylinders or planar disks) with radial and longitudinal errors consistent with the numbers above. The goal for the circumferential placement is 25 μm. The alignment process would then involve measuring this one coordinate within the 5 μm limit above. The

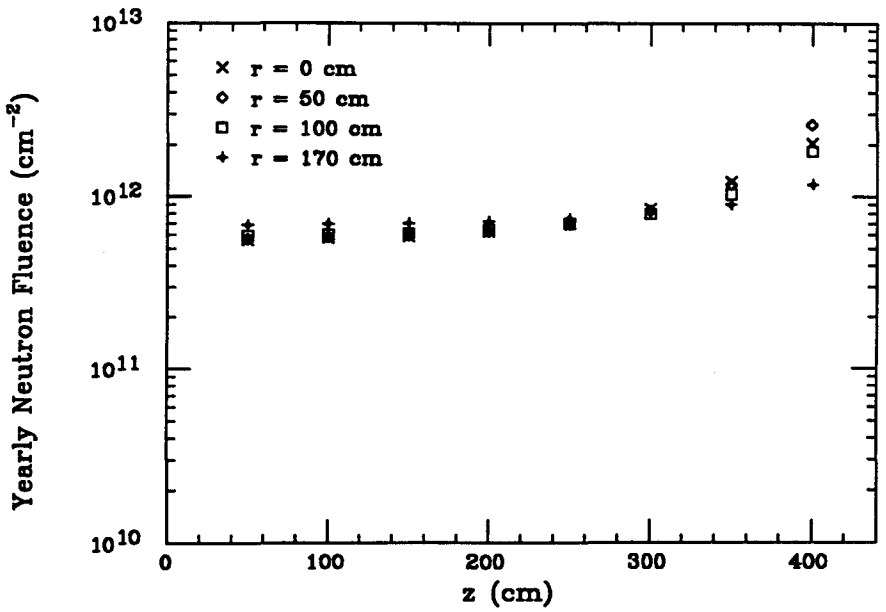


Fig. 16. Yearly neutron fluences in the SDC tracking volume, at $L = 10^{33}$ (cm^2 sec^{-1}).

subassemblies would then have to be accurately located within the large mechanical framework which must have a long term position stability consistent with our goals. We plan to measure and monitor locations with beam particles to continually verify the alignment.

E. Radiation Lifetime

1. Neutrons in the Tracking Volume

Neutrons from the calorimeter albedo are the principal source of neutrons (typically 1 MeV) inside the SDC tracking volume. Following the prescription of Ref. 9, we have simulated the spatial distribution of the neutrons from the SDC Lead-Scintillator (Pb-Sc) calorimeter containing a cylindrical cavity of half length $L = 420$ cm, radius $R = 205$ cm and beam hole radius $O = 42$ cm at $z = 420$ cm. Details of the simulation are given in Ref. 10.

The average number of reflections from the calorimeter face was assumed to be equal to one for an unlined calorimeter. For the yearly fluences, the luminosity assumed was $10^{33}\text{cm}^{-2}\text{sec}^{-1}$ for 10^7 sec. Figure 16 shows the fluences for radii $r = 0$, 50, 100, and 170 cm, respectively. The increase for large z, close to the beam hole, is obvious.

We also consider the case of lining both endcap faces with 10 cm polyethelene [11]. The effect of the polyethelene for a spherical calorimeter void is shown in

Fig. 17 (from Ref 11): accounting for a factor 2 due to reflections we deduce, for a 10 cm liner, a reduction of a factor of 5 in the direct albedo and a total suppression of the reflected albedo from the lined surface. In our simulation, shown in Fig. 18, this results in a reduction of the neutron fluence of about 2 in the low z region and up to 5 close to the endcaps. Moreover in this case the fluences become extremely uniform over the whole cavity. Typical yearly fluences are:

	No liner	End caps lined
all r, $\|z\| < 250$ cm	6×10^{11}	3×10^{11}
$r = 100$ cm, $z = 400$ cm	2×10^{12}	4×10^{11}

Based on the above, the desired liner would cover the full endcap and have a thickness of 12 cm, to allow a small safety factor relative to the neutron predictions we are using for the 10 cm case. It has also been suggested that the liner include a thin layer of boron to absorb neutrons below 100 keV, which we will have to investigate in the future.

2. Charged Particle Fluences

We quantify below the fluence from particles produced directly from the beam–beam interactions. For the case of an endcap liner which suppresses neutrons, the fluence is dominated by charged particles from interactions over the whole silicon tracker.

For a uniform rapidity distribution, with no magnetic field, the particle fluence is a function of the radius in cylindrical coordinates. For the silicon detectors in a given cylindrical array the number of particles incident per unit area at larger rapidity decreases but the path length in the detector increases such that the radiation damage is constant in the layer. The varying path length will have to be taken into account when setting optimum thresholds in the different modules making up a layer.

With a magnetic field, charged particles are trapped, increasing the particle fluence. For particles from photon conversions this increases the occupancy but has a negligible effect on the detectors, since electrons create very little displacement damage to the crystal lattice. For the charged hadrons, with the coil radius of 1.7 m and a B field of 2 Tesla, all particles with transverse momentum below 510 MeV will be trapped. The fluence increase depends on radius, does not vary greatly with z, and is typically a factor of 1.5 for the silicon. The fluence expected for a year of running at the standard SSC luminosity is shown in Fig. 19, as a function of the radial distance.

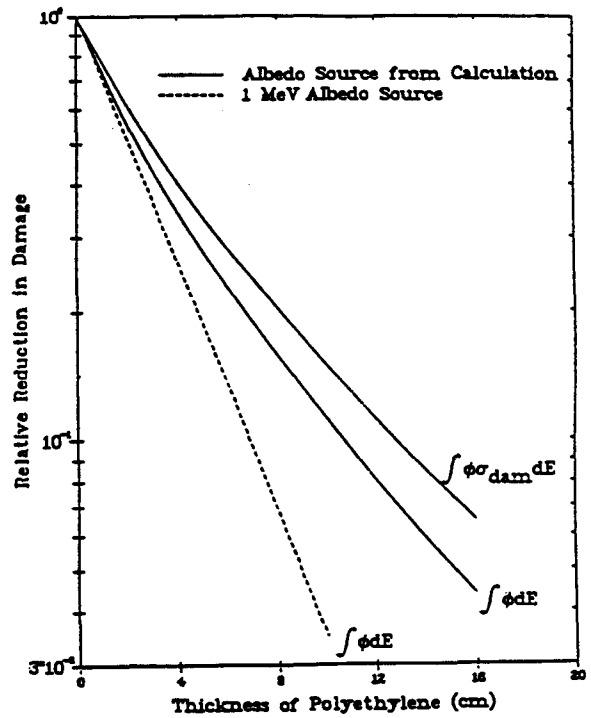


Fig. 17. Relative reduction in the damage as measured by the integral flux and integral flux times a damage function. Also shown is the integral flux, assuming the source is comprised of 1 MeV neutrons. (From Ref. 11.)

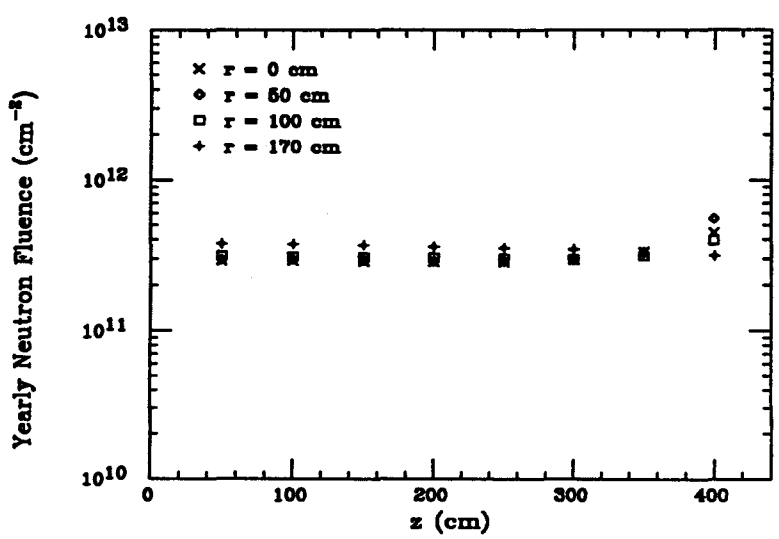


Fig. 18. Yearly neutron fluences in the SDC tracking volume with endcap calorimeters lined with 10 cm polyethelene at $L = 10^{33}$ ($\mathrm{cm}^{-2}\ \mathrm{sec}^{-1}$).

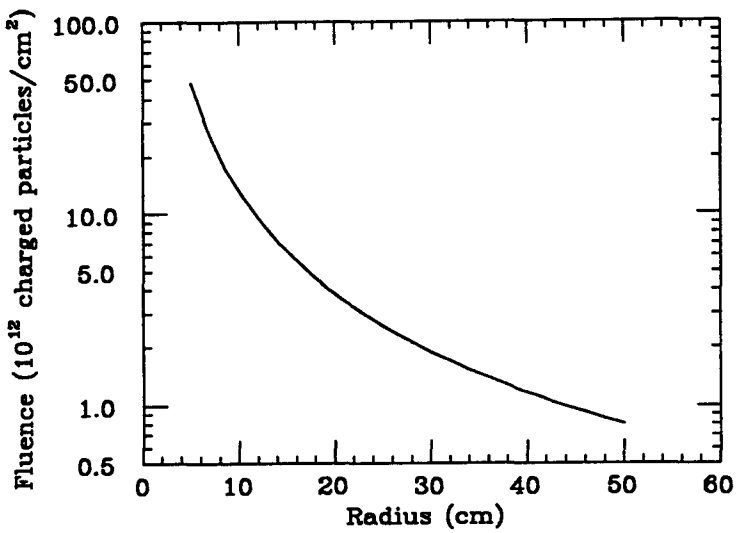


Fig. 19. Charged particle fluence vs. radius for one year at Standard Luminosity.

3. Lifetime for Proposed Detector

Table 6 shows the expected yearly fluence from charged hadrons at design luminosity for various radii. We ignore the effect of neutrons since their contribution ($3 \times 10^{11}/\text{cm}^2$) is expected to be very small, as discussed earlier.

Table 6. Yearly Fluence Versus Radius

Radius (cm)	Fluence Particles/cm^2	Number of Years to Reach $10^{14}/\text{cm}^2$
10	11×10^{12}	9
15	5.9×10^{12}	17
20	3.3×10^{12}	30
25	2.2×10^{12}	45
45	$.95 \times 10^{12}$	105

The detector lifetime is expected to be about 10^{14} particles/cm^2 for 1 MeV neutrons or 800 MeV energy protons as shown in section IV. For the particles at the SSC, mainly relativistic pions, the damage is on average a factor of two smaller. We take this factor as a safety margin on our calculations. We see from the table above, that our detector has 7 layers at all rapidities with lifetimes $\geq$ 10 years at Standard Luminosity. The inner most vertexing layer is the only one with an expected lifetime less than 10 years. All forward disks have a lifetime $\geq$ 17 years. The electronics on the forward disks never comes closer than about 27 cm to the beam.

4. Experience at High Fluences

Single-sided strip detectors have been used in experiments for about a decade and in the case of fixed target experiments have run successfully after large fluences. In such applications detectors have run with larger occupancies than planned at the SSC. In the case of the NA-32 experiment, the beam defining detectors accumulated a fluence of 6×10^{13} particles/cm^2 over three years [12]. The measured leakage current after this dosage is in very good agreement with expectations based on the discussion in section IV.A below. The detector capacitance remained very stable.

More recently, the Fermilab fixed target experiment E789 has begun to take data at very high rates. The system of strip detectors is performing well after a fluence of about 5×10^{13} particles/cm^2 accumulated over a time of a few months [13]. These detectors use electronics with $\sim$ 7 ns rise time and are therefore expected to be more sensitive to charge collection time than the SSC design. Tests of the detectors at LAMPF prior to the experiment indicated good performance up to fluences of 7×10^{13} protons/cm^2 at detector voltages compatible with those expected based on the data in section IV.A [14]. These tests stopped at 7×10^{13} protons/cm^2 because of the effect of leakage current on the preamplifier used.

Fixed target experiments have typically used remote electronics for which AC coupling and input protection is relatively easy. Beam spills into the detector have the effect of discharging the detector voltage into the electronics. We plan on carefully testing that the front-end electronics has sufficient input protection, so that this does not present a failure mode.

F. Upgrade Options

The silicon system outlined in this report is aimed at the first decade of operation at the SSC. The SSC program is, however, expected to be very long lived and upgrades of the present system emphasizing vertexing, pattern recognition, or momentum resolution are possible and may be desirable. The evolution of pixel detectors would allow further improvements in vertexing. For very high luminosity operation, the outer half of the silicon with several additional layers at larger radii would provide a very low occupancy system with good resolution. For radii larger than 50 cm the lifetime limit is larger than 100 years at design luminosity. In the situation where momentum resolution is of paramount importance, an extra layer of single-sided detectors at the outer radius of 1.7 m would allow a vertex constrained $\sigma_{P_\perp}/P_\perp^2 = 5\%$ (TeV^{-1}).

Although it is unclear what physics requirements will be like after an initial exploration of the SSC energy frontier, the intrinsic performance capabilities of the detectors allows for flexibility and various high performance future options.

III. Introduction to Physical Design

The previous sections have provided the conceptual framework and physics oriented goals of the silicon tracker project. To achieve these goals requires significant developments in the areas of radiation-hard detectors; fast, low-power, radiation-hard electronics; low-mass, highly-stable mechanical structures; and low-mass, highly-stable cooling structures. Much progress has been made in each of these areas as discussed below.

In addition, the detector elements have to be integrated into a whole structure. This is an area where we are just at the beginning. Primary emphasis so far has been on the design of the basic detector module, which has been chosen to be a 12 cm long detector, made by bonding together two 6 cm units. A plan for stiffening the unit by the addition of edge ribs should provide an adequate mechanical structure. A design for the local electronics, shielding, local cabling, and positioning relative to cooling structures is nearing completion. Basic measurements on cross-talk and noise for the chosen configuration still need to be done.

The detector subassemblies listed in Table 2 have been chosen to fit with the choice of a 12 cm long detector module. The central region barrel detector can be made of 5 detector units, each 12 cm long. The forward disks are generally made of either one or two 12 cm units and require the fabrication of eight detector types. For the disks the electronics is assumed to be at the outer periphery, where the pitch is approximately 50 μm. The position accuracy thus improves at radii smaller than the maximum for such a 12 cm disk module.

Figures 20a and b show the configuration of barrel detectors and the largest disk detector as fabricated using a 4 inch silicon wafer. The detectors have been arranged to lie within a 9 cm circle to optimize yield in fabrication. The barrel detectors are made two to a wafer, the disks one to a wafer. The barrel detectors have 5 chips per side for the readout, the disks 10 per side. Table 7 lists the number of 6 cm long detectors per layer, the number of readout channels per layer, the number of modules in ϕ per layer, and the detector overlap (to minimize dead areas) per layer. The details of the individual detectors are discussed in IV.D below.

Alignment goals for the full system have been defined, as discussed earlier. Initial plans for alignment and subassembly fabrication have focussed on the barrel configuration. These ideas should be tested and refined in the coming year.

We discuss below critical design goals and progress in the relevant technical areas: detectors, electronics, data acquisition, triggering, and mechanics and cooling. In general, in order to clarify why given choices were made, the discussion addresses the main design alternatives we have looked at.

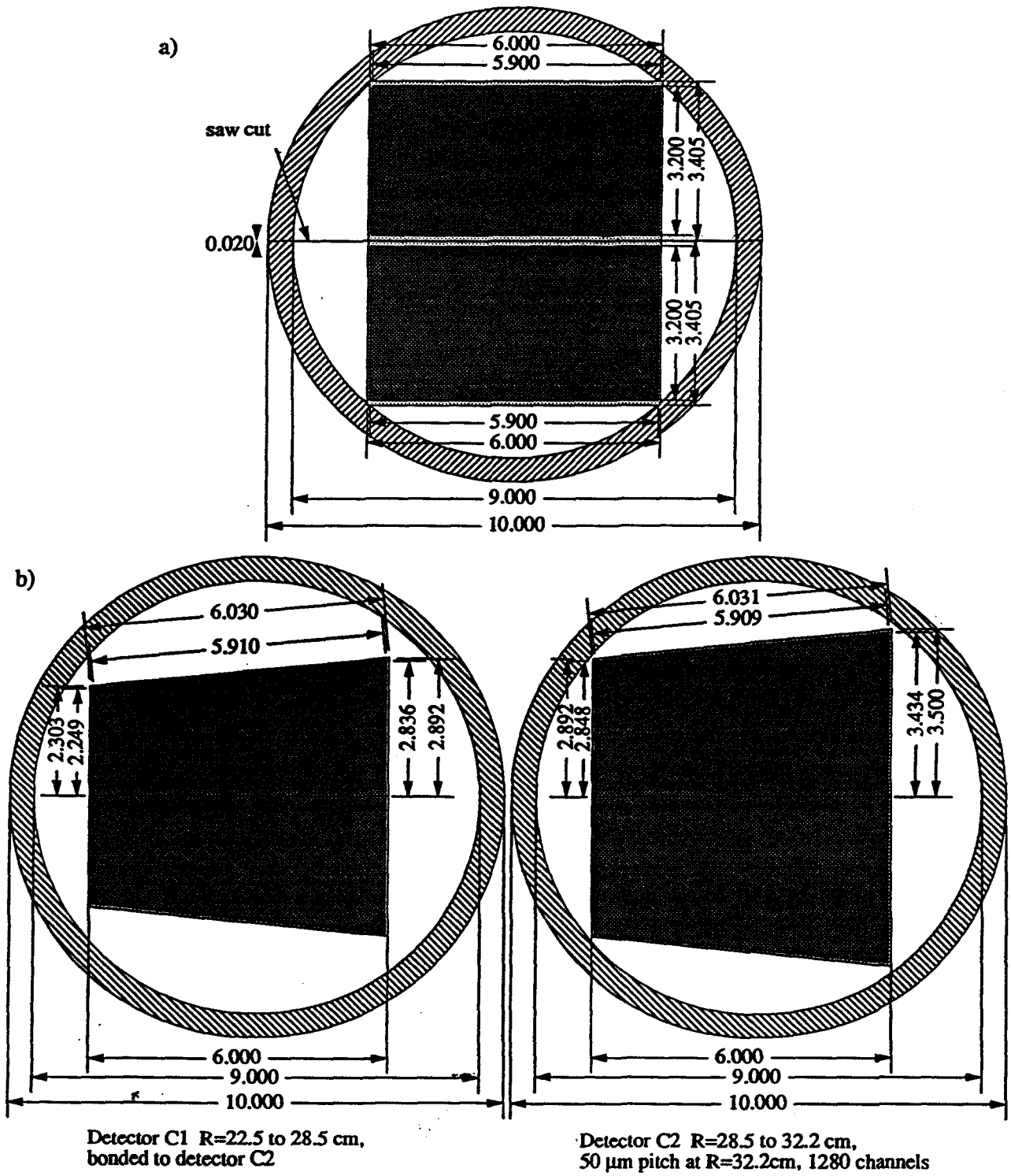


Fig. 20. a) Configuration of two barrel detectors made from one wafer; b) Geometry of largest disk detector as configured on a wafer. Also shown is detector bonded to it.

Table 7. Detector and channel count for the Silicon Tracking System

Barrel

Barrel #	Modules in ϕ	Active Overlap μm	6cm long Wafers in Layer	Electronic Channels
1	18	545.6	180	115200
2	24	429.4	240	153600
3	36	347.2	360	230400
4	42	329.8	420	268800
5	48	318.6	480	307200
6	54	310.9	540	345600
7	66	301.3	660	422400
8	72	298.2	720	460800
		Sum	**3600**	**2304000**

Disk

Disk #	Module A in 1 Disk (Active Overlap 806 μm)	Module B in 1 Disk (Active Overlap 837 μm)	Module C in 1 Disk (Active Overlap 775 μm)	Module D in 1 Disk (Active Overlap 740 μm)
1	26	38		
2	26	38		
3	26	38		
4	26	38		
5	26	38		
6	26	38		
7	26	38		
8	26	38		
9	26	38		
10			32	44
11			32*	44
12				44
13				44*
Electronic channels	1198080	1751040	327680	901120
		Channels Total, All Disks		**4177920**

* Module made of 6 cm units, instead of 12 cm. All others 12 cm.

IV. Status of Detectors and Detector Module

A. Radiation Hardness of Detectors

1. Increase in Leakage Current

The increase in leakage current ΔI under irradiation of a detector is a volume effect and a consequence of the displacement damage by hadrons. It is proportional to the fluence Φ

$$\Delta I = \alpha \cdot \Phi \cdot \text{Vol.}$$

The linear dependence has been verified up to large fluences (10^{15} cm^{-2})[15] and for a large range of fluxes[16]. It is important to note that we are interested in the value of the leakage current constant after annealing (more than a factor 2 reduction) because the fluxes used in the tests tend to be several orders of magnitude larger than those anticipated at the SSC.

In general one would expect high energy protons to have larger leakage current constants than high energy charged pions or 1 MeV neutrons [17]. The newest measurements give the following numbers, after annealing and at 20° C:

$$\alpha \approx 2 \cdot 10^{-17} \text{ A/cm for 1 MeV neutrons}$$
$$\alpha \approx 3 \cdot 10^{-17} \text{ A/cm for 800 MeV protons.}$$

The damage coefficient for typical pions at the SSC is expected to be a factor of two smaller than the value for protons above. Throughout the remainder of the text we will use $\alpha = 2 \times 10^{-17}$ A/cm as a good average for the various particle types, including annealing. The temperature dependence has been measured [15] to be proportional to $e^{-0.62(eV)/k_BT}$ over the temperature range of interest (–10°C to 25°C). For AC coupled detectors, the leakage current per se is not important if the biasing resistors are small, but the current fluctuations are an additional noise source. The biasing resistors will be of the order of 200 kΩ, leading to voltage differences of 0.2 V for a strip current I=1μA. The noise is

$$ENC = \sqrt{2eIF_i\tau} \text{ electrons}$$
$$= 500 \text{ electrons}$$

for a CR-RC shaper ($F_i = 0.924$) with time constant $\tau = 20$ ns and $I = 1$ μA. For the detector module chosen: 12 cm strip $\times$ 50 μm pitch $\times$ 300 μm thickness, using the average value of α above and assuming 0° C, the leakage current per strip at the limiting fluence of 10^{14} particles/cm^2 is about 0.7 μA.

2. Change in Depletion Voltage

As a consequence of the creation of charged damage sites in the bulk during irradiation with hadrons, the effective donor concentration N_D decreases during irradiation. This changes the depletion voltage:

$$V_{dep} = \frac{e \cdot |N_D| \cdot d^2}{2 \cdot \epsilon}$$

where d is the detector thickness and ϵ is the permitivity of the silicon. Note that this effect is independent of the strip length or pitch. Recently the effect has been shown [18] to consist of a two component process: donor removal and acceptor creation. The effective concentration is found to be

$$N_D = N_0 e^{-c\Phi} - \beta\Phi$$

with N_0 the initial doping concentration, and c and β experimentally determined parameters. Data for protons and neutrons are shown in Fig. 21a and b with the following measurements of c and β.

$$c = 8 \cdot 10^{-14}\ \mathrm{cm}^2,\ \beta = 0.015\ \mathrm{cm}^{-1} \text{ for 1 MeV neutrons,}$$
$$c = 5 \cdot 10^{-14}\ \mathrm{cm}^2,\ \beta = 0.03\ \mathrm{cm}^{-1} \text{ for 800 MeV protons.}$$

The consequences of this fluence dependence are:

Type inversion: at a fluence of between 1 and $2{\cdot}10^{13}$ cm^{-2} the n-type bulk inverts to p-type ($V_{dep} = 0$) and with increased irradiation, the depletion voltage increases again [18],

Universal behavior for large fluences: for large fluences the depletion voltage is independent of the initial doping concentration N_0, as shown in Fig. 21b) [19].

The annealing behavior is complicated: annealing to a depletion voltage characteristic of half the fluence within days is followed by a long term relaxation to somewhat beyond the point of initial damage [18].

3. Signal Collection

We can calculate the total time for signal collection either before or after type inversion in terms of the detector thickness d, the depletion voltage, detector voltage V_{tot}, and hole mobility which is $\mu = 450\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{sec}^{-1}$ at room temperature.

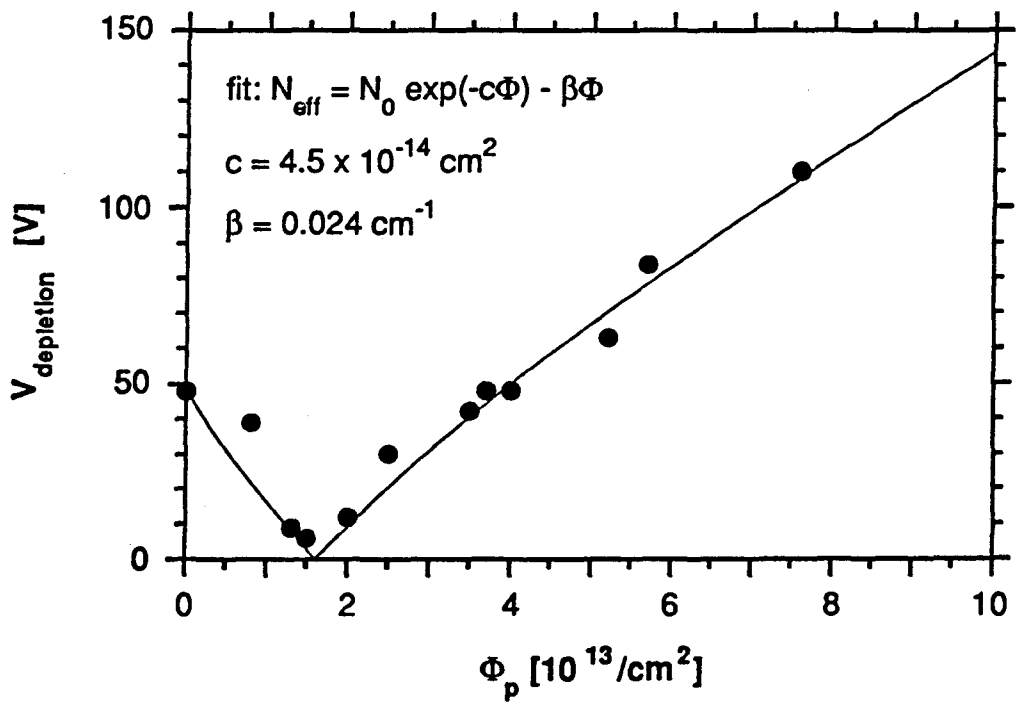


Fig. 21. a) Depletion voltage vs. proton fluence for SI detectors. Type inversion occurs at $\Phi = 1.5 \cdot 10^{13}/\text{cm}^2$. The proton energy was 800 MeV.

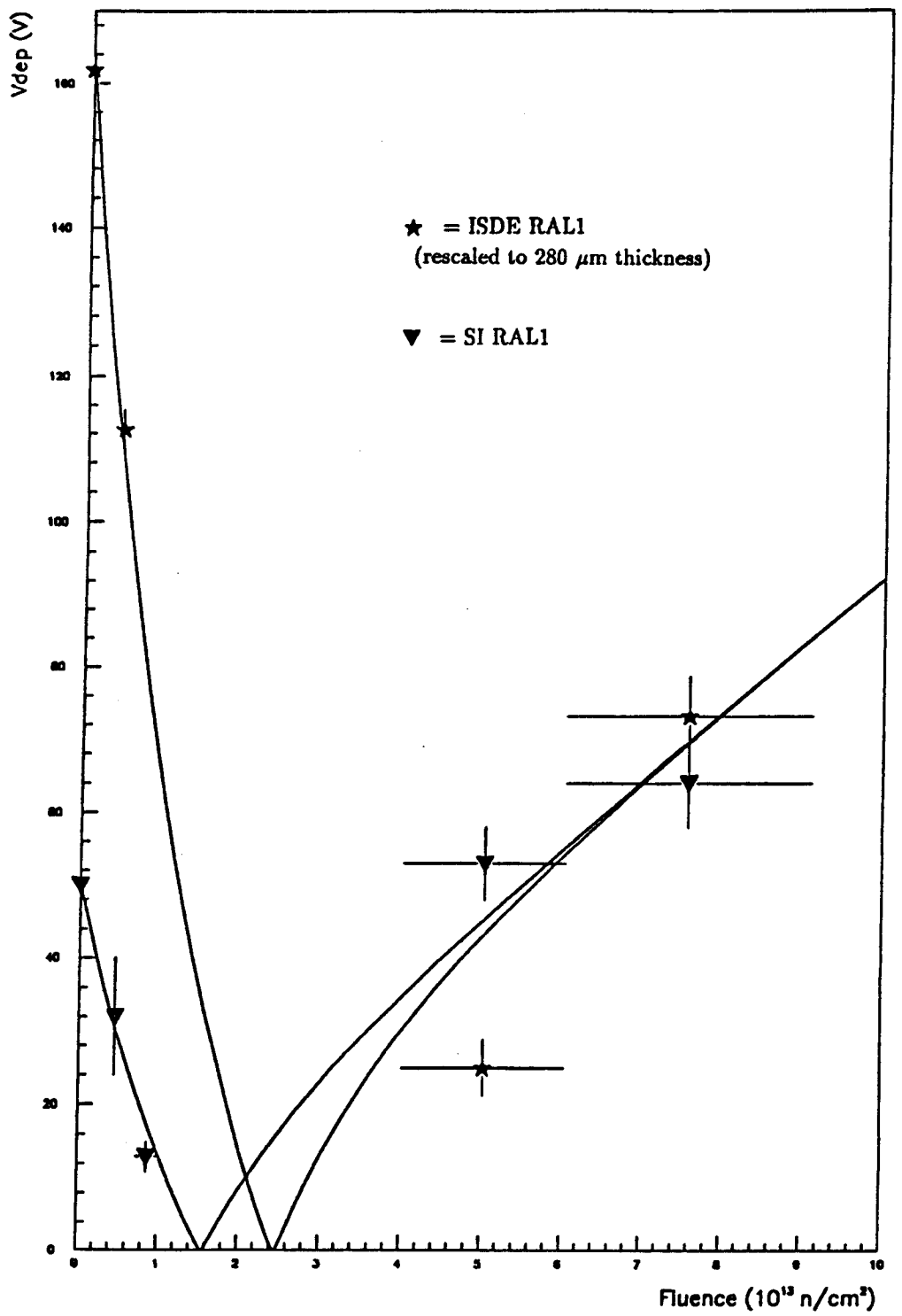


Fig. 21. (continued) b) Depletion voltage vs. neutron fluence for SI and ISDE detectors. The neutron energy was 1 MeV.

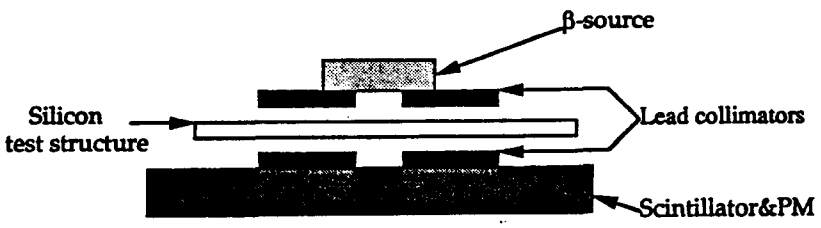


Fig. 22. Physical arrangement for measuring charge collection.

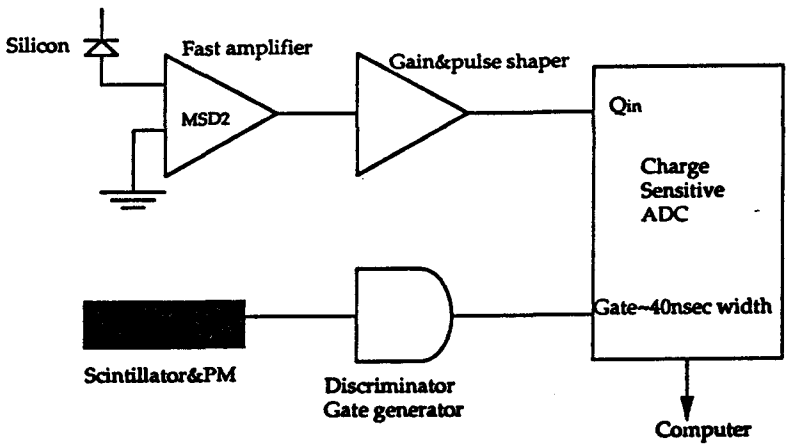


Fig. 23. Electronics setup for measuring charge collection.

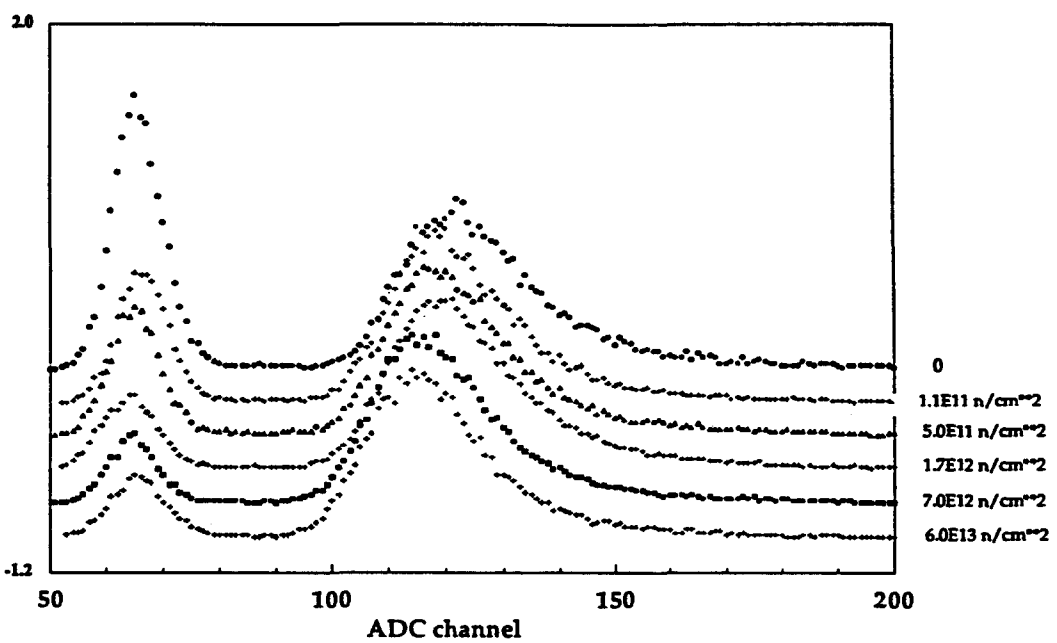


Fig. 24. Beta spectra from non-irradiated and irradiated detectors biased at 100 V.

Note that the electrons, which have a larger mobility, are collected much more quickly. The resulting total collection time is [20]:

$$t = \frac{d^2}{2\mu V_{dep}} \ln\left(\frac{V_{tot} + V_{dep}}{V_{tot} - V_{dep}}\right).$$

For a 50 V depletion voltage, we require 90 V to collect all of the charge in 25 nsec at room temperature. At the inversion point ($V_{dep} = 0$) this drops to 22 nsec if we leave the voltage at 90 V. For a 100 V depletion voltage, we require 118 V to collect all of the charge in 25 nsec. The latter would be typical of a detector which has been exposed to 10^{14} particles/cm^2 at the SSC. These collection times all decrease by 25% by running at 0°C, when we include the temperature dependence of μ which is proportional to $1/T^{2.4}$ [21].

We expect to run the detectors initially with a voltage of $\geq$ 90 V and $\geq$ 40 V beyond depletion (assumed to be 50 V). This implies, given the data in section IV.A, that we could run the detectors at a fixed voltage up to a fluence of 8×10^{13} particles/cm^2 if we assume the damage from the relativistic pions is typically half that of 800 MeV protons. Beyond this point we would have to raise the voltage.

4. Data on Fast Signal Collection in Silicon Detectors

As discussed above, a key issue regarding the radiation hardness of the silicon detectors is the charge collection speed after high doses. The gradual change in doping from n to p-type due to bulk damage from irradiation leads to changes in the electric field distribution which is expected to influence the overall charge collection time. We have examined some of the diodes which were irradiated with high fluences of neutrons using electronics comparable in speed with that expected to be used at the SSC.

4.1. Measurements

The method was to employ the standard technique of observing signals from minimum ionizing β electrons in a silicon diode. Figure 22 shows the arrangement. A square diode of 2 mm $\times$ 2 mm area was placed between a scintillator-phototube and a ^{106}Ru source. A lead collimator was placed between the silicon detector and the scintillator, and another above the detector, to raise the trigger efficiency and maximize the number of βs detected in the diode. The scintillator signal provided a fast trigger and generated a gate for a charge sensitive ADC so that the amplified signal from the silicon could be integrated. Figure 23 shows the overall arrangement.

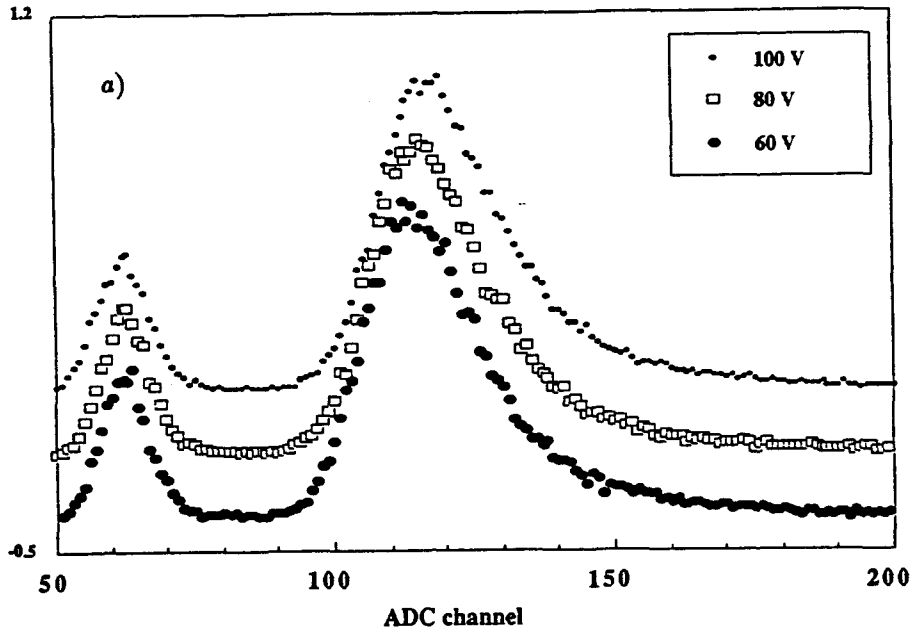
The influence of gate width on charge collection was examined. Prior to irradiation signal saturation occurred with gate widths greater than about 40 nsec with most probable charge deposited of $\sim 25,000$ electrons, calibrated using ionization by ^{241}Am x-rays. The data presented below were taken with a gate width of 42 nsec.

The diodes were irradiated at the ISIS facility at Rutherford Appleton Laboratory using neutrons with a similar energy spectrum to that expected at any hadron collider. Details of this and other aspects of the performance of the irradiated devices are given elsewhere [23].

4.2. Results

Typical spectra from detectors are shown in Fig. 24. The detectors are operated at 100 V which represents significant over-depletion for unirradiated detectors; prior to irradiation the full depletion voltages were in the range 30–65 V. A characteristic Landau-like distribution of signals was observed with a noise peak corresponding to false triggers from photons or βs which did not cross the diode. The alignment of the lead collimators, which were moved frequently to exchange detectors, had a marked effect on the trigger efficiency. The fraction of noise triggers thus varied from run to run due to geometric effects. However, no significant increase in the width of the noise peak was observed from irradiated detectors. Given the short shaping time, and the measured leakage currents, this was as expected.

The spectra show that the effect on charge collection with fast shaping electronics is not large; there may be some evidence for a gradual decrease in the charge collection efficiency at high fluence, but this is not marked. The most significant evidence for imperfect charge collection comes from comparison of data taken at different bias voltages (Figs. 25a and b) from detectors exposed to different doses. Although a clear reduction in collection efficiency is observed in the detector exposed to 6×10^{13} n/cm^{-2} when biased to 60 V, it appears to be almost fully restored when biased to 100 V. This correlates well with the depletion voltage curves in the previous section. These measurements give encouraging indications that the charge collection from a minimum ionizing particle continues to be fast even after high fluences of neutrons. These conclusions need to be sharpened using the final SSC electronics.



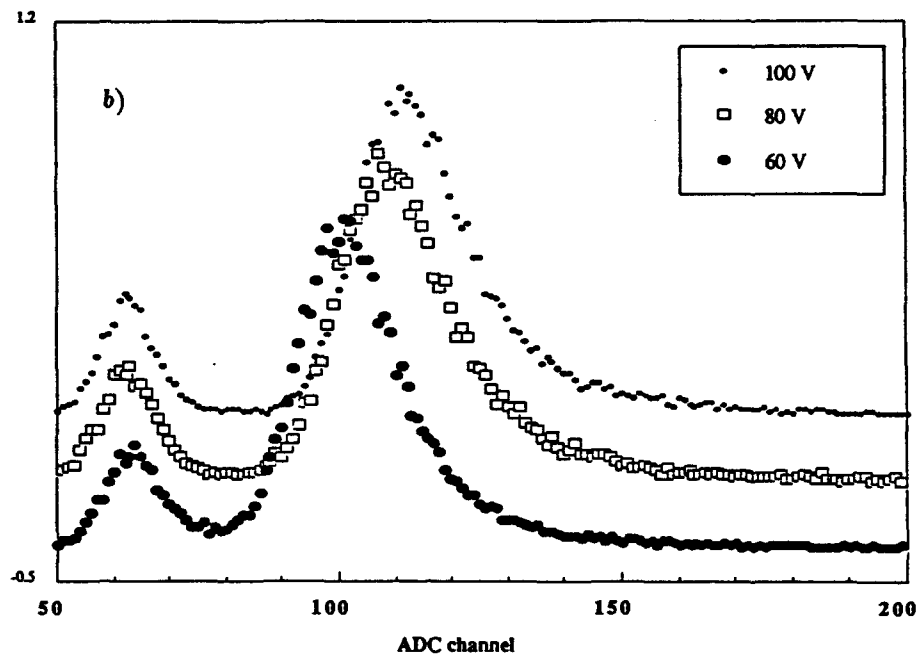


Fig. 25. Beta spectrum from irradiated diode. a) fluence = 1.7 10^{12} n/cm^2 b) fluence = 6.0 10^{13} n/cm^2.

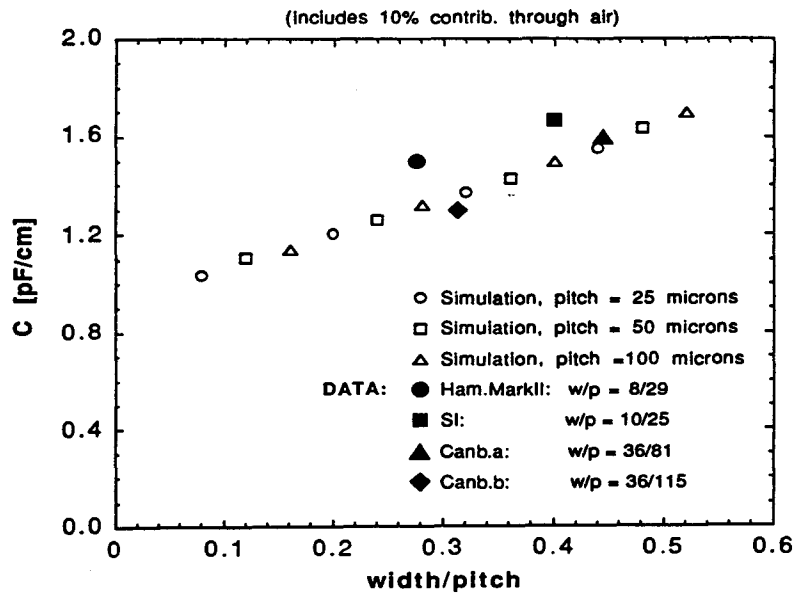


Fig. 26. Strip capacitance as a function of implant width/strip pitch.

B. Capacitance

The total capacitance of a strip is an important parameter for the design and performance of the frontend amplifier. It determines the signal-to-noise ratio of the front-end. The interstrip capacitance from one strip to its neighbors accounts for 80-90% of the total, while the rest is due to the back plane. The latter is shown to be stable during irradiation, provided the biasing voltage is kept above the changing depletion voltage (see Sec. IV.A.2 above). Our simulations [24] show that the interstrip capacitance is mainly a function of the ratio x = implant width/strip pitch and we have verified the simulation with measurements on single-sided p-type detectors (Fig. 26). We have specified an implant width of less than 10 μm which, at 50 μm pitch, results in a capacity of less than 1.2 pF/cm. For double-sided detectors, the n-side has the additional complication that the strips become shorted together by accumulated charges under the oxide unless prevented with either p-implants or with field plates over the n-strips. Potentially the capacitance can be quite high for these structures and we have to investigate the isolation schemes to make sure that our choice both minimizes the capacitance and is radiation resistant.

The effect of ionizing radiation on the interstrip capacitance is not known for the n-side and depends on the isolation scheme. On the p-side only preliminary data on non-optimized single-sided detectors exist. They show an increase in the interstrip capacitance of less than 30% after 2.2 Mrad. This measurement has to

be repeated with detectors which have the final geometry.

The specification of the n-side isolation and the evaluation of its radiation resistance will be the major subject of detector R&D in FY92.

C. Surface Damage Effects

The silicon strip detector has been developed by utilizing planar processing techniques for microelectronics. Its important functional structures, such as implanted fine strips, bias feeding and signal readout structures are implemented in a thin layer at the surface. At the surface of the silicon device there is also an SiO_2 layer for insulation. This layer traps positive charge when exposed to ionizing radiation. Therefore we have to investigate surface damage effects due to irradiation as well as bulk damage effects to develop a radiation-hard sensor.

Double-sided readout of the silicon sensor is essential to attain maximum information with a minimum material thickness. Our recent studies have accumulated good knowledge related to the surface structure of the double-sided strip sensor and its radiation hardness [25]. These studies have led to the conclusion that we can make a radiation-hard double-sided silicon strip sensor (DSSS) for the SDC.

The critical points for development of a robust DSSS are channel isolation, a bias feed method for each strip, and decoupling capacitor implementation. Several structures were proposed and have been tried [26] but any surface structure is potentially affected by bad isolation problems from the charge accumulation in the silicon dioxide surface layer. The problem is most severe for the isolation of the ohmic contact side.

1. Detector Structure

We have studied samples having two different methods for the bias feed and two different methods for channel isolation. The first sample had as a biasing method a punch-through gap on the junction side and an accumulation layer resistor on the ohmic contact side. The second had polycrystalline silicon resistors on both sides as bias resistors. The channel isolation methods on the ohmic contact side that have been studied are an implementation of p^+ blocking lines between n^+ strips and a field effect isolation using a potential applied to a MOS type electrode. All samples were fabricated at Hamamatsu Photonics Co using n-type 300 μm thick, 4 inch diameter wafers with resistivity 2–8 kΩ·cm. These wafers are most cost effective for mass production.

The quality of the silicon planar process at Hamamatsu Photonics was confirmed to be excellent by inspecting the surface and monitoring dark current of samples fabricated. No serious surface defects have been observed in 30 samples

of 1 cm^2 sensors. Dark current with full depletion was $\sim$ 5 nA/cm^2 for 300 μm thick single-sided detector and $\sim$ 10 nA/cm^2 for double-sided detectors. High quality samples were essential to evaluate the radiation damage effects on surface structures.

Both types of bias feeding and both types of channel isolation were perfectly functional before irradiation, showing small leakage current, stable depletion voltage, good breakdown margin for the bias potential and excellent channel isolation on both sides. Chip to chip uniformity was excellent, as needed for stable operation of a large scale detector, since a chip-to-chip adjustment of operating condition is almost impossible for such a large number of detectors.

2. Radiation Hardness of Bias Feeding Method

With an increase of radiation dose, different characteristics for the different methods mentioned above became clear [25]. Our experimental results show that polycrystalline Si resistors of several hundred kΩ for biasing both sides is a good choice because it is radiation hard [25,18] very stable and its resistivity is controllable during the production. The punch-through gap and the accumulation layer resistors for biasing were not hard enough for more than one Mrad proton irradiation.

3. Isolation of *p–n* Junction Side

Channel isolation on the *p–n* junction side of our samples was maintained up to 6 Mrad.

An explanation of the channel isolation mechanism after irradiation, for the *p–n* junction side is complicated by the simultaneous bulk type inversion [18,27] and positive charge accumulation in the SiO_2. Prior to irradiation, we don't need any special isolation structure implemented on the *p–n* junction side, since *p* strips in an *n*-type substrate can easily be isolated. However, after the *n*-type substrate inverts into *p*-type due to irradiation, this no longer works. This means naively that channel isolation will be lost after type inversion by irradiation, while real detectors actually still maintain good isolation even with rather low bias voltage applied as shown in Fig. 27. What we have measured is the bias voltage dependence of inter-strip resistance as a function of irradiation dose by 65 MeV proton. An ideal isolation ends up with the resistance value twice the biasing resistor. The *n*-type substrate inverts to *p*-type between 1 Mrad and 2 Mrad dose in this case. The bulk type inversion has been confirmed by pulse height measurements using infrared injected pulses. The reason why the isolation is maintained after significant irradiation can be explained by the effects of the positive charge accumulated inside the SiO_2. The positive charge attracts electrons in the region facing the SiO_2.

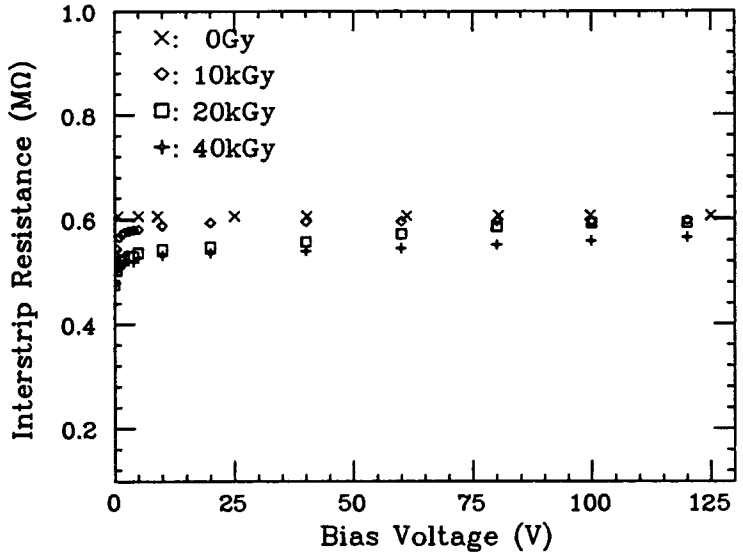


Fig. 27. Interstrip resistance vs. bias voltage p–n junction-side.

These electrons keep the surface n-type between adjacent p-strips, resulting in good isolation.

4. Isolation of Ohmic-contact Side

We have tested two different isolation methods. The first one was a MOS type electrode implemented between n^+ strips. We confirmed that the potential needed to isolate adjacent strips increases steeply with ionization irradiation, in order to compensate the effect of positive charge accumulated in the SiO_2 layer sitting between the isolation electrode and detector substrate. The thickness of the SiO_2 layer was 2000 Å and the charge density accumulated was estimated to be $1 \times 10^{12}/cm^2$ [28]. To compensate this charge and attain good isolation, a potential of more than 20 V on the MOS isolation electrode was needed with 1 Mrad dose [28]. This is significant in comparison with the full depletion voltage of 70 V. We conclude that the MOS type isolation electrode is not favored for use in a high radiation environment.

The second isolation method was an implementation of p^+ blocking lines between adjacent n^+ strips. Two different concentrations of boron implanted for the p^+ blocking line were tested. A low concentration sample was implanted with $\sim 5 \times 10^{12}$ borons/cm^2 and a high concentration one with $\sim 1 \times 10^{14}$ borons/cm^2. Both samples had excellent isolation characteristics before irradiation. As the radiation dose is increased, the low concentration sample shows degradation of the channel isolation, while the high concentration one keeps its excellent isolation characteristics up to 4 Mrad [25] as shown in Fig. 28a, b, respectively. When the positive charge density inside the SiO_2 approaches the density of the boron in the p^+ blocking line, electrons in the silicon are attracted by the positive SiO_2 charge

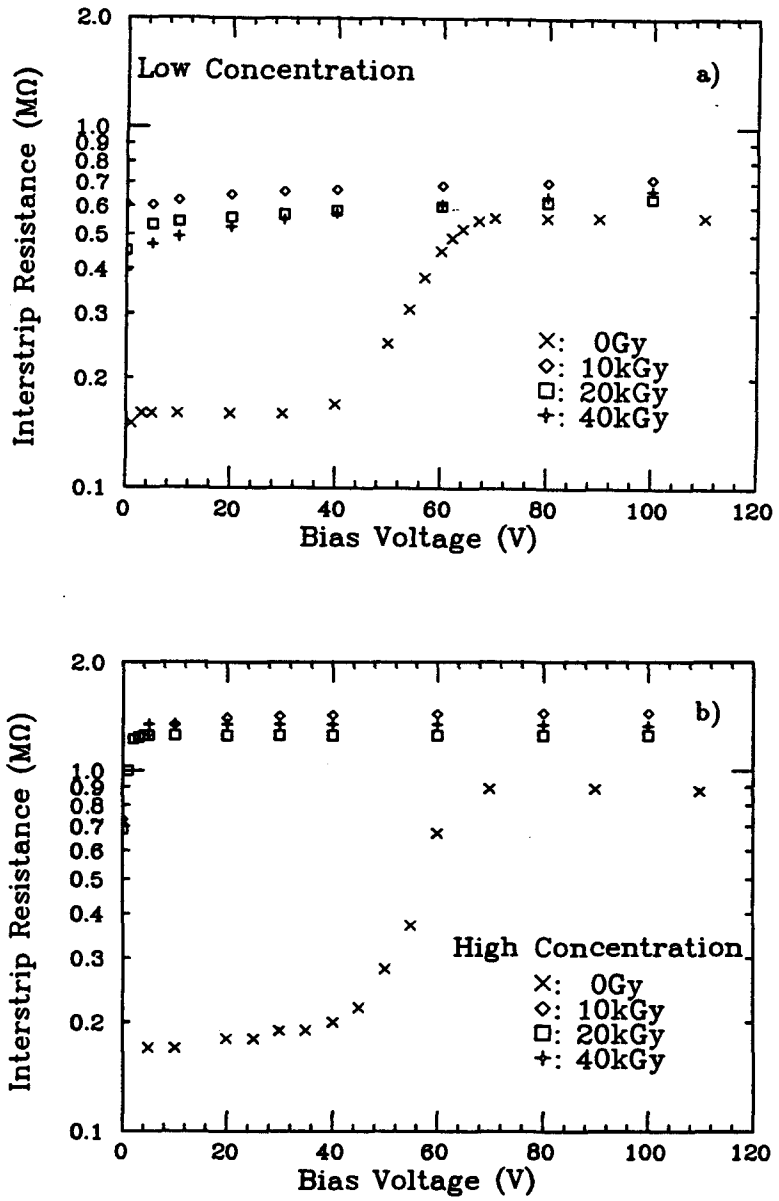


Fig. 28. Interstrip resistance vs. bias voltage for the ohmic contact side of the detector, a) for low doping concentration of *p* isolation strips and b) for high doping concentration.

degrading the performance of the p^+ blocking channel. Fortunately, the positive charge accumulation saturates at $\sim 10^{12} e/cm^2$, where e is the electron charge. Therefore the high concentration implant maintains its functionality. Note, even after inversion p^+ blocking lines are needed to maintain isolation, because the electrons attracted by the positive charge in the SiO_2 maintain a thin surface of n-type silicon between the n-strips. Our radiation tests therefore favor the channel isolation method of inserting p^+ blocking lines between n^+ strips on the ohmic contact side.

5. Decoupling Capacitor

The decoupling capacitor was formed with a readout electrode above the SiO_2 layer and implanted strips underneath. With 0.2 μm thickness of SiO_2 a breakdown voltage across the insulator should be more than 100 V but less than 200 V. We observed in some samples that the high potential difference (more than 50 V) between strip and readout electrode degraded the breakdown margin of the junction because of the high field at the strip edge. The charge accumulation by irradiation increases the electric field at the edge and can further degrade the breakdown margin. A careful design study of the edge structure will be undertaken to solve this discharge problem. One specific detector sample did not breakdown with more than 100 V of potential difference.

In conclusion, we confirmed that the DSSS fabricated at Hamamatsu Photonics that had polycrystalline silicon resistors for biasing on both side and the p^+ blocking lines for n-side isolation were radiation hard and kept their functionality up to 4 Mrad of proton irradiation.

D. The Basic SDC Silicon Detector and Performance Optimization

1. Strip Detector

The SDC silicon detector unit has been chosen to have dimensions to minimize overall fabrication costs, and with structures to optimize radiation hardness at the lowest capacitance. The basic wafer units are then bonded together to achieve a ladder of maximum length consistent with signal-to-noise requirements. This results in 6 cm long wafers and 12 cm long ladders. We summarize in Table 8 the specifications for the individual SDC double-sided silicon detectors, for the barrel geometry. The disk detectors are rather similar except that they are about twice as wide. Table 9 lists the dimensions of the active area of the various disk modules and the pitch on the inside and outside.

Figures 29 and 30 show the pattern of structures for each side of a barrel detector. Figure 31 shows a detail, with dimensions, of the readout structures.

Table 8. Specifications of Double-sided Silicon Strip Detector (Barrel Part)

1) Substrate
   - Type: n-type
   - Resistivity: 4–8 kΩ·cm
   - Thickness: 300 ± 10 μm
2) Size
   - Overall dimension: 60 mm × 34.1 mm
   - Effective area: 58.8 mm × 32.0 mm
   - Dead area: 600 μm from edge
3) Strip
   - Pitch: 50 μm on both surfaces
   - Strip isolation of ohmic side: p^+ blocking line method
   - Pattern accuracy
     - Position: ±1 μm
     - Size: ±1 μm
     - Relative position of both sides: ≤ 5 μm
4) Bias Resistor
   - Poly-crystalline silicon line on both surfaces
   - Resistance value: 250 ± 50 kΩ
5) Electric properties
   - Initial leakage current: ≤ 1 μA (overall); ≤ 100 nA/channel
   - Bias voltage tolerance: ≤ 150 V
   - Decoupling capacitance of strip
     - Breakdown voltage: ≤ 100 V
     - Capacitance: ≥ 30 pF/cm
   - Readout capacitance: ≤ 1.2 pF/cm (junction side); ≤ 1.4 pF/cm (ohmic side)
6) Fiducial mark for integration
   - (Pattern and position are defined in Fig. 30.)
   - Position accuracy relative to strips: ± 1 μm
7) Dicing
   - Full cutting by diamond saw
   - Cutting zone: ± 30 μm

Table 9. Dimensions for Various Disk Modules

Detector Type	Active Width at R Out (cm)	Pitch In (μm)	Pitch Out (μm)
A	6.64	28.68	51.63
B	6.55	35.34	51.05
C	6.87	34.94	53.57
D	6.73	38.94	52.48

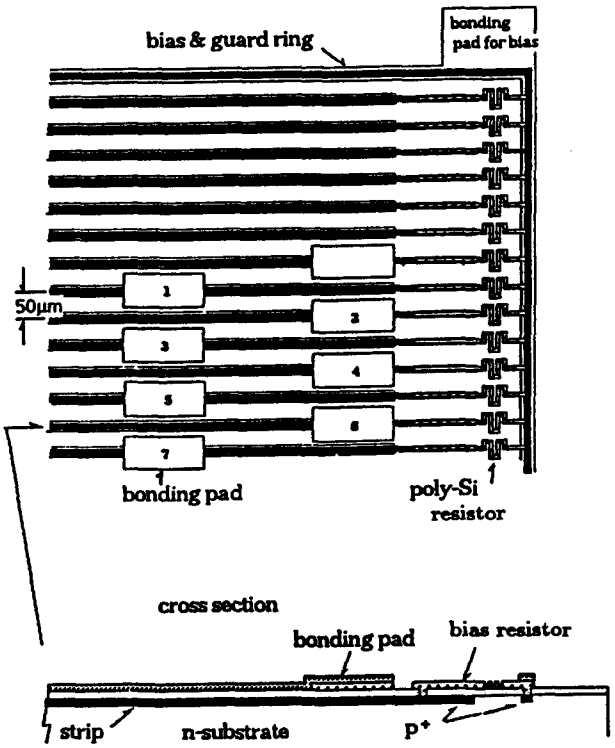


Fig. 29. Axial strip side structure.

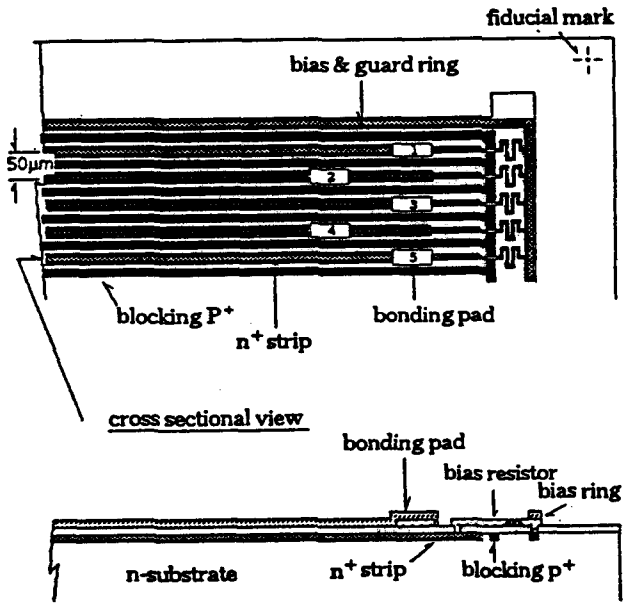


Fig. 30. Structure of stereo strip side (ohmic contact side).

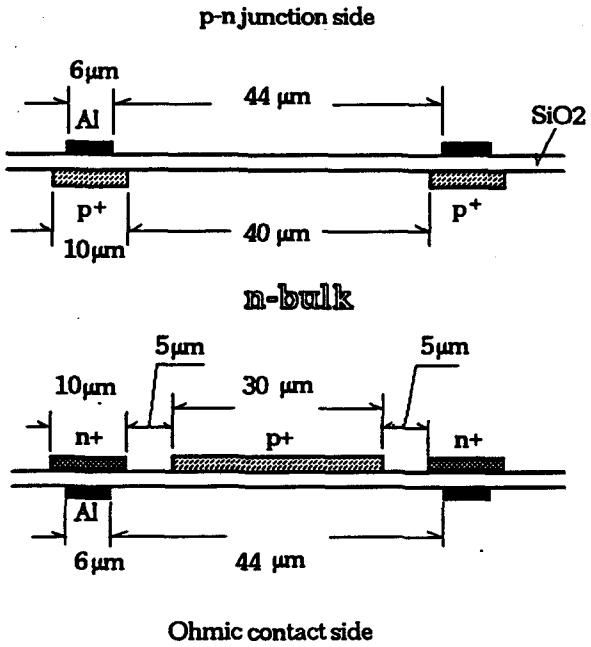


Fig. 31. Detailed structure of both surfaces.

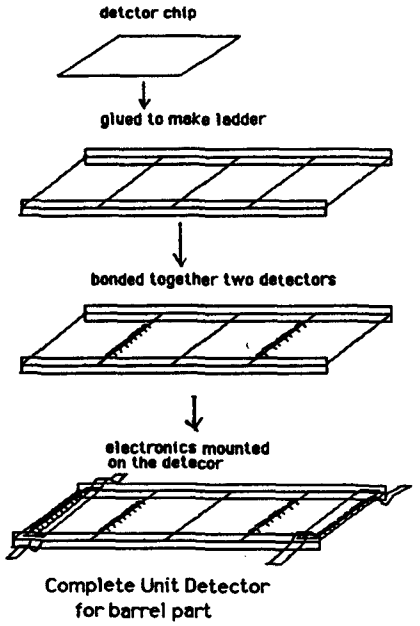


Fig. 32. Detector Module Construction

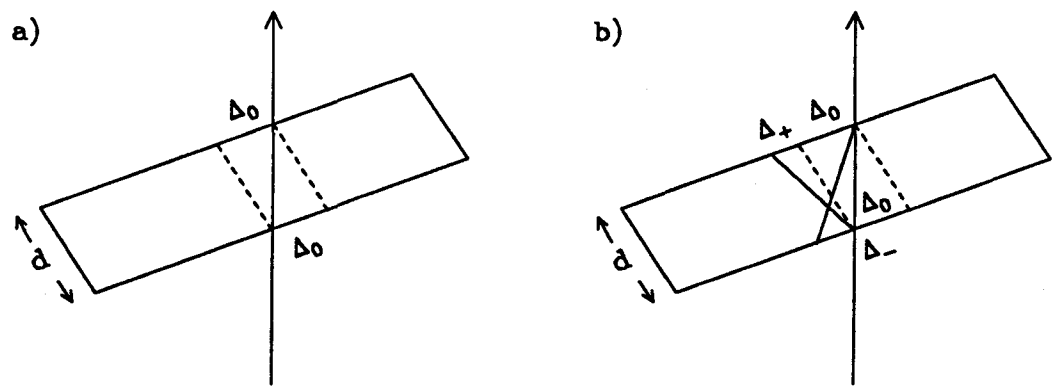


Fig. 33. Charge collection – tilted detector, a) no B field, b) with B field. Edge-on view.

These dimensions are not yet final, but should be finalized later this year after completion of capacitance and radiation measurements. Figure 32 shows the steps in constructing a detector module from the individual detectors. This involves gluing detector units together into a mechanical unit, stiffened by edge strips. The readout units are then bonded together, with electronics and cables at the ends.

2. Tilting of Barrel Detectors

The SDC barrel detectors have their charge collection significantly affected by the magnetic field. To minimize this the detectors need to be tilted around an axis given by the B field.

Figure 33a shows a tilted detector, of thickness d, in the absence of a B field. We assume holes are collected at the top, electrons at the bottom. The collected charges lie in swaths of width Δ_0 as shown in the figure for the passage of a high transverse momentum particle.

With a B field the drifting particles experience an extra force given by the (charge) $\vec{v} \times \vec{B}$. For both holes and electrons, the direction of the force is the same since both the charge and velocity change sign when going from holes to electrons. With the B field present, the charges are collected in swaths (solid lines) shown in Fig. 33b. The tilt angle has been chosen relative to the B field so that Δ_+ adds to Δ_0 and Δ_- subtracts from Δ_0. Note Δ_- is much larger than Δ_+. The swath for the collected holes and electrons is now $\Delta_+ + \Delta_0$ and $\Delta_- - \Delta_0$, respectively. Equating these two gives a value of

$$\Delta_0 = \frac{\Delta_- - \Delta_+}{2}.$$

Here, $\Delta_- = \mu_B^- Bd$, $\Delta_+ = \mu_B^+ Bd$ and μ_B^-, μ_B^+ are the respective Hall mobilities. For these values, both swaths have a width $\Delta = (\Delta_+ + \Delta_-)/2$. The tilt angle of

the detectors is given by $\tan\theta = (\mu_B^- - \mu_B^+)B/2$. Our best estimate [20,29] at present, for room temperature, is

$$\mu_B^- = 1350\text{cm}^2\text{V}^{-1}\text{sec}^{-1} \quad \mu_B^+ = 310\text{cm}^2\text{V}^{-1}\text{sec}^{-1},$$

giving $\Delta = 50$ μm and $\theta = 6°$. These numbers have an uncertainty which is about 25%. This includes uncertainty from the temperature dependence which needs to be measured. We assume in our design that the Hall mobilities will increase at lower temperature and have chosen a tilt angle of 7.4° for the baseline design. Given the value of Δ, we expect to get typically one or two strips with signals above threshold. For both cases we will have to measure and calibrate the associated mean position and error. Note, the signal arrival time for the swath of charge varies with position relative to the strip centers, which affects how often we get one or two strips with signals above thresholds and in the correct time bucket. An optimum resolution would be gotten by setting the discrimination threshold to give 1/2 single hits and 1/2 double hits, providing an ideal resolution of 7 μm for each side of the detector.

3. Calibration

In this section we discuss calibration of the detector and readout electronics. The electronics design is discussed in section V below. We focus here on the two main problems of calibration in the SDC silicon tracker:

(i) Setting the comparator threshold voltage and

(ii) Determining the detector full depletion voltage.

In setting the threshold voltage (v_T) for the comparator we must take into account the amplifier noise, the amplifier gain (i.e. the size of a signal from a minimum ionizing particle), the required time resolution, the maximum allowable noise hit rate and the required hit efficiency per plane. In addition, other effects must be considered such as channel-to-channel and chip-to-chip variations in the comparator response (due to gain variations, radiation-induced changes in transistor characteristics, etc.) and the effect of detector noise increases due to radiation damage. A procedure for calibrating the amplifier-comparator can be described with reference to Fig. 34.

A test pulse voltage is injected into the calibration line of the amplifier-comparator chip which injects a known charge into every channel. The test pulse can be adjusted to give a signal equal to that deposited by a minimum ionizing particle. For a 300 μm thick detector this is equivalent to $\approx 25,000$ electrons. The comparator threshold is then varied and the count rate is measured using the digital data storage and data acquisition system. Figure 35 shows the result of such a

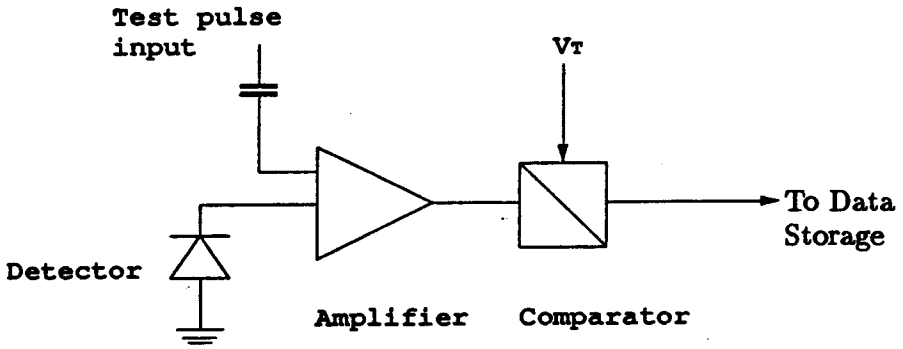


Fig. 34. Block diagram of one channel of the silicon readout electronics.

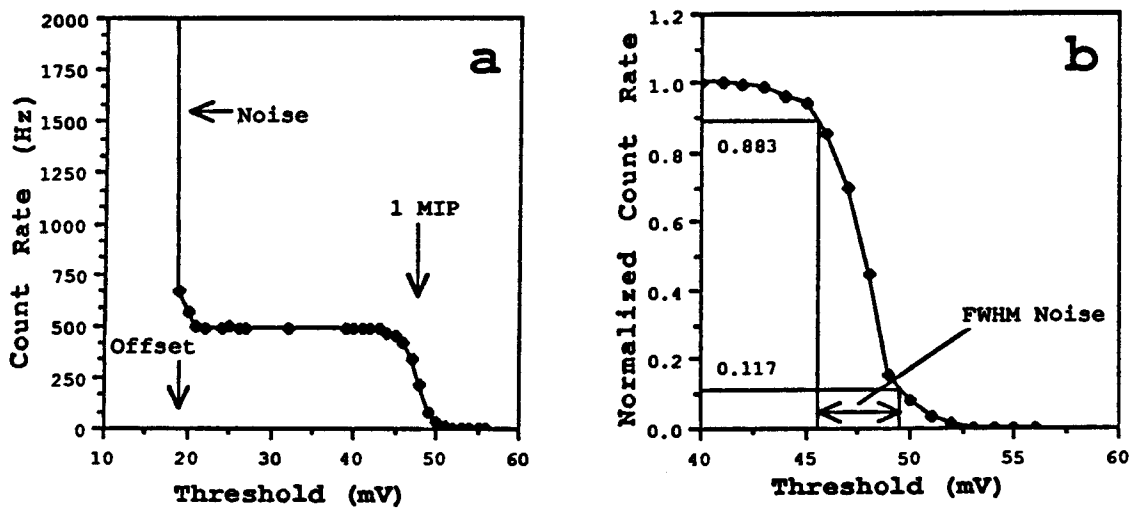


Fig. 35. (a) Count rate as a function of discriminator threshold. (b) Normalized count rate vs. v_T plotted in the range 40–60 mV. The 1 m.i.p. test pulse produces a pulse with a peak at 48 mV.

measurement made with a set-up consisting of a charge-sensitive preamplifier, a CR-RC shaper and a discriminator.

The curve in Fig. 35a has three regions of interest: (i) at low thresholds the discriminator triggers on noise, leading to a very high count rate; (ii) in the plateau region v_T is well above the noise and the count rate is equal to the test pulse rate (500 Hz); (iii) when v_T is close to the 1 m.i.p. level the count rate falls off rapidly. From (i) we get the dc offset at the input to the comparator and using (iii) we get a calibration of the gain of the system. In principle, we can also determine the amplifier noise from (iii). Assuming the noise is Gaussian we can read off the FWHM noise from the curve as shown in Fig. 35b. In this case the noise FWHM

is 4 mV. Since the dc offset is at 19 mV and the 1 m.i.p. test pulse is at 48 mV then the r.m.s. noise can be shown to be equivalent to 1,470 electrons, giving a signal-to-noise ratio of 17. A suitable threshold could be set at about 30 mV ($\equiv 1/3$ m.i.p.) – low enough so that the noise trigger rate is negligible and high enough to obtain an efficiency close to 100%, even when the effects of charge sharing and Landau fluctuations are taken into account.

Further work is needed to fully evaluate this calibration procedure. Future work will concentrate on measurements of the kind described above using a prototype amplifier-comparator chip which is due to be fabricated in bipolar technology in early 1992. This will allow studies of uniformity of the threshold across single chips and chips from different wafers. Threshold scans will also be carried out using minimum ionizing particle signals from a microstrip detector bonded to the input of the amplifier-comparator chip. This will help elucidate the effects of charge sharing and Landau fluctuations.

The determination of the depletion voltage of the silicon detectors for doses well beyond 2×10^{13} particles/cm^2, will be necessary during SDC operation. Two principal calibration methods will be studied this coming year:

(1) Measurement of the pulse height of particles in the detectors as a function of bias voltage. The pulse height of a particle traversing a silicon detector at normal incidence is proportional to the depletion layer thickness. Therefore the expected behavior is a rise in the pulse height as the bias voltage is increased and a saturation of the pulse height at voltages above V_{dep} when the detector is fully depleted. We will initially use standard readout electronics to evaluate this method and then carry out tests using the amplifier-comparator chip.

Since the pulse height is not directly measurable, an average pulse height will be obtained by using the threshold scan technique described above (and illustrated in Fig. 35a).

(2) Measurement of the pulse height from a 820 nm wavelength light spot as a function of bias voltage. The light spot would be focussed on the p-side of the detector, as we are mainly interested in the case where the detector has already gone through inversion. Since photons of wavelength 820 nm have a mean free path of $\sim$ 30 μm in silicon a very small pulse height will be seen at low bias. This is because the photons liberate electron-hole pairs within $\sim$ 30 μm of the silicon surface in an undepleted field-free region of the detector. When the voltage gets near V_{dep} the pulse height rapidly increases, and then saturates. Tests of this technique will be carried out in parallel with method (1). The effects of radiation damage on both methods will be evaluated by comparing results from non-irradiated detectors and detectors irradiated with charged particle fluences up to $\sim 10^{14}$cm^{-2}.

E. Detector Modules and Cabling

1. Introduction

Integration of the detectors, readout ICs and connecting cables is a critical area where definitive results are not yet available. Although a substantial body of semi-quantitative work has established guidelines for the electronic and mechanical design, very careful and detailed measurements are necessary to verify crucial aspects of the concept. The following discussion outlines our current design approach, which has resulted from several iterations of interacting electronic and mechanical designs. We are now focussing on a set of critical measurements to verify the design concept. This work is a top priority.

2. General Layout

2.1 Mechanical Layout

Detectors and their associated readout electronics are combined in individually testable modules. A module is an integrated mechanical unit consisting of a set of detectors, the associated readout ICs, and a connection cable. In the barrel, for example, a typical module is a 12 cm long detector array with 2×640 strips, 2×5 sets of readout ICs, and integrated interconnect substrates and cables. Critical issues are cross-talk from the readout chips to the detector and reduction of added material to a small fraction of the detector silicon.

We are investigating techniques that minimize material associated with mounting and connecting the readout ICs. The baseline design utilizes aluminum/Kapton ribbon cables as substrates for the readout chips; this assembly (including an intermediate Be shield and insulator sandwich) is mounted directly on the detector with a minimum of additional mass. A conceptual module layout is shown in Fig. 36. A cross section of the IC-detector sandwich is shown in Fig. 37. Note that the Be shield also serves the important function of providing a thermal path from the readout ICs to the cooling ring. This reduces the heat path through the silicon to the area subtending the cooling ring. Since about 85% of the detector extends beyond the cooling ring away from the readout, heating of the detector is minimized. Thermal analysis shows that the detector temperature is increased by only about 3° C above the cooling ring temperature of 0° C on the end near the heat source. The maximum mechanical deflection due to heating by the readout ICs is $< 2\ \mu$m.

2.2 Electronics and Bussing

Since the Silicon Tracker has several million channels of electronics, efficient on-chip data sparsification is crucial. With only a hit/no-hit indication one is essentially "flying blind" with respect to signal diagnostics. Hence, reliable control of

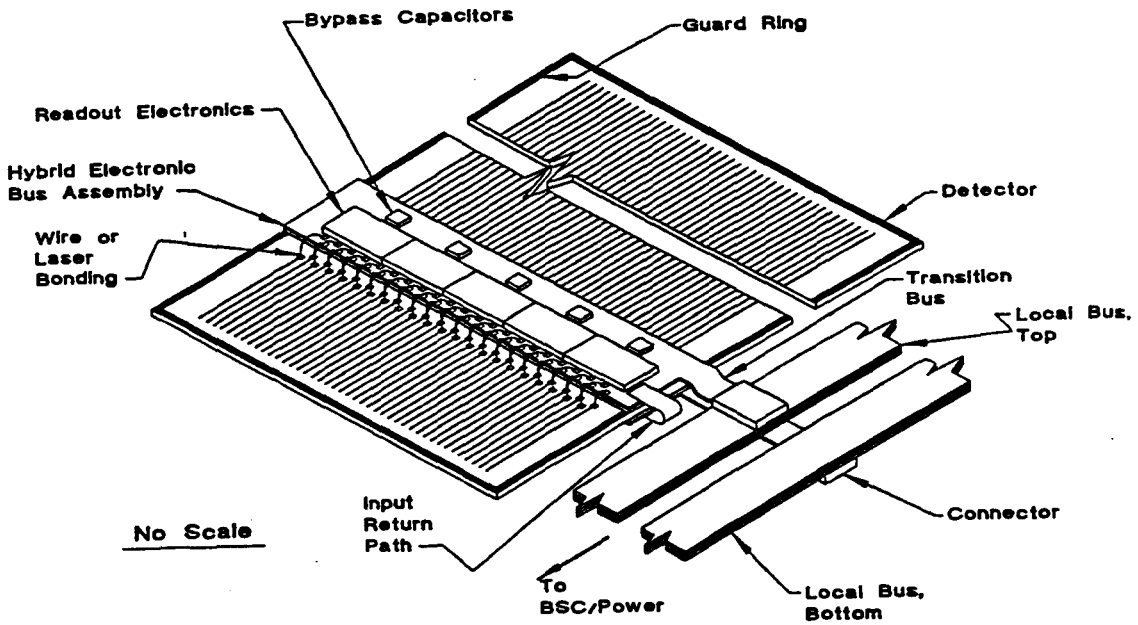


Fig. 36. Conceptual layout of a detector module.

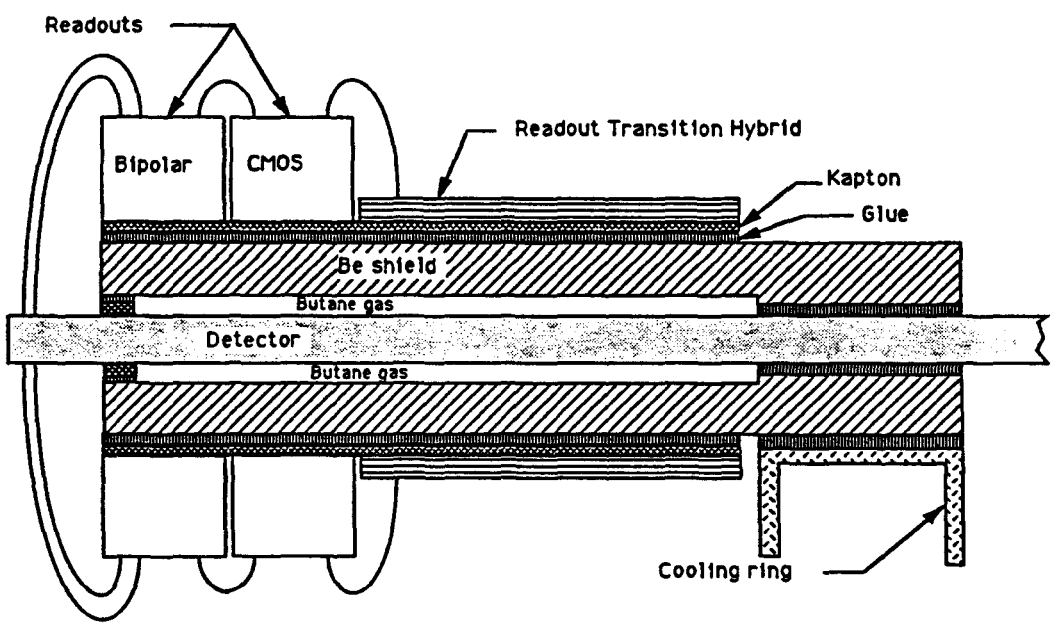


Fig. 37. Cross section through a detector module.

cross-talk and any other causes of spurious hits is of extreme importance. Specifically, coupling from the digital circuitry on the readout ICs to the detector is a serious concern. Measurements are being set up using existing ICs designed for readout of short-strip detectors at the SSC. Furthermore cross-coupling between cables and from signal cables to the detector is critical. Cross-talk from cables can be reduced by proper selection of the front-end shaping time constants, to reduce electronics response to the spectral distribution of bus activity (especially high-frequency clocks). Differential lines are required to reduce coupling from the cable to the input amplifiers through the detector strips. For local bussing the signal levels on these lines can be kept small; just how small must be determined by careful analysis and experiments.

Decoupling capacitors are an additional significant contribution to mass (constituents being Ag, Sn, Pb, Ba, Ta, etc.); circuit and bus designs are under investigation to minimize the number and size of capacitors, or possibly eliminate them altogether. This is being addressed at two levels:

1. Circuit Design
The analog circuitry is specifically designed for noise immunity and small transient currents. The comparator threshold voltage is brought in differentially. Signal transmission in the front-end chain from the analog IC to the digital IC is by a localized loop that allows separation of the analog and digital grounds.

2. Power Bus Design
All power supply lines are configured as low-impedance transmission lines to present a low-impedance return path over a wide frequency range. The power bussing is subdivided to isolate sensitive circuit blocks. The detector bias supply lines are isolated from IC supply lines (the on-chip referencing preserves common-mode rejection). Analog and digital supply lines (and grounds!) are segregated.

Fig. 38 shows the local connection scheme for a pair of readout ICs connected to opposite faces of a double-sided detector. Since the input signal current loop includes electronic channels on both sides of the detector, the connections must be arranged carefully to preclude pickup through common signal paths (especially from the digital circuitry). The configuration shown in Fig. 38 supplies the detector bias voltage differentially; the voltage is referenced to the readout ICs by a high-resistance divider. The analog IC is connected to the digital circuitry through a local signal loop, which has only one connection per channel and a single return per chip (two connections per channel are prohibitive because the channels are effectively on a 50 μm pitch). This local loop uses special drivers and receivers to establish a high impedance between the analog and digital circuitry. The overall arrangement provides a well-controlled input signal path and, by isolating the

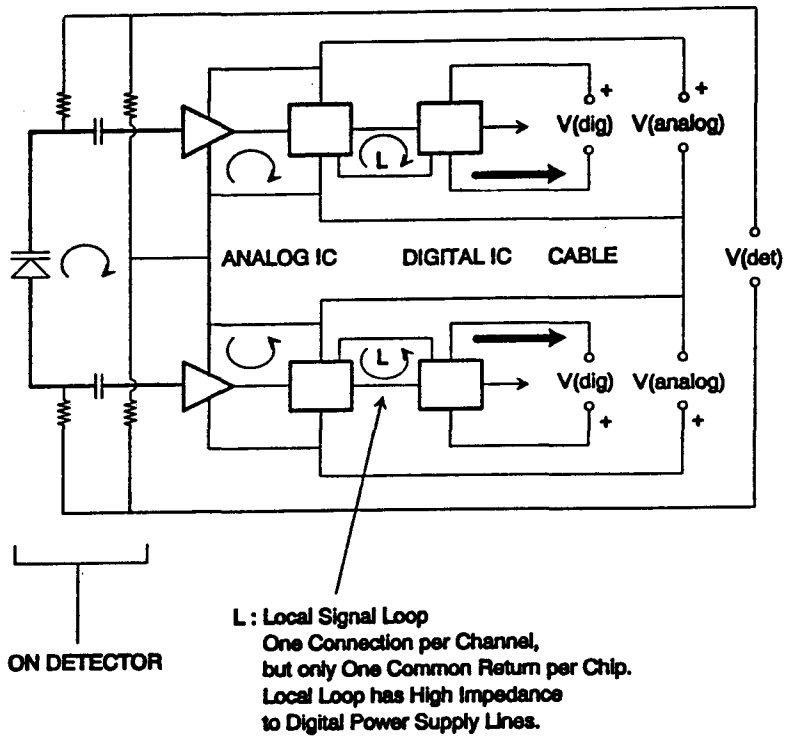
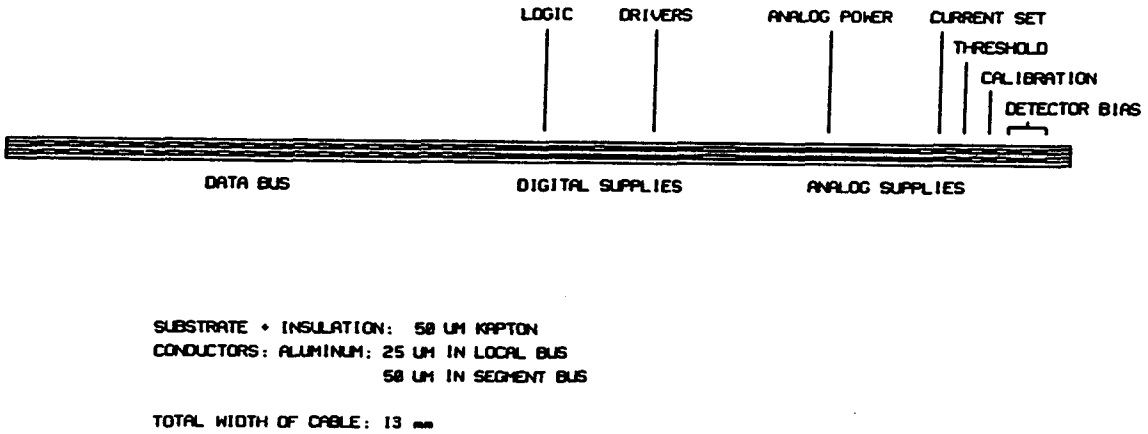


Fig. 38. Local connection scheme for double-sided detectors.

detector bias, analog supply and digital supply lines, substantially reduces noise coupling through common loops.

The power lines and associated front-end controls are organized by layer in the barrel and by ring in the disk region. Each layer or ring is subdivided in phi into 8–12 segments, each of which has a dedicated power cable that is not electrically connected to any other part of the system until the cable terminates outside the detector at a distribution unit. This isolation reduces cross-coupling and limits the fraction of the detector that would be affected by a segment or cable defect. Segmentation also serves to distribute the mass of the power and signal busses more uniformly around the detector. This scheme results in between 160–240 power lines emanating from each end of the detector. These are routed to the ends at the outer detector radius.

A representative cable geometry is shown in Fig. 39. The substrate is 50 μm thick Kapton with aluminum conductors. A partial data bus is shown with broadside differential lines of 150 μm width and 150 μm spacing between pairs. The complete cable is shown in Fig. 39; it includes 10 DC lines and 18 differential signal



SUBSTRATE + INSULATION: 50 UM KAPTON
CONDUCTORS: ALUMINUM: 25 UM IN LOCAL BUS
50 UM IN SEGMENT BUS

TOTAL WIDTH OF CABLE: 13 mm

Fig. 39. Complete module supply cable (power, control lines, and data).

lines for the 63 MHz clock, control signals, and output data. The signal lines are used in the DAQ scheme that reads out by segment and utilizes fiber-optic drivers at the outer surface of the silicon tracker volume, as described in Section V.E.2 below. The DC power and control lines are needed in any case. The width of the cable is estimated at about 13 mm. Aluminum test cables have been fabricated with 150 micron traces. Preliminary work on forming electrical vias in aluminum cables has shown promising results. Technology to integrate termination resistors in the cables is also under investigation and test structures should be available within a few months.

V. Electronics

A. Design Considerations for Front-end Electronics in the Silicon Tracker

1. Approach

In this section we assess the power requirements and the signal-to-noise for various strip configurations in the Silicon Tracker. These considerations have led to the choice of a 12 cm strip length as the baseline design.

Each electronic channel contains the following functions:

Low-noise preamplification

Pulse shaping

Discrimination

Time stamping

Data buffering

Sparse readout circuitry.

The preamplifier design is strongly influenced by strip length, or more precisely strip capacitance, which governs the front-end noise. Pulse shaping time would be determined by strip length if only shot noise were relevant. In this system the shaping time is dictated by the SSC timing requirements. Time stamping (timing discriminator and the basic storage scheme) is dictated by the bunch frequency of the SSC. The depth of data buffering is determined by the occupancy per channel and therefore depends on strip length. The sparse readout circuitry is independent of strip length. Although the power consumed by this circuit block depends on the hit frequency per chip, the frequency of hits in the whole detector is independent of segmentation and so the total power consumed by sparse readout and output drivers is independent of strip length.

2. Block Diagram

Figure 40 shows the block diagram used for the purpose of analysis. An integrating preamplifier is assumed. The speed of this stage determines the primary bandwidth limit of the system. The current in the first stage is determined by the required noise level and the feedback capacitor is chosen to provide the desired band-width. The subsequent shaper is a CR differentiator to limit the pulse width. This function can be included in other stages without incurring additional power. A subsequent amplifier stage provides the gain required for proper operation of the timing discriminator (comparator).

The scaling approach which is used below assumes that the gain-bandwidth product of the preamplfier is roughly constant (since it will be operated in weak to

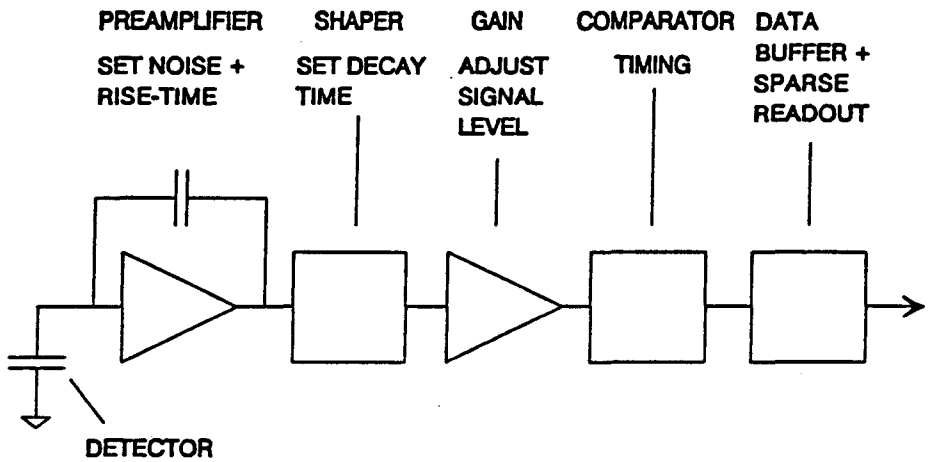


Fig. 40. Block diagram of front-end system.

moderate inversion to reduce power, the transconductance per unit current, and hence the gain-bandwidth product, varies by no more than a factor of 2 to 3). For larger strip length, the feedback capacitor must be increased correspondingly to obtain the same rise-time. This entails less signal voltage at the output of the input integrator, and the subsequent gain stage is required to preserve the same signal level at the comparator input. Since the allowable input noise in this stage is substantially higher than in the preamplifier, the required power is relatively small.

This model also applies to systems using current-sensitive preamplifiers designed for the same peaking time, since this implicitly performs integration.

3. Required Signal-to-Noise Ratio

The required signal-to-noise ratio depends on the need to

set the threshold low enough to accept the full dynamic range, and

set the threshold high enough to obtain adequate suppression of noise hits, while

obtaining adequate overdrive at the comparator input to yield good timing.

3.1 Dynamic Range

For tracks collected on one strip the Landau distribution extends from about 1/2 of the most probable charge (4 fC for a 300 μm thick silicon detector) to over twice that signal; i.e., a range of about 2–8 fC. If charge is shared between two strips, the charge collected on one strip will be at least equal to half the total, i.e., a worst case of 1 fC. For the following we will adopt a dynamic range of 1–8 fC.

3.2 Noise Suppression

The noise spectrum presented to the comparator has both an amplitude and a time distribution. Both are Gaussian. The amplitude distribution is given by the system noise level ν_n. From the rate of noise pulses one can determine the ratio of threshold-to-noise needed for adequate noise suppression so as not to exceed the number of true hits. Although the frequency distribution of noise is familiar to most, the time distribution is less commonly known.

Rice [30] gives an expression for the frequency of noise maxima above a threshold V_t for an rms noise level ν_n and a frequency of zero crossings f_0

$$f_m = e^{-V_t^2/2\nu_n^2} \cdot f_0/2, \tag{1}$$

which he states is "equal to the precise expression" of times that the signal will pass through the threshold with positive slope.

The frequency of zero crossings at the output of an ideal band-pass filter with lower and upper cutoff frequencies f_1 and f_2 is

$$f_0 = 2\sqrt{\frac{1}{3}\frac{f_2^3 - f_1^3}{f_2 - f_1}}. \tag{2}$$

For a CR-RC filter with τ = RC the ratio of cutoff frequencies of the noise bandwidth is $f_2/f_1 = 4.5$ and to a good approximation one can use expressions for low-pass filters, i.e., for the frequency of zeros

$$f_0 = \frac{2}{\sqrt{3}} f_2 = 1.155 f_2. \tag{3}$$

The noise bandwidth of an RC low-pass filter with time constant τ is

$$\Delta f_n = \frac{1}{4\tau} \tag{4}$$

Setting $f_2 = \Delta f_n$ yields the frequency of zeros

$$f_0 = \frac{1}{2\sqrt{3} \cdot \tau} = \frac{0.29}{\tau}. \tag{5}$$

Inserting this result into (1) yields the frequency of noise hits

$$f_n = e^{-V_t^2/2\nu_n^2} \frac{1}{4\sqrt{3} \cdot \tau} = e^{-V_t^2/2\nu_n^2} \frac{0.14}{\tau}. \tag{6}$$

Hence, the required threshold-to-noise ratio for a given frequency of noise hits f_n

is

$$\frac{V_t}{\nu_n} = \sqrt{-2\ln(4\sqrt{3}f_n\tau)}. \tag{7}$$

The average hit rate in a strip of 12 cm length and 50 μm pitch at $= 10^{33}$ cm^{-2}s^{-1} is about 2.10^5 s^{-1} at $r = 9$ cm and 10^4 s^{-1} at $r = 36$ cm (including loopers and interactions). For $\tau = 20$ ns, the frequency of noise zeros is $1.4 \cdot 10^7$. If we allow the rate of noise hits to equal the number of true hits, then the required threshold-to-noise ratio ranges from 2.7 to 3.6. Setting the threshold-to-noise ratio to 4 reduces the rate of noise hits to $2.4 \cdot 10^3$. Note that the noise rate is a very strong function of V_t/ν_n; reducing the threshold-to-noise ratio from 4 to 3.6 (corresponding to a 10% variation in gain, threshold, or noise) more than quadruples the noise rate. For stable operation one should design for $V_t/\nu_n > 4$ to provide a safety margin with respect to noise hits.

Since the threshold must be set at about $\frac{1}{4}$ of the nominal signal, i.e., 1 fC, the noise level must be < 0.25 fC, corresponding to a signal-to-noise ratio > 16 with reference to the nominal signal. This required signal-to-noise ratio is based on suppression of noise hits alone; timing considerations will increase it.

3.3 Comparator Overdrive

"Overdrive" is the difference between the applied signal and the threshold. The required overdrive depends on the gain-bandwidth product of the comparator stage; low-power comparators require more overdrive.

Figure 41 shows the output pulse shape calculated using SPICE for a preamplifier with $\tau_{int} = 20$ ns, a shaper with $\tau_{diff} = 20$ ns, and a gain stage with $\tau_{int} = 5$ ns. Curves are shown for a detector rise time of 0 and a rise time of 10 ns (linear ramp), chosen to approximate the initial slope of the actual detector pulse. Table 10 shows the time walk for various thresholds and values of overdrive for the above time constants (the gain is chosen so that 4 fC yields an amplitude of 1V).

Ideally, one would set the threshold substantially higher than needed for noise suppression, and lower than needed for the required time resolution, to provide a band that would accommodate threshold variations (due to channel-to-channel gain variations, baseline shifts, imperfect device matching, radiation-induced changes in transistor characteristics, etc.) without compromising performance. The above results do not offer much latitude in this respect, although higher values of overdrive alleviate this problem somewhat. For the following calculations we have adopted 50 mV overdrive with a threshold at 200 mV, corresponding to S/N=20 for a 4 fC signal.

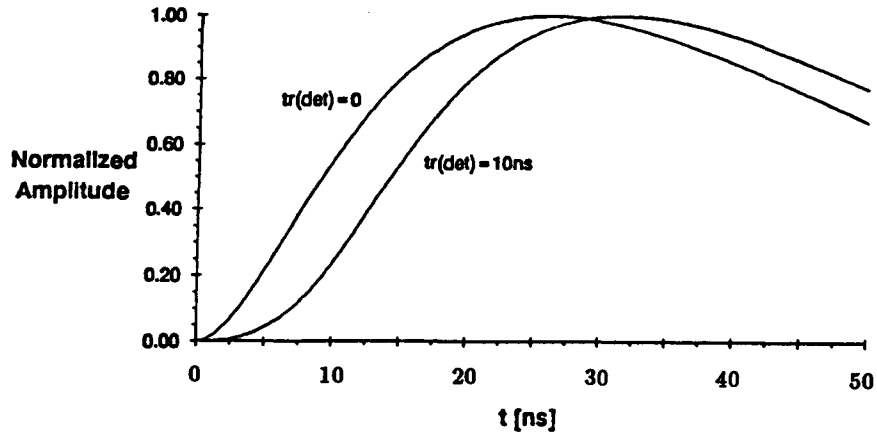


Fig. 41. Pulse shape: $\tau_{int} = \tau_{diff} = 20$ ns; $\tau_{int2} = 5$ ns.

Table 10. Time walk vs. overdrive and threshold for dominant time constants $\tau_{int} = \tau_{diff} = 20$ ns, a gain stage with $\tau_{int} = 5$ ns, and $t_{rise}(\text{det}) = 10$ ns.

Overdrive dV Threshold V_t [mV]	Relative Trigger Point vs. Q_{signal} 1 fC	4 fC	Required S/N (ref. 4 fC) vs. Noise Margin $V_t = 3\sigma_{noise}$	$V_t = 4\sigma_{noise}$	Time Walk Δt [ns]
$d_V = 25$ $V_t = 225$	0.9	0.225	13.3	17.8	13.4
$d_V = 50$ $V_t = 200$	0.8	0.2	15.0	20.0	10.9
$d_V = 75$ $V_t = 175$	0.7	0.175	17.1	22.9	9.1
$d_V = 100$ $V_t = 150$	0.6	0.15	20.0	26.7	7.7

4. Preamplifier Power

From the above discussion one desires a signal-to-noise ratio of 20 for a signal charge of 4 fC, i.e., an equivalent noise charge $Q_n = 0.2$ fC or about 1200 electrons. The noise level actually achievable is determined by:

Shot noise from the detector,

Noise from the detector biasing resistors shunting the input,

Amplifier noise.

4.1 Shot Noise

The detector leakage current after substantial irradiation is, as discussed earlier in this report,

$$I_{det} = (\alpha_c \Phi_c + \alpha_n \Phi_n) p_{strip} L_{strip} d_{det}$$

where α_c and α_n are the damage coefficients for charged particles and neutrons, respectively; Φ_c, Φ_n are the respective fluences; p_{strip} and L_{strip} are the strip pitch and length, and d_{det} is the detector thickness. The corresponding shot noise is

$$Q_n^2 = 2 q_e I_{det} F_i \tau$$

where q_e is the electron charge and $F_i = 0.924$ for a CR-RC shaper with time constants $\tau_{diff} = \tau_{int} = \tau$. For 12 cm strips and a limiting fluence of 10^{14} particles/cm^2, the expected leakage current is 0.7 μA which gives a contribution $Q_{ni(det)} = 420$ electrons.

4.2 Noise from the biasing resistor

Shunt resistance R_p at the input contributes a noise current

$$i_{nr}^2 = \frac{4 k_B T}{R_p} \; [A^2/\mathrm{Hz}]$$

with a corresponding noise charge

$$Q_{nr} = \sqrt{i_{nr}^2 F_i \tau} \; [\mathrm{C}]$$

$$Q_{nr} = \sqrt{\frac{4 k_B T}{R_p} F_i \tau} \; [\mathrm{C}],$$

where k_B is the Boltzmann constant and T the temperature of the resistor. For a CR-RC shaper, $F_i = 0.924$. For $R_p = 200$ kΩ and $\tau = 20$ ns, $Q_{nr} \approx 250$ el. The specification for R_p is 250 k$\Omega \pm 50$ kΩ, so 200 kΩ is a reasonable lower limit.

4.3 Preamplifier Noise

To maintain the required noise charge Q_n the amplifier noise Q_{na} may not exceed

$$Q_{na} = \sqrt{Q_n^2 - Q_{ni(det)}^2 - Q_{nr}^2}$$

where $Q_{ni(det)}$ and Q_{nr} are the contributions from the detector leakage current and the biasing resistor, respectively.

4.3.1 CMOS Preamplifiers

An MOS preamplifier with a CR-RC shaper exhibits an equivalent noise charge

$$Q_{na}^2 = \left(e_n^2 \frac{F_v}{\tau} + 4A_f\right)(C_{det} + C_i)^2$$

where e_n is the spectral density of the equivalent input noise voltage, F_v the form factor associated with the shaper ($F_v = 0.924$ for a CR-RC shaper with $\tau_{diff} = \tau_{int}$). A_f expresses the intensity of the 1/f noise

$$A_f \equiv f \frac{\partial e_{nf}^2}{\partial f}.$$

C_{det} is the detector capacitance and C_i the input capacitance of the amplifier.

The equivalent input noise voltage can be expressed as

$$e_n^2 = 4k_B T_o \frac{\gamma_n}{g_m}$$

where $T_o \equiv 300$ K, g_m is the transconductance of the FET, and the noise coefficient γ_n is an empirical constant dependent on device type, geometry and operating conditions.

In tailoring amplifiers to various values of detector capacitance, one makes use of the fact that the key parameters of the transistor scale with device width W, i.e., $g_m = W \cdot g_m'$ and $C_i = W \cdot C_i'$. In scaling the device width, the ratio of drain current I_d to width W is kept constant, i.e., $I_d/W = \text{const}$. Then $e_n = e_n'/\sqrt{W}$. This allows one to formulate the above equations in terms of quantities determined for a specific device at a given value I_{d1}/W_1, e.g.,

$$C_i' = \frac{C_i}{W}, \quad g_m' = \frac{g_{m1}}{W_1}, e_n' = e_{n1}\sqrt{W_1}.$$

This applies to the "white" noise regime. For some forms of $1/f$ noise

$$A_f \equiv \frac{K_f}{WLC_g^2},$$

where W and L are the channel width and length of the FET, C_g is the gate-channel capacitance per unit area, and K_f is an empirical constant that is device and process dependent. One should note that this model is not universally applicable. First, excess noise usually does not exhibit a pure $1/f$ dependence; often one

finds several slopes. Furthermore, it does not apply to generation-recombination noise, which is also present in MOSFETs. In practice, one must test the applicability of this parametrization by comparing it with data before one applies it to scaled amplifiers. Nevertheless, as a general rule wider devices tend to exhibit better "$1/f$" noise characteristics. In the systems considered here the device sizes are sufficiently large and the shaping time small enough to make the "$1/f$"-noise contribution small, so it will not be included separately in the following analysis. Specifically, the measured values of e_n were taken at the peaking frequency of the filter response and include some $1/f$ noise contributions.

Using the above parametrization one can write a scaleable noise equation in terms of measured quantities,

$$Q_{na}^2 = \frac{e_{n1}^2 W_1}{W}(WC_i' + C_{det})^2 \frac{F_v}{\tau},$$

which for a given Q_{na} yields a device width W. The required supply current is

$$I_d = W\frac{I_{d1}}{W_1}$$

and the input capacitance of the device is

$$C_i = WC_i'.$$

The normalized input capacitance C_i' was obtained from the measurements in Ref. 31. The adopted values are 1.5 fF/μm for $L = 1.2$ μm and 4.2 fF/μm for $L = 3.2$ μm. Data are available for both NMOS and PMOS devices with $L = 1.2$ μm and $L = 3.2$ μm. Although the longer channel devices have better values of γ_n, especially at $I_d/W = 0.1$ and above, their figure of merit

$$\kappa_n = \frac{g_m'}{\gamma_n C_i'}$$

is much inferior due to the larger input capacitance C_i'.

The measured white noise e_n (at constant I_d/W) is practically the same for NMOS and PMOS devices. PMOS devices at $I_d/W = 0.1$ and 0.3 have inferior transconductance and hence speed. Further analysis of the irradiated devices is necessary to determine whether PMOS devices may be advantageous with respect to increased $1/f$ noise. The following data use NMOS devices.

The subset of the data used for the results presented here is summarized below. It should be noted that these are pre-radiation data. Preliminary data after irradiation (5 Mrad of ^{60}Co) indicate that the values of e_n increase by 60–70%.

I_d/W [A/m]	W [μm]	$e_n[nV/\sqrt{\text{Hz}}]$	$e_n'^2$ [V^2 cm/Hz]
0.3	1332	2.5	$8.33 \cdot 10^{-19}$
0.1	1332	3.3	$1.45 \cdot 10^{-18}$
0.03	1332	4.5	$2.70 \cdot 10^{-18}$

4.3.2. BJT Preamplifiers

The noise of a preamplfier using a bipolar junction transistor input is given by

$$Q_n^2 = i_n^2 F_i \tau + e_n^2 (C_i + C_{det})^2 F_v \tau$$

where

$$i_n^2 = 2q_e I_b = 2q_e \frac{I_c}{B}$$

and

$$e_n^2 = \frac{2(k_B T)^2}{q_e I_e} \approx \frac{2(k_B T)^2}{q_e I_c}$$

under the condition that $B \gg 1$ and that the base resistance $r_b \ll k_B T/2q_e I_e$. I_b, I_e, and I_c are the base, emitter, and collector current of the transistor. B is the DC current gain and q_e the electron charge. Again, $F_i = F_v = 0.924$.

The noise of bipolar transistors is well described by simple theory and does not require empirical constants as for FETs. One obtains

$$Q_n^2 = 2q_e \frac{I_c}{B} F_i \tau + \frac{2(k_B T)^2}{q_e I_c} (C_i + C_{det})^2 \frac{F_v}{\tau},$$

which yields a quadratic equation in I_c. The smaller of the two solutions yields the lowest power for a given noise level, and should be used if the gain-bandwidth product is adequate. Radiation measurements [32] indicate that BJT noise does not change appreciably well into the Mrad range, provided that the device current is controlled.

5. Power for the Front-end Chain

The required power for the front-end chain includes power for the preamplifier discussed above, shaper-gain stage, comparator, and digital data buffer and sparse readout. The power requirements for the elements following the preamplifier are independent of strip length and are discussed later in section V. Based on these

Table 11. MOSFET Drain Current I_d vs. Input Noise Q_n, Strip Length L, and Current Density I_d/W. Strip Capacitance = 1.2 pF/cm; CR-RC Shaping Time τ = 20 ns. Shunt Resistance R_p = 200 kΩ, Strip Leakage Current= 60 nA/cm. Total Noise = 1.1 × Noise of Input Transistor Alone.

Q_n [el]	L [cm]	I_d/W = 0.3 A/m		I_d/W = 0.1 A/m		I_d/W = 0.03 A/m	
		I_d [μA]	C_{tot} [pF]	I_d [μA]	C_{tot} [pF]	I_d [μA]	C_{tot} [pF]
1000	6	915	11.8				
1100	6	490	9.7				
1200	6	341	8.9				
	8	845	13.8				
1300	6	260	8.5	252	11.0		
	8	569	12.4				
1400	6	207	8.2	167	9.7		
	8	429	11.8				
1500	6	170	8.1	126	9.1		
	8	341	11.3	325	14.5		
	12	1085	19.8				

Table 12. Total Power of CMOS Front-Ends vs. Input Noise Q_n and Strip Length L. Strip Capacitance= 1.2 pF/cm; CR-RC Shaping Time τ = 20 ns. Shunt Resistance R_p = 200 kΩ. Power of Stages Following Preamplifier P_{fix} = 0.5 mW. Detector Leakage Current= 60 nA/cm.

Q_n [el]	Power [mW] vs. Strip Length			
	6cm	8cm	12cm	18cm
1000	6.1			
1100	3.5			
1200	2.6	5.6		
1300	2.1	4.0		
1400	1.6	3.1	10.7	
1500	1.3	2.5	7.1	

estimates we will assume a fixed power of 500 μW excluding the preamplifier. We focus below on the preamplifier power and noise and its dependence on strip length. Since the detector area is fixed by physics requirements the total power for the detector is approximately proportional to the power per strip/strip length.

Results for CMOS preamplifiers are summarized in Tables 11 and 12. V_{dd} = 6 V is assumed for the preamplifier and 10 μA are allocated to a source follower buffer stage. The overall noise stated in the tables is 10% greater than the noise

from the input transistor alone to account for contributions from the second stage and other noise sources in the preamplifier. The strip leakage current has been taken to be 60 nA/cm, the expected value for a fluence of $\Phi = 10^{14}$ particles/cm^2. All calculations are for a shaping time $\tau = 20$ ns. The bias resistance is chosen to be 200 kΩ, a lower limit. Tables 11 and 12 show the required drain current in the input MOSFET vs. noise and strip length for various values of I_d/W. At longer strip lengths one can see a rapid increase in required current, since the input capacitance of the FET becomes a significant fraction of the detector capacitance (illustrating the fact that capacitive matching is unfavorable with respect to power efficiency). Table 12 shows the total front-end power calculated under the same conditions. Here the lowest current for a given noise level and strip length was chosen from the possible values of I_d/W. Blank entries signify that the stated noise level cannot be achieved. Note that these are pre-radiation noise levels; after irradiation the lowest attainable noise level is about 1500 el for 6 cm strips only, with a preamplifier power dissipation of 5–6 mW.

Table 13 shows results for BJT front ends. Data are presented for two values of DC current gain, $B = 30$ and $B = 100$ to indicate the sensitivity to this parameter. Radiation damage data indicate that $B = 100$ is a reasonable design goal. The supply voltage is assumed to be $V_{cc} = 3.5$ V, and 10 μA have been allocated to an emitter follower buffer stage. Again, the tables state the overall noise, which is assumed to be 10% larger than for the input transistor alone. Blank entries signify that the stated noise level cannot be achieved.

6. Conclusions

Although portions of this analysis require further detailed study, one can draw some general conclusions from the data presented here.

- CMOS front-ends are potentially interesting only for strip lengths up to ~ 6 cm.
- Bipolar transistor front-ends offer superior performance. Strips longer than 12 cm are only usable with relaxed S/N requirements. A total front-end power of 1 mW per channel appears feasible with careful design.

Bipolar transistor circuitry is clearly the compelling choice for the analog front-end circuitry (preamplifier through timing comparator). For the substantial amount of digital circuitry in this system (time-stamping, data buffering, and data sparsification) CMOS is clearly the technology of choice, because of both circuit density and power. Although combining all circuitry on one chip is attractive, lack of a readily available BiCMOS process with the required characteristics imposes a two-chip architecture, i.e., a BJT analog chip and a CMOS digital chip. The

Table 13. Total Power of BJT Front Ends. Strip Capacitance= 1.2 pF/cm; CR-RC Shaping Time $\tau = 20$ ns. Shunt Resistance $R_p = 200$ kΩ; Leakage Current= 60 nA/cm. Preamplifier. Supply Voltage= 3.5 V; Current in Output Buffer= 10 μA. Total Noise = 1.1 × Noise of Input Transistor Alone.

Q_n [el]	Preamplifier Current [μA] vs. Strip Length				Power per Channel [mW] vs. L_{strip} (P_{fix} = 0.5 mW)			
	6cm	8cm	12cm	18cm	6cm	8cm	12cm	18cm
DC Current Gain of Input Transistor $B = 100$								
1000	46	134			0.70	1.00		
1100	34	66			0.65	0.77		
1200	27	49	171		0.63	0.71	1.13	
1300	22	39	102		0.61	0.67	0.89	
1400	18	32	78		0.60	0.65	0.81	
1500	16	27	63		0.59	0.63	0.76	1.18
DC Current Gain of Input Transistor $B = 30$								
1000								
1100								
1200	34				0.65			
1300	25	56			0.62	0.73		
1400	20	38			0.60	0.67		
1500	17	30			0.59	0.64		

added effort for mounting and chip-to-chip interconnections is clearly outweighed by the superior performance that the two-chip architecture provides.

B. Analog Front-End Designs

The preceding discussion shows that bipolar transistors allow substantial savings in the power needed for the input amplifier. Bipolar transistors' superior transconductance and threshold matching also simplify the design and reduce power requirements of the subsequent gain and comparator stages. In the following we present results on a bipolar transistor front-end implemented with a "radiation-soft" process as a test of the basic concept. We then present simulation results on a design specifically directed toward meeting the design specifications of the Silicon Tracker.

1. Dynamic Measurements on a Bipolar IC

Work described in Ref. 33 shows some useful results for bipolar front-end chip development. Using the recently introduced MOSIS 2 μm CMOS with bipolar complement, amplifier/comparator circuits were designed using bipolar fronts, JFETS, CMOS, and capacitors.

An extended minimum geometry bipolar component has a measured base resistance of 250 ohms, and measured noise indicating an effective resistance of 300 ohms. Beta is 100. The experimental p-channel JFETS have a pinch-off voltage of 5 V, inconveniently high if system power consumption or complexity is a concern, but of little consequence for prototyping. The designer has complete control of W/L ratios, so a prototyping program can use a very broad range of series resistors or active load values, as with CMOS. Tektronix P-JFETs, which could be used similarly, are supported by Tektronix in a short channel structure only. Experience with JFET structures from MOSIS will help in developing more useful JFETs from commercial vendors. The MOSIS devices are moderately rad hard, but extreme hardness is not needed in their prototyping role. This process provides an inexpensive and relatively speedy prototyping path to resolve front-end chip system issues.

Two amplifier/comparator versions were designed: one uses JFET as active loads and the other CMOS. The JFET version is shown in Fig. 42. The preamplifier uses J1 as an active load, and J2 as a linear feedback resistor. Q6, J4, Q7, and J6 are a second gain stage. Q8, J7 are the comparator stage using a ground referenced threshold, and Q9, J8 provide another gain stage. The comparator has time-over-threshold operation. Gain before comparison is 12 mV/fC, with noise of 2000 electrons for a 10 pF load. This includes a significant contribution from the rather large base resistance in this process. DC bias voltages and AC performance are within 10% of simulation values. Power consumption is less than 1 mW.

The Rice formula discussed in the preceding section was nicely verified using the JFET chip. Figure 43 shows the counting rate fraction versus a range of input charges, for which the error function fit gives a sigma of 0.317 fC. Figure 44 is a semilog plot of noise hit counts versus the threshold square, which includes a fit using the Rice formula:

$$f_n = f_{no} \exp\left(\frac{-V_t^2}{2\sigma^2}\right) = 4.1 \times 10^6 \exp(-4.95 V_t^2) \Rightarrow \sigma = 0.32 \text{ fC}$$

Using $f_{no} = 0.14/\tau$, the fit corresponds to the measured shaping time constant of 35 ns, which implies $f_{no} = 4$ Mhz. This is an important verification of the Rice analysis as it applies to the SSC threshold versus noise hits estimates. Time walk measurements for shaped input signals indicate 15 ns of walk for signals from 2 fC to 8 fC. MOSIS is presently fabricating a 64 channel, 80 μm pitch design with AC coupling between amplifier and the comparator, using the experience with the JFET amplifier discussed here. This circuit is expected to have about half the timewalk of our initial design.

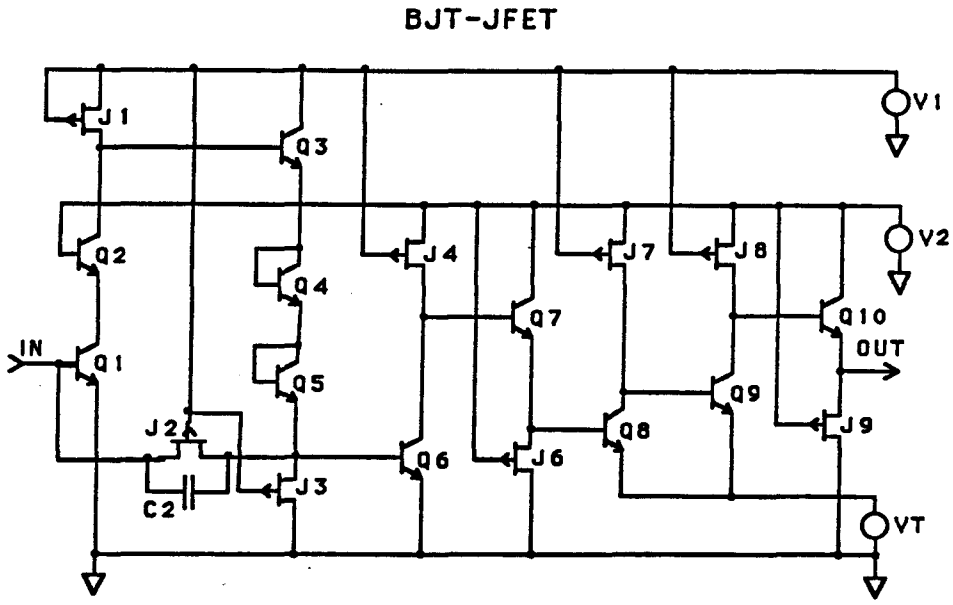


Fig. 42. Preamp discriminator.

2. Design of a Front-End Prototype

Critical tests of the module concepts described in IV.E require a front-end IC that meets the key performance goals. Assembling a prototype detector module that allows system tests of electronic characteristics and radiation resistance is crucial to establishing a production design. Here we present results on a preliminary design that is being refined for fabrication. The data shown here are for a design based on the Tektronix SHPi process, which offers low parasitic capacitances and high packing density. Unfortunately, proton irradiations have shown that the current gain of both the vertical *npn* and the lateral *pnp* transistors is marginal. AT&T and Westinghouse offer processes with substantially better radiation characteristics, but with lower circuit density and higher junction capacitance. Adaptations of the circuit to these processes are being investigated to assess the necessary trade-offs.

The circuit follows the basic scheme outlined in V.A. A simplified circuit diagram is shown in Fig. 45. Each channel comprises a charge-sensitive preamplifier followed by gain stages and a comparator. CR-RC pulse shaping is implemented by the discharge time constant RfCf in the preamplifier feedback loop and by an RC integrator formed by R11, R12 and C11 at the output of the differential gain stage Q11–Q12. The threshold is applied differentially to Q13 and Q14 to avoid threshold variations introduced by noise or voltage drops on the supply lines. The

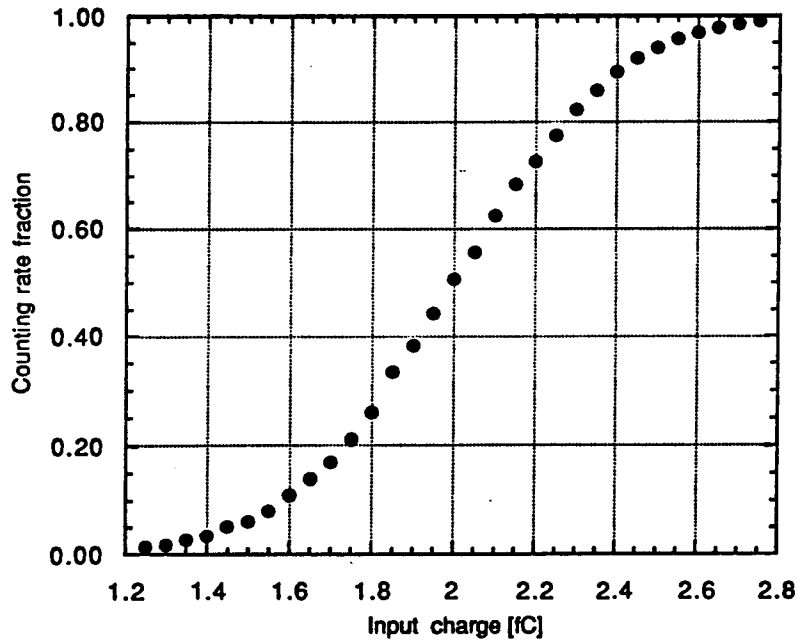


Fig. 43. Discriminator turnon vs. input charge.

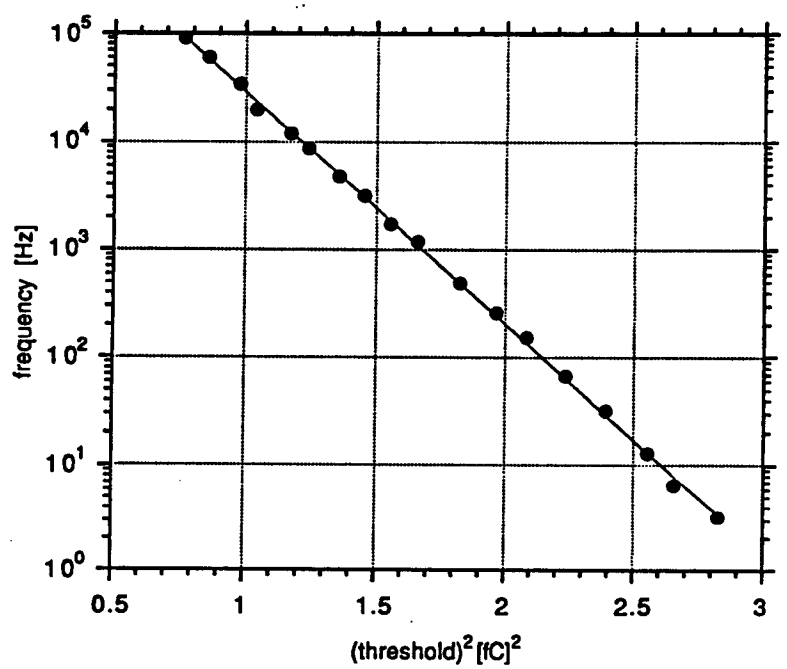


Fig. 44. Noise counting rate vs. threshold.

reference voltage applied to the base of Q12 is provided by a "dummy" amplifier identical to the stages feeding Q11. One "dummy" amplifier serves an entire chip. The circuit is easily adaptable to either positive or negative input signals (as required for double-sided detectors), by juxtaposing the output connections at Q11–Q12 or, since the circuit will handle bipolar signals, by inverting the digital output. The output stage is shown as a current driver, which can be scaled easily to match the drive requirements of the following IC. Alternative output drivers are being considered.

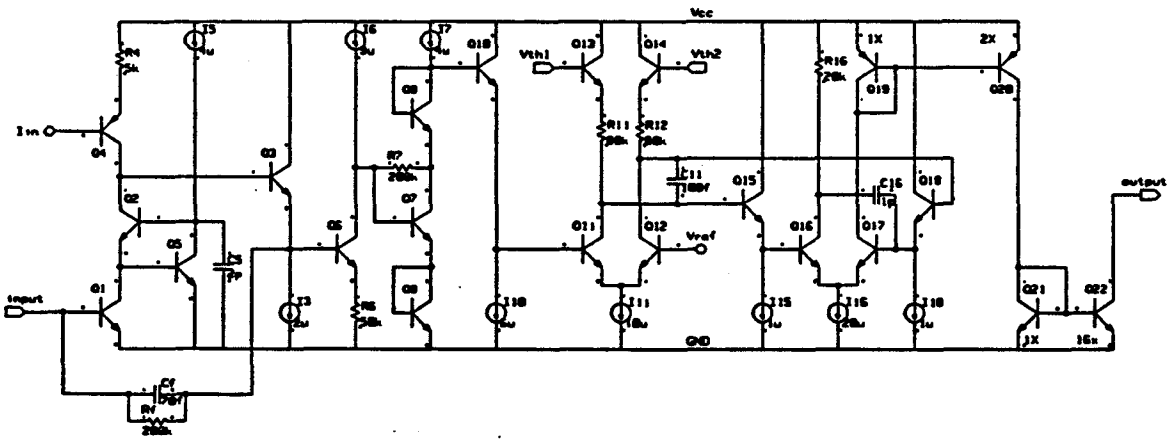


Fig. 45. Simplified circuit diagram of the analog front-end IC.

The circuit was simulated using realistic detector current pulses, including detector coupling capacitors, bias resistors, etc. The detector leakage current was set to the expected value after a particle fluence of $1.5 \times 10^{14}\text{cm}^{-2}$. Results are summarized in Table 14. The circuit is very close to meeting the target specifications; only the time walk needs to be reduced somewhat. These results are achieved at a very low power dissipation of 620 μW, which, together with the power estimated for the digital circuitry in the following discussion, is well within the target of 1 mW per channel.

C. Development of a Working Specification

There are five functional blocks in a bipolar front-end chip: preamp, amplifier, comparator, calibration, and die support circuitry. The major design issues fall into three groups. The first group has been discussed extensively in the previous two sections:

Table 14. Simulation Results for the Prototype Analog Front-end IC

Detector Parameters	
Strip Length	12 cm
Strip Capacitance (1.2 pF/cm)	14.4 pF
Leakage Current (100 nA/cm)	1.2 μA
Bias Resistor	200 kΩ
Blocking Capacitance	144 pF
Electronics	
Shaping Time Constant (CR-RC)	20 ns
Equivalent Input Noise Charge	1225 el rms
Comparator Threshold (4Qn)	165 mV
Time Walk (1 fC - 8 fC)	17 ns
Supply Voltage	3.5 V
Power Consumption	620 μW

Power consumption

Signal/noise

Timing accuracy.

We can list the design objectives in these areas as follows:

< 1200 electrons noise

Less than 15 ns time walk for 1 fC < Q (signal) < 8 fC

Less than 1 mW/channel power including digital section

Dead time less than 100 ns after a hit

Less than 0.5% inefficiency in a channel.

Note the signal-to-noise affects how crisp the discriminator threshold will be. For a threshold at 0.25 times the mean signal, and a 20-to-1 mean signal-to-noise ratio, the discriminator will be 99% efficient for signals = 0.37 times a mean signal. The noise also sets a reasonable limit for the required threshold matching of the discriminators. In particular, a $\pm 10\%$ variation on the absolute value of the threshold is a reasonable goal.

The second group of design objectives speaks to unwanted system interactions:

Supply voltages and filtering

Front end digital pickup, grounds, and shielding

Front end channel and die crosstalk.

The third group addresses the realities of the process chosen for the front-end chip:

Radiation hardness, design tolerances, calibration accuracy

Available radiation-hard auxiliary devices to npn transistors

Device tolerances over production

Production testability of circuit design

Reliability of circuitry and its contribution to failure modes.

A complete design needs to address all the above issues. We expect to complete the specifications in the latter two areas this coming year.

D. Digital Data Storage

1. Introduction

Several possible architectures which are suitable for the digital readout of strip detectors at the SDC have been evaluated. This section describes the two architectures which are most suitable for this application and it offers some conclusions on their merits. One of the architectures is a data-driven scheme and the other is a clock-driven scheme. The design of the data-driven architecture is dependent on the mean occupancy of the strips, while the clock-driven scheme is most sensitive to the trigger latency. The conclusion of the analysis is the choice of the data-driven scheme as our baseline design.

1.1 Design Assumptions

The design parameters assumed are listed in the Table 15. They are appropriate for the inner layers of the SDC silicon tracking detector at a luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$. This very high luminosity has a striking impact on the architectures through its effect on mean strip occupancy.

Table 15. Design Assumptions for $10^{34}\text{cm}^{-2}\text{s}^{-1}$ Luminosity

1) Beam crossing (bc):	Every 16 ns (RF clock)
2) Max. Occupancy of a strip (Oc):	1% (uniform distributions, uncorrelated)
3) Level-1 latency (T1):	256 beam crossings (4.0 μs)
4) Max. mean Level-1 accept rate:	100kHz
5) Min. separation between two Level-1 triggers:	1 beam crossing
6) No. of channels per chip:	128
7) Strip pitch:	50 μm

It is assumed that the data from each strip is buffered at every beam crossing for a period of time called the Level-1 latency. During the Level-1 latency, a Level-1 trigger decision is made either to reject the data from the corresponding beam

crossing or to retain it for transmission off of the chip. The data from a beam crossing will be channel address encoded once a decision is made to retain the data from that beam crossing. Then the encoded data will be serially transmitted off of the chip.

The channel address encoding is achieved by only encoding addresses of the channels that received hits. The process of encoding the data from a beam crossing will take a few beam crossings. A pre-channel encoding buffer will be employed to store the data that arrived at the encoder while processing data from another beam crossing.

The encoded data from the beam crossings that received Level-1 triggers will be transmitted in the same order as the Level-1 triggers. Furthermore there will be a pre-data transmission buffer to store the encoded data corresponding to a Level-1 trigger while transmitting (or waiting to transmit) the encoded data corresponding to another Level-1 trigger.

Since it is necessary to transmit all the data out of the Level-1 buffer it is assumed that a Level-2 buffer will not be required. If it is required, a Level-2 buffer can be incorporated into the design at a later stage.

1.2 Concept of the Readout Architectures

Sections 1.2.1 and 1.2.2 outline the concepts of the data-driven scheme and the clock-driven scheme respectively. In the case of the clock-driven scheme, either "hit" or "no hit" datum from each strip is stored for every beam crossing. In the case of the data-driven scheme, only "hit" datum from each strip is indirectly stored by storing the "time stamp" of the beam crossing at which the hit was generated.

Since the maximum occupancy of a strip is 1%, the area overhead of the data-driven scheme will be smaller than that of a clock-driven scheme. The data storage efficiency of the clock-driven scheme is 100%, but in the case of the data-driven scheme, the efficiency is dependent on the buffer length. Therefore in designing the data-driven architecture, a compromise must be made between the efficiency and the area overhead.

1.2.1 Data-driven Readout

Figure 46 shows an abstract representation of this architecture. In this scheme there is a CAM (content addressable memory) ARRAY assigned to each channel. Each array may contain one or more locations, determined by the necessity to keep the efficiency high. Each location is capable of storing the time stamp generated by the time stamp counter and also indicating at every beam crossing whether the contents match the desired time stamp. The length of the time stamp sequence is

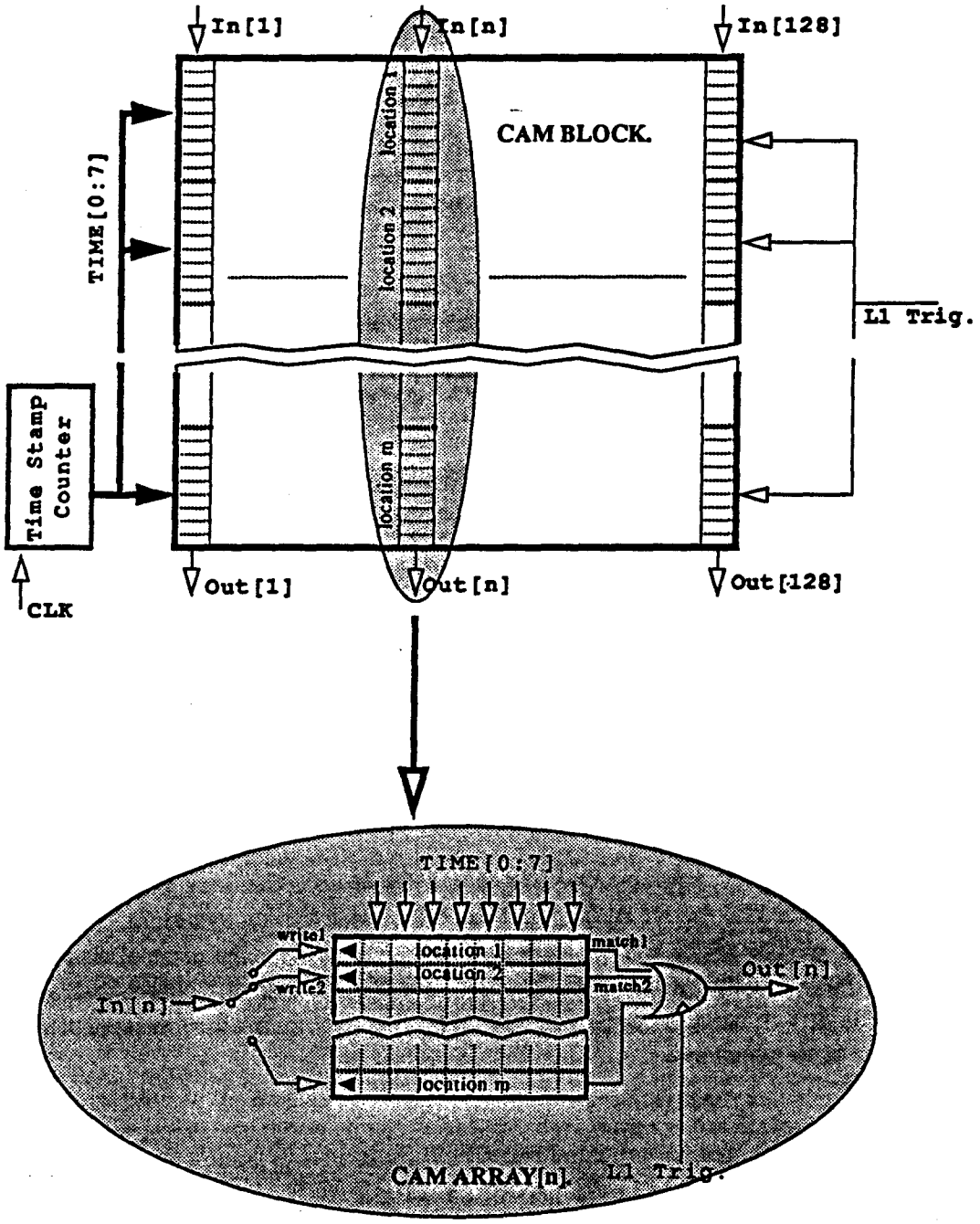


Fig. 46. Outline of the data-driven readout.

T1 (8 bits if T1 = 256) and it is synchronized to the beam crossing. Therefore, within every time stamp sequence, each time stamp corresponds to a beam crossing.

If there is a hit at a beam crossing in a given channel, i.e., its input is active, then the time stamp of this beam crossing will be stored into a location for this channel. After the Level-1 latency the time stamp will be the same as the stored time stamp. At this point if there is a Level-1 trigger (which will correspond to the beam crossing at which the time stamp was stored) this channel will output a MATCH signal. Therefore this scheme enables the data at the input to a chip to be reconstructed after Level-1 latency by grouping MATCH outputs from all the channels.

In order to avoid any undesirable interaction between read and write operations, the read operation is performed during the first half period of a beam crossing and the write operation is performed during the second half period of a beam crossing. Location contents that are stored at one time stamp should be accessible only at the next occurrence of the same time stamp. In order to determine whether the contents of a location are "valid", a flag (RPFLAG - Read Permission FLAG) is employed with each location. This RPFLAG could be set at any time between the point of the completion of the write operation and before the next (first) occurrence of the stored time stamp. Similarly, RPFLAG could be reset at any time after the next (first) occurrence of the stored time stamp and before the second occurrence of the same time stamp.

If there is more than one location per channel then each location must be written in turn. In order to access each location in turn for writing, another flag (WPFLAG - Write Permission Flag) is employed with each location.

1.2.2 Clock-driven Readout

Figure 47 shows an abstract representation of this architecture. Functions of this architecture are similar to those of a FIFO (a dual port RAM). The RAM-block consists of "T1+1" locations and each location contains 128 static memory elements, i.e., one for each channel.

At every beam crossing, hit information from all 128 channels (irrespective of whether there was a hit in any channel) will be written into a location that is pointed to by the WRITE POINTER. The WRITE POINTER is clocked by the RF-Clock. The READ POINTER lags the WRITE POINTER by Level-1 latency. Therefore data stored into a location will be read out after the Level-1 trigger latency, provided there is a Level-1 trigger.

The READ and WRITE POINTERS are generated using two 257 (for T1=256) bit shift registers. These shift registers are clocked by the RF clock.

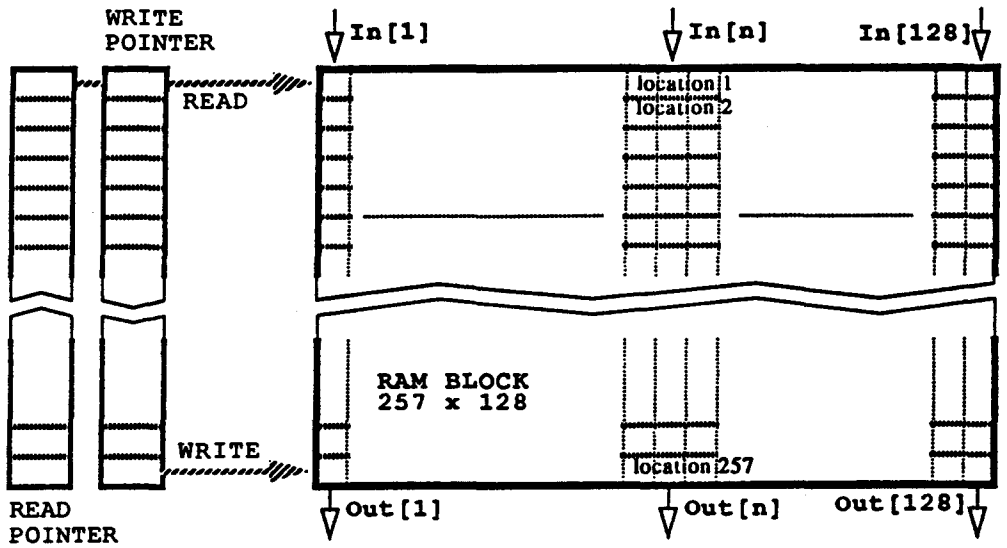


Fig. 47. Outline of the clock-driven readout.

2. Design of the Data-driven Architecture

Figure 48 shows the floor plan for the data-driven architecture. This plan is based on the design assumptions shown in Table 15. It is critical to estimate the power dissipation and the area overhead of each architecture. In this estimation, it is assumed that the design will be fabricated in a typical 1.2 μm CMOS process. Since the dominant factor in determining the power dissipation is the clocking of capacitors at the frequency of the RF clock, only the power dissipation due to clocking of the gate and the substrate capacitances by the RF clock are considered. The width of the chip is fixed by the strip pitch (128 $\times$ 50 μm); therefore the area overhead is expressed in equivalent total length per channel.

2.1 Input Section

This section is divided into 64 vertical segments pitched at 100 μm. Each segment consists of 2 input pads, 2 input protection circuits and 2 logic level shifters for a pair of (two adjacent) channels. It is assumed that the size of an input pad is 80 μm $\times$ 80 μm and the spacing between two adjacent pads is 20 μm (i.e. 100 μm pitch). As the nature of the input signal has not been decided, the length is estimated to be 400 μm. Furthermore, it is assumed gates of two minimum sized MOSFETs from each channel will be clocked at the same rate as the beam crossing. Therefore the power dissipation per channel is

$$(CV^2\ \mathrm{f}) = 2 \times 7\ \mathrm{fF} \times 5\ \mathrm{V}^2 \times (1/16\ \mathrm{ns}) = 22\ \mu\mathrm{W}$$

where the input gate capacitance of a minimum sized MOSFET in a 1.2 μm process is taken to be about 7 fF.

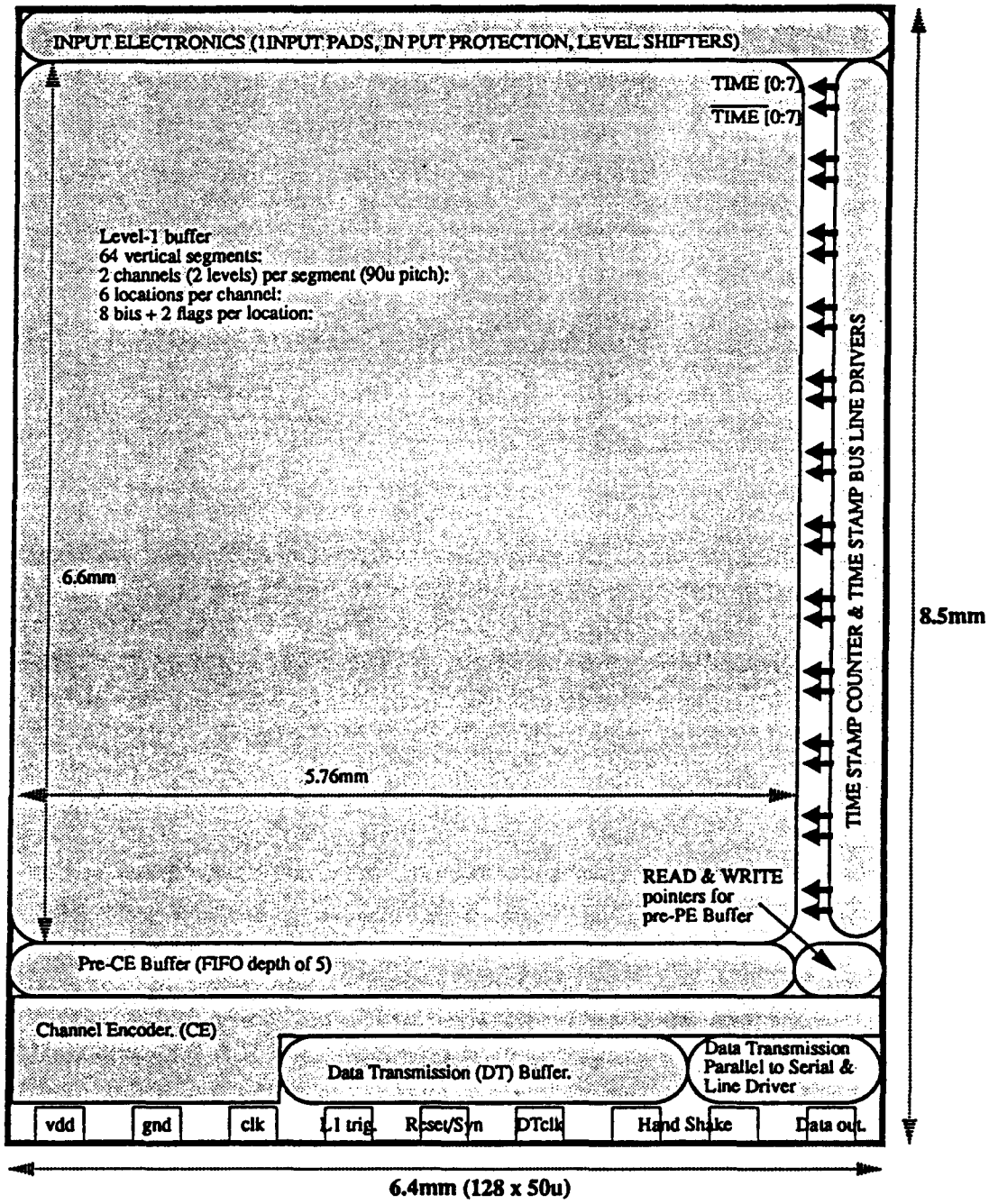


Fig. 48. Floorplan of the data-driven architecture.

Table 16. Efficiency of the Data-driven Architectures for 1% Occupancy

No. of locations per channel	Data recording efficiency
Level-1 Latency = 128	
1	44%
2	74%
3	90%
4	96.8%
Level-1 Latency = 256	
1	28%
2	52%
3	72%
4	85%
5	92.6%
6	97%

Table 17. Efficiency of the Data-driven Architectures vs. Occupancy Level-1 latency = 256

	Occupancy		
Depth	0.1%	0.2%	0.5%
1	79%	68%	46%
2	98%	92%	76%
3	99.99%	98%	92%
4		99.62%	97%
5			99.63%

2.2 Level-1 Buffer and Time Stamp Counter

This section is divided into 64 segments pitched at 90 μm. The length of this section depends on the number of locations necessary for high efficiency. Simulations using a Verilog behavioral description simulator with a random occupancy of 1% give the results shown in Table 16. The Level-1 latency is either 128 beam crossings or 256 beam crossings. Table 17 shows the dependence of the efficiency on the occupancy for a Level-1 latency of 256 beam crossings. A choice of 6 locations gives an estimated efficiency of 97% for the worst case of 1% occupancy. For the case of 6 locations each segment consists of 12 time stamp storage locations (CAM ARRAY) for a pair of two adjacent channels. The top six locations form one of the channels and the bottom six locations form the other channel. The length of a location is 550 μm, therefore the total length of this buffer is 6.6 mm.

The remaining space (of 640 μm $\times$ 6.6 mm) adjacent to the buffer is used to implement the time stamp counter and the line drivers for the time stamp lines. The pair of complementary time stamps are routed through 12(rows) $\times$ 2(a pair) $\times$ 8(bits) lines, i.e, a pair of time stamp buses per row of locations. The time stamp is gray coded; therefore only a pair of bits will make the logic transition per beam crossing. Each location will present a capacitance of 10 fF to each line of the time stamp buses. This capacitance is due to the junction capacitance of a minimum sized drain/substrate parasitic diode. Therefore, the power dissipation per channel due to charging and discharging time stamp buses is

$$2 \text{ (pair)} \times 6 \text{ (locations)} \times 10 \text{ fF} \times 5 \text{ V}^2 \times (1/16 \text{ ns}) = 188\ \mu\text{W},$$

Furthermore, power will also be dissipated in clocking the time stamp counter and in routing the time stamps to the line drivers for the time stamp buses. This will

present an equivalent total capacitance of 2 pF. Therefore, power dissipation per channel is

$$2 \text{ pF} \times 5 \text{ V}^2 \times (1/16 \text{ ns}) \times (1/128 \text{ (no of channels)}) = 24 \ \mu\text{W}.$$

and the total power dissipation is 212 μW.

2.3 Channel Address Encoder and Data Transmission

Figure 49 shows a flow chart for the functions of the channel address encoder. This scheme will take a minimum of 17 clock cycles (when there is no active data) and a maximum of 161 clock cycles (when there is active data in every bucket) to process data from a retained beam crossing. If it is assumed on average there are four buckets that have active data per beam crossing, it will take 38 clock cycles to process the data.

The main reason for choosing this scheme is its favorable area overhead. This scheme takes 144 latches, 16 8-input clocked or-gates, 8 shift registers, a 3-bit counter and a 4-bit counter. All the 144 latches and the 8-input or-gates could be laid out within an area of 200 μm in length across the chip. The rest of the components could be confined to an area of 500 μm $\times$ 2 mm.

It is estimated the total equivalent capacitance is about 1 pF, but this capacitance will be clocked only while processing data from a beam crossing that received a Level-1 trigger. The average period (10 μs) between two Level-1 triggers is much larger than the processing time (600 ns average), therefore the power dissipation per channel in the channel encoder will be insignificant when it is averaged at the same rate as the Level-1 trigger.

The pre-channel encoder buffer is employed to buffer the data from a retained beam crossing while processing the data from another beam crossing. This buffer is a RAM configured as a FIFO. It has five locations and there are 128 bits per location, i.e. one per channel. The depth of five will give data recording efficiency of 99% for the processing time of 600 ns (average) and Level-1 trigger rate of 100 kHz. This buffer will occupy an area of 0.5 mm in length across the width of the chip. The power dissipation for this will be insignificant because this buffer will be asynchronously clocked by the Level-1 trigger.

The channel encoded data will be buffered into the pre-data transmission buffer (a FIFO) before the transmission off of the chip. This buffer has 8-bits per location: 7 bits for the channel address and another bit to indicate whether the data in a location is from the same beam crossing as the data in the previous location, or from a new beam crossing. The depth of this buffer depends on the data readout protocol which is not yet clear at this time; however it is assumed this will not have any impact on the overall merits of this architecture. An area of 0.5 mm $\times$

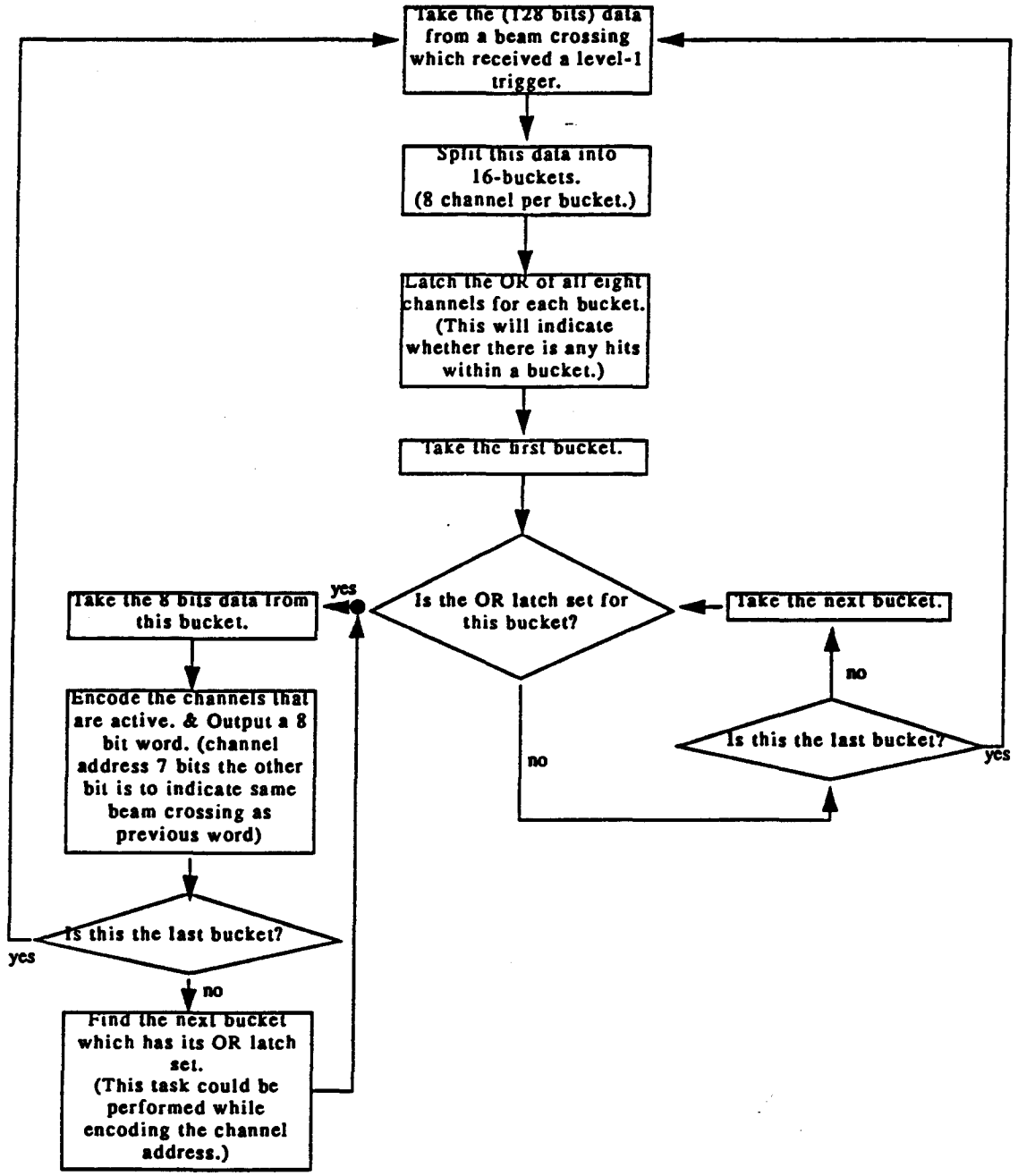


Fig. 49. Flow chart for channel address encoder.

3 mm is allocated for this buffer. This area will accommodate about 35 locations. The power dissipation of this buffer is also insignificant.

The channel address that is being readout from the pre-data transmission buffer will be converted from parallel to serial before transmission. An area of 0.5 mm × 1.4 mm is allocated for the 8-bits parallel to serial convertor and the electronics associated with the data transmission. If it is assumed that it takes 350 ns (4 × 7 bits at the same rate as the beam crossings) to transmit data corresponding to a Level-1 trigger and each chip is accessed at rate of 200 kHz, then the average power dissipation per channel due to the data transmission can be set under 25 μW allowing each chip to dissipate up to 5 mW during the transmission. Therefore, the total area overhead of this section is (0.5 + 0.2 + 0.5) mm × 1.2 mm = 1.2 mm total length × 6.4 mm width. The total power dissipation of this section is 25 μW.

2.4 Pads for the Control signals and the Data Lines

An area of 300 μm in length across the width of the chip is allocated for the pads and the electronics associated with these pads. It is estimated there will be about 9 pads. Their purpose is as follows:

vdd, gnd:	power supply pad
clk:	clock signal synchronized to beam crossing
L1 trig:	input for Level-1 trigger
Reset/Sync:	input to reset the chip to its initial conditions
DTclk:	another clock if the data transmission needs to be done at a slower rate
Hand shakes:	To signify the beginning and the end of data transmission off a chip
Data out:	Serial data out from the channel address encoder

It is assumed that the power dissipation associated with pads will not have any significant effect on the power dissipation per channel.

3. Design of the Clock-driven Architecture

Figure 50 shows the floor plan for the clock-driven architecture. The concepts of the input section, channel encoder and the data transmission are the same as that of the data-driven architecture, but in the case of the Level-1 buffer the CAM block is replaced by the dual port RAM.

The RAM block is constructed using an array of 257 (locations) × 128 (bits) static memory elements. The size of a static memory element is 80 μm × 45 μm; therefore the overall size of the Level-1 buffer is 20.56 mm × 5.76 mm. The remaining space adjacent to the buffer is used for the shift register chain for the read and the write pointers.

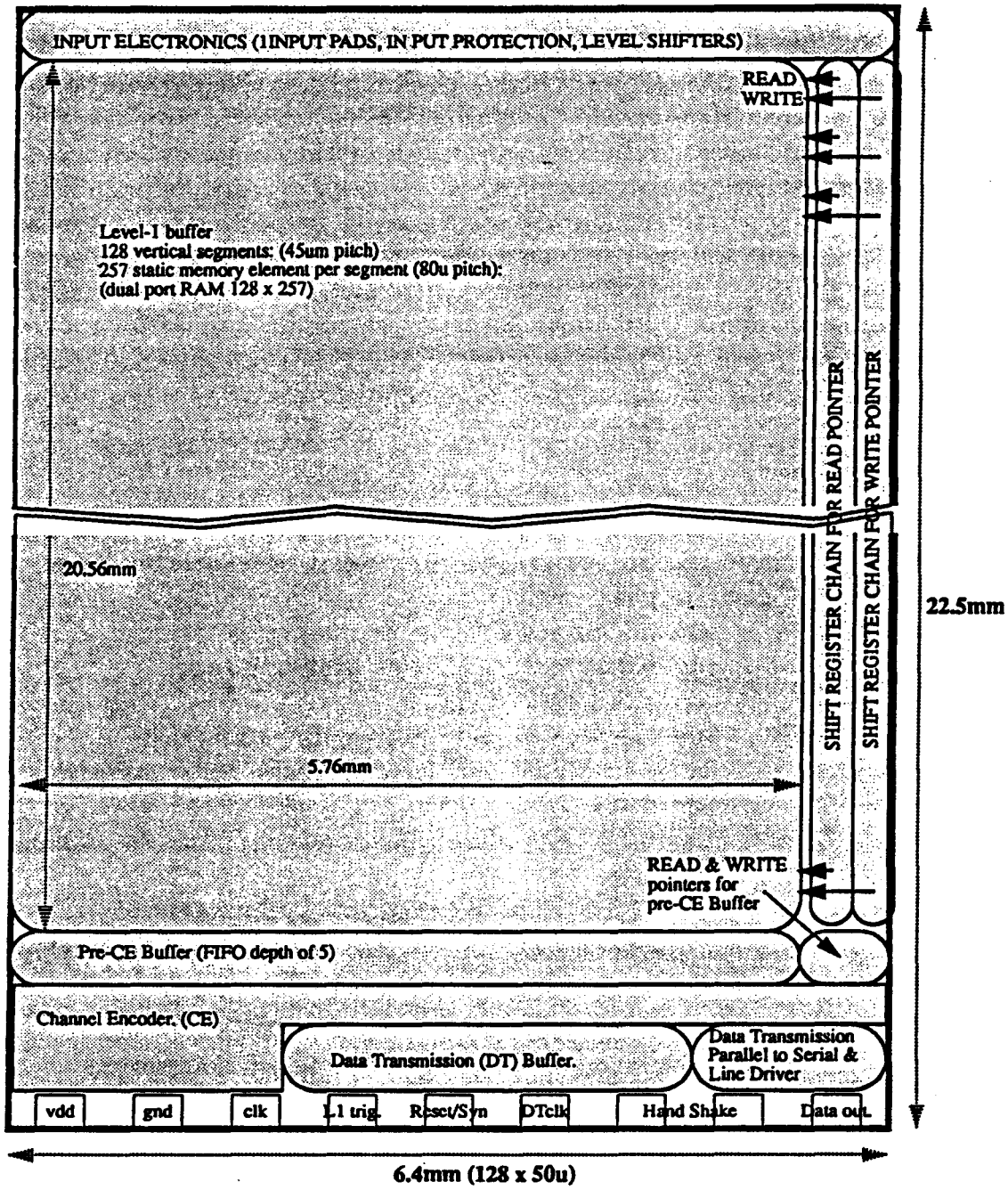


Fig. 50. Floor plan of the clock-driven architecture.

The read and the write pointers will propagate through the buffer at the same rate as the beam crossings. Each static element will present a capacitance of 14 fF to both the read and the write lines. This capacitance is due to gates of two minimum sized MOSFETs. Therefore the power dissipation per channel in clocking the pointers is 2×14 fF $\times$ 5 $V^2 \times (1/16$ ns$) = 43$ μW.

Each static element will present a capacitance of 10 fF to each of the lines of the pair of complementary input buses. This capacitance is due to drain/source junction capacitance of the minimum sized MOSFETs. The power dissipation due to driving the pair of complementary input buses with the occupancy of 1% and at the same rate as beam crossings is

$$2 \times 257 \times 10 \text{ fF} \times 5 \text{ V}^2 \times (1/16 \text{ ns}) \times 0.01 = 80 \ \mu\text{W}.$$

Each shift register from the shift register chain will present the gates of 8 minimum sized transistors to the clock lines.

The power dissipation per channel due to clocking the shift registers is

$$8 \times 2 \times 257 \times 5 \text{ V}^2 \times (1/16 \text{ ns}) \times (1/128) = 350 \ \mu\text{W}.$$

(The shift registers used in this scheme are master-slave flip flops. The above contribution to the power dissipation could be halved by replacing the flip flops with quasi-shift registers, but this will require two non-overlapping clocks with a period of 16 ns and a duty cycle of 25%.)

The total power dissipation per channel is 473 μW.

4. Conclusions

Table 18 gives the summary on the merits of both architectures, for Level-1 latency equal to 128 and equal to 256. It can be seen from the table that the data driven scheme looks more viable than the clock-driven scheme: specifically, in the case of the Level-1 latency equal to 256 beam crossings, the length of a chip using the clock-driven scheme is too long. A certain percentage of the hit information will be lost in the data-driven scheme; this has been minimized at the expense of power and area overhead. The loss at luminosities below $10^{34}\text{cm}^{-2}\text{sec}^{-1}$ is, however, negligible. In addition, for the majority of detectors at larger radii, 4 rather than 6 storage locations would be adequate.

A test structure for a CAM storage location has been fabricated (using a 3.0 μm process) and tested for its functions. This test structure has proved the feasibility of the time stamp storage and the content match. Furthermore a test structure which consists of 16 channels with a depth of four CAM locations has been designed and submitted for fabrication using a 1.2 μm CMOS process.

Table 18. Summary of the Merits of the Architectures

Architecture	Power dissipation	Length	Efficiency
Level-1 latency = 128			
data-driven	197 μW	6.30 mm	96.80%
clock-driven	330 μW	12.22 mm	99.99%
Level-1 latency = 256			
data-driven	256 μW	8.50 mm	97.00%
clock-driven	520 μW	22.50 mm	99.99%

At present, the design of a 64 channel chip based on the data driven architecture is under way. This will be submitted in the near future. The design and testing of this 64 channel chip will help to confirm:

a) the feasibility of the complete design (time stamp storage, sparse readout etc.)

b) the assumptions made for power estimation

c) speed of the overall design

d) fault immunity of the overall design.

E. Data Acquisition

Elements in the readout chain are shown in Fig. 51. The first element is the front-end chips, which contain the Level-2 pipeline, and since the architecture is data driven automatically provide zero suppressed information. Read-out buffering and control is considered part of DAQ, but the initial logic must be contained within the pipeline chip. A single front-end chip services 128 strips.

The output from the front-end chip is transmitted off the detector; transmission is considered a separate element in the readout chain since several options are available, some of which represent quite complex systems in themselves. In the most general case there are two transmission routes, one to a Level-1 and one to a Level-2 trigger system: no further consideration is given to Level-1 triggering past the observation that transmission schemes with sufficient bandwidth to allow a silicon Level-1 trigger exist. Readout for the Level-2 occurs upon receipt of a Level-1 trigger. The transmission scheme is bi-directional in the sense that control signals are routed into the detector along the same physical path that the data leaves.

At the remote end of the transmission system, the data is received; this third element in the readout chain is in practice embedded in the Level-2 trigger logic. It is considered a separate element since its format is driven by the structure of the front-end chips and the transmission scheme as well as the trigger logic itself.

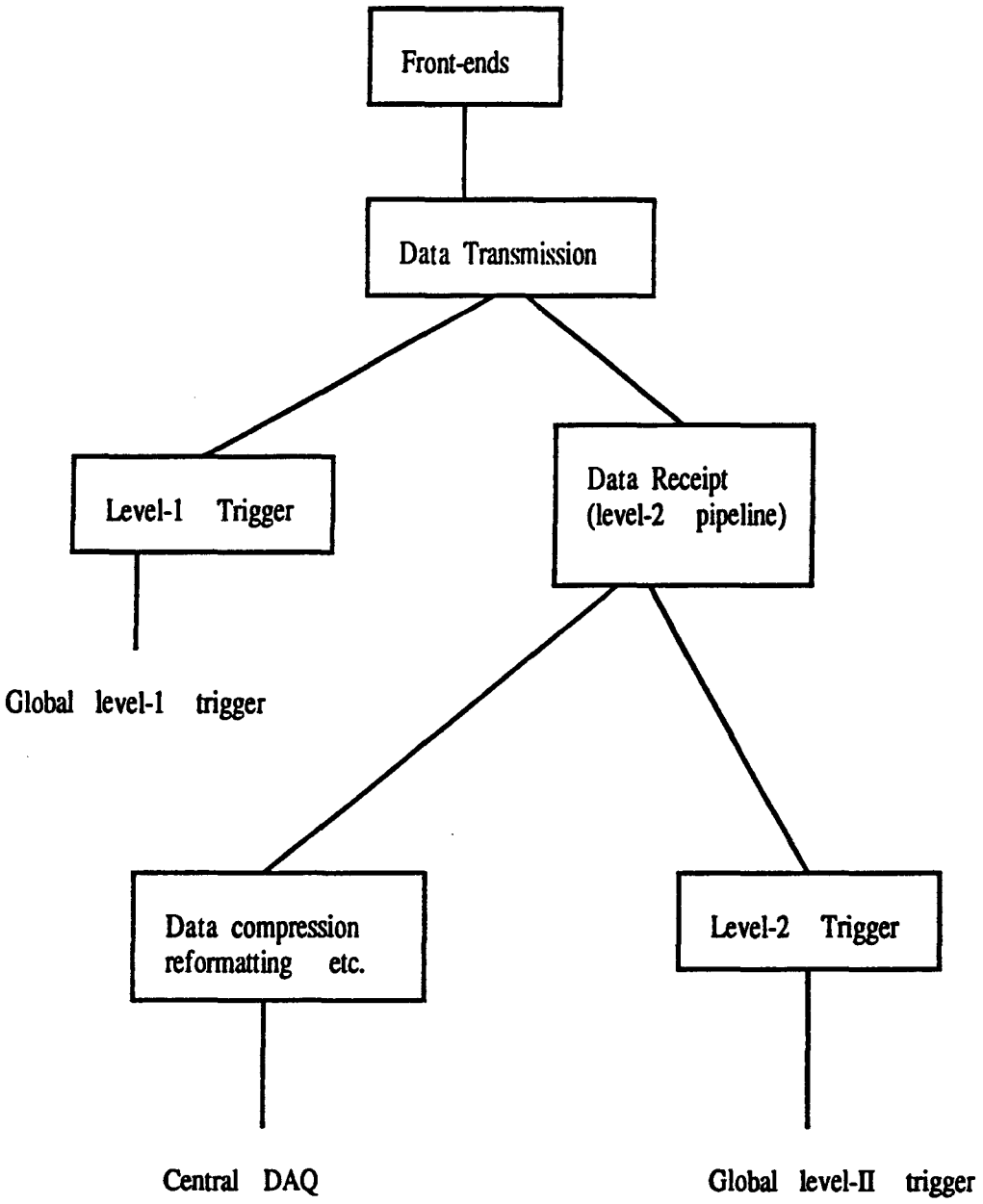


Fig. 51. DAQ chain.

The primary elements in the data receipt logic are the receivers and the Level-2 pipeline, which stores the data during the Level-2 trigger latency period. The Level-2 trigger influences the receiver logic, but is not considered further as an element in DAQ here.

The final element in the readout chain is the reformatting logic, which is the interface between the silicon Level-2 pipelines and the SDC general DAQ system. This system cannot be defined until the Level-3 processor farm protocols are understood. Its functions, executed under the control of the Level-3 farm, are reformatting and compression of data into the format used at Level-3; and interface to the control of the Level-2 pipelines.

The following sections describe the on and off detector DAQ elements in more detail. Selection of the data transmission technique drives both the front-end chip design and the data receipt logic, so it is considered first.

1. Data Rates

There are two important data rates. The first is the maximum mean rate that hits must be transferred from the detector; this determines the minimum bandwidth that any transmission scheme may have and in the case of a high degree of multiplexing is also an acceptable design bandwidth. The second is the rate at which data may be extracted from a single front-end chip; this limits the time it takes to read out an event. In the case that all the strips corresponding to a chip have hits the read-out time must be compatible with the Level-2 trigger requirements.

Hit rates are discussed elsewhere. Using 1% as the worst case maximum mean occupancy for Level-2 events yields

$$(\text{occupancy}) \times (\#\text{channels}) \times (\text{L} - 1\text{rate}) = 10^{-2} \times 128 \times 10^{5} = 128 \text{ kHz}$$

as the hit-rate per 128 channel read-out chip.

The maximum read-out time for any event must be much less than the 100 μs maximum Level-2 trigger decision period. For jets, where many strips might be hit in a single 128-wide region, this has a major effect on the system design. Data output from the chip must be either in parallel format, or in the case of serial data transmission a two-format data transmission scheme must be employed to ensure fast read-out. One format, used in the case of a high number of hits, is simply a hit-bit pattern. This ensures that for any event the maximum chip read-out time is 2 μs so that the event read-out time is dominated by the capability of the multiplexing scheme employed in data transmission. Assuming 63 MHz data transmission would limit the acceptable degree of multiplexing to of order 10 chips.

2. Transmission Schemes

Two data transmission schemes are under development. One employs printed aluminium cables to create a high degree of local multiplexing, routing the data into high-speed laser links. The second uses a highly parallel approach in which a 63 MHz LED driven fiber is dedicated to each front-end chip. Selection will be made on the basis of cost-benefit taking into account robustness and technical risk. Intermediate solutions involving fibers shared between a small number of front-end chips are also under evaluation.

2.1 Readout Using High Speed Fiber Drivers

In this scheme signals from a given detector segment are transmitted outside the detector by optical fibers operating at 300–500 Mbits/s after significant multiplexing. Since high speed optical transceivers tend to be power-hungry (due to the high-speed serialization circuitry) and bulky (compared to the strip readout ICs), they are situated at the outer radius of the Silicon Tracker volume. Signals from the individual detector segments are brought out radially to the optical transceivers by low-mass ribbon cables that carry both power and signals. Data on these lines are transmitted on a 12-bit wide bus at 30 or 60 Mbits/s (to be determined), which still allows rapid readout of high-density jets, which will tend to be concentrated in one module.

The bussing scheme within a barrel segment is shown in Fig. 52. Since only a limited number of readout ICs can be daisy-chained with reasonably sized on-chip drivers, Bus Selector Chips are used to organize the readout of no more than 15 readout ICs. These BSCs are also shown in Fig. 52. The segment bussing brings the signals to the end of the barrel, from which the cables are brought radially to the outer shell of the Silicon Tracker (a representative cable arrangement is shown in Fig. 53), where the optical transceivers are located. Bussing in the disks is organized in a similar manner.

Two possible options for the location of the optical transceivers are shown in Figs. 54a and b. Option 1 shows the transceivers at the end of the Silicon Tracker volume where they are accessible for maintenance. The second option reduces the lengths of metal transmission lines by placing the optical transceivers at the end of the barrel and at the outer radius of the disks. In the first option the metal lines would consist of two parts. Ultra-low-mass cabling would be used to bring the signals from the detector modules to the outer radius. At this point the larger available area allows the use of wider conductors with less dispersion, and a larger cable geometry (ribbon width and dielectric thickness scaled to preserve the characteristic impedance) can be used for the longer run to the end of the detector. A more detailed analysis of cable characteristics together with signal drivers and

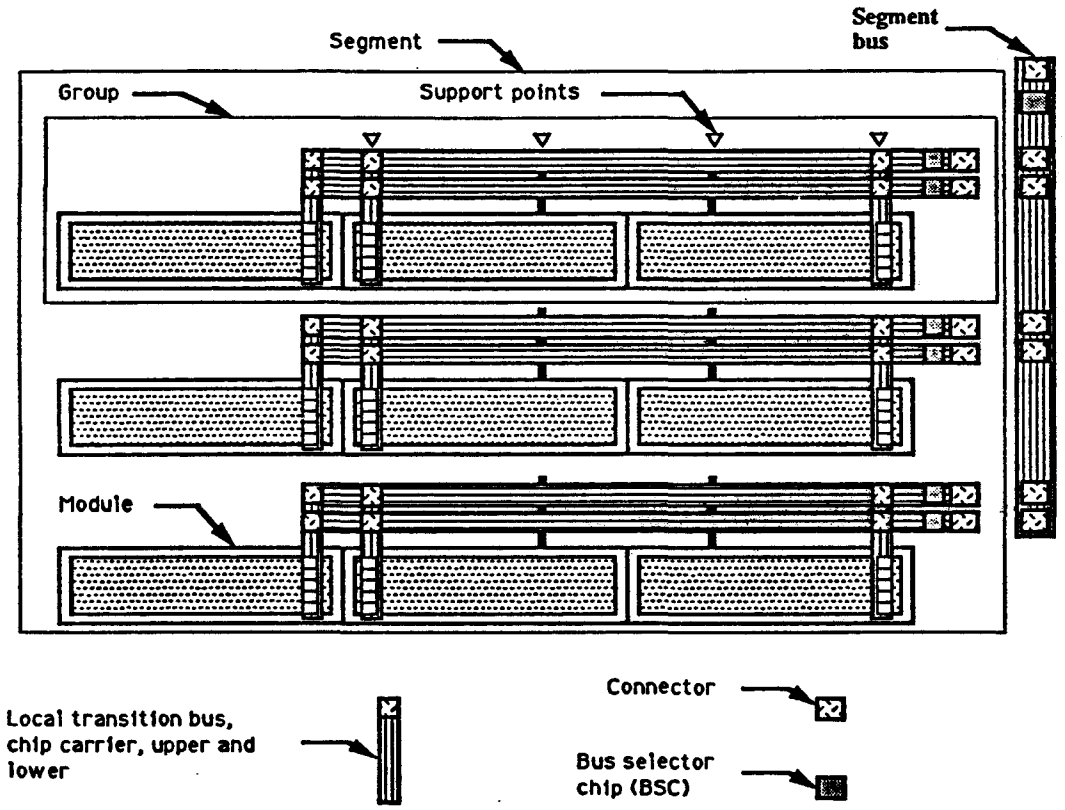


Fig. 52. Bussing scheme within a barrel segment.

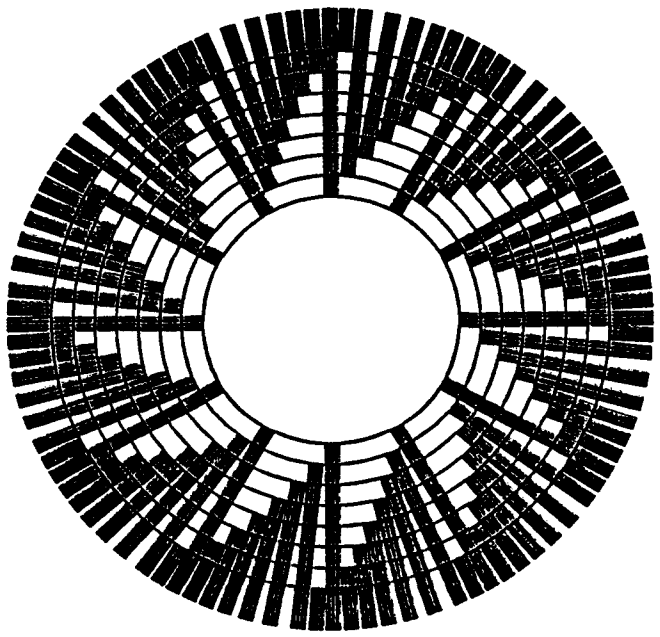


Fig. 53. Arrangement of ribbon cables from individual layer segments to the outer radius of the Silicon Tracker.

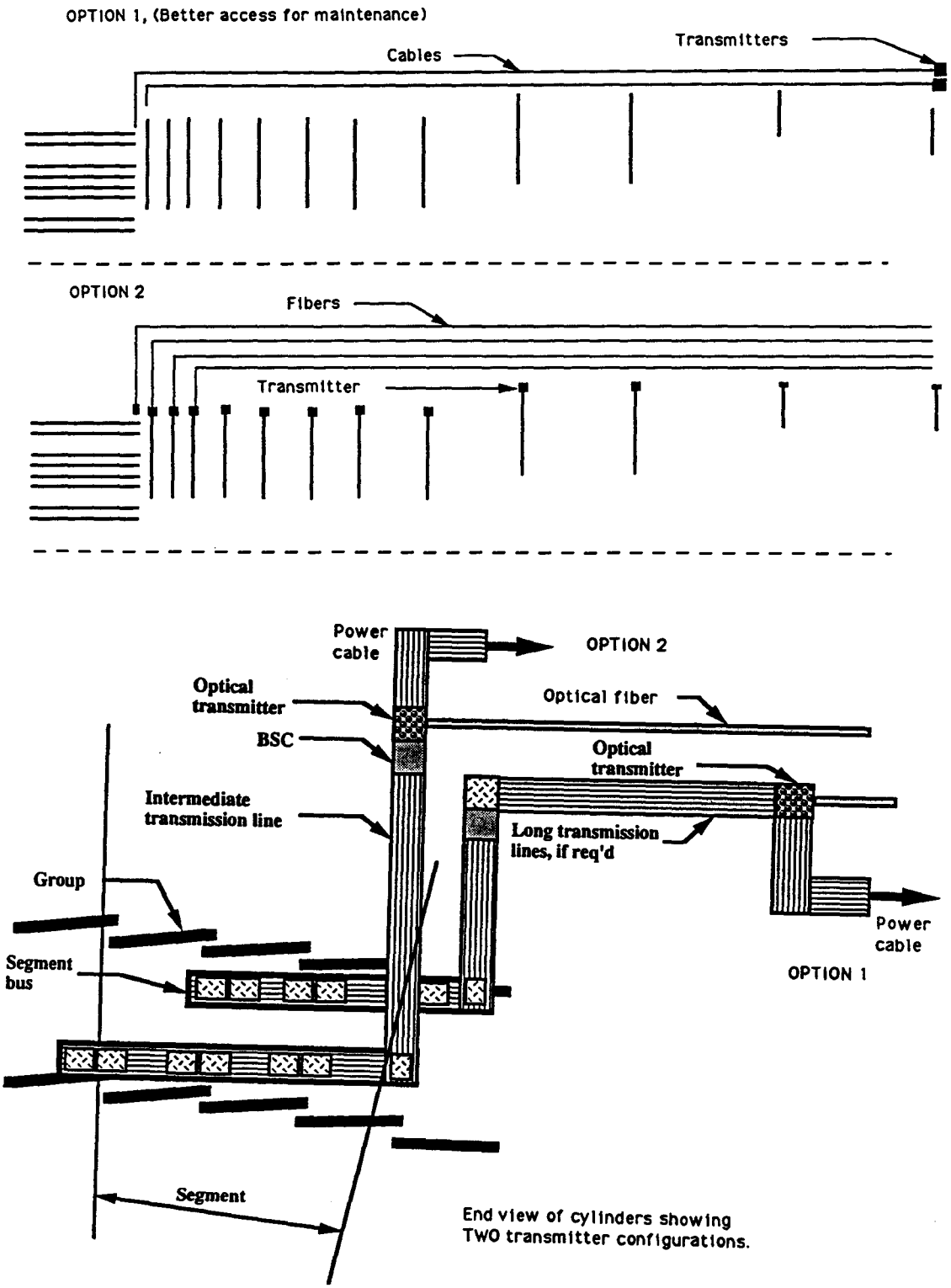


Fig. 54. Two options for the placement of the optical transceivers. a) a general layout. b) the arrangement of the data transmission ICs.

receivers is needed, but initially Option 1 seems feasible and is more attractive because of improved maintainability.

2.2 Readout Using Low Speed Drivers

LED driven links based on existing low-cost components are being developed. Links have been operated in a NRZ mode at 63 Mbit/s. Radiation tests done by the manufacturers show adequate resistance to neutron fluences up to $10^{14}/cm^2$ and almost no degradation with photon doses of 1 Mrad. Both LEDs and PIN diodes are radiation hard. The system is low mass; at the detector end the only drive circuitry required is the diode itself and possibly one bipolar transistor. These are surface mounted on a flex circuit, which is an integral part of a fiber harness containing a group of up to 16 fibers. In tests to date, the fiber to diode alignment was accomplished by a low-mass photo fabricated copper "block". Facilities are being upgraded to allow aluminium to be used, however even with copper, the total mass of the detector end system is a very small fraction of the silicon wafer thickness ($< 8\%$). Power consumption is negligible since the LEDs are off when not transmitting a one-bit and require of order 10 mW during one bit transmission. The estimated cost per unit bandwidth is less or comparable to high-speed links, in part because the alignment problem is much simplified.

The most robust scheme using such links involves associating one such fiber link with each front-end chip. The virtue of this is that the bussing of high speed signals is minimized, which simplifies the front-end DAQ architecture considerably and shunts any bandwidth limit to the off-detector systems, which can be upgraded if required. Such a system has a total bandwidth of approximately 3 Tbit/s and any event can be read out in a maximum of 2 μs using the two-format scheme (see below).

Control and clock signal are also routed into the detector on fibers. All control information is routed as serial control words through the L-1 trigger signal, which is not in use as an L-1 during control operations. A continuous string of 10 one-bits on the L-1 input is detected by the front-end chips and the following 8 bits interpreted as a control word. No high-speed signals are routed on electrical buses, which contain only the power and DC analog control levels. These buses are, therefore, simplified in comparison with the high-speed driver case, but are still required.

In addition to one read-out fiber per chip, each detector wafer has associated with it four incoming fibers. Two copies of the clock and two copies of the Level-1. These are translated to electrical signals and routed to the chips on the wafter (both sides) on a four line local bus. Each front-end chip uses all four signals, but (under external control) only one L-1 and one clock will be active at any time.

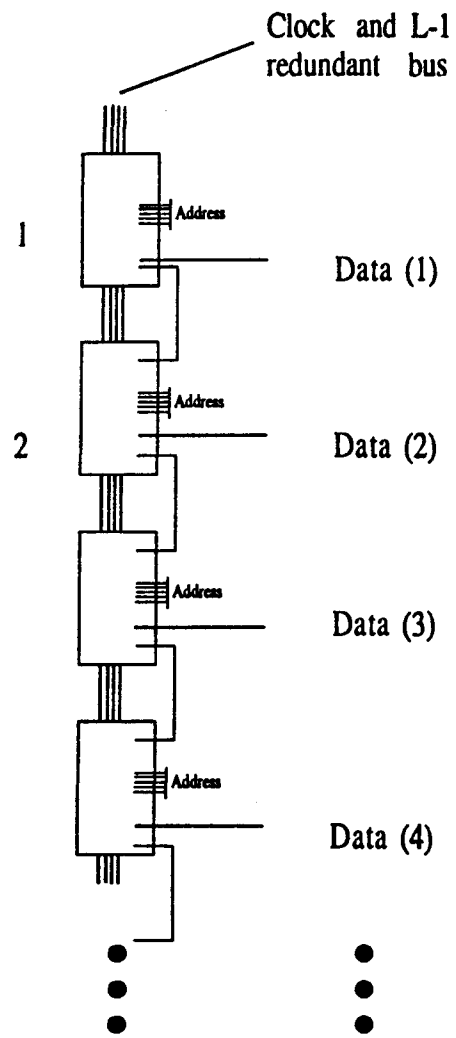


Fig. 55. Front-end connections.

The clock and L-1 are in common to all chips on a wafer; the redundancy in clock and L-1 is incorporated to increase system reliability. Failure of a read-out fiber in this highly parallel approach is not critical, since chips have connections to their neighbors, as shown in Fig. 55. In the case that a fiber fails, the data from a chip can be routed through the adjacent chip into the fiber that services it. This increases the maximum possible read-out time to 4 μs, but has no other impact on the system. Since the average chip is connected to two neighbors, this system is highly robust, requiring at least three failures before any significant impact on the system results.

In order to allow the routing of data in failure mode, the front-end chips must have an address localizing them on the L-1 (control) bus. This is shown in Fig. 55

as a bit pattern supplied from hard-wired local connections, but may be done differently in the final system.

It is possible to reduce the number of fibers by *a priori* having front-end chips share read-out fibers. Provided the degree of multiplexing is low enough that the multiplexing functions can be incorporated into the front-end chips, no assembly penalty results from this and the cost of fibers may be reduced. Clearly robustness and maximum event read-out time are adversely affected.

3. Off Detector DAQ

The fibers from the detector transfer the data to the off-detector receivers. After the receivers the data is in the form of parallel streams of asynchronous serially encoded data with a bit rate of 62.5 MHz. This is true independent of whether high-speed links are employed or not. The number of such streams is determined by the details of the data transmission scheme and does not affect the basic architecture of the rest of the DAQ chain. The model employed uses 10^4 input streams, which is at neither extreme of the possible fiber transmission schemes.

The first element in the chain is data receipt where the data is synchronized to the system clock (62.5 MHz), translated from serial to parallel format and stored in line receiver buffers. From here the information is grouped according to $\eta - \phi$ bins suited to the Level-2 trigger logic.(see section V.F). The fibers themselves have sufficient segmentation that information does not need to be moved on the basis of the hit location, but exclusively on the basis of the data stream from which it originated. Once collated the data is moved in parallel to both the Level-2 pipelines and the trigger system, which is designed to accept an asynchronous data stream.

Data in the Level-2 pipeline is either discarded or, in the case of a Level-2 accept moved to a Level-3 buffer, from which it goes to the processor farm under the control of the Level-3 trigger system. In between the Level-3 buffer and the Level-2 pipeline it may be necessary, or efficient, to include a data reformatting step. Any reformatting may be better accomplished in software using the farm so that this element has not been considered to date.

Further description requires the data format to be defined: Front-end chips service 128 strips. When transmitting data the front-end chips use one of two formats. If the number of hits within the group of 128 is less than 10, hit addresses are encoded and transmitted serially. In the case of more than 10 hits, a string of 128 bits is sent, with the hit locations set to 1 within the string. This format ensures that the maximum time required by a front-end chip to transmit data for an event is 2 μs. Every chip sends a header word in response to a Level-1 trigger which starts with a marker, is followed by a format defining bit, and a 7-bit code

giving the number of data words (which may be zero). The multiplexing scheme collects such strings and uses the same format in transmitting the data, adding a chip address to each word group and to each 128-bit group, but eliminating zero word headers. In the case of no data in multiplex branch a header is sent with a zero word count. When data is present the header contains the number of active front-end chips, in exact analogy to the front-end chip format. This format is one of several considered; it does not minimize the number of words that need to be transferred, but considerably simplifies several issues associated with identifying to which L-1 trigger data belongs. It also maximizes the independence of the elements in the DAQ chain, which results in a conceptually simple system with a minimum of control problems.

Figure 56 shows a block diagram of the data receipt logic for one input data stream. The data is first synchronized with the system clock. This is accomplished by routing the data stream through a variable number of buffer gates under the control of a phase sensing circuit. The length of the fibers and delays through any logic prior to this circuit are rendered irrelevant by this step since the transmission is asynchronous. The only necessary condition is that the data stream and fiber logic is driven by the same clock as the rest of the DAQ system.

After synchronization, the data is directed into a shift register; the readout process is started when a non-zero bit is detected and the number of chip data sets to record is split off for control purposes. Each group of words is shifted in serially and moved to the line buffer as a parallel word with the address expanded to include the chip address. Each 128-bit hit pattern is encoded as addresses and shifted to the buffer so that after the last chip group has been read in, all the hits corresponding to one event in the area serviced by the data stream are stored in the line buffer.

When all the data for an event has been read in, an entry is made in the event stack containing the number of data words and the starting location in the buffer. Events with no hits also result in an entry, but the starting location is a code indicating no data.

Line buffers share an output data bus inside the receiver chips and buffers corresponding to a trigger η–ϕ region share a data bus across chips. Data is moved to the Level-2 trigger and to the L-2 pipelines simultaneously along this bus under local control. Data from all stacks must be shifted before any stack is repeated to ensure events are properly aligned: Since all L-1 triggers are processed sequentially, if an event stack has any complete events recorded, the oldest one is the next to be processed. All stacks will contain data for each event since zero word headers are written.

Data remains in the Level-2 pipeline, stored as complete events by $\eta - \phi$ region

(One channel in ASIC shown)

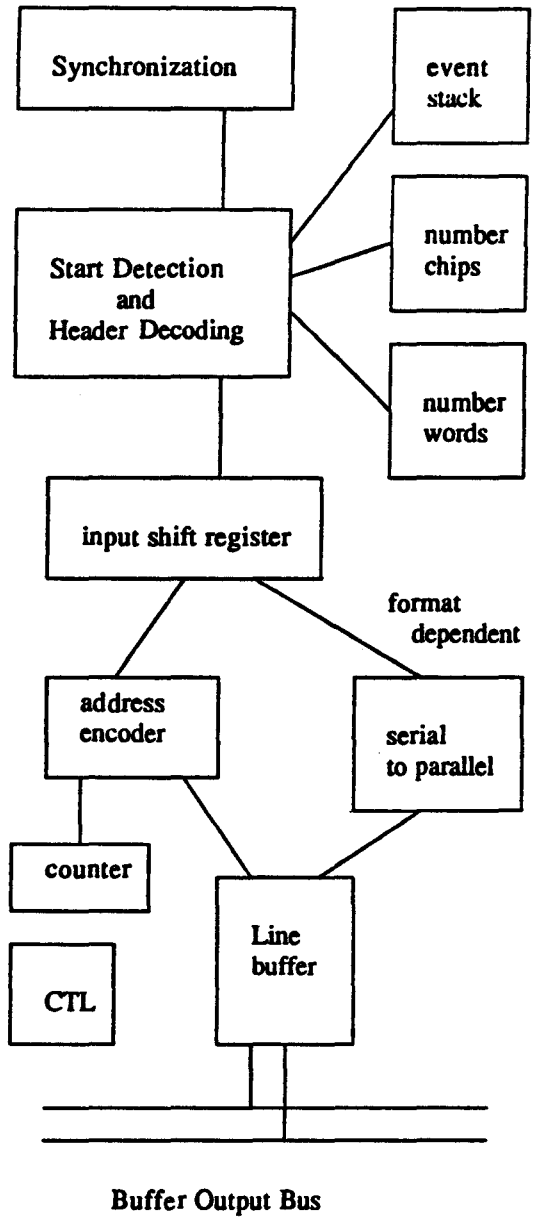


Fig. 56. Data receipt.

until the Level-2 reject or accept is received. These arrive in order, so that the oldest event is either shunted to the Level-3 buffer or discarded. From the Level-3 buffer the data is moved synchronously to the processor farm.

Physically the hardware is an integral part of the silicon Level-2 trigger processor and housed in the same SDC standard crates.

F. Triggering

Trigger studies are emphasizing the reconstruction of high transverse momentum tracks for a second-level trigger. This requires readout of the silicon after a first-level trigger. A specific second-level trigger scheme using hit patterns has been defined and an estimate of the number of trigger cards completed. This scheme will be looked at carefully, including simulation studies, next year. At lower priority, schemes for generating a contribution to the first-level trigger are also under study.

Using the ϕ measurements in the silicon a momentum resolution of $\sigma_{P_\perp}/P_\perp^2 \simeq 1$ (TeV^{-1}) is possible using the full granularity of the detectors. Thus, given the trigger goals which are 5 (second level) to 10 (first level) times less demanding, the trigger could use groupings of strips. To use the full granularity of the strip detector requires accurate centering of the detector on the interaction point to a precision on the order of a strip width. This issue needs to be looked at more carefully. The use of all of the detector tracking devices together would allow substantial relaxation of the centering requirement. In the discussion below we assume that we will want to use the full silicon precision.

1. Second-Level Trigger – General Principles

The second-level trigger of SDC is designed to accept an input rate of up to 10^5 Hz. Data from the silicon tracker in the form of a list of hit strip numbers is multiplexed up to the processors on optical fibers. The data from a given first-level trigger is completely assembled within about 2 μs of the first-level trigger being issued.

The second-level trigger for the silicon tracker is based on simple pattern recognition algorithms operating on tables of hit positions in a two-dimensional space. In the case of the barrel silicon modules the two dimensions are the radial distance of the silicon layer from the origin and the azimuthal angle ϕ. In order to utilize the full precision of the silicon detector while keeping the amount of hardware to a minimum we adopt a two-stage approach to the pattern recognition problem. We first attempt to recognize regions of interest in the table by means of a "coarse scan". Having established areas of the two-dimensional space likely to contain high $P_\perp$ tracks, we then carry out a second, "fine scan", in which these areas are examined with the full granularity of the silicon detector. This allows a high precision

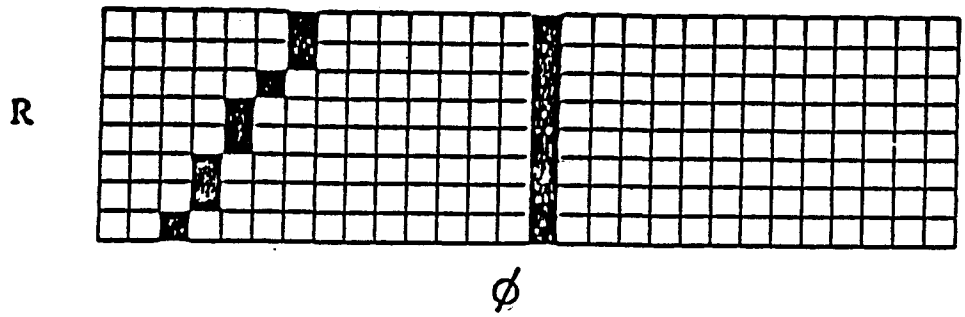


Fig. 57. Schematic showing the appearance of two-dimensional tables from the second-level trigger in the barrel region. The left pattern shows the expectation from a track with low transverse momentum, the right pattern one from a track with very high transverse momentum.

measurement of the transverse momentum of those tracks found by the pattern recognition.

In the coarse scan the data from the barrel region is tabulated in 1920 bins in ϕ. This bin size is chosen to approximately match the ϕ granularity of the calorimeter and to keep the number of inputs to the processors to a manageable number while maintaining good resolution in transverse momentum. The two-dimensional table is formed by combining the 1920 bins from 8 layers of the silicon ordered by increasing radius. Clearly in such a table high transverse momentum tracks have a very small or zero variation in ϕ bin as a function of radius, whereas low $P_\perp$ tracks bend considerably as they pass through the eight silicon layers. Typical resultant patterns from low and high $P_\perp$ tracks are shown in Fig. 57. The trigger processors must be able to discriminate between the presence of a track and of random noise in the table and, in addition, to discriminate between high and low transverse momentum tracks. In the conceptually simple case of infinite $P_\perp$ and full efficiency in each layer of silicon, this problem reduces to being able to recognize tables with eight hits in the same ϕ bin. Allowance for inefficiency and for finite $P_\perp$ requires somewhat more complicated algorithms, but clearly the pattern recognition problem is at least conceptually rather simple.

An almost identical approach is used for the endcap modules of the silicon detector, except that, rather than filling a table of ϕ versus radius of the silicon layer, we construct a table of ϕ against z, the distance along the beam line. The same granularity in ϕ is used as for the barrel. Again, high transverse momentum tracks have a small variation in ϕ as z changes, whereas low $P_\perp$ tracks curve considerably. The pattern recognition problem is therefore exactly analogous to

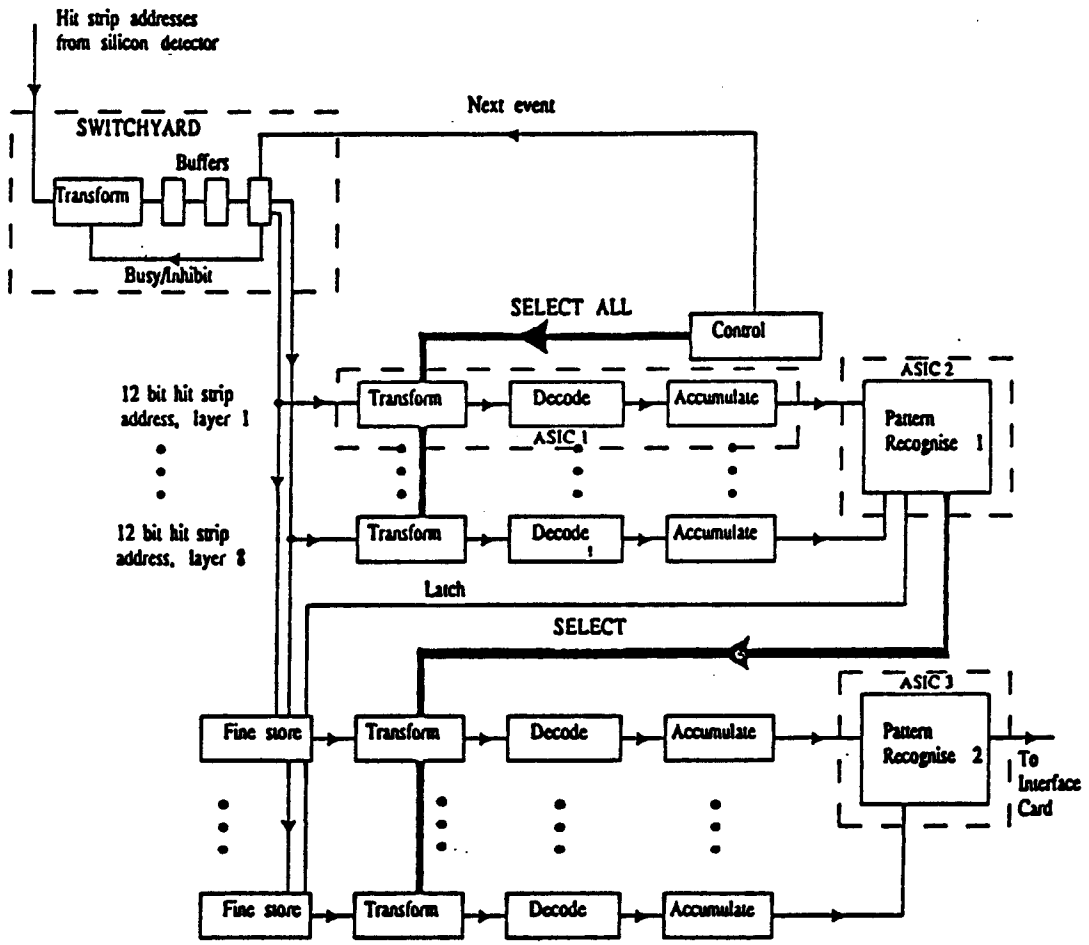


Fig. 58. Block diagram showing the main elements of the second-level trigger. The switchyard module shown at the top left directs the hit strip data to the appropriate processor cards. The remainder of the figure shows the processing on one half of a PRC module. The areas enclosed in dashed lines and labelled ASIC1, 2 and 3 indicate the parts of the logic which could profitably be manufactured as ASICs.

that in the barrel once the z versus ϕ table has been constructed, so that identical trigger processors can be used. The case of tracks which cross the barrel-forward interface needs further study and is an important class of tracks.

In both the barrel and endcap modules there is a further subdivision of the data in bins of pseudorapidity η. These bins correspond in the barrel to the length of silicon wafers bonded together to form a readout unit which is expected to be two wafers. This η subdivision is somewhat coarser than that of the calorimeter, but should still allow satisfactory matching of tracking information and energy deposition.

2. Second-Level Trigger – Possible Hardware Implementation

Having described the general outline of the approach to triggering which we intend to use, we now proceed to give some details on possible implementation in hardware. In Fig. 58 we show a block diagram of the Pattern Recognition Card (PRC), the main trigger processing card in the system. The tables will be filled in overlapping sectors of 64 ϕ bins and a PRC will bring together the one-dimensional tables of this ϕ sector from each of the 8 layers of the barrel silicon detector. (An analogous layout obtains for the endcap modules, but for simplicity we will discuss only the barrel here.) Currently we envisage that two such ϕ sectors will be processed on each PRC.

The data carried on optical fibers leaving the detector will be split, one copy being stored in a Level-2 pipeline, while the other is routed to a "switchyard". This module will reformat the hit strip address as a 12 bit number representing its value in increasing $\Delta\phi$ in this sector and then store it in one of a small number of buffer stores designed to derandomize the input rate. When the input circuitry on the PRC is ready, the switchyard will drive an internal bus on the crate down which the data on hit strips will be distributed to those cards requiring it. We would expect each switchyard module to handle the data from about 100 optical fibers, corresponding to half of the total ϕ coverage in one of 6 η bins.

On the receipt at the PRC the data from the switchyard is simultaneously written to the coarse scan tabulation circuit and to a data store ready for a possible fine scan. The tabulation circuit has three main functions. The hit address is first transformed into a bin number with the appropriate granularity. This part of the circuitry also responds to select lines indicating which ranges of addresses are to be transformed and passed on. In the case of the coarse scan, the full range of data is selected. The second stage of processing is a 6:64 line decoder which then passes the data on to the final stage accumulate. This is controlled by a New/Accumulate control signal which ensures that only data associated with a particular first-level trigger is examined. While the Accumulate signal is asserted any bit which becomes set in the register remains set until the New signal is asserted. When all hits from this Level-1 event have arrived at the processor, the control logic enables the next stage of processing, PR1.

The Pattern Recognize 1 (PR1) circuitry applies a simple pattern recognition algorithm to the 8×64 table produced by the tabulation circuit. A simple case which we have examined in Monte Carlo simulation would recognize a good track by asking for 6 out of 8 possible hits in r in a two-column wide mask in ϕ. Such a mask with the granularity proposed here begins to become efficient at a $P_\perp$ greater than about 15 GeV/c. The block of data satisfying a PR1 mask can then be passed on to the Pattern Recognize 2 circuitry for the fine scan to be implemented. This

is achieved by using the ϕ address of the PR1 mask to set select lines. The data from the fine scan store is strobed into the transform circuit and those addresses lying within the $\Delta\phi$ of the accepted PR1 mask as specified by the select lines are decoded and accumulated into a fine scan table. This tabulation circuit is identical to that used in the coarse scan. On the receipt of a New signal the data, which has the full granularity of the silicon detector, is latched into the PR2 circuit.

The PR2 circuitry needs to be considerably more complex than for PR1. A rather wide mask is required in order to have good efficiency for tracks with $P_\perp$ near the threshold of the PR1 circuit. In addition, at this point it would be advantageous to have rather complex algorithms more sensitive, for instance, to photons converting in the detector. This can be done by recognizing patterns with missing hits in the innermost silicon layers. Tracks satisfying the PR2 algorithm would be output with their measured $P_\perp$ to an interface card in each crate. Here the found tracks would be parametrized and forwarded to the global second-level trigger processor where they would be integrated with other tracking detector and calorimeter information to form an overall trigger decision.

The non-standard elements of the PRC hardware are the decode/accumulate function of the tabulate circuitry and the elements of the PR1 and PR2 circuits. For the decode/accumulate function we propose to use one of the Xilinx family of user programmable gate arrays. These have an architecture similar to that of standard gate arrays, with the important difference that configuration of the internal logic, input/output pins and routing are controlled by on-chip static memories. These can be reconfigured via a serial link in about 20 ms. These devices are rated at speeds up to 100 MHz. For the simple pattern recognition required in PR1 it should be possible to use a 64 k RAM lookup table into which the date could be multiplexed. This size of RAM can accommodate all the possibilities of a 2×8 bit mask. However, this solution seems out of the question for more complicated masks for PR1 and certainly for the functions of PR2, since the size of RAM required rapidly becomes prohibitive. For the PR2 function a novel solution would seem to be required in order to fully utilize the precision and granularity of the silicon detector.

In the framework of the two-step approach outlined above, other hardware solutions can be implemented, which preserve the basic logic design and can replace part of the PRC card, especially as far as the PR1 and PR2 sections are concerned. Their pattern recognition function can be accomplished using a Pattern Matching technique, *i.e.*, comparing the incoming stream of hit addresses with a known, precomputed sample of hit patterns, thus identifying the matching configurations. Each pattern would correspond to a physical track of known transverse momentum. In order to perform this task in the time constraint of the Level-2 trigger,

one can use the Associative Memory chip (AMchip) [34] developed at Pisa-INFN. The AMchip behaves as a Content Addressable Memory, but features an internal circuitry which allows the comparison of the stream of incoming 12-bit addresses with the pre-loaded patterns to take place on the fly, thus avoiding the problem of combinatorics which would be unaffordable in a crowded multi-hit environment such as ours. All the AMchips in a system can be loaded in parallel with incoming data, in much the same way as the PRC card is, and as soon as the last data have been input, they are ready to be read out and to give as output a series of pointers to a subsequent RAM which holds the tracks' parameters. The existing version of the chip can be loaded at a frequency of 25 MHz, and has been designed to allow the recognition of patterns with any number of missing hits to allow for inefficiencies. The number of different patterns which can be pre-loaded in the AMchip system (which is a measure of the capability of the system to recognize tracks of lower momentum) only affects the "memory size" of the system, *i.e.*, the number of AMchips needed, and not the address field of the AMchip itself, which in our case would remain fixed at 8×12 bits. For these reasons, this approach could be a satisfactory solution to the problem of the complexity hidden in PR2 (or even PR1). Studies are under way to establish the feasibility of this approach in terms of chip count and efficiency, and to optimize the matching of the AMchip operation with the PRC card.

The second-level trigger for the silicon detector based on the scheme we outlined above is both powerful and flexible. It allows the full granularity and momentum resolution of the detector to be utilized at an early stage in the trigger. It provides a powerful aid in rejecting photon conversions which form the main background to electron triggers at the first level. It seems possible that the required processing can be achieved within the average time separating SDC first-level triggers, although a much more detailed timing simulation will be necessary before this type of detail can be finalized. However, even if this is not possible and some pipelining is necessary, then this is easy to implement given the modular nature of the PRC.

The flexibility inherent in the processor is again a consequence of its modular nature. For instance, the PRC can be simplified by using a pair of PR1 circuits rather than developing the more complex PR2. However, this clearly degrades the $P_\perp$ resolution of the trigger. Alternatively, a relatively simple PR2 unit can be developed initially and replaced by a more complex upgrade. The granularity of the system can also be changed easily. We use a 12 bit strip address rather than the 11 bits which are adequate for the ϕ granularity proposed. This allows the system to operate with double the final granularity and therefore half the hardware.

Our current estimate is that the triggering system can be built in approximately 12 crates. Most of the PRC functionality, with the exception of the PR2 circuit,

could be built with commercially available components. Indeed, several elements, particularly the tabulation and PR1 circuits, are very similar to electronics which has been developed for the ZEUS Central Tracking Detector First Level Trigger. However, it would almost certainly be cost effective to develop ASICs for the three major functional elements described above. Clearly a specification for the PR2 function and for these ASICs as well as the overall system layout will require extensive Monte Carlo simulation work which is now under way.

VI. Mechanical Engineering and Design

A. Silicon Detector Arrangement

The silicon tracking system (STS) is composed of silicon wafers arranged both in a cylindrical array and an array of flat panels centered on the beampipe. The cylindrical array is referred to as the central or barrel region and the flat panel arrays, which are normal to the beam axis, are referred to as the forward regions. The overall length is 5.2 m, and the outer diameter, including the shell enclosure is approximately 1.2 m. Figure 59 depicts the design without the structural support.

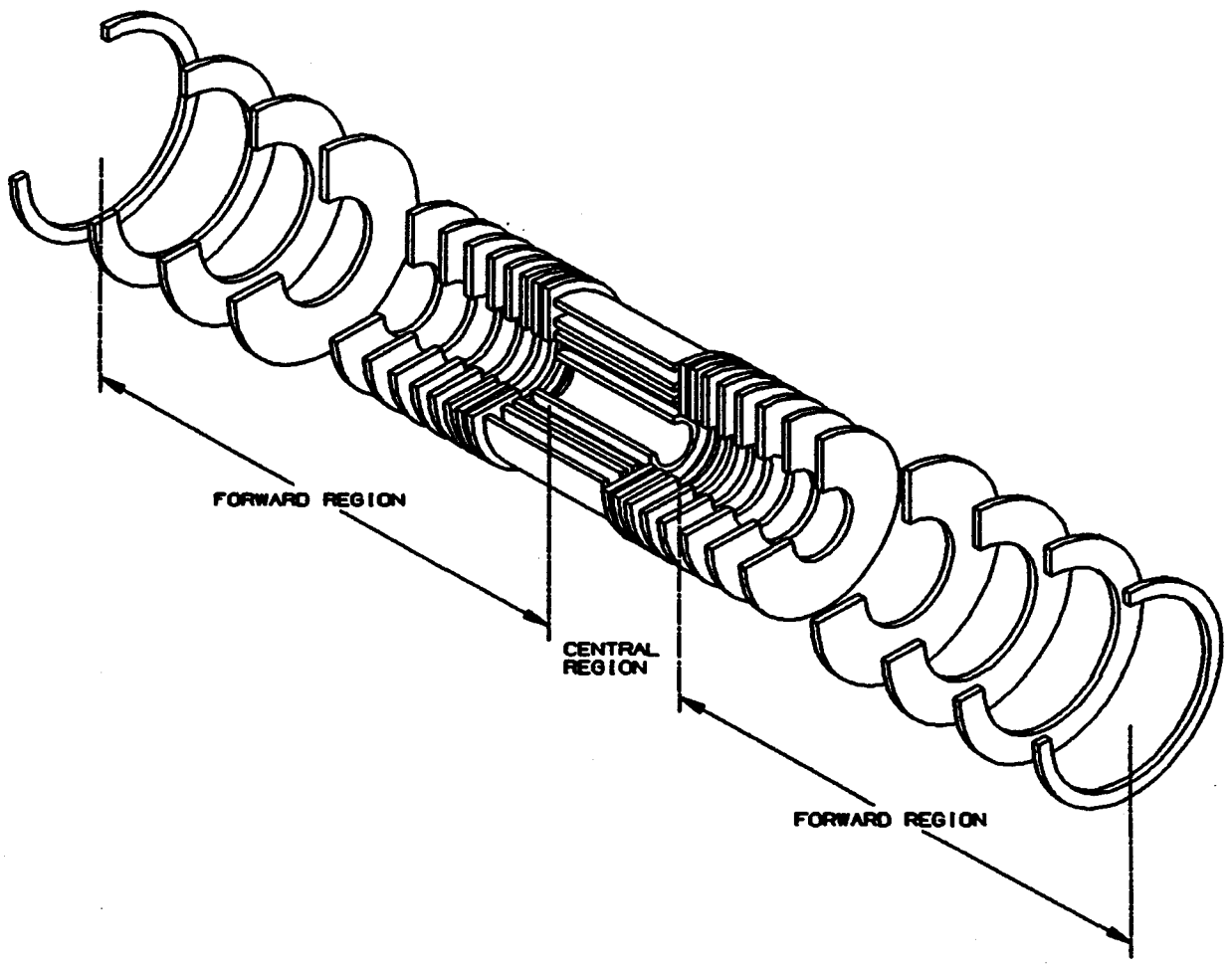


Fig. 59. Silicon detector array.

The current STS is considerably different from the version described in an

earlier Los Alamos report [35]. Much of the design and analysis performed on that system, however, are germane to the current system under study, hence that report may be consulted if the evolution of the current design is sought.

1. System Design Requirements

The STS baseline design arrangement is shown in Fig. 60, while the baseline design requirements are listed in Table 19. The stability requirements are quite stringent when one considers the overall detector size, thermal heat load, and the potential effects of the radiation environment on material properties. The requirement to use the absolute minimal amount of material for the support and service structures is also a rigorous design constraint.

2. Mechanical Design Considerations

The method chosen for supporting the individual barrel silicon layers combines adjacent layers into superlayers. Two such layers can be supported separately as a pair. This provision offers the potential for minimizing the structural support material, hence minimizing the effective percentage radiation length. For each layer, a maximum active detector strip length of 12 cm was chosen based on strip detector performance considerations. Two 6-cm detectors are electrically connected to form a 12-cm active strip length. Four, 300-μm-thick, silicon detectors are edge-bonded together to effectively form a ladder. Electronics for powering the strips and data readouts are mounted at each end of the ladder assembly. The silicon ladder unit is stiffened by edge bonding two ultra-thin graphite/epoxy strips along the length of the detector edges. A drawing of this concept is shown in Fig. 61. It is intended that these individual detector ladder assemblies be structurally robust in order that they can be assembled and pretested without danger of damage.

The silicon ladder assemblies are bonded to structural rings made from graphite/epoxy. A silicon wafer shell assembly is illustrated in Fig. 62. The rings, hereafter denoted as cooling rings, in addition to providing structural support, provide a passage for an internal heat pipe wick/artery structure. A hydrocarbon working fluid is wicked to an area as close as practical to the electronic heat load. Heat flows through the thin-walled composite cooling ring and evaporates the cooling medium. The baseline design uses butane as the working fluid. An in-depth discussion of this can be found in section VI.E.3.

This evaporative cooling technique greatly simplifies the process of cooling the enormous number of individual wafers. The heat flux associated with the wafer electronic package can be effectively handled with a minimum temperature gradient by minimizing the conductive path. Distortions in the silicon shell substructure are avoided by minimizing the thermal gradient and through an appropriate material choice for the cooling ring. Because the silicon subassembly will be operated

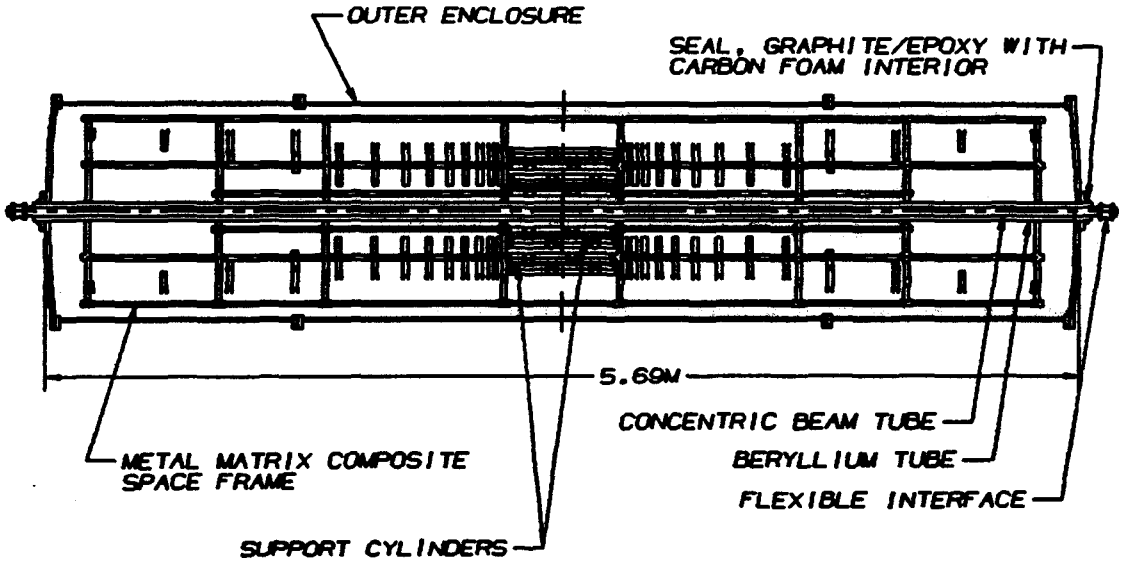


Fig. 60. Baseline silicon tracking system arrangement layout.

Table 19. Baseline Design Requirements

Detector Characteristics	Silicon, longstrip technology 50 μm pitch, double-sided
Detector Assembly	Maximum module length, 24 cm Maximum readout unit length, 12 cm Individual wafers edge bonded, 300 μm thickness, Maximum wafer length, 6 cm. Mounting precision: R, Rϕ, Z - 80, 25, 250μm Angular, 1 milliradian Positional stability: R, Rϕ, Z - 80, 5, 250μm Angular, 0.2 milliradian Detector cant angle, 7.4° Operational temperature, 0°C
Detector heat load	Heat flux, 1.33 W/cm^2 12 kW Total, providing safety factor of 2 over expected value.
Radiation exposure	10 Mrads over 10 year service life No measurable stability effects >5 μm
Material radiation length budget	Structure and related service connections 3% (except in limited regions e.g., transition from central to forward)

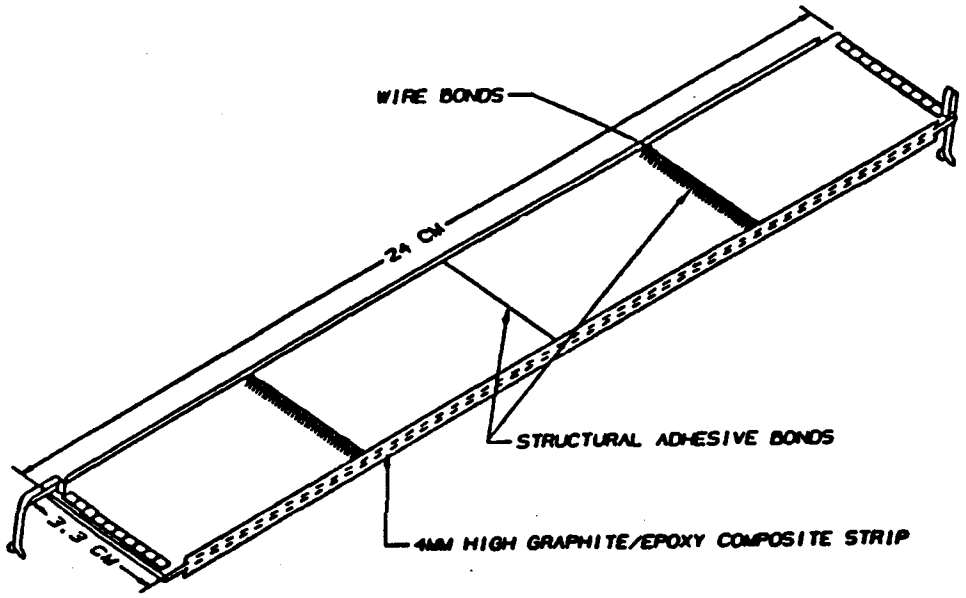


Fig. 61. Silicon wafer module with wire and adhesive bonds and graphite/epoxy composite edge-strip reinforcement.

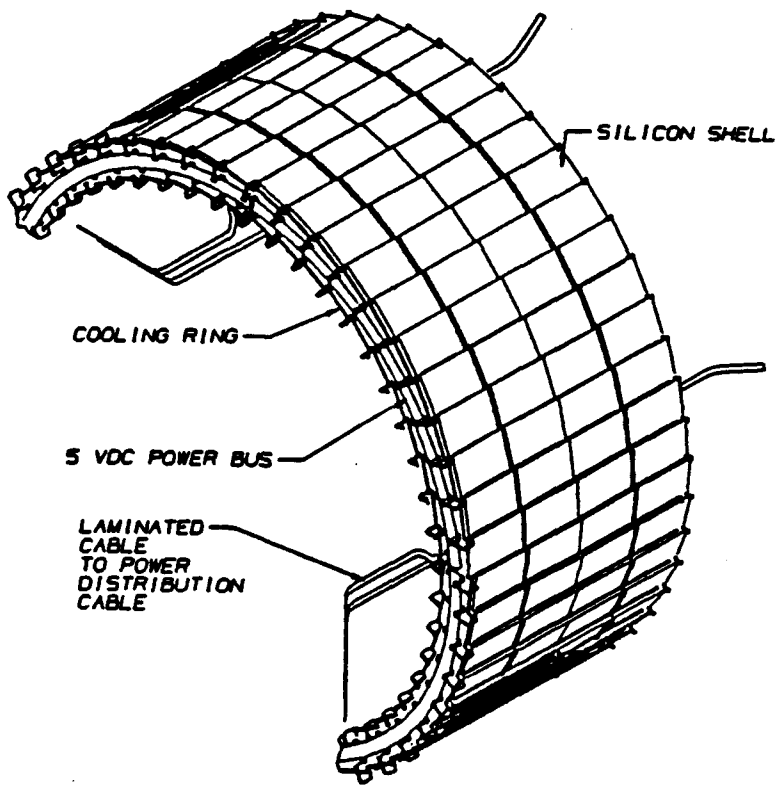


Fig. 62. Silicon wafer shell assembly demonstrating cooling rings, power bus, and cabling.

at temperatures well below room temperature, coefficients of thermal expansion (CTE) for materials composing this assembly must be carefully selected and tailored to match that of silicon. This will further avoid undesirable distortion.

The silicon shell assemblies are mounted onto the composite shell support structure of the silicon detector central region. These assemblies are supported on kinematic supports to avoid introducing distortions and can be seen in Figs. 63 and 64. The plan is to use a shell support structure material such as graphite/epoxy or a metal matrix composite (MMC) that can be engineered to exhibit a zero CTE. Factors that enter into the final selection process are discussed in section VI.D.

Silicon ladder modules are also planned for the forward detector regions. In this instance, the ladders are pie-shaped to fit as individual arc sectors. The technique envisioned for cooling the silicon wafer module electronics would be evaporative as previously discussed. Cooling rings, which support pie-shaped silicon layers, must track the contraction of the silicon or they will introduce the possibility of distortion. Our calculations show that the CTEs of the cooling ring and silicon must match to avoid wafer distortion. The plan for achieving the desired CTE equality is to tailor the expansivity of a graphite/epoxy composite to match that of silicon. Prototypes of the envisioned ring construction techniques are discussed in section VI.C.2.

The central and forward detector regions will be supported by a frame network that must have high dimensional stability throughout the life of the detector. Problems which must be considered are

- thermal distortion,
- physical property changes due to radiation effects and/or chemical attack from the heat pipe working fluid, and
- creep.

Also, radiation length restrictions must be considered in formulating the design. For the baseline design concept, an open, lightweight space frame structure was chosen. This was done specifically to minimize the percentage effective radiation length. The space frame network would be assembled in sub-sections to provide a natural jigging fixture when assembling the silicon subassemblies. The present plan would be to assemble the central detector region first, and then add the adjacent forward regions. The modular construction will also make assembly and servicing of the STS much easier. It would be possible to support this assembly inside the external shell structure on support points that will later become the nominal quarter-points. The outboard forward regions would be cantilevered off the first assembly. The actual support locations will be set after determining the distribution of mass in the longitudinal direction for the entire assembly.

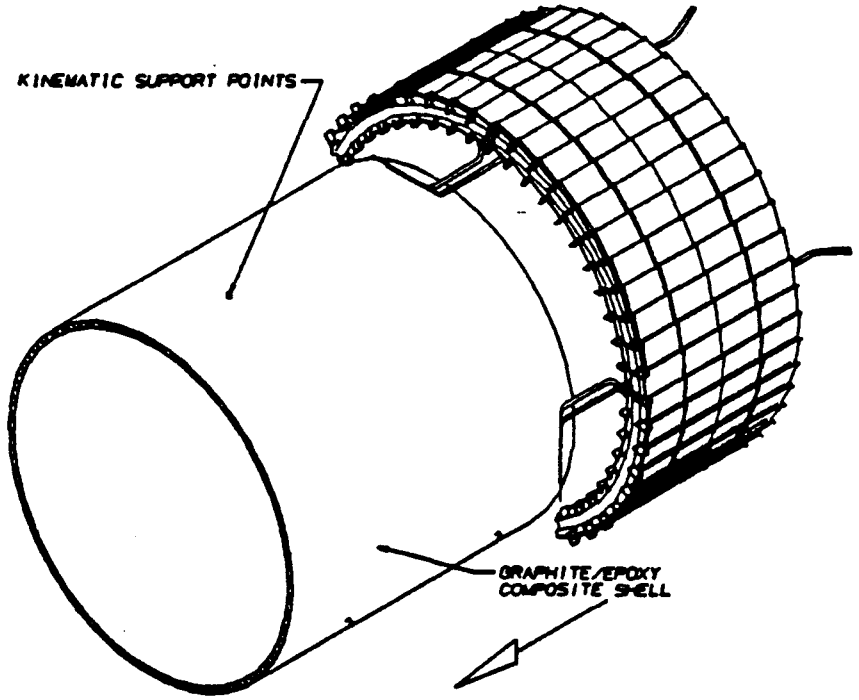


Fig. 63. Mounting the wafer shell assembly to the graphite/epoxy sandwich shell.

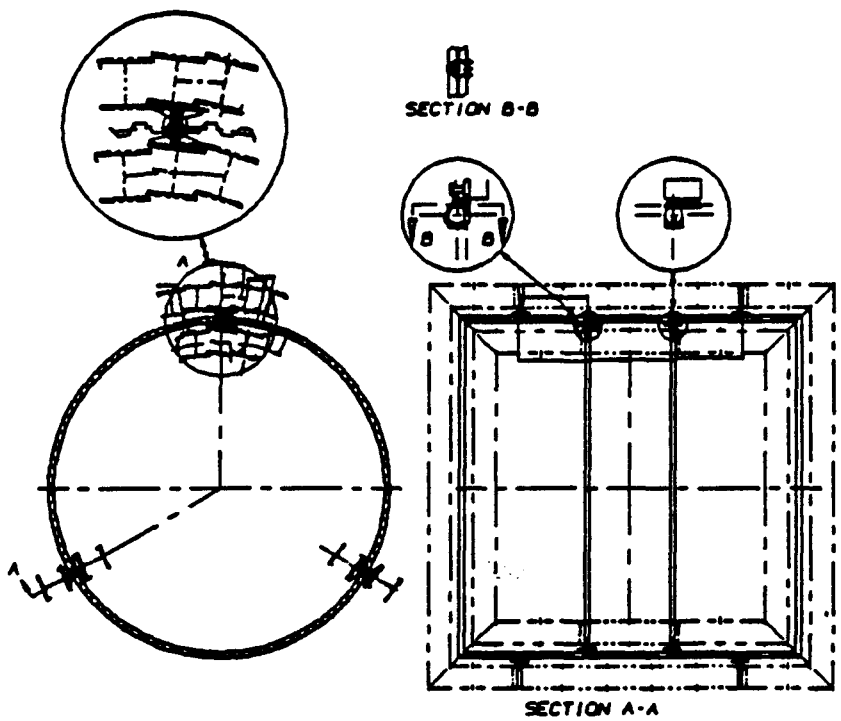


Fig. 64. Central region kinematic mounts.

The entire silicon tracking subsystem will be enclosed in a vessel capable of withstanding small differential pressure during butane filling or evacuation, as discussed in section VI.D.3. Kinematic supports will be used to mechanically isolate the silicon tracking subsystem from the shell external pressure load. Overly constraining, non-kinematic, rigid supports between the shell and the ultra-lightweight silicon detector support structure would cause severe localized distortions and unpredictable movement. To insure 5 μm stability, these external loads must be isolated. The baseline design approach for the external enclosure is a sandwich graphite composite that is very lightweight. Beryllium is an alternative material choice for this enclosure.

B. Materials Options

In most design applications many factors are considered in material selection. However, the material selection for the silicon tracking subsystem is driven by three primary factors:

1. 5-μm platform stability,
2. radiation length restrictions for the structure, cooling, etc., and
3. radiation resistance in the presence of hydrocarbon fluids.

Our preliminary studies have shown that achieving these goals will require the application of state-of-the-art material composites which have high stiffness-to-weight ratios.

Table 20 summarizes pertinent data for candidate materials for the structures under investigation. If material specific stiffness were a singularly important attribute, then boron carbide would be an ideal candidate. It is radiation hard and shows no evidence of creep under load. However, the material is brittle and exceedingly hard. Attainment of precise geometric shapes would be difficult and expensive. Another factor that detracts from its choice for this application is its modest radiation length.

Graphite/epoxy composites have specific stiffnesses slightly higher than beryllium as indicated in Table 20. However, the value quoted is for unidirectional properties. Structural panels composed of individual graphite/epoxy plies with fiber orientations arranged to achieve quasi-isotropic properties, have noticeably lower stiffness properties (see Table 21). The STS can effectively use both composite property classes, that is, unidirectional and quasi-isotropic. The internal truss space frame is an example of the use of a unidirectional laminate. However, a zero CTE in the direction of the truss member is desired. Achieving this goal requires a trade-off in fiber properties and fiber-to-epoxy matrix volume fraction.

Table 20. Selected Material Properties.

Material	Elastic Modulus E (GPa)	Density ρ (g/cm^3)	Specific Stiffness E/ρ (10^8cm)	CTE α (ppm/K)	Thermal Conductivity k (W/m-K)	Specific Heat C_p (J/g-K)	Radiation Length L_R (cm)
			Material Candidates				
Beryllium	290.0	1.84	16.08	11.60	146.0	1.88	35.43
Boron Carbide	448.2	2.52	18.15	4.73	43.0	0.90	19.90
Carbon/Carbon[a]	152.0	1.90	8.16	0.10	246.0	1.00	18.80
Graphite/Epoxy[b]	311.7	1.68	20.00	−1.13	46.2	0.92	25.00
Mg-MMC[c]	190.3	2.03	9.56	−0.35	412.0	1.00	16.80
Al-MMC[c]	196.5	2.39	8.39	0	409.0	1.02	13.22
			Reference Materials				
Silicon	**131.0**	**2.33**	**5.74**	**2.60**	**129.0**	**0.70**	**9.37**
Aluminum	68.9	2.70	2.59	23.58	168.0	0.90	8.89
Boron	344.7	2.34	15.03	8.30	1.0	1.29	22.52
Fused Silica	73.0	2.20	3.39	0.50	1.0	0.92	12.30
Copper	117.2	8.91	1.34	16.90	400.0	0.39	1.44
SiC	325.0	3.00	11.05	2.30	200.0	0.89	8.52

[a]Unidirectional properties.
[b]Graphite Fiber (P75) / Epoxy matrix (1939-3), unidirectional, ~60% fiber.
[c]Graphite Fiber (P120) MMC-Metal Matrix Composite, quasi-isotropic, ~60% fiber.

Table 21 illustrates the candidates being considered for shell and ring structures for which a quasi-isotropic CTE is needed or where a particular CTE value is to be matched; for example, IM6/3501-6 (2.9 ppm/°C) compares favorably with that of silicon (2.6 ppm/°C).

Table 21. Graphite/Epoxy Composite Material Systems Quasi-Isotropic Laminate Engineering Parameters

System	Elastic Modulus E (GPa)	Density ρ (g/cm^3)	Specific Stiffness E/ρ (10^8 cm)	CTE α (ppm/°C)	Poisson Ratio ν	Shear Modulus G (GPa)
P75/1939-3	109.2	1.68	6.6	−0.43	0.321	41.3
P75/3501-6	107.8	1.68	6.5	−0.5	0.321	40.8
GY70/3501-6	98.9	1.66	6.1	−0.016	0.318	37.5
UHM3501-6	95.8	1.60	6.1	0.18	0.314	36.4
IM6/3501-6	78.3	1.56	5.1	2.9	0.296	30.2
AS4/3501-6	55.9	1.56	3.7	1.96	0.30	21.5
AS1/3501-6	51.7	1.56	3.4	2.32	0.298	19.9

Graphite/epoxy composites have been tested in a radiation environment and data exist on the aromatic amines (Hercules 3501-6) and aromatic isocyanates (ERL 1939-3), which show that structural degradation after exposure to 10 Mrads is not a problem. However, none of the existing data on graphite/epoxy composites is useful in understanding how dimensionally stable the material will be after exposure to a radiation environment in the presence of a hydrocarbon. Creep may become a serious problem. We are conducting radiation and physical property tests to qualify the materials. Tests will be directed toward establishing whether residual stresses in panel fabrication are relieved through an annealing process that results in micron-level distortions. Uncertainty in material long-term dimensional stability will remain a major concern until our material studies are complete. An additional concern is the dimensional change that occurs after exposure to the vapor that will exist in a completely open heat pipe working fluid system. Structural materials swelling, caused by the absorption of the cooling system working fluid, will stabilize, so dimensional changes will not occur randomly from this source; but the change must be factored in when establishing the final location of all silicon wafers to the required placement accuracy.

Recent studies have resulted in a better understanding of what matrix material would be best suited to the SSC environment. Three types of resin systems have been examined; aromatic amines (Hercules 3501-6), aromatic isocyanates (ERL 1939-3), and cyanate esters (Fiberite 954-3). Each resin system has its advantages, but for our particular application, cyanate esters will become the baseline for the STS design. Cyanate esters are radiation resistant, have a high elastic modulus, and demonstrate the least moisture ingress and egress of all organic resins.

Tests of panels and tensile specimens composed of graphite and a cyanate ester resin are underway. Modulus of elasticity and hygrothermal properties of some graphite fiber and organic resin composites are given in Table 22. The maximum processing temperature of the cyanates is the same as epoxies and the cyanates demonstrate only a marginally lower elastic modulus, on the order of 3 GPa, and a bit larger CTE, on the order of 60 ppm/°C. These characteristics can be used with ultra-high modulus graphite fibers to yield a laminate CTE approaching 2.6 ppm/°C, that of silicon, or zero as desired. A fractional volume increase of the resin during cure produces a lower void content laminate, hence more inherent structural stability. The fiber selection will be either Hercules UHM or Amoco P75. These fibers offer a readily available thin prepreg which can be tailored for our desired CTE requirements. Material testing will be undertaken in FY92 to evaluate the candidates.

Table 22. Elastic Modulus and Hygrothermal Properties of Some Candidate Materials

Candidate	Quasi-Isotropic Elastic Modulus (GPa)	Thermal Strain (ppm at −20°C ΔT)	Moisture Elongation (ppm at max H_2O Absorption)	Max H_2O Absorption (% by Weight)[a]
Epoxy Resin				
IM6/3501-6	78.1	−28.70	610	1.9
AS4/3501-6	54.6	−48.24	684	1.9
UHM/3501-6	95.8	−3.77	446	1.9
P75/3501-6	107.8	+10.10	349	1.9
GY70-930	113.9	+0.99		
P75/PR500			45	N/A
P75/ERL 1962			110	N/A
P100/ERL 1962			47	N/A
Cyanate Ester Resin				
P75/954-3			10	N/A

[a] Butane absorption unknown; expected < 1%
N/A not available

1. Radiation Length Considerations

To first order, a radiation length in a material is given by

$$L_R \propto A/(\rho Z^2)$$

where A is the atomic weight, ρ is the material density, and Z is the atomic number. This clearly demonstrates the need for a sparse mechanical structure of very low Z composition. A single 300-μm-thick silicon detector represents $0.0032L_R$. However, the silicon detectors must be supported and serviced by a mechanical structure. Therefore, an attempt must be made to rigidly support the detection medium with as little structural mass as possible. Our objective is to achieve the design stability requirement while using less structural mass than payload mass. One goal is to keep the structural materials and necessary services, such as power cables and cooling, to an equivalent radiation length equal to that of the detection medium, roughly 3%, or less if at all possible.

Table 23 lists the effective radiation length of components which make up the tracking system. The list comprises discrete components for which the material has been normalized to an effective thickness and a particular reference material. In some instances the component is composed of several materials; for example, the electronics comprise a sandwich of silicon chips, kapton foil, adhesives and a beryllium ground plane. In this instance the component assembly was referenced to the radiation length associated with silicon. The present electronics arrangement

spans nominally 2.7 cm and has variable thickness. We have averaged the material thickness over that span. For example, the cooling ring and electronics were treated as a package, consequently, the ring was normalized to the 2.7 cm span as well. This technique was used in the interest of expediting the estimation of the tracking system radiation length.

Table 23. Central Region Radiation Length Characteristics for Zero Pseudorapidity.

Component	Material	Effective Thickness	Material Effective Rad. Length L_R (cm)	% of Rad. Length
Silicon Strip Detector (with G/E ribs)	silicon[a]	0.0318	9.37	0.34
Electronics	Si/Be composite[b]	0.0517	9.37	0.55
Cooling Ring	G/E & wick	0.125	25.0	0.70
Composite Shell	G/E	0.067	25.0	0.27
Space Frame Tube (0.11 cm wall)	Mg-MMC	0.220	16.8	1.31
Cables	Be & Kapton	0.046	35.3	0.13

[a] Primarily silicon, plus for ribs, adjusted to equivalent thickness.
[b] Composite layer of silicon, Be ground plane, Kapton, conductors, etc., adjusted to equivalent silicon thickness.

The information contained in Table 23 provides some insight as to radiation length contributions from various components. For example, a single cooling ring, including wick structure and butane, represents 0.7% of a radiation length. This estimation is based on a 450-μm-thick graphite/epoxy wall structure and a butane-saturated 1-mm thick polystyrene wick. To lower this value, considerable development will be required. To date, we have achieved a 450-μm-thick graphite/epoxy ring. In contrast, we have not achieved a 1-mm-thick wick structure; future wick development tests scheduled for FY92 are planned to achieve this objective. The design goal is to reach a thickness of 250 μm for the wick.

A metal matrix composite material was chosen for the baseline space frame, which is a sparse arrangement with frame members placed azimuthally at 60° intervals. Both Al- and Mg-MMCs can be tailored to provide near zero CTEs. Also, the unidirectional elastic modulus for a MMCs is exceptionally high, a very important attribute for minimizing the frame mass. Mg-MMC has an effective radiation

length slightly longer than Al-MMC. For this reason it is the chosen candidate. The Mg-MMC technology, however, is not as mature as the Al-MMC. Future space frame design/cost evaluations must consider this fact. Another important aspect is that MMC candidates do not have moisture expansion problems characteristic of graphite/epoxy composites.

A graphite/epoxy based material has a radiation length of 25 cm, which is considerably greater than the 16.8-cm length for Mg-MMC. However, the lower elastic modulus for a graphite/epoxy material completely offsets this positive benefit. The space frame cross sectional properties must be increased for the graphite/epoxy candidate to maintain the same structural behavior. If a graphite/epoxy material were used in place of the Mg-MMC, it is possible that a degradation in radiation length would be experienced. The positive benefit in using a graphite/epoxy material would be cost.

The electronics present another significant source of material mass intercepted by the particles. In view of the large number of electronic packages, their contribution is quite significant. The DC power bus system is moved to as large a radius as possible and spread uniformly over the circumference. As such, it would be approximately 600-μm-thick and represent less than 0.2% of a radiation length if beryllium is used for the bus. Local connections are made using Al as the conductor. The material estimates are calculated in the next section, section VII, based on the numbers discussed above.

2. Materials Testing

Materials have been subjected to physical and radiation tests to quantify their suitability for the SSC operating environment. Detailed results from this testing will be presented in the following two sections.

2.1 Physical Testing

Material swatches were fabricated to undergo tensile testing. Fifteen specimens were prepared. Ten were used in chemical baths to simulate exposure to the two cooling fluid candidates, and five were used for high-dose radiation damage testing as described in section VI.B.2.2. Baseline tensile tests were conducted prior to soaking, and repeated after soaking. The results of the tensile specimen tests are shown in Table 24. These results indicate that there are no apparent incompatibilities between the graphite/epoxies and working fluids. The small changes in elastic modulus are of no concern at this time.

The panel-facing material properties were calculated analytically and were subsequently verified in a standard tensile test. The tensile tests revealed an error in the ratio of graphite fiber to epoxy in the material used. Vendor specifications are

Table 24. Graphite/Epoxy Tension Test Results, Before and After Hydrocarbon Soak

Fluid	E (GPa) Before	After
cis-2-Butene	65.1	64.8
	64.3	63.9
	65.3	65.0
	69.0	54.1[a]
	68.4	68.4
Butane	73.1	67.9
	63.0	63.6
	68.6	69.8
	64.7	63.2

Note: Material used—P75/1939-3, Quasi-isotropic, 8-ply laminate; 38% graphite by volume; prediction would be 70.8 GPa. Soak period: 13 days at 24°C.

[a] Suspected strain-gage failure.

Table 25. Graphite/Epoxy Moduli and Poisson Ratio Analytical and Tension Test Results

	E (GPa)	ν
Analytical	70.3	0.31
Experimental (15 averages)	67.6	0.30

55% graphite and 45% epoxy by volume. Testing demonstrated 38% graphite and the remainder epoxy. Table 25 shows the analytical and experimental predictions for the tensile test pieces. The quasi-isotropic modulus of the panel should have been approximately 106.4 GPa for 60% graphite composition, but it was found to be closer to 70.3 GPa, indicating approximately 38% graphite fiber by volume. The analytical elastic modulus in Table 25 is based on the corrected value of fiber volume fraction.

2.2 Radiation Testing

The mechanical support structure for the silicon tracker will be subjected to radiation damage from charged particles and photons that emanate directly from the interaction point and neutrons that result from the interactions of the primary particles and their interaction products in the calorimeter. Over the 10-year lifetime of the experiment, at a radial distance of 10 cm, the total fluences are expected to consist of approximately 10^{14} charged particles/cm^2, an equivalent

Table 26. Elastic Modulus Tests of Graphite/Epoxy (P75/1939-3) Radiation and Chemical Exposure

Group Number	Baseline E (GPa)	Chemical Exposure E (GPa)	Radiation/Chemical E (GPa)
1	68.88 (6)	Butane (5) 67.41	73.24 (1)–No butane exposure 72.16 (1)–After butane exposure
2	65.46 (4)	Cis-2-butene 64.60 (4)	75.86 (3)–After cis-2-butene exposure
3	73.94 (5)		70.41 (5)–No chemical exposure

Notes: Baseline average of 15 specimens, total = 69.65 GPa; Radiation > 10^{14} n/cm^2; 1 sigma = 4.54 GPa; number of specimens shown in parentheses.

fluence of photons, and less than 10^{13} n/cm^2.

Although these radiation levels are low compared with those commonly encountered in fission power reactor facilities, the problem here is of a different scope and involves unique materials and structures. We are interested in effects such as creep, warping, and swelling, which lead to the slightest dimensional changes of the items these structures support. The required positional stability is approximately 5 μm. This applies to a structure that is over 5 m long and 1 m in diam. Because it is necessary to attain maximum stiffness of the structure, using minimal support mass, degradation of the mechanical properties of the materials used to construct the structure must be known. The materials testing effort is seen as a several year project. This effort has begun with an examination of samples of various materials and will evolve into testing full-scale modules.

A study plan was devised to look at the first-order effects of radiation and chemical degradation. These initial material tests provided a first critical step in assessing which materials will perform satisfactorily in the given physical environment. It is important to verify the suitability of candidate materials early in the program. In principle, the high-intensity beams and facilities available at LAMPF and the high-intensity ^{60}Co source at the University of California at Santa Cruz make it possible to perform the appropriate tests. The doses accumulated over the lifetime of an SSC experiment can be achieved at these facilities over a time period of several weeks. Testing on a small lot of tensile test specimens was conducted to ascertain first order effects of radiation fluences of 10^{14} n/cm^2. The results of the tests are shown in Table 26. Because of the small number of samples it is not possible to determine statistically significant changes between the individual samples. However, it appears that there were no significant effects caused by the radiation and butane exposure combination.

Graphite/epoxy sandwich construction panels were also exposed to neutrons at the Los Alamos Spallation Radiation Effects Facility (LASREF). This test provided an opportunity to observe the performance of the graphite/epoxy structural materials as they accumulated a total dose near that expected at the SSC over the lifetime of the system.

Two sandwich panels were fabricated and mapped for flatness prior to exposing the panels to radiation. The intent was to identify whether dimensional instabilities would be encountered as the result of a radiation dosage several times the expected SSC level. It is conceivable that the radiation could cause the residual fabrication stresses to relax and, thus, alter the shape of the panels.

The initial panel, after having acquired a neutron fluence of approximately 3×10^{13} n/cm^2, was removed from the neutron flux, inspected for ply delamination, core debonding, and gross warping, and was then remapped. No catastrophic conditions were observed. In the second panel, an accurate measurement technique was used for initial and after-irradiation surface mappings. The second panel showed less than 5 μm of measurable distortion. The metrology measurement system, however, still needs to be improved to reliably measure to the order of 1 μm.

C. Structural Considerations

1. Cooling Ring Composite Structures

As cited earlier, the electronics for the silicon detector ladder are concentrated at the two ends of the assembly. Heat removal from these two ends is accomplished by attaching the ladders to cooling rings, which also provide support for the silicon structural assembly. In the baseline concept for this shell assembly, the ring structure is formed by compression molding a graphite fiber/polymeric composite material. The fiber and resin combination will be tailored to achieve a silicon-CTE match. A hydrophobic resin has been selected to minimize the moisture expansion effects that generally detract from the ultrastability of graphite/epoxy composites.

To date, ring arc segments have been produced with a nominal thickness of 450 μm, using AS4 chopped prepreg and phenolic resin. These ring segments were constructed for our heat pipe development tests. Our ring segment embodied the required features of the ultralightweight ring construction, but did not reflect our final material choices. The combination served as a means of expediting the heat pipe thermal studies.

The potential for silicon shell assembly distortion from moisture and/or thermal expansion effects of the cooling ring structure is a serious design issue. The preliminary design effort and experimental program will address these issues. Our

conceptual design studies have pointed out that thermal conductivity enhancements of the graphite fiber/polymeric matrix must be achieved to minimize the thermal gradients in the cooling ring structure.

2. Silicon Shell Module

Various means of achieving transverse stiffness in the silicon ladder module have been studied. Transverse stiffness is essential to minimizing distortion in a ladder assembly where forces or moments act normal to the ladder longitudinal axis. Gravity sag is a major contributor to transverse deflection. This contribution can only be dealt with by increasing the ladder stiffness. With careful design, thermal distortion within the ladder framework should normally not be a problem. Figure 66 illustrates various concepts considered for enhancing the bending stiffness of the silicon ladder assemblies. For these configurations the gravity sag of a ladder was calculated as a function of length. Both the I-beam and the Pi-beam configuration provide adequate stiffness, i.e., for 24 cm ladder lengths the deflection is significantly less than the 80-μm design goal. The I-beam concept is the preferred concept, since the reinforcement strips are a graphite fiber/epoxy composite, and could introduce undesirable thermal expansion effects when configured asymmetrically as in the Pi-beam concept.

3. Forward Region Module

Design of the forward region flat planar arrays has proved particularly challenging. The large planar arrays tend not only to be less stiff than their cylindrical counterparts but are also more prone to thermoelastic distortion resulting from the CTE mismatch between the inner and outer support rings. This latter problem presents difficulty in strain free, kinematic, mounting and mandates attention to a means of strain relief for the assemblies. An internal ring structure concept was chosen for nearly strain-free mounting of the wedge-shaped detectors. Also, static and dynamic calculations were employed to define structural shapes, material thicknesses, and basic material properties.

Static and dynamic stiffness as well as the response of the structure to temperature changes were assessed for a large planar region array using a kinematic mounting scheme such as three support points on its outer edge. The kinematic internal ring mounting was developed to neutralize the effect of differential thermal expansion in the inner and outer rings supporting the forward region wedge-shaped detectors.

We describe the structure which was analyzed in some detail. Its area is somewhat larger than the present baseline forward detector panel. The substructure to which the silicon detector strips are attached, conceptually comprises three concentric rings of graphite/epoxy composite. These rings are connected by three

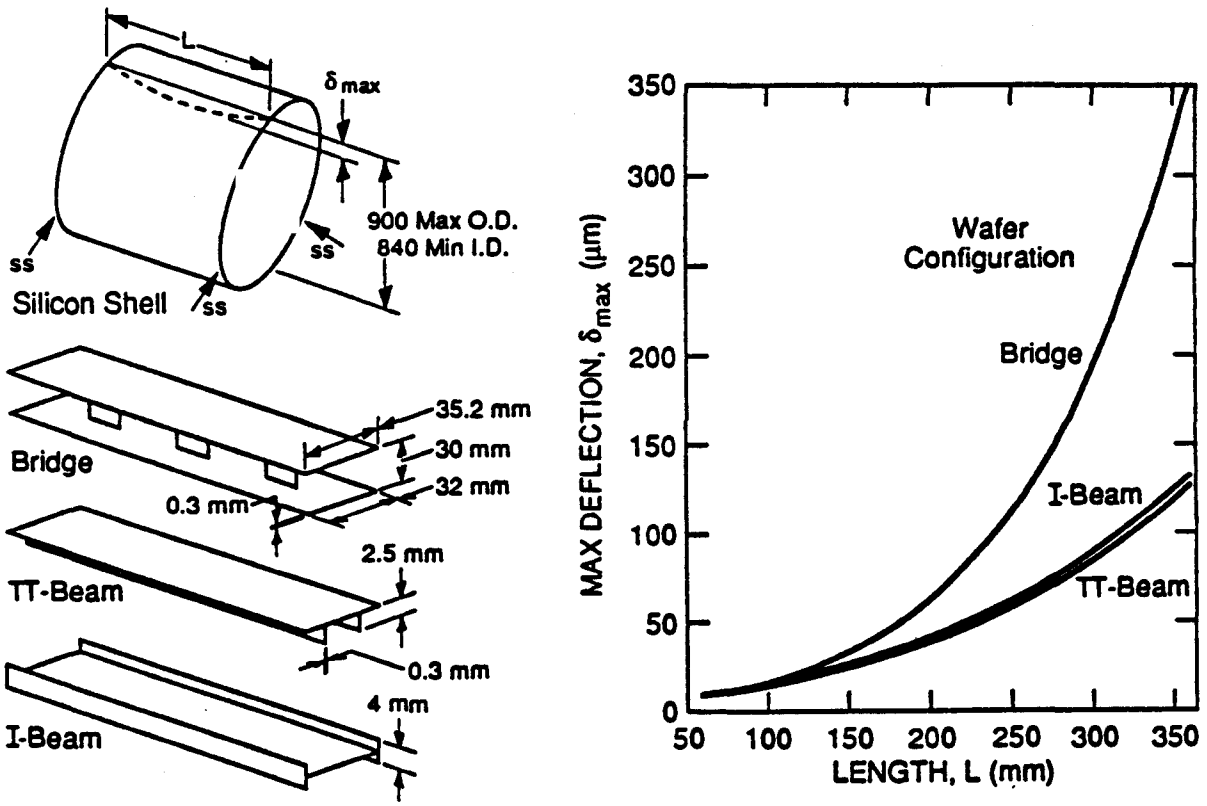
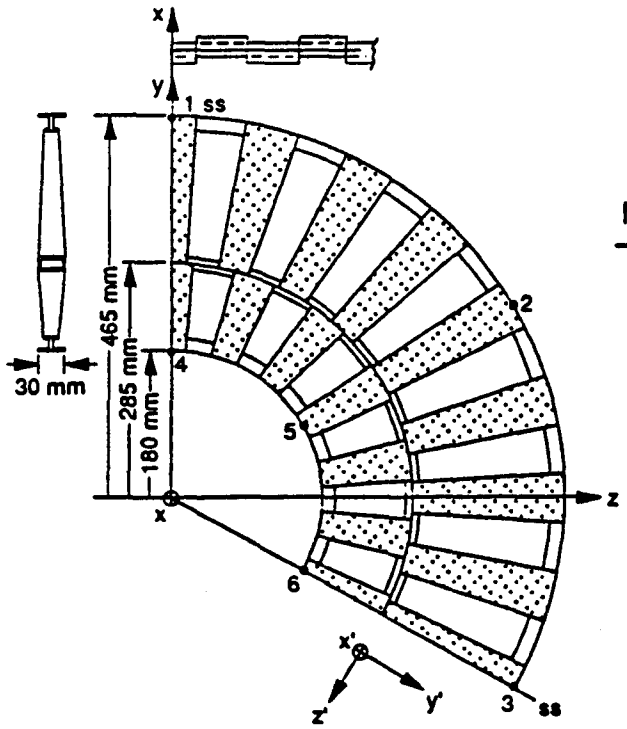


Fig. 66. Silicon wafer configurations and displacements expressed as a function of assembly length.

equally spaced radial webs. A kinematic mount is located at the outmost end of each web. The inner ring, which has a minimum radius of 180 mm, is similar to a conventional wide-flange beam in cross section. The inmost flange is cut away in an alternative pattern to form castellations to which the inner ends of the internal array of silicon strips are attached. When the structure is subjected to a temperature change, the castellations, which appear to be short cantilever beams, act as compliant members to accommodate differential contractions due to differences in material CTE. The outer ring has a maximum radius of 465 mm. This ring, which is closed-cell structure 12 mm × 30 mm in cross section, provides cooling for the strips. The strips are arranged on the substructure in an alternating pattern so that half are mounted on the upstream axial, or z-direction, face and half are mounted on the downstream face.

Static analyses show that when the structure is mounted in a vertical attitude, characteristic of its installed state, with one of its kinematic mount points at the

uppermost position, its maximum sag is approximately 22 μm in a downward radial sense. This is indicated as the Δy value for node 1 in Fig. 67. The finite element FE modal analysis performed for the assembly yielded a fundamental natural vibration frequency of 70 Hz.The magnitude of the number is not critical excepting the fact that it reflects a reasonably stiff structure that should not be excited by 60 Hz vibration sources.



Gravity Sag Displacements (μm)
(vertical orientation)

	w/o Wafer Stiffening			I-Beam Wafer		
Node	Δx	Δy	Δz	Δx	Δy	Δz
1	0	-21.94	0	0	-14.97	0
2	0	-11.14	6.26	0	-7.74	4.33
3 (L)	0	21.75	0	0	15.05	0
4	0.01	-21.87	0	0.04	-15.23	0
5	0	-12.89	7.28	0.01	-9.13	5.15
6 (L)	-0.02	22.03	0	-0.04	15.31	0

Fig. 67. Forward region schematic, demonstrating pie-shaped detectors and radial webs, and gravity-induced static displacements for the vertical orientation.

D. Support Structures

1. Space Frame

The space frame provides structural support for the structural shells in the central region and the planar arrays in the forward region. The design criteria applied to the development of this structure are based largely upon dimensional stability, high stiffness to weight ratio, minimal intrusion on the paths of energetic particles emanating from the interaction region, and structural integrity. Consideration of each of these is important for assuring the silicon tracking system is capable of achieving its operational objectives. In attempting to design the space

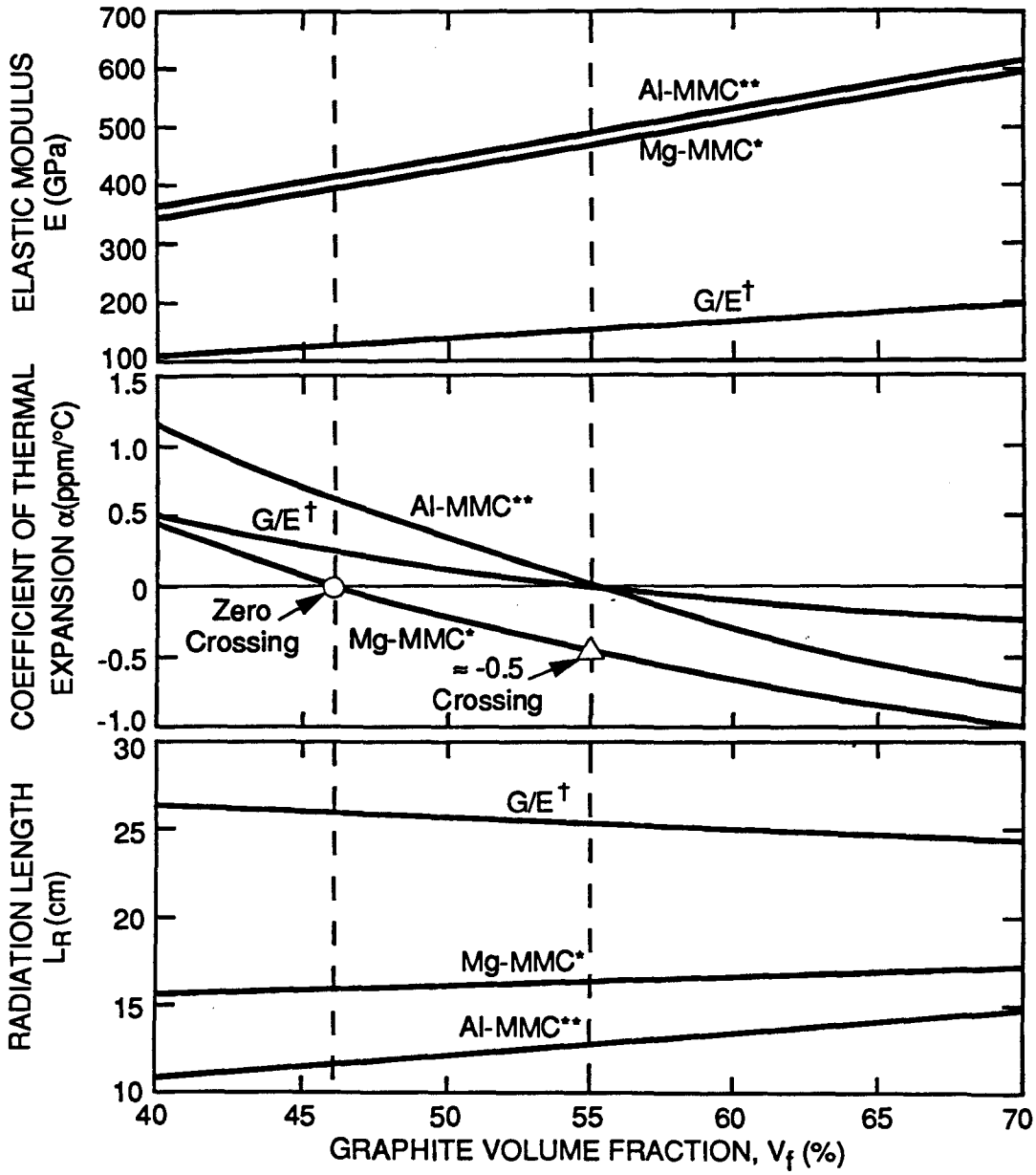
frame it becomes readily apparent that these different criteria are often in direct conflict and that the interrelationship between different structural materials and design configurations is very complicated. An effort will be made to describe the detailed effects of material choices and configurations on system performance.

Stringent dimensional stability is required of the space frame. Achieving the demanding baseline design requirements for the detector assembly enumerated in Table 19 rests primarily on the structural performance of the space frame. Monolithic metals possess CTEs large enough to exceed the dimensional tolerance of wafer placement during a temperature excursion of less than 1°C. This is only one motivation driving the selection of advanced composite materials for space frame construction.

For MMCs, fibers increase modulus and strength, and allow tailoring of such properties as CTE and thermal conductivity. Matrix materials are useful structural elements in their own right. The appropriate selection of fibers, matrix, and layer orientations can allow properties of a component to be tailored to meet specific design needs. Strength and stiffness could be specified in one direction, for instance, with CTE in another. Also, unidirectional continuous-fiber MMCs are non-isotropic—stronger and stiffer in the direction of the fibers than perpendicular to them. Nevertheless, transverse strength has typically proven great enough for use in components such as stiffeners and struts on both military aircraft and scientific experiments.

The CTE information presented in Fig. 68 reflects the large tailorability range, expressed as a function of fiber volume fraction, that is possible with both polymeric and metal matrix composites. The effect of fiber volume fraction variation on elastic modulus must be considered in concert with that of CTE. To ensure axial dimensional stability of the 5-m-long space frame, a CTE approximately equal to zero is required. This can be accomplished with a unidirectional or quasi-isotropic construction composed of either a polymeric or a metal graphite-reinforced matrix. The quasi-isotropic construction would provide a nearly zero CTE in both the axial and transverse dimensions of the body. The effective elastic modulus of such a construction would be much less than if a unidirectional construction possessing a CTE near zero were used. In fact, the tubular design of the space frame reduces the importance of the transverse CTE, because of the small lengths for expansion present in the tubes radial directions. Based upon this scenario, the unidirectional Mg-MMC construction composed of approximately 60% graphite fiber with a slightly negative CTE and an axial elastic modulus of about 515 GPa is the baseline choice for the space frame's structural members.

The Mg-MMC material combination has a radiation length of 16.8 cm. It is not clear at this juncture if a change to graphite/epoxy material combination would



* Mg-MMC Features Mg (AZ91)/Graphite (P120S)
** Al-MMC Features Al(6061 - T6)/Graphite (P120S)
† G/E Features Polymeric Resin (3501 - 6)/PAN Graphite (IM - 6)

Design Parameters

○ α = ~ 0 ppm/°C, E = 385 GPa
△ α = -0.5 ppm/°C, E = 490 GPa

Fig. 68. Unidirectional material properties.

be beneficial solely on the basis of minimizing the percentage effective radiation length.

An FE model of the initial space frame design was constructed in an effort to estimate the static deflection and structural modes of vibration as a function of structural tubing size and modulus as well as support method. The masses considered in that analysis represented an earlier design with 33.4 kg of silicon, representing 48 vertical planes and 10 cylinders, 33.2 kg of cooling rings, using both graphite/epoxy and Al-MMC, and that of the space frame structural tubing. Table 27 provides information regarding the structural mass for four cases of interest. Fig. 69 displays the fundamental vibrational frequency and maximum displacement for each case.

For a long cylinder, a bending mode existing as the fundamental, first, natural frequency indicates a sound structural support arrangement and yields a higher frequency value than other twisting or collapsing modes. Using only three support points, FE models indicated a twisting mode would be developed by the structure as its fundamental. As shown in Fig. 69, the bending mode fundamentally is generally achieved where four discrete points are used for structural support. Unfortunately, this method is not ideal from a kinematics standpoint. Maximum deflection and first bending mode expressed as a function of elastic modulus, tube size, and wall thickness, and number of support points are displayed. A stiffer structure would exhibit less deflection and possess a higher fundamental frequency value. For example, if the space frame were constructed solely of 33.7 mm (1 3/8 in) tubing with a wall thickness of 1.1 mm (0.045 in) an elastic modulus of 515 GPa, and a four point support scheme, the maximum deflection would be 0.22 mm and its fundamental natural mode of vibration would be bending occurring at approximately 35.7 Hz. This arrangement was selected for the initial baseline. For a silicon tracking system incorporating far less silicon the deflection would be noticeably reduced. The design calculations must be repeated after a complete system definition has been obtained including the weight of the power distribution system (cables) and other services. It is not clear whether effective size of the frame tubular members can be reduced at this stage.

2. Graphite/Epoxy Structural Support Cylinders

The cylindrical panel geometry used for silicon wafer support will incorporate ultralightweight panels. These panels will have facings and a core optimized for strength and CTE. During the conceptual design process, it was important to understand the mechanics of such panels.

Analytical and experimental techniques were used to explore and verify the design concept. Prototype panels were built from graphite/epoxy and beryllium to

Table 27. Space Frame Structural Member Dimensions and Resulting Structural Mass

Case	Structural Member Dimensions (mm) Inside Tube*	Outside Tube*	Structural Mass (kg)
A	35 (1.1)	35 (1.1)	31.7
B	25 (1.1)	35 (1.1)	27.2
C	17 (0.8)	35 (1.1)	18.9
D	17 (0.8)	25 (1.1)	16.3

*Tube diameter and (wall thickness).

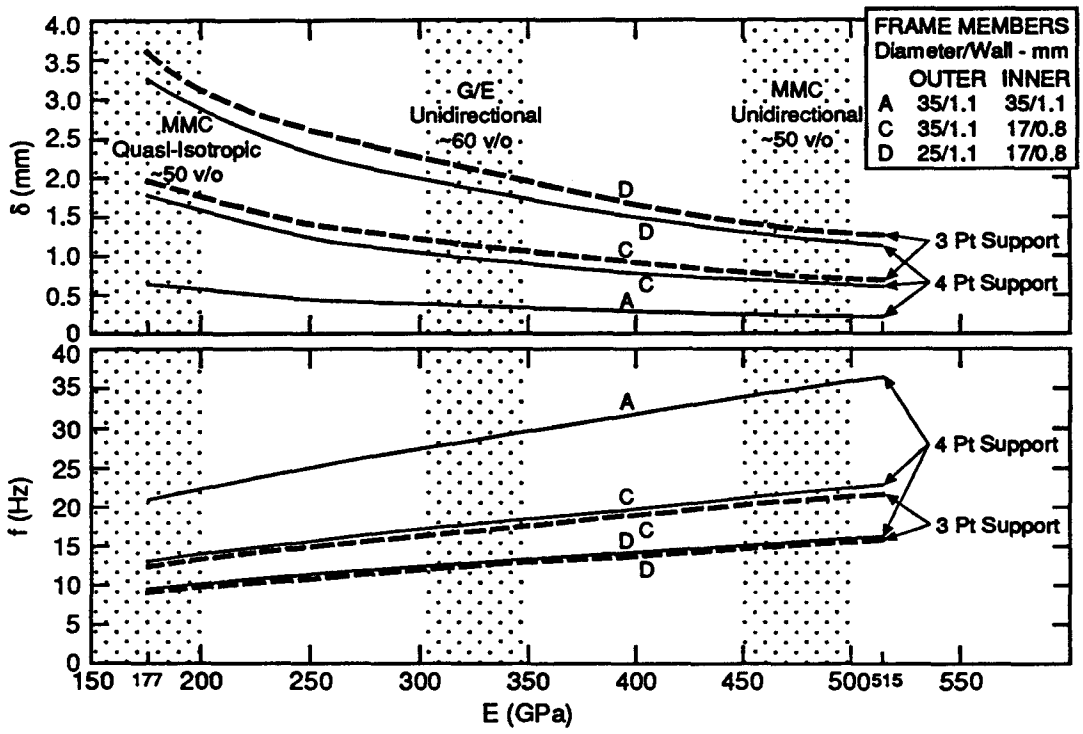


Fig. 69. Space frame gravity-induced displacements, δ, and fundamental natural vibration bending frequency, f.

verify our analytical methods. These sample sandwich panel fabrications are also providing useful information regarding manufacturing techniques. Although the sandwich geometry selected is not necessarily the final configuration, the construction features will demonstrate most of the requirements for a detector component.

2.1 Sandwich Panel Core Optimization

An optimization study for a graphite/epoxy panel has been performed. The objective of the study was to parametrically investigate the effects of material geometry trade-offs on the panels' physical properties. Two analytical models

were constructed. The first consists of the entire panel modeled as a sandwich, and the second models a detailed section of the panel.

These studies were then used to predict deflection resulting from a four-point bend test of a full panel. The actual hardware, depicted in Fig. 70, was tested and used to verify the analytical model. This step is essential for further designs to ensure a proper understanding of the panels' behavior. The calculated core shear modulus is 2.0 MPa using the theoretical model. Fig. 71 demonstrates the numerical results for the test panel. Using the calculated shear modulus, the predicted deflection is 0.624 mm. The actual measured deflection (average of two outer measurements and one midpoint measurement) is 0.592 mm. This excellent agreement, within 5%, was achieved even though deflection is a function of rapidly varying shear modulus for the case analyzed.

The results of the sandwich panel core optimization are contained in Ref. 35. The conclusion of this report summarizes the material and geometric trade-offs used to optimize the structural panel. Further optimization studies will be undertaken to study curvature effects. To date, only the deflection in a flat panel has been addressed, but further studies will model an entire cylinder made from the graphite panel. These studies will explore the relationship between panel thickness and deflection leading to an optimized corrugated core design. Other factors, such as utilities, cooling, and cabling, will have a bearing on the design. These considerations will be integrated into the design as it matures.

3. Detector Outer Enclosure

The outer enclosure, in conjunction with the inner enclosure, provides a containment volume for the butane vapor. The outer enclosure also serves as the structural interface with the internal space frame and the mechanical support of the entire STS. As a conduit for transferring the support reactions, the outer enclosure becomes a key member in maintaining the stability of the STS. The outer enclosure must provide a stiff, very low mass structure also capable of resisting external buckling from a one atmosphere pressure differential. Although during operation the differential across the enclosure is near zero, a one atmosphere differential may be encountered in one of the likely butane filling and evacuation scenarios. An external view of the containment vessel with the outer tracker support interface is shown in Fig. 72. This support concept requires further structural study before being accepted as the baseline approach. At present, we plan to fabricate all structural barrels out of a corrugated core commonly referred to as a "truss core" (Fig. 70). This structural approach requires the minimum amount of our radiation length budget, but is also likely to be expensive due to tooling costs and assembly.

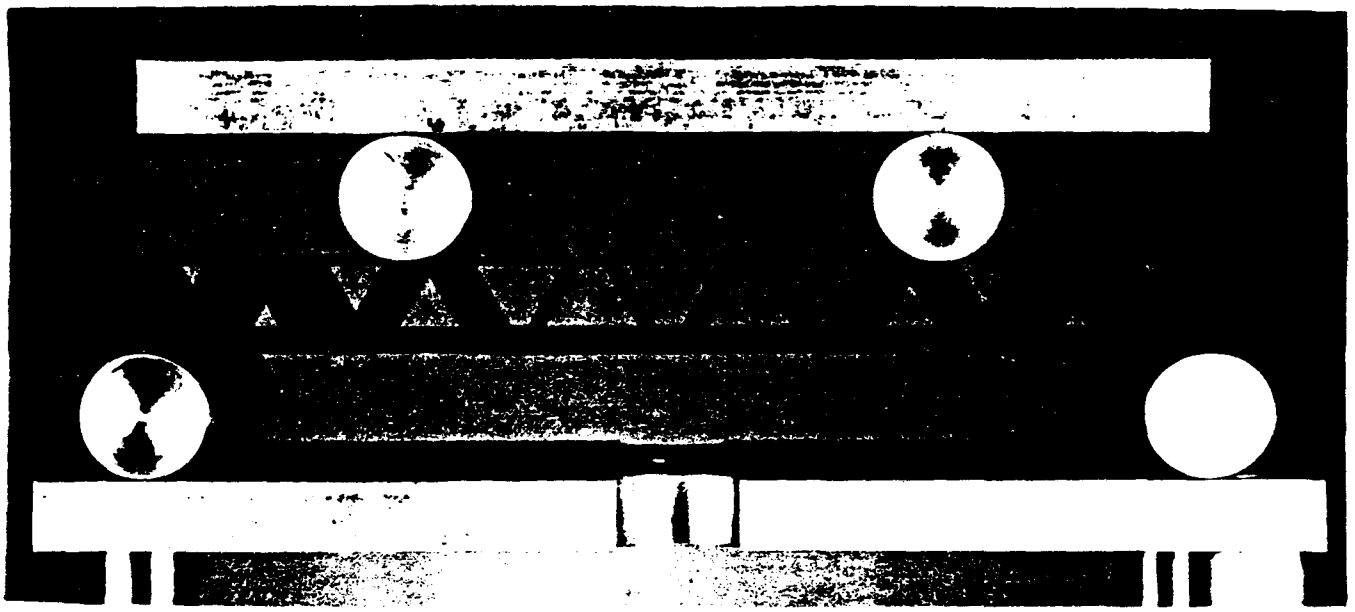


Fig. 70. Four-point bend test experimental setup.

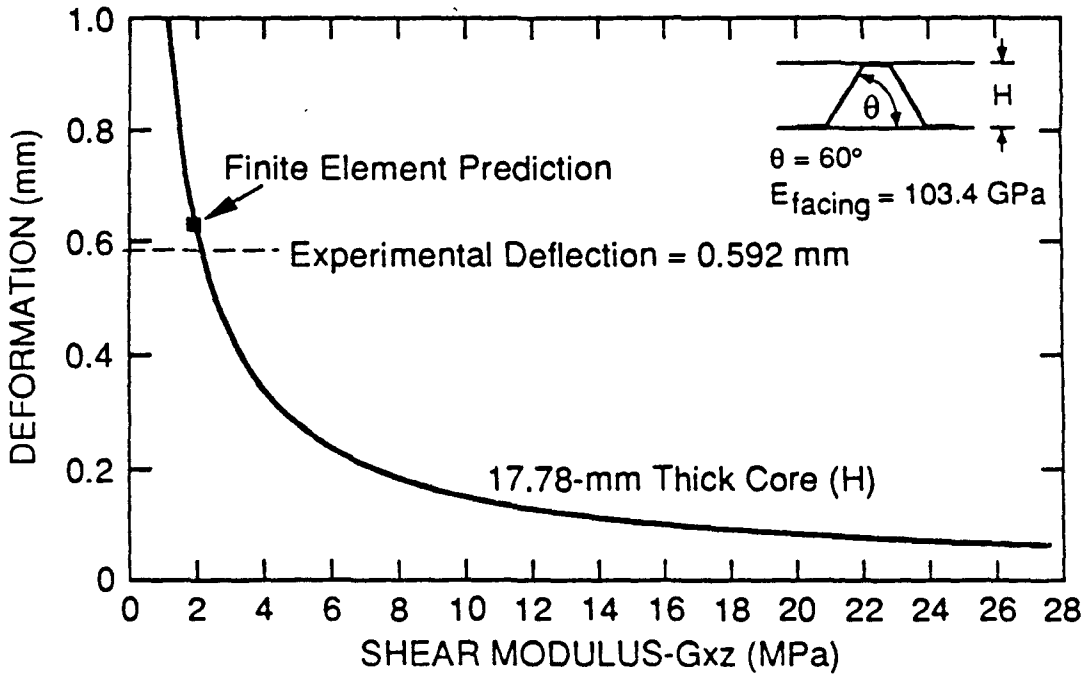


Fig. 71. Numerical and experimental results of four-point bend test.

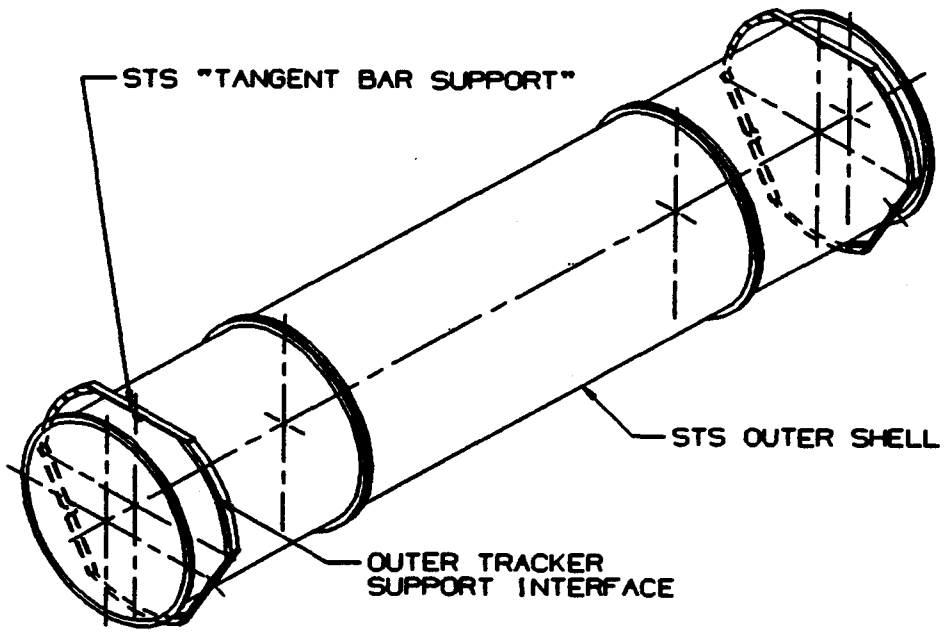


Fig. 72. Outer containment vessel with outer tracker support interface.

The engineering design of the enclosure includes the capability to remove the end cylindrical sections and access the detector's electrical service connections. These service connections could be disengaged in order to remove the end spools of the detector while the detector continues to be firmly supported by its space frame. Access to both forward regions would be possible as well as some limited access to the central region of the detector, providing the STS is completely removed from the SDC detector assembly.

4. Detector Inner Enclosure

For the baseline design, the particle beam beryllium vacuum pipe or a separate tubular liner will provide the vacuum interface, and contain the butane vapor. There are several factors that contribute to the choice of beryllium over a graphite fiber/polymeric matrix composite. First, beryllium is roughly three times stiffer than a quasi-isotropic composite and second, one radiation length of beryllium allows the use of 40% more material than graphite/epoxy. Both factors contribute heavily to the choice of beryllium for the inner liner. In fact, the entire butane vapor enclosure vessel would be fabricated from beryllium, if fabrication costs were not a factor.

Inner enclosure liner buckling must be considered in the design process. The external load imposed on the beam tube from the butane vapor under normal conditions would be one atmosphere of differential pressure. To allow for an adequate margin of safety in an elastic instability situation, we chose 3 atmospheres as a

critical buckling load. The beryllium tube wall thickness for a 10-cm diameter beam tube would then nominally be 0.76 mm (0.22% radiation length at normal incidence). The critical buckling pressure is a function of t/r, so an increase in beam tube radius will require a similar increase in tube wall thickness, for the same critical load. It is possible to use ring stiffeners to raise the critical buckling pressure.

E. Evaporative Cooling System

1. Cooling System Concept

The mechanical stability requirements of the STS array dictate precise thermal control of the entire array to a nominal operating temperature with minimal thermal gradients within the array. These requirements have led to the development of a liquid-vapor phase change system to isothermally cool the detector array. Butane has been selected as the phase change medium, denoted the working fluid. The cooling system consists of an array of evaporators located within the detector at each electronically heated surface, vapor return lines, a glycol cooled condenser, and a network of liquid feed lines. Fig. 73 shows a schematic representation of the cooling system design. Liquid is distributed to the heated surfaces by a combination of gravitational and capillary forces. The heat produced in the electronics is transferred to the liquid which is vaporized. The vapor is removed from the heated surfaces by pressure gradients generated by the condensing process. The baseline detector is currently designed for a total heat load of 12 kW with a heat flux at the electronic surfaces of 1.33 W/cm ^{2} allowing a factor of two safety margin. The entire phase change cycle and detector array are fully contained in an hermetic enclosure. To minimize the structural loads on the enclosure, the cooling system operates at atmospheric pressure.

A 0°C detector operating temperature is the design choice to minimize leakage current, which is a strong function of temperature, in the silicon strip detectors. Leakage current is reduced by a factor of about 2.5 for every 10°C temperature reduction.

The temperature drop across the electronics to the cooling surfaces may be significant. If the mechanical configuration of the silicon and electronics causes them to be significantly above the cooling system sink temperature, then a lower system operating temperature will be required. This will necessitate the selection of an alternative working fluid with an atmospheric pressure boiling temperature below 0°C. Isobutane has a normal boiling point of −10°C and will be used if a lower operating temperature becomes necessary.

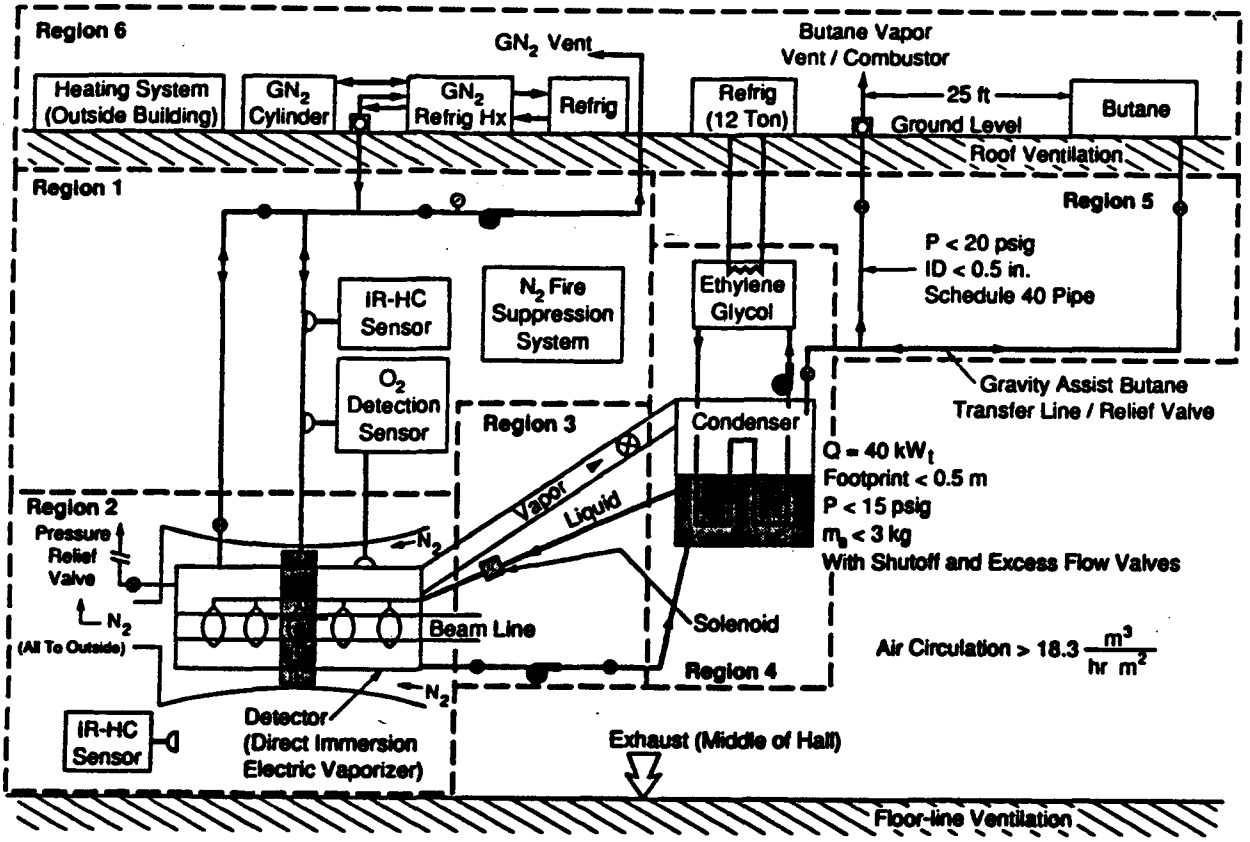


Fig. 73. Schematic representation of the cooling system design.

2. Alternative Cooling Concepts

Evaporative cooling has been selected because it offers many distinct advantages over all other potential cooling methods. It is characterized by extremely high local heat transfer rates that promote isothermalization over a large structure, very low liquid inventories, minimizing the radiation length contribution of the cooling system, and a completely passive operation. In addition to these features, liquid priming and temperature stability are both self regulating, no pumps or compressors are required during operation, and a phase change system provides uniform pressurization of the containment structure.

Several alternatives to the evaporative cooling system have been considered. These include forced convection of helium or air or a water/glycol mixture. Forced convection with gases is considered inferior to evaporative cooling due to thermal drifts and gradients. The cooling rate at the detector surface for typical gas cooled systems is two orders of magnitude below the demonstrated cooling rates of an evaporative system. Also the cooling at the heated surfaces is highly nonuniform. These cooling characteristics detract from the dimensional stability of a gas cooled

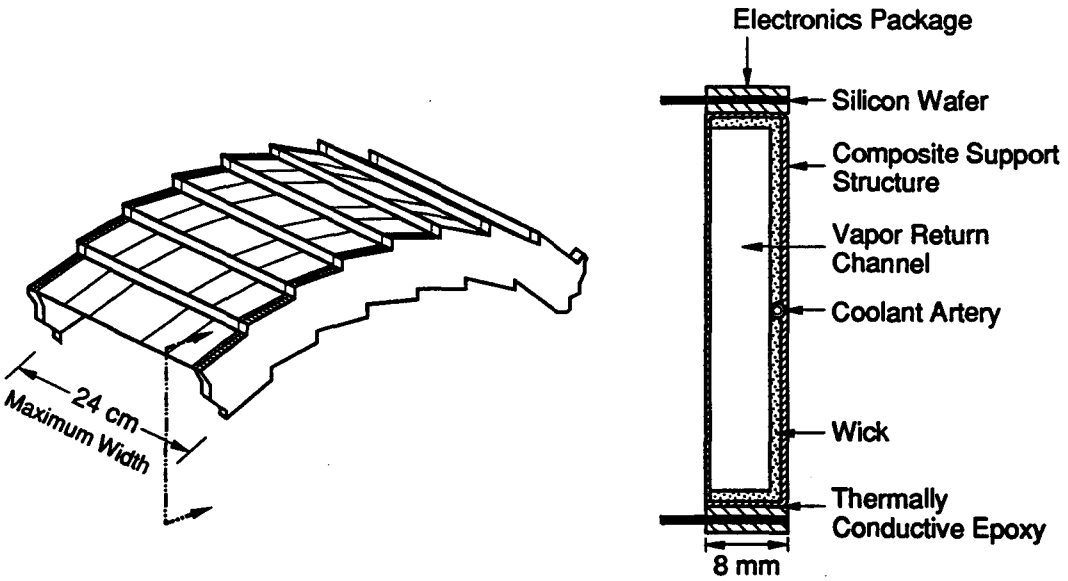


Fig. 74. Detector cooling ring, cross sectional view.

detector. A gas-forced convection cooling system also requires high flow rates which impose undesirable differential pressure loads across the silicon layers. These pressure differences will further degrade detector dimensional stability. Gas cooling also introduces the prospect of turbulence induced vibrations. Additional system mass would also be required for the primary structure and flow distribution scheme, increasing the detector's total number of radiation length.

Large percentage radiation lengths are also associated with a detector cooling system employing forced convection with a water/glycol mixture. In addition, the surface heat transfer coefficients of a water-cooled system are only one tenth that of an evaporative cooling system. This means that water cooling requires ten times the temperature drop to remove a given heat flux from a surface as an evaporative system. Structural support requirement of a water/glycol cooled system are substantial because of the large working fluid inventories. Water cooled systems, like gas cooled systems, introduce the prospect of turbulence-induced vibrations.

3. Butane Cooling System Description

3.1 Liquid Feed and Vapor Return Subsystems

Fig. 74 shows a cross sectional view of a detector cooling ring. Two coaxial lines run from the condenser to either end of the detector. The liquid feed lines run in the core of the coaxial lines. The vapor return line is an annular pipe that surrounds the liquid feed line. The primary liquid feed lines are connected

to secondary lines which in turn connect to the cooling ring artery network shown in Figure 73. The vapor lines open into the detector vapor space. The lines are then enclosed in a coaxial shroud of refrigerated flowing nitrogen gas. The distance between the detector and the condenser can be as much as 25 m. It is desirable to keep the flow induced pressure drop in both the vapor and the liquid lines to a minimum. To minimize the liquid side pressure drop, the liquid line diameter will be kept above 2 cm. This corresponds to a liquid side pressure drop of 100 Pa. To minimize vapor side pressure drop, the vapor annulus diameter is kept above 7 cm diameter. This corresponds to a vapor line pressure drop of less than 100 Pa for smooth walled pipe. The total thermal load on a 93-cm-diameter cooling ring, with an electronics power density of 1.33 W/cm^2, is about 700 W. This assumes double-sided electronics on both sides of the cooling ring. The mass flow rate of butane into this cooling ring would be 2.1 g/s, or 3.5 cc/s liquid. Locally, the flow out of the artery is about 5.1 mg/s per cm of length. Since the wick pores are sized to prevent wick bleeding with no flow, it is permissible to accept a flow induced pressure drop no greater than the hydrostatic pressure at the bottom of the cooling ring. For a single artery system, the artery diameter must be about 1 mm. Because artery pressure drop is inversely proportional to the fourth power of the diameter, a double artery system, which divides the flow in half, only reduces the required artery diameter to 0.9 mm.

If the butane liquid flowing through the liquid feed manifold closely approaches the saturation temperature then the potential exists for vapor formation. Vapor formation could occur in regions where the local pressure is temporarily reduced by sudden expansions. Vapor bubbles formed in this manner are unstable and will disappear upon entering a higher pressure region immediately downstream. The formation of vapor in contracted regions such as arteries is extremely unlikely since the local pressure will be higher.

The liquid feed lines are designed to minimize the chances of vapor formation. The liquid path between the condenser and the heated surfaces is a progression of successively smaller lines. This avoids vapor formation in expanded regions. Also, the lines and arteries are sized so that the total pressure drop between the condenser and the heated surfaces is less than 100 Pa. A 100 Pa frictional pressure drop corresponds to a 0.03°C temperature difference for butane at 0°C. Therefore, a liquid subcooled to 0.03°C below the saturation temperature would be adequate to prevent vapor formation in a horizontal line. The liquid exiting the condenser will be subcooled to several degrees below the saturation temperature. Also, once the liquid reaches the heated surface it will be pressurized under 1 m of hydrostatic head corresponding to 6000 Pa. Vapor formation in a properly insulated liquid feed lines is thus very unlikely.

One approach to the design of a cooling system artery network is a series of uniquely sized wicks and arteries for each cooling ring diameter. For simplicity and ease of manufacturing, this approach has been abandoned for a more uniform distribution system. Whenever possible the wick-artery structure within the cooling ring will be designed in a modular fashion. This philosophy extends to the connections between the cooling rings and the secondary liquid feed line system as well.

The liquid distribution wick is the key technology development component for the evaporative cooling system. The radiation length of the wick must be maximized by using low-Z materials and limiting wick thickness. The wick must be attached or bonded to a geometrically complex surface. The design goal for pore size of 6 μm has been established so that the wick can hold the liquid against up to 2 m of hydrostatic head. This will prevent any control valves from being necessary to standoff liquid bleed from the cooling ring wick structure. The wick thickness required to distribute an adequate supply of liquid over the heated surface is a function of wick pore size, wick permeability, capillary pumping distance, and power density. The wick pore size defines the available maximum capillary pumping pressure.

A number of wick designs have been considered to date. Some of the concepts tried and subsequently rejected include the spraying of graphite particles in an epoxy carrier solution, the laying of graphite fibers in an epoxy matrix, and the forming of porous structures out of wood pulp products. Of the wick fabrication methods considered thus far the polystyrene wick appears to be the most promising in terms of wicking properties and circumferential artery integration. Polystyrene foams are now the baseline wick material for the detector cooling system.

The highly porous polystyrene foam material was originally developed as target material in inertial confinement fusion systems. The foam is formed by mixing water with a monomer with a ratio of 90/10. An emulsifying liquid and an initiator is added to the mixture. The emulsion is polymerized at 60°C and then dried. The resulting foam has densities of less than 0.1 g/cc and high porosity. The porosity of sample foams have been measured and are typically 95%. Forced flow permeability measurements have also been made. A value of 1.9×10^{-12} m^2 was obtained across a solid sample 1.5-inches long, and 0.75-inches diameter. The pore radius of these samples, determined from scanning electron photomicrographs, varies between 1 and 6 μm. This pore size is acceptable for use as a wick material on the cooling ring. A number of polystyrene wicks have been fabricated and attached to cooling ring arc segments. The first attempts at polystyrene wick fabrication were very encouraging. An electron micrograph of the polystyrene wick structure is shown in Fig.75. The structure consists of a matrix of large cells interconnected by numerous

smaller pores. Experimental evidence has indicted that the effective pore size of the material is governed by the size of the smaller pore and not by the larger cells. The wick structure enhances the vaporization process by providing multiple liquid supply channels to the vaporization surface. In addition, the capillary structure reduces the liquid pressure resulting in vapor formation at lower wall superheats. The vapor travels from the heated surface to the outer surface of the wick through a series of vapor "chimneys." These chimneys consist of pores that are located on the cell structure on a outward path normal and away from the heated surface.

Tests have been conducted to measure the cooling performance of the polystyrene wick material under a variety of conditions. The results of these performance demonstration tests indicated a power density dependent temperature drop across the cooling ring to the wick surfaces. Locating these temperature drops has been complicated by the directional nature of the cooling ring's thermal conductivity. The temperature distribution on the surface of the wick and on the back of the cooling ring during operation with power, have been measured with IR temperature sensing equipment. The thermal conductivity of the graphite epoxy cooling ring material has been measured in directions both parallel and transverse to the carbon fibers. These data have been used in a thermal-conduction analysis that established the temperature drops across the cooling ring assembly. A plot of heat flux at the cooling surface versus temperature difference between the heated surface and the saturated butane vapor is shown in Figure 76. The linear curve on the right side of the plot demonstrates the temperature difference across the cooling ring and wick. The linear curve on the left side of the plot indicates the temperature drop attributed to the vaporization process alone. The vaporization heat transfer rates have been found to be quite high ranging up to 4,000 $W/m^2 \cdot °C$. The corresponding temperature drop at the vaporization interface is then typically less than 2.5°C at heat fluxes around 1 W/cm^2.

3.2 Condenser Design

The working fluid rejects its heat load to a liquid cooling loop that has been chilled by a standard refrigeration system to some temperature below the working fluid temperature in the condenser. At the baseline 0°C operating temperature, a glycol/water mixture is required to keep the water from freezing.

The baseline condenser, of a standard shell and tube design, allows for large heat transfer surface areas in a small volume. In the baseline configuration the condensation occurs on the shell side. Shell side condensation minimizes the vapor pressure drop, while the water/glycol mixtures flows through the tubes at a temperature depending upon the desired detector operating condition. A slight tilt allows for removal of condensate from the lowest point at the extreme end of the tube. A vertical condenser orientation is preferred because the system temperature

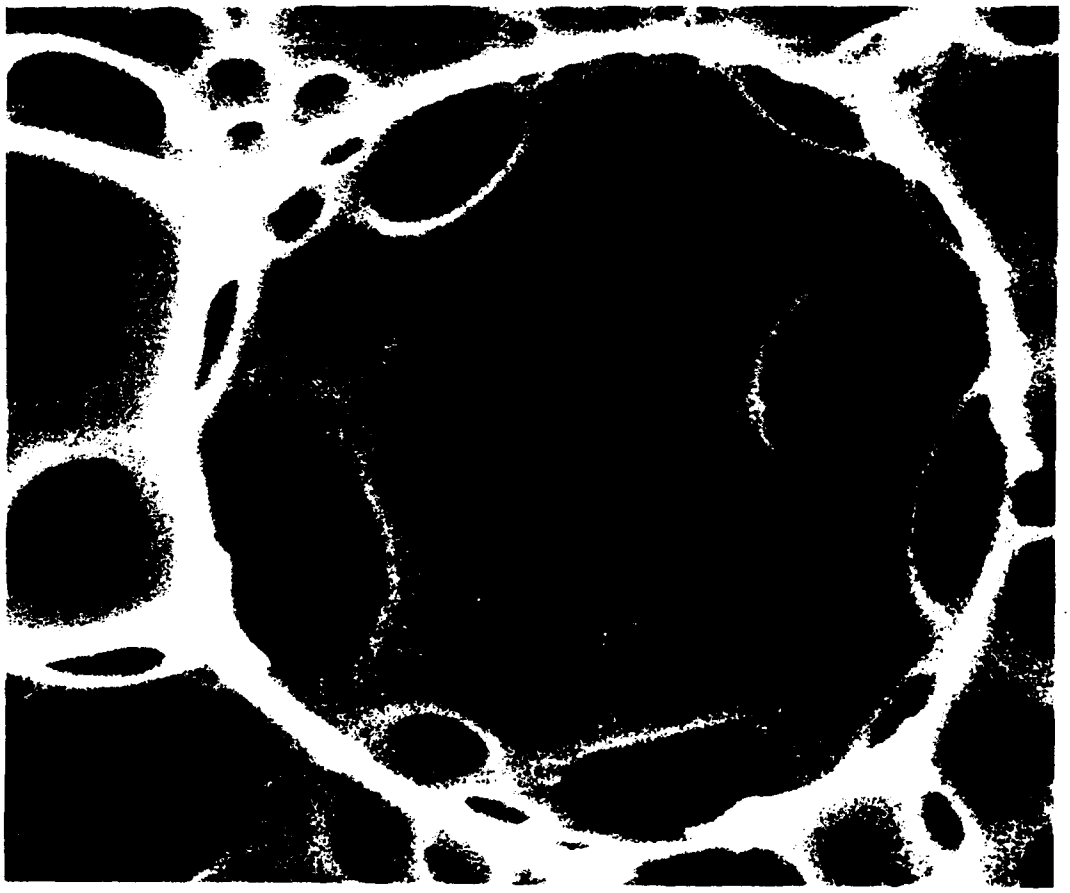


Fig. 75. Electron micrograph of the polystyrene wick structure showing pores.

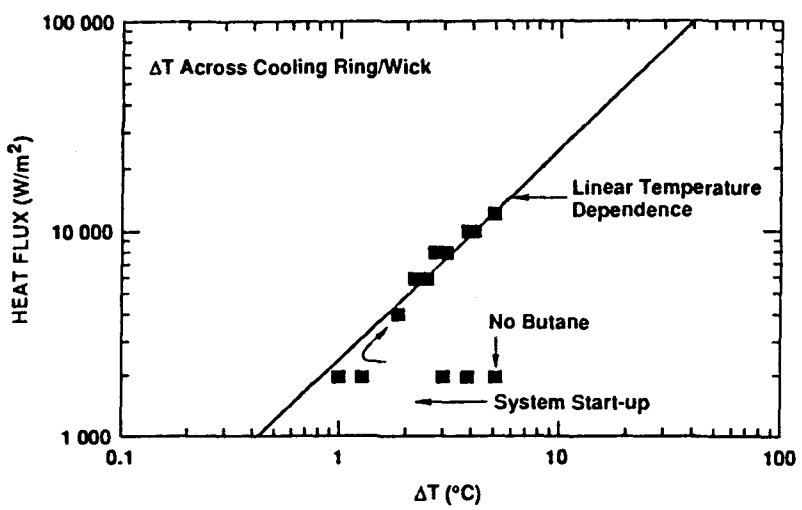


Fig. 76. Cooling surface heat flux expressed as a function of temperature difference between heated surface and saturated butane vapor.

control response mechanism will be to vary the temperature at the liquid vapor interface. As condensate accumulates in the bottom of the condenser, part of the condenser tubes will be submerged. The temperature of the interface between the liquid and the vapor will govern the system saturation temperature and pressure. By actively controlling the temperature at the liquid vapor interface the saturation pressure and operating temperature of the system can be regulated.

A 12 kW butane condenser operating at 0°C can be easily realized with a 20-tube shell-and-tube condenser bearing 0.5 m-long tubes. The 20 tubes could be accommodated in a smaller diameter shell, but it is desirable to keep the tube spacing large so as to minimize the vapor velocities and the resulting pressure drop. The condenser design will be optimized to suit geometric constraints when those constraints are better characterized. Stainless steel has been selected as the wall material for the condenser for ease of fabrication, strength, and resistance to corrosion.

3.3 System Start-up Procedure

Prior to initial detector start-up or restart following any shutdown, the detector containment shell will be filled with room temperature air at the local humidity. A start-up procedure is required that completely replaces this air with 0°C butane without damaging the detector system and without endangering the safety of personnel due to exposure to flammable mixtures of air and butane. Butane is flammable in air only if the volume percent of butane is between 1.9% and 8.5%. Start-up begins with the replacement of the room temperature air with room temperature dry N_2. This N_2 will be introduced to the bottom of the containment vessel through a gas feed line at the bottom of the vessel. O_2 sensors within the vessel monitor the decrease in O_2 until the percent by volume drops to near zero. The exhausted air will be vented directly to the surface through a bypass in an existing line that is provided for the emergency release of a high pressure condition within the vessel. At this time, both the N_2 inlet and air-N_2 outlet line will be valved off and the system allowed to rest. During this rest period, the O_2 level in the vicinity of the O_2 sensors may increase due to diffusion from relatively stagnant regions within the vessel. In this event, the warm, dry N_2 flush will be continued, as necessary. It is now safe to introduce the butane, but it is desirable to pre-cool the system to the operating temperature. This will be accomplished by introducing cold N_2 in the same manner as was done with the room temperature N_2, except that the N_2 source will be an LN_2 supply that will be allowed to expand and warm to about −10°C. The N_2 will be exhausted from the vessel as before. During the above processes, the condenser has been isolated from the vessel and evacuated by a vacuum pump at the surface through an exhaust tube. Butane has subsequently been introduced into the condenser by a standard fill procedure.

Once the detector system is filled with cold N_2 and the system is at temperature, liquid butane will be slowly introduced at 0°C to the bottom of the containment vessel. The amount and flow rate will to controlled so as to minimize mixing of the vapor resulting from the evaporation of the butane with the N_2 in the vessel. In this way a significant fraction of the N_2 in the vessel can be exhausted directly to the surface. Butane sensors within this exhaust line will monitor the percentage of butane and, at the appropriate butane concentration, as determined by safely regulations, close the exhaust line and open the vapor line to the condenser. At this time the liquid butane supply to the detector array will be switched from the bottom feed to the normal liquid feed system. A significant fraction of the gas leaving the containment vessel and entering the condenser will be N_2.The N_2 will cause a decrease in the heat removal capacity of the condenser. When the capacity is reduced to an unacceptable level, as apparent by an increase in pressure and temperature, the pressure build-up will be relieved and the escaping mixture directed to a cold trap. The cold trap is essentially a condenser operating at significantly lower temperature. It can be used to reduce the fraction of butane to any desired level. The cold trap operating at −73°C prevents the partial pressure of butane from exceeding 2000 Pa. In this case, a mixture of N_2 and 2% by volume butane is vented to the surface, which is sufficiently low in butane concentration to eliminate any fire hazard after venting, unless separation occurs before dispersion. A venting and/or burn-off procedure is part of the system safety plan currently under review. Other viable options are available which do not require a cold trap at this low temperature. For example, the gas mixture removed from the condenser at 0°C could be mixed with additional N_2 at that temperature before venting to the surface at any desired concentration. Another option is to vent the mixture as is, add O_2 sufficient for complete combustion, and burn off the butane at the surface. In time, the accumulation of N_2 in the condenser will be minimal. The system is then ready for the electronic heat load. Any subsequent accumulation of N_2 in the condenser will be evidenced by a degradation in condenser performance. At such times, the condenser will be relieved of excess pressure as was done during the start-up. Proper condenser design should allow for partial separation of the lower density N_2 so that a minimal amount of butane need be removed with the noncondensable.

4. Wick Investigations

Detector cooling system research and development during FY 92 will concentrate on development and testing manufacturable polystyrene wick structures, the construction of a fully functional prototypical detector cooling system, and completion of several major safety assessments for approval from the SSCL.

Molds and procedures for polystyrene foam wick structure fabrication must be

developed. This effort consists of an exploratory phase that will require adaptation of an existing automatic syringe system to provide mold filling capability. A mold material that will promote precision molding will be selected. The mold will then be designed, fabricated, and tested with various polystyrene mixtures. The exploratory portion of this effort will probably require several iterations before a satisfactory procedure is developed.

An experimental prototype of the heat pipe wicking-silicon wafer configuration with liquid supply lines will be designed and fabricated. This prototype will simulate the silicon wafer-cooling ring segment. Resistive heat loads will be placed atop the wafers to simulate the electronics heat dissipation. The most promising artery-wick design will be used on the cooling ring. Closed loop operation with feed back will be established between the condenser and the evaporator sections. A complete experimental testing program will be completed using this representative cooling ring-silicon assembly. Startup, operational transients, and shutdown principles will be demonstrated. Performance limits including boiling and/or capillary limiting heat fluxes will be determined. The operating limits will be evaluated and correlated to characterize system thermal performance.

F. Butane Cooling System Safety Plan

The evaporative cooling system is being designed in accordance with SSC specific policies and procedures. These policies incorporate numerous federal regulations, design codes, and orders including: NFPA 101 Life Safety Code, NFPA 58 Standard for the Storage and Handling of Liquefied Petroleum Gases, MIL STD 882, ASME Boiler and Pressure Vessel Code, ANSI Standard B31.3, OSHA 29 CFR 1910, DOE Orders 5480.4, and DOE order 5483.1A.

Analysis reports are required by the SSCL from individual subsystem developers at each stage of the safety review process. The butane cooling system will be examined at length for its compliance to OSHA and DOE safety regulations. The review process consists of four stages, each requiring input from the STS, these stages are: the Preliminary Hazard Assessment (PHA), the Preliminary Safety Analysis Report (PSAR), the Safety Analysis Report (SAR), and the Final Safety Analysis Report (FSAR). The PHA and the PSAR must be submitted and approved by SSCL during FY92. A PHA of the Butane Cooling System is due April 1, 1992 with the Subsystem Technical Proposal. The PHA is to be largely qualitative, identifying potential problems in the subsystem design. The PSAR, SAR, and FSAR are to contain quantitative risk evaluations. The Butane Cooling System PSAR is due September 1, 1992. This effort includes the analysis and the preparation of these reports to be submitted to the SSCL.

The baseline detector design operates with butane vapor at a slightly positive gage pressure. A positive pressure ensures that leaks flow out of the detector and prevents oxygen and other noncondensables from entering the detector volume. At this point, the two primary fluid candidates are butane and isobutane, based on their normal boiling points, availability, and cost. The butane or isobutane will be instrument grade (99.5 percent) or purer to prevent higher vapor pressure impurities from increasing the system pressure significantly above atmospheric pressure at the design temperature. A positive operating pressure requires operation at above −10°C for isobutane or −0.5°C for butane.

The potential flamability of a hydrocarbon in air is bounded by lean and rich limits, also referred to as lower and upper explosive limits. These are the limits, expressed as a percentage either by volume or of stoichiometric mixture, between which, if ignition occurs, combustion will propagate through the mixture. For butane in air, the lean and rich limits are 1.9 and 8.5 volume percent. These values are typical of the hydrocarbons, although the lean limit can be as low as 1 percent (octane) and the rich limit as high as 14 percent (methane). Safe operation of a positive pressure system can be achieved by the detection and measurement of hydrocarbons in air by a well-established technology based on catalytic combustion. These sensors can detect from 0%–100% of the lower explosive limit (LEL) or the lean limit. They can be used to sound an alarm and to actuate the response plan.

In the STS cooling loop, most of the working fluid inventory during operation is located in the condenser and the liquid feed lines. The total working fluid inventory will be less than 2 gallons of liquid butane. All structures containing working fluid are to be double enclosed whenever possible, with the outer enclosure filled with flowing nitrogen gas. All seals and joints shall be designed to be leak tight. Both hydrocarbon and oxygen sensors are to be placed inside the enclosure for early detection of leaks. An appropriate response to a leak is to vent the system either to the open atmosphere outside the detector hall or to a tank available for that purpose. Additional sensors would be placed outside the double enclosure to detect leaks from other parts of the system. The responses to a significant leak outside the detector containment would include closing valves to isolate that part of the system and venting the containment vessel to the surface.

In addition to the precautions mentioned above, several interlock mechanisms will be placed in the detector to prevent potential damage in the case of a loss of cooling capacity. Interlocks between the condenser refrigeration system and the detector power supply will shut off the electronics in the event of a refrigeration system failure. A pressure-activated interlock will also be placed between the liquid return line solenoid valve and the detector power supply. This will shut off the electronics if the liquid supply to the detector is interrupted.

G. Alignment and Assembly Considerations

The overall alignment and assembly concept must be integrated with the mechanical structure in many important ways. First of all, the concept must provide a method for positioning silicon ladders to micron scale accuracies while they are being attached to the cooling rings and provide a method to integrate the structural shells and forward region planar arrays onto the detector space frame. Second, the concept must include alignment considerations for the completed detector including alignment shifts in shipping, reassembling and positioning the detector onto the SSC beam line, *in situ* alignment, verification, and calibration, and maintaining knowledge of alignment changes over the operating life of the detector. These are not the only alignment and assembly tasks, because component and subassembly testing, structural verification, and correlation of test data with FE models are important parts of the overall alignment and assembly process.

One of the most important and challenging alignment tasks is realizing an alignment maintenance system for the calibrated detector. This is an especially important operational system because calibration is a time consuming activity. With a recently developed fiber optic system, it will be possible to continuously monitor the relative 3-dimensional position of one subassembly relative to another and the position of the detector to the outside world using a compact, non-intrusive system. For this to be possible, the integrity and stability of the subassemblies must be assured so that the subassemblies can be treated as rigid bodies. This is another important reason for careful subassembly testing.

1. Alignment Concepts

Concepts have been developed for most of the important detector alignment and assembly tasks. Proof of principle alignment and assembly demonstrations are now being developed. Figure 77 outlines the major alignment tasks: (1) place the silicon ladders onto the cooling rings, (2) assemble silicon shell modules onto graphite/epoxy structural shells, (3) place assemblies from step 2 into the space frame, (4) build the forward region subassemblies and attach them to the space frame, (5) place the assembled detector onto the SSC beam line, and (6) monitor alignment status throughout the detector lifetime.

Initial tolerance goals for internal detector alignment and alignment relative to other detector systems have been defined and are listed in Table 28.

A survey of available alignment equipment reveals that the tolerances listed in Table 28 are within the existing capability of off-the-shelf measurement and alignment equipment. The challenges are to adapt and customize commercially available equipment to the required alignment tasks without compromising their

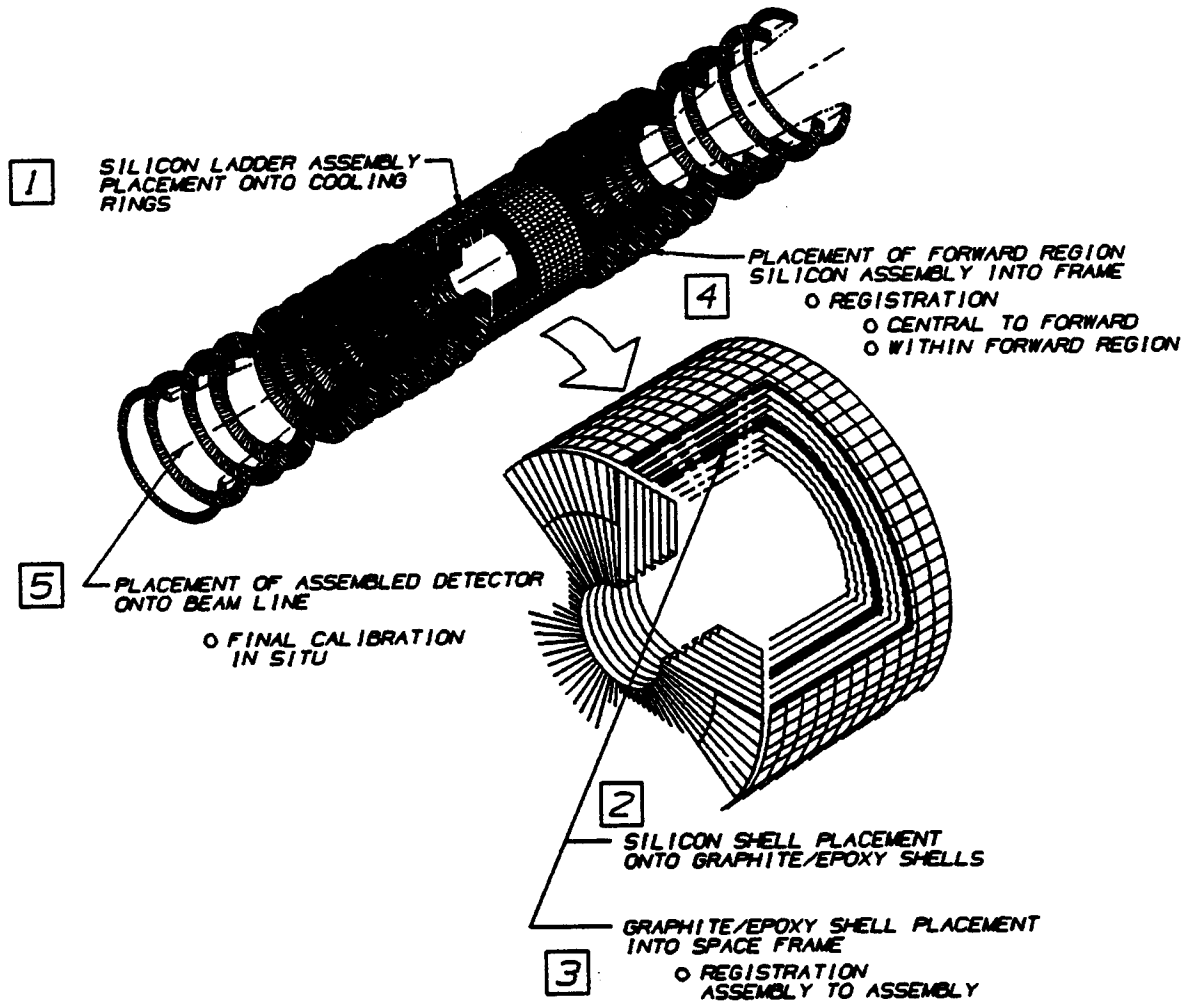


Fig. 77. Detector alignment and assembly tasks.

accuracy and develop concepts for the always difficult tasks of verification and alignment maintenance during shipping and operation.

An alignment concept for assembling the silicon ladders onto cooling rings is shown in Fig. 78. The essence of the approach is to establish and maintain an assembly axis and to precision-place four microscopes, in sets of two one above the other, to observe ladder placement onto the cooling rings. There is a sequence of detailed set-up, verification, and checkout procedures to establish the assembly axis, microscope positions, and cooling ring orientation; but once these are established, the ladders will be systematically guided into position by watching targets on each end of the ladders with the microscopes. Once the first ladder is placed, the cooling rings are rotated until the first ladder is in its rotated correct position,

Table 28. Summary of Maximum Positioning and System Errors.

Maximum uncorrelated positioning errors:		
Silicon detector:	Circumferential	5 μm
	Radial	80 μm
	Longitudinal	250 μm
Straw superlayer:	Circumferential	35 μm
	Radial	1200 μm
	Longitudinal	250 μm
Maximum correlated system error, silicon relative to straws:		
Rotational alignment:		10^{-5} radians
Radial alignment:		600 μm
Longitudinal coordinate:		250 μm
Displacement of detector centroids:		15 μm

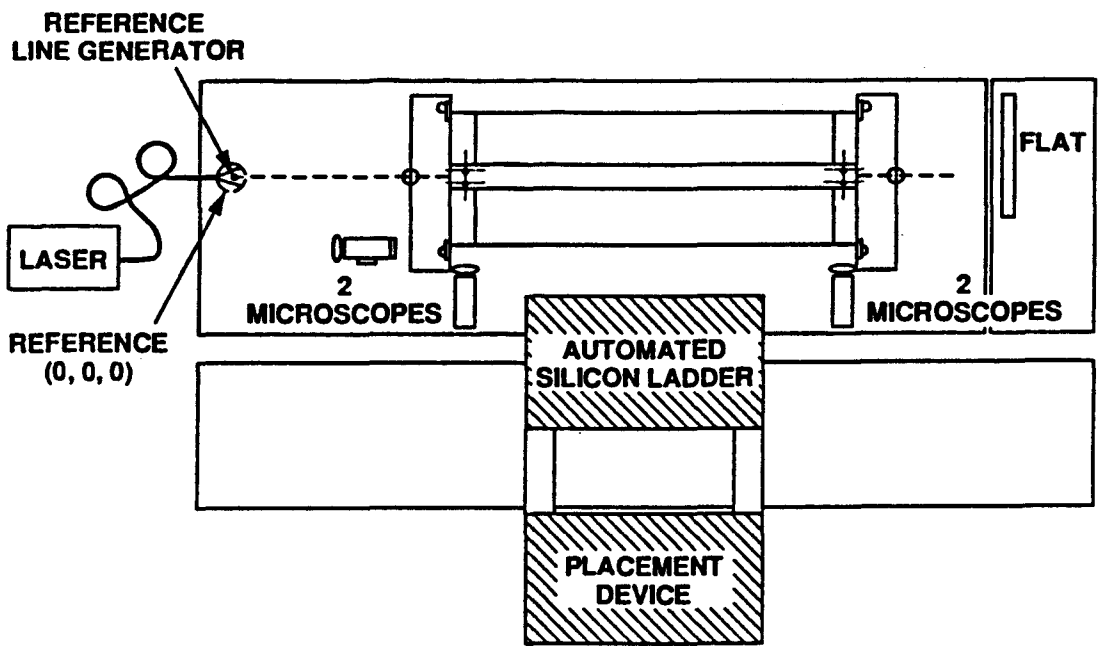


Fig. 78. Conceptual alignment schematic for assembling silicon ladders onto cooling rings.

which is monitored by the two microscopes, one at each end, directly above the first set; then, the next ladder is moved into position and placed, just as the first ladder was placed. This process is continued until a complete shell is built. Provided that the microscopes are properly placed, this alignment approach does not allow errors to build up as ladders are placed around the cooling ring circumference because each ladder is placed independently by the same microscopes. Once a shell

assembly is completed, the kinematic mount assemblies on the cooling rings are precisely located by auto-collimating by means of spheres and locating the spheres relative to targets on the ladders. The kinematic spheres will be used to locate the completed shells relative to other shells and other detectors. As shells are attached to the space frame, rad-hard fused silicon fiber motion sensors will also be attached to every shell to monitor 3-D motions of the previous shell in the assembly. In this way alignment status is passed from the inner shell to the outer shells and to the reference system outside the detector. In this way, the alignment status of the detector can be monitored continually over the lifetime of the detector, from initial assembly through shipping and installation and after final calibration during operational use. In addition, the same technique can be used to monitor the detector's position relative to the outside world to determine the status of the overall detector alignment relative to beam parameters and other detector systems.

Alignment and assembly techniques for the forward region are not yet as fully developed as for the barrel region, but they will surely be modifications and adaptations of the techniques used to build, align, and maintain the barrel region alignment. An additional technique, which uses an infrared laser that could pass through the ladders and be observed by a camera, might be useful for placement of the large plate assemblies relative to each other and for end-to-end registration. Such a technique might also be useful for alignment verification as the subassemblies are built into the complete detector.

The final proof of alignment and assembly is a direct verification and calibration. X-rays from a precisely positioned collimated source are directed through the detector and interactions are detected with the electronic circuitry. If the subassemblies are well characterized and can be treated as rigid bodies, then the final mapping and calibration process would be greatly simplified. It is our ultimate goal to align and assemble the detector so that X-ray mapping and calibration will be easy and quick. Once the detector is calibrated the 3-dimensional fiber optic monitoring system can monitor alignment status during the operational life of the detector.

2. Optical Techniques to Optimize and Verify Subsystem Designs and Mechanical Stability

Complete knowledge of subassembly mechanical properties is the key to a well understood assembled detector. Quantitative and qualitative information about small and large subassemblies with micron resolution over a large field of view are needed to verify and optimize mechanical designs. To gather the required information, we are developing a state-of-the-art TV holography system. TV holography systems have been built before, but only the latest systems, which are not available commercially, provide quantitative data. These systems will provide detailed

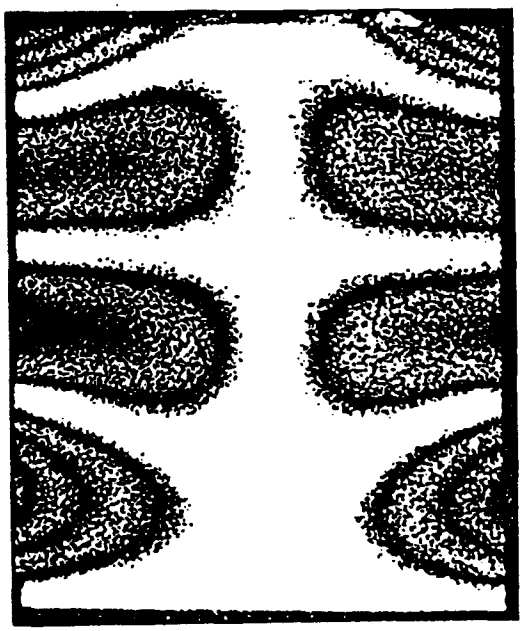
quantitative, as well as, qualitative information about structural integrity, shape, shape changes, structural stability, vibration resonant frequencies and their resonance Q. The results will be used to evaluate and optimize subassembly designs, aid in the choice of appropriate adhesives and bench mark finite element models. The experimentally tested analytical models can then be used with increased confidence for predicting many detector mechanical performance features and structural performance characteristics under unusual operating conditions. The information needed for design verification will be gathered on prototypes rather than on the detector for the SSC. The prototype information needs to be sufficient to predict with confidence the performance of real detector parts and assemblies.

Shape changes under heat or mechanical loads are a direct measurement of the mechanical stability of major subassemblies. TV holography is an ideal tool to use for stability testing. But, there are two important limitations: 1. TV holography is an optical technique; only surfaces which can be exposed to a light beam, can be observed, and 2. the surfaces being observed cannot be specular reflectors.

An example of TV holography data is shown in Figure 79. The test piece is a 115-mm-wide, 135-mm-high, 2.3-mm-thick cantilever plate vibrating at 3787 Hz. The contour fringes, which are displayed in real time on a TV monitor, give useful qualitative information about the vibrating plate. Recently developed techniques for gathering and processing contour fringes lead to the quantitative information about the mode shape and vibration amplitude shown in the wire frame plot. Both types of information are useful: the qualitative information for quick, full view inspection, and the quantitative data for detailed comparison with analysis. When mechanical forces, electronic heat loads or forced heating/cooling are applied to the structure similar displays and results are gathered for design analysis and verification.

In summary, TV holography is an ideal tool to use for testing and optimizing silicon detector mechanical designs, measuring the structural stability of prototype ladder assemblies attached to cooling rings and the structural stability of complete prototype shells under typical or abnormal operating conditions.

a)



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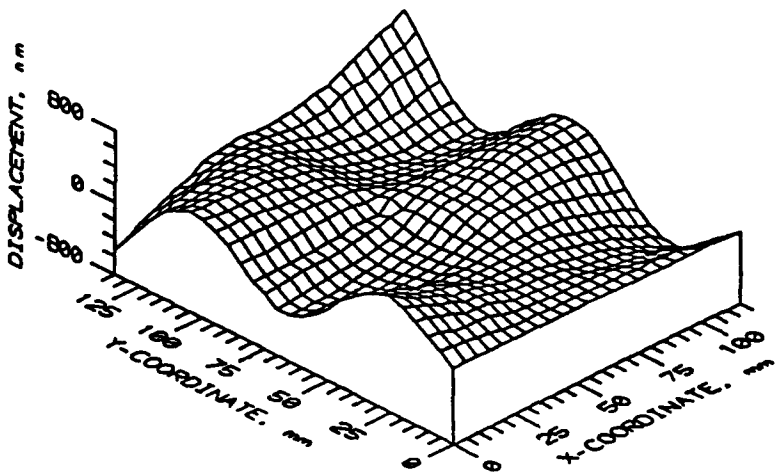

Fig. 79. Cantilever plate vibrating at 3787 Hz: (a) image of the plate and the fringe pattern produced by the TV holography system during the time-average recording of the plate vibrating at its resonance without bias modulation of the object beam, (b) wire frame representation of displacements computed from the images recorded.

VII. Material in Detector

To better understand the impact of the various materials included in the detector configuration, a detailed model of the silicon detector system with its supports and services was developed. The amount of material in different components was calculated as a function of rapidity and phi using RTRACE, a package in the SDC simulation program SDCSIM.

RTRACE calculates the radiation length, nuclear absorption length, and geometric extent of materials as a function of rapidity/phi. It does that by propagating geantinos—massless, noninteracting, neutral particles—through the detector and adding up the material they traverse at each rapidity/phi value. The origin of the geantino can be fixed, or defined to have a uniform or Gaussian distribution.

RTRACE also calculates the length of the lever arm of the detector systems, both radially and along the beam axis. There are options for averaging quantities over the location of the origin, the rapidity, or phi.

In the data shown here, at each rapidity/phi value, twenty geantinos propagate through the detector from vertex locations that are smeared in x, y, and z according to Gaussian distributions. The standard deviations are 0.0005 cm, 0.0005 cm, and 5.0 cm, respectively. These values correspond to the best estimate of the actual beam-crossing size at the SSC. The resulting radiation lengths and crossing counts are averaged to produce one point at each rapidity value. Because all components except the space frame are symmetric in phi, all but the space frame calculations are at a single value of phi. The space frame has a twelve-fold symmetry in phi. Its contribution to the total radiation length at each rapidity value is an average over a 30° span in half-degree steps. The detector model includes all elements listed in Table 29.

Figure 80 shows the material in the silicon detectors alone as a function of rapidity. Figure 81 shows the radiation length as a function of rapidity for all silicon tracker components modeled and the beryllium beam pipe. There is 5.4% of a radiation length at 90°; this slowly rises to about 8.5% around a rapidity of 0.8, then tapers off slowly until a rapidity of 1.8, where there is some variation as the boundaries of components are reached. Above a rapidity of 2.5, material contributions are solely attributable to the beam pipe, inner wall and endplates of the enclosure vessel, and the butane gas atmosphere.

Table 29. Detector and Material Parameters

Component	Material	Radiation Length (cm)	Thickness (cm)	Average X_0 at 90° (%)	Comments
beam pipe	beryllium	35.3	0.036	0.10	at r = 2.5 cm
inner enclosure vessel	beryllium	35.3	0.072	0.20	at r = 5.0 cm
outer enclosure vessel	graphite/epoxy	24.9	0.071	0.29	at r = 50 cm, length = 530 cm
silicon detectors	silicon	9.36	0.030	2.56	cylinders and disks, 8 at 90°
barrel support	graphite/epoxy	24.9	0.071	0.57	between layers 2 and 3 and 6 and 7
space frame	Mg MMC	16.80	0.110	0.05	tubes of 2.54 OD in a hexagonal arrangement
cooling ring	graphite/epoxy	24.9	0.045		rings of rectangular cross section, 3 cm long by 0.8 cm wide
wick	liquid butane	148	0.040		against three insides of each cooling ring
silicon chips	silicon	9.36	0.030		width = 1.3 cm
kapton substrate	kapton	28.4	0.020		width = 2.6 cm
beryllium shield	beryllium	35.3	0.030		width = 2.6 cm
cabling	beryllium	35.3	variable		both power and signal: 0.063 cm at the inner face of the outer wall of the enclosure vessel; also annular disks extending from there to the innermost detector layer, and located in the 2 gaps between the barrel and forward regions
filler gas	gaseous butane	16000.	filler	0.28	fills remaining space inside enclosure vessel

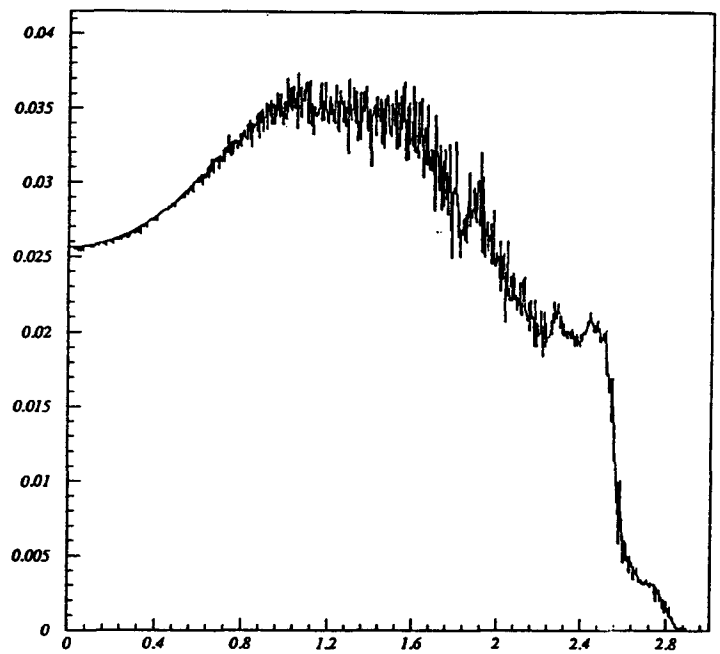

Fig. 80. Average fraction of a radiation length as a function of rapidity in the silicon detectors alone.

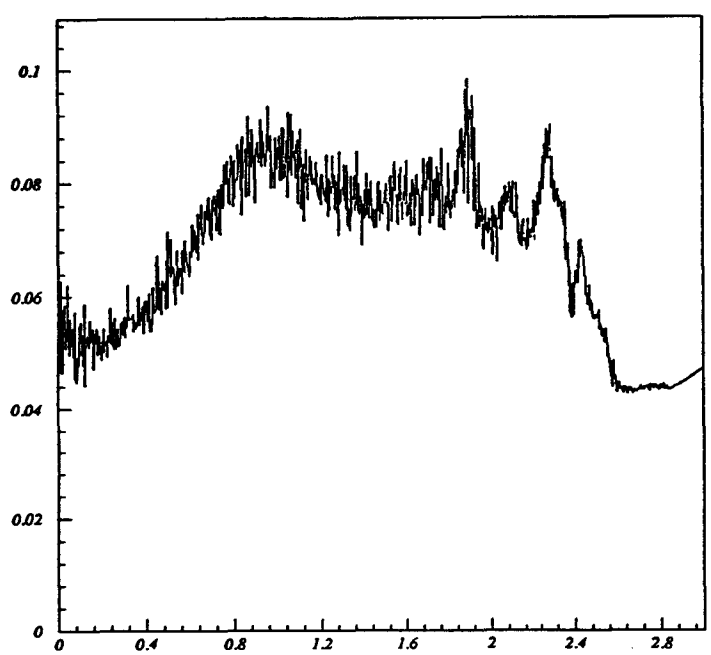

Fig. 81. Average fraction of a radiation length in the entire silicon tracker (including supports and services) and the beam pipe as a function of rapidity.

VIII. Pixel Detector Option

A. Role of Pixel Detector

High quality track detection close to the beam pipe is very desirable for improved momentum resolution and for increased definition of primary and secondary vertices and improved pattern recognition. At the same time, the very high radiation levels and track densities close to the beams create a difficult technical challenge. It appears that pixel detectors based on contemporary hybrid silicon technology can best provide the needed tracking capability with sufficient radiation hardness. There is very little experience within the high energy physics community as yet with pixel devices, but the level of activity focussed on adapting this technology to the SSC has been increasing steadily[36]. The main efforts currently are on VLSI circuit design, architectural studies, and mechanical systems, all of which have produced significant results.

In addition to superb secondary vertex detection, pixel detectors might provide a very substantial enhancement of pattern recognition capability, reducing the computational effort by a very large factor. The incorporation of pixel detectors in the pattern recognition process could radically change the overall strategy, and make possible an approach that is fast, linear with track density, and amenable to implementation with specialized processors. The pixel detectors would permit the pattern recognition process to begin at a radius of a few cm. At such small radii, the effect of curvature is minimized and it is possible to find tracks and event origins with a simple, but very efficient, linear algorithm.

B. Technology: Hybrid or Monolithic?

In a hybrid technology, pixel detectors are made by joining two independently fabricated silicon devices by a matrix of metallic bonds. "Bumps" of gold, indium, and solder are among the possible materials that have been successfully employed. In the present case, one silicon device is a p-i-n detector with the appropriate pixel pattern on the n side, and the other is a radiation hard CMOS VLSI integrated circuit. Separate processing permits optimization of each device. Costs may be greater than with a monolithic approach, but all the required technological elements appear to be mature.

In a monolithic technology, the detector and readout circuitry are fabricated simultaneously within a single wafer, although the wafer may itself be "composite". The advantages of a monolithic technology derive mainly from working with a "chip" that may be more robust physically, less costly ultimately, and which should offer a slightly smaller overall material thickness. In this case, the technology is still developing, and it is not possible yet to define a convincing schedule for completion. Nevertheless, very substantial progress has been made at LBL,

and separately by the Hawaii-Stanford (CIS) collaboration. At LBL, a high-performance CMOS process has been demonstrated in high resistivity silicon; at Hawaii-Stanford, monolithic PMOS pixel arrays (CMOS periphery) have been successfully tested with particle beams, showing excellent charge collection and spatial resolution. In both cases, however, radiation hardness remains to be incorporated and/or demonstrated.

Because the hybrid technology is the only one for which a clear technological path is available, this approach has been emphasized in current engineering effort and schedule development. Nevertheless, new avenues for monolithic integration will continue to be explored as resources permit.

The thickness of the p-i-n detector is envisaged to be between 250 and 300 μm thick. Although the pixel detector can function well with detectors thinner than 250 μm, such thin wafers cause processing difficulties. The readout IC may be thinned after fabrication to only 50 μm, to minimize material. Our industrial partner, Hughes Aircraft Company, has extensive experience with an indium bump process (256×256 arrays are routinely fabricated, with bump densities exceeding $10^5/\mathrm{cm}^2$). Hughes also has capabilities for readout thinning to 50 μm.

The maximum size of the hybrid is determined in part by yield considerations, and in part by rate effects during SSC operation. In the present case, our standards for yield would be considerably less stringent than for typical commercial devices, as a dead pixel or two, or even several, may have a negligible effect on efficiency.

C. Physical Arrangement and Rates

The pixel detector is envisaged as a two layer barrel with two disks at each end, covering a rapidity interval of about ± 2 units of η. The extended luminous region along z makes the boundaries of η coverage fuzzy. The proposed geometry is given in Figs. 82–84.

Because of the extended length along z of the luminous region, tracks in the central region can traverse the pixel detector over an angular range of more than $\pm 45°$ in the r–z plane. For the more inclined tracks, the deposited charge will be shared among several pixels along z if the pixel length is short compared to the $\simeq 250$ μm detector thickness. Sharing charge over many pixels substantially reduces the S/N ratio. From the limited perspective of preserving a high S/N ratio, therefore, there is a "natural" pixel length of about 250 μm along z.

For vertex reconstruction purposes, however, a much smaller dimension is desired. The ideal resolution is on the order of 5 μm rms in both r–ϕ and r–z. Square pixels, $\sim 40 \times 40$ $\mu\mathrm{m}^2$, would be nearly ideal. It does not appear feasible with current technology to pack the needed circuitry into such a small area. A choice can be made between large, square pixels, or rectangular pixels of equal area, which

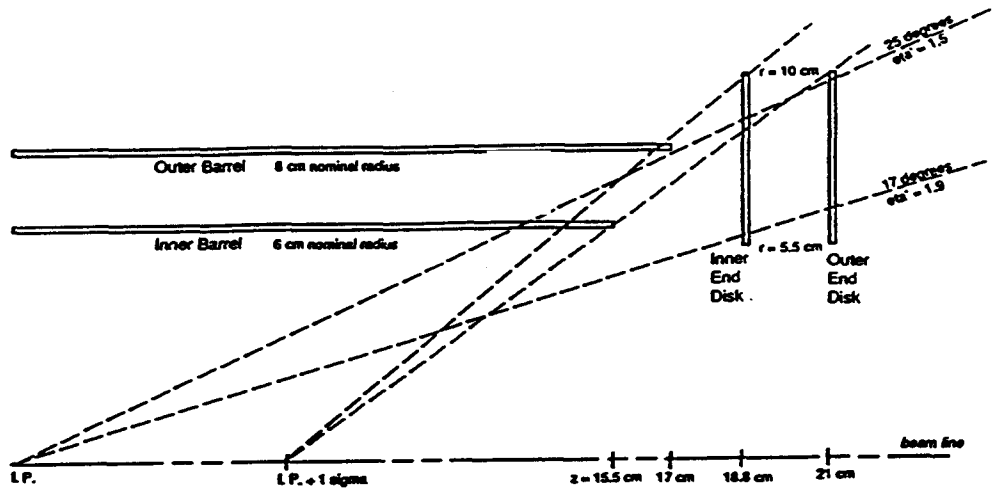

Fig. 82. Diagram of pixel vertex detector layout.

can at least provide good resolution in one dimension. For rectangular pixels with short dimension of about 50 μm, the long dimension appears to be approximately the "natural" length mentioned above. Whether a rectangular pixel is the right choice for physics has not yet been demonstrated through simulation.

The "natural" dimension in the r–ϕ plane is $\simeq$ 50 μm, and is given by simple geometric relationships encountered in covering a cylindrical surface with finite planar shingles. In the following discussion, the pixel cells are taken to be 50 μm$\times$250 μm, with the long dimension parallel to the beam axis. With the illustrated geometry, there are about 2×10^7 pixels in the system, and $\sim$ 0.25 m^2 of active silicon.

At the standard SSC design luminosity, 10^{33}cm^{-2}sec^{-1}, and at a radius of 6 cm from the beams, pixel cells of this area will be struck at about 340 Hz. The pixel array itself is taken to be 256 rows $\times$ 64 columns, giving an active area of 1.28 cm $\times$ 1.6 cm = 2.048 cm^2, and a total pixel count of 16384. The array can be subdivided electrically into two, three, or even four semi-independent interdigitated pieces to permit separate readout of adjacent rows for charge interpolation, e.g., for three, every third pixel along a column would be connected to a common hit line. In the case of subdivision into four parts, the row and column activity levels are nearly equal. Sub-division into two parts is probably not the optimum choice, as charge sharing can frequently involve a pixel and both neighbors. In what follows, it is assumed that the array is subdivided into four parts.

The array as a whole will be struck by primary tracks at a rate of 5.6 MHz. The chance of the array being hit on any given beam crossing is 9%, a rather

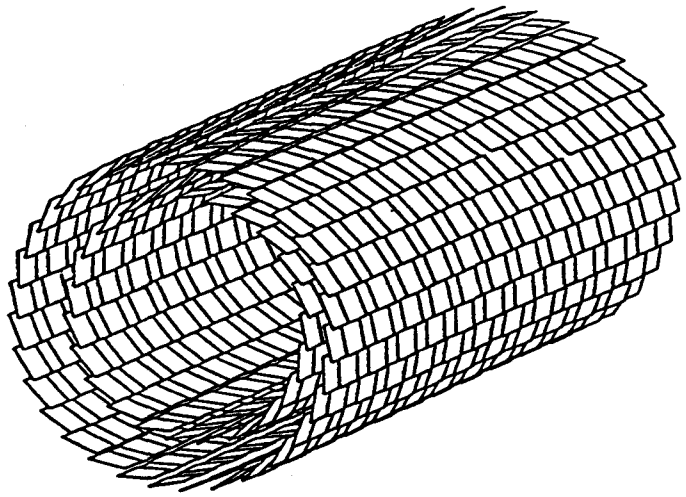

Fig. 83. Arrangement of pixel arrays in barrel module.

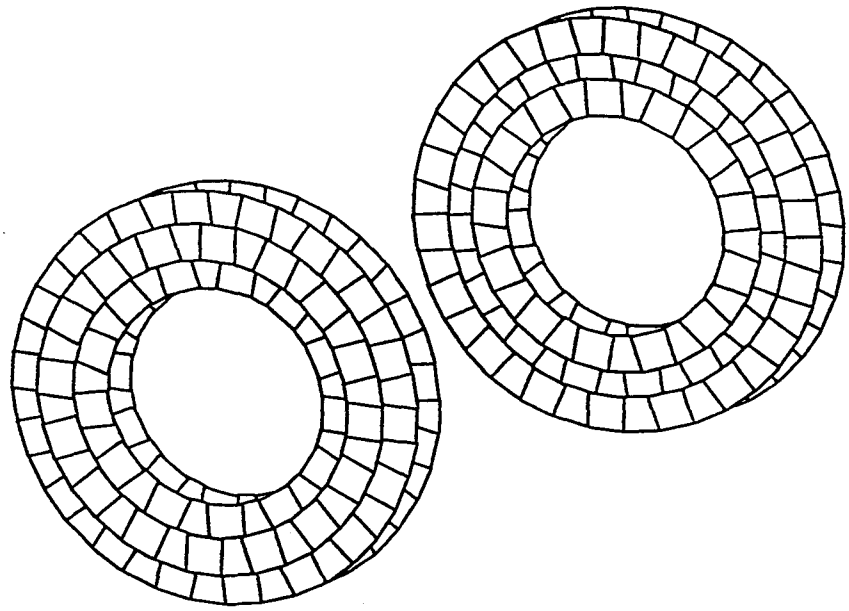

Fig. 84. Arrangement of pixel arrays in disk modules.

large probability. This fact has a major impact on circuit architecture, ruling out centrally managed activity, except during valid data readout.

D. Radiation Hardness Issues

Both detectors and readout IC's must survive radiation doses in excess of 10^4 Gy/year. There exist now quite encouraging results concerning the UTMC process, presented within SDC, and reports have occurred in the literature discussing CMOS performance even at the 10^6 Gy level. Needless to say, the pixel detector faces the most severe radiation levels within the tracking system, and much work remains to be done to establish viability beyond reasonable doubt.

The situation regarding detectors is also encouraging. Although annealing effects are poorly understood, low-temperature operation may reduce the formation of twinned defects due to suppressed defect migration rates. In any event, the recent data suggest that the cumulative effects of impurity creation/removal are not overwhelming. Charge collection appears to be nearly constant even above fluences of 10^{14} particles/cm^2.

Since the radiation effects lead to n $\rightarrow$ p type-inversion, or increasingly p-type material, it is natural to arrange the junction and pixel pattern at the n^+ side. Because the pixel detector is single-sided, it is possible to operate the system quite effectively with partially depleted detectors. This is not the case for the double-sided strip system, which must always be operated in an over-depleted mode. When a voltage limit is reached, the depletion depth will shrink rather gradually, as the square root of the fluence. The pixel detector system should thus experience a graceful maturity, at least from the perspective of available signal. The single-sided pixel detector also allows the ExB tilt angle to be optimized for a single carrier, since the compensating tilt angles are quite different for holes and electrons. The choice of n-side readout also has the advantage that the pixel signal is derived from the electron current, which is considerably faster than the holes.

The effects of detector leakage current are expected to be very small for the pixel detector, even at very large fluences. The pixel array, by its large segmentation, partitions the leakage current to tiny values. Because of this, the detector may not even need to be AC-coupled, using the pixel cell design discussed below.

The effects of radiation on the Foresight 1 pixel cell, fabricated by Hughes in an SOS CMOS process, are being studied at SLAC. This proof-principle-device contains a charge-sensitive preamplifier, a comparator, and a charge-storage element in a 50×150 μm^2 cell. This Hughes SOS process is expected to operate to the one MRad level, and will provide us with valuable experience; the desired radiation hardness is ultimately at the 10 MRad level.

E. Pixel Cell

The pixel cell is envisaged to operate in an autonomous fashion, requiring no resets or clocks to establish a quiescent, sensitive state. Thresholds and biases are controlled by DC levels. During operation, the only interaction of the peripheral circuitry with the pixel cell is during trigger level 1 valid data readout, to eliminate ambiguities. Signal communication with the periphery is accomplished using currents, rather than voltage swings, to reduce noise from parasitic couplings to a negligible level. Design principles that maximize radiation hardness must be incorporated *a priori*, increasing the size somewhat. The block diagram of the proposed pixel cell is indicated in Fig. 85. Many of the features have been successfully tested in an "advanced" design made by LBL.

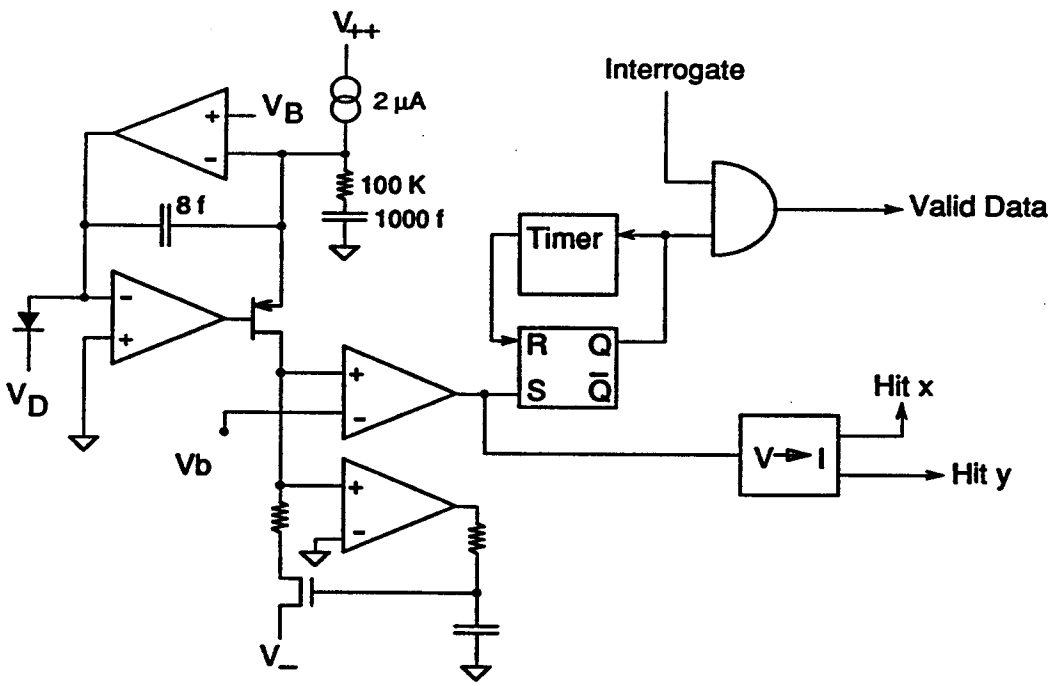

Fig. 85. The proposed pixel cell architecture.

At the amplifier input, the very small capacitance of an individual pixel, C_p, offers important dividends in circuit design. C_p is expected to be about one fourth of a pF. This provides the possibility, with careful design, of electronic noise of much less than 100 electrons rms, corresponding to a signal/noise ratio S/N in excess of 200. In turn, this large intrinsic S/N ratio offers the circuit designer headroom to

optimize trade-offs among power dissipation, circuit size, noise, speed, and possible signal loss due to radiation damage of detectors.

To obtain the full extent of this advantage, it is necessary to include in each pixel cell a charge-sensitive amplifier, a bandwidth width limiting shaping element, and a comparator. The operating point of the charge-sensitive amplifier is maintained by an active feedback current source, taking the place of the traditional resistor. With this design, the detector leakage current is directly absorbed at the amplifier input, eliminating the need for AC-coupled detectors and a possible resistive noise source. The feedback current source, combined with a CR differentiator ($\tau = 100$ nsec) at the charge sensitive amplifier output, roll off low-frequency noise components very effectively. Even at large fluences, shot noise should be a small contribution to the overall S/N ratio.

This circuitry leads to pixel cell areas on the order of $\simeq (50 \times 350) = 17500\ \mu m^2$ in a 1.2 μm CMOS technology. While uncomfortably large, this is perhaps still acceptable, and effort will be focussed this coming year on reducing the length to about 250 μm.

Hughes Aircraft Co. has developed "Foresight 4", a 32×64 array of compact pixel cells with analog memory. The dimensions of the pixel cell are $50 \times 150\ \mu m^2$, realized in a 1.2 μm CMOS process. The Foresight 4 device has demonstrated both the smart pixel principle and sparse data readout. A primary design goal of the Hughes Aircraft Company project was to realize the smallest pixel cell consistent with SSC requirements, whereas the complementary goal at LBL was to demonstrate circuit design concepts needed for radiation hardness and autonomous behavior, without the constraint (just at this stage, not for future designs) of smallest possible area. The experience gained with these two approaches will permit a more rapid convergence to the final SSC design.

Both designs show low noise, and reliable measurements of the LBL pixel cell design show the noise to be only 50 electrons rms. The intended operating threshold of the comparator is 1000 electrons, referred to input, providing a good margin. A present problem, however, is the existence of unexpectedly large variations in transistor conduction characteristics, which lead to large differences in comparator threshold among various pixel cells, much greater than 50 electrons rms. The new pixel cell block allows design changes that can alleviate this, and the elimination of this problem will be a major goal of the work in the coming year. The radiation hard process of choice may be superior in this regard due to better dimensional and process control standards.

An improved version of Foresight 4, Foresight 5, is now available for testing at Hughes. After initial electrical tests at Hughes, the Foresight 5 device will be extensively tested on the bench at UC Berkeley Space Sciences Laboratory.

Completion of tests on the bench will lead to beam tests using the pixel telescope made by UCB/SSL and employed successfully at FNAL in December 1991.

In addition to the charge sensitive amplifier, signal shaping element, and comparator, the pixel cell also must contain a one-shot with a period of about eight microseconds. The one-shot serves as a temporary memory of the recent hit, so that interrogation by the periphery during valid data readout can produce correlated x–y information. The one-shot must stay on for a period corresponding to the time needed to readout a complicated event with many tracks in one array. This maximum readout time is not known with any certainty at present.

As noted above, the pixel cell will collect the electron current, providing a significantly faster charge collection time than for holes. Nevertheless, the combined effects of charge collection time, charge sharing, and finite circuit bandwidth, and carrier mobility degradation in both readout IC and detector due to radiation damage will introduce time-walk as a significant characteristic of circuit response. The present LBL pixel cell design (2 μm feature size) displays about 19 nsec time-walk for 2-8 fC input, and approximately 38 nsec for 1-8 fC. Future designs using smaller design rules are expected to be faster, but the likely existence of time-walk has been recognized in the conception of overall architecture, so that adverse effects on efficiency are brought to a negligible level.

The new pixel cell concept contains no explicit memory of analog information. This choice reduces the pixel cell area considerably. Instead, charge information is obtained by measuring time-over-threshold widths of the hit signals that the pixels transmit to the periphery. Eliminating analog storage within the pixel cell also minimizes interactions between the pixel cell and the periphery. Needless to say, the pixel cell signal shaping element and comparator design must be optimized to provide a useful representation of the input charge. As noted above, the LBL pixel cell amplifier design has a CR filter with 100 nsec time constant for low-frequency roll-off, a good match for the time-over-threshold scheme. The width of a typical comparator output pulse would be about 100 nsec. Linearity of the charge-to-width relationship is not essential, and the required charge resolution is quite modest, about 5 bits. A nonlinear ADC is appropriate to obtain the dynamic range.

The charge information obtained by time-over-threshold not only permits interpolation for improved spatial resolution, it also allows systematic correction of time-walk to reduce time resolution to a single beam crossing. This architectural feature is especially important, and the evaluation of this feature is a major goal of this year's work.

An obvious area-saving alternative, of implementing comparators only at the

end of each row and column, has also been considered. This approach leads inescapably to an increase of noise at the comparator input by $\sqrt{N}$ where N is at least 64, giving predicted noise levels of 400 electrons for the current design. Further emphasis on pixel cell noise reduction in the design may make this approach feasible. Complications in resolving ambiguities during readout would require special attention. This alternative is a conceivable avenue to obtain a further reduction in pixel cell size.

F. Array Architecture

The question of the optimal organization of pixel arrays for the SSC has led to the examination of several different schemes [37–41]. A rather detailed design has been made of one basic concept developed at Hughes Aircraft Company from specifications developed by the Pixel Development Collaboration[42]. This design includes all features of the smart pixel concept such as time-stamping, sparse data readout, ghost elimination, and neighbor logic. Charge information is obtained by analog storage within the pixel cell. Event recording is done in peripheral pattern registers managed by a central controller. Trigger level 1 valid data is found by event time comparison in a CAM. Concerns about the performance of this architecture have arisen as a consequence of increasing trigger 1 latency (up to 4 μsec), increasing luminosity aspirations(up to $10^{34}\text{cm}^{-2}\text{sec}^{-1}$) combined with smaller operating radius (6 cm), and time-walk effects that may spread the hits from a single event over several beam crossings.

However, it now seems that a new candidate architecture has been defined that alleviates these concerns to a great extent, and which also offers considerable simplification. This new concept no longer involves a centrally managed activity for recording of primary hits. It is data-driven, based on independent action of the rows and columns. This decentralization has the very beneficial effect of reducing circuit activity by a large factor, on the order of 250. The architecture is schematically indicated in Fig. 86.

The overall scheme follows a "minimum activity" strategy to reduce power dissipation and noise, and provides a fast response to level 1 valid data. It also appears to be economical in area requirements for the peripheral circuitry. Effects that corrupt data at the part per thousand level have been regarded as acceptable. Emphasis has been placed on maintaining hit detection efficiency at the highest practical level.

In essence, this concept is based on "smart" pixels that transmit hit information along shared row and column lines to temporary memory on the edge of the array. This peripheral circuitry stores uncorrelated x–y information during trigger level 1 latency. The sensing of valid data for trigger level 1 causes sequential readout of

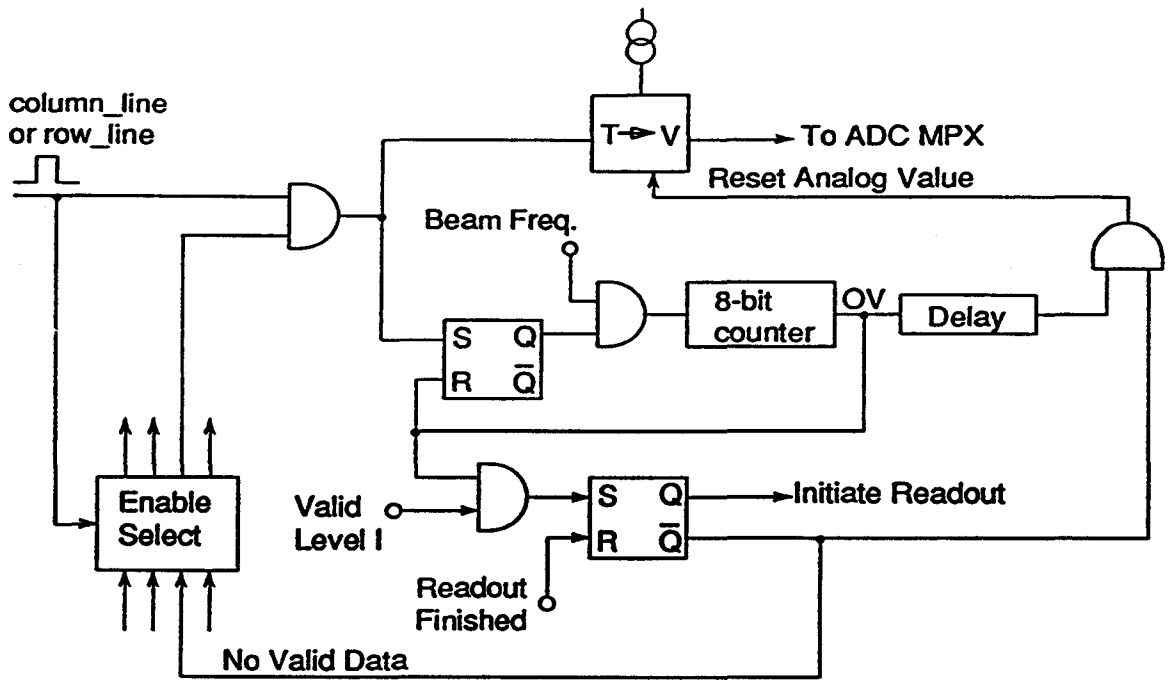

Fig. 86. The pixel array architecture illustrating digital delay, trigger level 1, and charge measurement using time-over- threshold.

valid data only, interrogating pixels to remove ambiguities. This sparse data scan results in a data stream comparable to a strip system. In addition to correlated x–y data, charge information is also obtained to permit high accuracy interpolation and diagnostic evaluation.

The pixel charge information is obtained by measurement of time-over-threshold of the row_line and column_line signals, generated by the pixel cell comparators. As noted above, this measurement is done not within pixels, but rather at the array periphery. The width of the signal could be stored by a simple time-to-voltage circuit (constant current gated onto a capacitor while row_line (column_line) signals are present), or possibly by a direct TDC with a nonlinear conversion characteristic. If a valid data condition occurs, the voltage is digitized by a flash ADC during the row and column interrogation process. The ADC precision needed is rather low, about 5 bits, as modest charge resolution saturates the possible spatial resolution improvement.

A limitation of this approach to charge measurement is that charge information may be partially corrupted in the highest energy QCD jets, because columns and/or rows will sometimes be hit by more than one track. This effect, however, should be insignificant for top quark decays or for other massive particle decays.

The row_line and (column_line) rates are both $\simeq$22 kHz, a rather comfortable activity level. If the array had not been electrically subdivided in four parts, the column_line rate would be 88 kHz, increasing the disparity between row and column activity. Charge sharing will increase the row rates more than the column rates. Pileup is small, $\simeq$0.2%, and affects mainly charge information. The row_line (column_line) signals are transmitted as currents rather than voltage transitions to avoid parasitic coupling effects. This also allows the sensing of overlap between more than one hit pixel, so that although charge information may become garbled, the efficiency is minimally affected.

In addition to the gated capacitor to convert signal width to voltage, the row_line (column_line) peripheral circuitry also has a flip-flop to receive the "hit" signals from struck pixels. Once set, the hit flip-flop enables a digital delay for a later coincidence test with the level I trigger signal. The delay is an eight-bit counter at the beam crossing frequency. Exactly 256 beam crossings later (four microseconds), the counter will overflow, producing a signal corresponding to the earlier event. The overflow signal will reset the first flip-flop, stopping the counter. If the overflow signal is also in coincidence with a valid trigger level 1 signal, then a second valid data flip-flop will be set, indicating the existence of valid data in a specific row (column). The width of the level 1 trigger valid data pulse can be tailored to match current operating performance characteristics, *i.e.*, if greater time-walk occurs after considerable radiation damage, a larger width can be utilized to maintain efficiency. A digital delay, rather than analog, was chosen because of the delay uniformity and stability requirements.

The setting of the valid data flip-flop initiates readout by a priority scan to find the first row with valid data. An interrogate signal causes all struck pixels in that row to respond along the column direction. A coincidence at the column periphery of the pixel response with the valid data flip-flop indicates unambiguous valid data. A priority scan along the columns finds the first correlated x–y coordinate, *i.e.*, the row-column address pair, which is then transmitted off-chip. The process is repeated for the next valid data column along that row, if any. If none, then the next row with valid data is scanned, and so on, till all the valid data information in the array is transmitted. It is worth noting that the valid data readout process occurs without interrupting the natural recording activity of the rows and columns, maintaining array efficiency near 100%. Although quite rarely, it can occur that an array will be involved in a second valid trigger level 1 occurrence during readout of the first. Partitioning of the two valid data sets would require the valid data flipflop to be twinned, with sequential enable after the first valid data flag is set.

Because more than one row_line (column_line) signal can occur while the digital delay is enabled, the basic peripheral circuitry must be repeated with sequential

addressing to permit full efficiency. The depth required depends on the anticipated rates, which of course are determined by the maximum expected luminosity. For the standard SSC Luminosity of 10^{33} $cm^{-2}sec^{-1}$, the probability to obtain more than three hits on a column_line during the four microsecond latency, divided by the probability to obtain one, two, or three hits, (hence a measure of inefficiency) is much smaller than 10^{-3}.

This low probability means that a pixel detector with a depth of three can operate at luminosities substantially higher than the standard 10^{33} with efficiencies still near 100%. Of course, one can choose the depth greater than three, permitting luminosities perhaps higher than 5×10^{33}. In any event, there is no "brick wall" lurking in this architecture near the standard luminosity. At the standard luminosity, only about 44 pixels in an array will be "on" at any given moment, corresponding to an occupancy of $\sim 3 \times 10^{-3}$. With the time resolution constraint added in, the occupancy is much smaller than 1×10^{-5}.

In principle, a fully efficient digital delay can also be realized with a shift register, but this would require far too much power and area to implement on each column and row. Also in principle, the digital delay could be equipped with a programmable reset value, to permit arbitrary delay intervals. While possible, this may not be worth the effort due to the area requirement for an additional buss; the value of delay could be easily chosen at the design stage.

In summary, this architecture promises seamless registration of hits, graceful behavior with increasing radiation damage and/or luminosity, good charge information without on-pixel analog memory, good time resolution with time-walk correction, and fully independent read-write for maximum efficiency. This architecture appears to be applicable to the strip readout as well, offering charge information at a very modest cost.

G. Mechanical Systems

A number of mechanical issues have been addressed during FY1991. One important result is the demonstration of a back-thinned readout. Back-thinning of the VLSI readout array to a thickness of 50 μm after bonding to the diode detectors has been demonstrated by Hughes Aircraft Co. A different thinning approach using a waffle grid etch has been pursued with success at LBL.

A concept based on gas-cooled silicon-carbide foam (3% density) was developed by Hughes for mechanical systems. The analysis showed that the effects of thermal gradients and of pressure deflections due to gas flow were very small. This attractive concept appears viable for both pixel detector and silicon tracker. The major advantage of the gas-cooled foam structures is simplicity, in comparison with liquid butane wicks. The foam concept can serve as a backup should insurmountable

difficulties arise, *e.g.*, with butane safety issues.

The primary effort in mechanical engineering during the last year has been to complete a conceptual design of a pixel subassembly. Several guidelines were established to ensure that a minimum of R&D effort would be required to develop a support structure for the pixel arrays. These included the use of the same materials that are being developed for the remainder of the silicon tracker. The structure has been designed using composite material for structural stiffness and minimum radiation length. Evaporative cooling by butane is considered the baseline method for temperature and dimensional control. A laboratory has been established to develop assembly techniques that will allow a cost-effective pixel subassembly to be produced.

An L-shaped carrier has been designed to support a tiled array of pixels. The baseline pixel configuration is shown in Fig. 87. The pixels are tiled in z by placing them on the top and bottom of the carrier and in ϕ by overlapping the carriers around a support ring. The pixel/carrier subassembly is shown in Fig. 88. This figure also illustrates the evaporative cooling concept using wicks to pump the butane to the source of heat. An ANSYS code calculation was completed for an 18 cm long carrier with a tiled pixel load on it. A maximum deflection of 54 μm was determined. A heat transfer analysis predicted a maximum electronic temperature of $\leq 0.3°$ C and a detector temperature of $\leq 0.2°$ for a heat input of 0.25 W/cm^2.

An initial layout of the L-shaped carrier joined to a support ring indicates that $\leq 1\%$ dead space may be achieved by butting two mirror carrier/pixel subassemblies end-to-end.

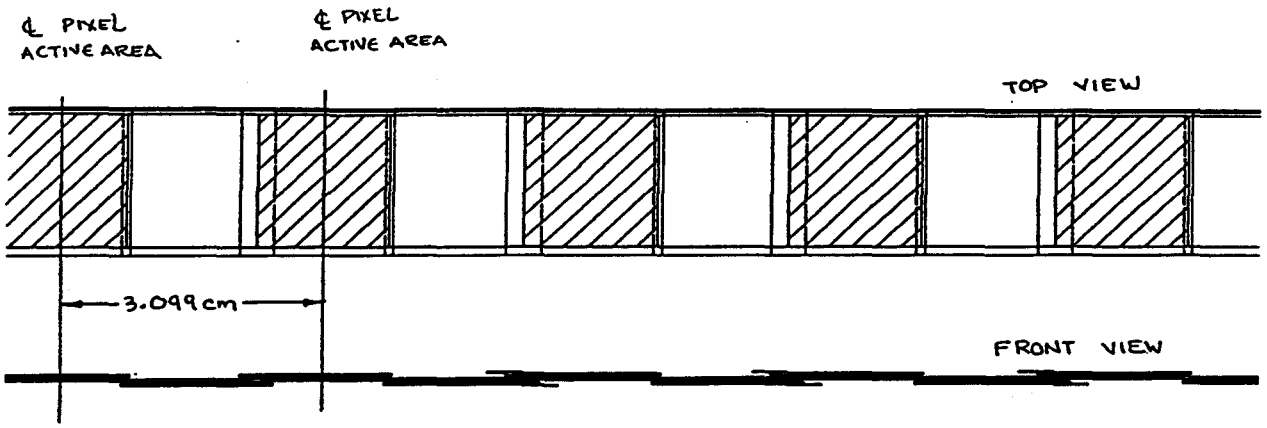

Fig. 87. Baseline pixel array configuration showing the L-shaped carrier.

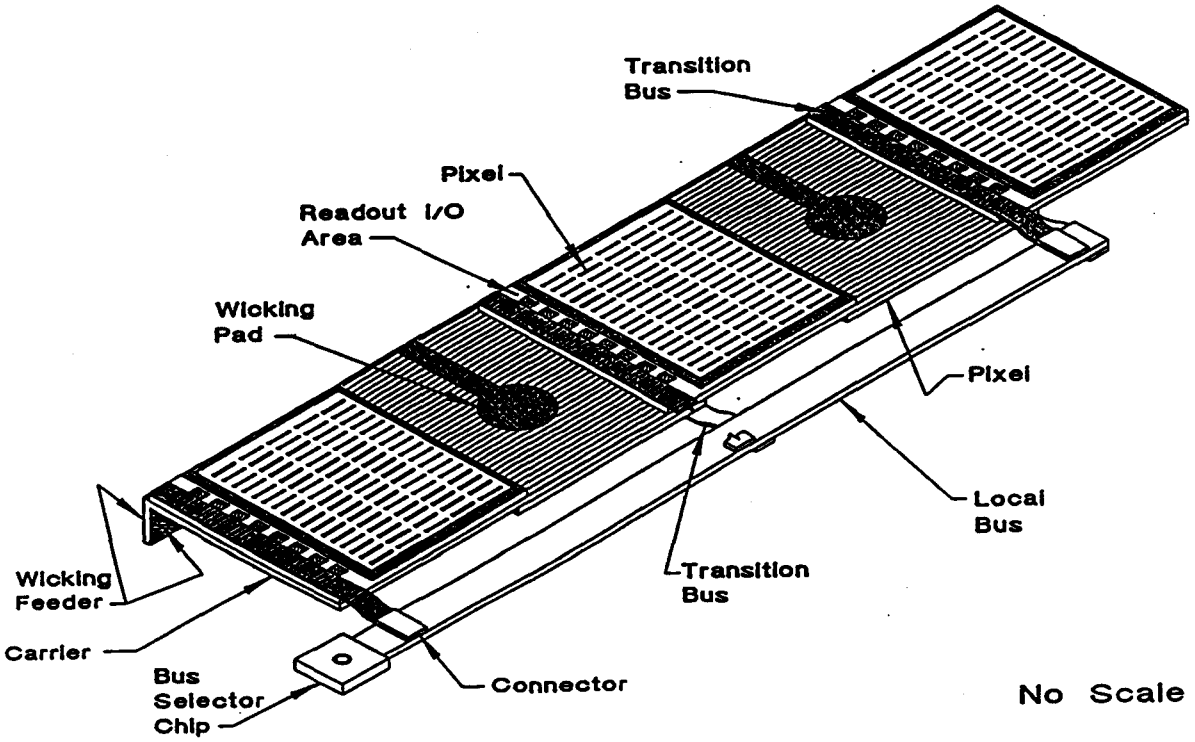

Fig. 88. The pixel/carrier subassembly illustrating the evaporative cooling concept.

IX. Cost Estimate

A. Introduction

In this section we present our calculation of the costs of the detector shown in Fig. 1 at the beginning of this report. Table 30 presents the basic component count for the full array. Listed are the component names, the number required, the cost/item and the total cost. The last column states the type of quote received or how the cost information was obtained. The detector is composed entirely of strip detectors. Costs are in FY92 dollars. The contingency, not shown in the table, is about 27%.

B. ME Structures/Integration/Assembly

Most of the costs associated with this effort were estimated by engineers using their past experience as a guide. Most of the raw material costs were quoted from vendors. The labor, materials, and tasks were broken down into considerable detail. In some cases, catalogue items were used and these costs are known accurately.

C. Detector and Front-end Electronics Module

Table 30 shows the number of components required for these subassemblies. Credible estimates were received for the rad-hard, AC-coupled, double-sided silicon detectors from Hamamatsu. An expected delivery time was also given by Hamamatsu for these detectors.

Quotes were received for both chips making up the front-end readout. These were from Tektronix for the bipolar chip and UTMC for the digital storage chip. The Tektronix quote assumes a very conservative 15% yield in fabrication.

Several discussions were held with vendors on means of assembling the modules. The baseline design calls for wirebonding the readout chips to the detector and the I/O pads to a data/power bus. The cost for wire bonding was determined by taking the quoted speed of an available bonder and reducing the rate by a factor of four. This was to account for setup, adjustment, and breakdown time. The number of bonds was determined and the total time to complete the task was calculated. A machine/operator time cost of $100/hr was estimated by one of the vendors. A quote of $28 per module was received for the beryllium shielding plates. Except for the detector, readouts, metal shield, and need for a cable, the module assembly is still not fully defined. An additional cost of $5/assembly was added to capture other materials or tasks that may be required. This low cost/assembly assumes development of the process to a level that is highly automated. The time for module checkout was an engineering estimate again based upon a developed, automated process.

Table 30. Major Item Costs

VQ = Vendor Quote
EE = Engr. Est.
C = Catalogue

Item	Unit Cost, k	Unit	Number	Total, k	BOE
Barrel Detector	$0.750	each	3600	$2,700	VQ
Frwd Readout	$1.500	each	3112	$4,668	VQ
Barrel Readout	$0.053	each	18000	$954	VQ
Frwd Readout	$0.053	each	32640	$1,730	VQ
Barrel Modules	$0.165	each	1800	$297	VQ/EE
Frwd Modules	$0.266	each	1632	$434	VQ/EE
Optical trans/rec	$0.500	set	1236	$618	C
FEE Design/test Labor	$3,008	effort	1	$3,008	EE
DAT Test Labor	$140	effort	1	$140	EE
Enclosure/supports	$881	each	1	$881	VQ
Space Frame/mounts	$501	each	1	$501	VQ
Ctrl Cooling Ring	$12.50	each	20	$250	VQ
Ctrl Support Rings	$12.50	each	4	$50	VQ
Ctrl Support Cyl.	$122.50	each	2	$245	VQ
Ctrl Ring/shell Mount	$1.04	each	72	$75	EE
Ctrl Coolant Dist.	$2.11	each	20	$42	VQ
Ctrl Align/assy/test	$10.00	each	12	$120	EE
Disk Cooling Ring	$11.30	each	48	$542	VQ
Disk Support Ring	$16.90	each	22	$372	VQ
Disk Array Mount	$3.10	each	78	$242	EE
Disk Coolant Dist.	$4.60	each	26	$120	VQ
Disk Align/assy/test	$8.60	each	26	$224	EE
Power Cable/bus	$5.60	each	68	$381	VQ/EE
Int. Optical System	$9.00	each	30	$270	EE
Heat Rejection System	$516	each	1	$516	VQ/EE
Power Sppls/Cables	$0.90	each	164	$148	EE
Tracker Assy/test	$879	each	1	$879	EE
Trans. Fixtures	$204	lot	1	$204	EE
Slow Controls	$150	lot	1	$150	EE
Mech. Int/exp	$2,254	effort	1	$2,254	EE
In-situ Alignment	$511	system	1	$511	EE
Labor Expenses	$1,550	effort	1	$1,550	EE
1.1 Prog. Man.	$848	each	1	$848	EE
Other	$6,548	misc.	1	$6,548	EE
			TOTAL	**$32,472**	

The cost for cables was an engineering estimate based upon discussions with a consultant. The cost of the raw material was obtained from a vendor and a multiple of 4 times this for cable fabrication was assumed. A cost/area was determined and the total cable area in the tracker was estimated.

D. Tooling

The STS is composed of many thousands of individual silicon wafers that originate from 10 cm diameter, 300 μm thick polished silicon disks. Constructing a precision tracking system from such an immense number of wafers requires significant investment in construction tooling, precision alignment equipment, assembly fixtures and checkout equipment. Precision tooling and operator controlled assembly placement devices are cornerstones to the cost effective construction of the large array of silicon detectors.

A conceptual design of an operator controlled assembly fixture, which aligns and permits simultaneous bonding of the individual detectors onto these structures, has been developed. Alignment fixtures for staging the assembly of the individual silicon subsections must also be designed and constructed, to achieve the stringent placement tolerances of one silicon substructure with respect to another. Sequential construction steps have been considered in developing the construction cost profile. A summary of these individual steps as well as the required tools and fixtures are as follows:

1. Silicon Detector Module	Bonding and alignment fixture. Optical microscopes align to wafer target fiducials.
2. Module Assembly Station	Align and bond individual modules to support structures, to better than 25 μm precision. Semi-automated, highly repetitive assembly station. Used for both central and forward region silicon regions.
3. Optical Alignment Platform	Align and state individual major silicon substructures as the overall detector is assembled. Array of telescopes, auto-collimators and interferometers.
4. In Situ Calibration	Insertable X-ray calibration point source. Optical monitoring of source location to global reference system.

Assembly jigs and special test equipment will also be required for construction

and checkout. Our precision construction tolerances dictate that care must be exercised in the design of these assembly aids. Our design philosophy has been to utilize commercially available tooling to the extent practical, and develop specialized designs for situations demanding extreme precision and or unique assembly operations.

E. Physicists' Contributions

Our cost estimate assumes a significant contribution from the physicists involved in this project, which is not included in the labor costs. In areas such as X-ray calibration, reliability testing of detectors and readouts, and possible repair of these components we have assumed main responsibility to lie with the physicists. For each of such tasks we have assumed the participation of at least one engineer to provide management and accountability and some fraction of a technician to provide technical assistance.

F. Contingency

Contingency estimates were made at as low a WBS level as practical using the guidelines published by the SDC program office. Table 31 lists the results of the analysis. In some cases, contingencies were estimated for a specific task or component, but no costs were assigned. This precluded determining the actual contingency at the next higher level, therefore, it was estimated based upon a perception of how the costs might be distributed.

Table 31. Contingency Table

WBS	Description	Base ($k)	Contingency %	Total ($k)
1.1.1	Main Mechanical Assembly			
1.1.1.1	Enclosure/supports	18	5.0	19
1.1.1.1.1	Outer shell	1,166	20.0	1,399
1.1.1.1.2	End plates	177	20.0	213
1.1.1.1.3	Shell supports	219	22.0	267
1.1.1.1.4	Inner shell	195	17.0	229
1.1.1.1.5	Assy/alignment/test	36	8.0	39
	Total Enclosure/supports	1,811	19.5	2,165
1.1.1.2	Space frame	240	5.0	252
1.1.1.2.1	Tubes	407	31.0	534
1.1.1.2.2	Joints	210	31.0	275
1.1.1.2.3	Frame mounts	175	24.0	217
1.1.1.2.4	Assy/alignment/test	242	8.0	261
	Total Space Frame	1,275	20.8	1,539
1.1.1.3	Central region subassembly			
1.1.1.3.1	Cooling rings	453	36.0	616
1.1.1.3.2	Structural support rings	93	36.0	127
1.1.1.3.3	Shell support cylinder	667	28.0	853
1.1.1.3.4	Ring/shell mounts	231	35.0	311
1.1.1.3.5	Module - central	107	44.0	155
1.1.1.3.6	Coolant distribution	120	44.0	173
1.1.1.3.7	Silicon shell assembly	473	24.0	587
1.1.1.3.8	Assy/alignment/test	289	24.0	358
	Total Central region	2,433	30.7	3,180
1.1.1.4	Forward subassembly	61	5.0	64
1.1.1.4.1	Cooling rings	924	40.0	1,294
1.1.1.4.2	Structural support rings	627	31.0	821
1.1.1.4.3	Modules - forward	154	40.0	216
1.1.1.4.4	Silicon planar array mounts	422	32.0	557
1.1.1.4.5	Coolant distribution	311	44.0	448
1.1.1.4.6	Assy/alignment/test	792	20.0	950
	Total Forward region	3,291	32.2	4,350

Table 31(continued). Contingency Table

WBS	Description	Base ($k)	Contingency %	Total ($k)
1.1.1.5	Power cables - bus			
1.1.1.5.1	Cables	531	22.0	648
1.1.1.5.2	Feedthroughs	179	22.0	219
	Total Power cables	710	22.0	867
1.1.1.6	Coolant piping	51	12.0	57
1.1.1.7	Int. optical system	479	22.0	584
1.1.1.8	Coolant sys. instrumentation	58	12.0	65
1.1.1.9	Transportation fixtures	204	12.0	229
1.1.1.10	Main mechanical integration	2,256	25.0	2,819
	Total Main Mechanical Assembly	12,568	26.2	15,855
1.1.2	Internal electronics			
1.1.2.1	Modules			
1.1.2.1.1	Detector	7,528	24	9,335
1.1.2.1.2	Front-end electronics (FEE)	5,809	44	8,365
1.1.2.1.3	Readout Interface Hybrid (RIH)	52	36	70
1.1.2.1.4	Other module components	167	15	192
1.1.2.1.5	Assembly and test	512	24	635
	Total Modules	14,068	32.2	18,597
1.1.2.2	Data transmission (DAT)			
1.1.2.2.1	Bus selector chip (BSC)	348	12	390
1.1.2.2.2	Data/power cables	46	40	64
1.1.2.2.3	Electro-optic trans/rec (EOTR)	659	13	744
1.1.2.2.4	Fibers	178	5	187
1.1.2.2.5	Feedthroughs	160	32	211
	Total Data transmission	1,390	14.8	1,596
	Total Internal Electronics	15,458	30.6	20,193
1.1.3	External mechanical systems			
1.1.3.1	Heat rejection system	516	19.0	614
1.1.3.2	Gas systems	78	10.0	86
1.1.3.3	Slow control	150	10.0	165
1.1.3.4	Power supplies	139	10.0	153
1.1.3.5	Power cables	46	10.0	50
1.1.3.6	Safety systems	88	10.0	97
	Total External systems	1,017	14.6	1,165

Table 31(continued). Contingency Table

WBS	Description	Base ($k)	Contingency %	Total ($k)
1.1.4	External electronics systems			
1.1.4.1	Data interface			
1.1.4.1.1	Electro-optic trans/rec (EOTR)	500	13	565
1.1.4.1.2	Interface electronics	251	12	281
1.1.4.2	Assembly and test	442	12	495
	Total External electronics	1,192	12.4	1,340
1.1.6	Assembly/test/special			
1.1.6.1	Assembly	879	20.0	1,054
1.1.6.2	In-situ alignment	511	30	665
	Total Assembly/test/special	1,390	23.7	1,719
1.1.7	Project Management	848	10.0	933
	Grand totals	32,473	26.9	41,205

EDIA Percent	16.6

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