SDC-91-00090

**SDC**
SOLENOIDAL DETECTOR NOTES

# SDC GLOBAL LEVEL 1 PROCESSOR: CLOCK & CONTROL

November 8, 1991

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## 1 Introduction

The Global Level 1 Trigger Processor is the device that collects the Level 1 Trigger data from the subsystems, distributes the Level 1 Accept and 16 nsec clock signals to all subsystems, and controls the overall operation of the Level 1 subsystems. This document describes the function of the Global Level 1 Processor, its interface to the Subsystems and its physical layout. This document outlines in specific detail the functions needed for clock and control. It also outlines the design of a module that will simulate the function of the Global Level 1 Processor for use in the development of Subsystem front end electronics.

## 2 Function of the Global Level 1 Processor

### 2.1 Overall Data and Control Flow

The Global Level 1 Processor (GL1P) receives a subset of the data from subsystems participating in the level 1 trigger. The data for each 16 nsec bunch crossing is sent by each subsystem every 16 nsec and arrives at the input of the GL1P before 112 - 162 crossings have elapsed since the event occurred. The GL1P issues a Level 1 Trigger Accept/Reject at its output 132-182 bunch crossings after the event occurred. The timing is discussed in detail in ref [1]. The GL1P not only makes the final level 1 decision, but it also controls the start of any level 1 readout, disables this readout, and distributes scheduling signals for tests and calibrations. Therefore, all subsystems, even those not involved in the level 1 decision, must communicate with the GL1P.

All level 1 trigger and DAQ pipelines in the subsystems and the GL1P must be driven with a common clock synchronized to the SSC crossing frequency. This clock is distributed centrally through the GL1P. This clock is phase locked to the the SSC machine clock and has a 16 nsec cycle. The clock is high for $8 \pm 1$ nsec and low for $8 \pm 1$ nsec. The processing of the GL1P decision is driven by this cycle. For testing purposes, the GL1P operates on its own internal clock which can be varied in frequency from 70 MHz to 1 KHz.

Subsystems ship trigger data to the GL1P every 16 nsec. All of the data relevant to one crossing is shipped in one 16 nsec time period. All subsystems must send their data to the GL1P so that it arrives at the GL1P input within 1.8 - 2.6 $\mu$sec after the crossing occurred at the interaction point. Subsystems should send trigger data as soon as it is available and not delay sending trigger data for the purposes of synchronization. The subsystems must send data continuously even if they are being read out.

The GL1P receives the trigger data and aligns this data in time for all the subsystems since the arrival time for the data of a particular crossing is different among the different subsystems. The particular bunch crossing number of a subsystem's data is indicated by a

local bunch counter, named Bunch Phase. The Bunch Phase is used to check the alignment of the trigger data from each subsystem. The subsystem also counts Level 1 triggers. This number, Level 1 ID, is used to check that the data read out corresponds to the correct Level 1 Accept.

## 2.2 Level 1 Accept/Reject

After the GL1P processing, a decision is made to issue a Level 1 Accept or Reject for each bunch crossing. The GL1P sends the Level 1 Accept/Reject to all subsystems 132 - 182 crossings after the bunch crossing. This signal appears at the output of the GL1P. The Level 1 Accept/Reject arrives at the subsystem after additional delay due to the propagation of the Level 1 Accept/Reject from the GL1P. The Level 1 Trigger Accept is a Level that is 1 for accept and 0 for reject. The Level 1 Trigger Reject is a Level that is 0 for accept and 1 for reject. These are strobed by the clock. A signal called "data valid" also accompanies the Level 1 Accept/Reject. This signal is used by some components to generate a Level 1 Strobe. Data valid is low after a Level 1 Accept for the length of the pipeline propagation time. The Level 1 Accept/Reject signal is also accompanied by additional GL1P data. This data is not necessarily propagated to all components of a subsystem, but is used as a diagnostic by the central processing of a subsystem. The data includes data valid, the Bunch Phase, the Level 1 ID, and several bits of "readout type". The Level 1 ID counts Level 1 Accepts. The bits of "readout type" allow information to be sent to subsystems that may react differently to different trigger types.

## 2.3 Ambiguous and Overlapping Triggers

If a subsystem cannot identify data with a particular crossing, it sends the same data applicable to a number of crossings with each crossing. Since most triggers rely on a coincidence of components, the result will still be to select a single crossing for every L1 Accept. Subsystems determine the number of bunch crossings to store upon each Level 1 Accept. The present design does not allow back-to-back Level 1 Accepts. There is the possibility that we cannot uniquely identify a crossing from the trigger data or that we may have two Level 1 Accepts within the measurement time span of some subsystems. Following Dorenbosch, Botlo, Fry and Milner (SSCL-348), we define the Level 1 Accept as a level that is high for all clock cycles to be measured. The Level 1 ID is incremented on the rising edge of the Level 1 Accept. To attempt to limit overlaps as much as possible, we also follow their rules for minimal spacing for Level 1 Accepts:

- No more than 1 Level 1 Accept per 80 nsec.
- No more than 2 Level 1 Accepts per 260 nsec.
- No more than 3 Level 1 Accepts per 1 $\mu$sec.
- No more than 4 Level 1 Accepts per 4 $\mu$sec.

They determine that the total cost for these rules is less than 1% at a Level 1 rate of 100 KHz and 11.5% at 500 KHz.

## 2.4 Trigger Control

Subsystems send trigger control information to the GL1P. This includes a busy bit to indicate that the subsystem trigger did not process the event, busy bit to indicate that the subsystem DAQ cannot read out the event, a fatal error bit to indicate that the subsystem trigger has had a fatal error and a trigger data error to indicate that the subsystem trigger data may be corrupt. An example of a trigger busy would be a reset process that had not been completed. We must allow for subsystems that cannot complete a Level 1 Reset sequence in a single 16 nsec crossing. The trigger busy bit prevents a Level 1 Accept being issued to a subsystem that must use several crossings for a reset. An example of a fatal error would be a disagreement between the Level 1 trigger number counted by the subsystem and the number sent by the GL1P. An example of a trigger data error would be either a parity check failure or another type of internal data checking failure. The control information also includes the subsystem's crossing number associated with this data. All subsystems active during a run must send this control information to the GL1P, whether or not they send data used in the Level 1 decision.

## 2.5 Tests

The operation and scheduling of tests during a run are controlled by the GL1P. A schedule of all tests to be run is downloaded to the GL1P before the beginning of a run by the Central DAQ Control (CDAQC). The CDAQC also can modify this schedule during a run in response to changing detector status. The GL1P sends to all subsystems a Test Enable signal, with the type of test to be run indicated in the Test Trigger Type bits, a fixed number of crossings before the crossing when the test is to be done. This enables subsystems to prepare for the test. The tests are arranged in such a way as to allow many subsystems to do tests simultaneously. The subsystems set up their tests so that the test data will be contained in the exact crossing indicated by the GL1P Test Enable Signal. The GL1P inhibits normal triggers a fixed time before the test trigger crossing so that there will be no interference. The GL1P then sends out a Level 1 Accept for the appropriate crossing to read in the test data. This Accept is accompanied by a bit in the Readout Type set to indicate that it is a test trigger.

## 2.6 Functional Layout

The functional block diagram of the GL1P as it interacts with a subsystem trigger is shown in Figure 1. The Clock Distribution block generates the 16 nsec clock and associated data such as the Bunch Crossing 0 and Empty Bunch Indicators from SSC accelerator clock information. It then distributes this information to the subsystems and the rest of the GL1P. This block also monitors the relative phase of the accelerator clock and the beam pickup signal, which should remain constant. The Control Interface provides all of the control signals to the subsystems and reads all of the control signals from the subsystems. All data except for the trigger data from a subsystem is brought through the Control Interface. The test scheduling and Level 1 Accept are sent to the subsystem through this block. It also monitors the subsystem deadtime and status. The trigger data from the subsystems is processed in the Trigger Logic block. Here the data from the various regions of each subsystem are collected, counted, and placed in an appropriate format for correlation with other subsystem trigger data. This data is shipped to the Trigger Decision Block, which

contains the final logic to determine the Level 1 Accept. This logic also uses the output from the Control Interface to determine if the detector is able to accept the trigger and, if necessary, to determine the correct crossing to issue the trigger.

# 3 Clock and Control Subsystem Interface

## 3.1 Connections between Clock and Control System and other Subsystems

Each subsystem crate in the detector is linked to the Level 1 Clock and Control system through 3 basic connections as represented by the following 3 logical cable types: the Clock, Control, and Status cables. The Clock cable distributes the 16ns crossing clock to the subsystem crate, the Control cable distributes Level 1 trigger information, and the Status cable returns Level 1 status information from the subsystem crate to the Clock and Control system. The Control and Status cables are required to carry a 16-bit Control or Status word for each 16ns crossing, thus having a data rate of 1 Gb/s.

The actual physical implementation of these cable links may take a number of forms. For example, for long distance runs, between front end subsystem crates on the detector and off-detector Clock and Control distribution crates, each of these cables could be an optical fiber, with the Clock cable transmitting a pure 16ns clock, and the Control and Status cables running at a serial rate of 1 Gb/s. Alternately, the clock could be embedded into the Control cable optical fiber, with a result of one less physical cable connection in the link. For shorter runs between distribution and subsystem crates that are physically close together, conventional twisted-pair electrical cables could be used, with the Control and Status cables requiring each 16 pairs, and the Clock becoming possibly the 17th pair on the Control cable.

Tables 1 and 2 show the frame definitions for the 16-bit Control and Status cables. These definitions are described in the subsections below.

## 3.2 Control Cable

The Control cable carries the Level 1 trigger information from the Global Clock and Control system to the individual subsystem crates. This information is delivered as a 16-bit control word for each 16ns crossing clock, in a continuous pipeline fashion. The control word is organized into 3 different frame types, as shown in Table 1. The use of these frame types makes possible the consolidation of many different signals into a 16-bit format, thus minimizing the physical cabling requirements.

On each crossing clock, the Global Level 1 Trigger system issues the control frame type appropriate for the action to be taken for that crossing. The Idle frame type is the default, and is generally used when no Level 1 trigger or test strobe is to be transmitted. This includes the period of time during a Level 1 reset sequence. The Trigger frame is used when a Level 1 Accept or Test Enable signal is to be sent to the subsystems. Finally, the Utility frame may be sent in place of an idle frame to transmit numeric data such as a Level 1 Accept or Test Sequence number to the subsystem for periodic integrity checks of the detector alignment.

Individual subsystems may be designed to decode only those signals from the above frame types which are necessary for their operation.

Table 1: LEVEL 1 TRIGGER CONTROL CABLE:

| **Frame 0. Idle Frame** | |
|---|---|
| Bits | Data |
| 0–1 | Frame Type ID = 0 |
| 2 | Sync Pulse |
| 3 | Bunch Crossing 0 Indicator |
| 4 | Empty Bunch Indicator |
| 5 | Level 1 Reset |
| 6–7 | Spare |
| 8–15 | Level 1 Bunch Phase |
| **Frame 1. Trigger Frame** | |
| Bits | Data |
| 0–1 | Frame Type ID = 1 |
| 2 | Sync Pulse |
| 3 | Bunch 0 Indicator |
| 4 | Level 1 Accept |
| 5–7 | Level 1 Trigger Type |
| 8–10 | Level 1 Readout Type |
| 11–13 | Ambiguous Crossing Count |
| 14 | Test Enable |
| 15 | Spare |
| **Frame 2. Utility Frame** | |
| Bits | Data |
| 0–1 | Frame Type ID = 2 |
| 2 | Sync Pulse |
| 3–4 | Utility Command |
| 5–6 | Numeric Field ID |
| 7 | Spare |
| 8–15 | Numeric Field |

Table 2: LEVEL 1 TRIGGER STATUS CABLE:

| **Frame 0. Status Frame** | |
|---|---|
| Bits | Data |
| 0–1 | Frame Type ID = 0 |
| 2 | Trigger Busy |
| 3 | Data Busy |
| 4 | Trigger Error |
| 5 | Bunch Phase Field Valid |
| 6–7 | Spare |
| 8–15 | Subsystem Bunch Phase |
| **Frame 1. Test Data Frame** | |
| Bits | Data |
| 0–1 | Frame Type ID = 1 |
| 2–15 | Test Data |

### 3.2.1 Idle Frame Bit Definitions

This section describes the bit definitions for the Idle frame. Some of these bit definitions are shared common with other frames, others are unique to this frame type. As stated previously, the Idle frame is the default frame type, and is used transmitted on each crossing clock to the subsystem crates during a Level 1 reset and other times at which neither a Level 1 accept or Test Enable is to be generated.

**Bits 0–1: Frame Type ID.** These two bits indicate the frame type. An Idle frame is type 0.

**Bit 2: Sync Pulse.** This bit definition is common to all 3 frame types. The Level 1 Trigger System will assert the Sync Pulse signal once every 256 crossing clock cycles, beginning at bunch crossing 0 after a Level 1 reset. This signal may be used by subsystems for timing synchronization checking.

**Bit 3: Bunch Crossing 0 Indicator.** The Bunch Crossing 0 Indicator is set when the clock period corresponding to Bunch Crossing 0 is reached. The Bunch Crossing 0 is defined in the time coordinates of the Level 1 Accept. This means that if the Level 1 Accept is issued by the Gl1P approximately 132–182 crossings after the crossing where the triggering crossing occurred, Bunch Crossing 0 is issued by the GL1P approximately 132–182 crossings after Crossing 0 occurs at the interaction point. This signal is issued by the GL1P every 17,300 crossings, which is the approximate number of crossings the SSC beam takes to make one revolution. The phase of this signal is set up during the GL1P initialization. The Bunch Crossing 0 signal is used by the subsystem in combination with the Level 1 Reset. Upon receipt of the Level 1 Reset, the subsystem waits until it receives the Bunch Crossing 0 signal to release its counters and begin propagating data through its pipelines. This assures alignment after a Level 1 Reset. During the interval between Reset and Bunch Crossing 0 the Subsystem Trigger Busy bit is left on. The GL1P sends the reset a sufficient number of crossings before the Bunch Crossing 0 to assure all Subsystems are able to become

active (if functioning properly) upon receipt of Bunch Crossing 0. This number of crossing represents the time required for the Subsystem to execute the reset.

**Bit 4: Empty Bunch Indicator.** The Empty Bunch Indicator bit is set when the crossing corresponds to an empty bunch. The Empty Bunch Indicator is also defined in the time coordinates of the Level 1 Accept. As is the case for the Level 1 Accept and Bunch Crossing 0, the Empty Bunch Indicator arrives at the end of the Subsystem Level 1 pipeline just as the crossing with the empty bunch reaches it. This is because the GL1P issues the Empty Bunch Indicator again approximately 132–182 crossings after the empty bunch passed through the interaction point. The GL1P may use the empty bunches for scheduling a test event sequence, but will do this scheduling without the Subsystem having to check the Empty Bunch Indicator.

**Bit 5: Level 1 Reset.** The Level 1 Reset signal is set to initiate a Level 1 reset sequence. Upon receipt of this signal, each subsystem crate will assert its Trigger Busy signal, and leave it active until receipt of a Bunch Crossing 0 signal from the GLIP, at which point the reset is complete.

**Bits 6–7: Spare.** These bits are currently reserved for future use.

**Bits 8–15: Level 1 Bunch Phase.** These bits contain the lowest order 8 bits of the crossing number. These bits may be used by the subsystem for system alignment checking. If the subsystem detects an invalid crossing number, it responds by setting the Trigger Error bit in its status.

### 3.2.2 Trigger Frame Bit Definitions

This section describes the bit definitions for the Trigger frame. The Trigger frame type is used when a Level 1 Accept or Test Enable signal is to be issued. The Sync Pulse and Bunch Crossing 0 signal definitions are common to the Idle frame, to permit transmission of these signals regardless of frame type.

**Bits 0–1: Frame Type ID.** These two bits indicate the frame type. A Trigger frame is type 1.

**Bit 2: Sync Pulse.** Same definition as in Idle frame.

**Bit 3: Bunch 0 Indicator.** Same definition as in Idle frame.

**Bit 4: Level 1 Accept.** The Level 1 Accept is sent exactly at a predetermined number of clocks after the event occurs at the interaction point. The Level 1 Accept is a level that is high for all clock cycles to be measured. At present, it is not planned to allow back-to-back Level 1 Accepts.

**Bits 5–7: Level 1 Trigger Type.** These bits indicate the type of normal or test trigger that is being issued with the Level 1 Accept. The assignment of values for this field has not yet been made, but will include trigger types such as a scheduled test event, events associated with a beam crossing, and events not associated with a beam crossing. This latter group includes events such as cosmic ray triggers and other non-beam associated triggers.

**Bits 8–10: Level 1 Readout Type.** These bits indicate a particular readout type to be associated with the Level 1 Accept. Different subsystems may need different readout responses for different triggers. This could mean different numbers of switched capacitors being read out, or taking earlier or later samples, or changing the way the data is processed. Different subsystems will likely respond differently to individual readout type values.

**Bits 11–13: Ambiguous Crossing Count.** This 3-bit value indicates the nummber of subsequent crossings to which the Level 1 Accept refers. The GL1P will attempt to correlate the various subsystems to resolve triggers to a single crossing. However, to provide the possibility that the crossing may not be resolved for a small number of triggers, the Ambiguous Crossing Count provides the possibility of linking up to 8 crossings in an event from one Level 1 Accept. A non–ambiguous trigger has a value of zero for the crossing count.

**Bit 14: Test Enable.** The Test Enable signals to the subsystems the start of a test a predetermined number of crossings after recept of this signal. This permits subsystems to prepare for the test. When the correct number of cycles has elapsed after the Test Enable pulse is transmitted, a Level 1 Accept for the proper trigger type is generated.

**Bit 15: Spare.** This bit is currently reserved for future use.

### 3.2.3 Utility Frame Bit Definitions.

This section describes the bit definitions for the Utility frame. The Utility frame type is used in place of an Idle frame type to transmit miscellaneous utility commands, along with an 8-bit numeric field which can be used by the subsystem to verify system integrity. This frame type provides a general-purpose capability to distribute information to the subsystems at detector clock rates.

**Bits 0–1: Frame Type ID.** These two bits indicate the frame type. An Utility frame is type 2.

**Bit 2: Sync Pulse.** Same definition as in Idle frame.

**Bits 3–4: Utility Command.** These two bits allow for up to four different utility commands to be transmitted to the subsystem crates. An example of a utility command might be to have the subsystem crates verify the contents of the Numeric Field against their own expected internal values, and return a Trigger Error if an unexpected value is detected.

**Bits 5–6: Numeric Field ID.** These two bits identify the contents of the Numeric Field. The Numeric Field may contain a Level 1 Accept number, or a test trigger sequence number. In conjunction with the Utility Command, this field informs the subsystem as to what action should be taken with the contents of the Numeric Field.

**Bit 7: Spare.** This bit is currently reserved for future use.

**Bits 8–15: Numeric Field.** This field contains an 8-bit numeric value to be transmitted to the subsystem crates. The subsystem crates will use this value as determined by the Utility Command and Numeric Field ID fields.

## 3.3 Status Cable

The Status cable carries the status for each subsystem crate back to the Global Clock and Control system. This information is delivered as a 16-bit status word for each 16ns crossing clock, in a continuous pipeline fasion. The Status word is orgainized at present into 2 different frame types, as show in Table 2.

The two frame types are called the Status and Test Data frames. During normal system operation, each subsystem crate will transmit a Status frame on each crossing clock back to the Global Level 1 Trigger system. This frame contains the required status signals which are monitored by the Level 1 Trigger. For standalone and testing procedures, however, a Test Data frame may be transmitted in place of a Status frame on some clock cycles. Both of these frame types are described below.

A *null* frame is a frame in which none of the 16 data bits are set. This type of frame will be interpreted by the Clock and Control system as a Status frame in which none of the bits are set. Subsystems may transmit null frames if they have no status or crossing information to report.

### 3.3.1 Status Frame Bit Definitions

This section describes the bit definitions for the Status frame. This frame contains all of the signals necessary to return the subsystem status to the Level 1 Trigger system. This will be the frame type used during operation of the fully-configured detector, for both normal and test operation.

**Bits 0–1: Frame Type ID.** These two bits indicate the frame type. An Status frame is type 0.

**Bit 2: Trigger Busy.** The Trigger Busy bit is set by the subsystem if its trigger system was not active (able to process the data) during the crossing. This could be due to a reset or more detailed initialization procedures not being complete. If this bit is set, the GL1P will not use the subsystem trigger data in making the trigger decision. The GL1P will not take undertake any action on the subsystem, such as a reset, in response to the Subsystem Trigger Busy bit being set.

**Bit 3: Data Busy.** The Data Busy bit is set by the subsystem to request that the GL1P to halt triggers. The GL1P inhibits further Level 1 Accepts until a crossing occurs where the Data Busy bit is off. This may be due to buffers becoming full. The GL1P records the number of times the Subsystem Trigger Busy and Data Busy bits are set, and the number of inhibited Level 1 Accepts.

**Bit 4: Trigger Error.** The Trigger Error bit is set by the subsystem if its trigger or DAQ system has an error which is not recoverable except (possibly) by a reset from the GL1P. This error could occur if an internal parity check on the subsystem data fails, or if there is an internal subsystem trigger L1ID or Bunch Phase counter disagreement. In response to this bit being set, the GL1P will issue a Level 1 Reset. In addition, the GL1P will inhibit further Level 1 Accepts until it observes the setting and release of the Subsystem Trigger Busy bit. This is because the subsystem data will no longer be valid until the reset action is completed and the data from the crossing after the reset has propagated through the Level 1 pipeline. The GL1P records the number

of times the Subsystem Trigger Error bit is set and the number of inhibited Level 1 Accepts. The GL1P also informs the central data acquisition each time a Level 1 Reset is issued so that if the rate of Level 1 Resets becomes unacceptable, the run will be paused or stopped.

**Bit 5: Bunch Phase Field Valid.** This bit is set if the value returned in Subsystem Bunch Phase field is valid. Otherwise, the GLIP should ignore the bunch phase value in this frame for purposes of system alignment checking.

**Bits 6–7: Spare.** This bit is currently reserved for future use.

**Bits 8–15: Subsystem Bunch Phase.** The Subsystem Bunch Phase is the lowest 8 bits of a counter that counts the number of crossings since the last receipt of the Bunch Crossing 0 from the GL1P. The GL1P checks this counter for sequential incrementing, except during a Level 1 Reset sequence, when it is reset to a downloaded offset. The Subsystem Bunch Phase is also used to align the various subsystems with the GL1P and other Subsystems. This field contains valid data if the Bunch Phase Field Valid bit above is active.

### 3.3.2 Test Data Frame Bit Definitions

This section describes the bit definitions for the Test Data frame. This frame is primarily intended for use within subsystem crates performing testing in a standalone mode. The 14-bit test data field can be used by the local Clock and Control interface card to emulate the decision logic for issuing a Level 1 Accept in response to subsystem data. Though intended primarily for use with the early Level 1 Simulation Module (L1SM) to facilitate subsystem development, it is planned to be supported in the final installed system.

**Bits 0–1: Frame Type ID.** These two bits indicate the frame type. A Test Data frame is type 1.

**Bits 2–15: Test Data.** This 14-bit field can be used by the subsystem to provide a subset of its trigger data normally transmitted to the Level 1 Decision logic. This data will be used by memory lookup circuitry in the Level 1 Trigger simulation and test system to produce an emulated Level 1 Accept.

# 4 Global Level 1 Processor Clock and Control System Layout

Figure 2 shows the layout of the Level 1 Trigger and Subsystem Trigger logic. This figure shows the flow of Level 1 Trigger data from the front end subsystem crates through the Level 1 Decision Logic crates, ending at the Level 1 Final Decision crate. This crate delivers a Level 1 Accept/Reject and crossing ambiguity value to the Global Clock and Control crate, where this and other information is distributed to the detector subsystems. A further discussion of the Level 1 Decision logic can be found in [2].

Figure 3 shows the Level 1 Clock and Control distribution system. This system consists of two basic crate types, the Global Clock and Control, and the Level 1 Distribution crates,

which together distribute the crossing clock and control information to and receive status from all trigger and DAQ subsystem crates in the detector.

The Global Clock and Control crate uses the output from the Final Decision crate, along with machine clock and beam pickup information, plus operator control through the DAQ processor system to generate the root Clock and Control cable output. These signals are sent to up to 16 nearby Level 1 Distribution crates, which in turn can rebroadcast the Clock and Control cable signals to up to 64 subsystem crates each.

The Status cables from the subsystem crates to the Global Clock and Control crate follow the same path, in the reverse direction. Each Level 1 Distribution crate consolidates the status of up to 64 subsystem crates, and transmits that on a Status cable to the Global Clock and Control crate.

The Global Clock and Control and Level 1 Distribution crates reside off the detector in the counting house. They are located physically near each other, and are connected via Clock, Control and Status cables driven electrically. The subsystem crates reside both on and off the detector. Those on the detector, such as front end DAQ subsystem crates, are connected to the Level 1 Distribution crates using fiber optic Clock, Control and Status cables. Those off the detector, such as Level 1 Decision crates, are driven using electrical cables.

## 4.1 Global Clock and Control Crate

Figure 4 shows the Global Clock and Control crate. There is one Global Clock/Control Crate in the detector. It contains a Machine Clock Interface Board to communicate with the interface to the accelerator RF clock. It has a Beam Pickup Interface to communicate with the beam pickup electronics. It contains a Deadtime Monitor Board that tracks the disposition of each crossing, i.e. whether accepted, rejected, or lost due to downtime of trigger and/or DAQ. There is a Level 1 Control Generator card that connects to the Final Decision Logic (FDL) card in the Final Decision Crate as well as the cards described above to generate the contents of the Control cable. This card also reconciles the returned subsystem status such that it will only transmit a Level 1 Accept if the DAQ is able to read out the event and there are no outstanding error conditions that prevent accepting the event (i.e. clock phase confusion, etc.) Finally, this crate contains one Level 1 Clock Control Board (L1CCB) and up to 4 Level 1 Clock Control Fanouts (L1CCF). The L1CCB is the basic interface card for all subsystem crates to the Level 1 Trigger. The L1CCF is used in conjunction with the L1CCB through a backplane interface to provide a fanout rebroadcast of the Clock and Control cables to crates throughout the detector, and to consolidate returned Status cable data from these same crates. Together, the L1CCB and L1CCF cards reside in the Global Clock and Control for the purpose of distributing the Clock and Control to the layer of up to 16 Level 1 Distribution crates. There is a Global Clock Master that provides the phase lock of the 16 nsec clock and distributes the clock to Clock/Control Interface modules. There is a Global Control Master that distributes the Control signals to the Clock/Control Interface Modules. Finally, there are 2 Clock/Control Interface Modules that each communicate with 2 Local Clock/Control Crates. This crate also contains a DAQ Interface/Processor card.

The Global Clock and Control crate distributes Clock and Control information and receives Status information from up to 16 Level 1 Distribution crates through electrical cable interconnections on the L1CCF cards in that crate. Each L1CCF card can drive Clock and Control information to and receive Status from up to 4 Level 1 Distributio

crates through the frontpanel.

## 4.2 Level 1 Distribution Crate

Figure 5 shows a Level 1 Distribution crate. There may be up to 16 of these crates, with the exact number depending on the partitioning of the distribution system. Each crate contains one L1CCB and up to 16 L1CCF cards. Each Level 1 Distribution crate is connected to the Global Clock and Control crate by an electrical Clock, Control and Status cables through the L1CCB frontpanel. Each L1CCF card can drive up to 4 subsystem crates through electrical or fiber optic Clock, Control and Status cables connected on the frontpanel. The L1CCB communicates to the L1CCF cards through 4 identical fanout busses on the crate backplane. Each bus drives up to 4 L1CCF cards.

The crate also contains a DAQ Interface/Processor card. This processor is used to control and monitor the L1CCB and L1CCF cards in both normal and standalone operation.

## 4.3 Level 1 Clock and Control Board

Every front end electronics crate, as well as every trigger system crate has a Level 1 Clock and Control Board (L1CCB). A diagram of the L1CCB is shown in Figure 6.

The purpose of the L1CCB is to receive the machine clock and Level 1 trigger informations on Clock and Control cables via the frontpanel and rebroadcast this information to L1CCF or subsystem electronics cards across four identical backplane busses. Simultaneously, it is receiving and consolidating subsystem status information from these cards and transmitting it upwards on the Status cable connection on the frontpanel.

For test and development purposes, the L1CCB also has the capability to operate in a standalone mode in which it emulates the machine clock and Control cable flow from an on-board oscillator and pattern memory.

The L1CCB performs all of its functions under direct control of the DAQ Processor residing in the same crate. The L1CCB must be configured for any form of operation through the DAQ processor. During normal operation, the DAQ Processor monitors the card status of the L1CCB, and provides a path for reporting error and logging information taken by the L1CCB. In standalone operation, the DAQ takes on a more active role in controlling the L1CCB, serving as the programming source for the emulation programs downloaded into the card. The card is divided in to five subsections, each of which handles one general aspect of the cards functionality. They are described below.

### 4.3.1 DAQ Processor Interface Section

This section provides the interface between the DAQ Processor backplane bus and the on-board address and data busses. It provides the means by which the DAQ processor may access and control the L1CCB. Included in this section is the bus handshaking logic, coarse address decoding logic, and the general control and status registers not associated entirely with any other single section. It distributes the necessary read and write control strobes to the other sections of the L1CCB.

### 4.3.2 Clock and Control I/O Section

This section receives the information on the Clock and Control cables, and distributes it to the four backplane bus fanouts. This section also includes the necessary on-board distribution logic for the 16ns clock, as well as the Level 1 Control signals which are decoded from the Control cable frames.

A source selector sits between the receiver circuitry and fanout logic. Under DAQ Processor control, it selects either the incoming cables or the on-board emulation logic as the clock and control source to the fanout logic.

The fanout logic contains independent programmable delays for both the clock and control signals to the backplane bus. This capability allows the fanout busses to be tuned for optimal clock/data timing and minimal signal skew on the backplane.

### 4.3.3 Clock and Control Emulator Section

This section provides on-board emulation of the GL1P. It provides the capability for the crate to operate in a standalone mode with no information transmitted or received on the Clock, Control or Status cable links to the Global Clock and Control system. During normal detector operation, this section of the L1CCB is disabled. The emulator circuitry consists basically of a Control cable pattern memory, and a stop/start controllable 16ns clock source.

The pattern memory consists of a 4Kx16-bit RAM, which holds up to 4096 different Control Cable data patterns, and a programmable state machine, which controls the data flow from the RAM. The state machine provides the capability to divide the RAM into sequences of 1 to 4096 Control cable words, as well as to string different sequences together to emulate more complex behavior. The state machine also reacts to signals from frontpanel inputs EXT TRIG 1 and EXT TRIG 2, the subsystem test data MLU in the Subsystem Status I/O section, and the DAQ Processor to permit interrupting of the state machine, and a new sequence to be immediately started. Through these means, a signal applied to EXT TRIG 1, for example, can be used to generate a Level 1 Accept to the subsystem electronics within a consistent and small number of 16ns clock cycles.

The clock source consists of a free-running oscillator which is used to generate a 16ns clock that can be started and stopped cleanly as a result of an EXT TRIG input, DAQ Processor command, or Level 1 Accept. A programmable stop delay counter is included which can be used to stop the 16ns clock in the entire crate on a predetermined number of cycles after generation of a Level 1 Accept. This feature is intended to facilitate testing of subsystem electronics.

### 4.3.4 Subsystem Status I/O Section

This section receives the status information on the four backplane fanins, consolidates it to a single status word, and transmits it up through the Status Cable via the frontpanel. Each fanin contains information wire-OR or wire-ANDed on the backplane from up to four L1CCF or subsystem electronics cards.

Each fanin monitors its incoming status information for proper subsystem response prior to consolidating the statuses together. For example, each Trigger Busy signal is checked for proper response during a Level 1 Reset sequence. This facilitates the detection of improper subsystem behavior which might otherwise be obscured by the consolidation of

the subsystem statuses. Any error detected in this monitoring causes the L1CCB to assert the Trigger Error signal in the status it reports up to the Level 1 Distribution crate.

Any Trigger Error which is either originates at a L1CCB or is reported to a L1CCB in a subsystem crate from the subsystem electronics in that crate is latched in a status register which is accessable to the local crate DAQ Processor. This makes it possibly for the DAQ system to identify the crate or card source that originally reported the error when the Trigger Error is observed by the Global Clock and Control crate.

For use with the Clock and Control Emulator section during standalone mode only, this section has a Test Data MLU which is used to monitor any one of the four fanin sources. This MLU is used to monitor both the Status and Test Data frames sent by a subsystem when operating in emulation or standalone mode. It has the capability to redirect the pattern memory state machine to start a particular Control cable output test sequence. In conjunction with the emulator, this MLU makes it possible to program complex sequences such as a complete Level 1 Reset as a result of a Trigger Error reported by a subsystem.

The fanin receivers also have the capability to compare the received subsystem bunch phases against expected values, and to generate a Trigger Error if a mismatch is detected.

### 4.3.5 Logging Section

The purpose of the logger is to provide a means by which traffic on Control or Status cable interconnections in the Level 1 Clock and Control system can be captured and read out by the DAQ Processor system for subsequent analysis. The logger is a general purpose observability tool, which is crucial to the developement and testing of individual subsystems, as well as the debug and timing alignment of the partially or fully configured detector. The logger can be especially useful for debugging faults in Control or Status cable interconnections, with the L1CCB or L1CCF at each end logging both the transmitted and received data streams, with subsequent comparison for fault isolation.

The L1CCB contains a logging section which can log up to 16K samples from any one of six 16-bit cable sources, using a number of programmable modes and logging trigger sources under DAQ Processor control. The logging capability can be used for system timing alignment, as well as for detection and isolation of cable interconnection problems. The log runs entirely in the backround with respect to the normal fanout/fanin functions of the L1CCB.

The logger in the L1CCB can be selected to log the incoming Status cable data from any of the four backplane status fanins, the consolidated Status cable output, or the incoming or emulated Control cable.

Regardless of whether the L1CCB is operating in normal or standalone mode, the logging section is controlled by the DAQ Processor in the same manner. The DAQ Processor initially selects the cable cable to log from the list given above, the logging mode, and the logging event sources, which are described below. Depending on the mode and event sources selected, logging of cable data into the memory will occur automatically and continue until the log is full or until a stop event is detected. During this time, the DAQ Processor will monitor the status of the logging. When logging has completed, the DAQ Processor will read out the contents of the log and transfer it as necessary for analysis.

The logger has a variety of programmable data collection modes and event sources available. The modes refer to the different methods by which the logger samples the cable data, and the event sources refer to particular decoded control and status signals which are

used to start or stop logging in the specified mode.

The individual logging modes available are as follows:

1. **Event Start, Stop on Full.** Upon receipt of an event, the logging starts on the selected cable, and continues for each contiguous 16ns clock cycle, until the 16K memory is full, or until manually stopped by the DAQ Processor.

2. **Manual Start, Stop on Event.** In this mode, logging on the selected cable is manually started by the DAQ processor, and continues for each contiguous 16ns clock cycle, with memory wraparound, until a trigger is received. Upon receipt of an event, logging stops after a programmable delay of 0 to 256 clock cycles.

3. **Single Cycle.** In this mode, a single cycle snapshot of the contents of the selected cable is taken for each event. Logging continues in this manner until the memory is full.

The logging event sources consist of a number of decoded signals from the incoming Control cable and outgoing consolidated Status cable. These signals are applied to an AND-OR mask, which it makes it possible to generate a trigger based on an OR-combination of unmasked inputs. Note that all of the signals described below are available as logging events regardless of the cable input selected for logging.

These sources have been selected because together they comprise the set of key Control or Status signals which are used to run the Level 1 Trigger system. Proper selection of these events makes it possible to log on virtually any interaction of interest which may occur between the subsystem and the Level 1 Trigger system during subsystem development, testing, alignment, and debug.

1. **DAQ Event.** The event is supplied by DAQ Processor. This event is for circumstances where the logging interval is not associated with any particular Clock and Control or Status event. It is useful for backround logging at random intervals, for example.

2. **Sync Pulse.** The event is supplied by the Control cable Sync Pulse.

3. **Empty Bunch Indicator.** The event is supplied by the Control cable Empty Bunch Indicator.

4. **Bunch 0 Indicator.** The event is supplied by the Control cable Bunch 0 Indicator.

5. **Level 1 Accept.** The event is supplied by the Control cable Level 1 Accept.

6. **Level 1 Reset.** The event is supplied by the Control cable Level 1 Reset.

7. **Trigger Busy.** The event is supplied by the Status cable Trigger Busy.

8. **Data Busy.** The event is supplied by the Status cable Data Busy.

9. **Trigger Error.** The event is supplied by the Status cable Trigger Error.

## 4.4 Level 1 Clock and Control Fanout

The Level 1 Clock and Control Fanout (L1CCF) card is used in the Global Clock and Control and Level 1 Distribution crates to perform the 1-to-4 frontplane fanout of Clock and Control cable information received from the L1CCB via the backplane, and the 4-to-1 fanin of Status cable information received from the frontplane connections. It provides the link between the L1CCB residing in current crate and the L1CCBs in the next level of crates below, as shown in figure 3.

Figure 7 shows a diagram of the L1CCF. It accesses the four backplane fanout/fanin ports provided by the L1CCB, and provides an additional 1-to-4 fanout and 4-to-1 fanin to four Clock, Control, and Status cable interfaces on the frontpanel.

The card is divided into four subsections, all of which have nearly identical counterparts on the L1CCB. The main difference between the cards is that the flow of fanout/fanin data between the backplane and frontpanel is reversed. In addition, the L1CCF possesses no emulation capabilities.

### 4.4.1 DAQ Processor Interface Section

This section provides the interface between the DAQ Processor backplane bus and the on-board address and data busses. It provides the means by which the DAQ processor may access and control the L1CCF. Included in this section is the bus handshaking logic, coarse address decoding logic, and the general control and status registers not associated entirely with any other single section. It distributes the necessary read and write control strobes to the other sections of the L1CCF.

### 4.4.2 Clock and Control I/O Section

This section receives the Clock and Control information from the L1CCB fanout backplane connection, performs a 1-to-4 fanout on it, and retransmits it out the frontpanel on 4 pairs of Clock and Control cables. This section also includes the necessary on-board distribution logic for the 16ns clock, as well as the Level 1 Control signals which are decoded from the Control cable frames.

### 4.4.3 Subsystem Status I/O Section

This section receives the Status cables on the four frontpanel fanins, consolidates their contents to a single status word, and transmits it to the L1CCB via the backplane.

Each frontpanel fanin monitors its incoming status information for proper subsystem response prior to consolidating the statuses together. For example, each Trigger Busy signal is checked for proper response during a Level 1 Reset sequence. In this respect, the functionality of this section is identical to that on the L1CCB. Any errors detected will be encoded into the Status Cable as a Trigger Error, as well as reported to a board status register which is accessable and can be monitored by the DAQ Processor.

The fanin receivers also have the capability to compare the received subsystem bunch phases against expected values, and to generate a Trigger Error if a mismatch is detected.

#### 4.4.4 Logging Section

The logging section on the L1CCF is basically identical to that used on the L1CCB. It has six cable sources, programmable logging modes and a programmable trigger, all controlled by the DAQ Processor.

The logger on the L1CCF can select input from any of the four input Status cables, the consolidated Status being sent to the L1CCB, or the incoming Control word received from the L1CCB. The output Control cables are not logged because they contain an identical rebroadcast of the Control word received from the L1CCB on the backplane.

See the section on logging for the L1CCB card for a detailed description of the logger used on the L1CCF.

# 5 Physical Requirements

## 5.1 Crate Summary

Summary of Minimum Crate Usage in the Level 1 Clock and Control System:

| Crate Type | Quantity | Comments |
|---|---|---|
| Global Clock and Control | 1 | Master for Detector |
| Level 1 Distribution | 1 | for Level 1 Trigger Decision |
| Level 1 Distribution | 2 | for Calorimeter Front End |
| Level 1 Distribution | 2 | for Tracker Front End |
| Level 1 Distribution | 1 | for Muon Detector |
| Level 1 Distribution | 1 | for Silicon Front End |
| Total Crates: | 8 | |

Note: this summary assumes maximum utilization of capacity in the Level 1 Distribution crates, with partitioning of the Clock and Control system only along major subsystem boundaries, as shown above. Further partitioning within subsystems is possible through the use of additional Level 1 Distribution crates.

## 5.2 Card Summary

Summary of Card Usage in the Level 1 Clock and Control System:

| Card Type | Nominal per Crate Usage | Total Quantity | Comments |
|---|---|---|---|
| Clock and Control L1CCB | 1 | 8 | in Clock and Control system |
| Level 1 Trigger L1CCB | 1 | 50 | in Level 1 Trigger Decision |
| Calorimeter L1CCB | 1 | 96 | in Calorimeter Front End |
| Tracker L1CCB | 1 | 80 | in Tracker Front End |
| Muon L1CCB | 1 | 48 | in Muon Front End |
| Silicon L1CCB | 1 | 64 | in Silicon Front End |
| Total L1CCB Usage: | | 346 | |
| | | | |
| Level 1 Trigger L1CCF | 13 | 1 | distribution to Level 1 Dec. |
| Calorimeter dist. L1CCF | 12 | 2 | distribution to Calorimeter |
| Tracker dist. L1CCF | 10 | 2 | distribution to Tracker |
| Muon dist. L1CCF | 12 | 1 | distribution to Muon system |
| Silicon dist. L1CCF | 16 | 1 | distribution to Silicon system |
| Total L1CCF Usage: | | 85 | |

# 6 System Operation

## 6.1 Global Configuration

The basic architecture for the GL1P is that of a fully pipelined structure with a 16ns clock. The latency of data flow through all of both the Clock and Control and Trigger Decision cards is characterized in terms of machine clock cycles from data in to data out, as is the latency of all electrical or fiber optic cable connections containing trigger data or control and status information. The result is a complex structure in which raw trigger data flows to the GL1P decision logic from a number of front end subsystems, each at a different offset with respect to the absolute bunch phase. Each trigger decision subsystem in turn has its own offset with respect to the front end data as well as the other trigger decision subsystems. At the Final Decision crate, the remaining offsets between trigger decision data streams are reconciled to a single offset. Concurrently, offsets exists between individual subsystem crates for the distribution of Clock and Control data. These offsets reflect mainly the difference in cable interconnection lengths between those crates on the detector and those upstairs. Thus, each crate is assigned offsets which reflect both its position in the trigger decision pipeline as well as its distance from the Clock and Control crate in the clock and control pipeline. By assigning downloaded offsets to individual crates and then monitoring their returned bunch phases as described below, it is possible to adust for these different delays and to detect misalignment conditions which may occur during system operation.

During normal operation, the Clock and Control System hardware throughout the detector will be linked together through the Level 1 Distribution crates to form a single distribution tree. In this tree, all clock and control information originates at the Global Clock and Control crate, and all subsystem status information is funneled back to this crate.

The crates are linked together with Clock, Control and Status cables.

In this global configuration, the L1CCB and L1CCF cards throughout the detector in the Level 1 Distribution and individual subsystem crates serve essentially as repeaters in both directions of clock, control, and status information passed between the Global Clock and Control crate and the individual subsystem crates.

While serving as repeaters of traffic between these two end points, the L1CCB and L1CCF do have the capability to monitor this traffic. Specifically, these cards have the following capabilities:

1. To log the flow as a backround activity at any of the six input or output cable sources on a L1CCB or L1CCF card, namely the Control cable input, Status cable output, or any of the four Status cable inputs,

2. to intantaneously check the validity of a bunch phase transmitted on any Control or Status frame against an expected value, thereby providing a pervasive test of the system timing integrity during actual operation.

### 6.1.1 Level 1 Reset Sequence

A Level 1 Reset is issued by the Global Clock and Control crate in response to an operator request or as a result of a Trigger Error signal being propagated up from the detector or from the Level 1 Trigger Decision subsystem. The Trigger Error is originally asserted by a subsystem, a L1CCB, or L1CCF as a result of the detection of a non-recoverable error. The Trigger Error is propagated through the layers of status consolidation performed by the L1CCBs and L1CCFs through a logical OR tree. When it reaches the control logic in the Global Clock and Control crate, the reset sequence will be initiated.

The Level 1 Reset sequence consists of the following stages:

1. The control logic in the Global Clock and Control crate generates an Idle frame on the Control cable, with the Level 1 Reset signal active for one 16ns clock cycle.

2. The frame is distributed to all subsystem crates through the Level 1 Distribution crates.

3. The frame is received by the L1CCBs in all subsystem crates, and is rebroadcast down the crate backplanes to subsystem electronics cards.

4. During propagation of the Level 1 Reset signal throughout the detector, the Global Clock and Control crate internally inhibits the transmission of any further Level 1 Accept signals and waits for a Trigger Busy to be propagated back from the detector.

5. The subsystems respond to the Level 1 Reset by asserting their Trigger Busy signal in a Status frame back to the L1CCBs in the subsystem crates. This is the subsystems method for acknowledging receipt of the Level 1 Reset signal. Once asserted, Trigger Busy must remain active during the entire reset sequence.

6. The L1CCBs in the subsystem crates and the L1CCBs/L1CCFs in the Level 1 Distribution crates consolidate the individual subsystem Trigger Busy using a logical AND operation. This guarantees that the Global Clock and Control crate will not see the Trigger Busy until it has been asserted by *all* subsystems

7. The Trigger Busy is observed by the Global Clock and Control state, at which time it waits for a bunch 0 crossing, while still inhibiting the transmission of a Level 1 Accept.

8. The entire detector remains in this wait state until the next occurence of the bunch 0 crossing, at which point the Bunch 0 Indicator signal is sent from the Global Clock and Control crate. This signal propagates through the distribution system to all subsystem crates to restart them, thereby clearing the Trigger Busy condition.

Although the propagation time of a Level 1 Reset pulse to the subsystems to initiate the reset sequence is non-critical, the propagation time of the Bunch 0 Indicator pulse to terminate the sequence is. Each subsystem crate has a known calculated distance in terms of crossing clocks for signal propagation from the Global Clock and Control crate. These distances are used for the calculation of the timing offsets between individual subsystem crates.

From the time that the Level 1 Reset signal is transmitted from the Global Clock and Control crate until the first incidence of the Bunch Crossing 0 Indicator *after* the Trigger Busy has propagated back from all subsystem crates, a Level 1 Accept will **not** be transmitted from the Global Clock and Control crate to the subsystems.

### 6.1.2 Level 1 Accept Sequence

A Level 1 Accept is issued to all subsystems by the Global Clock and Control crate normally in response to input from the Level 1 Decision logic or due to an operator request. The Level 1 Accept as transmitted by the Global Clock and Control crate is always associated with a particular bunch crossing in the detector, even for those triggers such as cosmic ray triggers which are not directly associated with a crossing.

Level 1 Accepts are transmitted to all front end and trigger subsystem crates in the detector. They are used by front end subsystems to capture into buffer storage the data associated with particular crossings, and to hold that data for readout by the DAQ system. They are used by trigger subsystems to capture the raw trigger data coming up from the front end crates, and to similarly hold it for readout to the Level 2 Trigger.

The Level 1 Accept is transmitted from the Global Clock and Control crate at an offset that will be fixed and will be somewhere between 132–182 crossing clock cycles after the interaction. Through the use of preassigned downloaded crossing offsets, each crate will automatically know which crossing to apply the Level 1 Accept upon its receipt.

The Level 1 Accept sequence consists of the following stages:

1. An interaction of interest occurs in the detector.

2. Front end DAQ subsystems capture the event and hold it in analog or digital buffer storage pending transmission of a Level 1 Accept. They also transmit a portion of the event data off the detector to the Level 1 Trigger Decision crates as raw trigger data.

3. The trigger decision crates receive the raw trigger data and buffer it also, pending a Level 1 Accept.

4. The trigger decision crates process the data in a 16ns pipeline over a number of crossing clock cycles. This includes feed-forward interconnections between multiple layers of crates.

5. The last level of decision processing is performed by the Final Decision crate. At this point, the accept/reject decision is made for the interaction, with any ambiguity necessary applied.

6. The decision to issue a Level 1 Accept for the crossing is shipped to the Global Clock and Control crate, where it reconciled with any pending status conditions in the detector, such as a Data Busy or Level 1 Reset-in-progress. If the detector is able to trigger, then the Level 1 Accept is integrated by the control logic into a Control cable Trigger frame, along with the trigger and readout type values.

7. The Level 1 Accept is transmitted to all detector crates from the Global Clock and Control crate through the Level 1 Decision crates.

## 6.2 System Partitioning

Through the Control cable emulator capabilities built into the L1CCB, it is possible to split apart the subsystems of the detector, and operate each subsystem or crate independently, with a limited capability. This functionality makes it possible to separately install and test individual components of the detector prior to the full integration of the system.

Partitioning into subsystems is accomplished by shutting off the link between the Level 1 Distribution crate(s) for a subsystem and the Global Clock and Control crate. This shuttoff is accomplished by the DAQ Processors controlling both the L1CCB in the Level 1 Distribution crate, and the L1CCF in the Global Clock and Control crate. Under local DAQ Processor control, The L1CCB in the distribution crate then takes over the function of generating Clock and Control cable data and responding to Status cable information for the subsystem. The L1CCFs in the Level 1 Distribution crate continue to function as before, interfacing between the L1CCB in their crate and the L1CCBs in the individual subsystem crates.

Partitioning by individual crates is accomplished by shutting off the link between the Level 1 Distribution crate and the subsystem crate. As in the previous case, this is done under DAQ Processor control. In this case, the L1CCB in the subsystem crate acts as the Clock and Control emulator. In this configuration, the crate operates independently from all other crates in the detector.

The Level 1 Trigger Decision logic presents a special case in partitioning. Conceived as a subsystem of its own, alongside the various front end DAQ subsystems, it nonetheless has components within it that are closely associated with each of the DAQ subsystems. For some types of testing, it is desirable to include both the front end DAQ crates and their associated Level 1 Trigger crates in the same test partition. To accomodate this situation, the Level 1 Trigger Decision subsystem, along with the selected DAQ subsystems, can be controlled from the Global Clock and Control crate as a limited configuration using as much of the trigger decision logic as possible (based on which subsystems are available in the limited configuration). The remaining subsystems which are not in the configuration may be operated on a subsystem or individual crate standalone basis, using the emulation capabilities in the L1CCBs in their Level 1 Distribution and subsystem crates.

## 6.3 Timing Alignment

In order to guarantee that all subsystem crates come out of the reset with the proper timing relationships with respect to each other, it is necessary that each crate has the capability to apply an offset to its own returned bunch phase counter which reflects both the latency of data through that crate as well as the length of the connection to the Clock and Control section. Furthermore, some crates, particularly in the Level 1 Trigger Decision subsystems must have the capability to provide a programmable multi-clock buffer delay on data that they transmit to or receive from other crates. This delay is necessary to compensate for the different inherent processing latencies in the different crates, which must be reconciled by the time trigger decision data arrives at the Level 1 Final Decision crate.

With these capabilities, it is possible to both define the relative time of each individual front end or trigger subsystem crate in the overall Level 1 Trigger pipeline, and to adjust the timing delays of convergent data streams as necessary to guarantee the proper alignment of data for trigger decision calculations.

# 7 Level 1 Simulation Module

The Level 1 Simulation Module (L1SM) shown in Figure 8 emulates all of the above control sequences described above for the Level 1 Clock and Control System. Its purpose is to aid in the debugging of Subsystem DAQ and trigger circuits, and to serve the basic functions of a trigger module for test experiments.

## 7.1 General Overview

The L1SM has a subset of the functionality of a L1CCB. Basically, it operates as an L1CCB in standalone emulator mode. It has no frontpanel connections for Clock, Control or Status cables. Further, it does not provide a 4X fanout/fanin capability. Instead, the L1SM interfaces to a single Control/Status cable port on the backplane.

Physically, the L1SM is a 6 Eurocard Unit high VME module of standard depth (160 mm) with standard J1 and J2 Eurocard connectors, with Clock, Control and Status cable signal assignments made to the unallocated J2 connector pins. The expected density of components on the board will likely require the used of a mixture of both through-hole and surface-mount devices. All components will be mounted on only one side.

Electrically, the L1SM will consist primarily of TTL logic to implement the VME interface, and ECL logic, including high-speed memories, to implement many of the emulation functions.

To support off-crate Control and Status cable connections, a companion J2 buffer/-extender card will be developed with the L1SM. This card will provide an active bus interface between the Clock, and single-ended Control and Status signals on the J2 connector and differential equivalents to be sent or received from the subsystem electronics via an electrical cable interconnection.

## 7.2 Functional Description

The L1SM is divided into five functional sections. Some of these sections correspond generally to a counterpart on the L1CCB, with differences due primarily to the limited mission

and form factor of the L1SM. The sections are described below.

### 7.2.1 VME Interface Section

This section implements an (A32:D16) VME slave. This includes the bus interface logic, address decoding, and handshaking for DTACK generation. The upper 8 bits of the address are interpreted by the card as a slot address. The card will also be able to respond to a programmed Address Modifier (AM) code. Both the slot address and the AM code will be programmed by on-board DIP-switches.

This section also contains general control and status registers accessable to the VME bus master. This includes registers which are not explicitly inclusive to any other single section of the L1SM. The card will also have the capability to generate an interrupt request (IRQ) at a selection priority level.

The hardware in this section will consist primarily of commercially available TTL-type logic. This will include the use of one-time programmable logic devices (PLDs) such as combinatorial and registered PALs to implement the handshaking logic and some of the address decoding.

### 7.2.2 Clock and Control Emulator Section

The Clock and Control Emulator Section of the L1SM is essentially the same as that planned for the L1CCB. This section provides an emulated machine clock from an on-board clock source, as well as emulated Control cable data from a programmable 4Kx16-bit programmable high-speed SRAM, which is controlled by a programmable state machine.

The clock source consists of a free running 8ns oscillator, an 8-bit prescaling counter, and some sequential logic, which produces a clock which is both balanced in duty cycle, and able to be both cleanly stopped or started to or from a selectable high or low level. The 8-bit prescaler permits the the generation of a machine clock source which has a programmable period in the range of 16ns to 4.096$\mu$s, in 16ns increments. This clock is distributed both locally on the board, and to the backplane as the emulated Clock cable connection. The machine clock distributed to the backplane will be phased with respect to the Control cable such that it will serve as a data strobe for the Control cable data in addition to being a timebase source for the subsystems.

The Control cable output pattern memory is implemeted using a 4Kx16-bit high-speed ECL SRAM structure, with a access time of approximately 10ns for operation at the worst-case cycle time of 16ns. This pattern memory is user-programmable via the VME interface, and during emulation will produce a 16-bit Control word on each clock cycle.

The address control to the 4Kx16-bit pattern memory is provided by a programmable state machine. The state machine is build around a 32-bit descriptor word. A descriptor word defines the location and length of a stream of contiguous sequential Control cable words to be generated from pattern memory, the number of times that sequence should be generated, and the address in a descriptor word store of the next descriptor word to be processed. A total of 256 descriptor words are held in a programmable fast SRAM descriptor word store, which is accessable through the VME interface. Each descriptor word is divided into four 8-bit fields. They are defined as follows:

**Pattern Start Address.** This field contains the starting address of a contiguous pattern sequence to be generated from the pattern memory. Its 8 bits constitute the most

significant portion of the 12-bit pattern memory address. The low order 4-bits of the pattern memory start address are assumed to be zero. It is possible to begin a pattern sequence at any of 256 of the 4096 possible locations in pattern memory, at those locations which fall on 16-word boundaries. Thus, patterns can begin at pattern memory decimal addresses 0, 16, 32, 64, etc.

**Pattern Length** This field contains an 8-bit length of a contiguous pattern sequence to be generated from the pattern memory. This field makes it possible to specify a sequence length of 1 to 256 sequential words from pattern memory.

**Loop Count** This field contains an 8-bit loop count for the number of times the pattern sequence described in the fields above should be generated. If this field is zero, then the sequence will only be generated once, and then control will passed to the descriptor word referenced in the next address field described below.

**Descriptor Word Next Address.** This field contains the 8-bit branch address of the next control word to be executed in the descriptor word store. Upon generation of the full sequence for the specified loop count, output of a new sequence from pattern memory as specified by the next control word will immediately commence, with no gap or "bubble" in the emulated Control cable data stream. Through proper programming, control words can be linked together in such a way as to produce a single pattern sequence which uses the entire 4K of pattern memory. Infinite loops of any number from 1 to 256 descriptor words are implemented by having the next address field of the last descriptor word executed branch back to the first.

As is the case with the pattern memory, the state machine will be implemented largely with ECL logic and SRAMs, with a 16ns clock cycle time and 10ns RAM access times. A TTL interface to the memory will be provided for VME and on-board address and data bus read/write access to the 256 word control store for programming and verification.

Emulation of Control words thus requires the programming of both the pattern memory, which contains the 4096 words of data to be transmitted out the backplane as the Control cable information itself, as well as the descriptor word store, which contains the 256 descriptor words which define the location, size, and loop count of the pattern sequences to be generated.

The emulator section also contains an 8-bit bunch phase counter which can be used to provide the 8 bits of bunch phase which are included in an Idle frame of a Control word. This allows sequences of control words to be independent of the current bunch value.

### 7.2.3 External I/O Section

This section provides the electrical and mechanical translation between the frontpanel trigger connections and their on-board signal counterparts. At this time, the connector type has not been chosen.

There are two frontpanel external trigger inputs, labeled EXT TRIG 1, and EXT TRIG 2. There is also an external trigger output, labeled EXT TRIG OUT. The trigger inputs have the capability to force an immediate branch (in effect, an interrupt) in the emulator state machine to a descriptor word address vector preprogrammed in a VME-written register. A single vector register is shared by both inputs.

The descriptor word or sequence of descriptor words associated with the external trigger interrupt may be programmed to produce whatever emulated Control cable behavior that is desired as a result of that interrupt, such as a Level 1 Accept, or Level 1 Reset sequence.

The EXT TRIG OUT connector monitors the on-board Level 1 Accept signal, and produces a 16ns Level 1 Accept pulse from that produced by the Control cable emulator. This signal may be used by other electronics as a test trigger during development of subsystems.

### 7.2.4 Subsystem Status Section

The Subsystem Status Section provides a means of feedback by which data returned from the subsystem on the Status cable can affect the subsequent emulated output to the Control cable. This data consists of both Status frames, and Test Data frames. It also can check the bunch phase in a Status frame against an expected value, to provide timing integrity checking.

In normal subsystem operation, only Status frames are transmitted to the Level 1 Clock and Control system. Trigger data is transmitted up to the Level 1 Trigger Decision crates for processing. In subsystem or crate standalone configurations, however, these trigger decision crates may not be available. As a stand-in, the Test Data frame on the Status cable makes it possible for the subsystem to send a *limited amount* of trigger data to the L1SM. The L1SM can then perform some limited decision-making functions based on this data using MLUs.

The method of feedback is to force an interrupt branch in the state machine, like that described in the External I/O section, as a result of the contents of the Status cable. Two high speed memory lookup tables (MLUs) are used to provide the feedback capability. The first MLU is 16Kx1-bit in size, and is used to look at the 14 bits of test data if a Test Data frame is transmitted on the Status cable. The result of this MLU operation is a single flag which indicates if a interrupt branch should be taken for the test data provided. The second MLU is 1Kx12-bits in size, and is used to perform a lookup based on bits 0-7 of a Status frame transmitted on the Status cable. The result of this MLU operation is an 8-bit tenative interrupt vector to the control word state machine, an interrupt request flag due to status, a test data frame interrupt enable, and two generic state machine bits which are fed around back to the input of this status MLU. These last two bits are particularly important because the make it possible to program this MLU to implement a four-state state machine that can remember prior subsystem status activity and use it to generate more complex interrupt behavior.

The outputs of these two MLUs are tied together with combinatorial logic which produces a interrupt request and an interrupt vector to the control word state machine. The feedback within the status MLU makes it possible for the subsystem to generate its own fully-interlocked Level 1 Reset sequences automatically from a Trigger Error or any other status bit, as well as many other Control cable sequences.

As is the case with the Emulator Section, the Subsystem Status section uses high-speed 10ns ECL SRAMs, combined with ECL and TTL combinatorial logic. Both MLUs are accessable through the VME interface.

Finally, this section contains a preloadable 8-bit counter and equivalence comparator which can be used to compare the incoming bunch phase in a Status frame against programmed expected value. This feature can be used for runtime integrity testing, as well as system timing alignment.

Table 3: J2 BACKPLANE CONNECTIONS

| Level 1 Clock Cable | |
|---|---|
| Pins | Data |
| a1 | GND |
| a2 | 62.5 MHz clock + |
| a3 | 62.5 MHz clock − |
| a4 | GND |
| **Level 1 Control Cable** | |
| Pins | Data |
| a5–a7 | Reserved for Power/GND |
| a8–a23 | Control Frame Bits 0–15 |
| a24–a32 | Reserved for Power/GND |
| **Level 1 Status Cable** | |
| Pins | Data |
| c5–c7 | Reserved for Power/GND |
| c8–c23 | Status Frame Bits 0–15 |
| c24–c32 | Reserved for Power/GND |

### 7.2.5 Logging Section

The logging section in the L1SM is functionally very similiar to that defined for the L1CCB and L1CCF. The only differences are as follows:

1. The size of the log is 4Kx16-bits instead of 16Kx16-bits, and
2. rather than six possible input sources, the L1SM logging section may select only from either the emulated Control cable output, or single returned subsystem Status cable input.

In terms of the types of modes and triggers available, the L1SM logger is identical to that used on the L1CCB and L1CCF. The logger memory will be addressable from the VME interface for read and write operations.

The logger utilizes fast ECL SRAMs with a 10ns access time and a 16ns cycle time. The control circuitry in this section consists of a mixture of ECL and TTL logic.

## 7.3 Backplane Connections

As stated previously, the L1SM uses the standard J1 and J2 allocations for VME operation. This includes signals, power and ground. To support the Clock, Control and Status cable connections, additional allocations are made to J2 on pins not assigned by the VME interface.

Table 3 shows a preliminary assignment of these additional signals. All signals are defined as 100K ECL inputs or outputs. All outputs will be unterminated, and all inputs will be terminated on the L1SM to -2V at 100 ohms. All Control and Status cable signals are defined to be single ended, while the 16ns clock is driven out differentially.

# References

[1] W.H. Smith, T. Gorski, J. Lackey, *SDC Trigger Preliminary Conceptual Design*, SDC note SDC-91-00089, 1991.

[2] T. Gorski, J. Lackey, W.H. Smith, *Level 1 Trigger Decision Design for the SDC*, SDC Note SDC-91-00088, 1991.

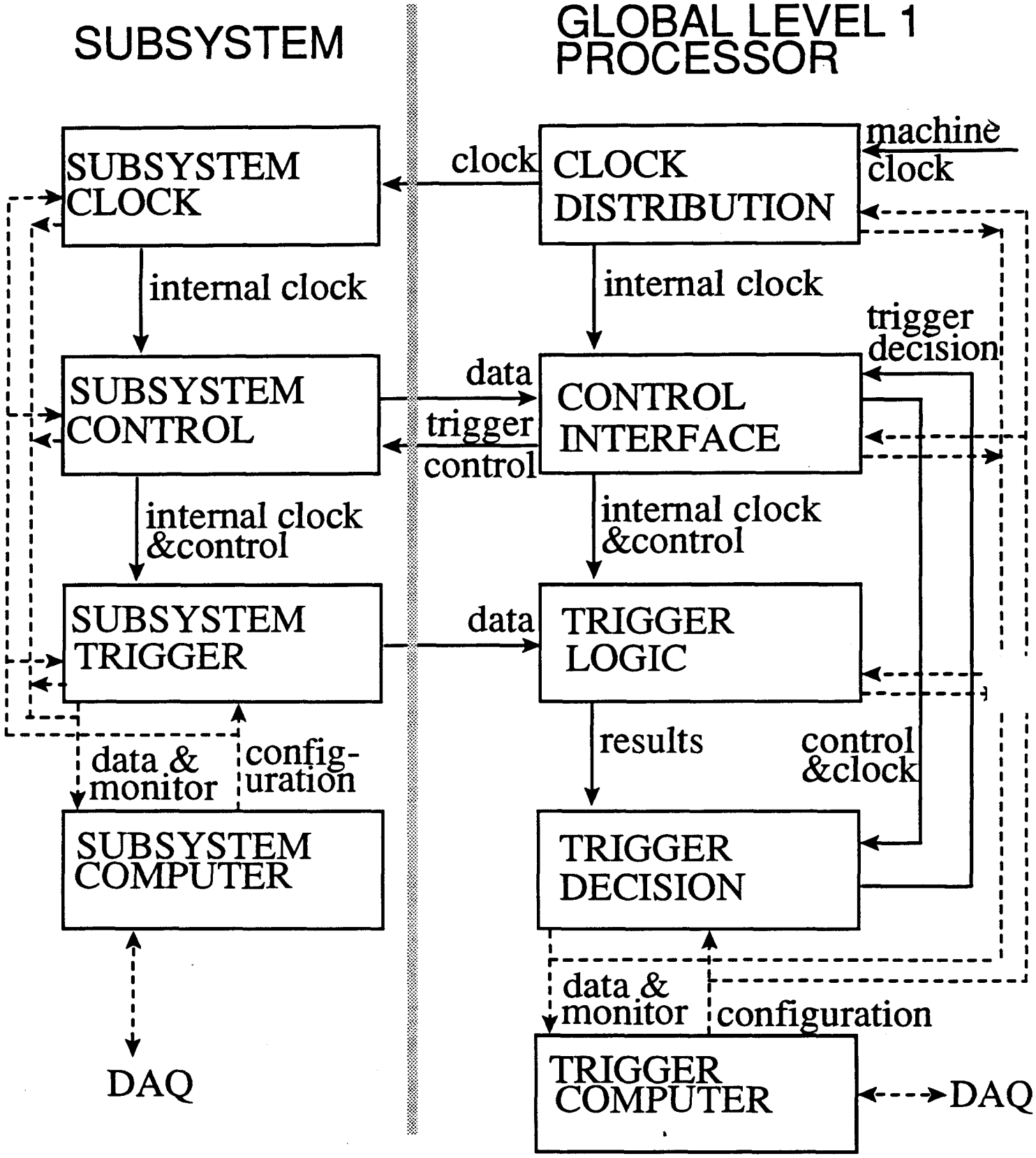


Figure 1. Functional Block Diagram of the Global Level 1 Processor

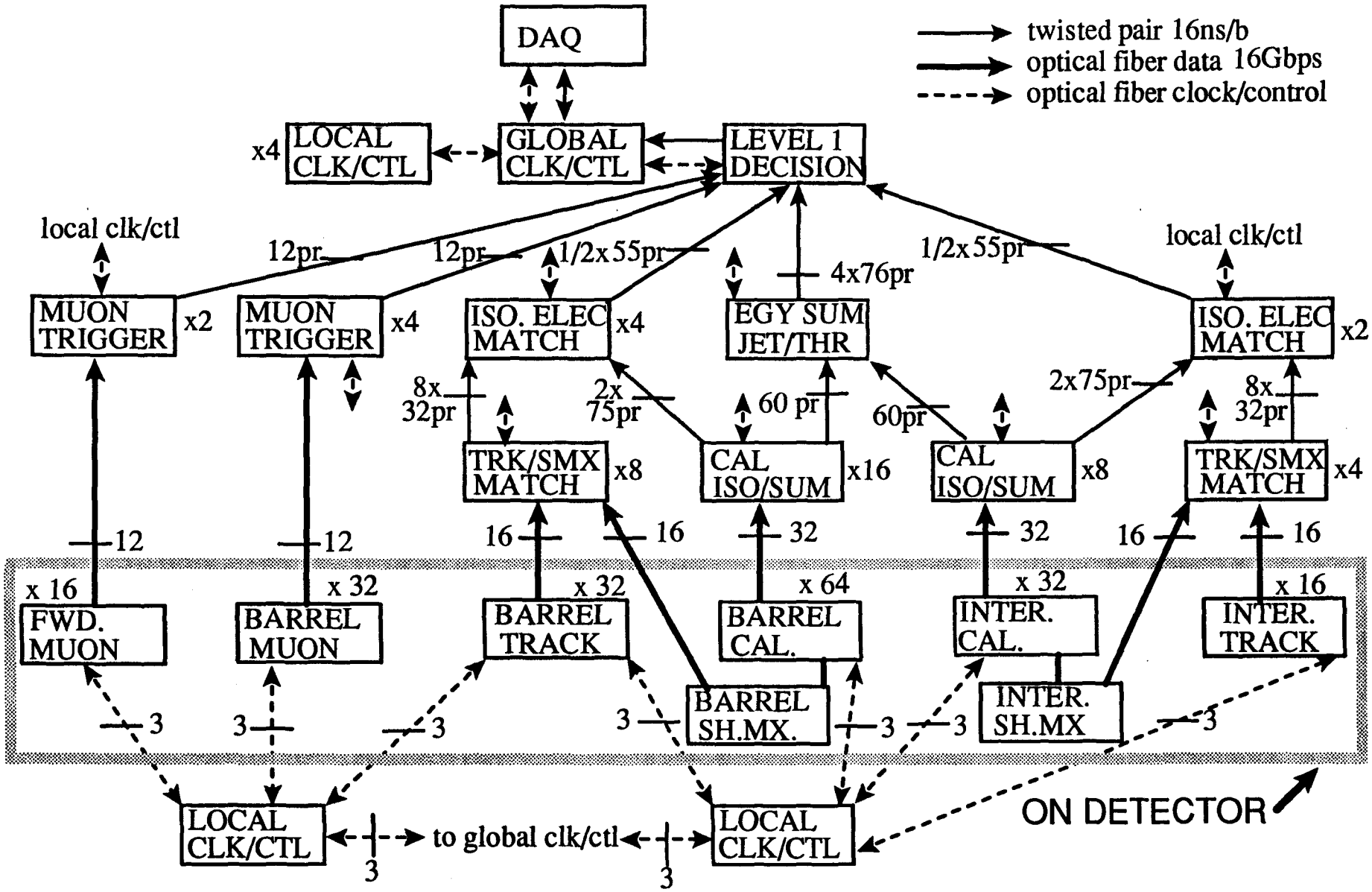


Figure 2. Layout of the Level 1 Trigger System

# Level 1 Clock and Control Distribution System

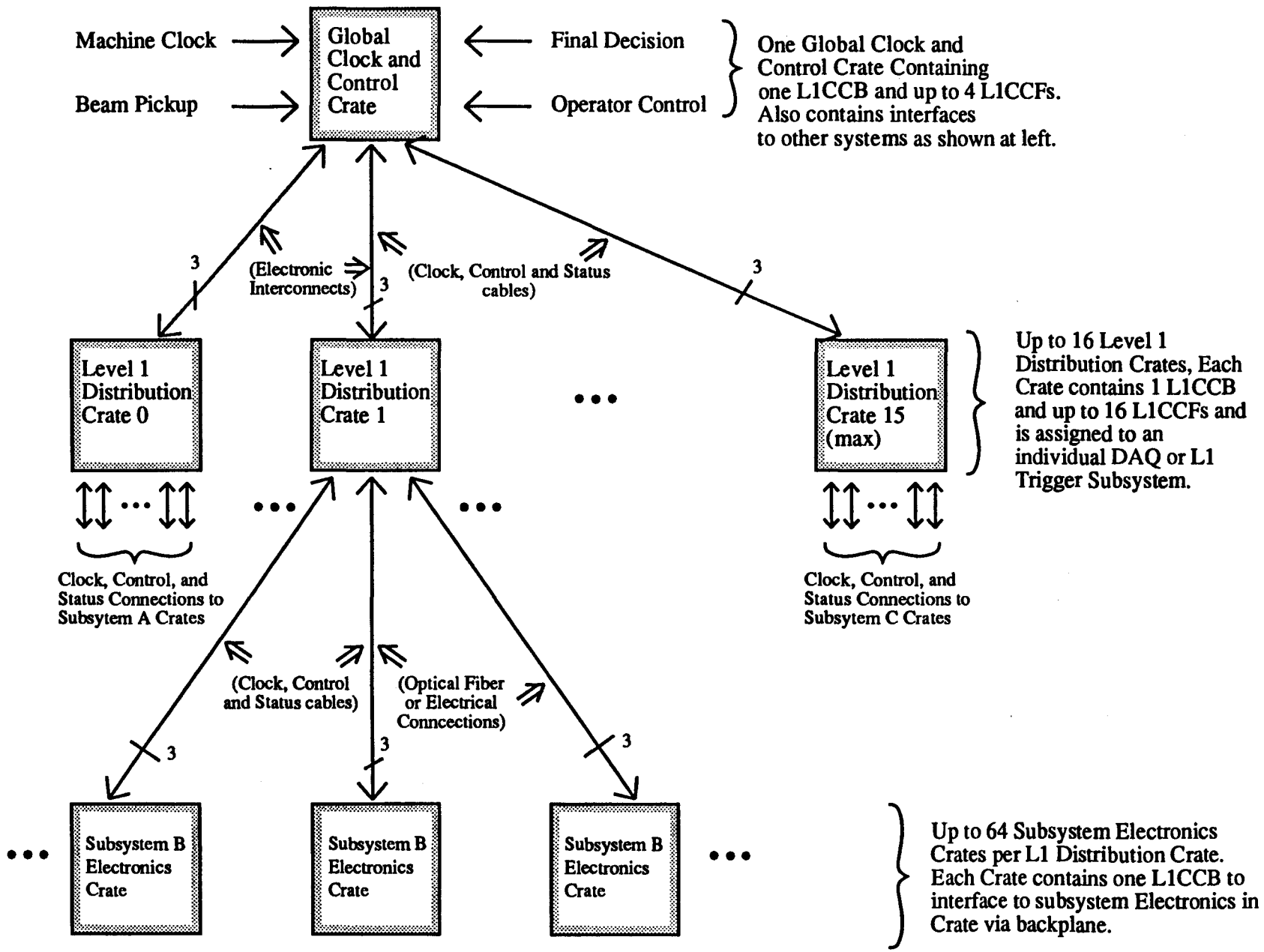


Figure 3

# Global Clock and Control Crate Coverage: Entire Detector

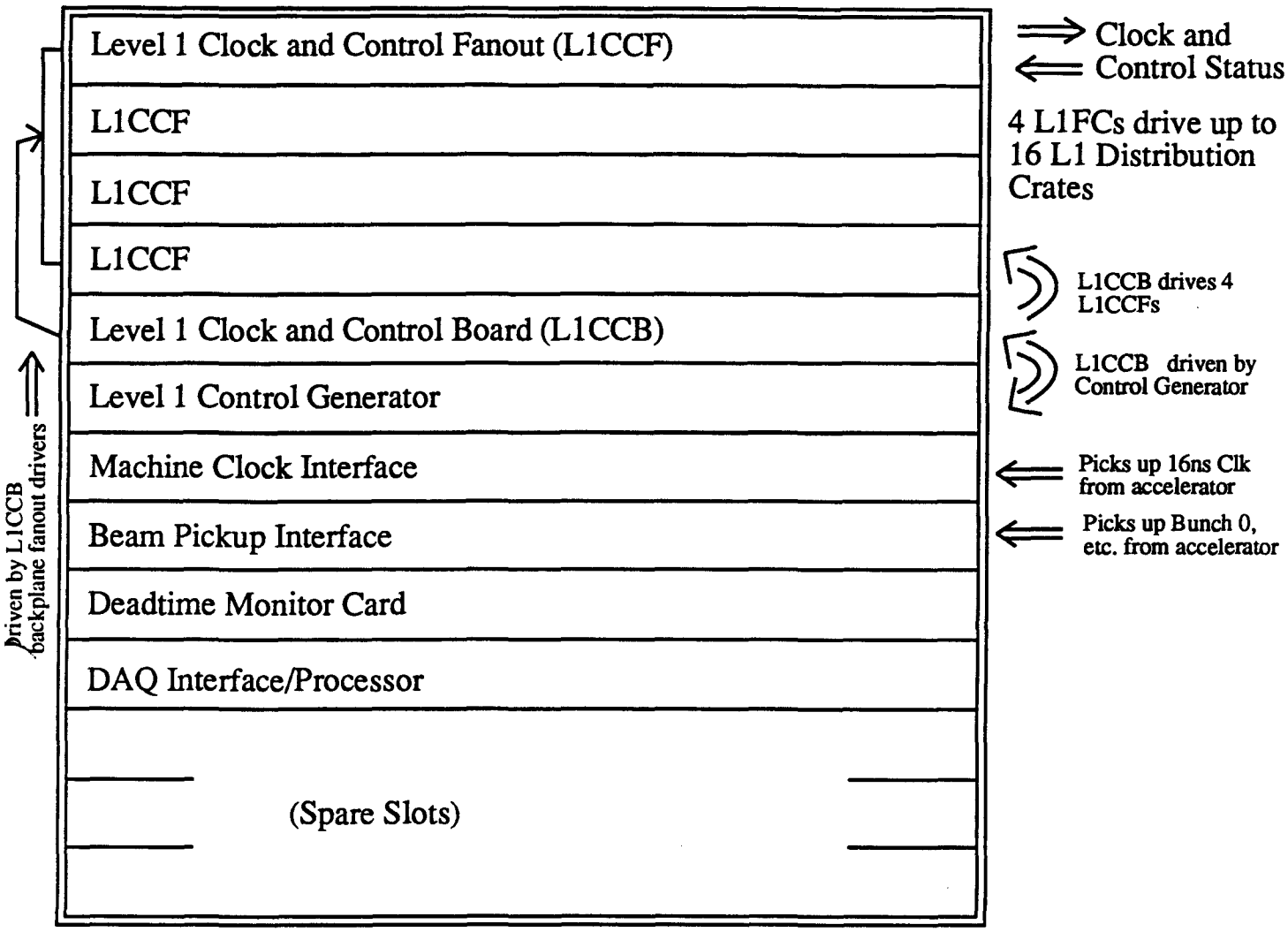


Figure 4

# Level 1 Distribution Crate

## Coverage: Up to 64 Subsystems Crates

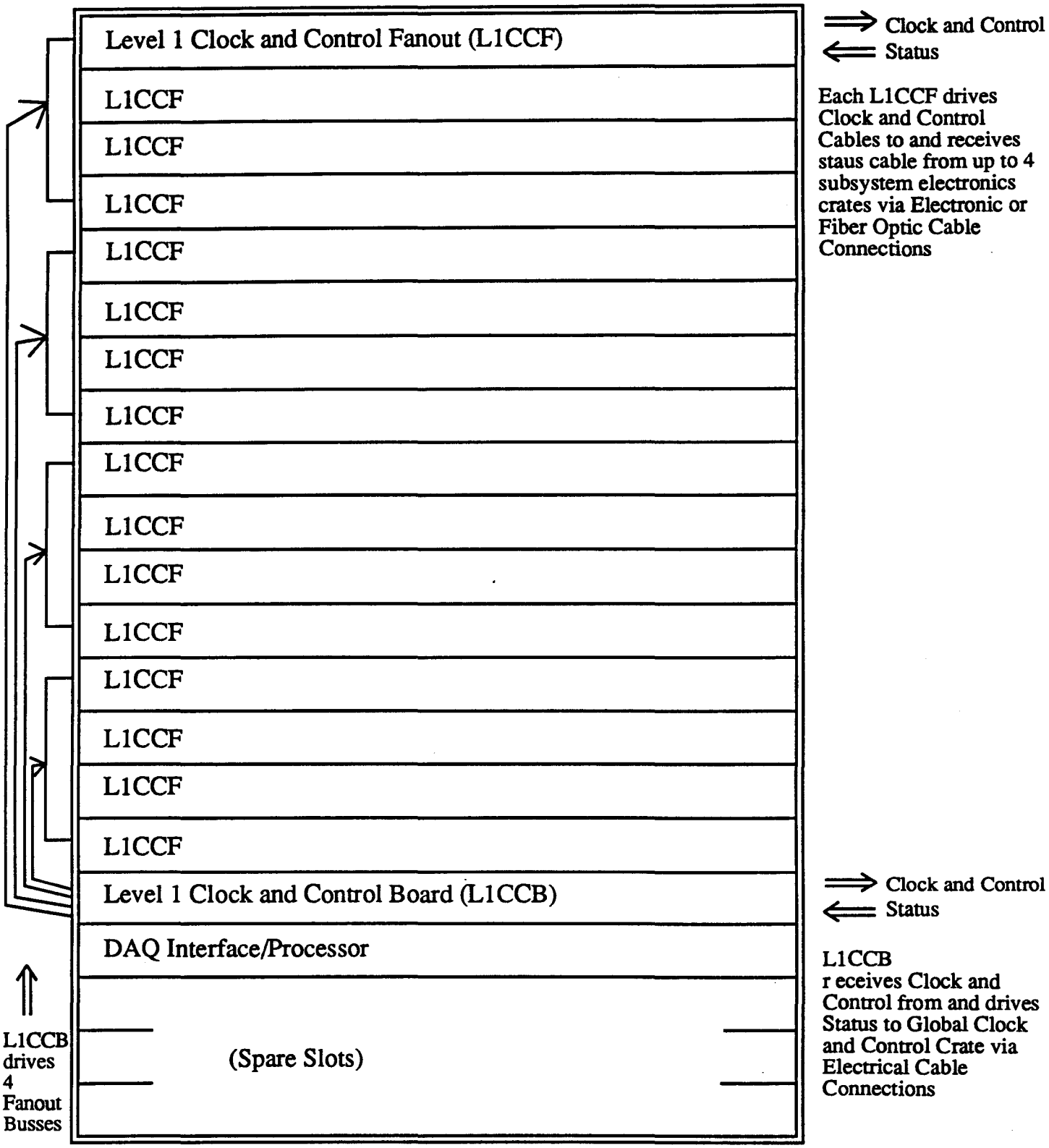


Figure 5

# Level 1 Clock and Control Board (L1CCB)

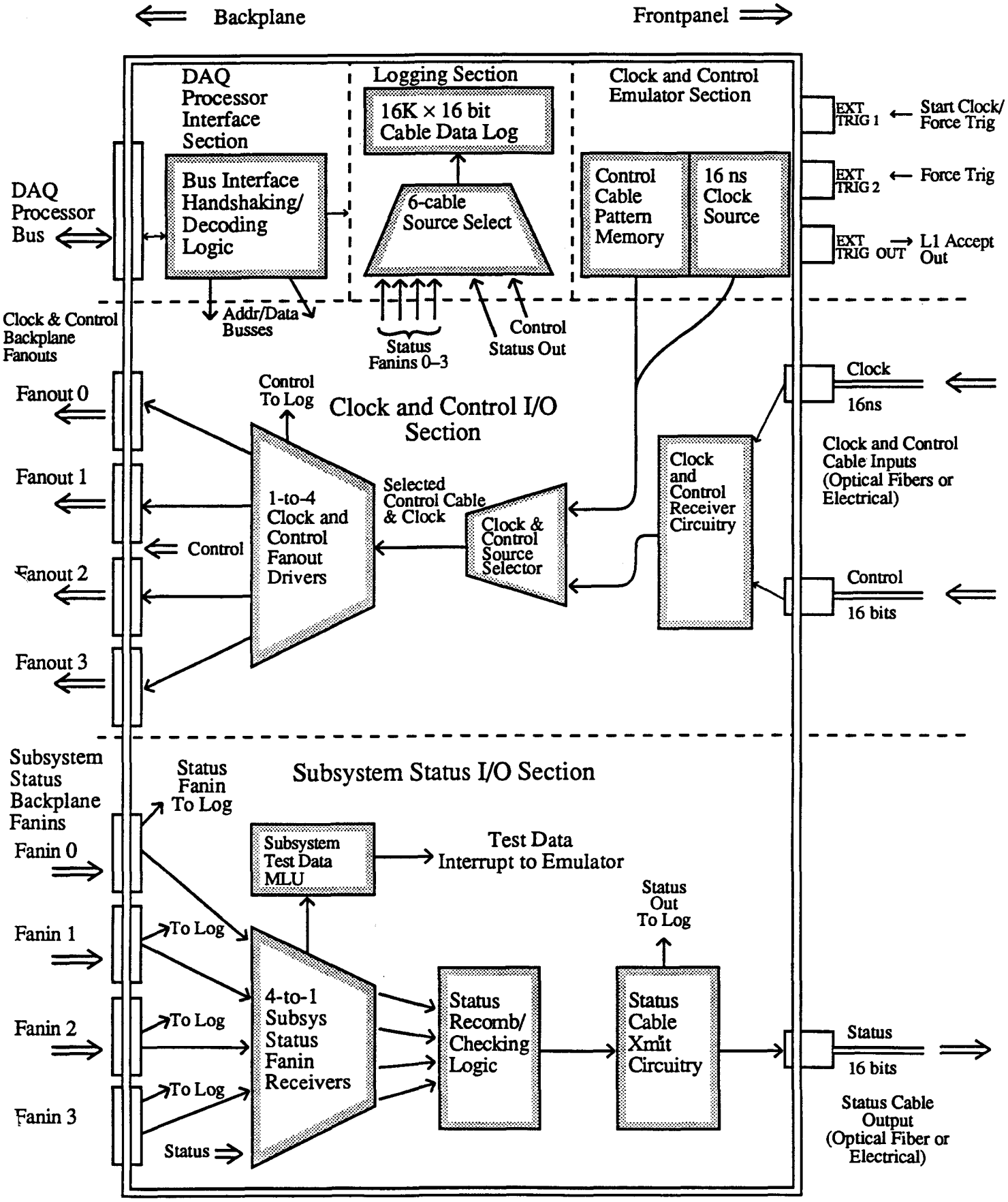


Figure 6

# Level 1 Clock and Control Fanout (L1CCF)

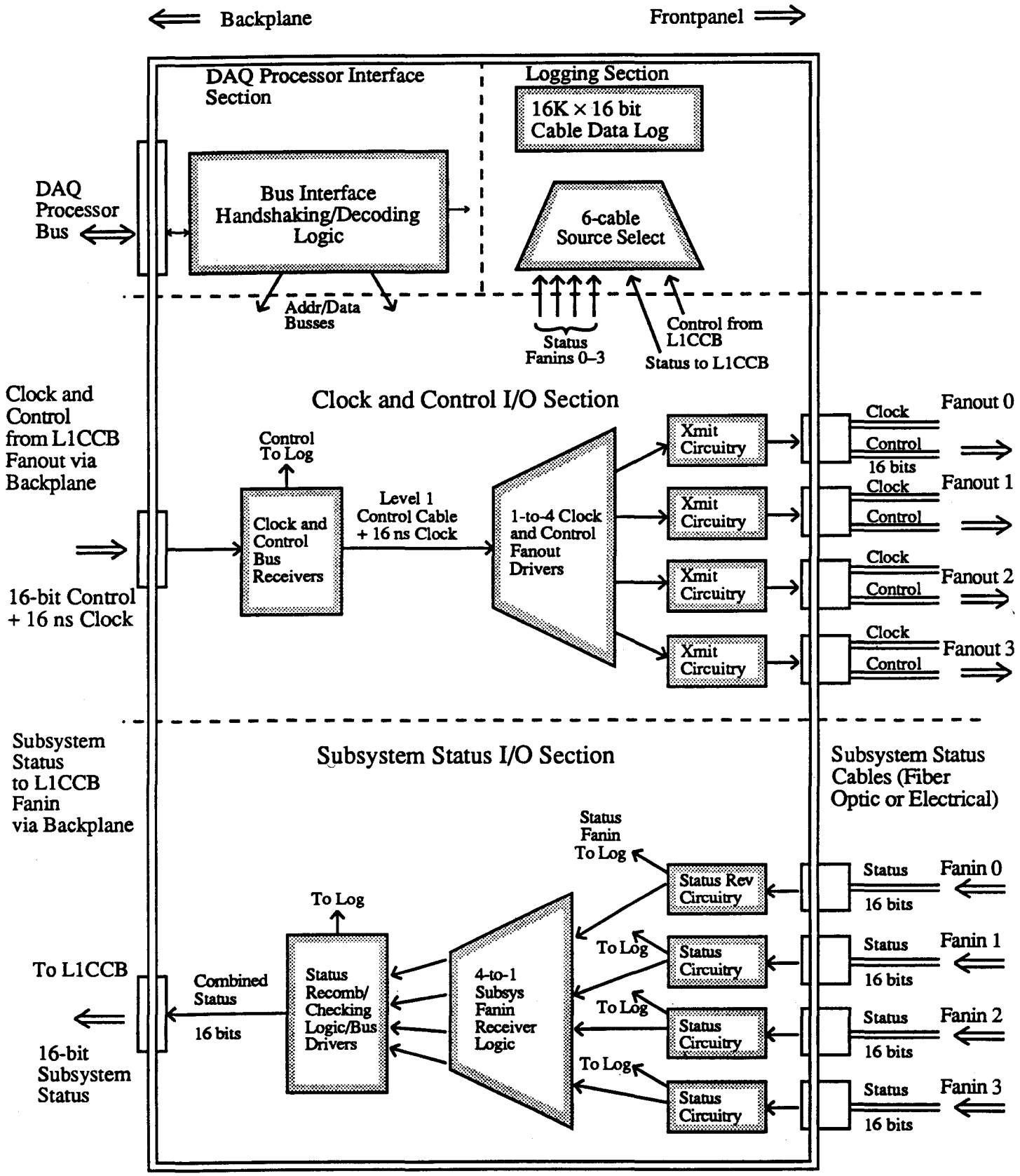


Figure 7

# Level 1 Simulation Module (LISM)

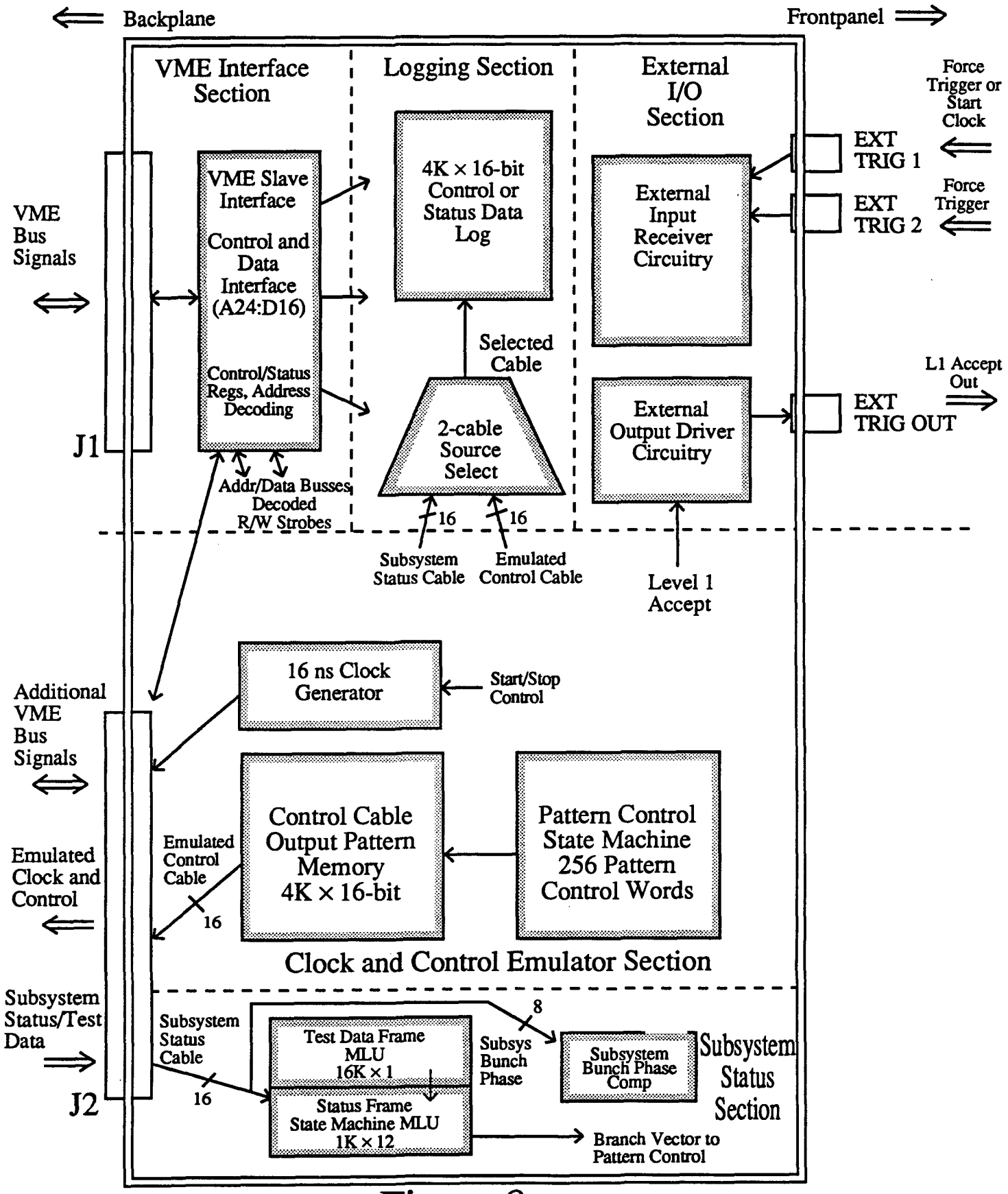


Figure 8