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SDC
SOLENOIDAL DETECTOR NOTES

SDC TRIGGER PRELIMINARY CONCEPTUAL DESIGN

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1. Introduction

1.1. Statement of the Problem

Triggering is one of the most daunting challenges facing a modern high luminosity colliding detector such as the SDC. At the nominal SSC design luminosity of 10^{33}, an average of 1.6 events occur at the beam crossing frequency of 16 nsec. This input rate of 10^8 interactions every second must be reduced by a factor of at least 10^5 to 1 KHz, the maximum rate that can be analyzed by an online computer farm. The physical size of the SDC detector imposes constraints on signal propagation that combine with electronics technology to require more than 2 μsec for any primary decision to discard data from a particular beam crossing. The high speed of trigger decisions coupled with the volume of data produced by the unprecedented high channel counts of the SDC creates a series of technological and systems problems that surpass those previously faced by high energy physics detectors. The possibility of an increase in SSC luminosity to 10^{34}, with the accompanying order-of-magnitude increase in pileup and channel occupancy, adds to the difficulty in developing solutions. Physics at the SSC is not possible without a trigger system that operates in this environment. Inasmuch as the design of the SDC detector trigger system impacts the design of the detector, the SDC detector cannot be designed without addressing how it is triggered.

1.2. Purpose of this Document

The overall goal of this document is to present a preliminary conceptual design of the SDC trigger system as an "existence proof". This includes a summary of the trigger requirements, overall architecture and dataflow, design of the level 1 and 2 trigger systems, technology of data transmission, design of clock and control systems, timing of trigger decisions, and cost information. Much of the detailed information about these aspects of the SDC trigger system is contained in supporting documents. This document summarizes the contents of these supporting documents and serves as a guide as to where the more detailed information is discussed.

1.3. Trigger Philosophy

The key to triggering the SDC involves tracking, calorimetry and muon systems as well as the correlation of information from these systems. As described below, the Level 1 pipeline data storage time is less than 4 μsec. Since signal propagation delays are included in this pipeline time, the Level 1 trigger calculations must be done in many cases under 1 μsec. In addition, the Level 1 Trigger system must be able to accept a new event every 16 nsec.

The general philosophy behind the SDC level 1 trigger system is to make local decisions about the presence of objects such as photons, electrons, muons, and jets, as well as global sums of E_T and missing E_T, and use the global compilation of this information to decide whether to keep (i.e. trigger on) a particular 16 nsec beam crossing. Each of the objects, such as electrons, muons and jets, are required to pass a series of p_t or E_t thresholds, which are used in making the Level 1 Trigger Decision. More information on the general trigger philosophy is found in ref 6.

The identification of trigger objects often depends on correlations between different subsystems participating in the trigger decision. The identification of an electron involves correlating information from the tracking and calorimeter systems. Identification of an electron in the calorimeter requires detecting isolated electromagnetic energy. The first step is to find a calorimeter trigger tower with energy in the electromagnetic compartment and little or no energy in its hadronic compartment (i.e. typically $E_{HAC} < 0.1 * E_{EMC}$). Next the towers adjacent to this tower are checked for having little or no energy in both electromagnetic and hadronic compartments. This establishes electromagnetic energy that is transversely and longitudinally isolated. However, since the size of the calorimeter trigger towers (nominally .1 x .1) is coarse, this isolation determination is improved with information from the shower max detector. Since a photon would also deposit the same pattern in the calorimeter, but would not deposit in the tracking system, the tracking system is used to distinguish between a photon and electron.

The identification of trigger objects in Level 1 must be completed within the constraints of the pipeline time and architecture. This means that correlations between some subsystems are more naturally made in the Level 2 trigger system. Since the muon trigger information is the last to arrive, processing of this information must be limited to avoid exceeding the trigger pipeline time. Therefore, while sufficient information to correlate the tracking and muon systems is available in Level 1, the correlation is done in Level 2 by reading out information stored in the Level 1 system. This is used to sharpen the muon p_t cut, which results in an important reduction in rate due to the steeply falling muon momentum spectrum.

Some of the information needed for trigger decisions is not available on the timescale of the Level 1 trigger decision. This information is then used in Level 2. An example is information from the silicon inner tracker, which provides track information in both the central and intermediate regions. The silicon tracker second level pattern recognition[7] should be sensitive to photon conversions, which form one of the largest background to inclusive electron triggers. The second level trigger correlates information from the silicon and outer tracker to reduce the electron rate by rejecting conversions. It also uses the silicon (along with the outer tracker as mentioned above) in correlation with the muon system to sharpen the muon p_t cut.

1.4. Requirements

The trigger system must be able to trigger efficiently on these processes:

1. Electrons from inclusive W's
2. Muons from inclusive W's
3. Jets at high p_t
4. High p_t photons
5. Missing E_t
6. Low p_t Multileptons (for B physics)

The benchmark for processes 1 and 2 is 50% efficiency for W's which enter the fiducial volume and would not be rejected by offline cuts. In other words, the trigger should get 50% of the W's it could in theory trigger on. The jet and photon p_t in processes 3 and 4 must be set such that there is a 1-2 decade overlap in jet and photon p_t data from other experiments (for example, CDF). The 50% efficiency is almost entirely due to the kinematic cut on lepton p_t. These requirements are set up to provide standards by which the trigger system performance can be assessed. They have been selected in the belief that this level of performance will provide high trigger efficiency for Higgs, $t-$quark, new Z', and other new phenomena, This is because the criteria listed here are established for moderate p_t single inclusive production, whereas the physics for which high efficiency is desired will feature pairs of leptons or jets or they will feature high p_t leptons or jets. These criteria are discussed in detail in Ref. 6.

1.5. Dataflow

The SDC dataflow diagram is shown in Fig. 1. The trigger and data acquisition systems have three levels. At the first level all information about the event is preserved. The first level decision is made on a subset of the total information available for the events. The deadtime at the first level is negligible. The first level decision is made at a fixed time after the interaction occurred and a first level decision is issued every 16 nsec. If the first level trigger generates an accept, the event data is moved or assigned to a buffer for the second level decision. The timing of the Level 1 decision and the time required for data storage before a Level 1 Accept is discussed below in the section on pipeline length.

The second level is defined as the decision, or series of decisions that exist between the first and third levels and is based on a subset of the total event data. A substantial part of the data may still be stored in analog form at this point. While the total processing time of the second level on an individual event may vary between 10 and 50 μsec, the second level issues a decision on the average every 10 μsec. The combined rejection factor of the first and second levels is 10^5.

After the second level trigger accept all information is digitized and read out. Full event data will be required for the third level decision. The event rate into the third level trigger is to be between 100 and 1000 Hz. Level 3 is implemented as a processing farm that is designed to achieve a rejection factor of 100, writing 10 to 100 events/second to mass storage. The bandwidth of the data path to the third level farm is designed to accept up to 10K events/second.

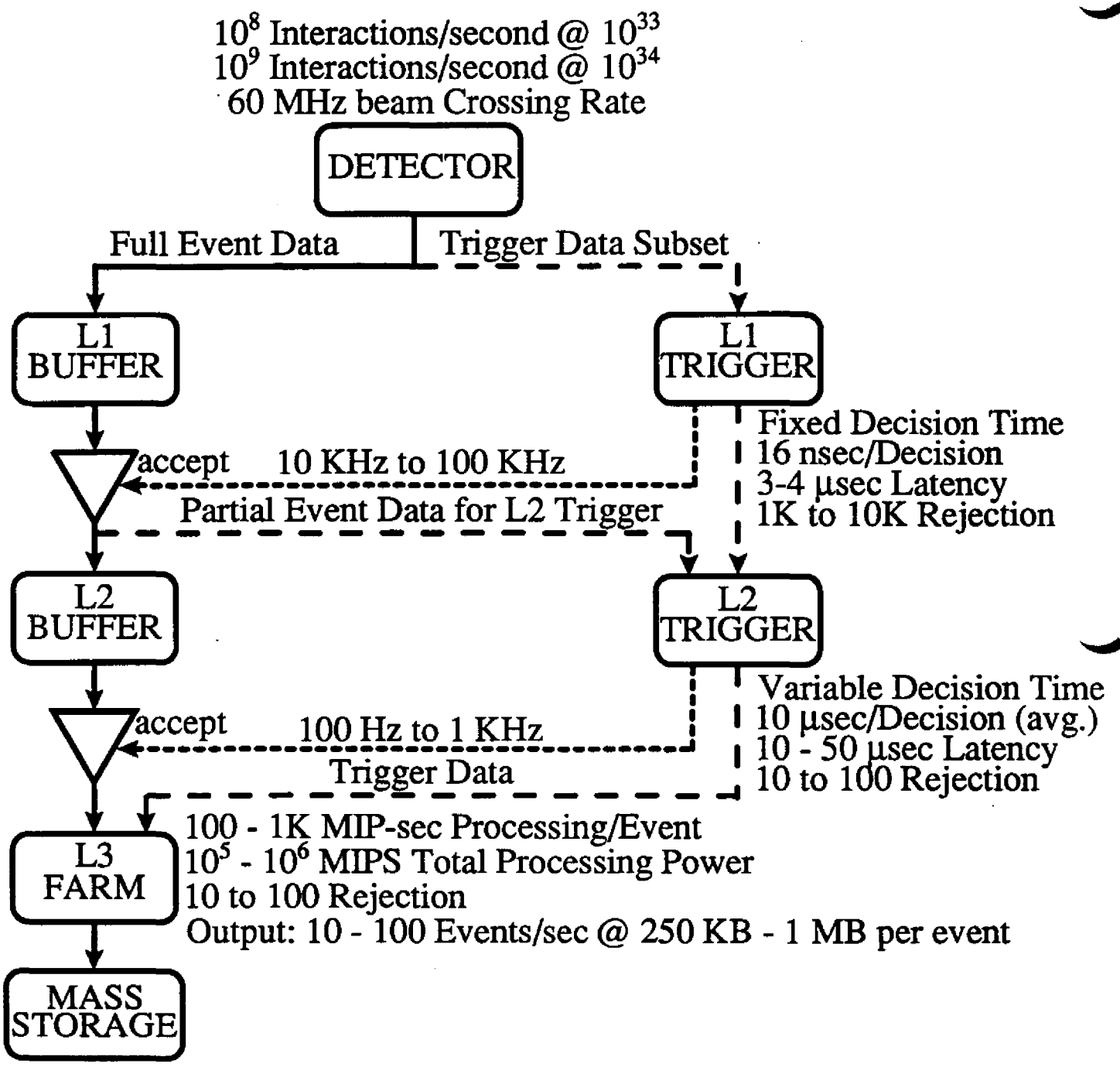

FIG. 1. Trigger and data acquisition dataflow for the SDC.

2. Level 1 Trigger

2.1. Introduction

The Level 1 Trigger finds electrons by searching for isolated electromagnetic energy in the calorimeter. It looks for .1 x .1 towers with energy in the electromagnetic compartment and little or no energy in the hadronic compartment surrounded by towers with little of no total energy. These isolated electron candidates are reported out on a .2 x .2 grid. In order to distinguish electrons from photons, correlation with the outer tracker is used. The shower max detector provides a local hit in .2 $\eta\times$ .00625 ϕ bins. The outer tracker provides tracks with p_t on a .00625 ϕ grid. The shower max is first correlated with the tracker to produce a coincidence hit with a p_t in .2 x .2 bins (after making the coincidence on a .00625 ϕ scale) for checking against the calorimeter in η, ϕ, and p_t. The photons are selected without the track match, but with a shower max match and a higher energy threshold. More details about these thresholds may be found in Refs. 2and 6.

The Level 1 Trigger finds jets by looking for .4 x .4 calorimeter towers over a series of thresholds. It finds muons by finding muon tracks over a series of muon p_t thresholds. The muon system is not correlated with the tracking system until Level 2. It must have a sharp enough p_t threshold to allow for a few kHz Level 1 rate while satisfying the trigger requirement above.

2.2. System Layout

Individual crates of the Level 1 Trigger logic are shown in Figure 2. The Front End Crates on the detector transmit their trigger information to the Level 1 Trigger off the detector on 1 Gbit/sec optical fibers. Every 16 nsec, each fiber carries 16 bits of data to the trigger system. The same type of optical fibers carry the clock and control communication from the trigger clock and control systems to the front end electronics systems. The Level 1 Trigger Crates transmit data between themselves on short runs of twist-and-flat pair cable. Each Level 1 Trigger Crate contains a Level 2 Trigger Interface card that gathers Level 1 information buffered in the Level 1 Trigger Input Cards and transmits this information to the Level 2 after a Level 1 Accept. Each Level 1 Trigger Crate also contains a processor board, of the standard variety provided by the DAQ. Its function is to download trigger tables, monitor trigger data and provide a data path to the event builder for trigger information to be supplied with the event record to be written to tape. Each Level 1 Trigger Crate also contains a Level 1 Clock/Control Board (L1CCB) that provides the 16 nsec clock and the other control functions described in the section about the interface to front end systems.

<u>Level 1 Decision</u>

The Level 1 Decision Logic is described in detail in 3. The calorimeter front end electronics crates transmit 8 bits of hadronic and electromagnetic compartment energy for each .1 x .1 trigger tower. The shower max detector transmits hits over threshold for 6.25 mrad ϕ by .2 η bins. The tracking detector transmits 4 p_t bits for tracks in 6.25 mrad ϕ bins. The muon system transmits 3 p_t bits for tracks in .2 ϕ by .25 η bins.

The calorimeter isolation/summation crates find isolated electrons by searching for towers with a small ratio of hadronic to electromagnetic compartment energy surrounded by quiet towers. They also sum up energy in .4 x .4 regions. These crates test the energy in the .4 x .4 towers against a series of 8 thresholds, as well as summing up the total E_t, E_x, and E_y energy found in the sum of .4 x .4 towers. The E_t, E_x, and E_y sums, as well

as the number of .4 x .4 towers over each threshold are sent to the calorimeter energy sum jet/threshold crates. The isolated electron information is transmitted to the calorimeter isolated electron matching crates These crates combine information on the boundaries of regions covered by the calorimeter isolation/summation crates to find isolated electrons on region edges. They also check the electron energy against 6 thresholds.

The shower max and tracking information is sent to the track/shower max match crates. These crates match the tracks and shower max hits on a 6.25 mrad ϕ scale. The η coordinate is found from the shower max hit η value with .2 bins. The p_t value is taken from the track p_t bits. The output is a series of shower max hits, some of which are matched with tracks carrying a p_t value, and all of which are on a 6.25 mrad ϕ and .2 η scale. These hits are sent the isolated electron/photon match crates. These crates match the shower max hits with the calorimeter isolated electrons. The shower match hits which have tracks attached also check the track p_t against the calorimeter tower energy threshold, as well as matching in η and ϕ. The result is a series of calorimeter-shower max matched isolated electromagnetic hits without track matches, which are considered "photons", and a second series of calorimeter-shower max hits with track matches, which are considered "electrons". Failures to find a shower max hit to match a calorimeter isolated electrons are also reported.

The muon system transmits the muon linked segments over several p_t thresholds to the Muon Level 1 Crates. These crates count the total number of muons over p_t and forward this information to the Level 1 decision crate. The calorimeter energy sum/jet threshold crates send the number of .4 x .4 towers over various thresholds as well as the total E_t, E_x, and E_y (the latter two are used to compute missing energy). The Level 1 Decision Crate then applies cuts on the energy sums and towers over threshold to form the trigger. The isolated electron/photon crates forward the number of isolated "electrons" and "photons" over various thresholds as described above. The Level 1 Decision crate then counts the total number over the thresholds to form the trigger. The Muon Level 1 crates forward the number of muons over several p_t thresholds to the Level 1 Decision crate which cuts on these to form muon triggers. The final trigger decision is converted to a Level 1 accept by the Global Clock/Control crate, which transmits the decision for fanout to the local clock/control crates and to the DAQ system.

Level 1 Clock & Control

The functionality of the clock and control crates is described in detail in the section on trigger interfaces, the section on communication between front end and trigger systems and in Ref. 5. The system consists of two basic crate types, the Global Clock and Control, and the Level 1 Distribution crates, which together distribute the crossing clock and control information to and receive status from all trigger and DAQ subsystem crates in the detector.

The Global Clock and Control crate uses the output from the Final Decision crate, along with machine clock and beam pickup information, plus operator control through the DAQ processor system to generate the root Clock and Control cable output. These signals are sent to up to 16 nearby Level 1 Distribution crates, which in turn can rebroadcast the Clock and Control cable signals to up to 64 subsystem crates each.

The Status cables from the subsystem crates to the Global Clock and Control crate follow the same path, in the reverse direction. Each Level 1 Distribution crate consolidates the status of up to 64 subsystem crates, and transmits that on a Status cable to the Global Clock and Control crate.

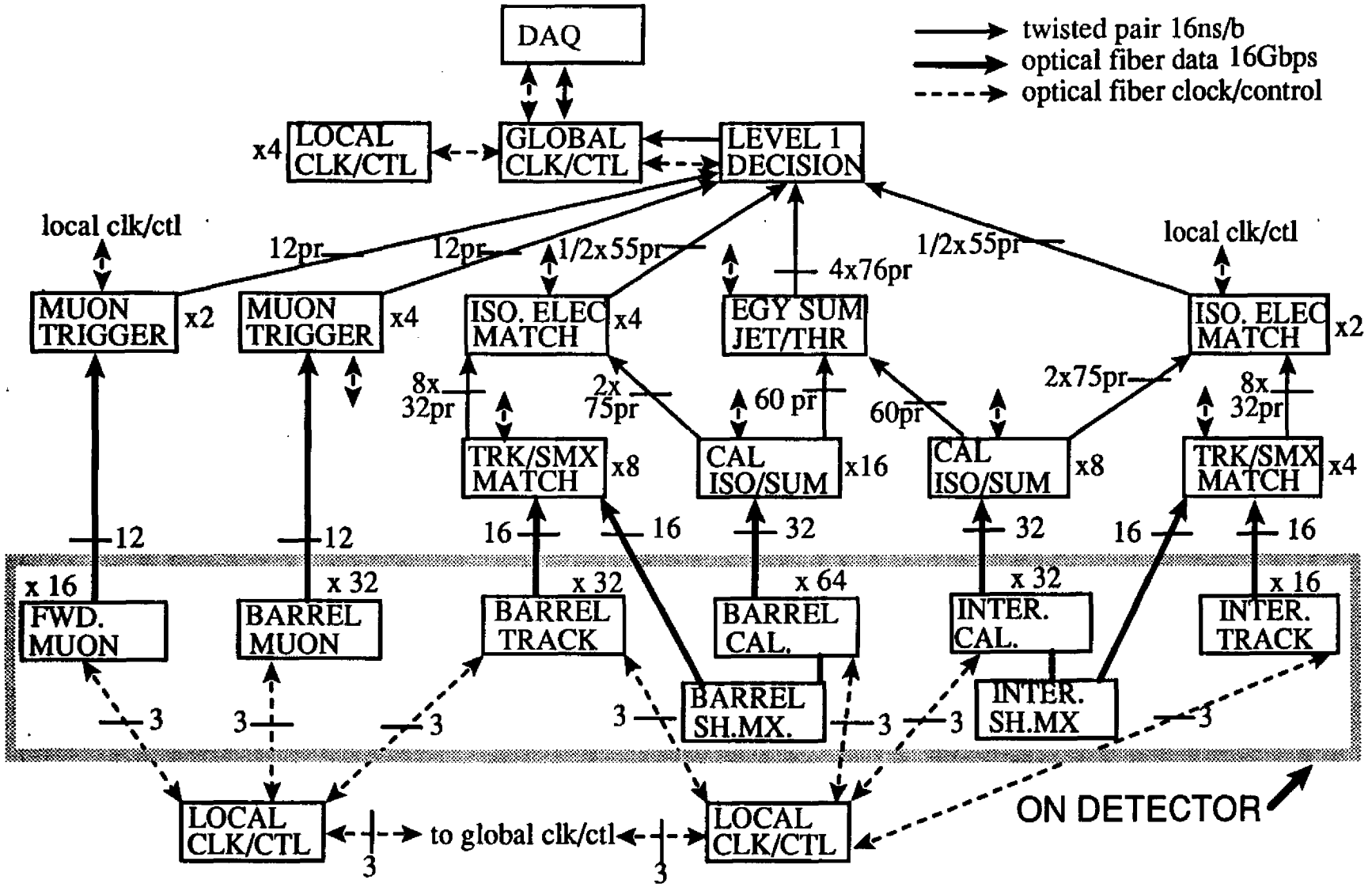

FIG. 2. Layout of Level 1 Trigger Crates.

The Global Clock and Control and Level 1 Distribution crates reside off the detector in the counting house. They are located physically near each other, and are connected via Clock, Control and Status cables driven electrically. The subsystem crates reside both on and off the detector. Those on the detector, such as front end DAQ subsystem crates, are connected to the Level 1 Distribution crates using fiber optic Clock, Control and Status cables. Those off the detector, such as Level 1 Decision crates, are driven using electrical cables.

2.3. Level 1 Trigger Crates

The functional descriptions of the crates in the level 1 system are presented below. More detailed descriptions of the individual boards in each of the crates, as well as the crates themselves are contained in Ref. 3.

Calorimeter Isolation/Summation

These crates find .1 x .1 calorimeter towers where $E_{em} \gg E_{had}$ surrounded by quiet towers. These isolated electron candidates are reported out on a grid of .2 x .2 towers. These crates also sum up the total E_t in .4 x .4 towers, as well as the total E_t, E_x and E_y in the crate. The total .4 x .4 tower sums are tested against 8 thresholds and the number passing each is calculated.

There are 24 of these crates: 16 for the barrel and 8 for the intermediate regions of the detector. Each barrel crate covers 1.6 η by 0.8 ϕ. It contains 8 Memory Lookup Boards (MLU) that each receive the hadronic and electromagnetic compartment energies from the .1 x .1 calorimeter tower sums. Details on the techniques of electronics that can integrate a PMT signal over 16 nsec with baseline restoration are found in Ref. 1. Each MLU board receives 16 optical fibers that contain 8 bits each of hadronic and electromagnetic energy in a .1 x .1 tower from the front end calorimeter crates. The MLU boards convert the input FADC tower sum values into E_t on a 12 bit linear scale, compute E_t sums in the .4 x .4 region of 16 trigger towers that each services (again on a 12 bit linear scale), and calculate an Encoded Tower Type (ETT) for each tower. This type is based on the amount of energy deposited in the hadronic and electromagnetic compartments. The ETT is 0 for a tower below any electromagnetic threshold, ETT 1 through 6 indicate an electron candidate exceeding one of 6 thresholds, and 7 indicates a hadron.

Each crate also contains 2 Pattern Recognition ASIC boards (PRA), which receive the ETT bits from 4 MLU's, corresponding to a region .8 x .8. These boards perform the search for isolated electron candidates in .2 x .2 regions that are contained or on the edge (partial) of the .8 x .8 region. The result is a series of isolated electron flags, one for each .2 x .2 region that are composed of 3 bits each with 0 meaning "quiet", 1-6 meaning an isolated electron above thresholds 1-6, and 7 meaning neither quiet nor an isolated electron. There are 25 regions x 3 bits of flag = 75 bits of isolated electron information from each PRA that are transmitted to the Isolated Electron Match Crate. Of these 25 regions, 9 are contained and 16 are partial regions that need further combination with other partial regions from other Calorimeter Isolation/Summation crates to find isolated electrons. The design details of the MLU and PRA cards, along with simulation results on the performance of this isolated electron pattern logic are found in Ref. 2.

Each crate also contains a double width Energy Card. This card covers a 1.6 η by 0.8 ϕ region and receives the energy sums in .4 x .4 regions from 8 MLU's on a 12 bit scale. In addition to computing the total E_t in the .8 x .8 region, it also converts the .4 x .4 E_t sums into E_x and E_y sums and adds these up to produce the total E_x and E_y in the

.8 x .8 region as well. The Energy Card also tests the E_t in each .4 x .4 tower against 8 thresholds and calculates the number of .4 x .4 towers above each threshold. Three bits of number above threshold are shipped for each of the 8 thresholds (24 bits total), along with 12 bits of E_t, E_x, and E_y (36 bits total) to the Energy Sum Jet/Threshold Crate.

Each crate also includes a Level 2 Interface Card (L2IC). After a Level 1 Accept each of the 8 MLU cards sends its stored tower electromagnetic and hadronic 8-bit FADC values over an individual differential pair on the backplane at 1 bit/16 nsec to the L2IC for subsequent transmission to the Level 2 processor. The simultaneous transmission of the 16 towers of information from each MLU takes 2.56 μsec.

Each crate also contains a Level 1 Clock/Control Board Card and a DAQ Interface/-Processor Board.

Track/Shower Max Match

These crates correlate the outer tracker hits with the shower max hits on a .00625 ϕ scale. The shower max is used to assign the track an η coordinate on a .2 scale. The p_t from the tracker is used to place the track on a 3-bit p_t scale used to match against the calorimeter E_t.

There are 12 of these crates: 8 for the barrel and 4 for the intermediate regions of the detector. Each barrel crate covers 1.6 η by 1.6 ϕ. It contains 8 double-width Track/Shower Max Hit Cards (TSMHC), each handling 1.6 η by 0.2 ϕ. The TSMHC cards each receive 16 Shower Max fiber optic cables that each cover 0.2 η by 0.1 ϕ with 16 ϕ bits at $\Delta\phi =$ 6.25 mrad apiece. They also receive 8 Tracker fiber optic cables that each cover 1.6 η by 0.025 ϕ with 4 ϕ bins of $\Delta\phi = 6.25$ mrad with 4 bits of p_t apiece for the case of the fiber tracker and fewer bits of p_t for the case of the straw tube tracker[9]. The TSMHC matches the Shower Max and Track hits on a scale of $\Delta\phi = 6.25$ mrad. These hits are assigned an η value from the Shower Max and a p_t value from the track. Since the Calorimeter electrons are on a 3-bit scale, the p_t value is calculated on the same 3-bit scale. Since the calorimeter electrons are assigned to .2 x .2 regions, the output is placed in .2 x .2 bins where each bin is characterized by a four bit code. The first 3 bits are the p_t value. The fourth bit indicates whether there was a Shower Max hit. If this is zero, there has been no shower max match and the track is placed in 8 .2 x .2 bins covering the η range from 0 to 1.6, using the highest p_t track in the $\delta\phi = .2$ region. If this is one, the 3-bit track p_t code is placed in the .2 η bin given by the shower max. The TSMHC output consists of 8 four-bit codes (32 bits) giving the track p_t and shower max hit information for a .8 η by .4 ϕ region in 8 .2 x .2 sections. This information is transmitted to the Isolated ELectron Matching Crates on 16 16-pair cables, two from each TSMHC, that each cover a .8 η by .2 ϕ region and all together cover the 1.6 η by 1.6 ϕ region.

Each crate also includes a Level 2 Interface Card (L2IC). After a Level 1 Accept each of the 8 TSMHC sends its stored shower max hits (8 η bins of 32 ϕ bits apiece = 256 bits) and track information (32 ϕ bins with 4 bits p_t = 128 bits) over an individual differential pair on the backplane at 1 bit/16 nsec to the L2IC for subsequent transmission to the Level 2 processor. The transmission of the information takes 4.22 μsec.

Each crate also contains a Level 1 Clock/Control Board and a DAQ Interface/-Processor Board.

Isolated Electron Match

These crates match up the shower max - outer tracker hits and the calorimeter isolated electron candidates on a .2 x .2 grid. The results are counted up in categories of track

(including shower max) and calorimeter agreement on p_t, disagreement on p_t, and shower max match only with the calorimeter (photon). For each category, the total number of matches above each of 6 E_t thresholds is accumulated. Failures to match shower max and calorimeter are also counted.

There are 6 of these crates: 4 for the barrel and 2 for the intermediate regions of the detector. Each barrel crate covers 1.6 η by 3.2 ϕ. It contains 8 Region Match Cards (RMC), each handling 0.8 η by 0.8 ϕ. The RMC receive 75 bits from 4 different PRA cards with 25 regions giving 3 bits of isolated electron flags apiece. The RMC matches up the partial regions to complete the isolated electron pattern search. The RMC also receives 4 cables from different TSHMC that bring 4 .8 η by .2 ϕ regions with 4 .2 x .2 bins with 3 bits of track p_t and 1 bit of shower max match information to cover the .8 x .8 RMC region. The PRA and TSHMC data for each .2 x .2 region are compared for matching an isolated electron in the calorimeter with a shower max hit and a track passing the appropriate P_T threshold. The output at the front panel from these RMC's is a 3-bit count of the number of coincident calorimeter - track - shower max matches above each of 6 thresholds where there was agreement between calorimeter and track energy, plus the number of coincident matches without p_t agreement are placed above the threshold of the calorimeter value, plus the number of calorimeter - shower max matches without a track match, and finally a single bit that indicates a failure to match calorimeter and shower max information. The total information from each RMC is 55 bits and is transmitted over individual lines to the Hit Summary Card.

Each crate has 3 double-width Hit Summary Cards (HSC). The HSC is the building block for hit sums. At the lowest level, the HSC's receive data from 4 RMC's. At the higher levels additional HSC's receive and combine data from 4 HSC's at lower levels. Each half of the first two HSC's in the crate receive the match data described above from 2 RMC's (110 bits per half HSC) covering a region 1.6 η by 0.8 ϕ, so that the two HSC's cover a 1.6 η by 3.2 ϕ region. The HSC's sum up their input data and output this data to half of a third HSC, which is resident in half of the Isolated Electron Match Crates. The other half of the HSC receives input data from the two HSC's in another Isolated Electron Match Crate. The resulting data from the third HSC then covers a 3.2 η by 3.2 ϕ region. This data is then sent to a third HSC that resides in the Electron Match Crate that sent the data from its first two HSC's to another Electron Match Crate. The first half of this HSC then sums up the HSC data from it and the pair of Electron Match Crates to cover the 3.2 η by 6.4 ϕ barrel region. The second half performs a similar sum to cover the intermediate region. The resulting data is a 3-bit count of the number of coincident calorimeter - track - shower max matches above each of 6 thresholds where there was agreement between calorimeter and track energy, plus the number of coincident matches without p_t agreement placed above the threshold of the calorimeter value, plus the number of calorimeter - shower max matches without a track match, and finally a bit that indicates a failure to match calorimeter and shower max information. The total information from the third HSC is 55 bits and is transmitted over twisted pair cable to the Electron Match Card in the Final Decision Crate.

Each crate also contains a Level 1 Clock/Control Board and a DAQ Interface/-Processor Board.

Energy Sum/Jet Threshold

This crate continues the global E_t, E_x, and E_y sums as well as adding up the number of .4 x .4 calorimeter towers above a series of 8 thresholds.

There is one Energy Sum/Jet Threshold crate, which covers both the barrel and the intermediate regions of the detector. It contains 4 double-width Energy Sum Cards (ESC), each handling 1.6 η by 6.4 ϕ, which receive the 12-bit E_t, E_x, and E_y sums from 8 Energy Cards (each covering a region 1.6 η x .8ϕ) in 4 Calorimeter Isolation/Summation Crates. The output consists of 12-bit E_t, E_x, and E_y sums, covering 1.6 η by 6.4 ϕ, which are transmitted over a 36-pair cable to the Total Energy Summation Module in the Final Decision Crate.

This Crate also contains 4 double-width Jet Threshold Sum Cards (JTSC), each handling 1.6 η by 6.4 ϕ, which receive the 3-bit numbers of .4 x .4 towers over 8 thresholds from 8 Energy Cards (each covering a region 1.6 η x .8ϕ) in 4 Calorimeter Isolation/Summation Crates, and sums these numbers into a series of 5-bit numbers of .4 x .4 towers over 8 thresholds. These 40 bits, covering, covering 1.6 η by 6.4 ϕ, are transmitted to the Total Jet Threshold Card in the Final Decision Crate.

Each crate also contains a Level 1 Clock/Control Board and a DAQ Interface/-Processor Board.

Muon Trigger Crates

These crates count up the number of muon tracks passing each of 4 programmable p_t thresholds. They also store 3 bits of p_t and the track location with a resolution of $\Delta\phi = .01, \Delta\eta = .05$ for use by the second level trigger.

There are 6 Muon Trigger Crates. There are 4 barrel crates that cover all of ϕ and cover $|\eta| < 2.5$ in four equal sections. In addition, there are two forward muon trigger crates, one for each end. Each Muon Trigger Crate services 8 Muon Regional Front End Crates. There are 32 Muon Regional Front End Crates in the barrel ($|\eta| < 2.5$) and 8 for each forward endcap. Each regional front end crate services an octant in ϕ over its η range. In the barrel region, this represents 1/4 of an octant (divided along η). The muon trigger relies on a scintillator signal in coincidence confirmed by a projective chamber wire pair. The trigger units are derived from the scintillator segmentation. As detailed in Ref. 4, there are two options for the scintillator layers. In the first there are two layers of scintillators that are arranged in slats sectioned to provide 32 divisions in ϕ and 156 divisions in θ. The θ divisions are composed of 96 units in the barrel region and 30 units in each of the end regions. In the second, there is one layer of scintillators, where the θ segmentation is no longer restricted by a momentum selection constraint and the differential timing of the two phototubes on each scintillator is used to enhance the ϕ binning from 32 to 128. Each barrel regional muon crate covers a region $1.2\eta \times 0.8\phi$ with 24 η bins and 4 ϕ bins (16 ϕ bins in option 2).

Each regional muon front end crate contains 14 cards, of which two are used for exchange of neighbor scintillator information, leaving 12 cards. Since isolated electrons are found in the calorimeter on a .2 x .2 grid, the muon η bins are combined into .2 η bins on each card. Therefore, each card covers a single η bins of .2 by a total ϕ range of .4, so that the 12 cards cover the $1.2\eta \times 0.8\phi$ area. This means that each card has either 2 ϕ bins (option 1) or 8 ϕ bins (option 2). In order to be compatible with either, 3 bits are needed for the value of ϕ for a track found by each card. Each track found by a card has 3 bits of p_t associated with it, corresponding to the full resolution of level 1 muon trigger system. Each card has a single 1 Gb/s optical fiber that carries the trigger information directly to a Muon Logic Card in the Muon Trigger Crates. Each card sends two tracks. Since the optical fiber bandwidth allows 8 bits per track, and the format described above uses 6 bits (3 bits of ϕ and 3 bits of p_t), an additional two bits per track are used to enhance

the ϕ resolution to 5 bits. This resolution is available since there are 15,360 barrel ϕ wires arranged in 4 η sections and 4 depth layers, giving 960 ϕ bins, distributed over cards that cover half of an octant in ϕ, or 60 bins.

Each of the 6 Muon Trigger Crates contains 8 Muon Logic Cards (MLC), each of which receives 12 optical fibers, one from each card in a single muon regional front end crate. Each optical fiber carries 3 bits of p_t and 5 bits of ϕ for the two highest p_t tracks in a .2 $\eta\times$ .4 ϕ region. This gives each MLC a coverage of 1.2 $\eta\times$ 0.8 ϕ, corresponding to one full muon regional crate. The 8 MLC's combine to give the Muon Trigger Crate coverage of a $\Delta\eta = 1.2$ slice for all ϕ.

The output of each of the MLC's is 4 2-bit numbers that indicates the number of muon tracks (none, 1, 2, 3 or more) above each of 4 programmable thresholds. Each Crate also contains a Muon Summation Module that accepts the 8 bits of tracks over thresholds from the MLC's and sums them to produce a series of 4 3-bit numbers that indicate the number of muon tracks above each of 4 programmable thresholds. These are then transmitted by a 12-pair cable to the Muon Decision Module in the Final Decision Crate.

Each crate also includes a Level 2 Interface Card (L2IC). After a Level 1 Accept each of the MLC's sends its stored 24 tracks with 3 bits p_t and 5 ϕ bits apiece, (total of 24 x 8 = 192 bits) over an individual differential pair on the backplane at 1 bit/16 nsec to the L2IC for subsequent transmission to the Level 2 processor. This transmission takes 3.1 μsec.

Each crate also contains a Level 1 Clock/Control Board and a DAQ Interface/-Processor Board.

Final Decision Crate

The Final Decision Crate sums up and makes cuts on calorimeter total and missing E_t (the latter from the individual E_x and E_y sums). It sums up the total number of calorimeter .4 x .4 regions over 8 thresholds and makes cuts on this. Is sums up the total number of isolated electron (and photon) candidates within the categories and p_t thresholds described above and makes cuts on these. It also sums up the total number of muons over the p_t thresholds and makes cuts on these. The resulting trigger decision is then forwarded to the clock and control logic.

There is one Final Decision Crate. It contains a final HSC, which accepts the 55 bits of information from two barrel and two intermediate crate HSC's. The information from this final HSC includes a 4-bit count of the number of coincident calorimeter - track - shower max matches above each of 6 thresholds where there was agreement between calorimeter and track energy, plus the number of coincident matches without p_t agreement placed above the threshold of the calorimeter value, plus the number of calorimeter - shower max matches without a track match, and finally a bit that indicates a failure to match calorimeter and shower max information. This information is sent to the Final Decision Memory Lookup Card (FDM) describes below.

The crate also contains one Energy Sum Card (ESC). This sums the 4 input 12-bit E_t, E_x, and E_y sums, which are transmitted over 36-pair cables from one of the Energy Sum/Jet Threshold Crate. the output of the ESC is also sent to the FDM.

The crate also contains one Total Jet Threshold Card which read in 4 40-pair cables carrying a series of 5-bit numbers of .4 x .4 towers over 8 thresholds for either an intermediate region or 1/2 of the barrel from the Energy Sum/Jet Threshold Crates.

The crate also contains a Final Muon Card that reads in a 3-bit number of muons

above a series of 4 thresholds from the 6 Muon Trigger Crates and forms a 3-bit trigger vector that is sent to the Final Decision Module.

The crate contains one Final Decision Module (FDM) card. This card has 4 separate memory lookup (MLU) architectures that on it, one each for total and missing transverse energy triggers, jet triggers, isolated electron triggers and muon triggers. Each of these MLU's produces a 3 bit code, yielding 4 3-bit codes that are sent to the Final Decision Logic Card (FDL). The energy sum MLU uses memory lookup to compute the total E_t, E_x, and E_y, uses the latter two to compute missing E_t, and then compares the total calorimeter global E_t and missing E_t sums against programmable thresholds to produce a 3-bit trigger vector that is sent to the Final Decision Logic. The jet trigger MLU compares the series of 5-bit numbers of .4 x .4 towers over 8 thresholds with a series of programmable trigger requirements to produce its 3-bit output trigger vector. The results from the electron match HSC are compared against a series of thresholds, such as one isolated electron over 20 GeV or two over 10 GeV to determine the isolated electron 3-bit output vector and a similar process is performed by the muon trigger MLU.

The Final Decision Logic (FDL) card receives this series of 4 3-bit output vectors from the Electron, Muon, Jet and Energy MLU's. The FDL contains another series of MLU's that make the final level 1 trigger decision based on programmable requirements on combinations and individual requirements on the 4 3-bit vectors. It gets its data from the FDM over the backplane. It also contains logic to prescale trigger according to downloaded factors, as well as logic to resolve triggers found in different crossings. The FDL card determines the Level 1 Decision based on physics information in the detector. If it is unable to resolve conflicting crossing information from 2 subsystems, it can issue a trigger that covers more than one crossing, along with an "ambiguity" bit to indicate the number of crossings involved. The FDL card decision is transmitted over a cable to the the Global Clock/Control Crate which turns this into a Level 1 Accept if the detector systems are able to read out the event (i.e. the DAQ is live and there are no extant errors that prevent functioning of the system).

This crate also contains a Level 1 Clock/Control Board and a DAQ Interface/-Processor Board.

Global Clock and Control Crate

There is one Global Clock/Control Crate in the detector. It contains a Machine Clock Interface Board to communicate with the interface to the accelerator RF clock. It has a Beam Pickup Interface to communicate with the beam pickup electronics. It contains a Deadtime Monitor Board that tracks the disposition of each crossing, i.e. whether accepted, rejected, or lost due to downtime of trigger and/or DAQ. There is a Level 1 Control Generator card that connects to the Final Decision Logic (FDL) card in the Final Decision Crate as well as the cards described above to generate the contents of the Control cable. This card also reconciles the returned subsystem status such that it will only transmit a Level 1 Accept if the DAQ is able to read out the event and there are no outstanding error conditions that prevent accepting the event (i.e. clock phase confusion, etc.) Finally, this crate contains one Level 1 Clock Control Board (L1CCB) and up to 4 Level 1 Clock Control Fanouts (L1CCF). The L1CCB is the basic interface card for all subsystem crates to the Level 1 Trigger. The L1CCF is used in conjunction with the L1CCB through a backplane interface to provide a fanout rebroadcast of the Clock and Control cables to crates throughout the detector, and to consolidate returned Status cable data from these same crates. Together, the L1CCB and L1CCF cards reside in the

Global Clock and Control for the purpose of distributing the Clock and Control to the layer of up to 16 Level 1 Distribution crates. There is a Global Clock Master that provides the phase lock of the 16 nsec clock and distributes the clock to Clock/Control Interface modules. There is a Global Control Master that distributes the Control signals to the Clock/Control Interface Modules. Finally, there are 2 Clock/Control Interface Modules that each communicate with 2 Local Clock/Control Crates. This crate also contains a DAQ Interface/Processor Board.

The Global Clock and Control crate distributes Clock and Control information and receives Status information from up to 16 Level 1 Distribution crates through electrical cable interconnections on the L1CCF cards in that crate. Each L1CCF card can drive Clock and Control information to and receive Status from up to 4 Level 1 Distribution crates through the frontpanel.

Level 1 Distribution Crate

There are 8 of these crates in the present design, with the exact number depending on the partitioning of the distribution system. Each crate contains one L1CCB and up to 16 L1CCF cards. Each Level 1 Distribution crate is connected to the Global Clock and Control crate by an electrical Clock, Control and Status cables through the L1CCB frontpanel. Each L1CCF card can drive up to 4 subsystem crates through electrical or fiber optic Clock, Control and Status cables connected on the frontpanel. The L1CCB communicates to the L1CCF cards through 4 identical fanout busses on the crate backplane. Each bus drives up to 4 L1CCF cards.

The crate also contains a DAQ Interface/Processor board. This processor is used to control and monitor the L1CCB and L1CCF cards in both normal and standalone operation.

2.4. Level 1 Trigger Physical Layout & Resource Requirements

The Level 1 Trigger System takes up 58 Crates. These will use 20 full-height racks with a power consumption of about 120 KW in the Counting House. There are approximately 5,000 optical fibers required to carry information from the detector to the Level 1 Trigger System.

2.5. Fiber Optic Transmission

A study of the SDC Trigger requirements by M. Thompson, *U. Wisconsin*, has some preliminary suggestions[11] for transmission of trigger information at 1 Gb/s on optical fibers:

1. Use signal optoelectronics with a frequency, above which a 3 dB loss of gain occurs, of 1.7 GHz to preserve the waveform of the worst case 1.125 Gbaud signal of ..010101010..
2. Use multimode fiber with a core diameter of about 60 microns to allow the use of the lowest cost optoelectronics.
3. Use words of 18 bits to carry both the 16 bits of information and two bits (a,b) with b=1-a. The (a,b) bits have the purposes of delineating words and allowing slight drifts and threshold shifts to be measured. The (a) bits are from a long fixed pseudo-random sequence which has a mean time for appearing in random data of 3.68×10^{60} years.
4. Allow the information in the words of each channel to be constant, all zeroes, all ones or change with no "forbidden values".

5. Use three adjustments for each signal:
   a) a Threshold Adjustment for each receiver,
   b) a Fine delay Adjustment with steps of 125 ps and
   c) a Coarse delay Adjustment with a range of ±14.2 ns.
6. We expect the high signal level to vary from signal to signal and to vary with time due to the use of low cost lasers and detectors and the use of imperfect optical connectors. The high signal levels and low signal levels are recorded by 2 diodes and 2 capacitors for each of the 5000 signals. The 2 voltages will be used to determine the threshold for each signal.
7. The Fine delay adjustment uses a tapped delay line with a 16:1 multiplexor and 3 fast decision circuits latching the signal just before the clock, at the clock and just after the clock. Signal transitions before and after the clock cause the charge on 2 corresponding capacitors to be incremented so that the difference of voltages on the 2 capacitors indicates the relative phase of the clock and signal transitions.
8. The Coarse delay Adjustment uses a 32 long shift register with a 32:1 multiplexor and uses 3 capacitors to collect the agreements of the signal's pattern of (a) bits with the expected pattern. During power-up or after timing errors are found, the 5-bit selection is changed until agreement of the signal and expected (a) bit patterns is found.
9. Use a multiplexing slow 8 bit or 10 bit ADC system with 128 inputs on each 9U board to read 8 analog levels produced by each of the 16 incoming Trigger Information signals. Similarly, use a multiplexing DAC to adjust the thresholds of the receiving circuits for each of the 16 signals on each 9U board.
10. Use an external computer with a 16 bit address, 16 bit data bus to sequentially and slowly monitor the status of the analog voltages produced by all 5000 signals. The computer makes changes when necessary to the Threshold, Fine and Coarse adjustments. This can both permit secure word and bit alignment during power up and recovery after major disturbances.

2.6. Level 1 Pipeline Length

The proposal for the level 1 pipeline is that its length will not be less than 3.0 μsec and not more than 4.0 μsec. Representatives from Silicon, Central Tracking, Calorimetry and Muon front end electronics systems were involved in this decision. The conclusion from these systems was that while all could manage 4.0 μsec, there were significant difficulties for some to go beyond 4.0 μsec. In addition, there would be significant, but not insurmountable, difficulties for the silicon system to reach a 4.0 μsec pipeline length for some architectures. The representatives of the Tracking, Calorimeter, Muon and Global trigger systems contributed to the calculations shown below that demonstrate the necessity for a range between 3.0 and 4.0 μsec. The actual calculation results in a range from 3.1 to 3.9 μsec. The pipeline length is determined by the muon drift time. The overall uncertainty in cable paths and electronics locations expands the range by 0.1 μsec on each side. However, it is important to add that the calculation is based on locating the central trigger decision and distribution in the counting house on the surface. If the trigger is located in the gallery, then the reduction in cable length of 40.7 m each way translates into a 0.4 μsec or 26 crossing savings.

<u>Calculation of Level 1 Pipeline Length</u>

The following table sums up the time for the trigger data from an interaction to reach

the trigger logic and proceed through this logic to the final decision for the Level 1 Accept. The particular system chosen is the muon system, since it takes the longest and varies between 50 and 100 crossings depending on whether the muon drift time is 800 to 1600 nsec, respectively.

Muon through Global:	
Propagation to Chamber	2
Drift in Chamber	50–100
Propagation along Wire	2
Segment Finder	2
Segment Linker	6
Transmission to LEVEL 1	50
LEVEL 1 Calculation	20
Total	**132–182**

The following table sums up the delay incurred in transmitting the Level 1 Accept signal from the Global Level 1 Logic back to the front end electronics storage pipelines.

Cause of Delay	Time (crossings)
LEVEL 1→pipeline controller (nearby)	1
Pipeline setup & synchronization	2
Pipeline Controller→Pipeline Fanout (far)	50
Local Fanout to Pipeline	10
Phase between pipeline and sample	±0.5
Pipeline overhead in sample select	1
Particle interaction→pipeline front	−5
Presamples	6
Signal shaping for sample of rise	−1
Total	**64**

The total pipeline length is the sum of the propagation of the trigger signals through the trigger logic to the final Level 1 Accept, which is 132 to 182 crossings for the muon system, and the propagation of the Level 1 Accept back to the front end pipelines, which is calculated to be 64 crossings. The resulting total crossings ranges between 196 and 246,

or between 3.1 and 3.9 μsec. This is the range of possible Level 1 pipeline lengths, where the lower figure corresponds to a muon drift of 800 nsec and the larger a drift of 1.6 μsec.

2.7. Trigger Interfaces

Global Level 1 Processor

The Global Level 1 Trigger Processor is the device that collects the Level 1 Trigger data from the subsystems, distributes the Level 1 Accept and 16 nsec clock signals to all subsystems, and controls the overall operation of the Level 1 subsystems.

The Global Level 1 Processor (GL1P) receives a subset of the data from subsystems participating in the level 1 trigger. The data for each 16 nsec bunch crossing is sent by each subsystem every 16 nsec. The GL1P not only makes the final level 1 decision, but it also controls the start of any level 1 readout, disables this readout, and distributes scheduling signals for tests and calibrations. Therefore, all subsystems, even those not involved in the level 1 decision, must communicate with the GL1P.

All level 1 trigger and DAQ pipelines in the subsystems and the GL1P must be driven with a common clock synchronized to the SSC crossing frequency. This clock is distributed centrally through the GL1P. The processing of the GL1P decision is driven by this cycle.

The Global Level 1 Processor (GL1P) receives a subset of the data from subsystems participating in the level 1 trigger. The data for each 16 nsec bunch crossing is sent by each subsystem every 16 nsec and arrives at the input of the GL1P before 112 - 162 crossings have elapsed since the event occurred. The GL1P issues a Level 1 Trigger Accept/Reject at its output 132-182 bunch crossings after the event occurred. The timing is discussed in detail in ref 5. The GL1P not only makes the final level 1 decision, but it also controls the start of any level 1 readout, disables this readout, and distributes scheduling signals for tests and calibrations. Therefore, all subsystems, even those not involved in the level 1 decision, must communicate with the GL1P.

All level 1 trigger and DAQ pipelines in the subsystems and the GL1P must be driven with a common clock synchronized to the SSC crossing frequency. This clock is distributed centrally through the GL1P. This clock is phase locked to the the SSC machine clock and has a 16 nsec cycle. The clock is high for 8 ± 1 nsec and low for 8 ± 1 nsec. The processing of the GL1P decision is driven by this cycle. For testing purposes, the GL1P operates on its own internal clock which can be varied in frequency from 70 MHz to 1 KHz.

Subsystems ship trigger data to the GL1P every 16 nsec. All of the data relevant to one crossing is shipped in one 16 nsec time period. All subsystems must send their data to the GL1P so that it arrives at the GL1P input within 1.8 - 2.6 μsec after the crossing occurred at the interaction point. Subsystems should send trigger data as soon as it is available and not delay sending trigger data for the purposes of synchronization. The subsystems must send data continuously even if they are being read out.

The GL1P receives the trigger data and aligns this data in time for all the subsystems since the arrival time for the data of a particular crossing is different among the different subsystems. The particular bunch crossing number of a subsystem's data is indicated by a local bunch counter, named Bunch Phase. The Bunch Phase is used to check the alignment of the trigger data from each subsystem. The subsystem also counts Level 1 triggers. This number, Level 1 ID, is used to check that the data read out corresponds to the correct Level 1 Accept.

Level 1 Accept/Reject

After the GL1P processing, a decision is made to issue a Level 1 Accept or Reject for

each bunch crossing. The GL1P sends the Level 1 Accept/Reject to all subsystems 132 - 182 crossings after the bunch crossing. This signal appears at the output of the GL1P. The Level 1 Accept/Reject arrives at the subsystem after additional delay due to the propagation of the Level 1 Accept/Reject from the GL1P. The Level 1 Accept/Reject signal is also accompanied by additional GL1P data. This data is not necessarily propagated to all components of a subsystem, but is used as a diagnostic by the central processing of a subsystem. The data includes data valid, the Bunch Phase, the Level 1 ID, and several bits of "readout type". The Level 1 ID counts Level 1 Accepts. The bits of "readout type" allow information to be sent to subsystems that may react differently to different trigger types.

Ambiguous and Overlapping Triggers

If a subsystem cannot identify data with a particular crossing, it sends the same data applicable to a number of crossings with each crossing. Since most triggers rely on a coincidence of components, the result will still be to select a single crossing for every L1 Accept. Subsystems determine the number of bunch crossings to store upon each Level 1 Accept. The present design does not allow back-to-back Level 1 Accepts. There is the possibility that we cannot uniquely identify a crossing from the trigger data or that we may have two Level 1 Accepts within the measurement time span of some subsystems. Following Dorenbosch, Botlo, Fry and Milner (SSCL-348), we define the Level 1 Accept as a level that is high for all clock cycles to be measured. The Level 1 ID is incremented on the rising edge of the Level 1 Accept. To attempt to limit overlaps as much as possible, we also follow their rules for minimal spacing for Level 1 Accepts:

1. No more than 1 Level 1 Accept per 80 nsec.
2. No more than 2 Level 1 Accepts per 260 nsec.
3. No more than 3 Level 1 Accepts per 1 μsec.
4. No more than 4 Level 1 Accepts per 4 μsec.

They determine that the total cost for these rules is less than 1% at a Level 1 rate of 100 KHz and 11.5% at 500 KHz.

Trigger Control

Subsystems send trigger control information to the GL1P. This includes a busy bit to indicate that the subsystem trigger did not process the event, busy bit to indicate that the subsystem DAQ cannot read out the event, a fatal error bit to indicate that the subsystem trigger has had a fatal error and a trigger data error to indicate that the subsystem trigger data may be corrupt. An example of a trigger busy would be a reset process that had not been completed. We must allow for subsystems that cannot complete a Level 1 Reset sequence in a single 16 nsec crossing. The trigger busy bit prevents a Level 1 Accept being issued to a subsystem that must use several crossings for a reset. An example of a fatal error would be a disagreement between the Level 1 trigger number counted by the subsystem and the number sent by the GL1P. An example of a trigger data error would be either a parity check failure or another type of internal data checking failure. The control information also includes the subsystem's crossing number associated with this data. All subsystems active during a run must send this control information to the GL1P, whether or not they send data used in the Level 1 decision.

Tests

The operation and scheduling of tests during a run are controlled by the GL1P. A schedule of all tests to be run is downloaded to the GL1P before the beginning of a run by

the Central DAQ Control (CDAQC). The CDAQC also can modify this schedule during a run in response to changing detector status. The GL1P sends to all subsystems a Test Enable signal, with the type of test to be run indicated in the Test Trigger Type bits, a fixed number of crossings before the crossing when the test is to be done. This enables subsystems to prepare for the test. The tests are arranged in such a way as to allow many subsystems to do tests simultaneously. The subsystems set up their tests so that the test data will be contained in the exact crossing indicated by the GL1P Test Enable Signal. The GL1P inhibits normal triggers a fixed time before the test trigger crossing so that there will be no interference. The GL1P then sends out a Level 1 Accept for the appropriate crossing to read in the test data. This Accept is accompanied by a bit in the Readout Type set to indicate that it is a test trigger.

Functional Layout

The functional block diagram of the GL1P as it interacts with a subsystem trigger is shown in Figure 3. The Clock Distribution block generates the 16 nsec clock and associated data such as the Bunch Crossing 0 and Empty Bunch Indicators from SSC accelerator clock information. It then distributes this information to the subsystems and the rest of the GL1P. This block also monitors the relative phase of the accelerator clock and the beam pickup signal, which should remain constant. The Control Interface provides all of the control signals to the subsystems and reads all of the control signals from the subsystems. All data except for the trigger data from a subsystem is brought through the Control Interface. The test scheduling and Level 1 Accept are sent to the subsystem through this block. It also monitors the subsystem deadtime and status. The trigger data from the subsystems is processed in the Trigger Logic block. Here the data from the various regions of each subsystem are collected, counted, and placed in an appropriate format for correlation with other subsystem trigger data. This data is shipped to the Trigger Decision Block, which contains the final logic to determine the Level 1 Accept. This logic also uses the output from the Control Interface to determine if the detector is able to accept the trigger and, if necessary, to determine the correct crossing to issue the trigger.

Clock and Control Subsystem Interface

Each subsystem crate in the detector is linked to the Level 1 Clock and Control system through 3 basic connections as represented by the following 3 logical cable types: the Clock, Control, and Status cables. The Clock cable distributes the 16ns crossing clock to the subsystem crate, the Control cable distributes Level 1 trigger information, and the Status cable returns Level 1 status information from the subsystem crate to the Clock and Control system. The Control and Status cables are required to carry a 16-bit Control or Status word for each 16ns crossing, thus having a data rate of 1 Gb/s.

The actual physical implementation of these cable links may take a number of forms. For example, for long distance runs, between front end subsystem crates on the detector and off-detector Clock and Control distribution crates, each of these cables could be an optical fiber, with the Clock cable transmitting a pure 16ns clock, and the Control and Status cables running at a serial rate of 1 Gb/s. For shorter runs between distribution and subsystem crates that are physically close together, conventional twisted-pair electrical cables could be used, with the Control and Status cables requiring each 16 pairs, and the Clock becoming possibly the 17th pair on the Control cable.

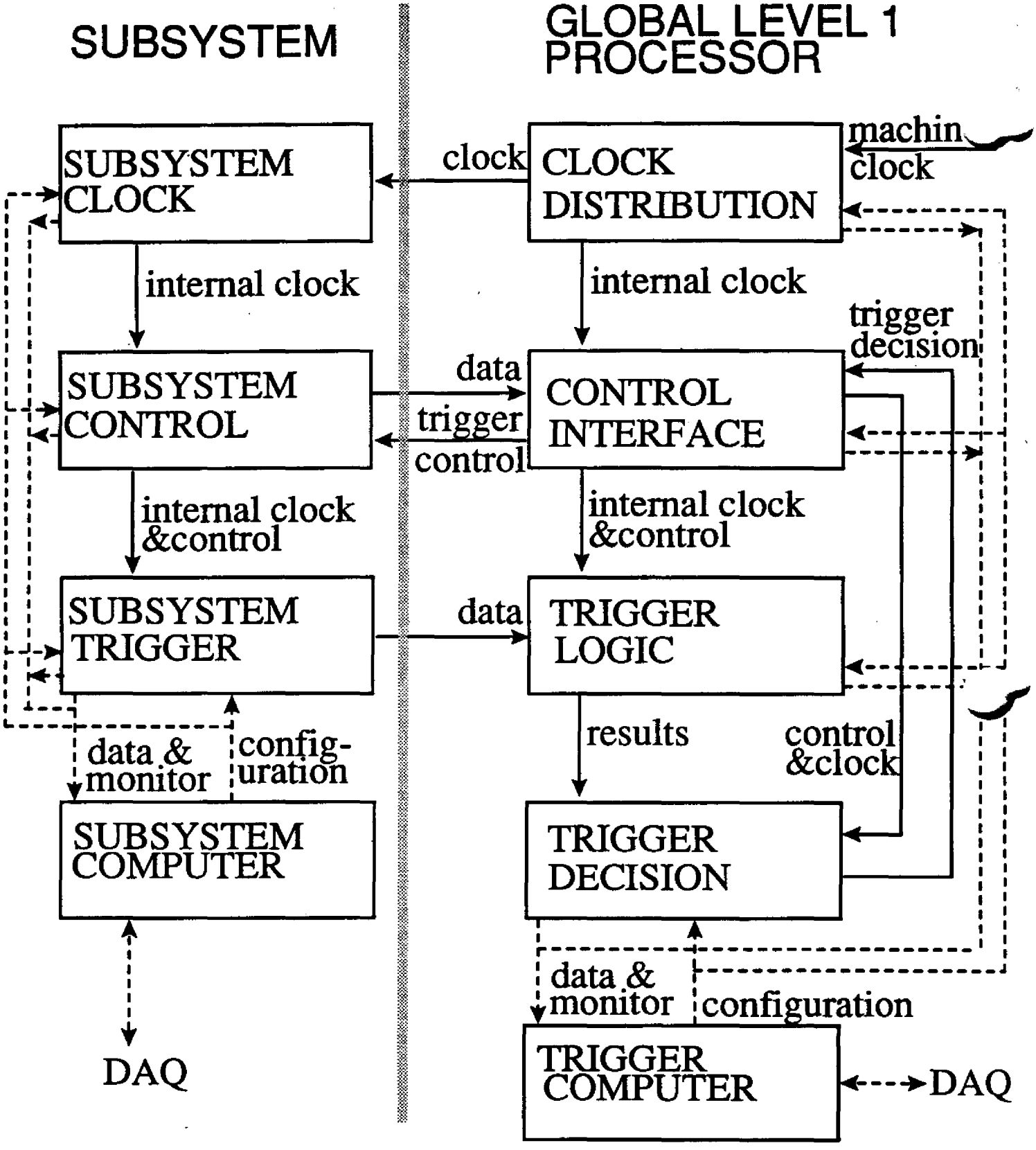

FIG. 3. Layout of the Global Level 1 Processor and Interface to Front End Systems.

3. Level 2 Trigger

3.1. Introduction

The Level 2 Trigger is used to reject conversions by matching silicon tracking information with outer tracker information and calorimeter isolated electrons. The silicon tracking is also used to find secondary vertices in jets, rejecting events which have relatively low-p_t jets that passed the Level 1, and lack secondary vertices as well as any other distinguishing features. The Level 2 Trigger also uses the full shower max information to improve the electron isolation cut. The Level 2 Trigger matches tracks in the muon system with those in the tracking system to sharpen the p_t cut.

The Level 2 decision is supposed to achieve a rejection factor of between 10 and 100 in a series of pipelined steps, each of which does not exceed 10 μsec in duration and the sum of which may vary between 10 and 50 μsec in latency. On average the Level 2 issues a decision every 10 μsec. The Level 2 decision uses flexible and programmable algorithms. The basic event selection is done by jet and lepton identification and geometrical or topological correlation[8].

3.2. Level 2 Subsystems

Silicon Tracking

The Silicon Tracking Level 2 Trigger is described in detail in Ref. 7, which is summarized here. The Silicon tracker first attempts to recognise regions of interest by means of a "coarse scan". Having established areas of the two-dimensional space likely to contain high p_T tracks, it performs a second,"fine scan", in which these areas are examined with the full granularity of the silicon detector. This allows a high precision measurement of the transverse momentum of those tracks found by the pattern recognition.

In the coarse scan the data from the barrel region is tabulated in 1920 bins in ϕ, which corresponds to a distance of 0.6 mm on the circumference of the innermost silicon detector. This bin size is chosen to approximately match the ϕ granularity of the calorimeter and to keep the number of inputs to the processors to a manageable number while maintaining good resolution in transverse momentum. A two dimensional table is formed by combining these 1920 bins from 8 layers of the silicon ordered by increasing radius. In this table high transverse momentum tracks have a very small or zero variation in ϕ bin as a function of radius whereas low p_T tracks bend considerably as they pass through the eight silicon layers. The trigger processors are designed to recognize the patterns of tracks with a p_t greater than 15 GeV/c. An almost identical approach is used for the end-cap modules of the silicon detector, except that rather than filling a table of ϕ versus radius of the silicon layer, it constructs a table of ϕ against z. The same granularity in ϕ is used as for the barrel. Again, high transverse momentum tracks have a small variation in ϕ as z changes, whereas low p_T tracks curve considerably. The pattern recognition problem is therefore exactly analogous to that in the barrel once the z versus ϕ table has been constructed, so that identical trigger processors can be used.

In both the barrel and end cap modules there is a further subdivision of the data in bins of pseudorapidity η. These bins correspond in the barrel to the length of silicon wafers bonded together to form a readout unit. This is either two or three wafers. This η subdivision is somewhat coarser than that of the calorimeter, but should still allow satisfactory matching of tracking information and energy deposition.

Data from the silicon tracker in the form of a list of hit strip numbers is multiplexed from the detector to the trigger processors cards in the counting house on about 1000 optical fibers. The output of the processors will be fed to the global level 2 trigger processor, which will combine the silicon trigger data with that from other second level triggers and/or with first level data if the component in question does not contribute to the second level. An interface card in each trigger processor crate will collect the trigger processor card outputs and forward them to the global level 2 system.

Tracking, Shower Max, and Calorimetry

The information for use in Level 2 from these system is described in detail in the section on Level 1 and is summarized here. The Calorimeter Level 1 Crates send their stored 8-bit electromagnetic and hadronic energy sums for the .1 x .1 trigger towers forward to the global level 2 processor after a level 1 accept. The Track/Shower Max Crates send stored shower max hits (8 η bins of 32 ϕ bits apiece = 256 bits) and track information (32 ϕ bins with 4 bits p_t = 128 bits) in 64 1.6 $\eta \times 0.2\phi$ regions to the second level trigger. This gives an η granularity of 1.6 for the tracker and 0.2 for the shower max, as well as a ϕ granularity of 6.25 mrad for both.

Muons

As described in the section on Level 1, the Muon Trigger Crates send the two highest p_t tracks per .2 $\eta \times .4\phi$ region with 3 bits p_t and 5 ϕ bits apiece, (giving ϕ bins of .01) to the Level 2 Processor.

As described in Ref. 4, additional information from the muon system can also be used in the Level 2 decision. The θ wires in the layer inside the toroid reduce the uncertainty from the spread in the beam spot, resulting in a $\sqrt{2}$ improvement in the p_t cutoff sharpness. The information from the inner θ wires is sent up and combined with the signals from the outer layers and the result is sent to the Level 2 Processor. The muon hits can be combined with stiff tracks in the central tracker. This allows use of the p_t information from the central tracker. Due to field nonuniformities, improvement on momentum resolution beyond 10% depends on use of z information. While the muon system does provide z information, the association of a muon system θ track with a tracking system ϕ track requires significant processing that is appropriate for Level 2. Finally, the muon hit in the ϕ wires can be combined with the stiff track in the central tracker. Here the scintillator ϕ information tags the hit and provides θ information, which can be used to improve the "sagitta" measurement, and correct for variations with z. This requires processing that is appropriate for Level 2.

3.3. Level 2 Global Processor

As described in Ref. 8, the Level 2 Processor, makes a refined tracking selection based on the η, ϕ, and p_t information in the silicon, central tracker and muon systems. The shower max information is used in combination with the electromagnetic and hadronic calorimeter information to refine the isolation and E_t determination for electrons and photons. More sophisticated cluster algorithms are used to verify the E_t of jets. The silicon tracker is used to search for secondary vertices. These calculations can be performed with such devices as Digital Signal Processors, Transputers, or Massively Parallel Processors such as the Associative String Processor.

4. Cost

4.1. Methodology

The cost for the trigger system was calculated by determining the numbers of ASIC's, boards, crates, and cables. Each electronics board was costed at 2 K$, with 1.2 K$ for parts, .4 K$ for the board, and .4 K$ for assembly. This cost is based on vendor quotes for manufacture and assembly of 270 9U x 400 mm deep 42 MHz VME Trigger Boards built for the Zeus experiment. The quotes are attached as Appendix B. The cost for the SDC boards is increased somewhat to account for stricter impedance control necessary at anticipated speeds in the range 63 - 125 MHz. Each crate was costed at 10 K$, with 2.5 K$ for hardware, 2.5 K$ for power supplies, and 5 K$ for the crate processor. Fiber optic links were costed at $ 300 per link with 35% contingency.

ASIC's and boards were divided into "easy", "average" and "hard" categories. Easy designs were estimated to take 1 man-year (MY) of engineering time. Average designs were estimated to take 2 MY and hard designs were estimated to take 3 MY of engineering time. In addition, each MY of engineering time was assumed to also use a MY of technician time, as well as 12.5 K$ of expenses for travel, supplies and computing (i.e. CAD).

Interfaces

There are a number of boundaries in the cost responsibilites between the trigger and front end electronics systems. These have been established in joint consultation with front end electronics groups. For central and muon tracking systems, the segment finding is costed with the front end electronics and the segment linking and all that follows is costed with the trigger. For calorimetry, the front end electronics costs all generation of the 8-bit hadronic and electromagnetic sums and the trigger pays for the optical link to bring the data up to the counting house. For the boundary between Level 1 and Level 2, Level 1 pays for the transmission of the data to the Level 2 Interface card (including crate and backplane), while Level 2 pays for the card. For the boundary between DAQ and trigger, the trigger pays for its crate and processor cards, while the DAQ pays for all the links that connect to the processor cards.

4.2. Summary

The following table lists the costs following the methodology and interfaces described in the previous two sections. The detailed cost breakdown is contained in Ref. 10.

Item	Cost (K$)	Conting (K$)	Total (K$)
Level 1:	17,772	6,082	23,854
Track	4,466	1,567	6,034
Calorimeter	4,871	1,583	6,455
Muon	3,892	1,407	5,299
Silicon	128	37	165
Global	2,148	721	2,869
Level 2:	6,429	1,864	8,294
Track	315	91	406
Calorimeter	435	126	561
Muon	255	74	329
Silicon	2,819	818	3,637
Global	2,605	756	3,360
Proj. Manag.	552	160	712
Total	24,753	8,107	32,861

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