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AN SSC PHOTOMULTIPLIER TUBE PREAMPLIFIER CIRCUIT

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An SSC Photomultiplier Tube Preamplifier Circuit

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Abstract

This study presents the design of the front end amplifier for a scintillator calorimeter with photomultiplier tube (PMT) readout. The design is based on analytical computations and SPICE simulations, and is checked against tests performed on a prototyped circuit. We were looking to achieve (1) a very low droop within the 4 ns after the integration of the photomultiplier tube (PMT) signal was completed, (2) a very low noise figure for the whole amplifier in a 100 MHz bandwidth, (3) an input impedance optimized for the PMT which is actually used, (4) baseline restoration as quick as possible at the output of the clip amps, (5) no loss of information due to the saturation at intermediary stages (e.g. integrator), and (6) an output driving 100 Ω twisted pair cables, or 50 Ω coaxial cables, in order to transmit the signal to switched capacitor arrays for analog storage.

I. Introduction

The calorimeter for an SSC detector requires good energy resolution, fast time response, fine segmentation, and a high degree of hermeticity [4]. The requirements are such that at a luminosity of 10^{33} there are 1.6 minimum bias events per beamcrossing (every 16 ns) due to 10^8 interactions/sec. The maximal signal of any calorimeter electronic channel is set at 5 TeV and the minimal signal of interest is determined to be 30 MeV. Thus the dynamic range of this section should be $20 \cdot \log \frac{5\ \text{TeV}}{30\ \text{MeV}} = 104$ dB. The reader is referred to [2], [11], [14], and [21], for more explanation regarding the energy bounds. The front end electronics has to be able to process the PMT output signal which has a minimum 16 ns duration and 104 dB dynamic range. For energies of 5 TeV and 30 MeV the output current of the PMT is 50 mA and 300 nA respectively. During the time required to make a trigger decision (< 4 μs) the signal has to be stored in an analog memory at a sampling period of 16 ns.. It was found, [10], that much of the electronics development for other type of systems, [13], was inappropriate for the very fast signals with a very high dynamic range from a scintillator calorimeter. Indeed, as presented in [3], and [8], new equipment and devices have to be used. A comparison between the performance of ZEUS calorimeter at HERA, [13], and the calorimeter for an SSC detector is given in table I. For ZEUS the minimum ionizing energy is 300 MeV in the electro-magnetic compartment, but for calibration purposes this is required to be in channel 100 and that implies a minimum level of 3 MeV. For an SSC calorimeter a larger bandwidth of the front-end amplifier and a better accuracy of the signal sampling are required. The circuit has to have also a very good noise performance in order to be able to accurately process the low energy signals too. Figure 1 presents the block diagram of the front end circuit which satisfies the general requirements derived above. In order to achieve the desired dynamic range and noise

performance the most feasible solution is to split the signal into a high gain path and a low gain path. The ratio between the gains of these paths is chosen to be equal to 32. The PMT output current is conditioned by the current amplifiers, shown as (1) and (2) in fig. 1, and is integrated by the fast and low noise integrators (3) and (4).

Table I.
Comparison between significant parameters of the calorimeters for the ZEUS detector at HERA and for an SSC detector

Parameter	Calorimeter of ZEUS detector at HERA	Calorimeter for SSC detector
Minimal energy	3 MeV	30 MeV
Maximal energy	400 GeV	5 TeV
Minimal PMT output current	75 μA	300 nA
Maximal PMT output current	100 mA	50 mA
Dynamic range	102 dB	104 dB
Interval between beam collisions	96 ns	16 ns
Sampling frequency in the pipeline	96 ns	16 ns

The gain of the integration is set in accordance with the overall gain of the two paths. After the integration is completed the baseline of the signal is restored in order to avoid the loss of information. This might occur if a high energy crossing is immediately followed by a very low energy one, and subsequently one of the circuit components is close to the saturation point,

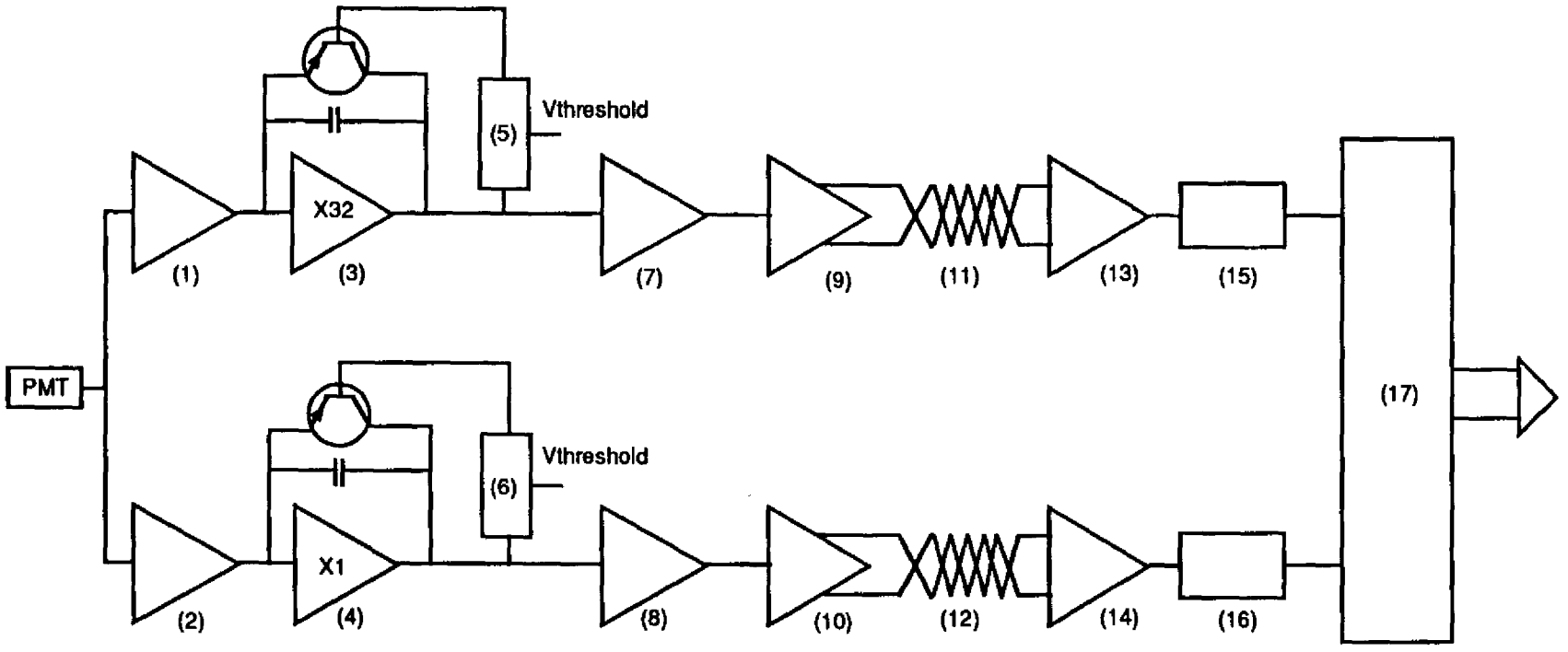


Fig. 1 The block diagram of the front end circuit

where non-linearities are likely to appear. Using passive delay lines, clip amps, shown as (7) and (8) in fig. 1, restore the baseline, and transmit the signal to the cable driver stages (9) and (10). The cables, shown as (11) and (12) in fig. 1, are connected to the line receivers (13) and(14) which serve as buffers for the switched capacitor arrays (15) and (16). The switched capacitor arrays (SCA) are read out after a trigger decision and digitized with a 12-bit ADC in the digital block, shown as (17) in fig. 1. Storage of the data is performed on the SCA card until the trigger determines that data should be read out. A detailed SCA presentation is provided by Kleinfelder et al., [18]. The primary function of the SCA card is to receive, process, and digitize the signal from 256 analog channels. It is physically composed of 16 SCA integrated circuits, each of them having 16 input and output channels. The SCA integrated circuit can sample and store the level of analog inputs at a 62 MHz rate. It can simultaneously store and retrieve analog samples from the different cells.To avoid large time jitter error, the integrated signal variation during the sampling process has to be less then 1 LSB within a 4 ns period after the integration is completed. This also means that the droop of signal at the output of the baseline restoration circuit has to be less than 1 LSB over a period of 4 ns after the integration is completed. Under certain conditions the accomplishment of this task can bring the integrators into saturation. Thus the integrators have to be protected against the loss of information in the vicinity of the saturation point by protection circuits, shown as (5) and (6) in fig. 1, which restore the baseline at the output of the integrators just before they can saturate. The functions of the digital block tare described in [15], and [16].

The goal of this study is to design the input amplifier which comprises the current amplifiers (1) and (2), the low noise and fast integrators (3) and (4), the protection against saturation circuits (5) and (6), the clip amps (7) and (8) and the cable drivers (9) and (10). The design is based on analytical computations and PSPICE simulations [19]. It is also checked

against tests performed on the real circuit. We were looking to achieve (1) a very low droop within the 4 ns after the integration of the PMT signal was completed, (2) a very low noise figure for the whole amplifier in a 100 MHz bandwidth, (3) an input impedance optimized for the PMT which is actually used, (4) baseline restoration as quick as possible at the output of the clip amps, (5) no loss of information owing to the saturation at intermediary stages (e.g. integrator), and (6) an output driving 100 Ω twisted pair cables, or 50 Ω coaxial cables, in order to transmit the signal to the switched capacitor arrays.

II. The Design of the Input Amplifier

We consider the input amplifier to be connected to a PMT which has fast time response and low background noise, thus being suitable for high energy physics applications. Reference [20] describes the features of the Hamamatsu R580-15 photomultiplier tube used for these applications. According to [5], and [12] the signal supplied by the PMT has exponentially shaped edges, being close to a triangle, thus within our SPICE simulations we used a piecewise linear signal which had a triangular shape. The falling and rising times were chosen to be 6 ns and 10 ns, respectively, adding to form a 16 ns overall duration pulse. The maximal output current, corresponding to 5 TeV for this tube is 50 mA while the minimal level, corresponding to 30 MeV, is 300 nA. In order to have proper raising and falling times at the PMT output, when the front end input amplifier is connected, a low input impedance for this stage is desired. A low value for this impedance also implies less additional noise in the input circuit, thus a better noise performance for the equipment. According to these requirements we chose the input impedance equal to 50 Ω.

A. The current amplifiers

Because the PMT output current is split between the high and low gain paths, the actual level of the lowest current which has to be integrated by the high gain path is lower than 300 nA. In order to avoid a too low SNR at the output of the integrator for this case, we chose to boost the PMT current before it is integrated. The current amplifiers, shown as (1) and (2) in fig. 1, are designed for this task. There are three main requirements which have to be satisfied by these two stages: (a) the overall input impedance has to be ≈ 50 Ω, (b) a proper ratio between the currents going into the low gain path and into high gain path has to be provided, and (c) their current gain has to be chosen such that taking into account the gain of the next stages, the output range of the front end amplifier needs to equal ± 2.5 V. The diagram of the current amplifiers used for these purposes is given in fig. 2. The transistors Q1 and Q2 make up the inverting current amplifier, while the feedback coefficient is mainly given by R4 and R6. R5 is used to fix the operating point of the circuit, and the diodes D1, D2 limit its gain if the input current exceeds $\approx \frac{2 \cdot V_D}{R4}$. The input impedance, as it is proved below, is mainly given by R1. The capacitors C2 and C3 compensate the transistors frequency characteristics, in order to avoid oscillations or underdamped responses. The circuit has a series-shunt type of feedback, thus the gain of the amplifier without feedback is (considering the hybrid parameters model for the transistors):

$$G_I = -\frac{(1+h_{21e2}) \cdot R2 \cdot h_{21e1}}{R1+(1+h_{21e2}) \cdot (R4 \| R5 \| R6)} \cdot \frac{R4+R5 \| R6}{R4+R5 \| R6+h_{11e1}} \tag{1}$$

The feedback coefficient, β_i, is given by (2):

$$\beta_i = -\frac{R5 \| R6}{R4+R5 \| R6} \tag{2}$$

Thus the circuit current gain with feedback is:

$$G_{ir} = \frac{I_{e2}}{I_{in}} = \frac{G_I}{1+\beta_i \cdot G_I} \tag{3}$$

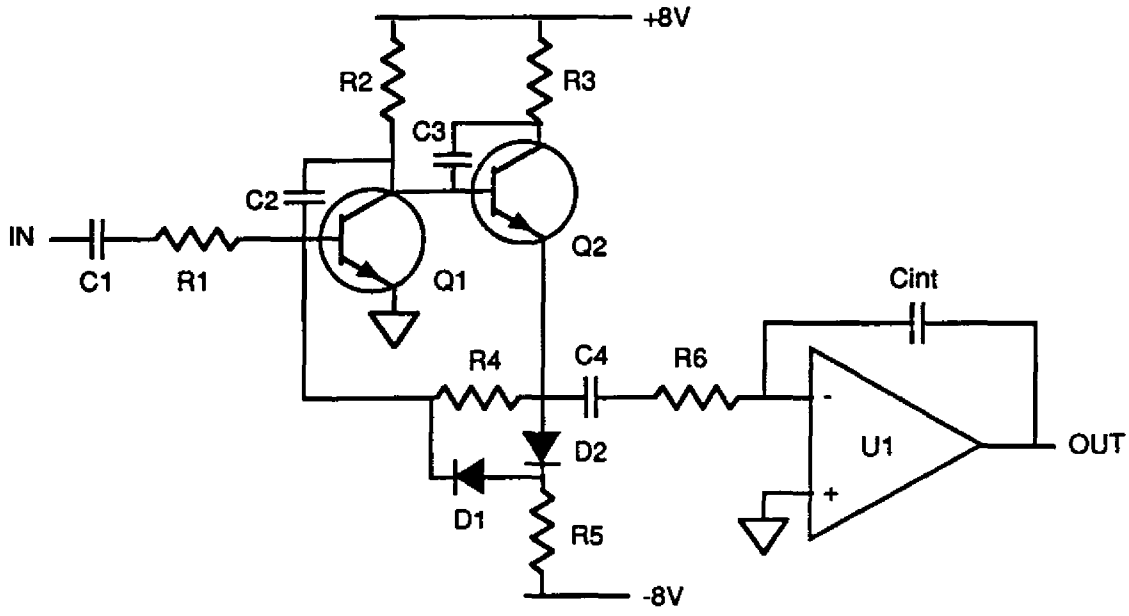


Fig. 2 The input current amplifier

This gain has to be adjusted in order to determine how much of the Q2 emitter current , I_{e2} ,goes through R6 into the integrator. Because the impedance in the base of Q1 is very low, owing to the current feedback, the current gain is adjusted by:

$$k = \frac{I_{out}}{I_{e2}} = \frac{R5 \| R4}{R6 + R5 \| R4} \tag{4}$$

Hence the actual current gain is:

$$G = G_{ir} \cdot k \tag{5}$$

The impedance in the base of Q1 may be computed as:

$$Z'_{in} = \frac{(R4 + R5 \| R6) \| h_{11e1}}{1 + \beta_i \cdot G_I} \tag{6}$$

The circuit input impedance is:

$$Z_{in} = R1 + Z'_{in} \tag{7}$$

In the calculations presented above the capacitors were considered to be large enough to be neglected. Choosing the operating collector currents for the transistors to be ≈1.5 mA for Q1 and ≈2 mA for Q2, and taking into account that the voltage developed across R2 is ≈8V-2·0.6V = 6.8V, and across R5 is ≈8V, we obtain R2 = 5.1 KΩ and R5 = 3.9 KΩ. We selected R4 and R6 to be as low as possible. Therefore, it is reasonable to assume that R5»R6 and R5»R4, which implies R5||R6 ≈ R6 and R5||R4 ≈ R4. In order to have a reasonable SNR at the output of the integrator for the lowest PMT output current, taking into account that the estimated integrator output noise voltage is ≈ 0.2 mV $_{rms}$, we chose the ratio between the current through the high gain path and the current through the low gain path to be ≈ 5.5, and the gain of the current amplifiers equal to 3. Thus we obtain R4 = 330 Ω and R6 ≈100 Ω (for these values and an infinite G_I we would have a gain of 3.3). The transistors employed were BFR 92, for which $h_{21e} \approx 20$, yielding $h_{11e} = h_{21e}\frac{V_T}{I_C} = 390\ \Omega$, $G_I = -167$, $\beta_i = -0.23$, k = 0.77 and G ≈ 3.2, according to the above formulas. The simulations by SPICE indicated a gain of 2.7, where the difference is due to neglecting the frequency characteristic of the transistors in the analytical computations above. Substituting the above values into eq. (6) we obtain $Z'_{in} \approx 5\ \Omega$, giving $Z_{in} \approx R1$. Therefore, the input impedance of the whole circuit (considering both high and low gain paths) will be approximately $R_{1H}||R_{1L}$ (the parallel combination of the input impedances of the two paths). This means that $R_{1H}||R_{1L} \approx 50\ \Omega$, and we have $\frac{R_{1L}}{R_{1H}} \approx 5.5$ (as it was found above). We conclude that $R_{1H} = 56\ \Omega$ and $R_{1L} = 330\ \Omega$. The resulting input impedance (considering Z'_{in}) is ≈ 51 Ω. In order to avoid phase shift between channels, the input time constants should be equal, $C_{1H}\cdot R_{1H} = C_{1L}\cdot R_{1L}$, which means C_{1H} = 100 nF , and C_{1L} = 18 nF. The diodes D1 and D2 are MBAL 99 ultra-fast switching diodes and they limit the gain and the output swing of the current amplifier, to avoid the hard saturation of the high gain path during large PMT pulses. These diodes are not used in the low gain path, and they limit the high gain when the PMT

output current exceeds 4 mA.

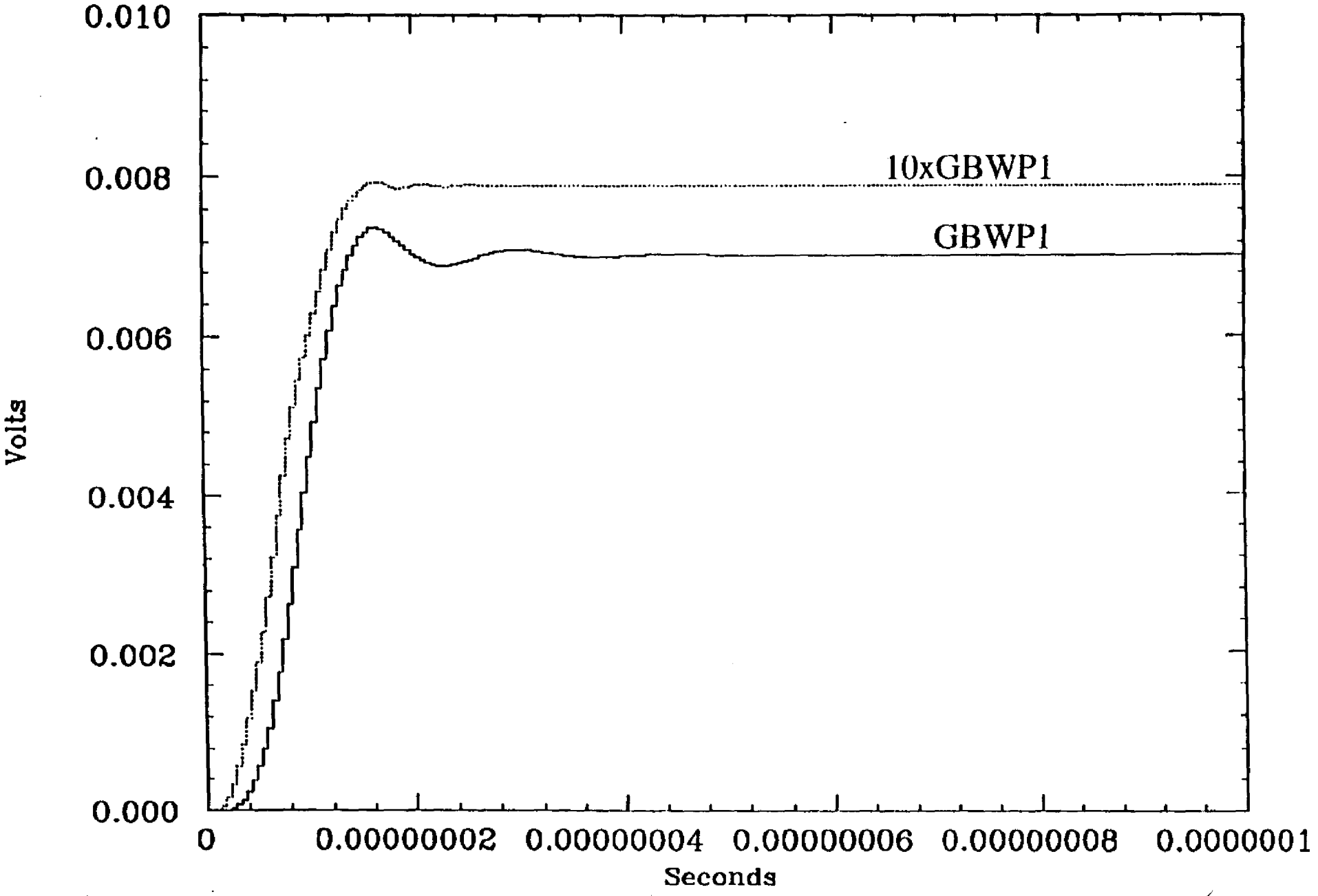
B.The fast, low noise integrator

We considered several alternatives for the design of the fast, low noise integrator: a customized IC, a hybrid circuit, and the use of high speed, low noise commercial available op-amps. It turned that the simplest solution was to employ high speed, and low noise op-amps, which also yielded better performance. We found that if the gain-bandwidth product (GBWP) of the op-amp was not high enough, an overshoot occurred at the end of the integration. In order to account more exactly for this requirement on the op-amp features, we used SPICE to simulate two different cases: (1) the op-amp had a $\approx 2.6 \cdot 10^8$ Hz GBWP, and (2) the op-amp had a $\approx 2.6 \cdot 10^9$ Hz GBWP. Fig. 3 shows the effects of the GBWP upon the integration. For a larger GBWP the overshoot is attenuated. These SPICE predictions led us to choose the AD 829 as an integrator, taking into account its 750 MHz transition frequency and its low noise performance. For a better overshoot compensation we used an AD 848 connected in a feedback network which also stabilized the d.c. output component. The outline of this integrator is presented in fig. 4, while the actual schematic is shown within the general diagram in Appendix A.

Because the minimum level of the integrator output voltage is about 0.4 mV, we have to verify the noise level at the integrator output is less than this. Fig. 5 presents the basic diagram of an op-amp connected to an integrator configuration which avoids the op-amp saturation by using the bleeder resistor R. It can be demonstrated that the voltage noise RMS value at the integrator output is given by (8), [22]:

$$V_{no}^2 = e_n^2 \cdot B + i_n^2 \cdot R/(4 \cdot C) + k \cdot T/C \qquad (8)$$

Fig. 3: Integrator Response Dependence on GBWP



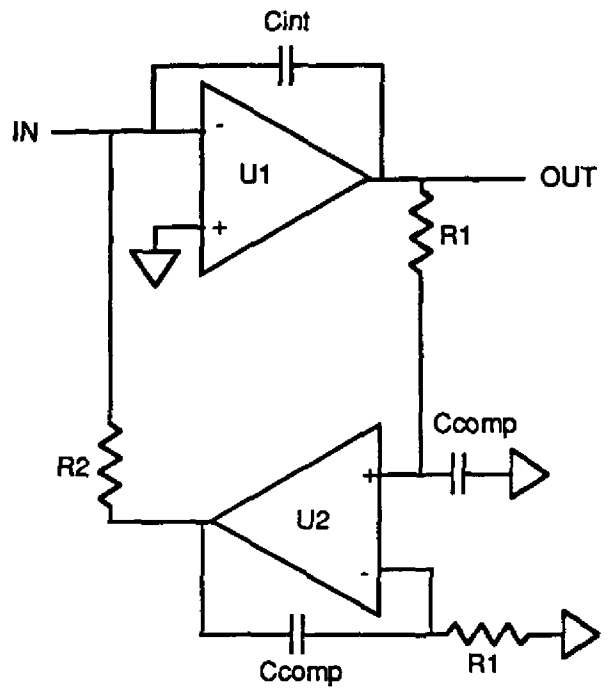


Fig. 4 The fast, low noise integrator

Where V_{no} is the noise RMS value at the integrator output, e_n is the op-amp voltage noise spectral density, i_n is the op-amp current noise spectral density, k is Boltzman constant, T is the operating temperature in Kelvin, and B is the operating frequency range, which in this case are 300 K and 100 MHz, respectively. Since $e_n = 2\ nV/\sqrt{Hz}$ and $i_n = 1.5\ pA/\sqrt{Hz}$ for an AD 829, according to [1], we calculate V_{no} to be about 0.13 mV_{rms}, hence the noise performance satisfies 104 dB dynamic range requirements. This value corresponds to C = 10 pF, and R = 300 KΩ, a value which simulates the d.c. compensation network behavior.

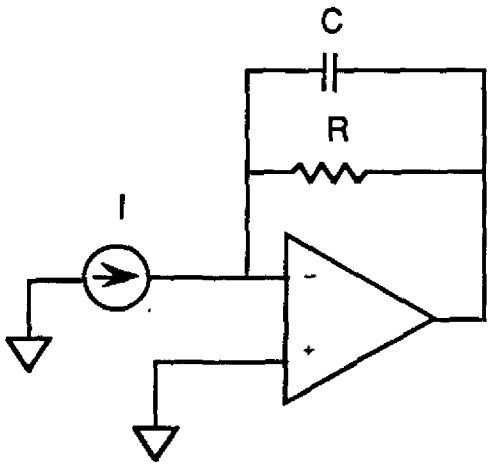
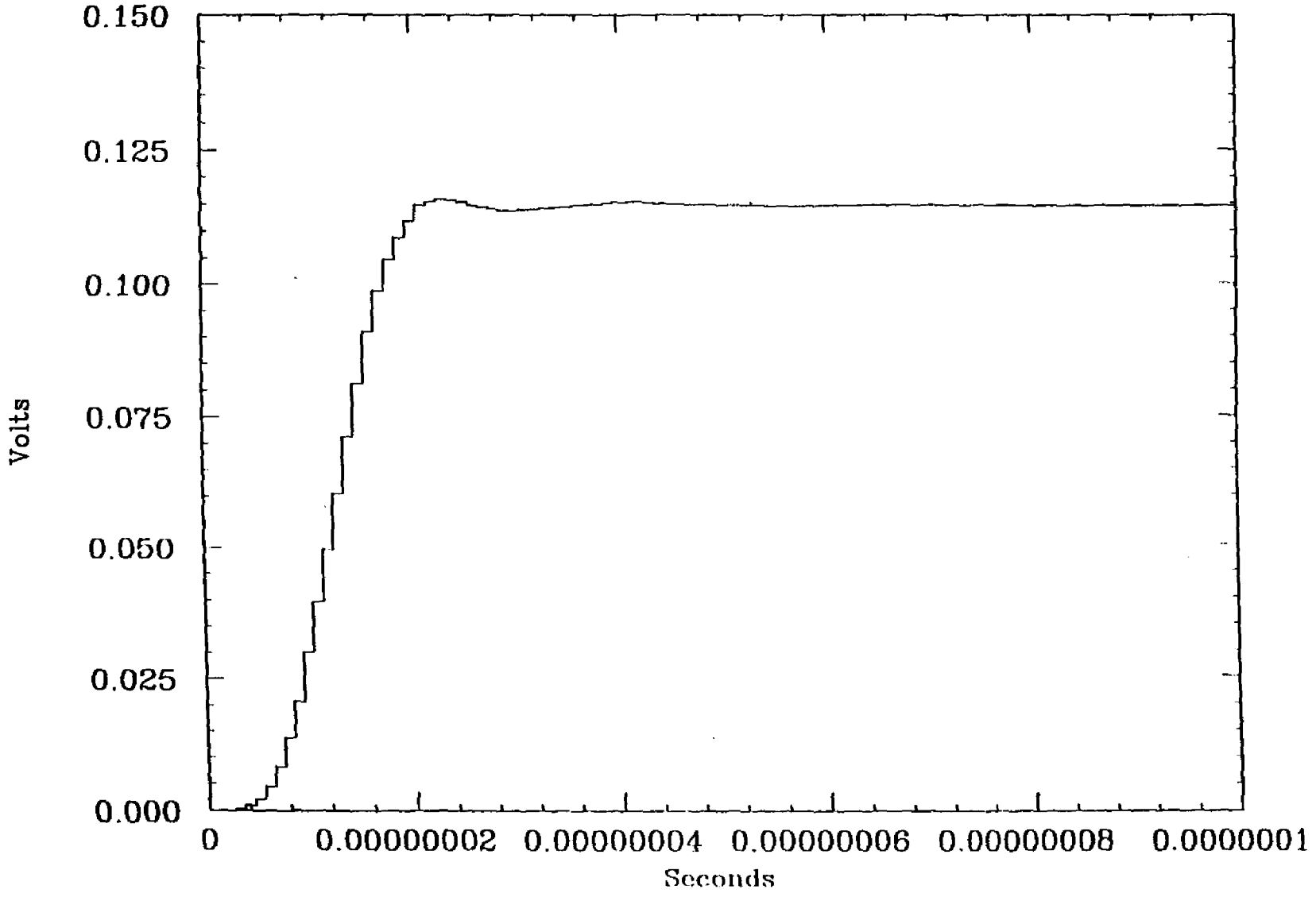


Fig. 5 The configuration for noise performance computation

For the configuration in Fig. 4 no bleeder resistor is needed because the d.c. and low frequency behavior is stabilized by the feedback network comprising R1, R2, Ccomp, and U2. The network was designed such that R2 can also compensate the overshoot which appears at the end of the integration, due to the limited GBWP of the op-amp. This solution makes the compensation easy to implement, but it has the drawback that it generates a damped low frequency oscillation at the integrator output. This oscillation does not affect the performance of the whole circuit because it is cancelled by the baseline restoration circuit. If the PMT output current pulse amplitude is equal to its minimum level of 300 nA then, according to section *A.*, about 254 nA will enter into the high gain path. The high gain path current amplifier amplifies this current up to about 762 nA. For a typical 16 ns PMT output pulse, as it was described before, this implies that the injected charge into the high gain path integrator is about 6 fC. For the integration capacitor equal to 10 pF this means an integrator output voltage of about 600 μV. This is the minimum voltage level at the integrator output. As was required it is higher than the voltage noise RMS value which was estimated to be about 130 μV. In order to have the ratio between the gains of the high and low gain paths equal to 32 the integration capacitor of the low

Fig. 6: Integrator Response to a Typical PMT Pulse



gain path has to satisfy (5.5 is the ratio between the currents flowing into the high gain and low gain paths, respectively):

$$C_{intlg} = C_{inthg} \cdot \frac{32}{5.5} = 10\ \text{pF} \cdot \frac{32}{5.5} = 58\ \text{pF}$$

Because both values have to be commonly available we chose to use 15 pF for the high gain path, and, subsequently, 91 pF for the low gain path. For these values the minimal voltage level at the integrator output is about 375 μV, which is still higher than the estimated voltage noise RMS value. Fig. 6 presents the SPICE-simulated response of the integrator to a typical 16 ns PMT output pulse. The droop, within 4 ns after the integration is completed, is about 0.1% from the peak level and it is expected to be possible to further improved it on the PCB by properly adjusting the value of R2.

C. The baseline restoration circuit

If a very high energy deposit is followed by a very low energy one, the accuracy of the front end electronics may be affected because some of the devices between integrator and digital block will operate close to the saturation point, thus the information about the low energy crossing can be distorted or lost. It turns to be useful to insert a stage which has the property to restore the signal baseline, rendering the dynamic range of the circuit unaffected following a large pulse. The diagram of this circuit is presented in Fig. 7.

The signal at the non-inverting input is delayed 20 ns by the delay line. The delay can be reduced, using its 10 taps which are 2 ns apart. If a shorter delay would have been used the output signal, after the integration was completed, would not have been flat enough to avoid unsatisfactory time jitter error. As it can be seen from the diagram, the signal at the output of the

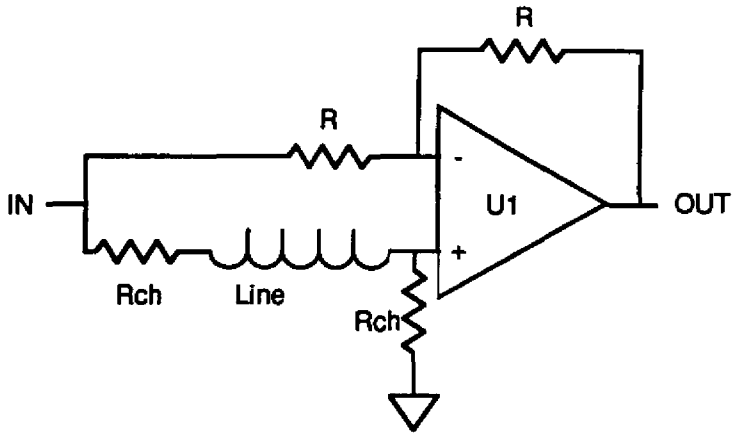


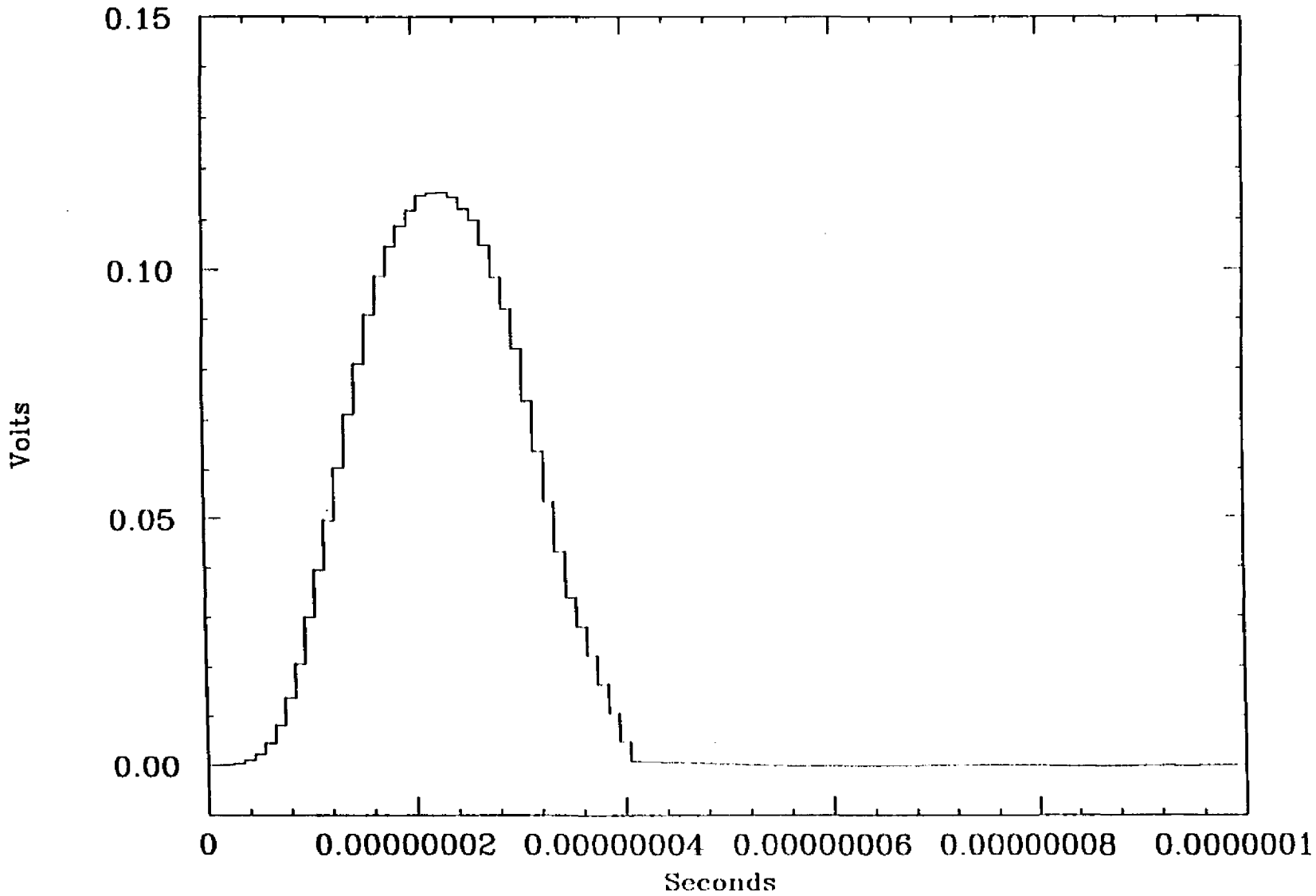
Fig. 7 The baseline restoration circuit

stage is equal to the inverted input signal during the first 20 ns, it returns to zero in the next 20 ns, and is zero after that. Considering the PMT output pulse lasting 16 ns, this means that the baseline is restored after 36 ns. For this application we employed CLC 400 current-feedback op-amp. There are three major reasons which justify this choice: (1) for current-feedback op-amps we have no gain bandwidth trade-off, (2) the slew rate is no longer a limiting factor, (3) and the CLC 400 has a very short propagation time and recovering quickly from saturation, [7]. For this op-amp the feedback resistor is required to be less or equal to 250 Ω, therefore we used R = 250 Ω. Because the pulse width is very short and the signal frequency spectrum very wide, in order to avoid the reflections which may appear at the ends of the delay line we terminated it with resistors, Rch, which match the line characteristic impedance at both ends. For the particular line we used (1P20, manufactured by ESC Electronics Corp.) these resistors had 100 Ω. Fig. 8 presents the SPICE-simulated response of the circuit to a typical integrator output signal.

D. The integrator protection against saturation

Even if the baseline is restored by the baseline restoration circuit, the pile-up of the signal at the output of the integrator can saturate it, causing loss of information during the actual

Fig. 8: Clip Amp Response to a Typical PMT Pulse



recovery from saturation. Unfortunately this time interval may be very long due to the fact that a very low droop at integrator output was required to minimize time jitter error. The circuit presented below is designed to discharge the integration capacitor C1 when the output of the integrator U1 reaches 2V, thus avoiding the loss of information which might occur if U1 gets saturated. The first pulse for which the 2V threshold is exceeded will be normally processed, and the discharge process is delayed about 40 ns in order to permit the baseline to be restored. After this delay, the discharging of C1 is triggered and takes 40-50 ns to restore the baseline at the integrator output. In order to avoid the saturation of the SCA, which may occur during the transition generated by the discharge of C1, the output stage is provided with ultra-fast switching and clamping diodes (MBAL 99) which limit the output swing to 5V. Fig . 9 presents the diagram of the integrator saturation protection circuit. The performance of this circuit might be affected when a high energy signal, which triggers the C1 discharge, is immediately followed by a very low energy one. If the information about the low energy crossing can't be stored in the low gain switched capacitors array and it occurs exactly during the time C1 is

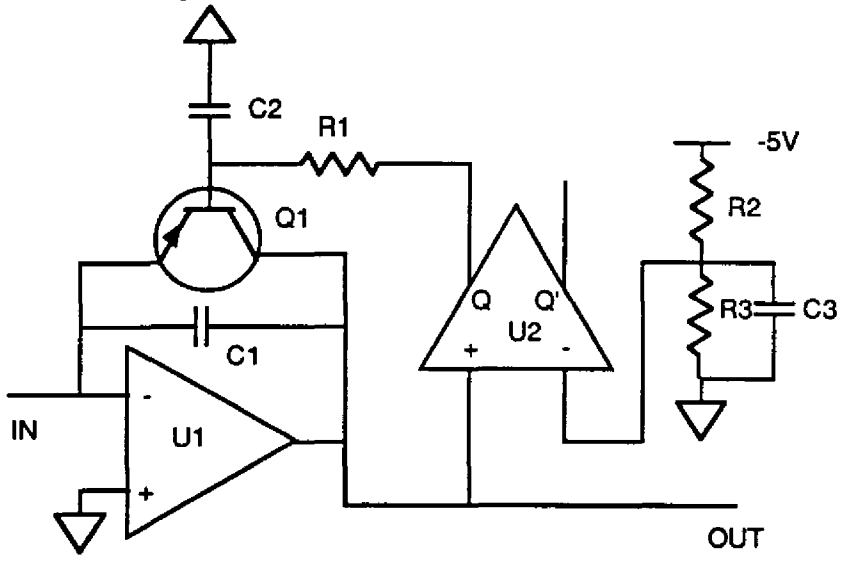


Fig. 9 Protection against saturation circuit

discharging, then the information is lost. However, the probability of an event like this is very low.The threshold which determines the triggering of the integration capacitor discharge is fixed by R2, R3 and is equal to:

$$Vthr = -5V \cdot \left(\frac{R3}{R2+R3}\right) \tag{9}$$

This circuit has to satisfy two major requirements: (1) to switch within 40 ns after the threshold is exceeded, (2) to generate very low additional noise at the integrator output. To satisfy the fast switching requirement we employed a very fast switching pnp transistor (2N5771) and a ultra-fast comparator (AD 96685). The comparator propagation time is about 2.5 ns while the transistor switching time is about 15 ns. R1 and C2 network adjust the delay to 40 ns. To check the second requirement we point out that most of the time the transistor Q1 is off. In the cut-off region the transistor generates a shot-noise due to the fluctuations which appear in the collector cutoff current. The spectral density of this noise is given by, [22]:

$$i_{sn} = 4 \cdot q \cdot I_{CB0} \tag{10}$$

where q is the electron charge, and I_{CB0} is the collector cutoff current. For the 2N5771 I_{CB0} is given to be equal to 10 nA. Substituting these values in (10) we get $i_{sn} \approx 6.4 \cdot 10^{-27}$ A/$\sqrt{Hz}$. In the worst case we have to add its effects upon the output voltage noise RMS value, to those of the op-amp current noise. Going back to (8) this means that we have to add $i_{sn}^2 \cdot (R/4 \cdot C)$ to the already computed squared output voltage-noise RMS. However, comparing the values of i_{sn} and i_n we found the effects of the shot-noise to be negligible compared to those of the op-amp current noise. Fig. 10 presents the SPICE simulations for the circuit behavior after the threshold was exceeded. We can see that it needs about 40 ns to recover after the capacitor is discharged, and this can cause loss of information if a very low energy crossing occurs during this period of time.

E. The cable drivers

The output stage has to be able to drive either 50 Ω coax cables or 100 Ω twisted-pair cables. The output swing in both cases has to be equal to ± 2.5 V. In order to protect the input of the switched capacitors array this stage output has to be provided with clamping diodes (MBAL 99) which will not allow the output to exceed the mentioned swing. For this purpose we employed CLC 420 which is an 1100 V/μs slew rate, 4 nV/√Hz voltage noise and 2 pA/√Hz current noise voltage feedback op-amp. The CLC 420 is able to drive 50 Ω cables, and in order to avoid reflections we inserted 50 Ω resistors at the output to match the cable characteristic

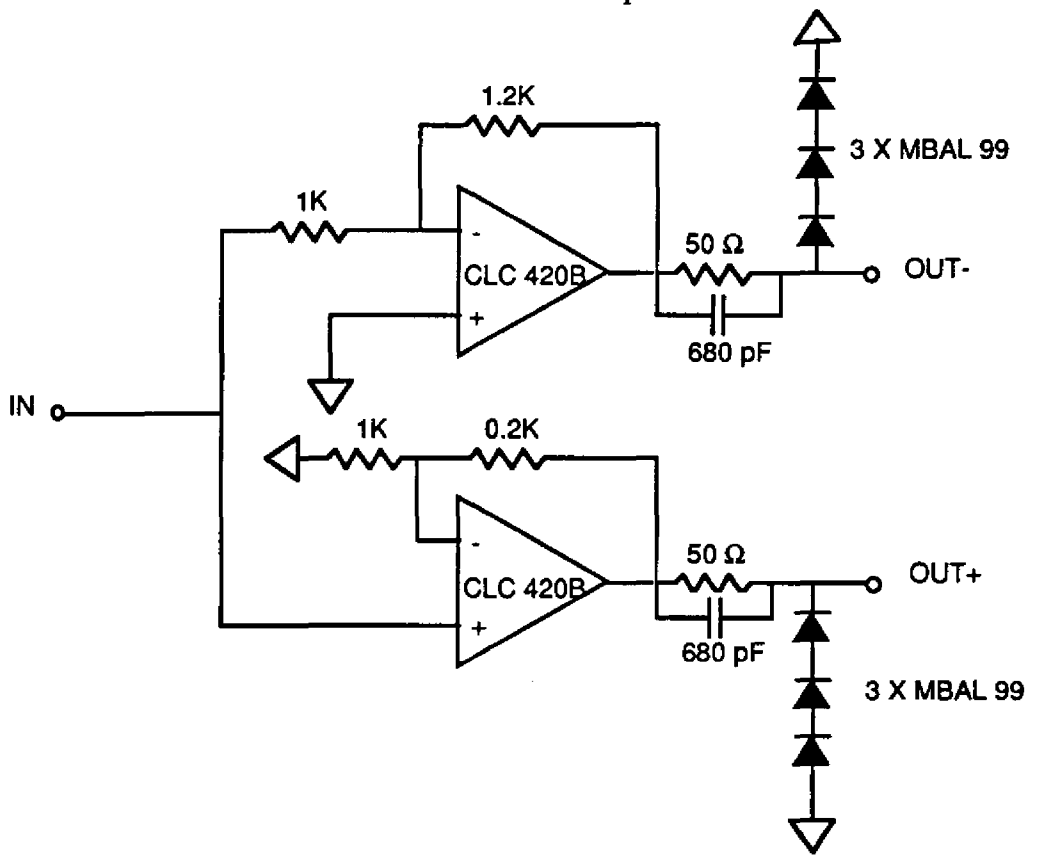
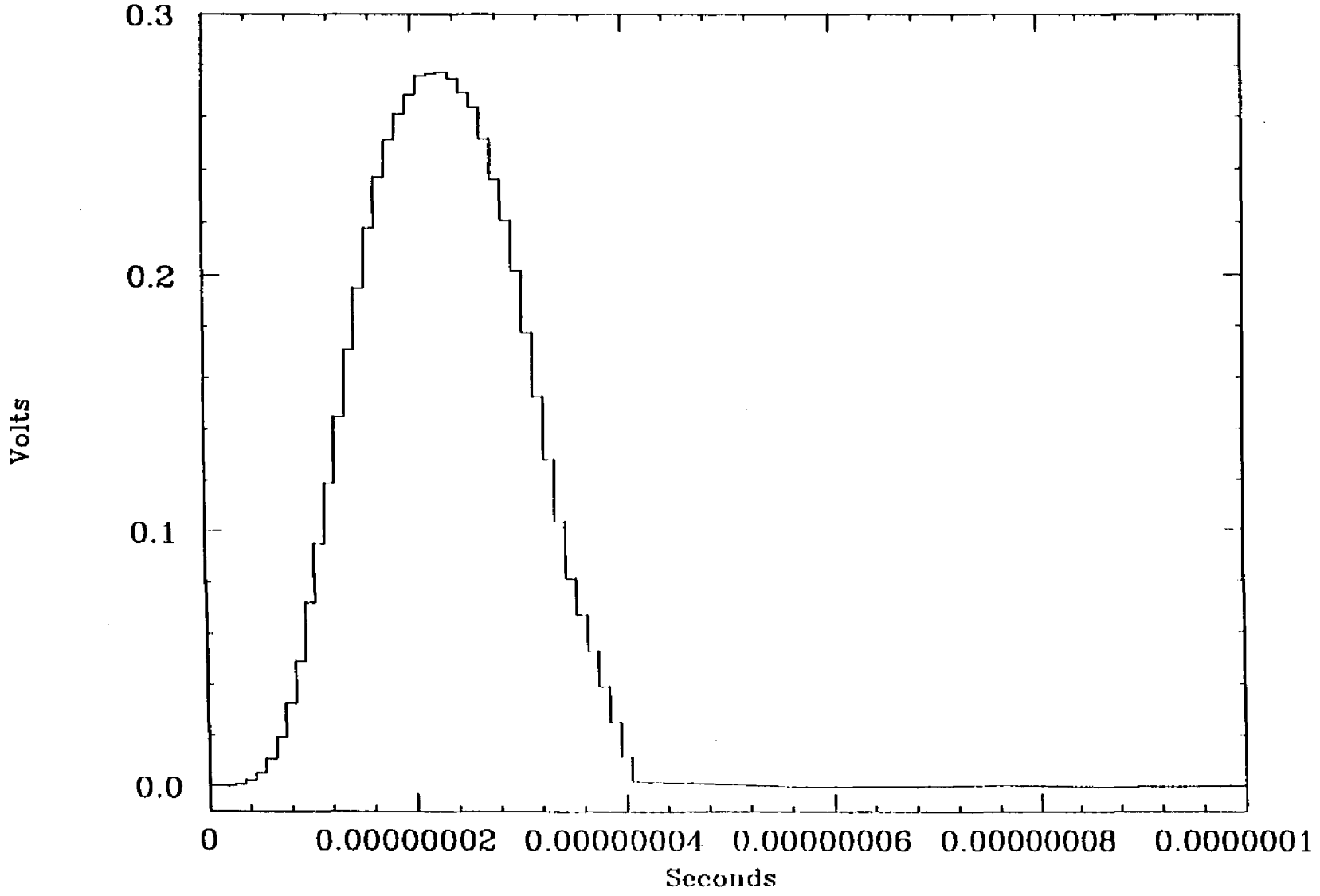


Fig. 11 The cable driver

impedance. The diagram of the cable driver is presented in Fig. 11. The 680 pF capacitors

Fig. 12: Output Stage Response to a Typical PMT Pulse



compensate the cable frequency characteristic. The stage has a gain of 1.2 such that together with the previous stages it provides the output with a ± 2.5 V swing.In order to check this assertion we consider the PMT output current pulse amplitude to be equal to 50 mA. In this case the peak current flowing into the low gain path is about 7.7 mA. After it is amplified 3 times by the low gain path current amplifier it will inject about 62 pC into the low gain path integrator. For a 91 pF integration capacitor this means a 2 V integrator output voltage. Considering the 1.2 gain of the cable driver stage the front end amplifier output swing will be about 4.8 V_{p-p}, which is close to the required output swing. Similarly to eq. (8) it can be found that this stage adds about 20 μV_{rms} voltage noise to each of the front end amplifier outputs. Fig. 12 shows the SPICE simulation results for the cable driver response. It can be concluded that, according to these simulations, the circuit meets the previously presented requirements.

III. Results

In order to test the previously presented design, we built the high gain path on a breadboard circuit. To have the current amplifier and the integrator working in the linear region for all the range of input currents we used ± 8 V voltage regulators as power supplies for this part of the amplifier. The baseline restoration stage, the protection against saturation circuit, and the cable driver were supplied from ± 5 V voltage regulators. The input signal was generated by a Hewlett Packard pulse generator which was converted into a current source by a voltage to current converter we built on the same breadboard. We used rectangular pulses in order to more easily estimate the injected charge. The results of the tests of the main parameters are summarized in table II. The results of the test regarding the crossover of the previous bunchcrossing in the present crossing are summarized in table III. The percentages represent the error introduced by the past crossing with respect to the expected peak value of the present crossing if it would have arrived alone. We tested both 16 ns and 20 ns delay lines. It can be

seen that a 16 ns delay line implies less crossover, but also it has too much droop over 4 ns after the integration is completed. This was the main reason we chose to work with a 20 ns delay. The measurements of the linearity with respect to the pulse width were affected by the errors introduced by the pulse generator, which could not maintain the rectangular shape of the pulses for lower width. To test the noise performance we used a Le Croy 9410 digital scope together with a low noise, 48.5 gain, and ≈ 100 MHz bandwidth voltage amplifier. The output voltage standard deviation within a 200 ms window was 11 mV, which corresponds, for the circuit itself, to 11/48.5 = 0.226 mV $_{rms}$. This figure is consistent with the

Table II.
Results of the tests for the breadboard circuit

Droop over 4 ns after the integration was completed	≈ 0.07 % from the peak value
Linearity with respect to the pulse width	≈ 1 % from the peak value
Output voltage noise RMS value	≈ 0.23 mV

theoretical expectation, taking into account the noise introduced by the clip-amp, and the input stage, and the fact that the test was performed on a breadboard circuit.

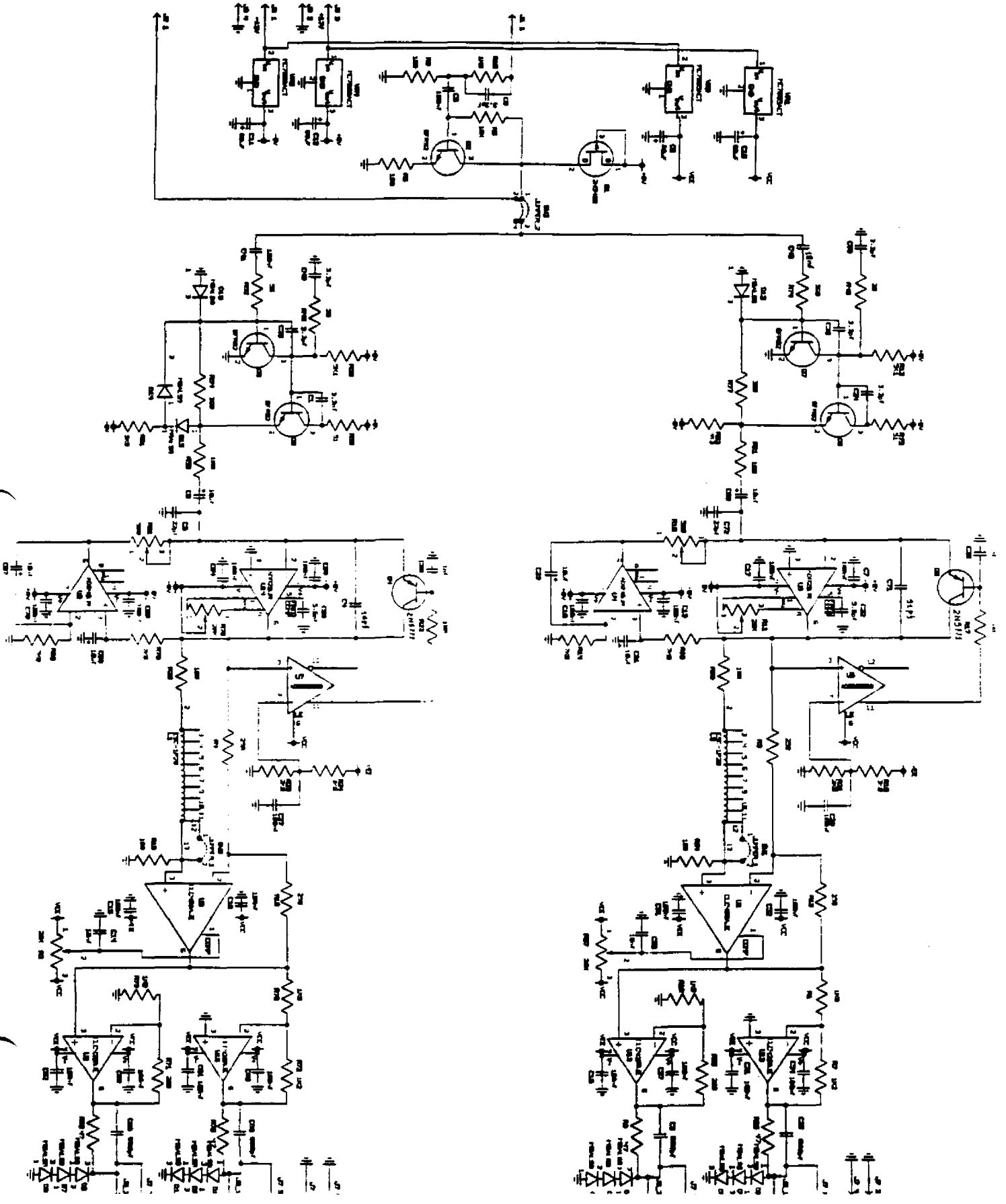
Table III
The crossover of the past bunchcrossing in the present crossing

Time lag between crossings	The 16 ns delay line	The 20 ns delay line
16 ns	≈ 6.3%	≈ 18%
32 ns	< measurement resolution	≈ 5.4%
50 ns	< measurement resolution	< measurement resolution

The front end amplifier will be built on a 6 layer ≈ 5"x3" PCB, using mostly surface mount devices. The signal was routed in two layers while the others were used as power and ground planes. In order to avoid the undesired effects of the reflections which may occur at the ends of the delay lines, the PCB was designed such that the characteristic impedance, for the traces which connect the delay lines to the rest of the circuit, matches the 100 Ω delay line impedance. We anticipate an improvement of the droop for the PCB version of the front end amplifier due to the attenuated effects of the reflections.

IV. Conclusions

As is customary, this design involves a trade-off between the noise performance, circuit speed, and dynamic range. Earlier work on front end amplifiers, [6], [9], and [17], illustrate that is difficult to achieve very good noise performance with very good speed performance for an ≈ 100 dB dynamic range. Because of the low level of the minimum input signal it is hard to achieve the needed dynamic range using only one integrator, since the noise performance is given mainly by this stage. Using only one integrator would imply a very low output voltage noise RMS value (about 30 μV). Trying to achieve a very low noise level at the output might have an undesired effect upon the circuit speed, and would make the circuit unable to distinguish crossings that are close together. Integrated versions of the front end amplifier, [9] and [17], show that a low output voltage noise level was achieved when the response time of the circuit was not fast enough to achieve a good droop performance for a typical 16 ns PMT output pulse. Also none of the solutions presented in [6], [9], and [17], reached such a low output voltage noise level to make it suitable for processing an ≈ 100 dB dynamic range fast input signal. Based on this reasoning we used a solution where one integrator was employed for each of the low and high gain paths. The results of the tests of the breadboard circuit show that the



solution is feasible and achieves the needed requirements. The circuit we presented has a droop over 4 ns, after the integration is completed, of ≈ 0.07 %, a linearity of ≈ 1 % and an output voltage noise RMS value of ≈ 0.23 mV_{rms} for an input signal dynamic range of ≈ 100 dB.

Appendix A.

The actual diagram of the front end amplifier is presented in fig. 13. The transistors Q1 and Q2 are used in a voltage to current frequency compensated converter which allows us to test the board using a constant voltage generator connected to the connector J1. By switching the jumper 2 in the position 2, the PMT can be connected to the amplifier input through the connector J2. The cables to the SCAs can be connected to the connectors J5 and J6, if they are coaxial, or to the connector J7, if they are twisted-pair. The board has to be connected to an external ± 12 V power supply source through the connector J3.

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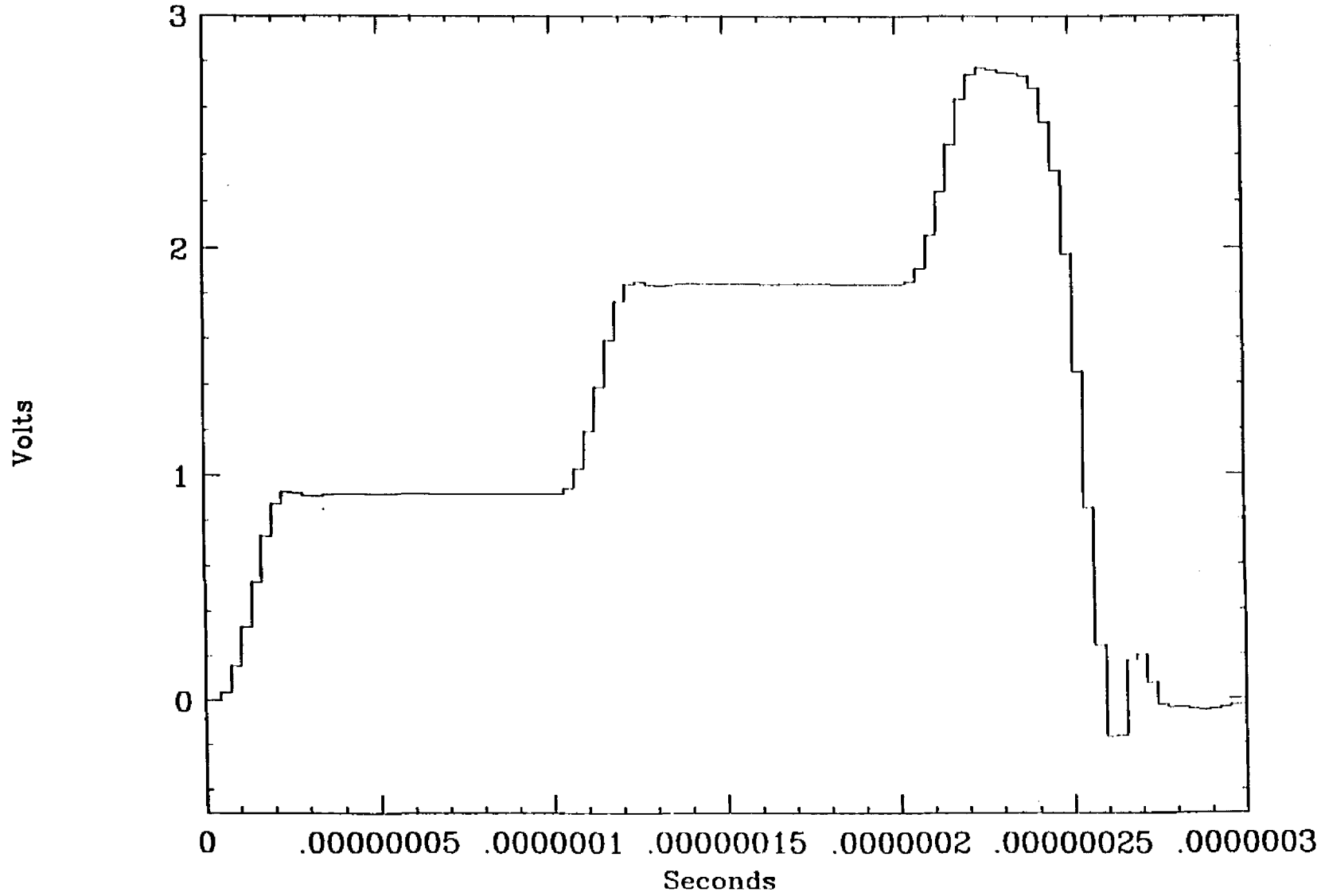
Fig. 10: Response of Saturation Protection Circuit