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SDC
SOLENOIDAL DETECTOR NOTES

CONCEPTUAL DESIGN OF STRAW TUBE READOUT WITH TMC

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Executive Summary

This document is a conceptual design report of the readout system for the straw tubes of the central SDC tracking system. The proposed system is based on the TMC (Time Memory Cell); a VLSI time digitizer newly developed in order to meet the specific requirements imposed by the SSC experiments. A prototype 4 channel TMC chip with 1μs deep pipeline memory (TMC1004) has been successfully developed at KEK using NTT 0.8μm CMOS technology. The prototype has demonstrated the feasibility of the basic concept as well as the following performance;

time resolution	$\sigma = 0.52$ ns
power consumption	7 mW/channel (1% readout duty factor).

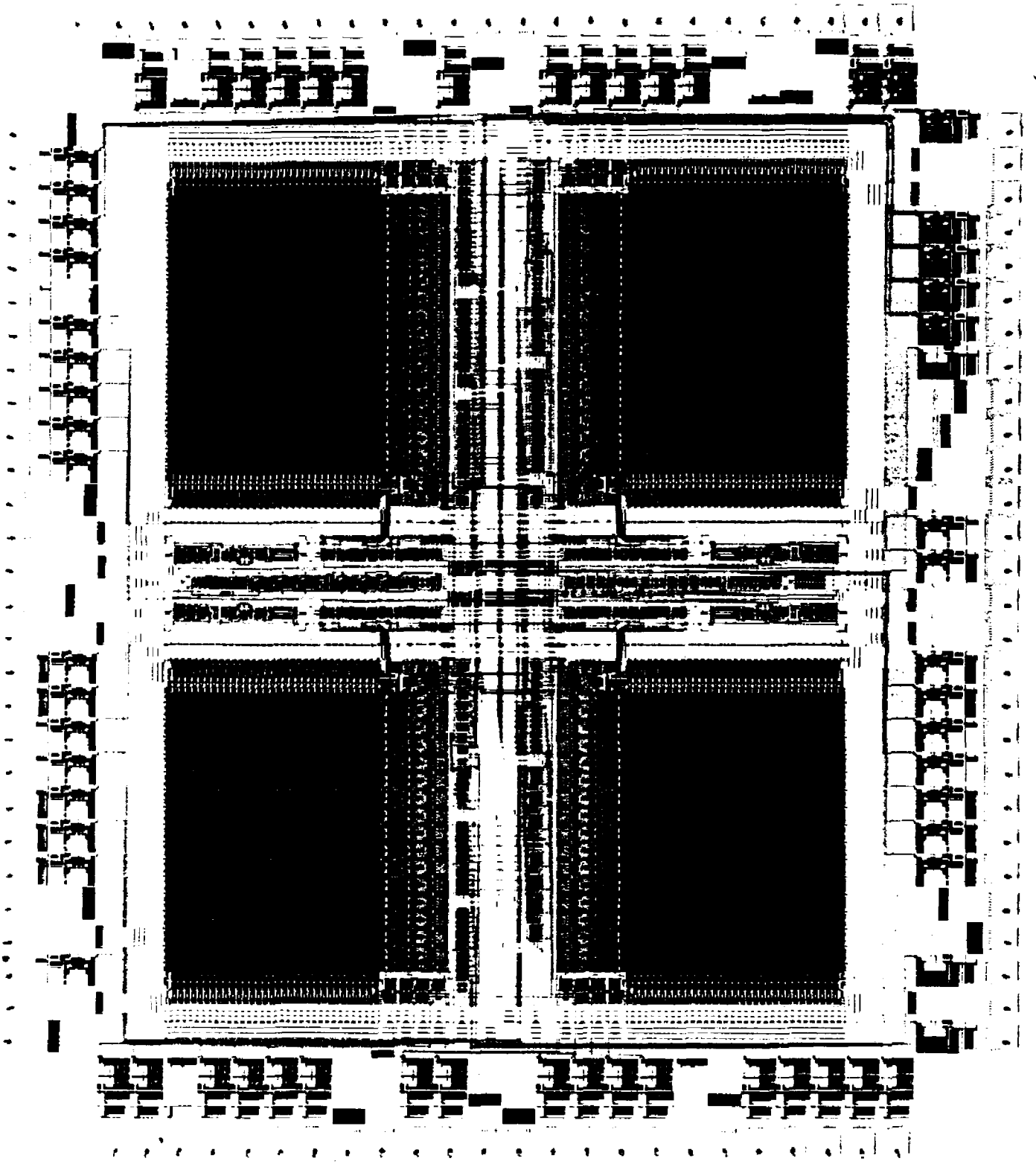
Amp/Shaper and Discriminator chips have also been developed at KEK using NTT bipolar process known as Super Selfaligned Transistor (SST). Prototype chips are successfully tested and used for straw-tube readout.

The present report describes the architecture of the readout system that can be accommodated physically with the current SDC detector design. The final TMC chip with the memory capability of 4μs for the level-1 trigger is proposed. The proposed readout system for the case of the 130K straw tracker is

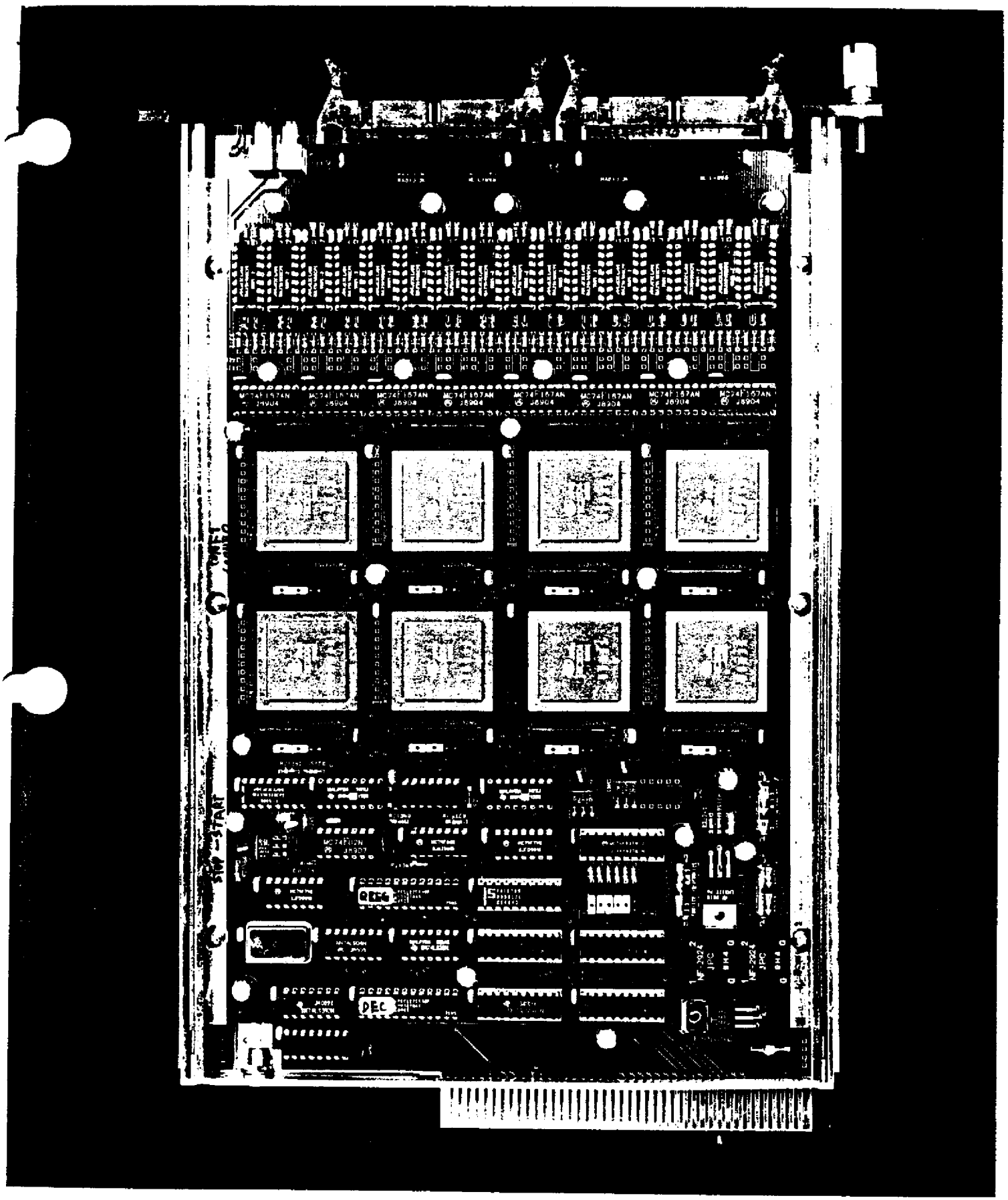
Amp/Shaper/Discriminator chip	4ch/chip
TMC chip	4ch/chip
TMC level 2 Buffer chip	4 ch/chip
Hybrid IC	8 ch/hybrid
Data Collection Chips	256 ch/unit
Front End Board (FEB)	256 ch/board
Multi Data Buffer (MDB)	1024 ch/module
Local Buffer Crate	8 crates x 2 sides.

The data transfer rate is examined to be reasonably practical with the present-day technology. An initial attempt of the cost breakdown showed approximately $8.7M for the total readout system. Radiation damage study is under way. The preliminary analysis has indicated promising results.

In conclusion, we have successfully developed the prototype preamp/shaper, discriminator, and TMC chips. The proposed readout system meets almost all the SDC requirements with few critical paths left.



Photograph 1. TMC1004 chip



Photograph 2. CAMAC 32 ch TDC module using the TMC chip

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Appendix A: A CMOS 4 ch x 1 k Time Memory LSI With 1 ns/bit Resolution

[abbreviations]

ASIC : Application Specific IC
CSR : Control and Status Register
DCC : Data Collection Chip
DTX : Data Transmission module
FEB : Front-End Board
KEK : Kou Energy Kenkyuusho, National Lab. for HEP
LBC : Local Buffer Crate
L2B : Level 2 Buffer chip
MDB : Multi Data Buffer
NTT : Nippon Telephone and Telegram Co.
P/S/D : Preamp/Shaper/Discriminator chip
P.S. : Power Supply
SCP : Superlayer Control Processor
SDC : Solenoidal Detector Collaboration
SST : Super Selfaligned Transistor
TMC : Time Memory Cell

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1. Introduction

We describe here a conceptual design of the readout electronics for the Straw-tube Detector. Our scheme is based on the Time Memory Cell (TMC) chip (photograph 1) which is developed at KEK with collaboration of NTT. The TMC chip is a low-power and high-density time-to-digital conversion VLSI which has enough ability for the wire chamber readout at the SSC. The prototype chip is already tested and a CAMAC module (photograph 2) which use 8 TMC chips are used for straw-tube readout [1,2,3].

In this document, we try to optimize the readout scheme to the TMC, but most of the parts except the preamp/shaper/discriminator and the TMC chips are very primitive stage. There remain many places which must be adjusted in a whole data acquisition system. There are many intensive studies for the Straw electronics by the people in Univ. of Pennsylvania [4].

Most of the electronics described here will be also applicable for the readout of muon chamber. We are trying to fulfill the requirements of both straw and muon detector to reduce the cost and development effort.

2. Conceptual Design

2.1 Requirements and Detector parameters

In the SDC, a straw-tube detector is proposed for the central tracking detector. Since the detector parameters are still not fixed, we assume following parameters for the Straw-tube detector presented at LBL meeting on Aug. 1991.

Table 1 Straw-tube detector parameters.

Superlayer	layers	angle(deg)	r (cm)	length (m)
SL1	6	0	70.4	2.8
SL2	6	3	104	3.2
SL3	8	0	134	3.9
SL4	6	-3	148	3.95
SL5	8	0	161	3.95

- Tube diameter : 4 mm
- No. of Straws/module 150 - 256 tubes
- No. of Channels : 135 k channels

Hit rate of the straw tube at the radius of 70 cm is a few MHz at a nominal luminosity of 10^{33} $cm^{-2}sec^{-1}$. The front-end electronics must work without deadtime and keep the information for 3 - 4 μs of the first level trigger decision time. The drift time of the straw tube is around 30 ns with fast gas of 100 μm/ns drift velocity. To get a spatial resolution of 150 μm, the timing error of the front-end electronics must be less than 1 ns. Furthermore, the front-end electronics must be low-power and high-density devices, because it is mounted in a very limited space. Finally the front-end electronics must survive from the radiation damage of γ rays and neutrons.

2.2 Data Flow Diagram

Figure 1 shows a data flow diagram of the proposed straw-tube detector readout system. Front-end boards (FEB) are mounted on the detector, and Local Buffer Crates (LBC) are placed outside of the barrel calorimeter. Since each straw module has 150 - 256 tubes, each board deals up to 256 channels. Assuming the data size of 4 byte/channel, 10% occupancy, and 10 kHz level 2 trigger rate, the required transfer rate at the output of the FEB is ~1 Mbyte/sec. Thus a data bus of a 2 MB/sec band width is enough for this purpose. Output data from the FEB are transmitted to a Multi Data Buffer (MDB) module outside the detector through shielded twisted pair cables. The MDB receives data from 4 FEB's. A Data Transmission module (DTX) collects the data from ten MDB's in a crate and sends it out through an optical fiber cable. The average data size transferred through the DTX is 6 kB/trigger. For level 2 trigger rate of 10 kHz, the data transfer rate becomes 60 MB/sec. Thus the transmission rate of 1Gbps is required here. Since the straw-tubes are read out at both ends of the detector, eight local buffer crates are placed at one side.

2.3 Control Path Diagram

Figure 2 shows a diagram of the control path for the front-end electronics. Each FEB has a serial network interface of 10 Mbps. The serial networks in each superlayer are linked to a Superlayer Control Processor (SCP) in electronics room at the surface. The SCP's are controlled from a host computer. The FEB includes test pulse circuits for the preamp and the TMC. All the monitoring, calibration, diagnostics are done through the serial network.

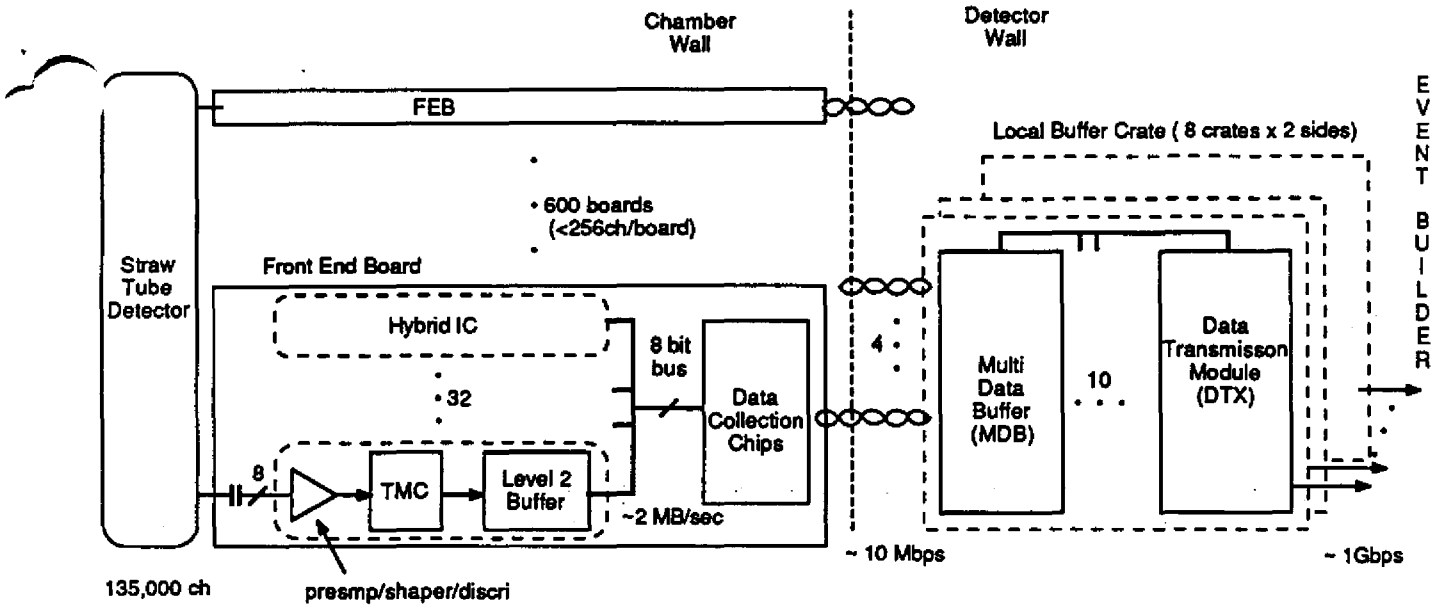

Fig.1 Data Flow Diagram of the Straw Tube

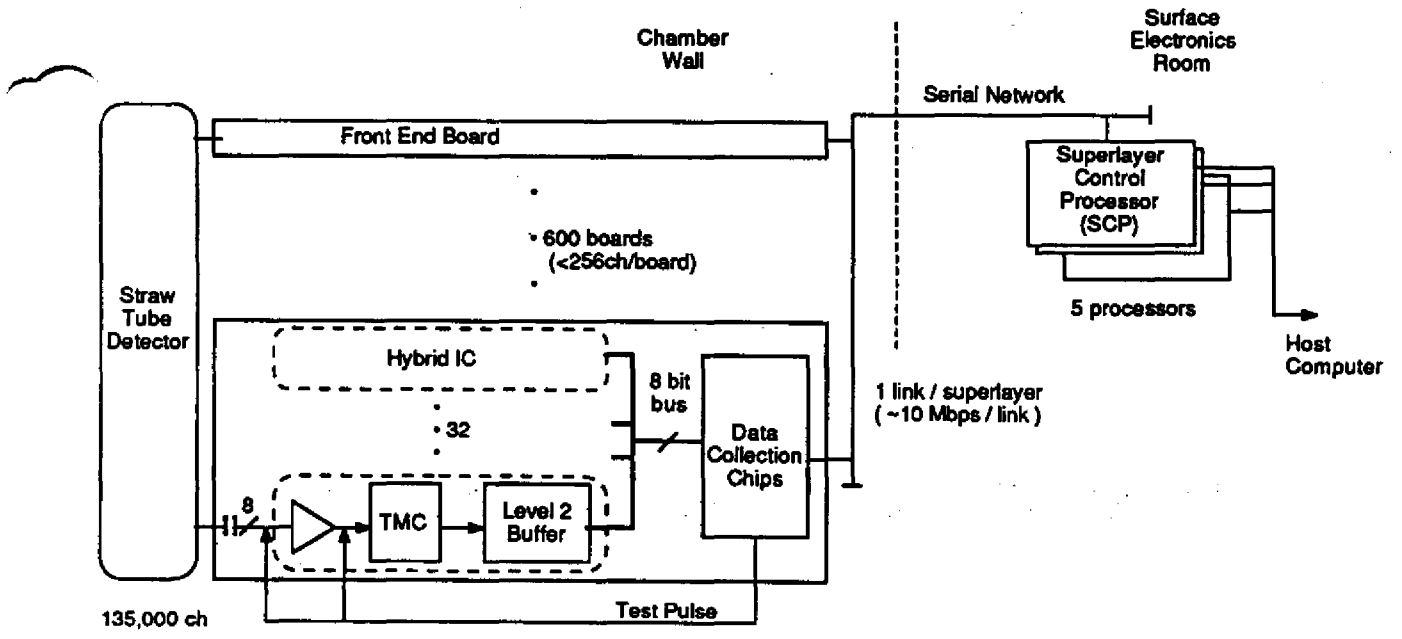

Fig. 2 Control Flow Diagram of the Straw Tube

2.4 Trigger Flow Diagram

Signals from the outer one or two superlayers are used to form track trigger signals. These trigger signals will be used with calorimeter, muon, and silicon tracker signals by checking ϕ matching. Since the straw-tubes are arranged in pointing to a beam interaction point and half-cell staggered, two types of trigger logics, time difference and time sum (mean timer), are possible.

Method of measuring the time difference within cells on a line is shown in Fig.3 -(a). The time difference is inversely proportion to the transverse momentum Pt. By changing the clipping time Tc, Pt threshold value is adjustable over a few GeV/c.

The mean timer circuit for the staggered cell is shown in Fig.3 -(b). Since the sum of straw signal timing is constant and equal to the maximum drift time, the mean timer circuit creates a pulse at fixed timing after passing the track. Although the signal has timing ambiguity depend on the z-position of the track, the ambiguity is only $< \pm 3$ ns, thus the timing from the mean timer can be used for identifying the bunch crossing.

There are several schemes to use combination of this information and compose a trigger signal. Jay Chapman (Michigan) is studying 9 cell and 8 cell track trigger circuits by using above circuit. Muon chamber and shower maximum detector will have 1024 ϕ bins, whereas the outermost superlayer has about 2600 ϕ bins. Thus it is better to combine several track trigger signals at the FEB to reduce the number of cables. We need further study to optimize the logic to be effective, reliable and flexible.

Figure 4 shows the trigger-information flow of the straw-tube detector. A key element in the above circuits is a delay line. The TMC itself is a combination of delay lines and memories, and has precise delay elements. It is natural to include the trigger circuits in the TMC, but it is also possible to implement the circuits in a separate chip. Several stiff track trigger signals which have different Pt thresholds can be used. To reduce the number of cables while keeping the several Pt thresholds, multi-value logic which has two or three different levels may be used.

More detailed Pt and track position information can be available for the level 2 trigger if necessary. We can send 500 bit information to the Global Level 2 Processor in 5 μsec by using a 100 Mbps serial line .

2.5 Functions of Each Block

2.5.1 Front End Board

Figure 5 shows a block diagram of the front-end board. The FEB includes HV decoupling capacitor, hybrid IC's, and Data Collection Chips (DCC). The Hybrid IC has 8 input channels and consists of two preamp/shaper/discri (P/S/D) chips, two TMC chips, and two Level 2 buffer chips (L2B). Those chips will be mounted on a ceramic substrate or printed circuit board by using TAB bonding, wire bonding or flip chip technique. These hybrids are connected to a simple 8 bit bus through which the DCC reads out data from the L2B and controls various functions in the front-end electronics.

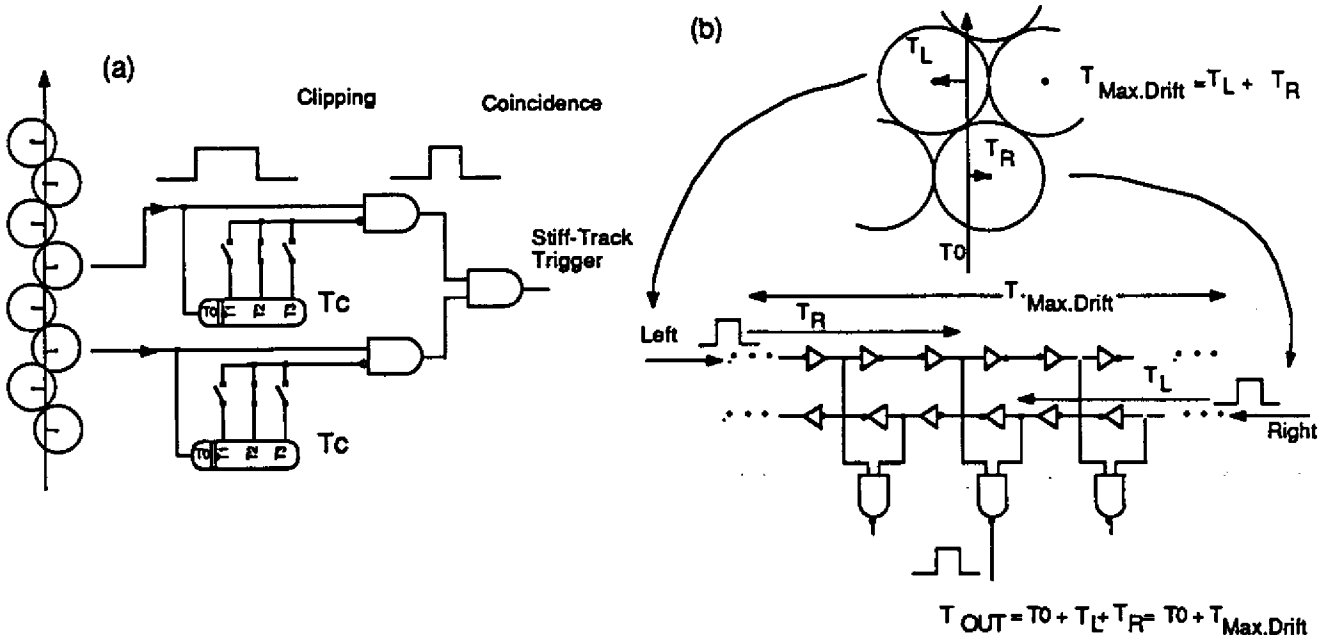

Fig.3 Basic Track Trigger Circuits. (a) Time difference circuit
(b) Mean Timer Circuit

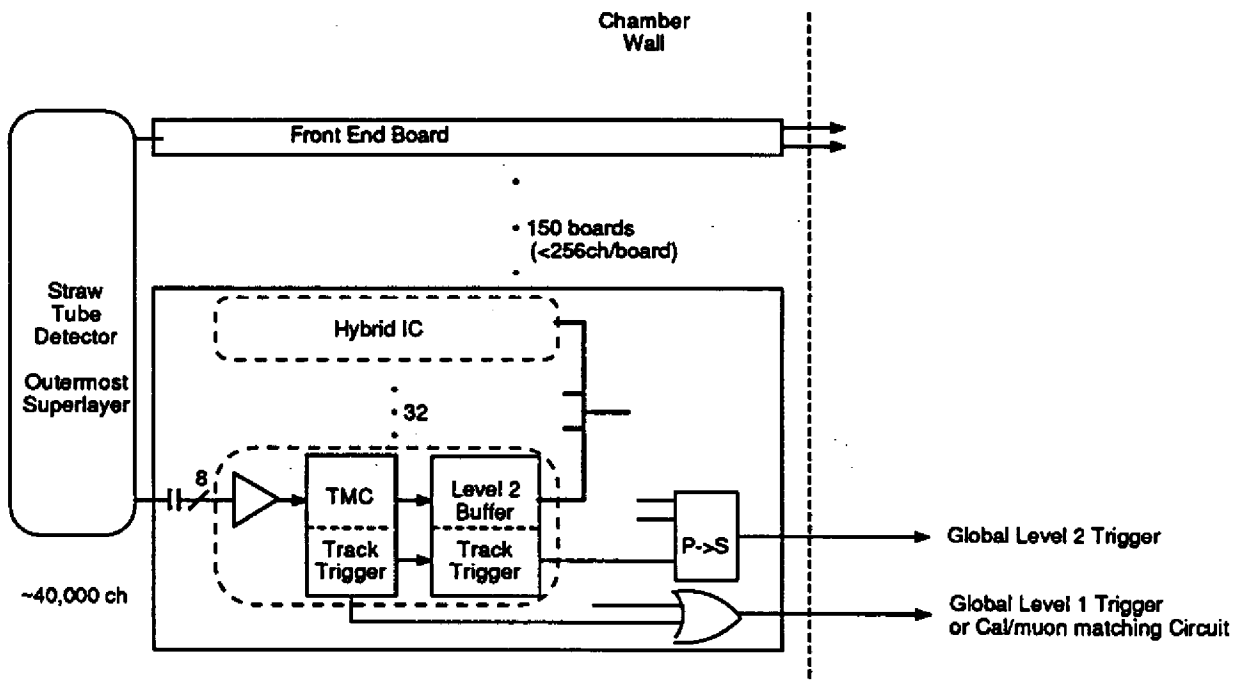

Fig. 4 Trigger Information Flow Diagram of the Straw Tube

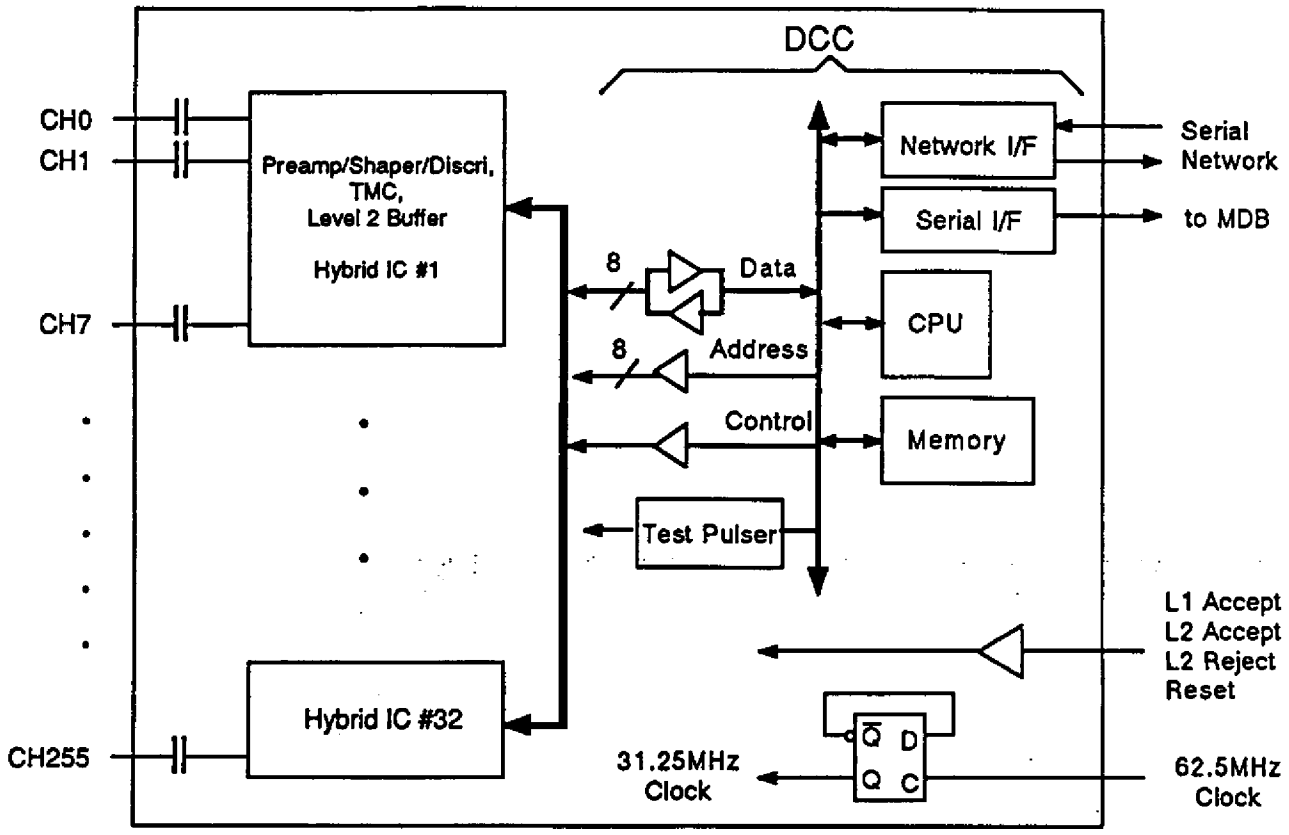

Fig. 5 Block Diagram of the Front-end Board

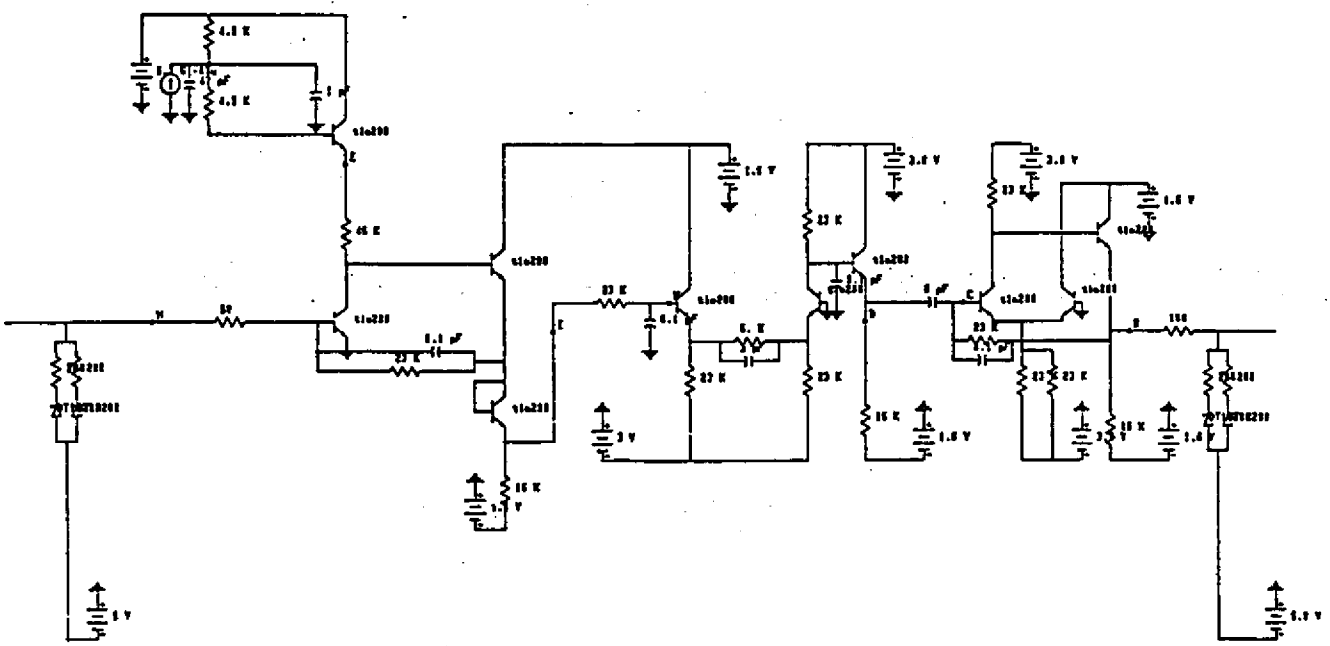

Fig.6 Schematics of the Prototype Priamp/Shaper Chips

2.5.1.1 Preamp/Shaper/Discri chip

Prototype preamp/shaper chips and discriminator chips are now being developed at KEK. The bipolar process used is NTT's Super Self-aligned Transistor (SST) with $f_T = 20$ GHz.

The preamp/shaper chip has 16 channel inputs. As shown in Fig.6, each channel has 4 integration stages, 1 differential stage, and a pole zero cancellation circuit. Two types of chip which have different time constants of 2.3 ns and 4.5 ns are designed. The gain is more than 300 mV/10^5 electron. One of the prototype preamp/shaper was tested with straw tubes by the Duke University group. Figure 7 shows the pulse shape for Fe^{55} γ-ray source.

The discriminator chip also has 16 channel inputs which contains input hysterisis circuit. The circuit diagram is shown in Fig. 8. In final chip, the preamp/shaper and the discriminator will be implemented in one chip, and will have 4 or 8 channels.

2.5.1.2 Time Memory Cell

Time Memory Cell (TMC) chip is a low-power time-to-digital converter chip which includes the first level buffer inside the chip. TMC records the history of the input signal to memory array in a digital method. The input signal is fed to the data line of CMOS memory cell, and each "write" signal to the memory cell is delayed with a variable delay element which is controlled by a feedback circuit. Table 2 summarizes the specifications of the present chip (TMC1004). The detailed explanation of the chip is given in appendix A.

Table 2.TMC1004 and TMC-SSC Specifications

	TMC1004	TMC-SSC
No. of Channels	4 channel	4 channel
Least Time Count	1 ns / bit	2 ns / bit
Time Range	1.024 μs (4 ch), 2.048 μs (2 ch) or 4.096 μs (1 ch)	4 μs
Clock Frequency	31.25 MHz	31.25 MHz
Time Resolution	$\sigma = 0.52$ ns	$\sigma = 0.75$ ns
Data Encoding	32 bit to 5+1 bit	16 bit to 4+1 bit
No. of Pins	I/O pins = 54 Power / Gnd pins = 34	I/O pins ~ 50
Supply Voltage	3.0 V	3.0 V
Power Consumption	7 mW/ch	~ 8 mW/ch
Chip size	5.0 x 5.6 = 28 mm^2	6 x 7 = 42 mm^2

Time resolution of the present chip is $\sigma = 0.52$ ns. This can be explained with a combination of the digitization error ($\sigma_{dig} = 0.29$ ns) and the TMC error ($\sigma_{TMC} = 0.43$ ns). To increase the buffer length while keeping the Si area within the acceptable level, we propose to increase the least count to 2 ns/bit instead of 1ns/bit of the present chip. If the σ_{TMC} of new chip is the same as the present

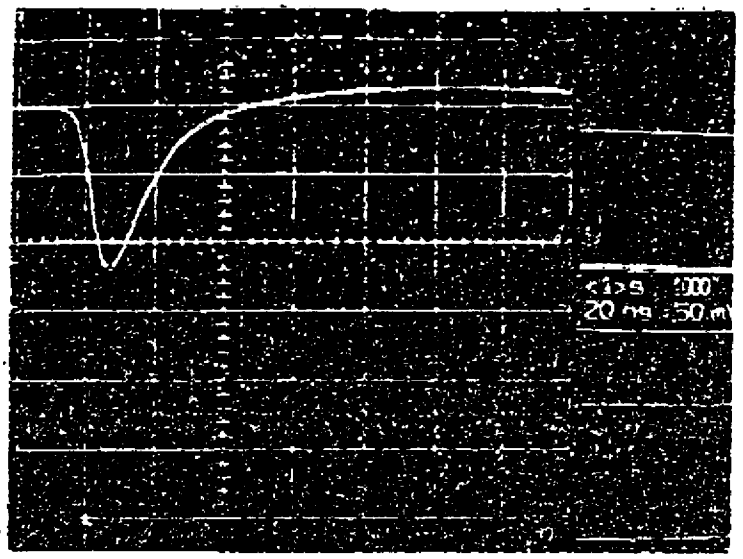

Fig.7 Output pulse shape of the prototype Preamp/Shaper for Fe^{55} γ rays.
(20ns/div and 50mV/div)

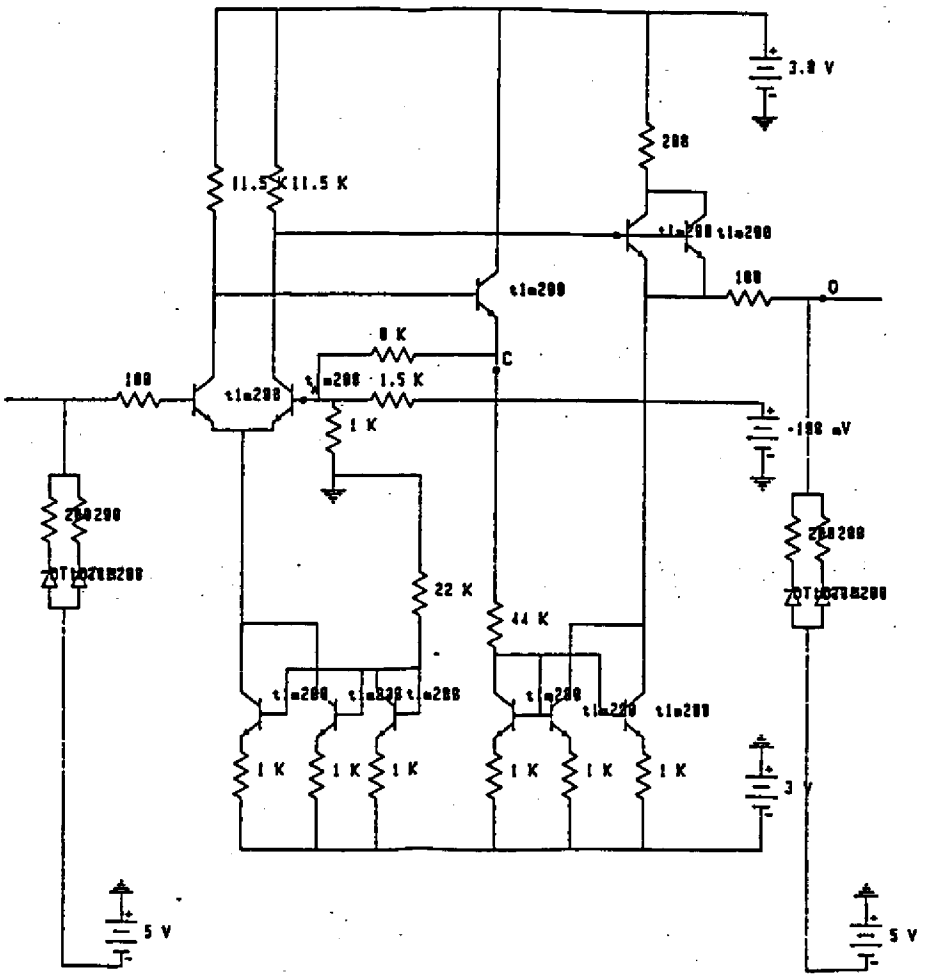

Fig. 8 Schematics of the prototype discriminator chip.

one, the time resolution will be 0.75 ns ($= \sqrt{(2ns/\sqrt{12})^2 + (0.43\ ns)^2}$). This resolution is expected to be within the requirement of the wire chamber readout.

The increase in Si area is only 50% even if we doubled the buffer length, because the control logic and pad occupy about 70% of area in the present chip. Table 2 also shows the specification of the proposed TMC-SSC chip.

Figure 9 shows a block diagram of the TMC-SSC. In the TMC-SSC, we propose to encode 16 bit data to 4 data bits plus one carry bit, and use the system clock of 31.25 MHz (32 ns period). As described in the next section, it is still possible to extract data synchronized with 16 ns trigger signal. The encoding scheme reduces required output pins and data size, and the lower clock frequency ease the chip design and reduce the power consumption.

2.5.1.3 Level 2 Buffer

Figure 10 shows a block diagram of the Level 2 Buffer (L2B). The L2B consists of an encoder logic and a buffer memory, a buffer controller, a bus interface, a TMC control logic, and a trigger control logic. The buffer controller has two pointers and the buffer works like a ring buffer. This chip is a fully digital chip using ASIC's such as gate arrays or standard cells.

In the L2B, the data from the TMC is reconstructed to drift time as shown in Fig.11. Since the maximum drift time of a straw is around 30 ns, several rows of data have to be read out from the TMC for a trigger taking into account of the uncertainty in beam crossing. The L2B reconstructs the drift time from those data. Referring to the phase synchronization of the level 1 trigger signal, the L2B recognizes starting point of the data then calculate the drift time. Although the figure shows only one hit data, but it is possible to process multi hit data.

2.5.1.4 Data Collection Chip

Data Collection Chip consists of several IC's as shown in Figure 5. The CPU moves the data from the L2B to the internal memory, and send it out through the serial I/F by adding information of a trigger number and straw address. The CPU also communicates through the serial network interface for monitoring, calibration, and diagnostic purpose. One of candidates for the CPU is a transputer which has 4 link interfaces and a high-speed external bus interface.

2.5.1.5 Power Consumption of Front-end Electronics

We estimate power consumption for the front-end electronics as shown in Table 3.

Table 3 Estimation of power consumption for the front-end electronics

P/S/D	8 mW/ch
TMC	8 mW/ch
L2B	8 mW/ch
DCC	6 mW/ch
Total	30 mW/ch

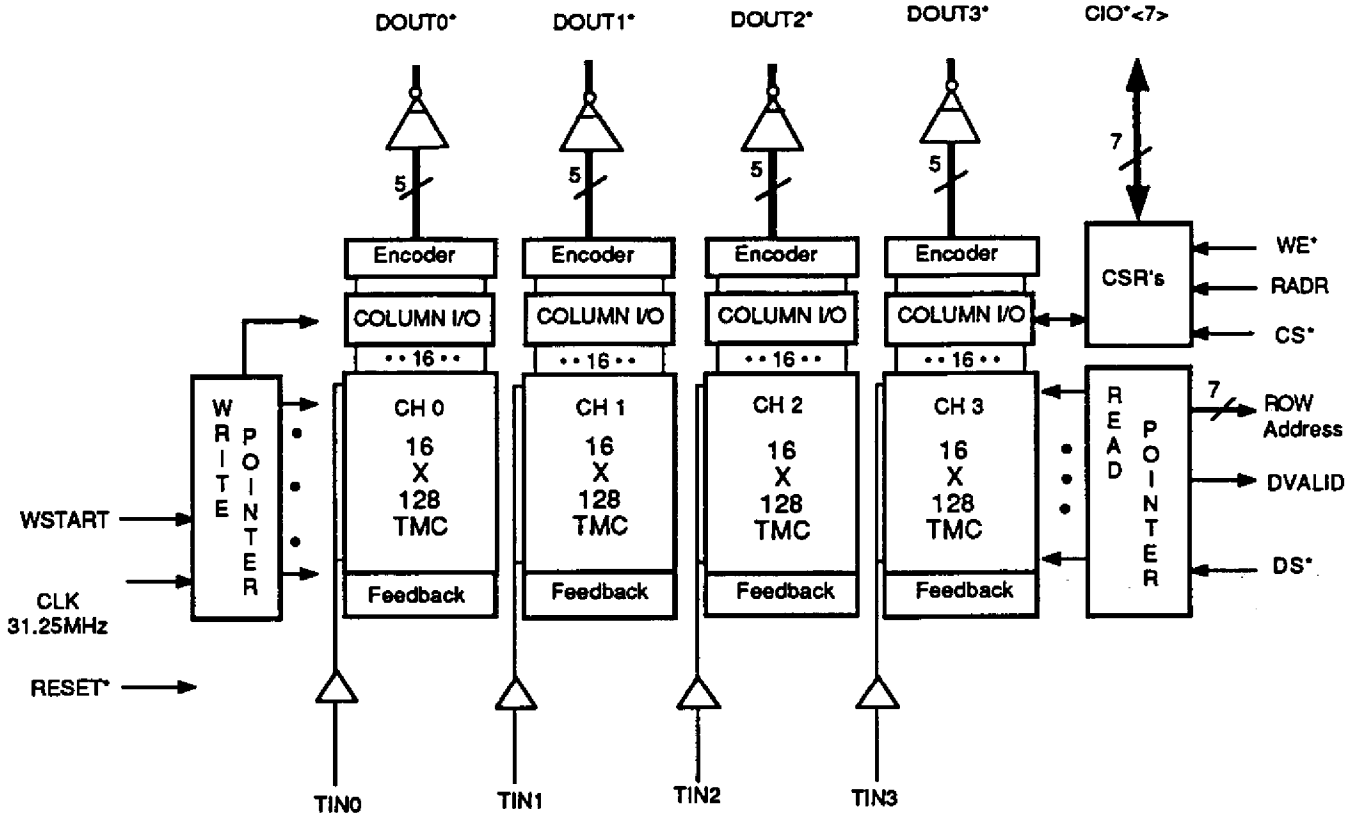

Fig. 9 TMC-SSC Block Diagram

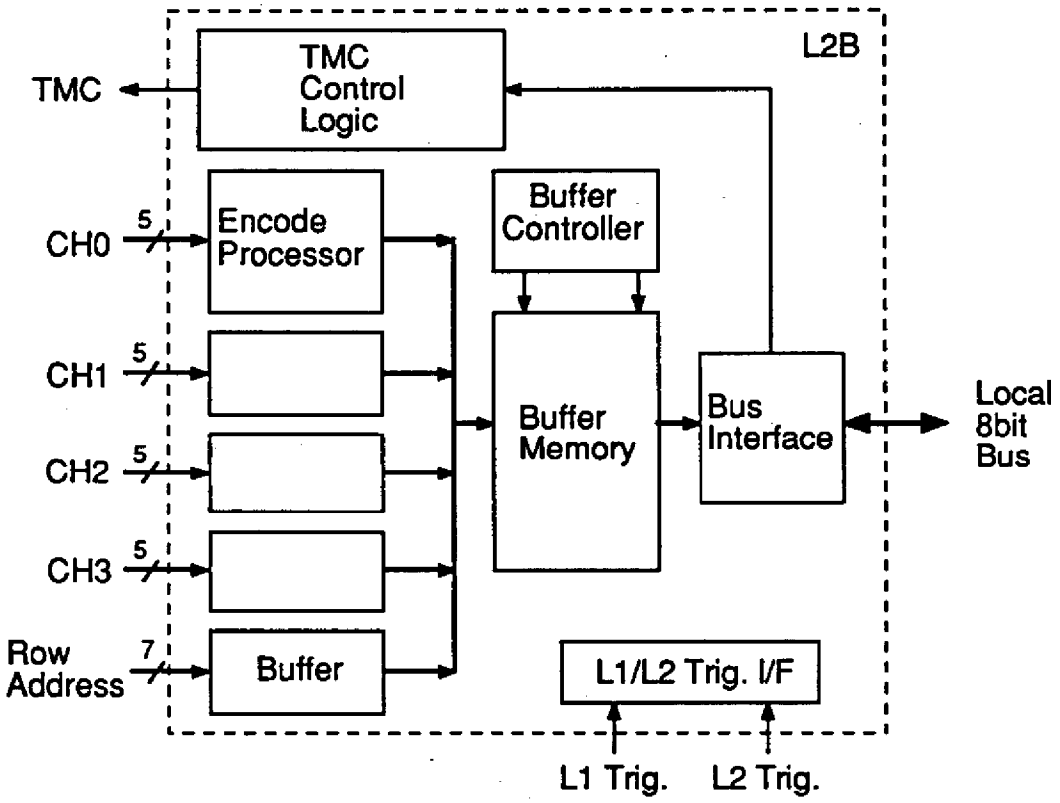

Fig. 10 Block diagram of the TMC Level 2 Buffer Chip

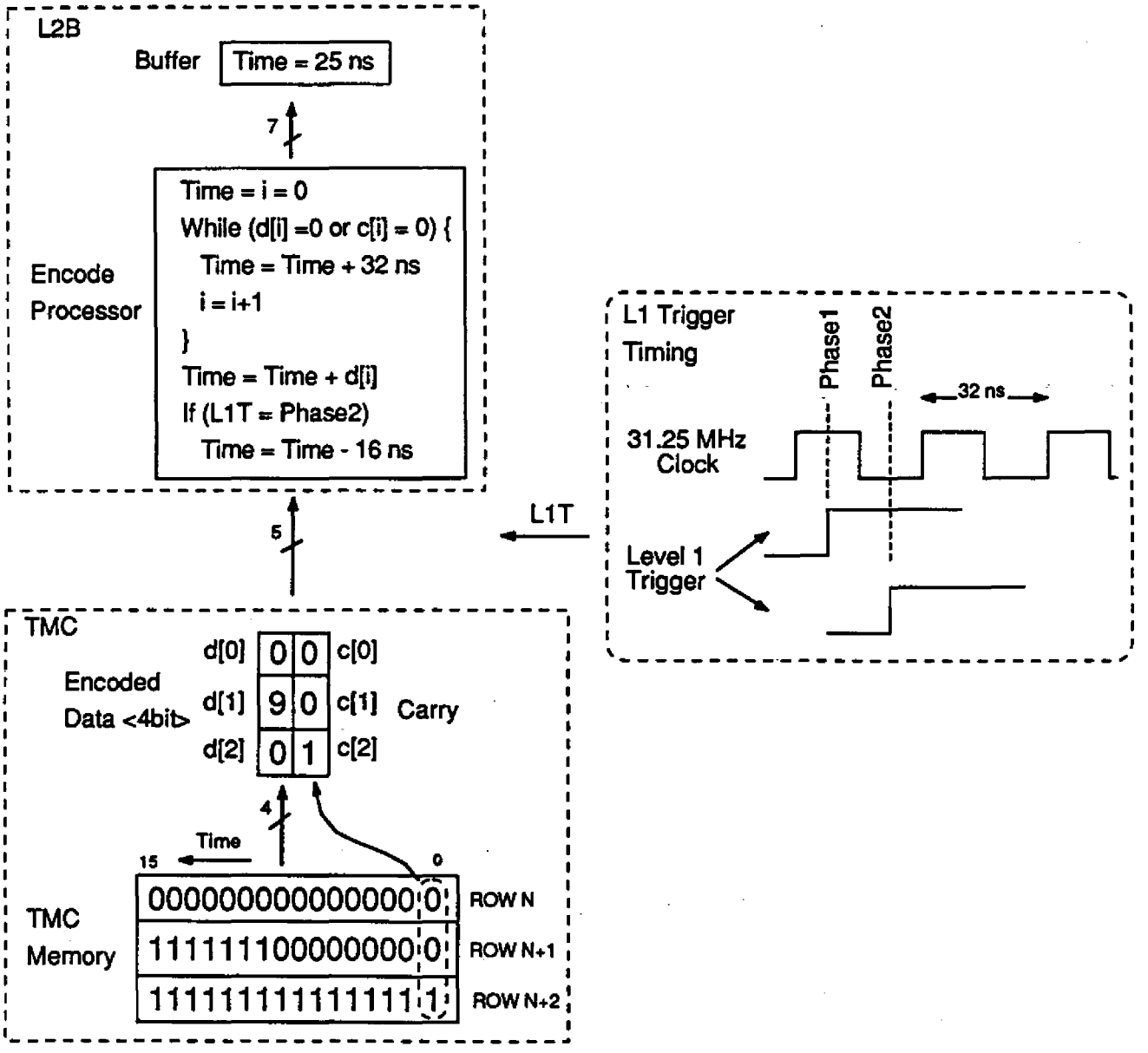

Fig. 11 TMC-SSC & L2B Data Encoding Scheme

The power consumption for the P/S/D as well as for the TMC is based on the working prototype chips. In total, we have a 2 kW heat source at one end. We think this magnitude of power consumption is manageable with a conventional cooling technique.

2.5.1.6 Higher density option

The proposed scheme of the front-end chips shown above is assuming 4 channels per chip and 8 channels in a hybrid. There is no difficulty in increasing number of input channels to 8 for the P/S/D. For the L2B, it seems possible to include 8 channel buffer in a chip, though the number of connections becomes somewhat high.

For the TMC, we have new idea which may possibly shrink the cell size by more than 30 %, and reduce power consumption. This enables us to make a 8 channels chip cost effective.

We continue to work on this option, because this reduces the cost per channels and eases the implementation of the front-end board.

2.5.2 Local Buffer Crate

The Local Buffer Crate (LBC) are placed at outside of the barrel calorimeter as described in the section of packaging. The crate contains 10 MDB modules and one DTX module. Four data cables from the FEB's are connected to one MDB module. The DTX transfers the collected data through optical fiber link with 1Gbps transfer rate.

In this crate, another module such as a clock driver, trigger driver/receiver, etc. may also be inserted.

2.6 Radiation Hardness

The radiation level induced by charged particles is about 10 krad/year at the inner most straw layer, while the neutron flux is an order of 10^{12} neutron/cm^2/year with almost no dependence on location. Thus the front-end electronics must survive for more than 100 krad and 10^{13} neutron/cm^2 radiation. Radiation damage tests are being done for both the bipolar process used in the preamp/shaper/discriminator and the CMOS process used in the TMC chip. The results of radiation damage test of the bipolar process for neutrons and γ-rays are reported in reference 5 and 6. It is shown that the process has radiation hardness up to 1 Mrad and 10^{13} neutron/cm^2.

A radiation damage test for the Co^{60} γ-ray has been done for the CMOS process. We have preliminary results. In power off condition, both PMOS and NMOS transistors show very little change up to 1 Mrad. In power on condition, PMOS shows little difference with power off condition, whereas NMOS transistors showed some degradation at the level of 100 krad.

We need further study about the radiation damage of the CMOS process.

3. Packaging and Layout

As mentioned before, front-end IC's are packaged in a hybrid as shown in Fig. 12-(a). One hybrid takes care of 8 channels. This hybrid is mounted on the FEB. Figure 12-(b) shows an

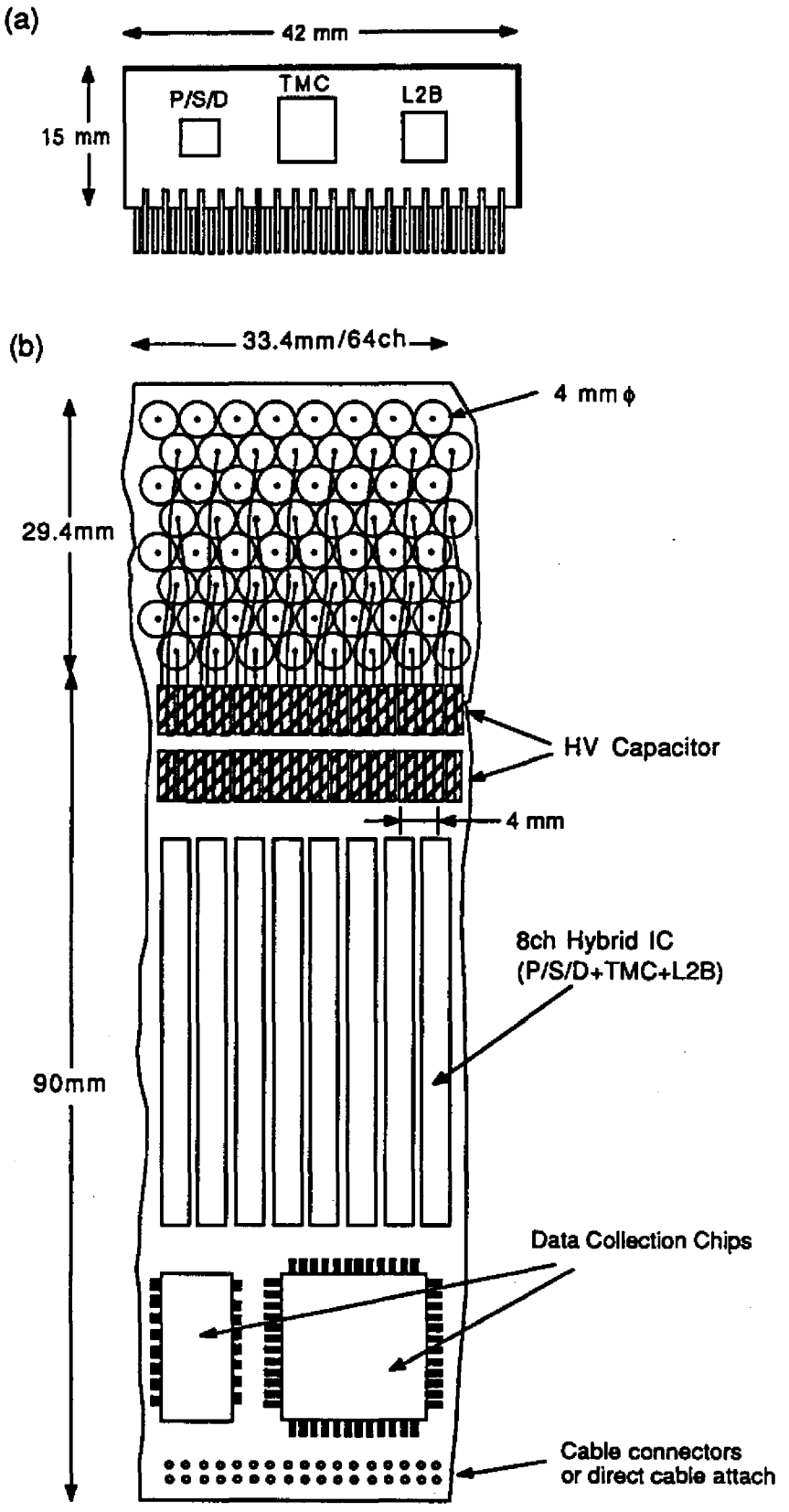

Fig. 12 Mounting Example of (a) the Hybrid IC and (b) the Front-End Board.

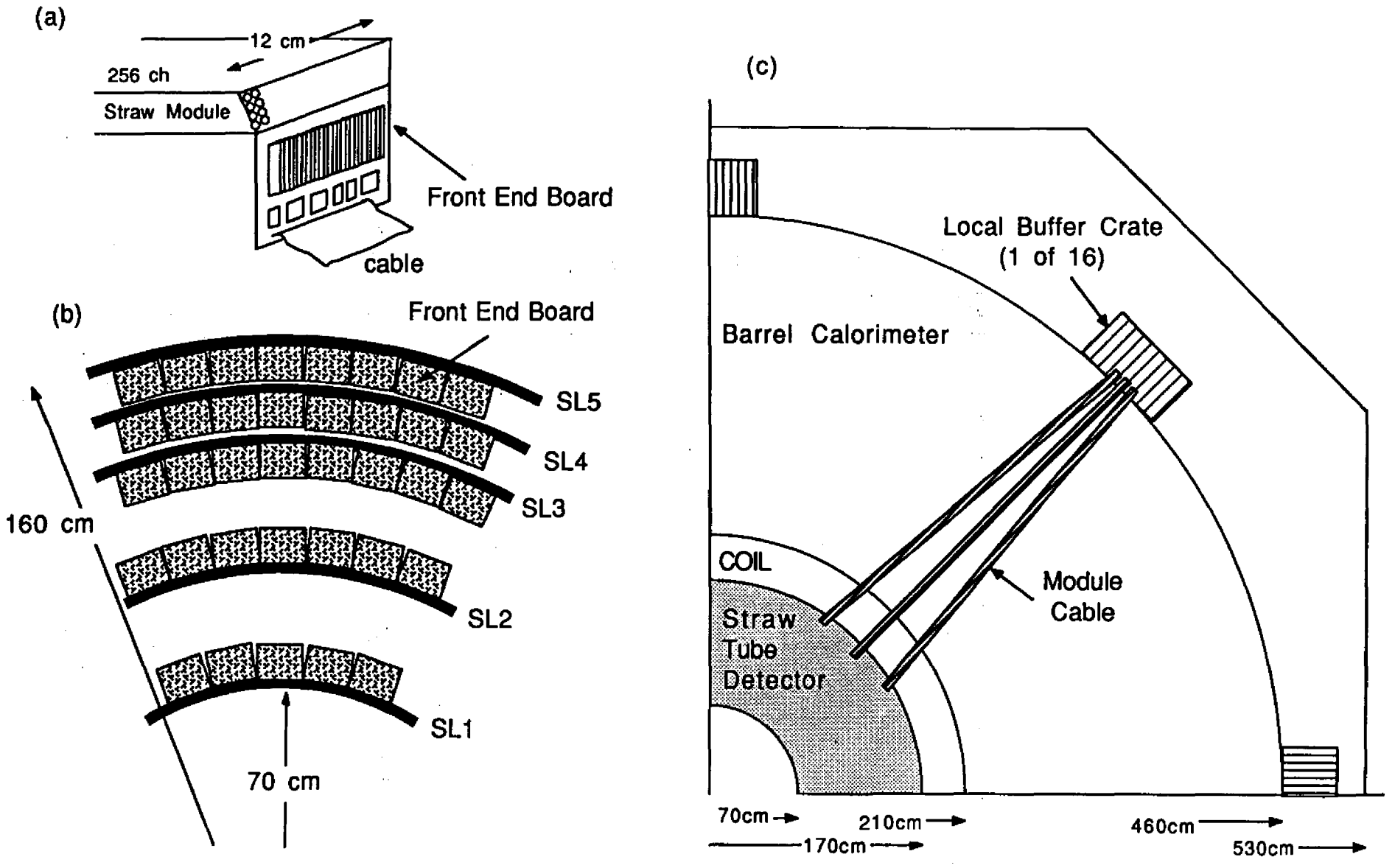

Fig. 13 Physical placement of the Front-End Boards and the Local Buffer Crates.

example of arrange around straw-tube end. Only surface copper lines from straw tube are shown. Another half lines are drawn in the real side. Since the minimum distance between superlayers is 13 cm with the current design of straw tubes, the maximum length used in the FEB is about 9 cm. As a hybrid takes 8 inputs, the pitch of the hybrid is 4 mm if it is implemented in one side. Space after the hybrid is used for the DCC's. Cables are connected with or without connector to the FEB.

Figure 13 shows the mounting scheme of the FEB to the straw superlayer structures. Since the spaces between SL1 and SL2, SL2 and SL3 are more than 30 cm, the front-end boards to the SL1 and SL2 can be mounted upside down to minimize the radiation effects and utilize maximum lever arm for tracker. The Local Buffer Crate is placed at outside of the barrel calorimeter, and module cables are connected between the MDB and the FEB.

4. Cost Estimate

Table 4 shows our cost estimate for the main parts. Cost for the FEB does not include IC's and HV capacitor listed in the table. Cost for other boards (MDB, DTX, etc.) includes all the part's cost used in the board. No R&D money is included in the table but it contains contingency. Total cost for 135k channels is about $8.7 M, or $65/channel.

Table 4 Cost estimate for the straw-tube electronics

Item	Channel/parts	Cost/parts ($)	Cost/ch ($)	Total Cost (k$)
HV Capacitor	1	3	3	405
P/S/D	4	20	5	675
TMC	4	60	15	2,025
L2B	4	40	10	1,350
Hybrid Packaging	8	60	15	2,025
DCC IC's	256	1,000	4	540
FEB*	256	1,000	4	540
Cables	256	1,000	4	540
MDB	1,024	3,000	3	405
DTX	10,240	4,000	0.4	54
LBC with P.S.	10,240	4,000	0.4	54
optical fibers	10,240	2,000	0.2	27
SCP	25,000	10,000	0.4	54
Total			64.4	8,694

(*) exclude cost of parts listed above.

5. Crucial R&D

Most crucial R&D is a radiation damage test for the front-end electronics. There is no problem for bipolar process used in the preamp, etc. The CMOS process used is relatively radiation hard compared with commercial ones, but still need further studies.

Another crucial R&D is high density readout. Although the packaging seems to be not so difficult with present technology, the system deals with small analog signal and high-speed digital signal in a very limited space. Cross-talks and oscillations must be carefully minimized or eliminated.

Most of the parts used in our scheme is based on very conservative design. Although it will take long time to develop and debugging each module, we think there is no crucial item in implementing data acquisition modules.

6. Schedule

Table 5 shows possible development schedule. Each front-end IC requires two prototype productions before the final mass production. The most of the mass production will be done in 1996. Final assembly test with straw-tube detector will be done in 1998.

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Table 5. Straw-tube Detector Electronics Development Schedule.

Item	'91	'92	'93	'94	'95	'96	'97	'98	'99
TMC(1st)	Design		Fabrication	Test					
(2nd)				Modify	Test				
(final)						Mass Product			
P/S/D (1st)		Design	Fabrication	Test					
(2nd)				Modify	Test				
(final)						Mass Product			
L2B(1st)		Design	Fabri	Test					
(2nd)				Modify	Test				
(filnal)						Mass Product			
Hybrid			Design	Test	Design	Test	Mass Product		
FEB				Design		Test	Mass Product		
small system test				Test					
module assembly								Assembly	Test
MDB				Design	Test	Mass Product			
DTX				Design	Test		Mass Product		
SCP					Design	Test	Mass Product		
Data Transfer test					Small System Test			Full system	Test

A CMOS 4CH x 1K TIME MEMORY LSI WITH 1 NS/BIT RESOLUTION

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Abstract - A 4-channel 1024-bit Time-to-Digital Converter chip, which records input signals to memory cells at one nano second intervals, has been developed. To achieve one nano second precision, the chip incorporates a feedback stabilized delay element. The chip was fabricated on a 5.0 mm by 5.6 mm die using 0.8 μm CMOS technology. It dissipates only 7 mW/channel under typical operating conditions.

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I. Introduction

Particle detectors for future high energy accelerators have demanding requirements for time-to-digital conversion. A VLSI circuit designed specifically for this application is an efficient way to meet the requirements. The circuit must achieve 1 ns resolution, and it must maintain the history of the input for more than 1 μs pending receipt of a readout trigger. The readout must not create dead time. As more than 100,000 channels of the time-to-digital electronics will be mounted in the very limited space of a detector, the chip must be high density and low power. Furthermore the device must not deteriorate in the ambient flux of particles and γ rays that is present in the vicinity of the detector.

The idea of Time Memory Cell (TMC) was proposed by us and tested by making a TEG chip [1]. The cell utilizes low-power and high-density characteristics of a CMOS memory cell and gate delay time. Figure 1 shows the basic operation of the TMC. As the write signal (WL) timing in each TMC cell is delayed by 1 ns, timing information of the input lines (TIN and TIN*) is recorded to memory cells sequentially. To keep the delay time constant, the delay time of the delay element is controlled through the Vg line by a feedback circuit which refers to an external system clock period.

In an alternative approach described by Stevens et al. [2] the timing information is stored in a switched capacitor array and digitized much later. Our approach depends much less on small signal analog electronics and is therefore preferable in the detector environment where levels of radiation and electrical noise may be high.

A new TMC LSI chip (TMC1004) has been developed using an 0.8 μm CMOS process. It contains 4 channels and each channel has 1024 TMC cells (32 rows and 32 columns). The chip achieves more than 10 times the density of a 1 GHz GaAs shift register [3] while dissipating less than 1 % of the power.

II. Time Memory Cell Technique

A. Concept

A GaAs shift register clocked at 1 GHz would provide the 1 ns precision that we require, but the power dissipation of this technology is unacceptably large. Therefore we sought to accomplish our objectives in CMOS technology for which the power dissipation is intrinsically low.

In CMOS circuitry the objective of low power is further served by use of a low clock frequency and minimization of data transfers from gate to gate. The difficulty with CMOS where timing is critical is that the propagation delay of a gate may vary by more than 20 % because of fluctuations in chip processing, supply voltage, and temperature. However, the delay time of a gate which has a same physical layout is fairly uniform within a chip. We make a feedback circuit which controls delay time of the series of gates, and eliminate the process, voltage and temperature variability.

In one channel of a TMC1004 chip, 1024 TMC cells are configured as 32 rows of 32 cells. Within a row the input is written to successive cells at intervals of approximately 1 ns. The rows are successively enabled for writing by an external clock with period 32 ns.

B. Feedback circuit

The principle of our feedback circuit is analogous to the principle of a phase locked loop (PLL). Whereas a PLL stabilizes an oscillator frequency by referencing to the phase of an external clock, the TMC feedback stabilizes a variable delay element by referencing to the period of an external clock.

Figure 2 shows the schematic of the feedback circuit. When an external clock (ϕ_1) sets the flip-flops F1 and F2 at its falling edge, capacitors C1 and C2 begin to charge. The charging of C1 stops at the falling edge of the pulse from the end of the reference row. The charging of C2 stops at the next falling edge of the clock pulse (ϕ_2). Hence, the voltage difference between C1 and C2 is proportional to the time difference between the delay line and clock period. Comparator A1 checks the voltage difference and adjusts the feedback voltage (Vg). If the delay time is less than the clock period, C3 charges during a store period increasing the delay of the delay line. If the delay time is longer than the one clock period, C3 discharges reducing the delay.

C. Timing Accuracy

We give here a rough estimate of the timing accuracy attainable by the TMC circuit. There are three main sources of error; the input and clock signals, the feedback circuit, and the non-uniformity of the delay element. In the following discussion, we assume the error distribution has the Gaussian shape, and use the word "error" as the standard deviation of the distribution.

Time jitter of the input and the clock (write) signals arise when those signals pass through buffers (see Fig. 3-(a)). We assume time jitter of 50 ps for the signal passing a buffer. Since we are using about 20 buffers between input pad to a TMC cell, the total time jitter is summed in quadrature, and will be $\sqrt{20}$ x 50 ps = 0.2 ns.

The signal jitters in the write line (WL) is accumulated from the first cell to the last cell in a row. In the last cell this jitter becomes $\sqrt{32}$ x 50 ps = 0.3 ns. By averaging the jitter in a row, it becomes 0.2 ns/bit.

Although those buffers have variation of delay time caused by the change of supply voltage and temperature, the delay variation for input and clock line is cancelled each other by designing the number of buffers from input to the TMC cell to be the same.

The errors in feedback circuit come from sensitivity of the comparator and controllability of the feedback voltage (see Fig. 3-(b)). Since the input voltage of the comparator changes 1.5V for 32 ns period (= 50 mV/ns), and the comparator detects ±25 mV voltage difference from the reference voltage, the sensitivity of the comparator is ±0.5 ns / 32 ns (= ±1.5 %), so the effect of this error to each bit can be neglected. Since the adjustment of the feedback voltage is < 20mV per feedback cycle, the corresponding delay time change is less than 30 ps / cycle. Thus this error can also be neglected.

Non-uniformity of the delay element may cause difference of delay time between reference row and actual row, and causes discontinuity in data between row. If there is 5% non-uniformity in delay time of each delay element, the discontinuity will be $\sqrt{32}$ x 0.05ns = 0.3 ns. Also the non-uniformity appears as differential linearity error.

In addition to these errors, digital conversion device has digitization error intrinsically. For 1 ns digitization step the digitization error σ_{dig} is $1 / \sqrt{12}$ = 0.29 ns. From these considerations, it may be possible to make the device which has the timing error of $\sigma \sim 0.5$ ns.

III. Circuit Description

A. Circuit Block

A Block diagram of the TMC1004 is shown in Fig. 4. The chip has four TMC arrays, each with 32 rows by 32 columns of TMC cells. Each array has a feedback circuit. For accessing the four

arrays, there are two pointers Write and Read each of which consists of a 7-bit counter and decoder. The Write Pointer is incremented in each clock (CLK) cycle which initiates a pulse in the write line of the designated row. The Read Pointer selects a row for readout and is incremented by the same clock (CLK). This scheme with two pointers and dual port cells enables read and write operations to proceed simultaneously. The four TMC arrays can be configured as 4, 2, or 1 channels by setting external pins. The 4, 2, and 1 channel modes utilize respectively the lower 5, 6 or 7 bits of the counters and retain the input history for 1, 2 and 4 μsec.

The 32 bits of row information are encoded to 6 bits at readout time so as to reduce the data size and the required number of leads to the chip.

The chip maintains various parameters in three control and status registers (CSR) which can be read as well as written.

B. Time Memory Cell

The schematic of the TMC cell is shown in Fig. 5. Each cell has one timing-information write port (TIN and TIN*) and one data-read/write port (BL and BL*). We used static memory in the TMC cell, because it may be more stable for radiations than the dynamic one. Two PMOS transistors (M1 and M2) are added to the previous design [1]. They make the write operation insensitive to the previous contents of the cell by interrupting the feedback paths during the write pulse. Transistor parameters of the delay element were selected to obtain a gate delay time close to 1 ns/bit.

The delay time of the delay element is controlled by the PMOS transistor M3. Since the input signal is latched in memory cell at the falling edge of the signal on WL', only the falling edge is controlled via the feedback voltage Vg. The transistor M3 changes the rise time of the signal at node A. At the input to the second inverter the pulse width changes and at its output the regenerated signal edge is again sharp.

C. Feedback Circuit

The operation of the feedback circuit was described in previous section. Figure 6 shows the result of simulation of the delay element. With Vg fixed the delay varies by more than ±20% with changes in power supply voltage (2.7 V ~ 3.3 V), temperature (27 °C ~ 70 °C), and transistor

threshold voltage (-10% ~ +10%). With Vg controlled by the feedback circuit (1.2 V ~ 2.3 V), the delay time is kept at 1 ns.

D. Encoder

The 32-bit row data is encoded to 6 bits. Since transition times are spaced by at least 32 ns in our application, the encoder logic accommodates only one "0" to "1" transition in a row of memory. Thus the encoding reduces the output pin requirement and the amount of data without sacrificing data quality. Table 1 shows the encoding scheme. The most significant bit shows the value of the first bit of a row, and the remaining 5 bits show the position of the first "0" to "1" transition.

E. Readout Pipeline

Simultaneous reading and writing require that the operations proceed in phase so that the memory operates as a ring buffer. One row must be read out during each 32 ns interval in which a row is written. The readout cycle (memory read and encoding) is pipelined to two stages and the cycle continues while the trigger signal DS* is asserted. The data are presented on the DOUT lines.

F. Control registers

There are three CSR registers which set / show the operating mode and the settings of the pointers. Two bits of CSR#0 encode the operating mode, and four bits provide serial access to the cells of the TMC arrays. This access path is used for testing each TMC cell. The Read Pointer can be written and read via CSR#1 and the Write Pointer via CSR#2. The CSR register is accessed through the CS* and the CIO lines.

III. Measured Performance

The specifications for the TMC1004 are summarized in Table 2. Each item is discussed below.

A. Linearity

Figure 7-(a) shows the linearity curve of the TMC1004. As the chip is referencing an external quartz oscillator (31.25 MHz), the slope of the linear fit to the data (time-to-digital conversion

factor) is very stable and has the value of 1.000 ± 0.001 bit/ns without any tuning. The integral linearity error (Fig. 7- (b)) is the deviation from the ideal response function. A Gaussian fit to the integral linearity error distribution shows $\sigma = 0.31$ ns, and the maximum deviation is less than 1.5 ns.

Figure 8 shows the fine structure of the linearity curve. The first part of the row has a nearly ideal response to input, but in the latter part of the row the response is rather broad. This trend reflects the accumulation of jitter along a row and the resynchronization at the start of the next row. Making the rows shorter could reduce the integral linearity error but at the cost of increased power dissipation.

Figure 9 shows the differential linearity error. We get $\sigma = 4\%$ from Gaussian fit to the data and maximum deviation is less than 20 %. This indicates the non-uniformity of the delay element is around 4%.

We observed discontinuity in data is less than 0.5 ns for row-to-row, and less than 1 ns for TMC array-to array.

B. Stability

While the chip has non-negligible amount of integral and differential errors, its overall characteristic is very stable. Figures 10-(a) and (b) show the variation in slope with voltage and temperature for a channel. The variation is plotted as a deviation from the data point of 3.0V and 25 °C. Due to the feedback circuit, the slope is stable within 0.1% for voltage variation of 2.6 - 3.4 V and temperature variation of 15 - 55 °C.

C. Power Consumption

The most power consuming part of the chip is a sense amplifier circuit. There are 128 sense amps on a chip, one for each column of each channel. To minimize power dissipation, the DC current to the sense amps is normally held off and is raised only when a readout trigger arrives. With the feedback circuit operating, the power dissipation is about 3 mW/ch in 4 channel mode. When continuous write operation starts, the power dissipation increases to about 6.5 mW/ch. Finally, during readout the power dissipation increases by 24 mW/ch. With a readout duty factor of 1 % as expected in a typical operating environment, the average power dissipation is 6.7 mW/ch

D. Time Resolution

Figure 11 shows results of time resolution measurement. In this measurement, the deviation from ideal response line is measured and plotted. Gauss fit to the data shows $\sigma_{total} = 0.52$ ns. Assuming the σ_{total} is the quadrature sum of digitization error ($\sigma_{dig} \approx 0.29$ ns) and the TMC error (σ_{TMC}), we get $\sigma_{TMC} \sim 0.46$ ns. This value is in good agreement with the our rough estimate in section II.

E. Layout

Figure 12 shows the photograph of a TMC1004 chip. Four TMC arrays are arranged in quadrants. Control logic is placed in the cross shaped area separating the arrays. The chip was designed by full-custom layout, and the size is 5.0 mm by 5.6 mm.

IV. Summary

A new time-to-digital converter chip, the TMC1004, has been designed. It has 1 ns/bit least count and can record for up to 4 μs. A novel variable delay element and a feedback circuit are employed to get 1 ns accuracy. Power consumption is very low due to the CMOS static memory-like structure. Tests show that overall linearity and stability are very good. This chip is designed for time-to-digital conversion chip, but the methods used to get 1 ns timing and to record to memory can be adapted to other applications such as a memory for recording high-speed signals.

Acknowledgments

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[2] A. Stevens et al., "A Time-to-Voltage Converter and Analog Memory for Colliding Beam Detectors", IEEE J. Solid-State Circuits, vol. SC-24, no. 6, pp. 1748-1752, Dec. 1989.

[3] O. Sasaki et al., "1.2 GHz GaAs Shift Register IC for Dead-Time-Less TDC Application", IEEE Trans. on Nucl. Sci. Vol. 36 (1989)512.

Table 1 Data Encoding scheme

Bit Pattern	Encoded Data
3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0	5 4 3 2 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0	0 0 0 0 0 1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 0	0 0 0 0 1 0
:	:
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 0 0 0 0
(not appear)	1 0 0 0 0 1
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 1	1 0 0 0 1 0
x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1 0 x 1	1 0 0 0 1 1
:	:
1 0 x x x x x x x x x x x x x x x x x x x x x x x x x x x x x 1	1 1 1 1 1 1

x..xx..x = 0..01..1

Table 2.TMC1004 Specifications

No. of Channels	4 channel
Least Time Count	1 ns / bit
Time Range	1.024 μs (4 ch), 2.048 μs (2 ch) or 4.096 μs (1 ch)
Clock Frequency	31.25 MHz
Time Resolution	σ = 0.52 ns
Integral Linearity Error	σ = 0.3 ns (< 1.5 bit)
Differential Linearity Error in a row	σ = 0.04 ns (< 0.2 bit)
row-to-row Discontinuity	< 0.5 bit
TMC array-to-array Discontinuity	< 1 bit
Variation of Slope (time-to-digital conversion factor)	< 0.1 % (2.6 - 3.4 V) < 0.1 % (15 - 55 °C) < 0.1 % (chip to chip)
Data Output	32 ns cycle 2 stage pipeline. 6 bit encoded output.
No. of Pins	54 I/O pins and 34 Power / Gnd pins
Supply Voltage	3.0 V
Power Consumption	7 mW/ch for 1 % readout duty factor.
Chip size	5.0 mm x 5.6 mm

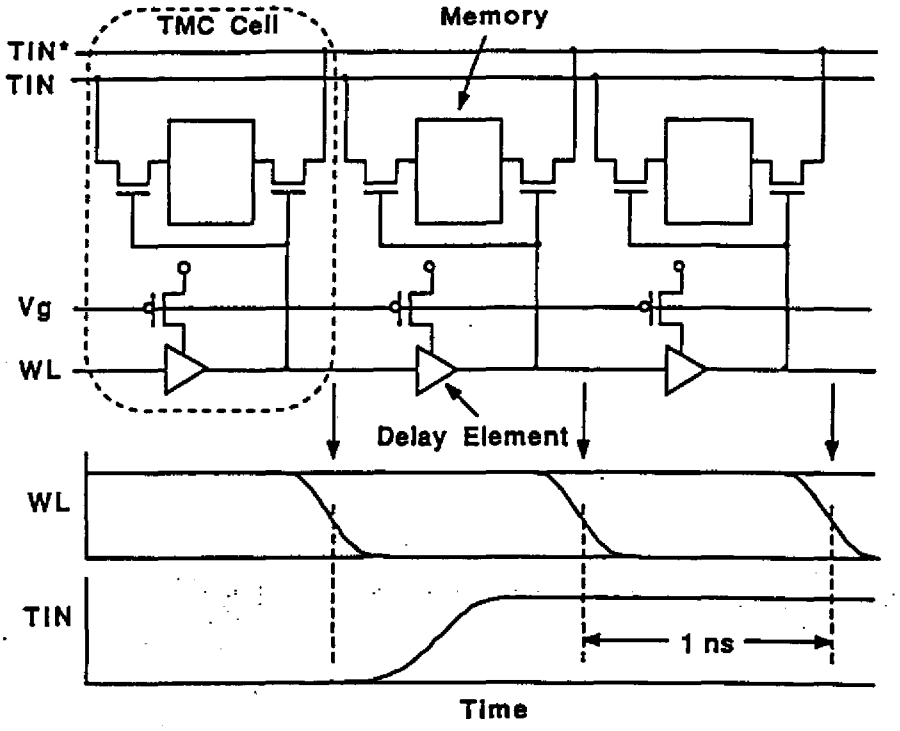

Fig. 1. Input timing write operation in the TMC cells.

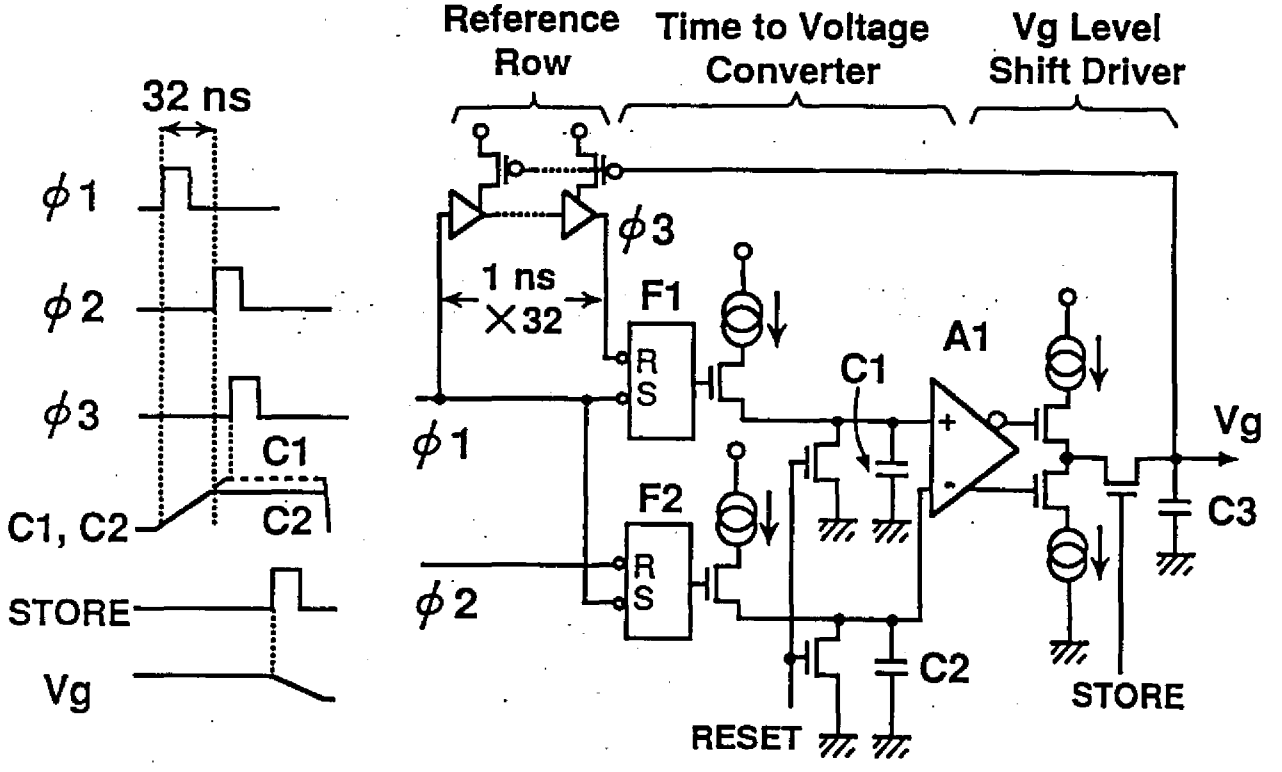

Fig.2. Feedback circuit.

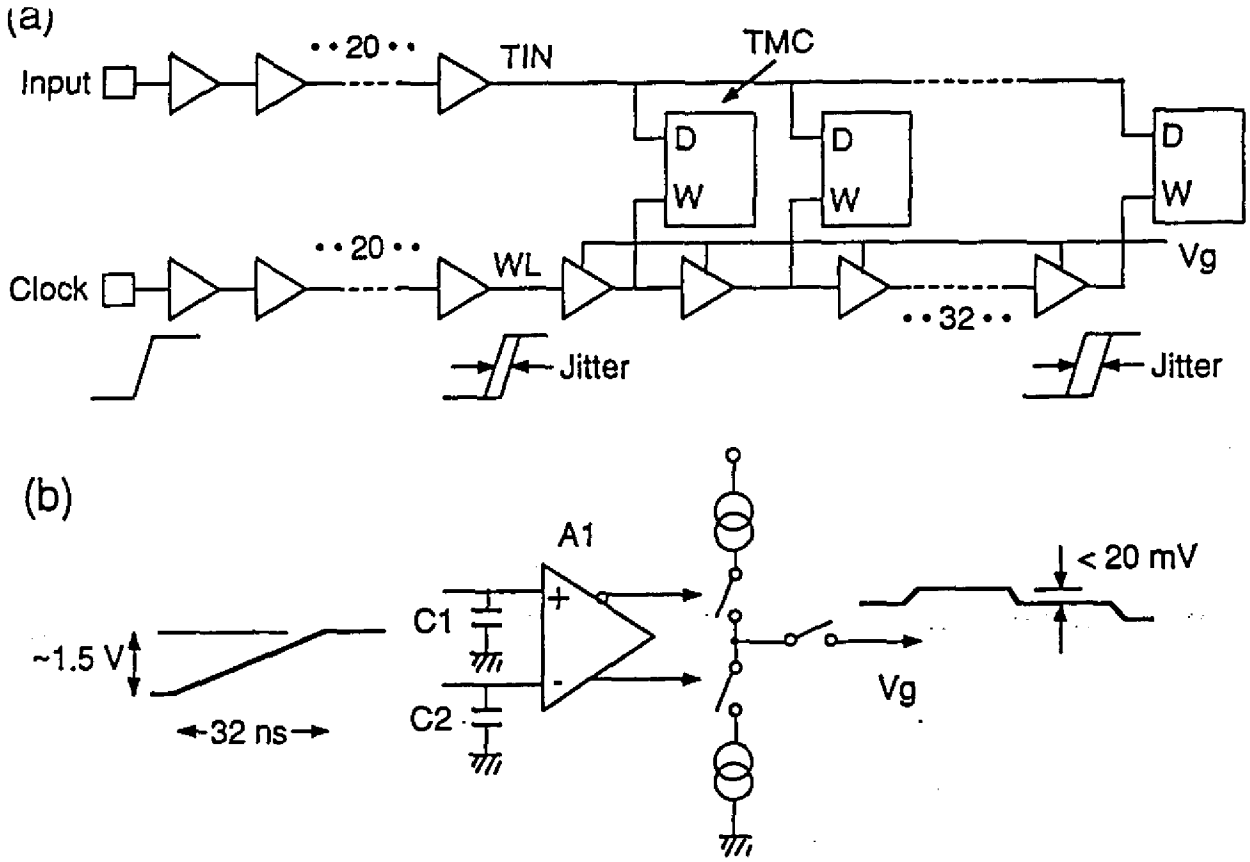

Fig. 3 (a) Signal jitter in the TMC circuit. (b) Signal Level in the feedback circuit.

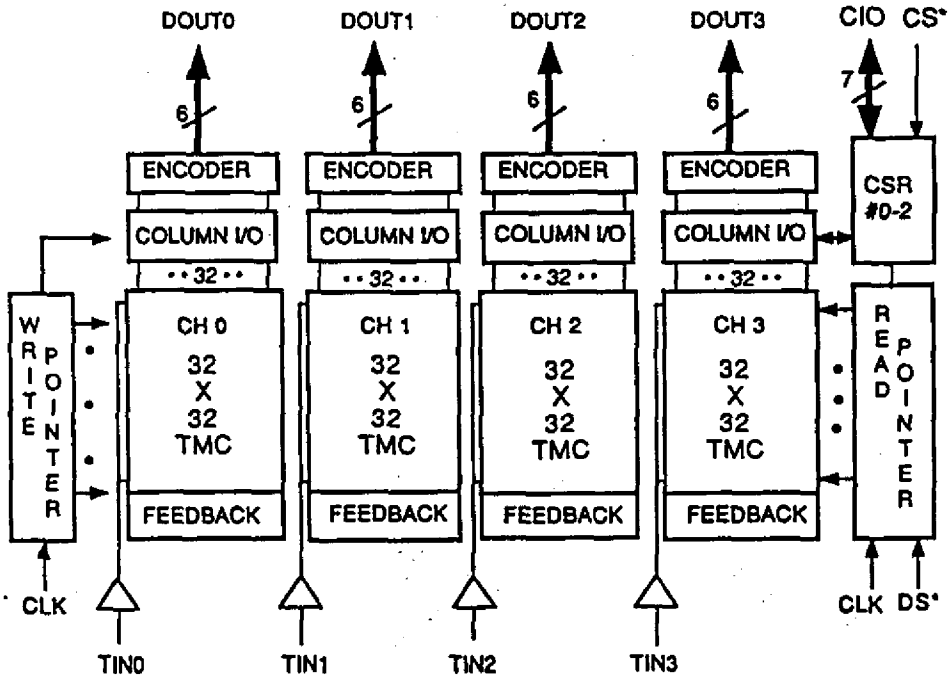

Fig. 4. Block diagram of the TMC1004.

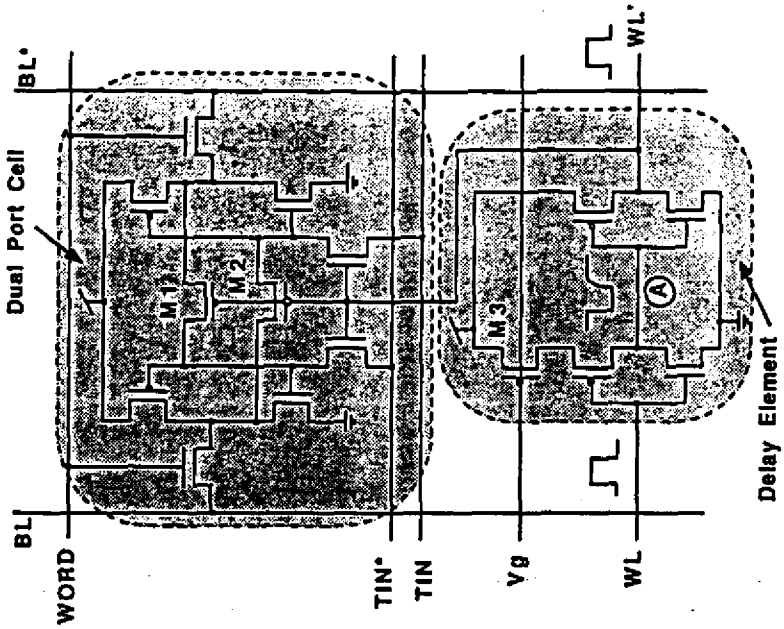

Fig. 5. TMC cell circuit.

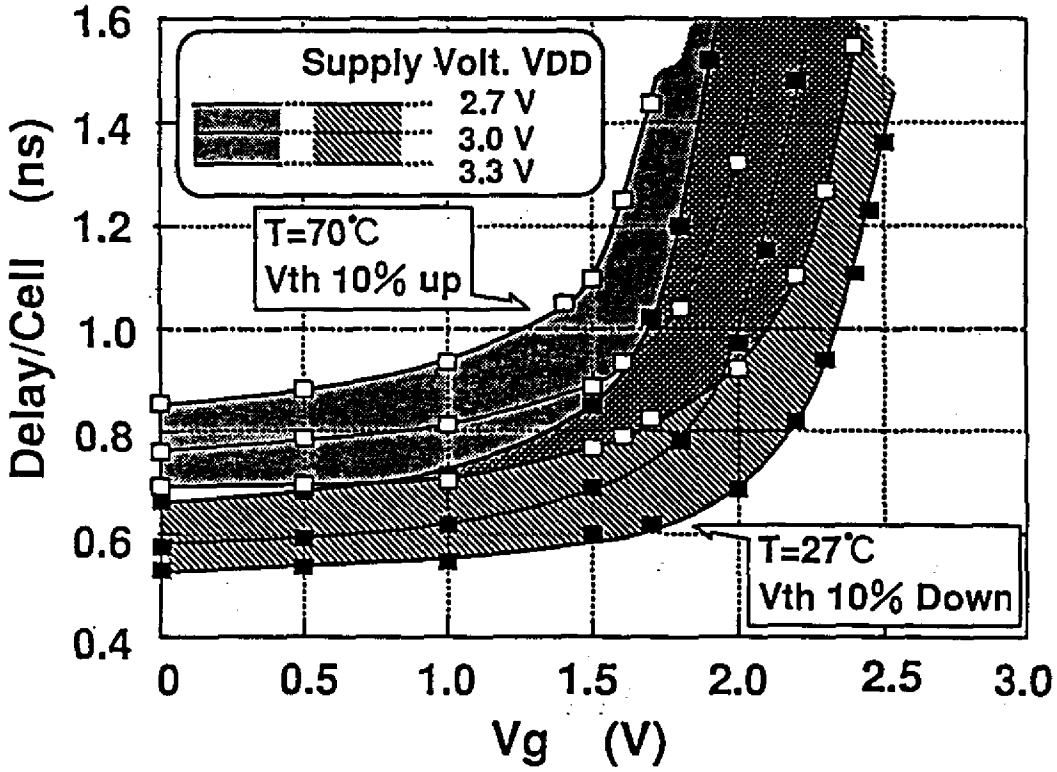

Fig. 6. Simulation of the delay time for the delay element.

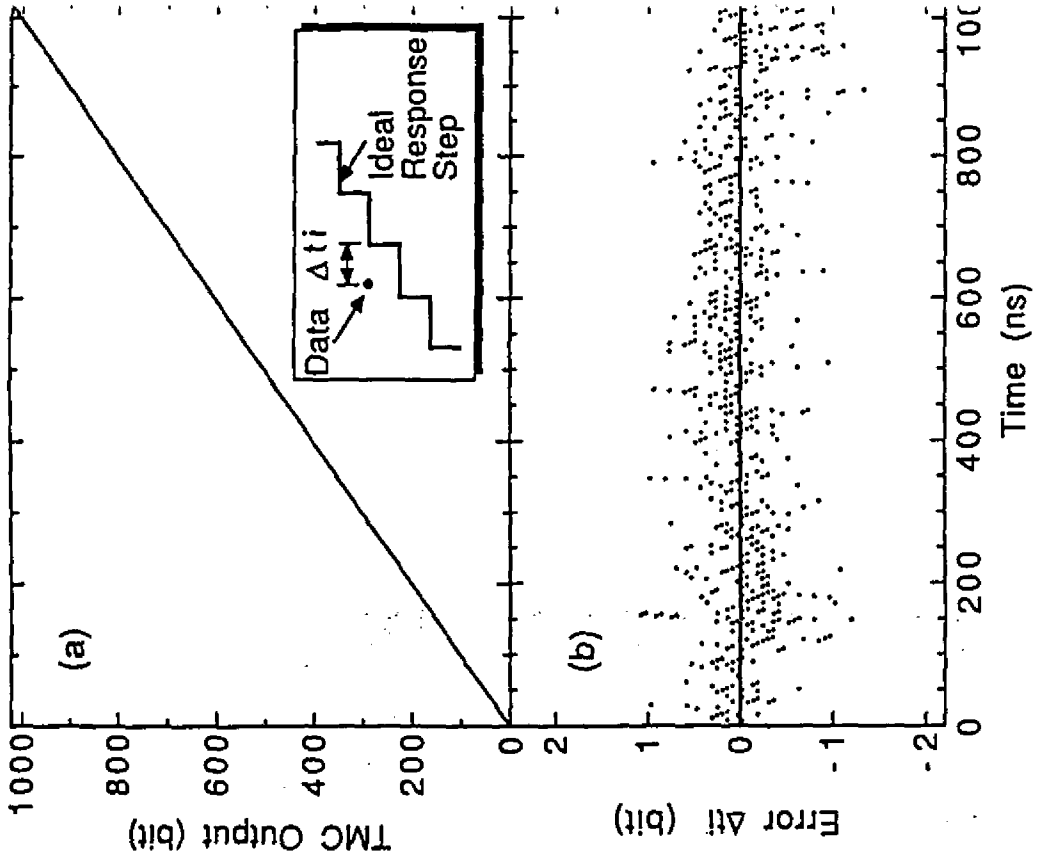

Fig. 7. (a) Linearity curve of the TMC1004. (b) Integral linearity error of the TMC1004. D taken for 0.61 ns step and 1672 points.

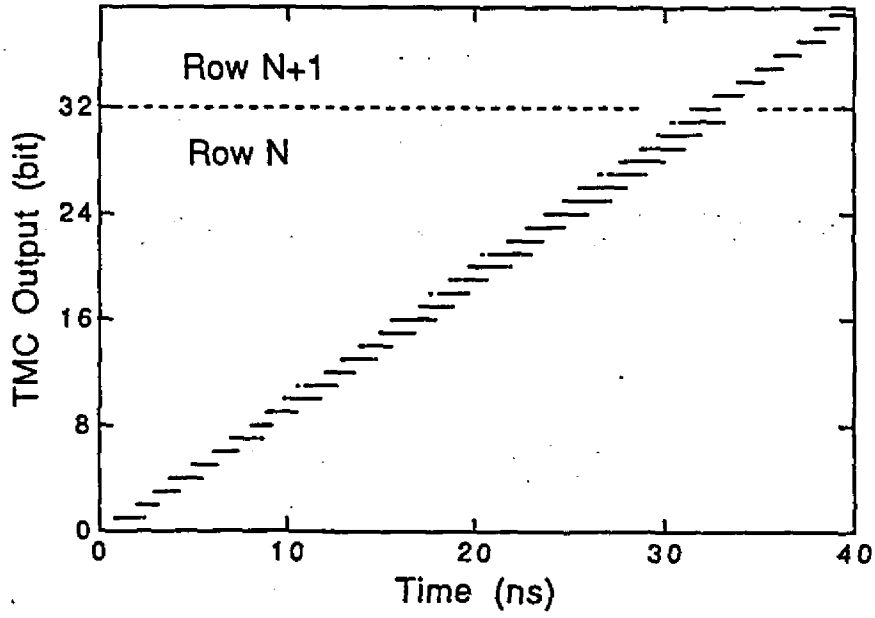

Fig. 8. Fine structure of the linearity curve. Output bits of 0 to 31 correspond to row N, and bits above 31 correspond to row N+1.

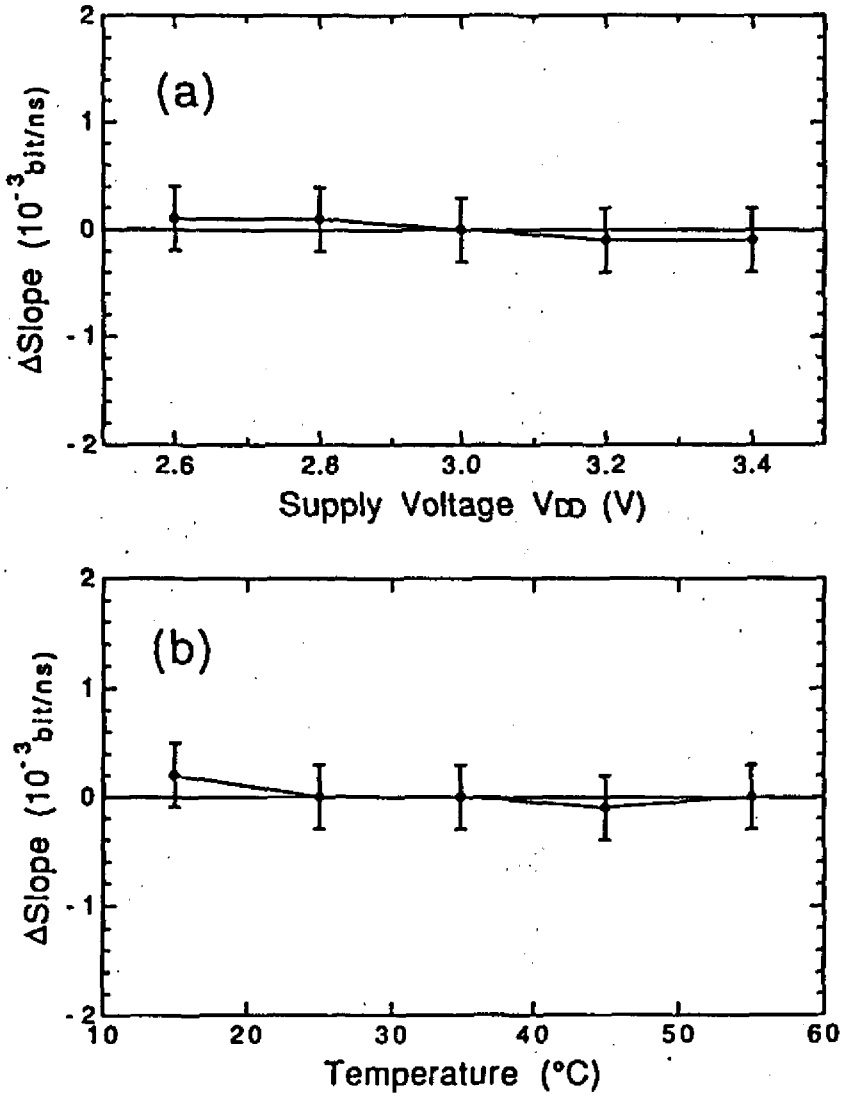

Fig. 10. (a) Slope variation for supply voltages between 2.6 V to 3.4 V. (b) Slope variation for temperature change from 15 °C to 55 °C. The data are plotted as a deviation from the data point of 3.0 V and 25 °C.

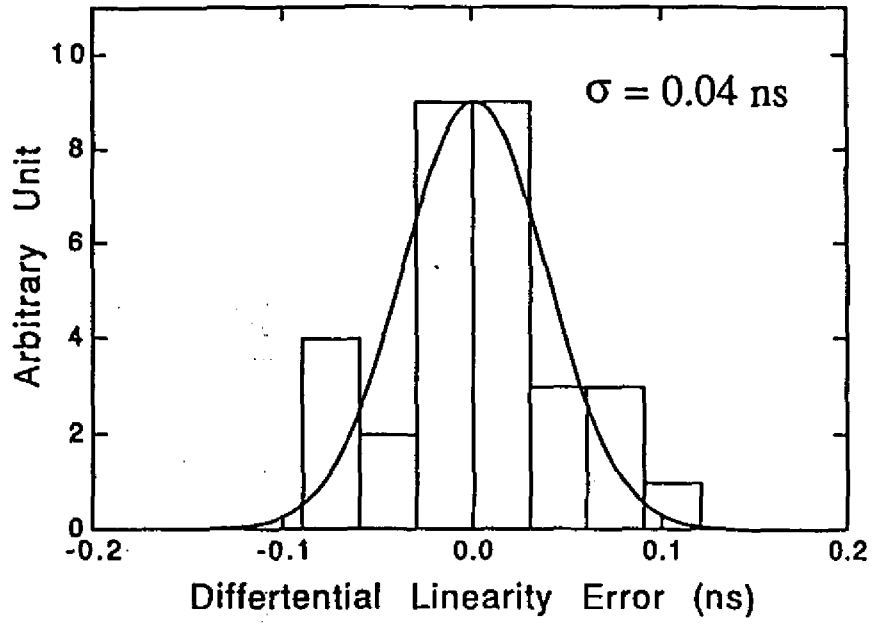

Fig. 9 Distribution of differential linearity error.

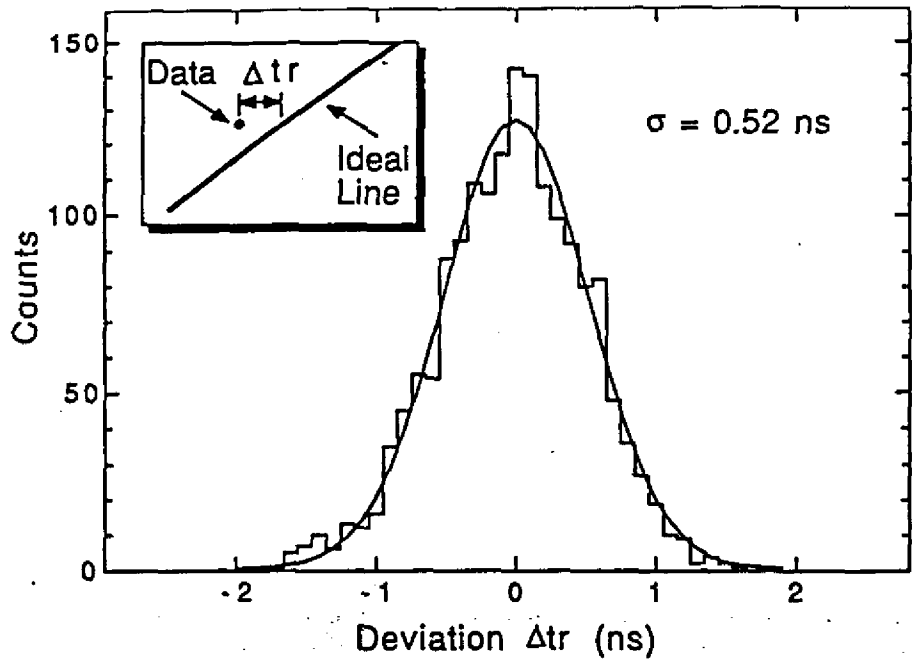

Fig. 11 Time resolution measurement. The deviation from ideal line includes both the digitization error and the TMC error.

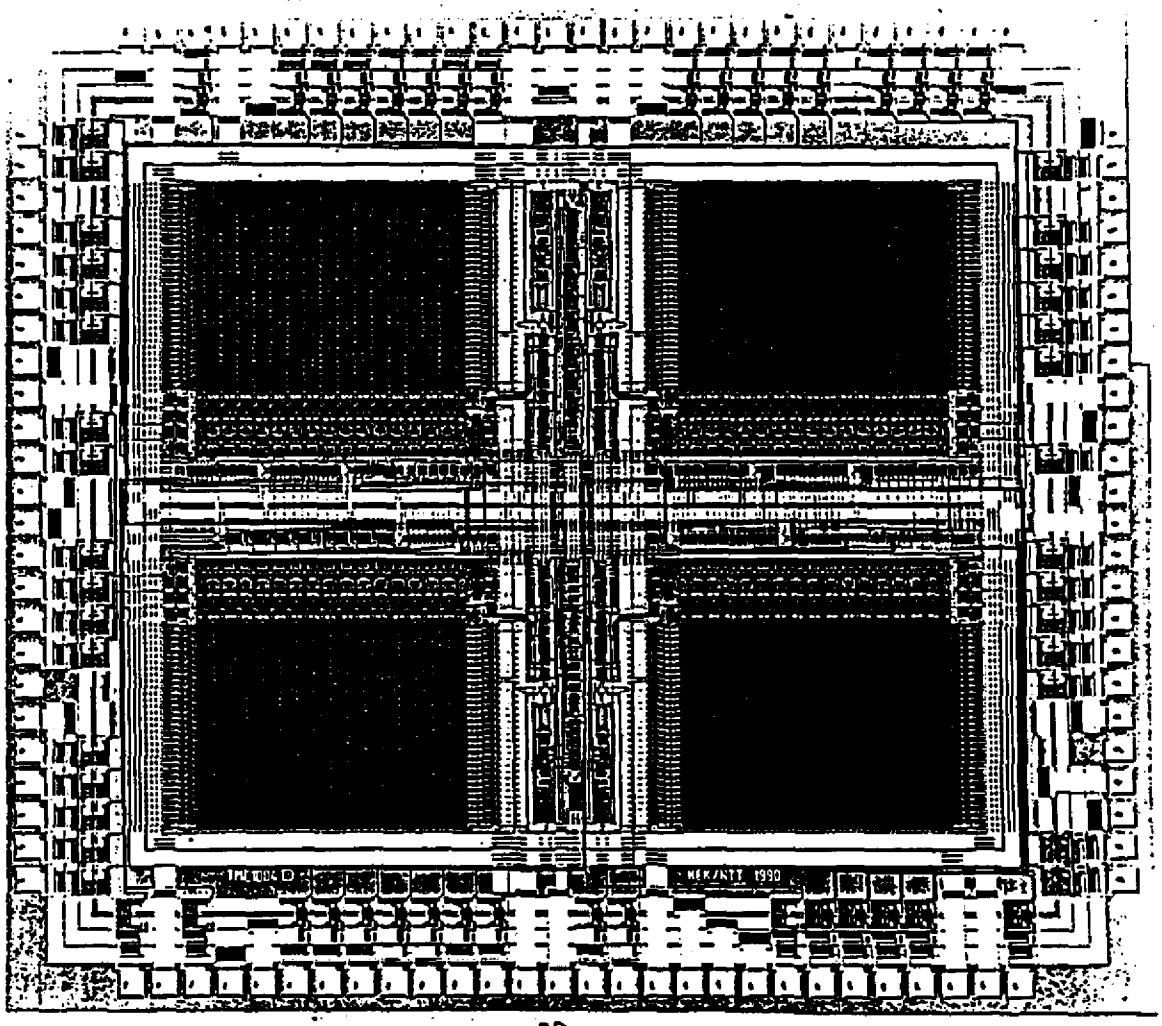

Fig. 12. Photograph of the TMC1004 chip.