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SOLENOIDAL DETECTOR NOTES

FRONT-END ELECTRONICS MEETING
AT LBL JUNE 6-8, 1990

Front-End Electronics Meeting at LBL June 6 - 8, 1990

Recent Developments in Ionization Calorimetry	V. Radeka (BNL)
JFET Developments: Devices, Monolithic Amps	S. Rescia (BNL)
Fast Shaping Amplifiers	J. Oliver (Harvard)
Fast Variable Pulse Shaping	P. O'Connor (BNL)
Fast Summing and Shaping Amplifiers	S. Rescia (BNL)
New Understanding of Long Transmission Lines in Ionization Calorimeters	C. de La Taille (Orsay)
Preamp/Shaper Circuits	I. Kipnis (LBL)
Switched Capacitor Memory/Address List Proc.	M. Levi (LBL)
ADC/Op-amp/Comparator	O. Milgrome (LBL)
Overall Calorimeter System Design/Costs	R. Jared (LBL)
Gated Integrator ASIC for all digital readout	G.W. Foster (FNAL)
Status of Electro-optic modulators	V. Radeka (BNL)
Overall System Design/Cost of FNAL Cal readout	G.W. Foster (FNAL)
Perspectives on Calorimeter Triggering	W. Smith (Wisc.)
Perspectives on Calorimeter Triggering	G. Sullivan (Chic.)
PMT Preamp	W. Smith (Wisc)
Level 2 Triggering	D. Hubbard (Saclay)
Scintillating Fiber REadout	A. Baumbaugh (FNAL)
Photodetectors for Shower Max. Detectors	D. Hubbard (Saclay)
Readout of Shower Max detectors	E. Beauville (Saclay)
Preamp/Shaper/Disc/TVCAMU	R. Van Berg (U. Penn)

AAD 7146

TMC	H.H. Williams (U. Penn)
Muon Chamber readout and Triggering	J. Chapman (Mich.)
Radiation Hard CMOS & Bipolars	H.H. Williams (Penn)
Digital Readout of Silicon Strips	K. Shankar (UCSC)
Charge Readout of Silicon Strips	N. Spencer (UCSC)
Protocols/Requirements for DAQ	E. Barsotti (FNAL)
Status of DAQ Simulations	J. Dorenbosch (SSCL)
A "baseline" DAQ System	E. Barsotti (SSCL)
Pixel Readout	D. Nygren (LBL)
Pixel/Preamp/Disc	M. Wright (LBL)

Recent Developments in Ionization Calorimetry and Implications for Front End Electronics

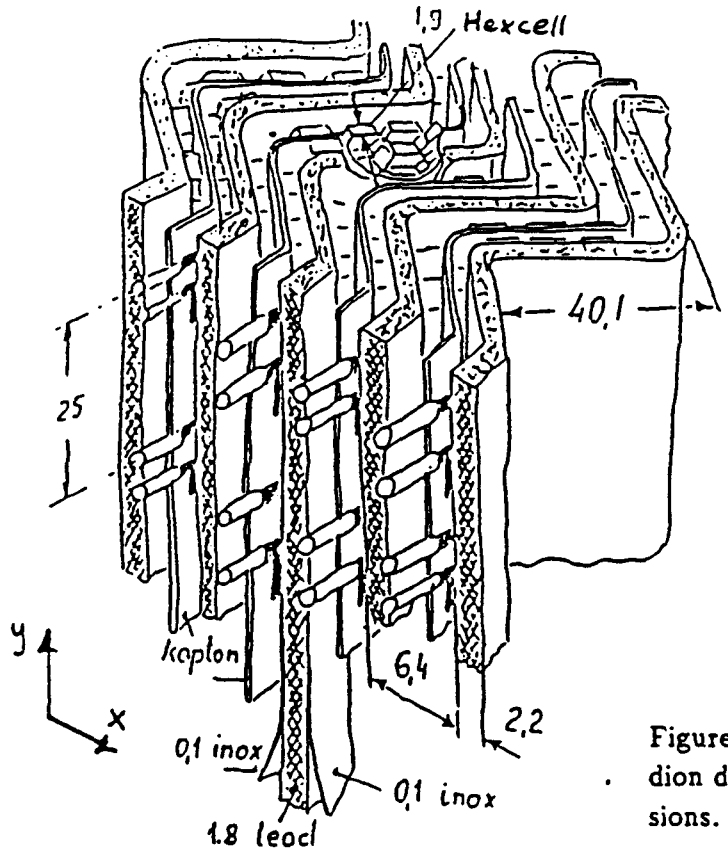
V. Radeka (BNL)

Recent Developments in Ionization Calorimetry and Implications for Front End Electronics

V. Radeka, BNL

1. Accordion results:
   - Good resolution and high speed;
   - Faster shaping necessary with good tolerances;
2. Large system calibration with high accuracy, $< 0.3\%$
3. Large signals and large dynamic range:
   - compression necessary in the preamplifier
4. Forward calorimetry:
   - new electrode configurations and high speed.
5. JFET rad. tests.
   → remote preamps (talk by C. De La Taille)

Accordion EM calorimeter



2.5×2.5 cm^2
tower $25 X_0$
$\rightarrow C \approx 3 \times 200$ pF

Figure 1: Artist's view of the accordion design. See text for the dimensions.

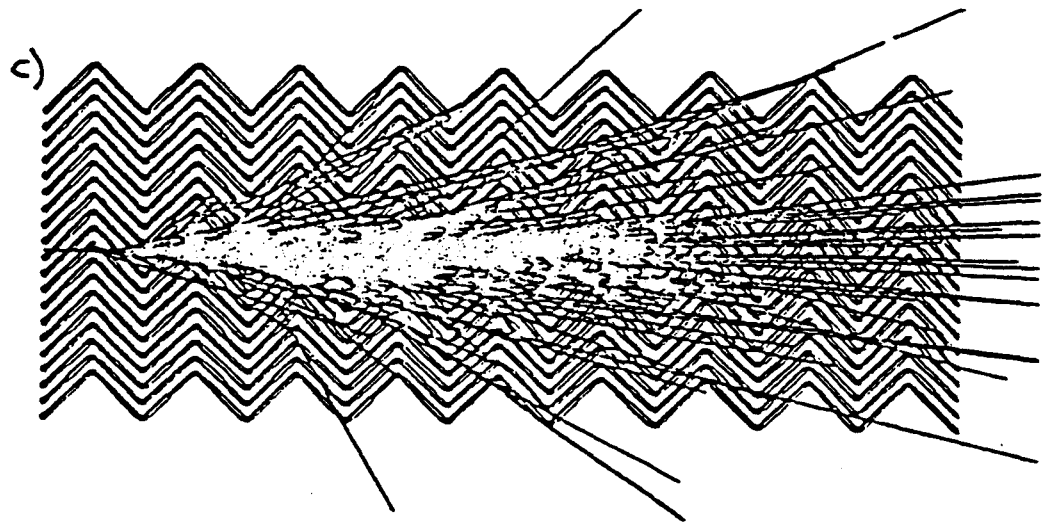


Figure 6: 40 GeV electron shower. All tracks are shown in (a). Only the charged and neutral tracks are shown in (b) and (c) respectively. In these figures, the cutoff energy for electrons and photons is 10 MeV.

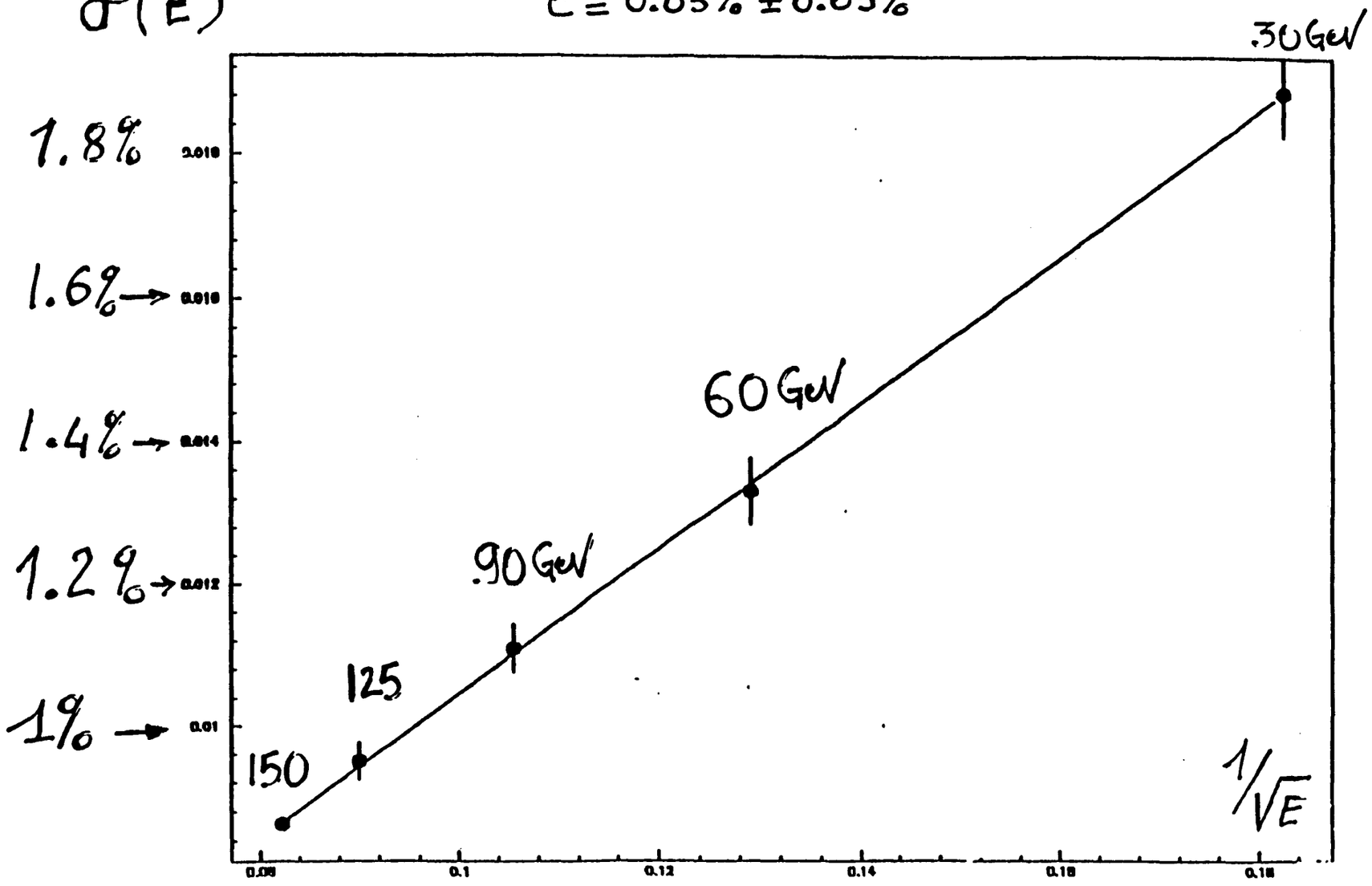
5

FIT: $\sigma = k/\sqrt{E} + c$

$k = 10.2\% \pm 0.5\%$

$c = 0.03\% \pm 0.05\%$

LOCAL:
2cm x 2cm



Accordion LAr EM Cal.

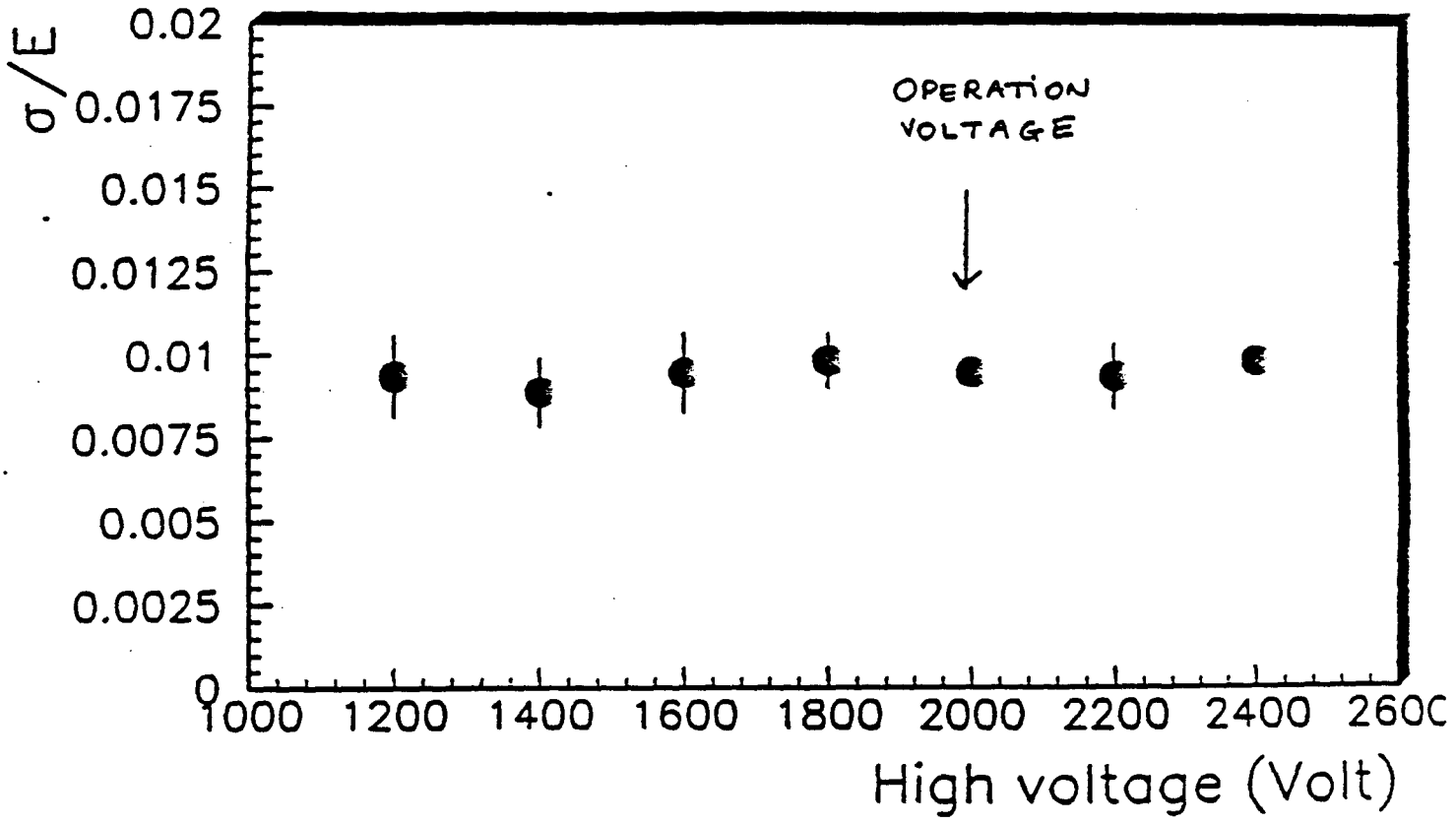


Figure 10: Energy resolution at 122 GeV/c as a function of the high voltage applied to the test module

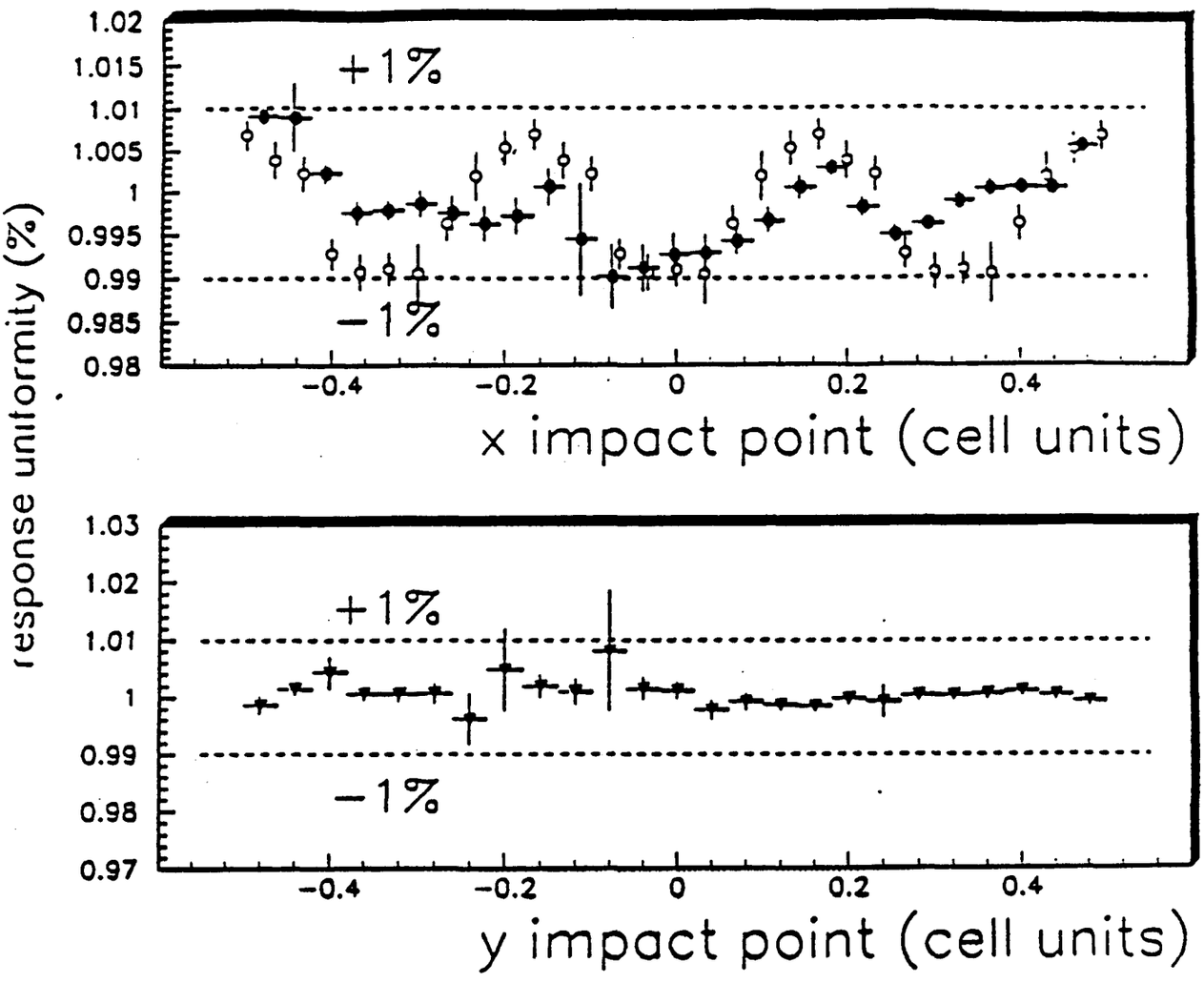


Figure 11: Relative variation of the calorimeter response over a cell as a function of the electron x (top) and y (bottom) position. Black circles: experimental points. Open circles: prediction of a Monte Carlo simulation of the Accordion.
The dotted lines delimit the $\pm 1\%$ deviation from the mean

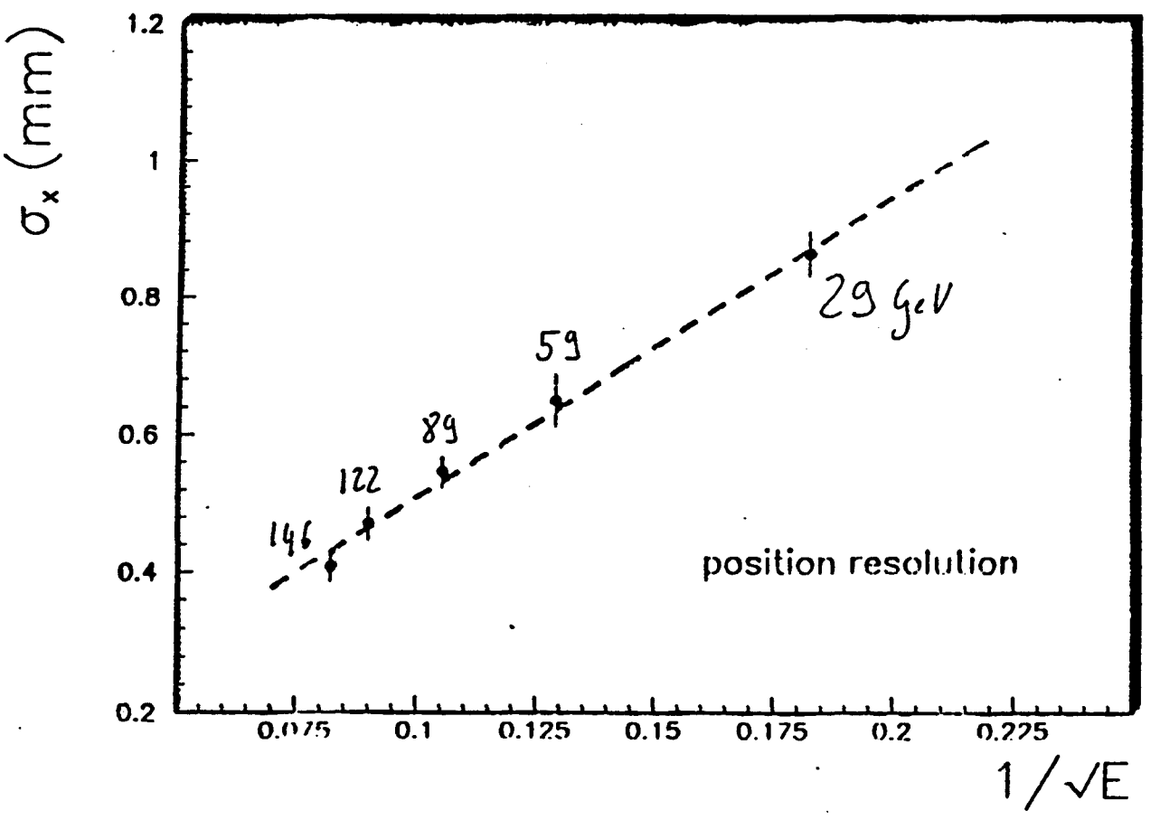


Figure 13: Space resolution of the prototype in the x view for different electron beam energies. The dashed line is a linear fit to the data points (see text).

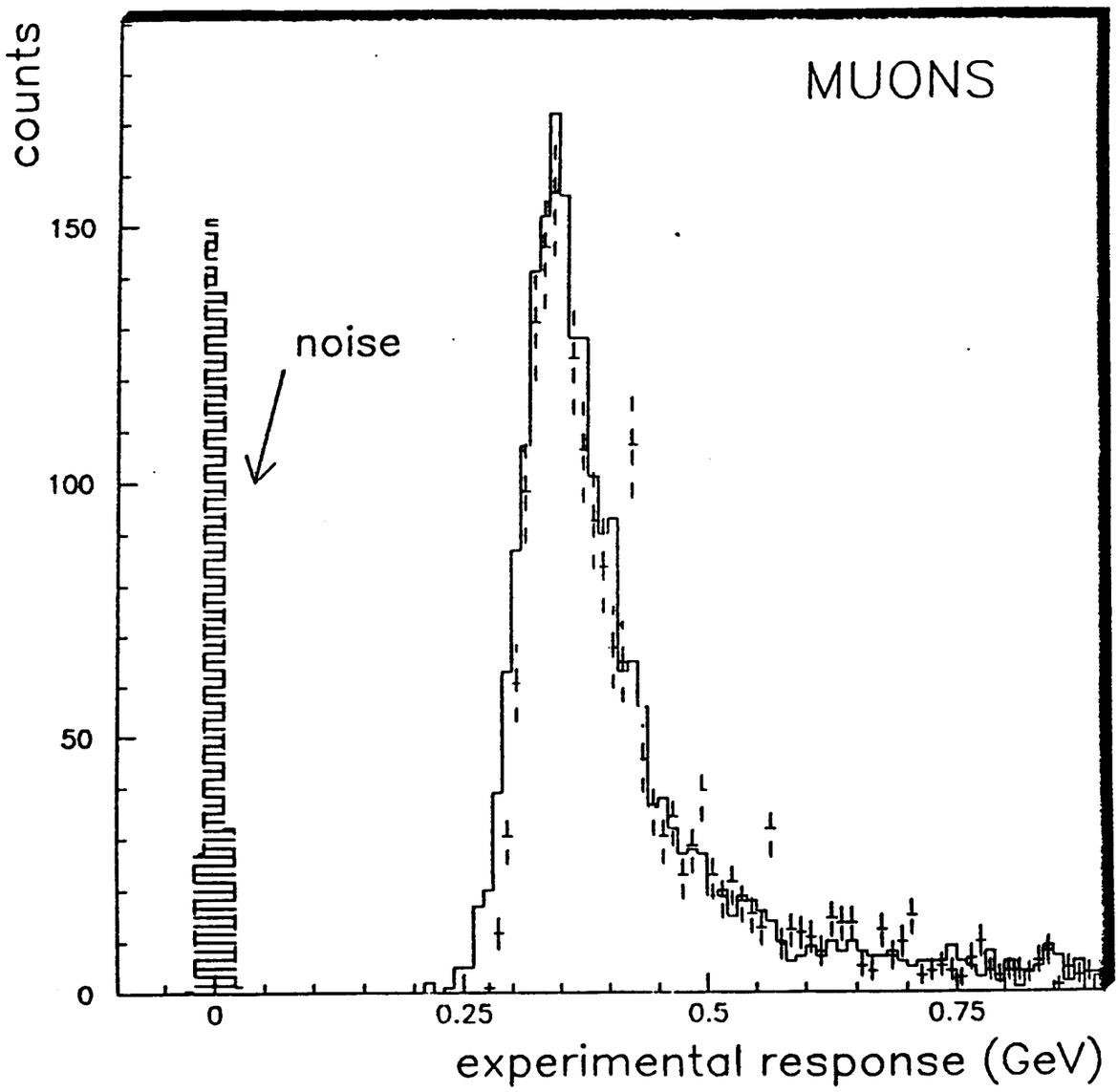
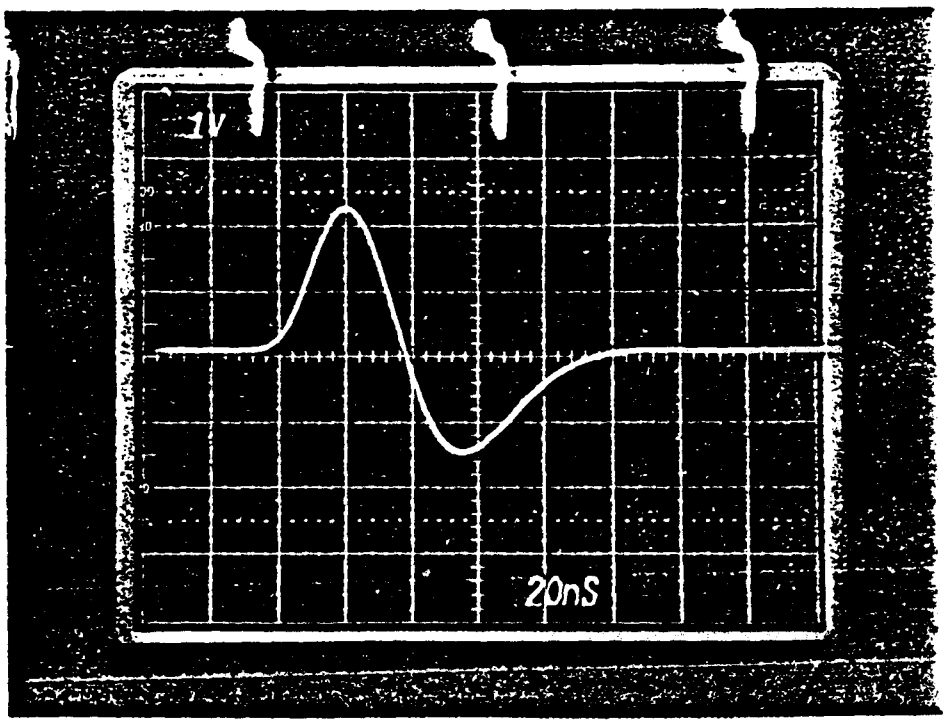


Figure 16: Energy deposited in the prototype by ~ 100 *GeV/c* incident muons The distribution for the test beam data (full line) is compared to the prediction of a Monte Carlo simulation of the calorimeter (points with error bar). The shaded area is the electronic noise in the muon cluster

Noise : $\sigma_E \approx 3$ MeV at $t_p = 100$ nsec / channel
16 MeV " for 27 channels
$\sigma_E \approx 18$ MeV at $t_p = 30$ nsec
96 MeV for 27 channels

10

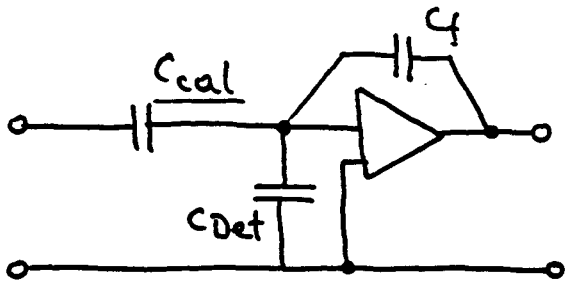
Pulse shaping : (impulse * response)



±0.015%

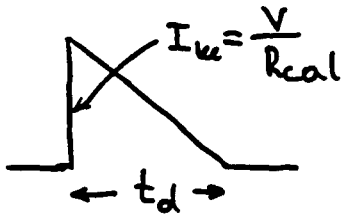
Charge Calibration

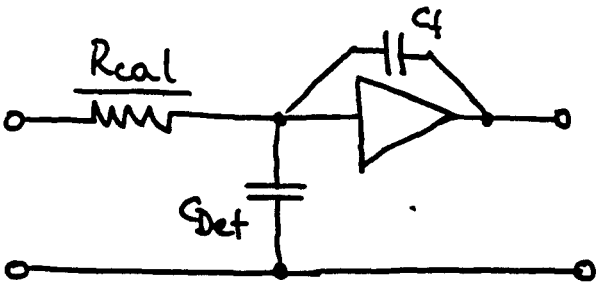
1) $Q = CV$



$\frac{\delta C_{cal}}{C_{cal}} \approx 2\%$

2)

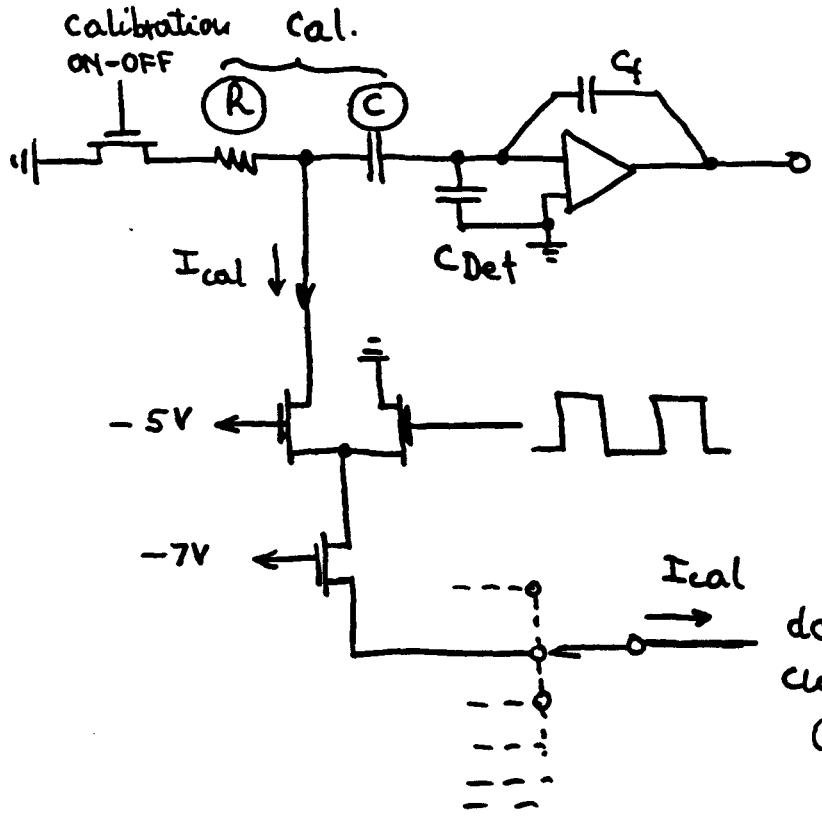




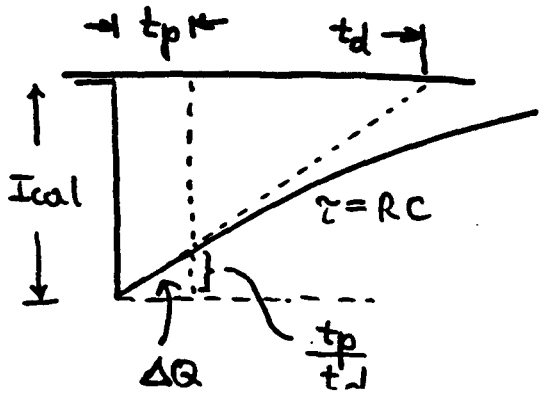
$\frac{\delta R_{cal}}{R_{cal}} \approx 0.1\%$

Problemes:
1. Low R needed
2. Distribution of precisely controlled pulses.

3)



1. R can be low
2. dc current distributed
3. 10% R's used result in 0.5% calibration



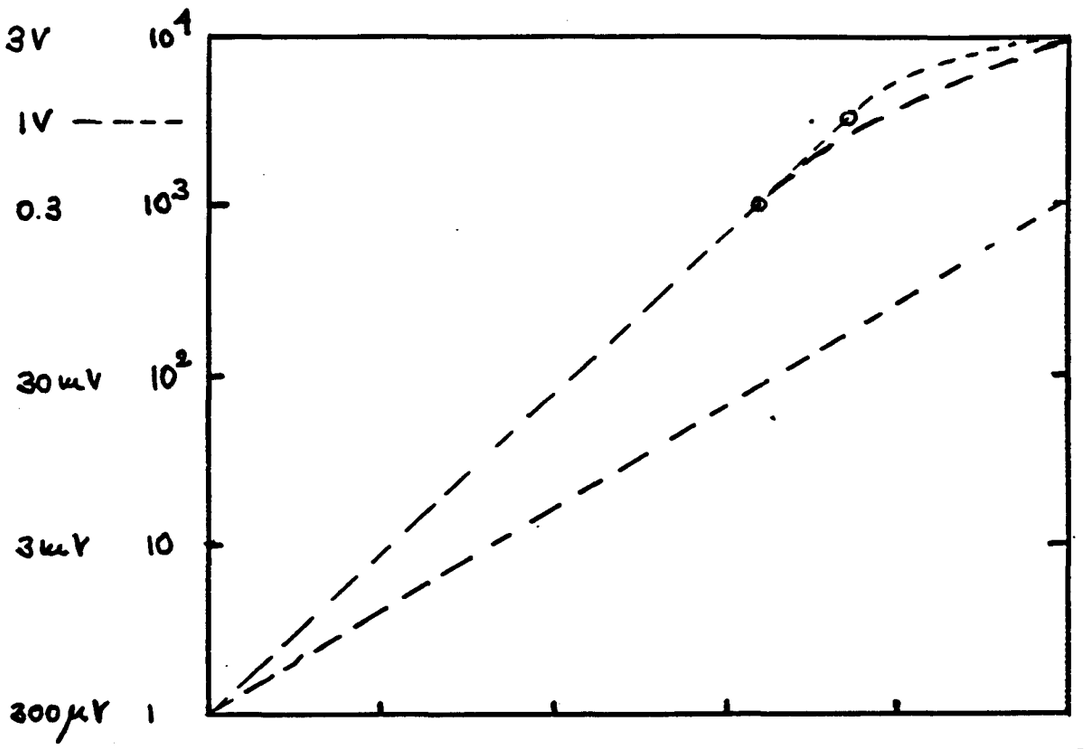
$Q_{cal} = I_{cal} \cdot t_p \left(1 - \frac{1}{2}\frac{t_p}{t_d}\right)$

$\frac{\Delta Q}{Q_{cal}} = \frac{1}{2}\frac{t_p}{t_d} \approx \frac{1}{20}$ for $t_p = 40$ μsec, $t_d = 400$ μsec

$\frac{\delta I_{cal}}{I_{cal}} = \frac{1}{20}\left(\frac{\delta R}{R} + \frac{\delta C}{C}\right)$

[illegible] 12

Dynamic range compression for EM calorimetry

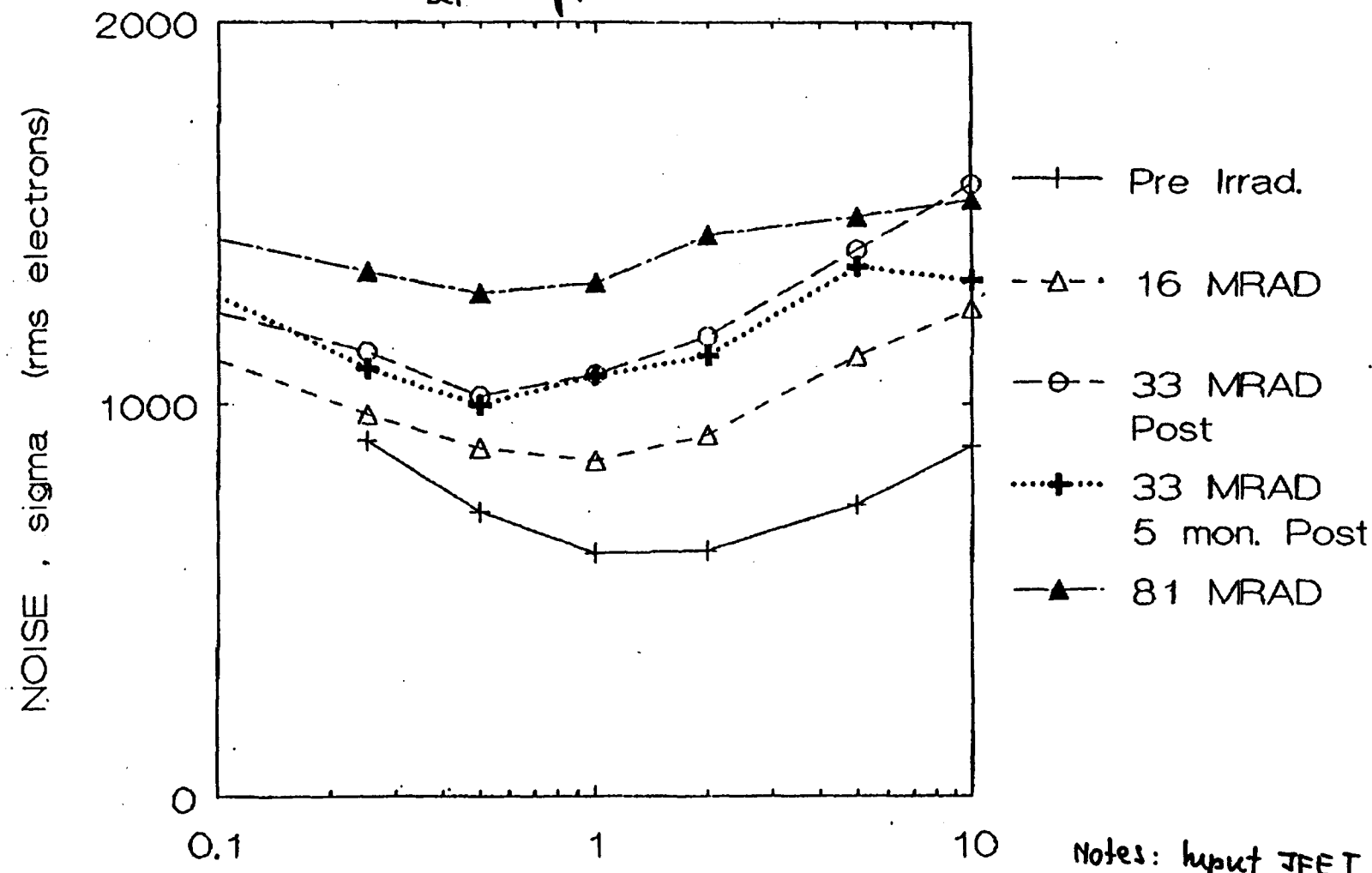


20 MeV	0.2 GeV	2	20	200	2 TeV	(1 channe
60 MeV	0.6 GeV	6	60 ↑ 180	600	6 TeV	(total)
0.01 pC	0.1	1	10 ↑ 30pC (30pF)	100 pC	1nC	

GAMMA IRRADIATED PREAMPS WARM

UNPOWERED with PROTECTION DIODE

C_{Det} = 100 pF

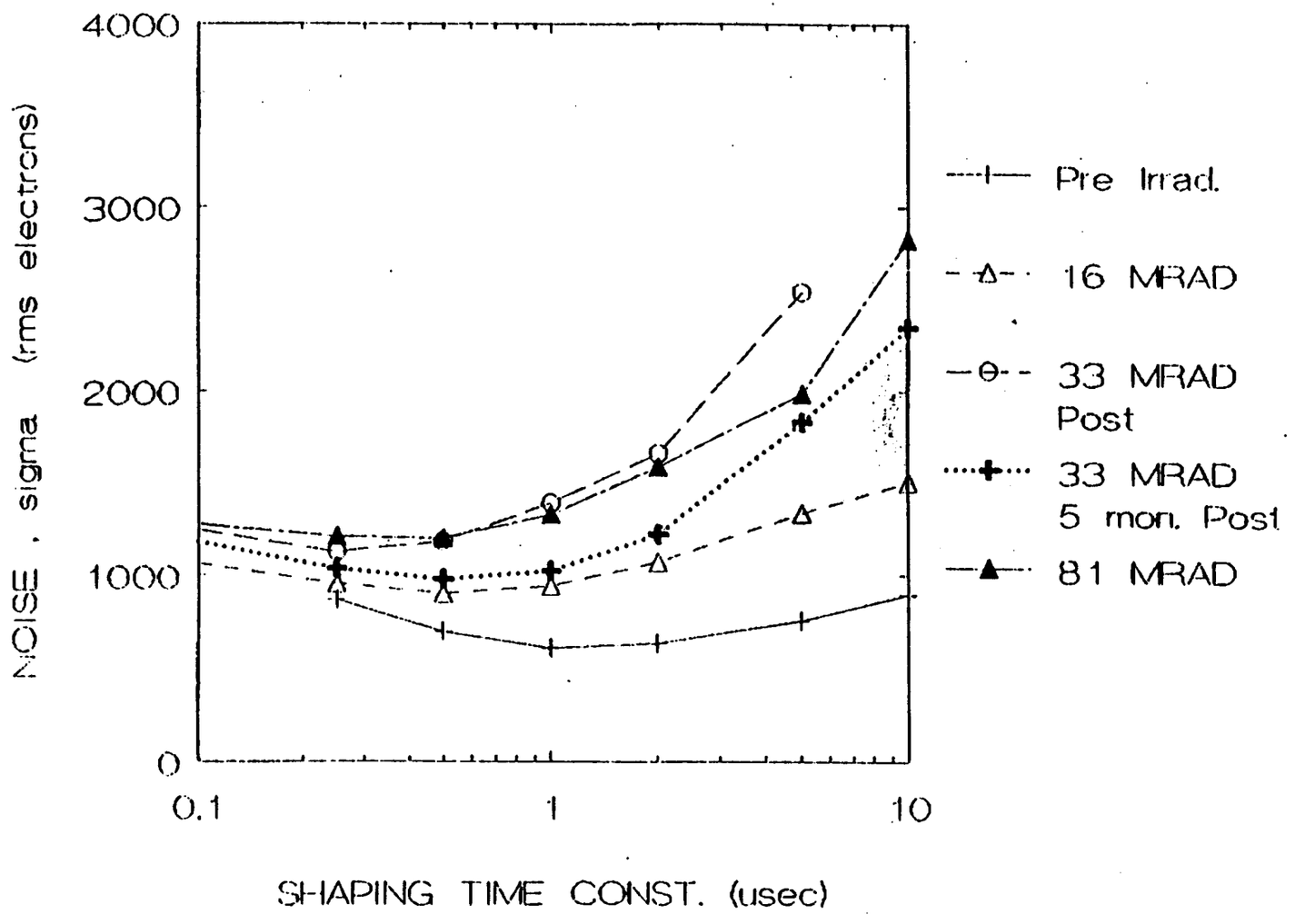


Notes: Input JFET, INTERFET NJ 132L with guard band
Protection diode, JFET without guard band

Peaking time $t_p \approx 2 \times$ Time constant

GAMMA IRRADIATED PREAMPS WARM

POWERED with PROTECTION DIODE



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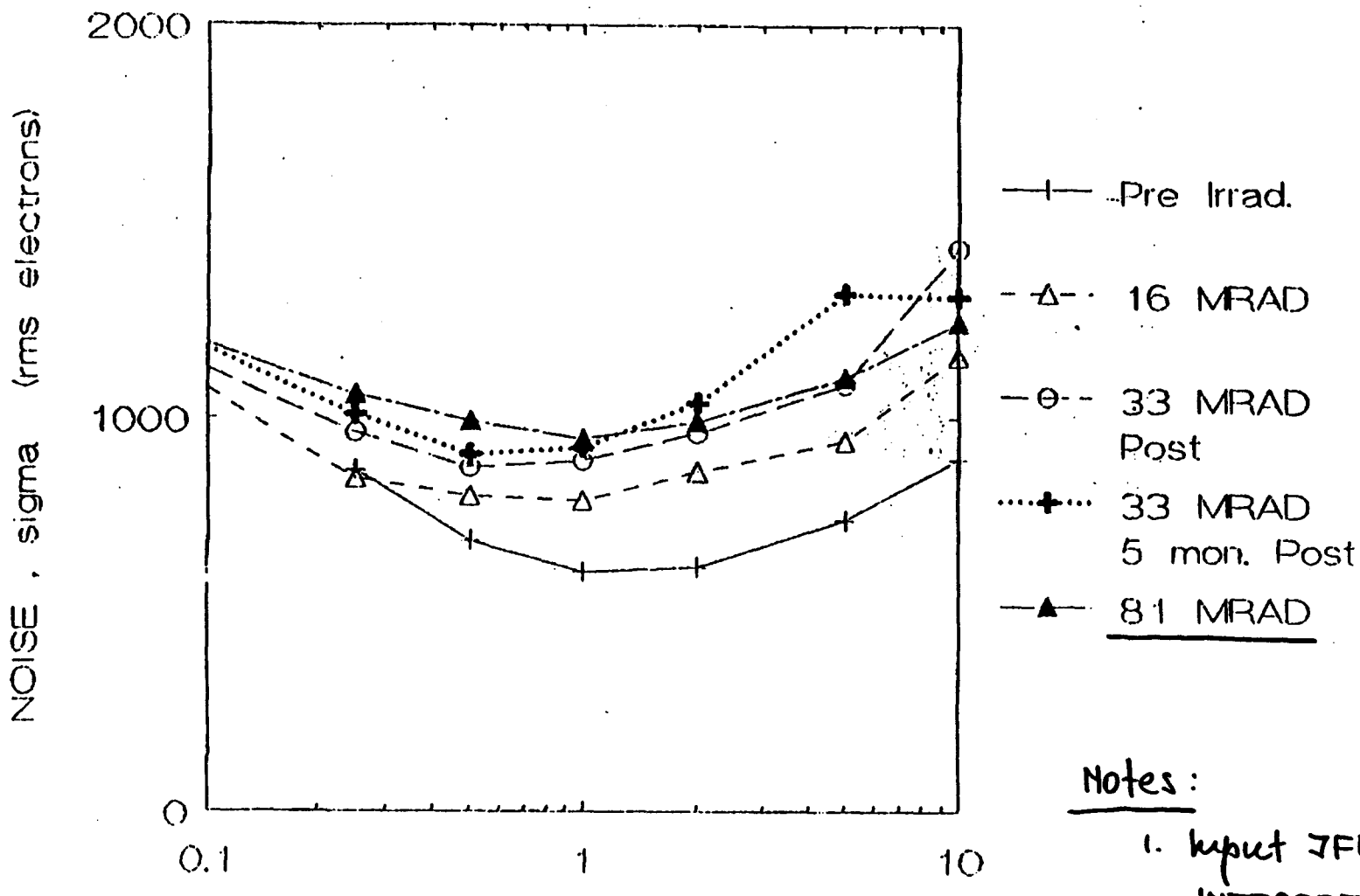
GAMMA IRRADIATED PREAMPS WARM

POWERED W/O PROTECTION DIODE



$t_p \approx 2\ T.C.$

Notes:

1. Input JFET INTERFET IF132L with guard band
2. Region of interest for calorimetry $t_p \leq 100$ usec

JFET Developments: Devices, Monolithic Amplifiers and Hybrid Amplifiers

S. Rescia (BNL)

E. RESCIA
BNL

JFET DEVELOPMENTS :

DEVICES
HYBRID AMPLIFIERS
MONOLITHIC AMPLIFIERS

FRONT END ELECTRONIC
MEETING
LBL JUNE 6-8 1991

DISCRETE DEVICE DEVELOPMENT :

) RADIATION AND NEUTRON RESISTANT JFET

a) guard ring improvement to prevent formation of inversion layer even at very high doses (> 20 MRad)

b) Reduction of feature size (L ≈ 2 μm)

- SMALLER VOLUME ⇒ HIGHER NEUTRON RESISTANCE
- HIGHER FIGURE OF MERIT g_m / C

) RADIATION HARDENED OXIDE

) OPTIMIZATION FOR LOW TEMPERATURE OPERATION

STATUS

HYBRID DEVELOPMENT

* EVEN WITH MONOLITHIC FRONT END SOME EXTERNAL COMPONENTS ARE NEEDED- (POWER SUPPLY FILTER, POSSIBLY FEEDBACK ELEMENTS).
  FRONT-END EVENTUALLY WILL BE AN HYBRID OF SOME FORM

* OUTSTANDING RELIABILITY (HELIOS)

* MIXING OF DIFFERENT TECHNOLOGIES POSSIBLE TO MAXIMIZE RELIABILITY, RADIATION RESISTANCE AND MINIMIZE POWER DISSIPATION

* FOR CALORIMETRY HYBRIDS COULD STILL PROVE THE BEST CHOICE BOTH TECHNICALLY AND ECONOMICALLY

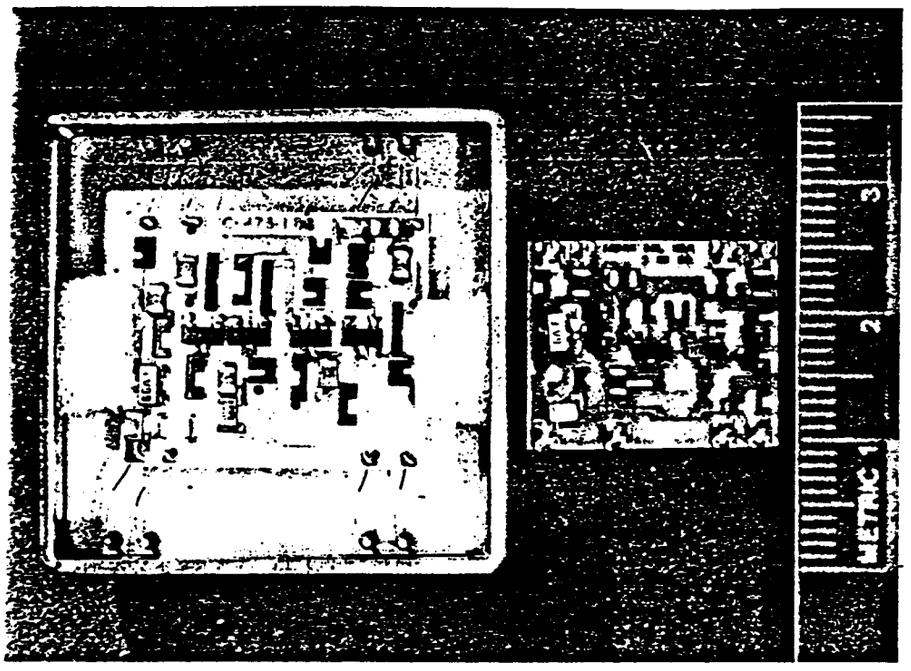


Figure 1.6.2: Charge sensitive preamplifier developed at BNL for liquid argon calorimetry. The large unit in a metal box was designed for the NA34 (HELIOS) experiment. The small hybrid is its successor and uses device optimized for low temperature operation.

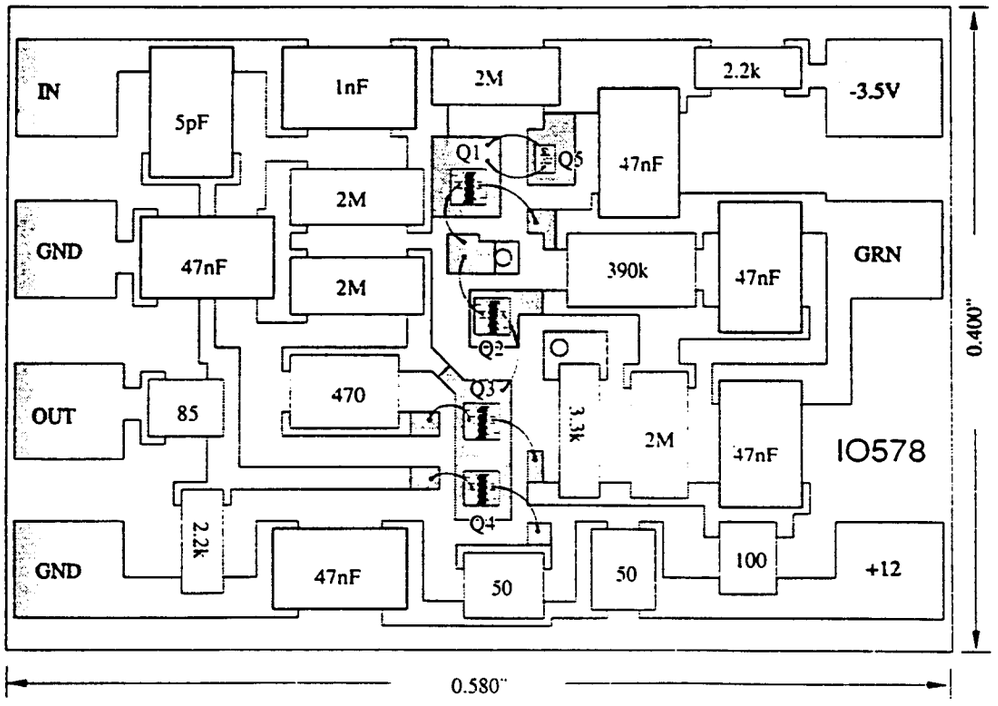
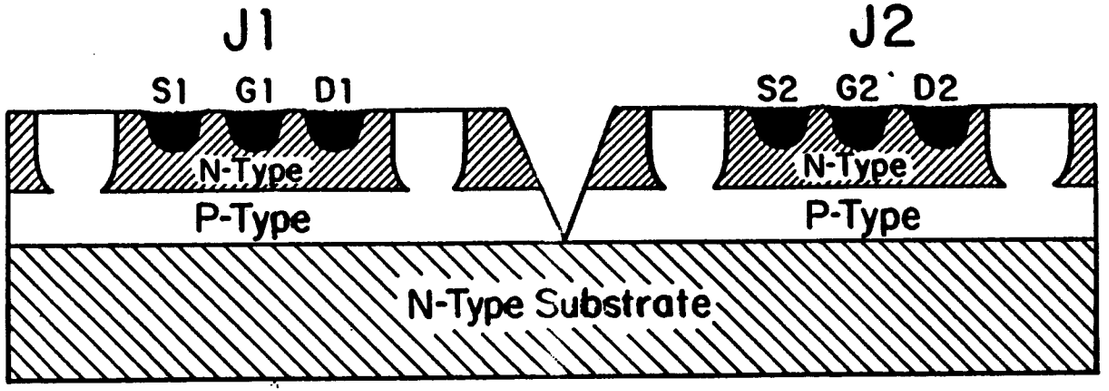
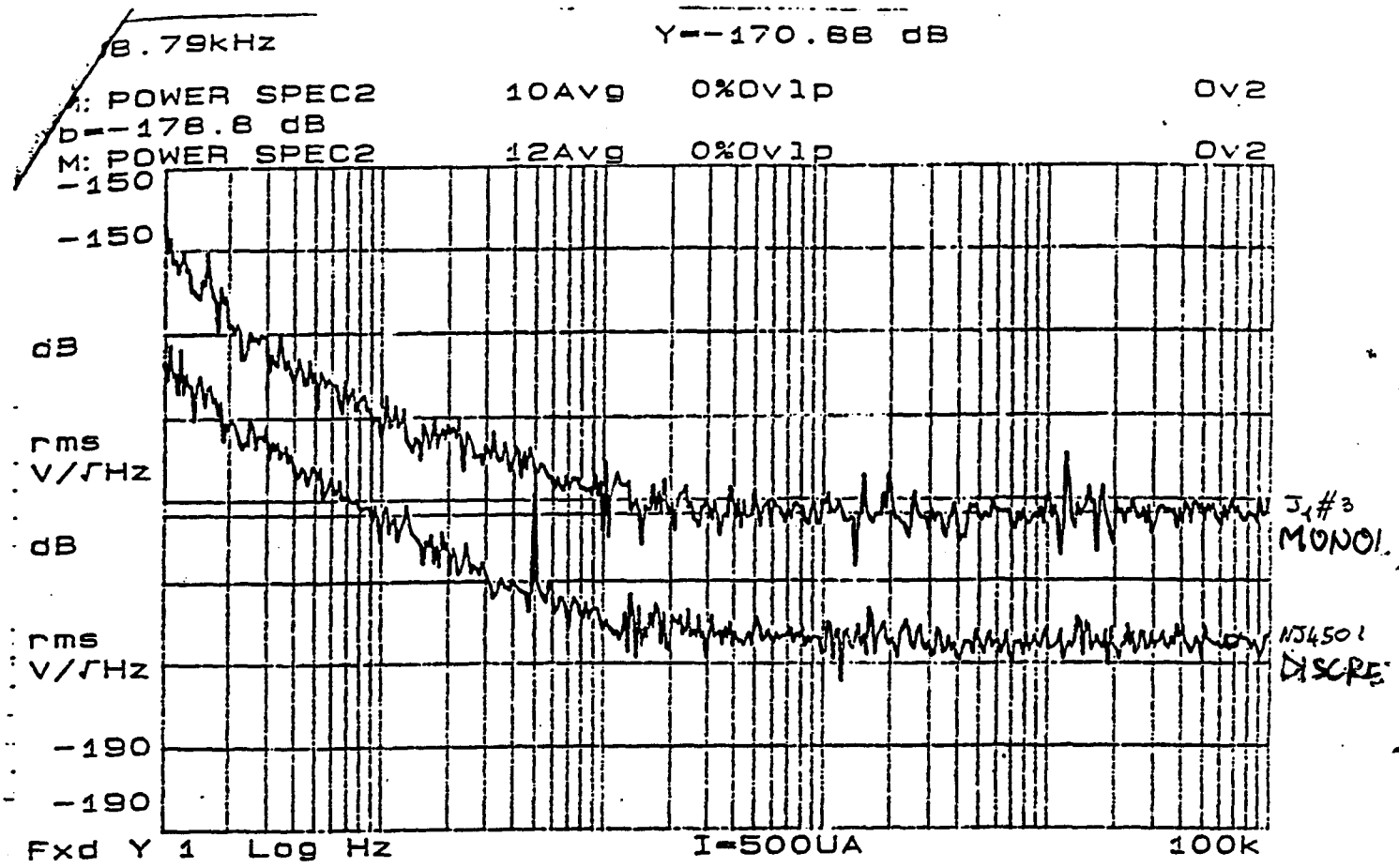


Figure 1.6.3: Hybrid layout of a charge sensitive preamplifier being developed for the SSC tests.

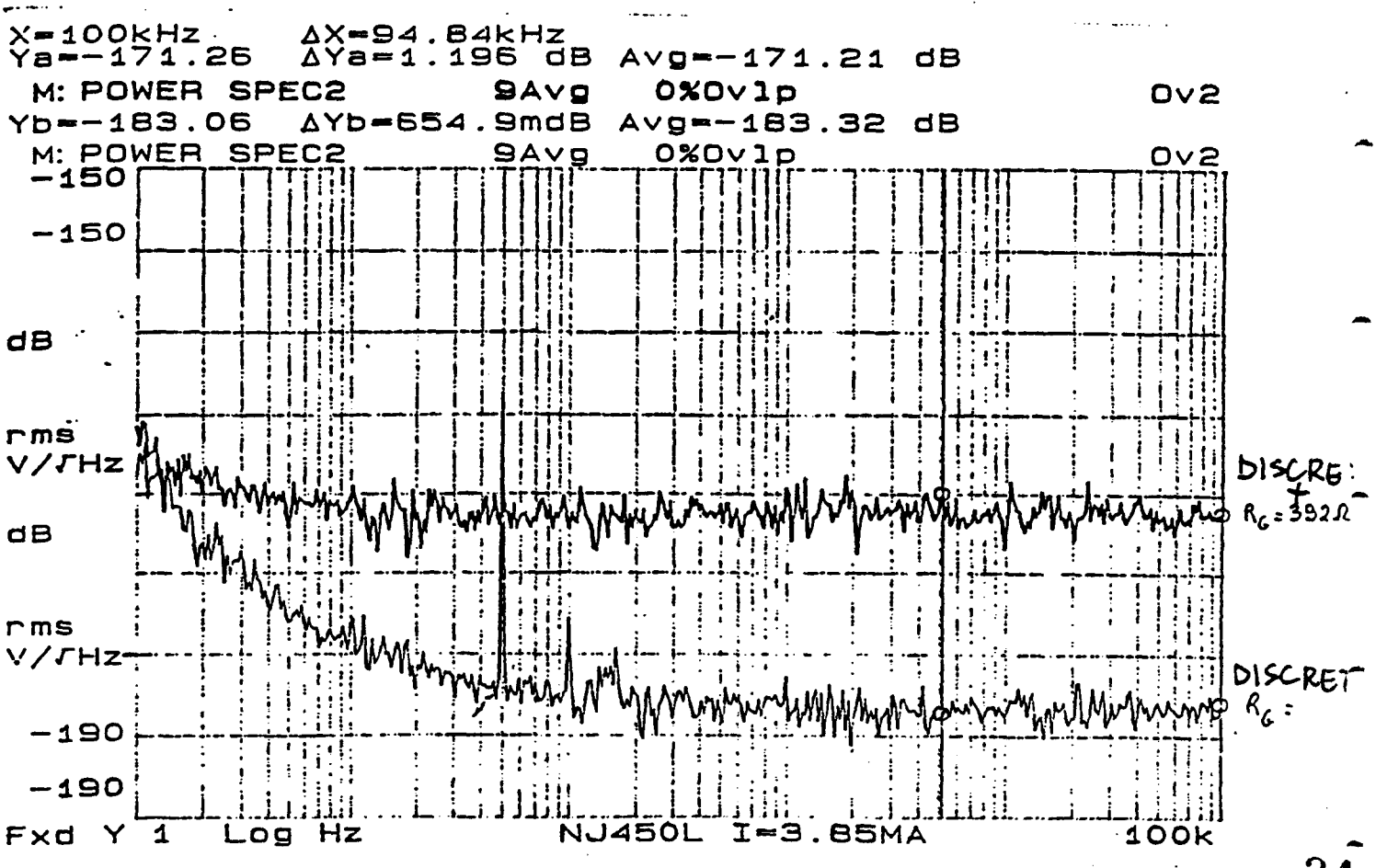


- V-GROOVE ISOLATION PROCESS

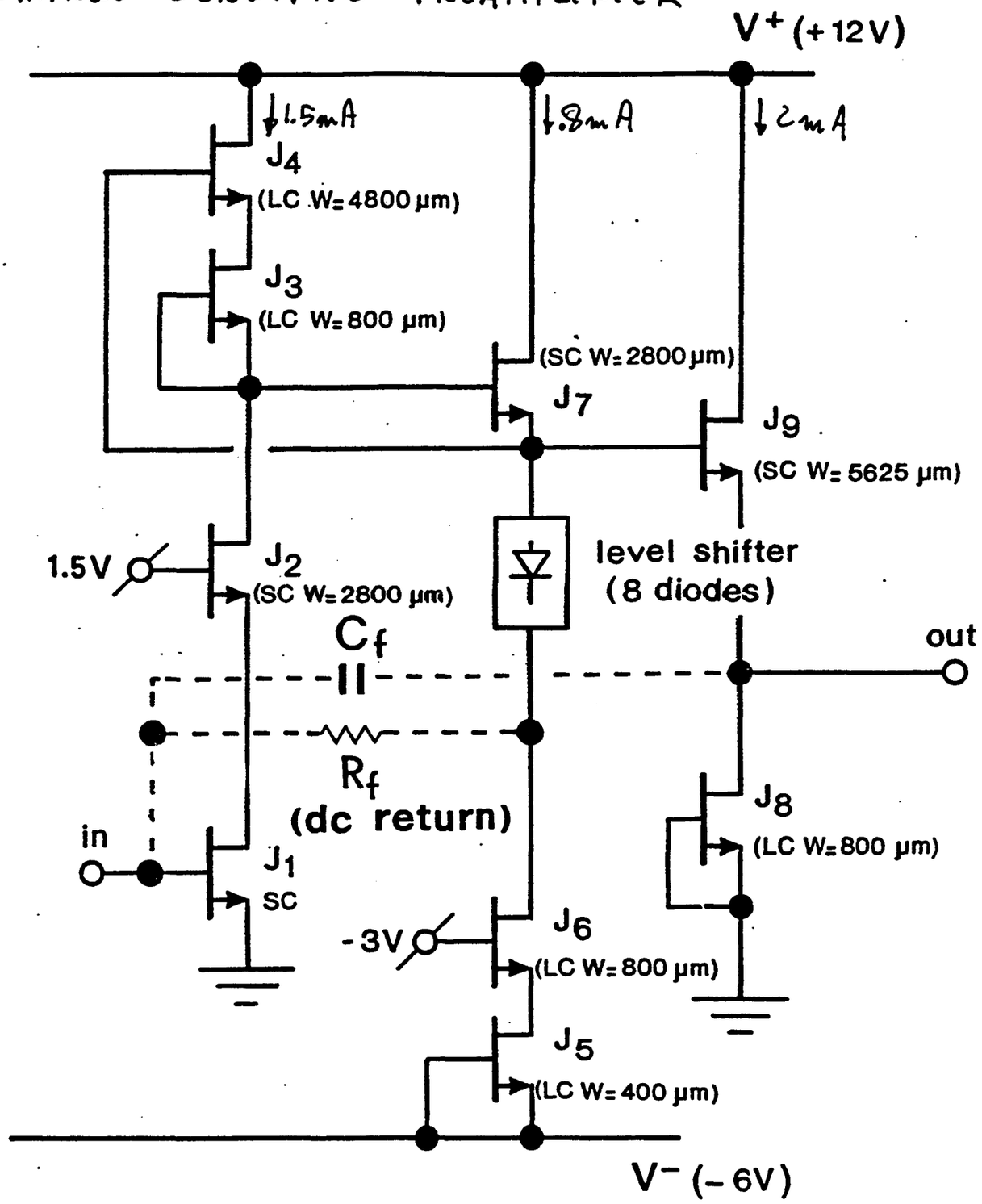
	Short Channel		Long Channel	
W	11.400 μm		400 μm	
L	5 μm		6.5μm	
	Monolithic	Discrete	Monolithic	Discrete
I_{DSS} @V_{DS} = 5 V	54 mA	37 mA	1.7 mA	1.1 mA
V_T	-1.3 V	-1 V	-1.25	-1 V
g_m @I_D = 2 mA V_{DS} = 3 V	20.1 mS	21 mS	2.1 mS	1.6 mS
I_G	1 pA	1 pA	.4 pA	.2 pA
R_{ds} @I_D = 2 mA V_{DS} = 3 V	12 kΩ	60 kΩ	57 kΩ	65 kΩ
μ @I_D = 2 mA V_{DS} = 3 V	240	1260	120	105

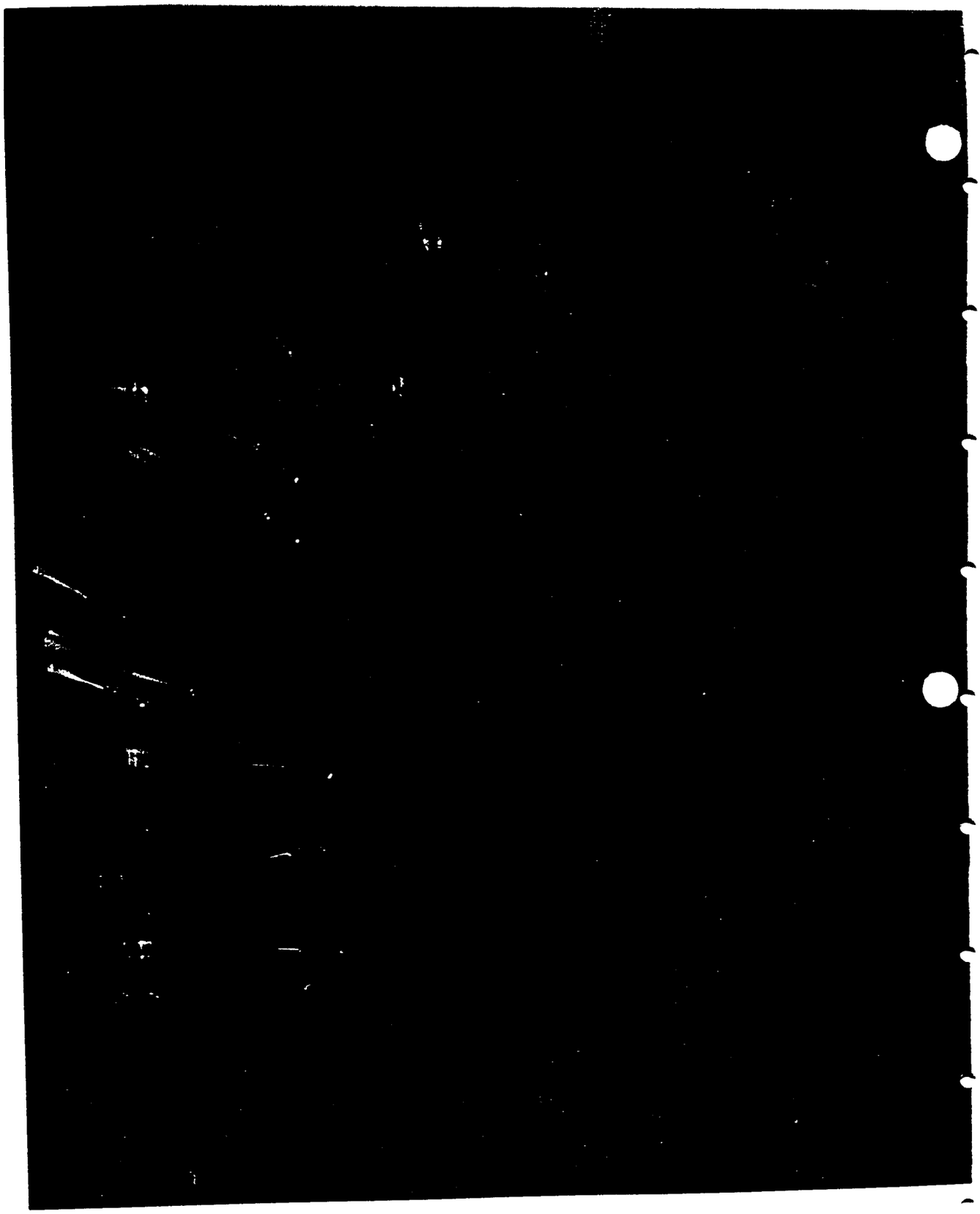


J_1#3 : g_m = 8.01 mA/V NJ450L : g_m = 8.92 mA/V

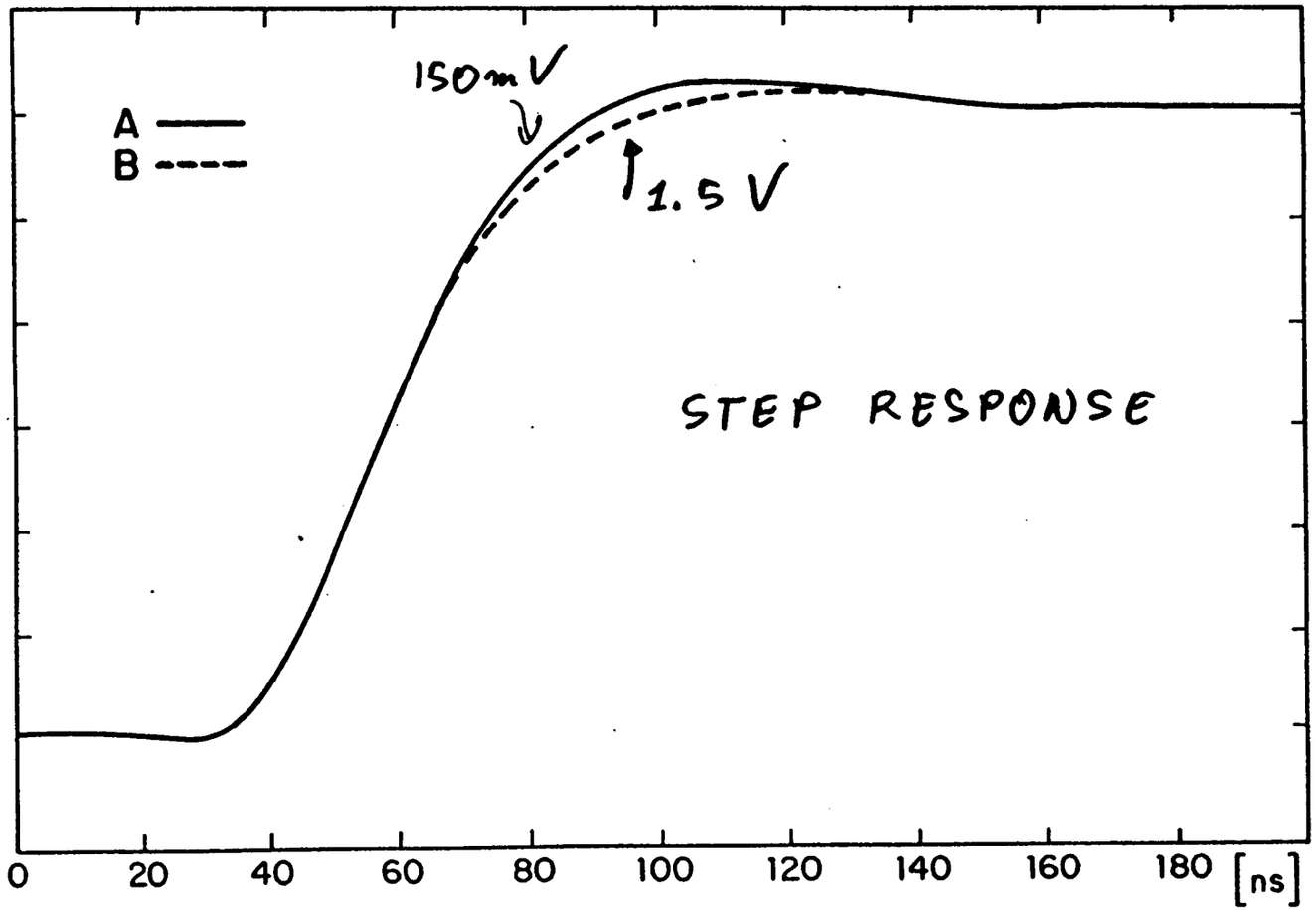


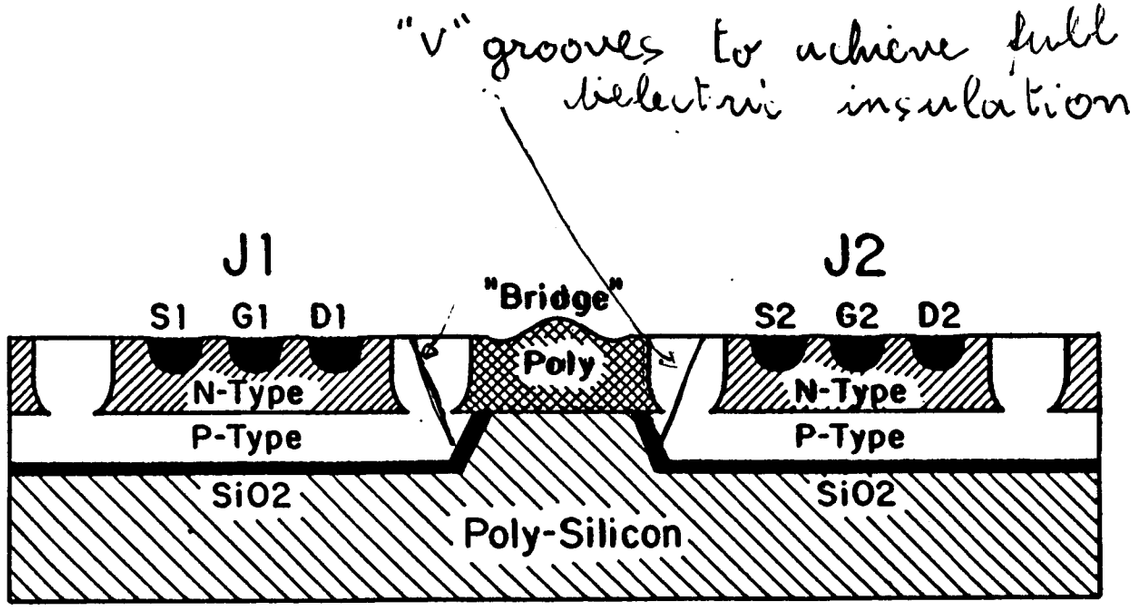
CIRCUIT DIAGRAM OF THE MONOLITHIC ALL-JFET CHARGE SENSITIVE PREAMPLIFIER



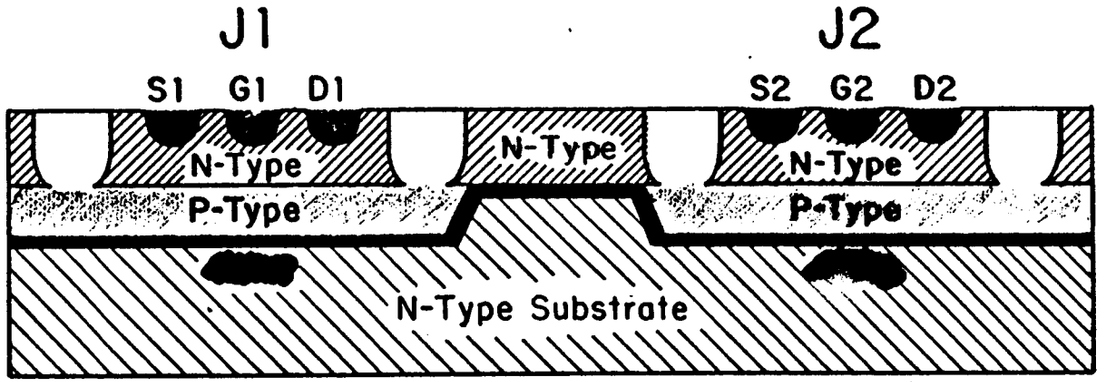


DOUBLE EPI V-GROOVE
"KIT PARTS" PREAMPLIFIER





- PLANAR PROCESS
- MESA ISOLATION PROCESS

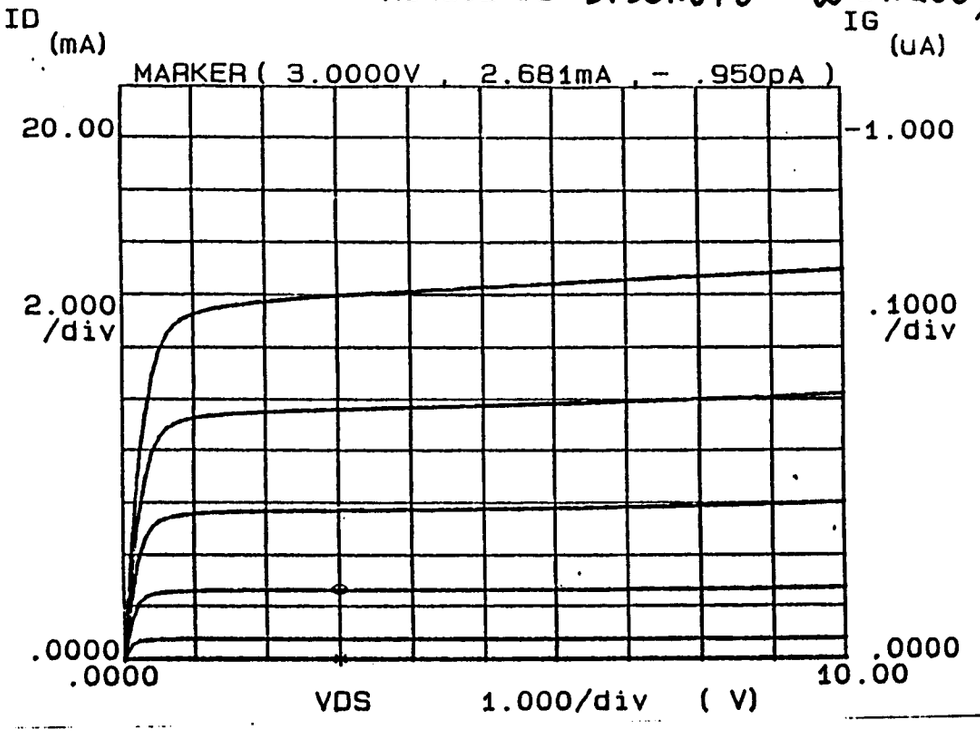


PLANAR TECHNOLOGY

BURIED LAYER - N EPI

****** GRAPHICS PLOT ******

NJ450L #3 DISCRETE W = 11400 μm L = 5 μm



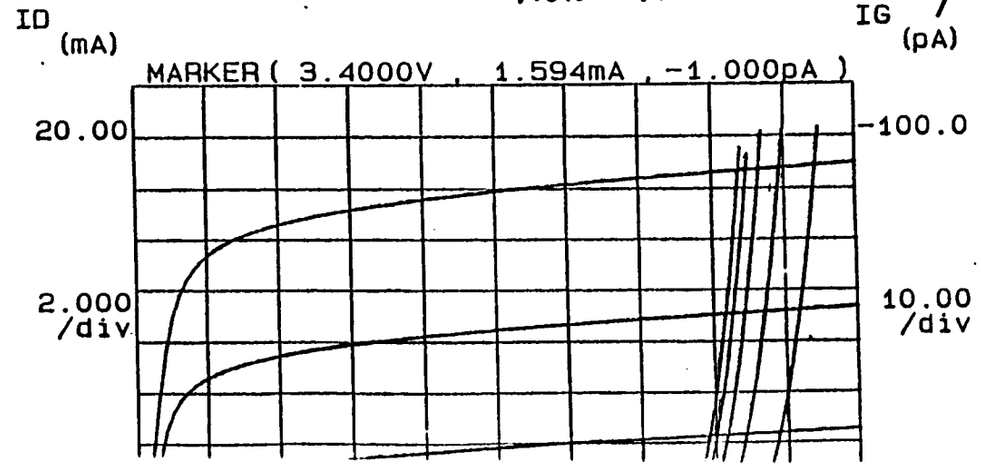
Variable1:
VDS -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Variable2:
VG -Ch3
Start - .3000V
Stop - .7000V
Step - .1000V

Constants:
VS -Ch1 .0000V

****** GRAPHICS PLOT ******

J1 #2 MONOLITHIC W = 11400 μm L = 6.5 μm

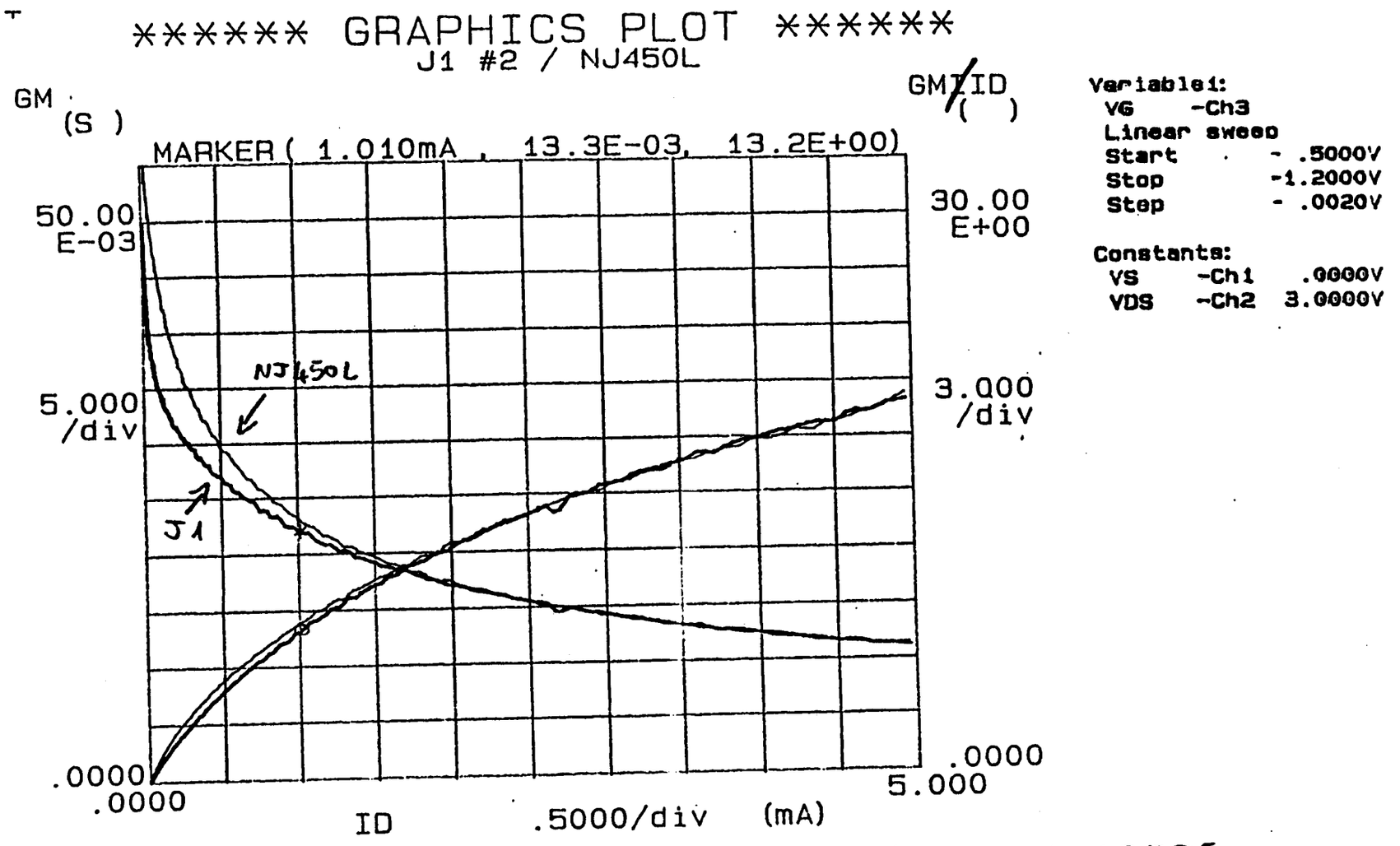


Variable1:
VDS -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Variable2:
VG -Ch3
Start - .5000V
Stop - .9000V
Step - .1000V

Constants:
VS -Ch1 .0000V

ID, VD



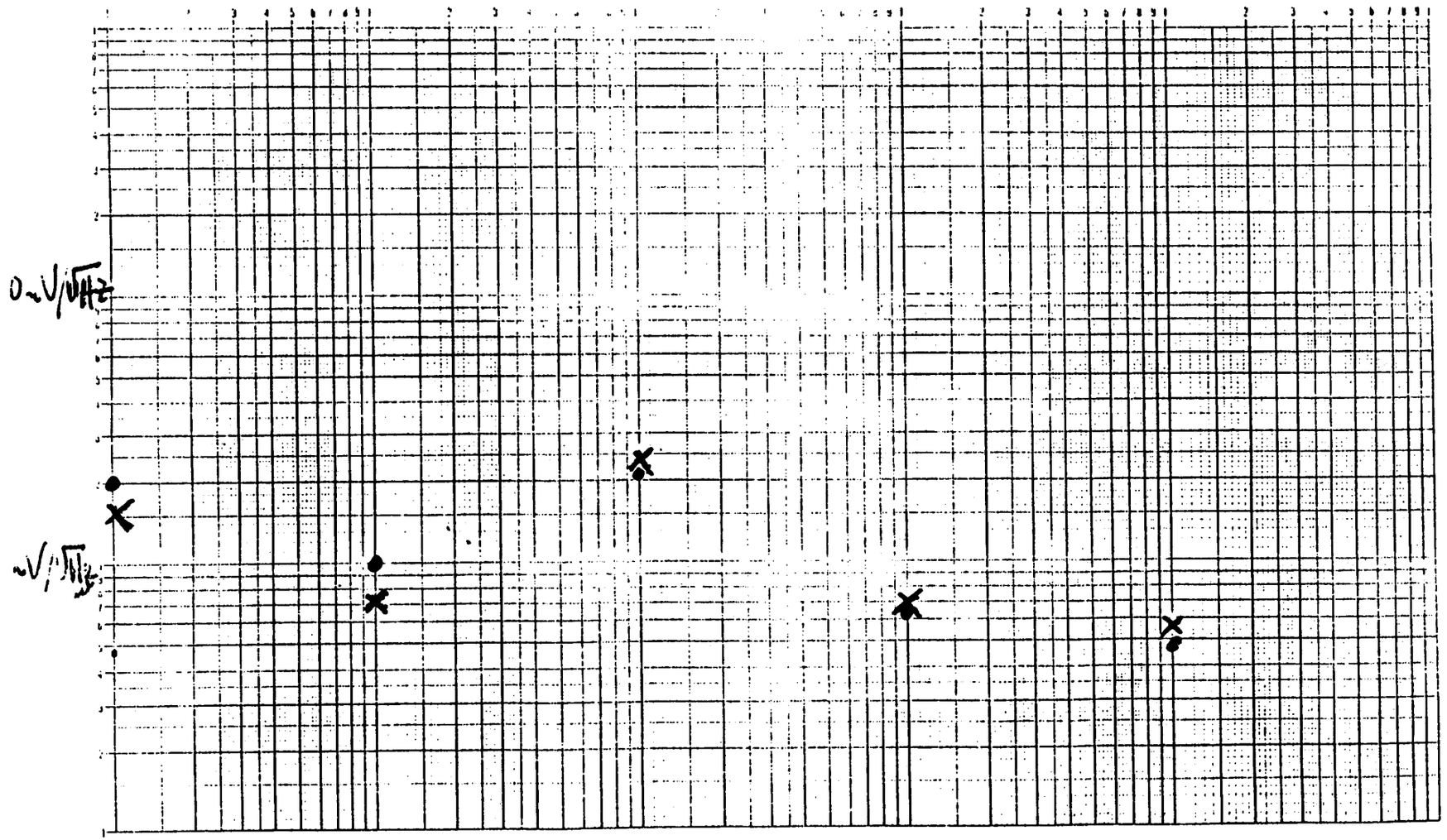
COMPARISON OF A MONOLITHIC AND A DISCRETE JFET OF EQUAL W = 11.400 μm

GM (S) = ΔID/ΔVG
GMIID ( ) = (ΔID/ΔVG)/ID

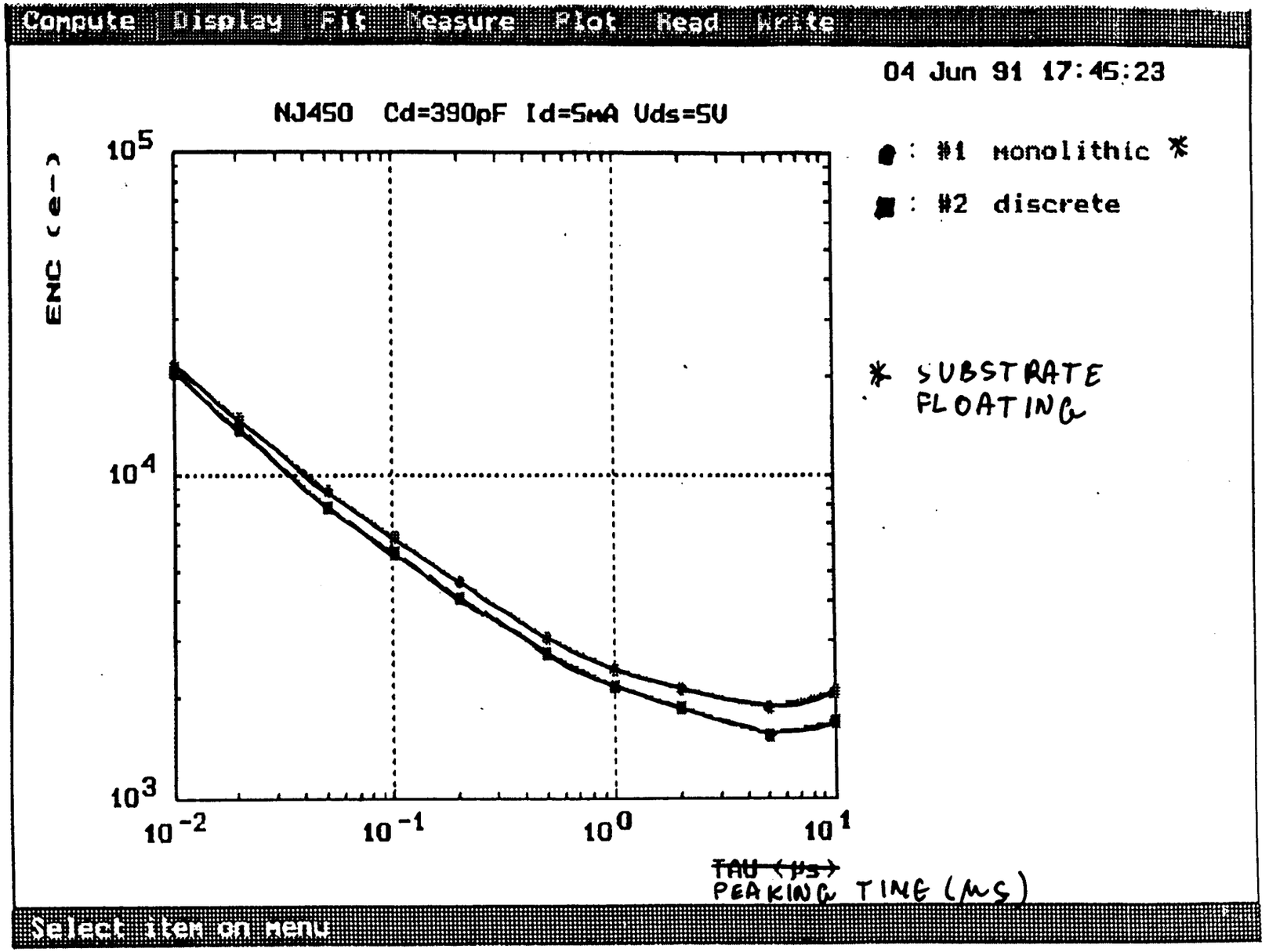
$I_D = 5\ mA$: NOISE - MONOLITHIC & DISCRETE JFETs

$V_D = 5\ V$

3 June 1991



- DISCRETE J 450L $g_m = 40 \sim A/V$ ($V_P \cong 1.5\ V$)
- MONOLITHIC J1 (#2) $g_m = 36\ A/V$ ($V_P \cong 2\ V$)


Compute Display Fit Measure Plot Read Write
04 Jun 91 17:45:23
NJ450 Cd=390pF Id=5mA Vds=5V
ENC (e-)
10^5
10^4
10^3
10^{-2}
10^{-1}
10^0
10^1
TAU (μs)
PEAKING TIME (μs)
● : #1 monolithic *
■ : #2 discrete
* SUBSTRATE FLOATING
Select item on menu

Fast Shaping Amplifiers

J. Oliver (Harvard)

Status of work on

1. Bipolar shapers - translinear circuit approach
2. BiCMOS shapers - CMOS switch selectable components (resistors, capacitors

Craig Blocker - Brandeis
John Oliver - Harvard
Velyco Radeka - BNL
Paul O'Connor - BNL

TRANS-LINEAR CIRCUIT APPROACH TO EXTERNALLY PROGRAMMABLE SHAPER

OBJECTIVE: TO IMPLEMENT BIPOLAR SHAPING FUNCTION

$$\text{eg. } F(s) = \frac{(sT)^2}{(1+sT)^4}$$

WITH PEAKING TIME $\approx$ 50ns — 100ns.

REQUIREMENTS:

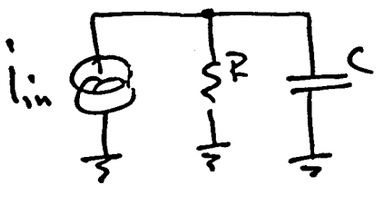
1. EXTERNALLY PROGRAMMABLE TO TAKE OUT PROCESS VARIATIONS ($\pm \approx 25\%$) $\rightarrow$ (1.67:1)

   GREATER TUNING RANGE TO TAKE OUT CALORIMETER & PREAMP VARIATIONS AND ALLOW ONLINE OPTIMIZATION (eg. VARY WITH LUMINOSITY ETC)

   2:1 to 3:1

2. ¼% LINEARITY OVER 12 BITS.

SOLUTION BASED ON CURRENT DIVIDER



RESISTIVE BRANCH CURRENT

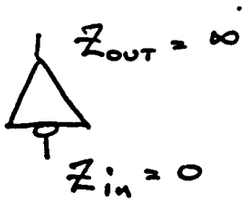
$$\frac{i_R}{i_{in}} = \frac{1}{1+sRC}$$: INTEGRATOR (LOW PASS)

CAPACITIVE BRANCH CURRENT

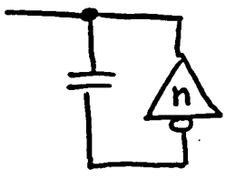
$$\frac{i_C}{i_{in}} = \frac{sRC}{1+sRC}$$: DIFFERENTIATOR (high pass)

PROGRAMMABLE ELEMENT IS CAPACITOR TUNED BY A CURRENT GAIN CELL OF GAIN n

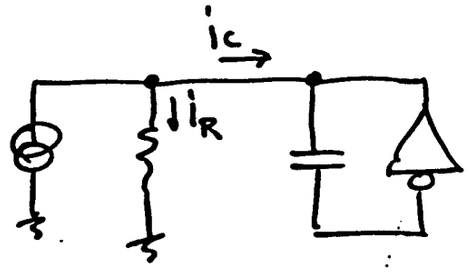
GAIN CELL



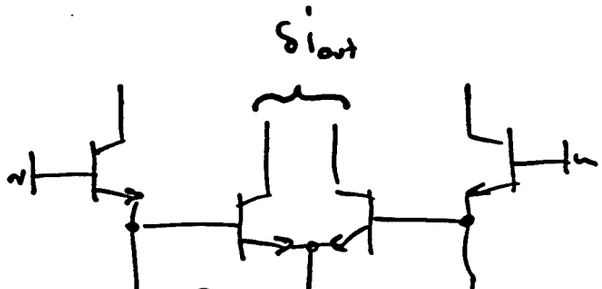
$C_{eff} = (n+1)\vec{C}$



If GAIN n IS EXTERNALLY PROGRAMMABLE, INTEGRATOR & DIFFERENTIATOR SECTIONS PROVIDED BY RESISTIVE & CAPACITIVE BRANCH CURRENTS



GAIN CELL ⇒ GILBERT GAIN CELL ("TRANSLINEAR GAIN CELL")



FROM EXPONENTIAL VOLTAGE-CURRENT RELATION,

$$\frac{\delta i_{out}}{i_{in}} = \frac{I_2}{I_1}$$

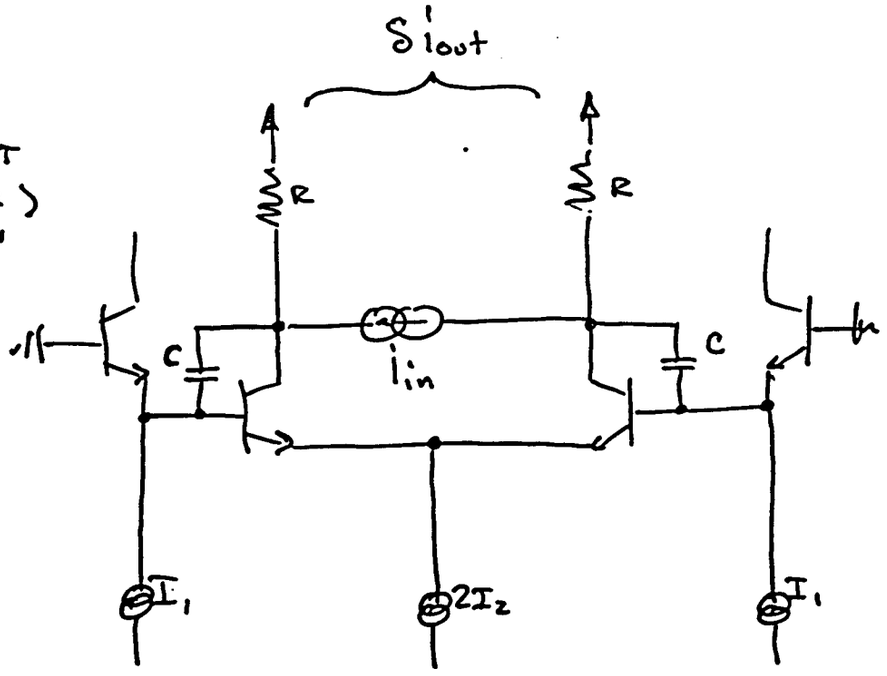
and is highly linear and temperature independent over signal range almost equal to bias current.

INTEGRATOR

TIME CONSTANT

$$T = RC\left(1+\frac{I_2}{I_1}\right)$$

$$F(s) = \frac{1}{1+sT}$$

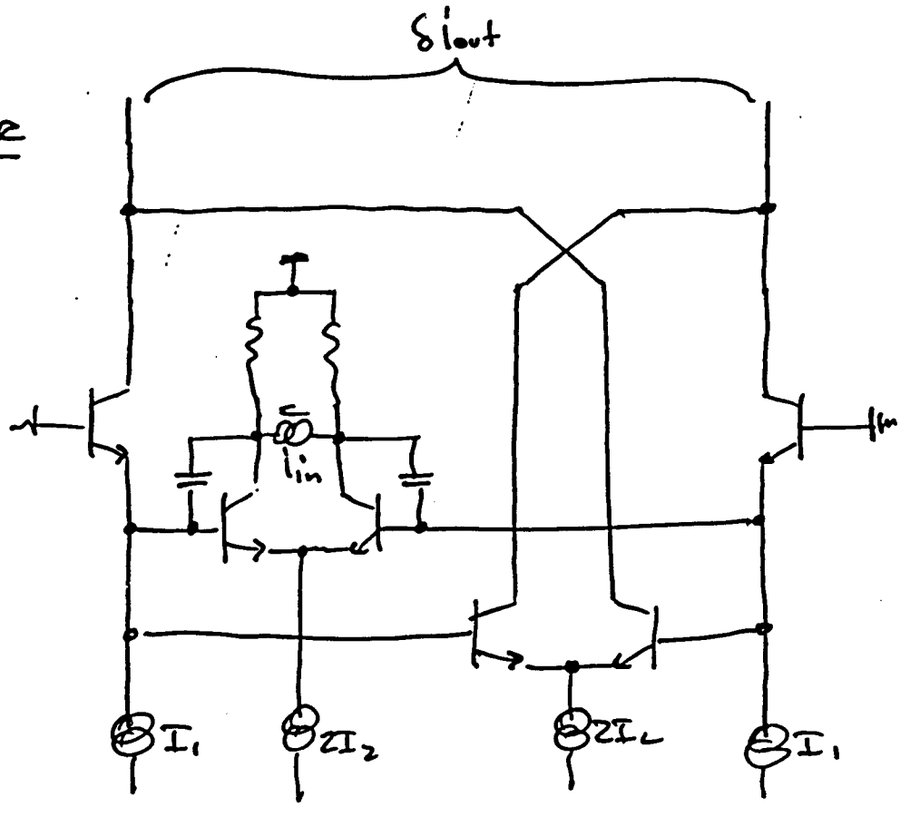


DIFFERENTIATOR

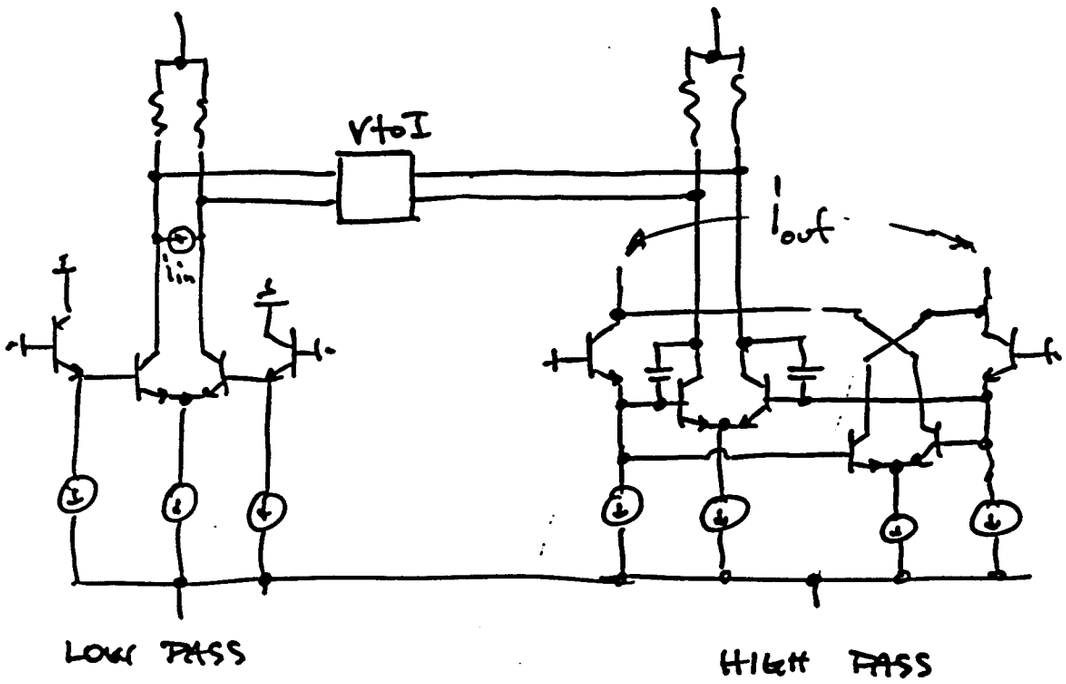
TIME CONSTANT

$$T = RC\left(1+\frac{I_1}{I_2}\right)$$

$$F(s) = \frac{sT}{1+sT}$$

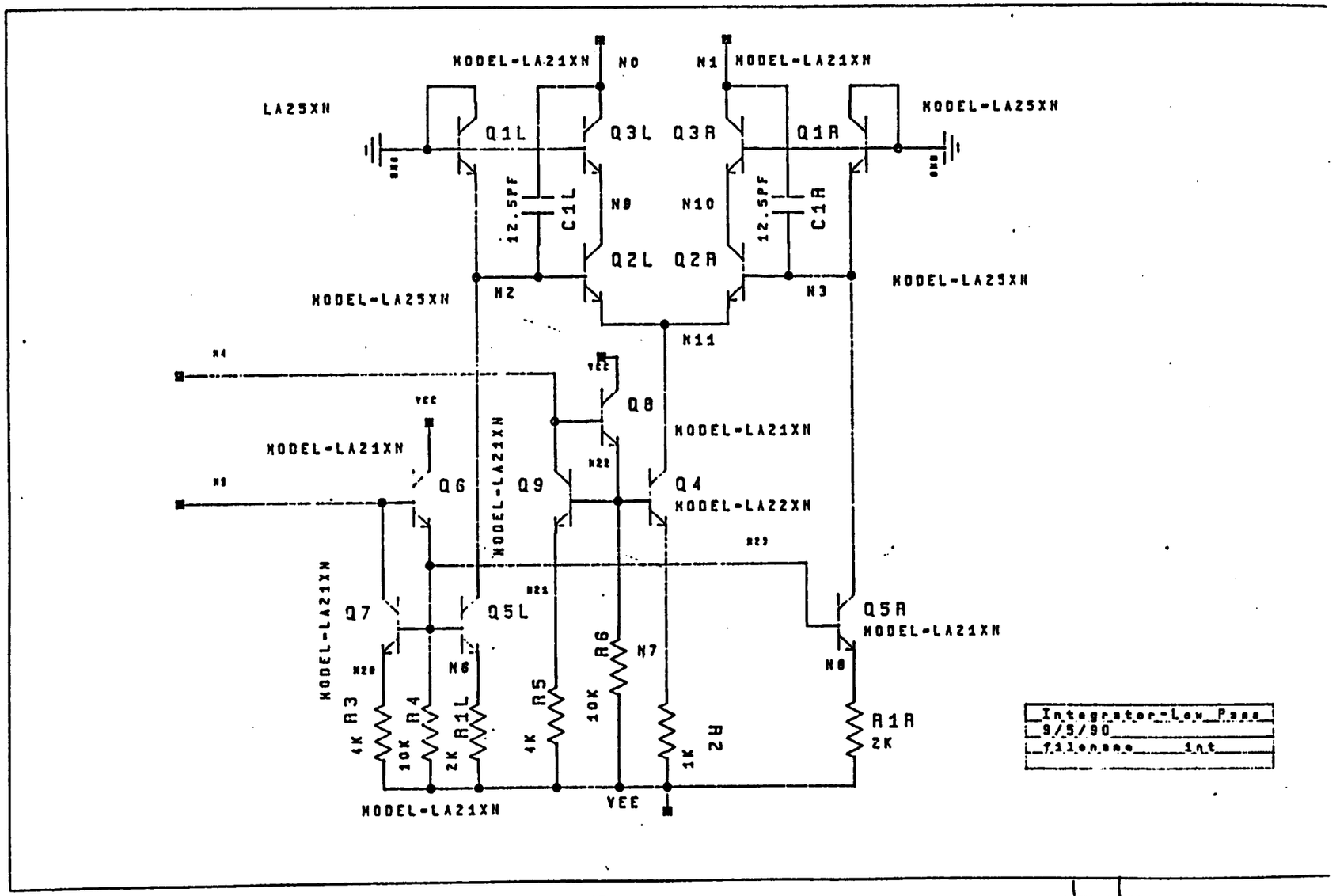


Stage interconnection



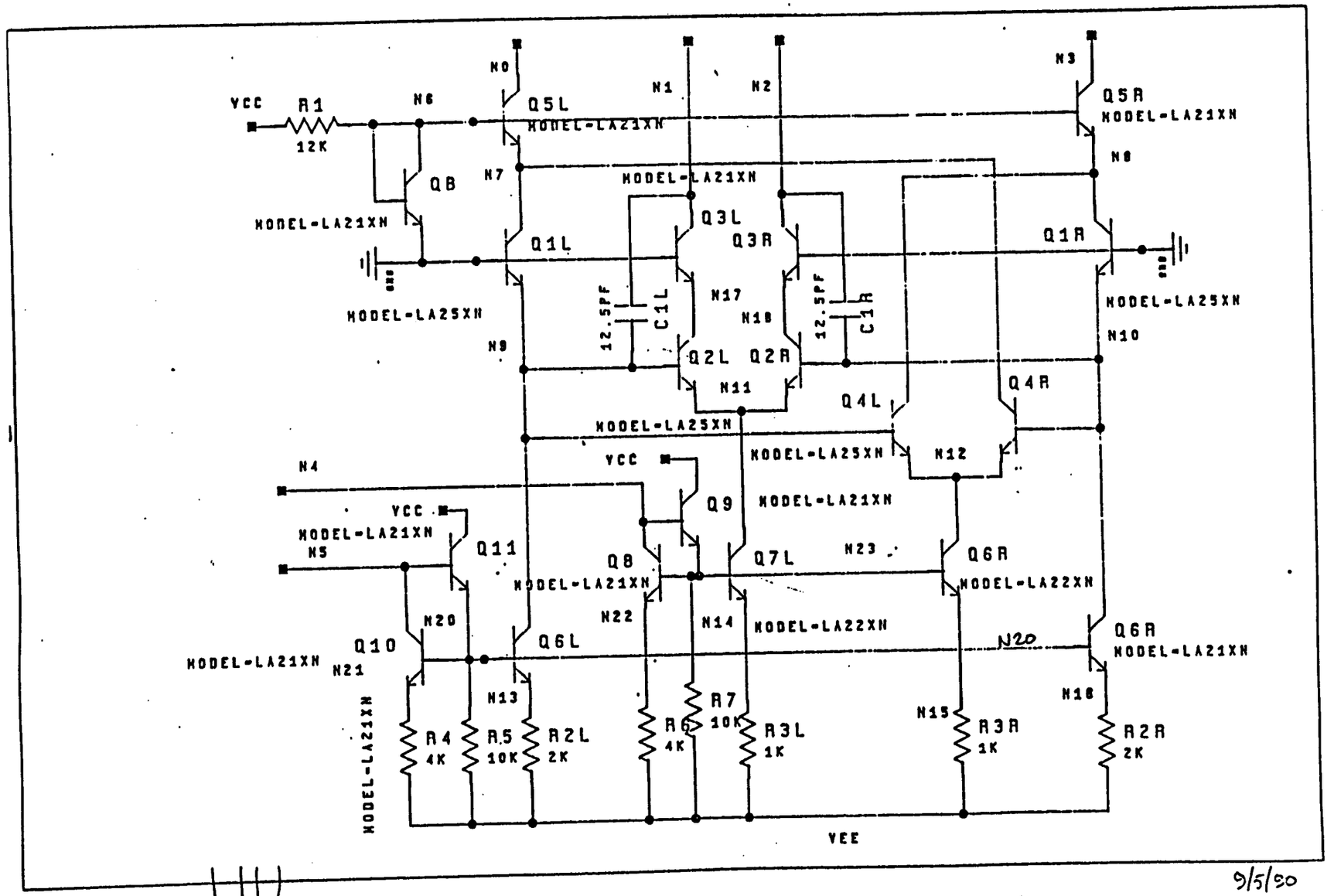
V2I stage essential between LP & next stage

" " optional " HP & next stage


MODEL=LA21XN
N0
N1
MODEL=LA21XN
LA25XN
MODEL=LA25XN
Q1L
Q3L
Q3R
Q1R
12.5PF
C1L
N9
N10
12.5PF
C1R
Q2L
Q2R
MODEL=LA25XN
N2
N3
MODEL=LA25XN
N11
N4
VCC
Q8
MODEL=LA21XN
MODEL=LA21XN
Q6
Q9
Q4
MODEL=LA22XN
N5
N22
MODEL=LA21XN
N23
N21
Q7
Q5L
Q5R
MODEL=LA21XN
N20
N6
N7
N8
4K R3
10K R4
2K R1L
4K R5
10K R6
1K R2
R1R
2K
MODEL=LA21XN
VEE
Integrator-Low Pass
9/5/90
filename int

Low-Pass

2 OF



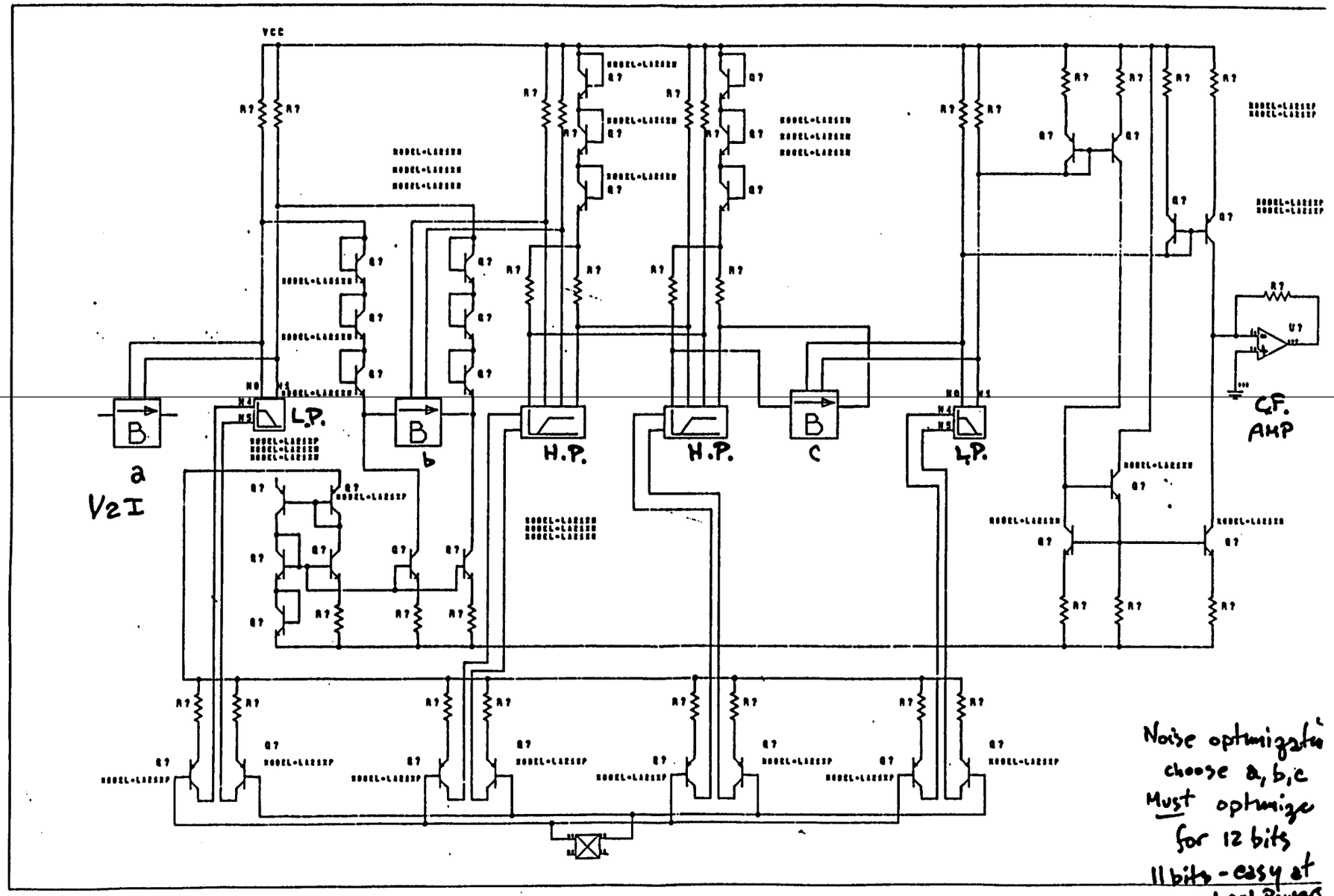
9/5/90

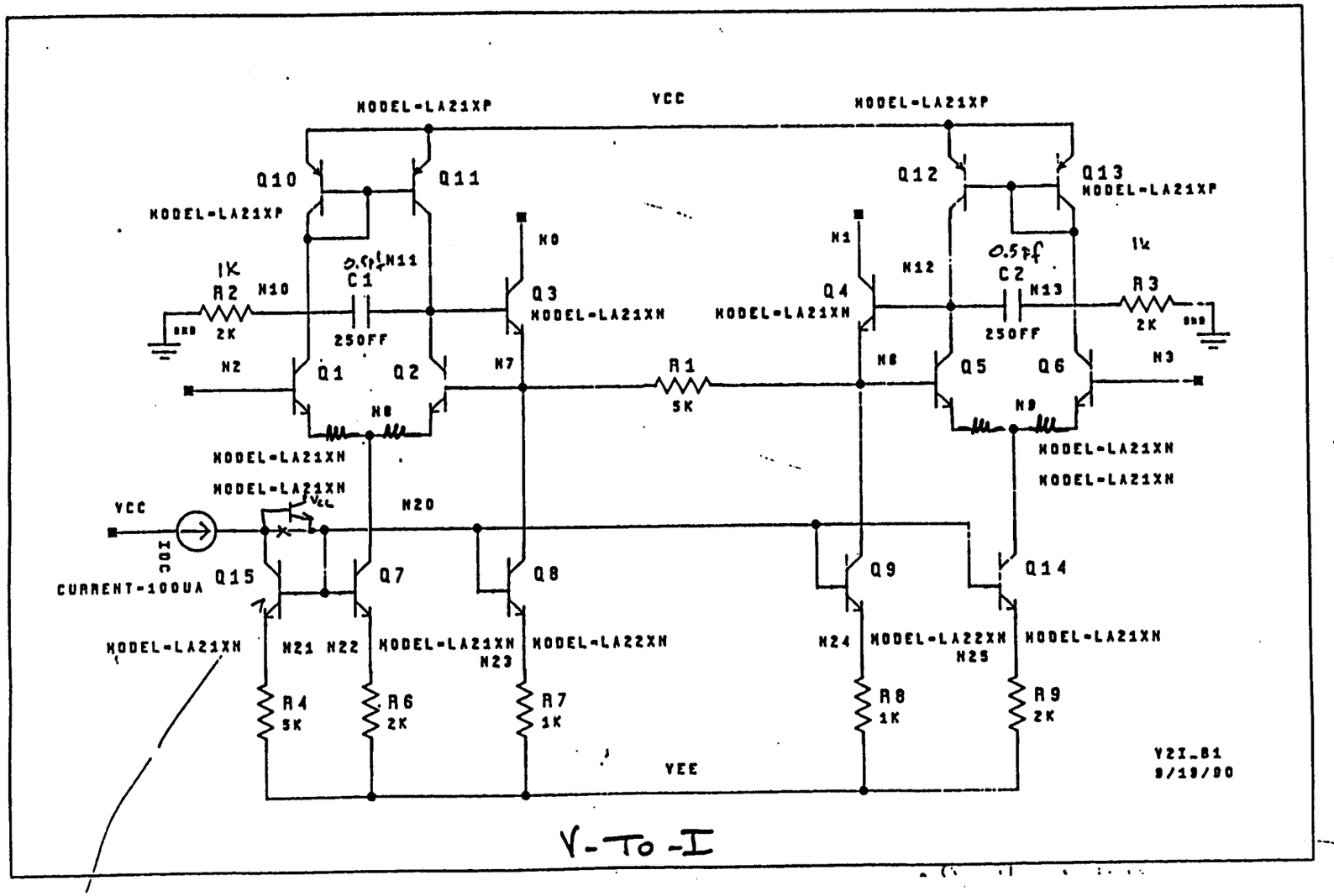
2 OF

41

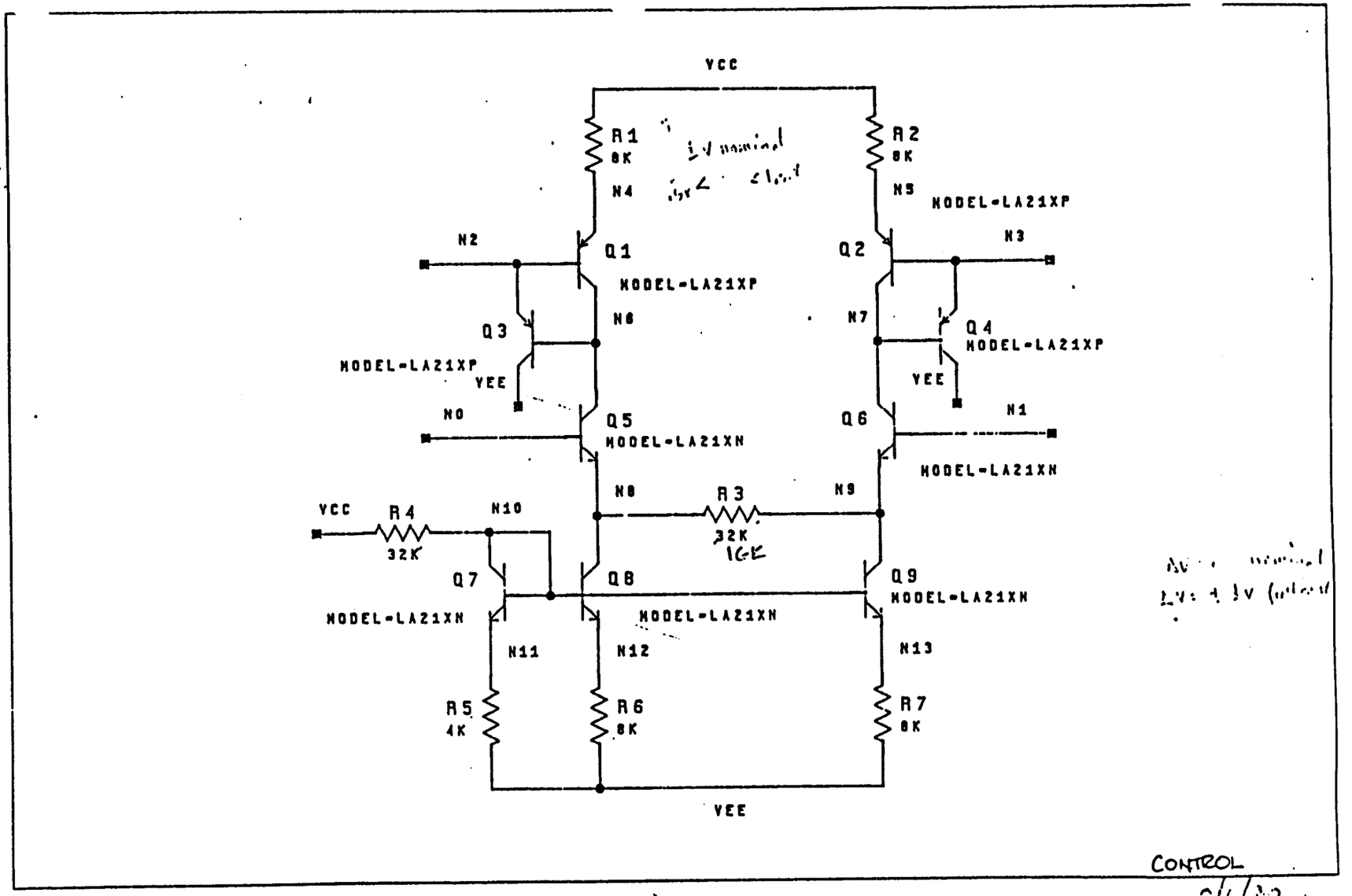
High Bias

Overall Structure




MODEL=LA21XP
VCC
MODEL=LA21XP
Q10
Q11
Q12
Q13
MODEL=LA21XP
MODEL=LA21XP
N0
N1
1K
R2
N10
C1
N11
Q3
MODEL=LA21XN
Q4
MODEL=LA21XN
N12
C2
N13
R3
1K
2K
250FF
2K
250FF
N2
Q1
Q2
N7
R1
5K
N8
Q5
Q6
N3
N8
N9
MODEL=LA21XN
MODEL=LA21XN
MODEL=LA21XN
MODEL=LA21XN
VCC
N20
100
CURRENT=100UA
Q15
Q7
Q8
Q9
Q14
MODEL=LA21XN
N21
N22
MODEL=LA21XN
N23
MODEL=LA22XN
N24
MODEL=LA22XN
N25
MODEL=LA21XN
R4
5K
R6
2K
R7
1K
R8
1K
R9
2K
VEE
V2I_81
9/19/90

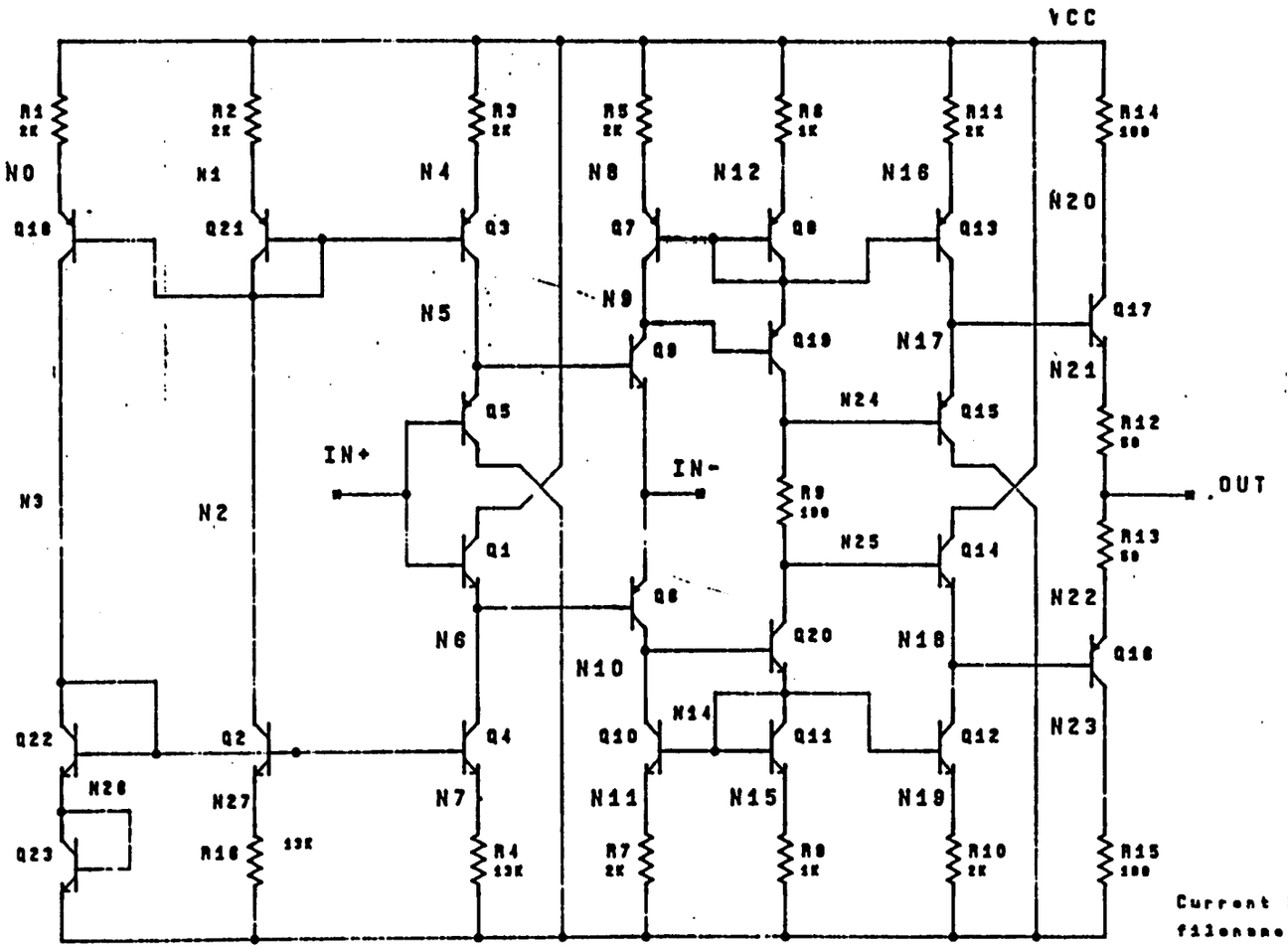
V-To-I



1 of

CURRENT SOURCES
TIE INTO @ N3 & N2

CONTROL CURRENT SOURCE

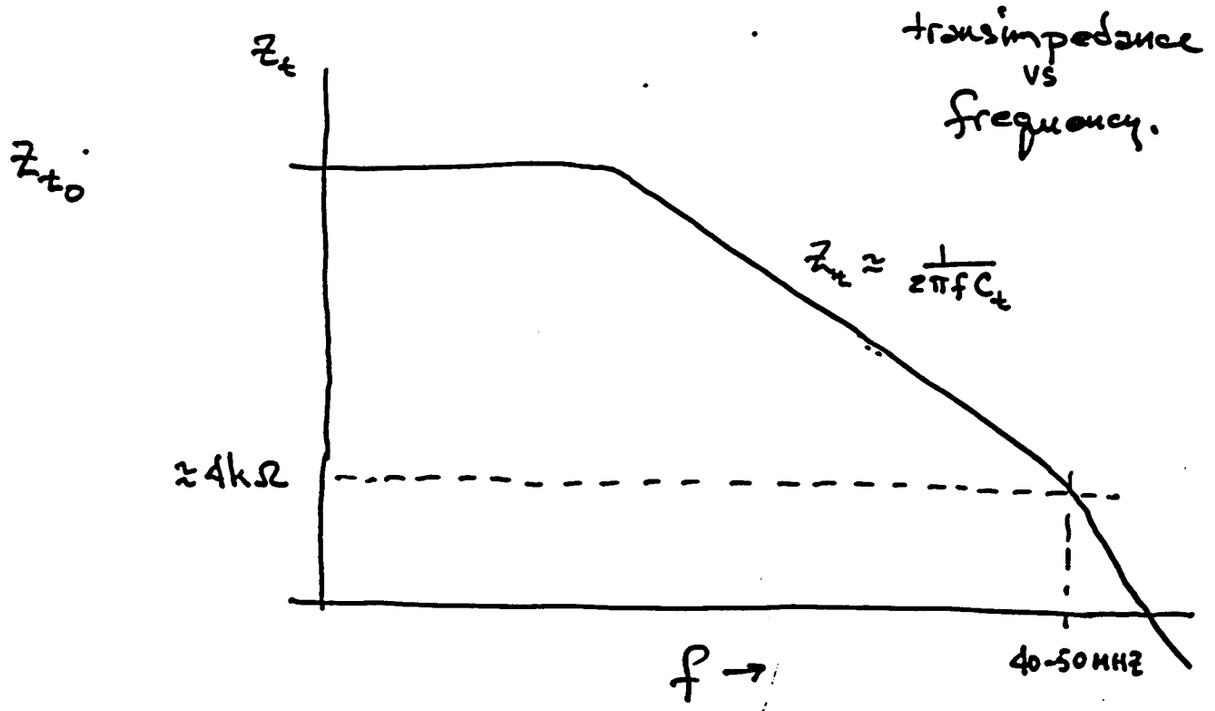


Current Feedback Op-amp
filename : cfamp
11/5/90 J.D.

P ≅ 5 mW

Z_c = 5MEG || 1pf

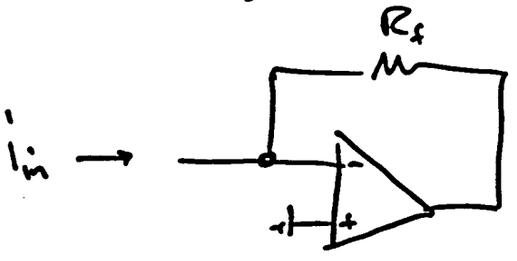
Current feedback op-amp specs.



transimpedance vs frequency.

$Z_{t_0} > 5$ MHz
$C_t \approx 1$ pf
@ $P_D = 5$ mW

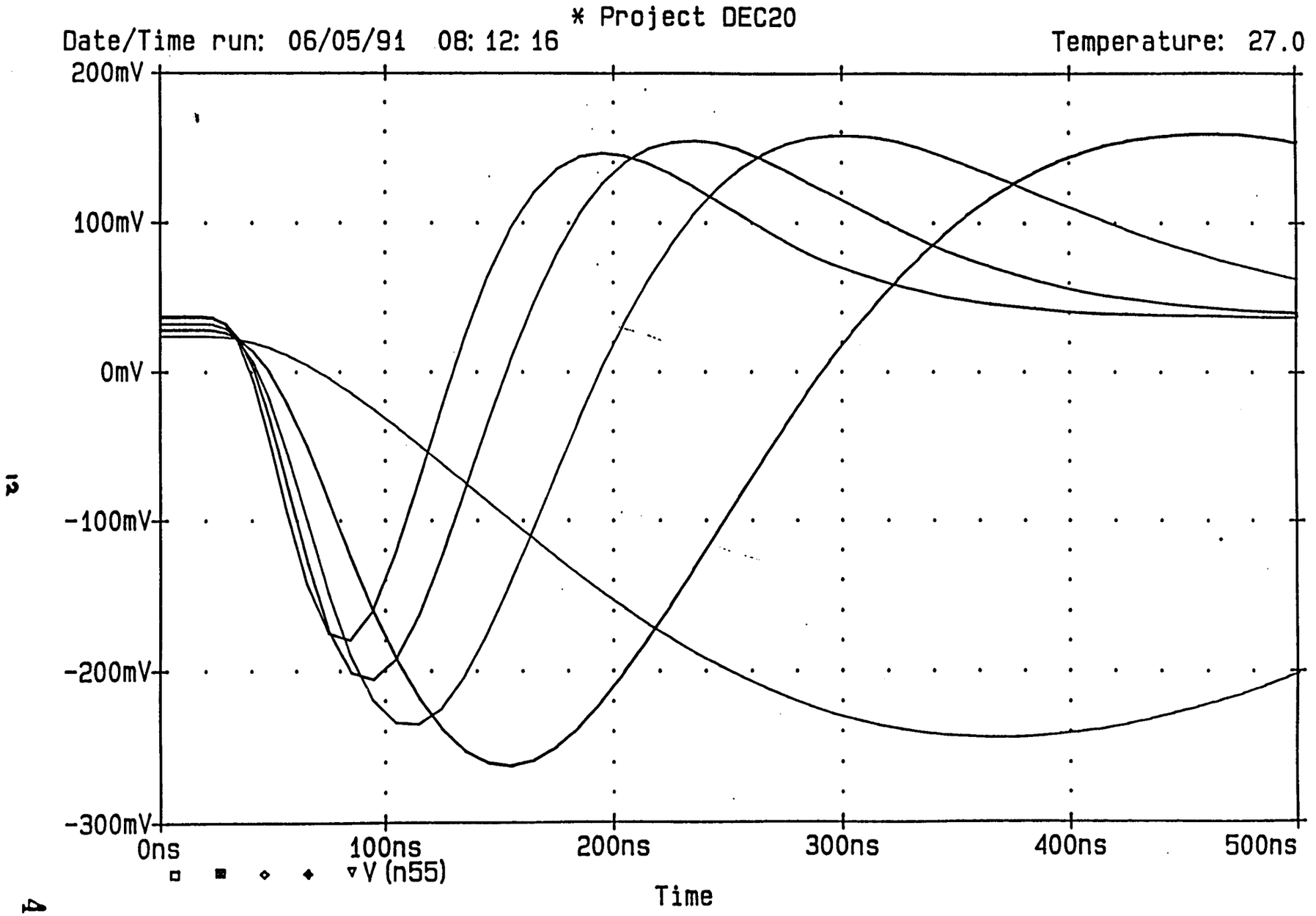
} eg. ATT ALA202 transistor parameters.



For stability $R_f \gtrsim 4k$

Signal risetime $\tau = R_f \cdot C_t$

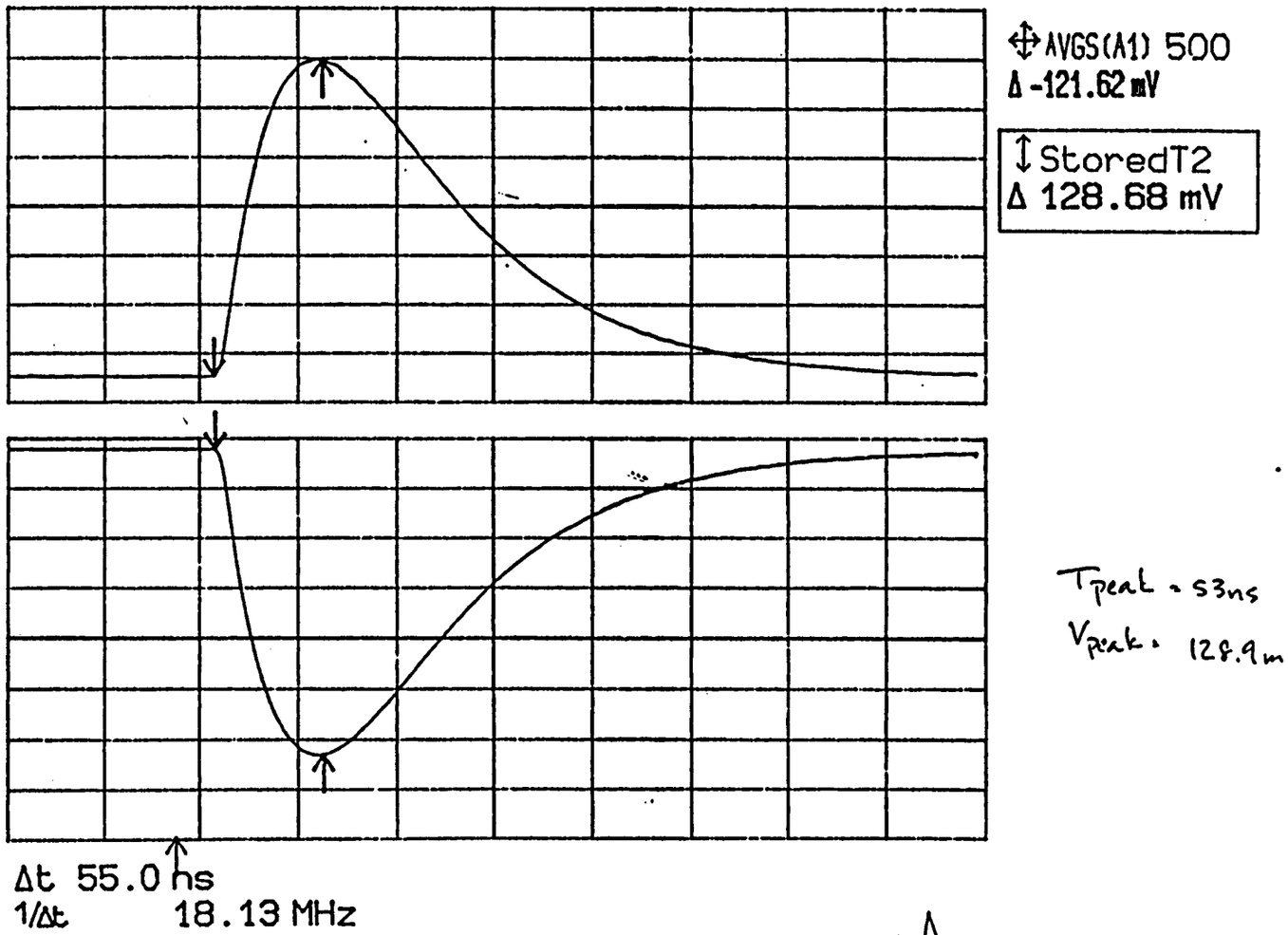
eg. $8k\Omega \cdot 1pf = 8ns$



5:1 tuning rang

SCOPE TRACE OF 2-POLE TEST CIRCUIT USING CA3127 TRANSISTOR PACKAGES

TUNING RANGE = 50-110 ns (2.2 ii)



Tpeak = 53ns

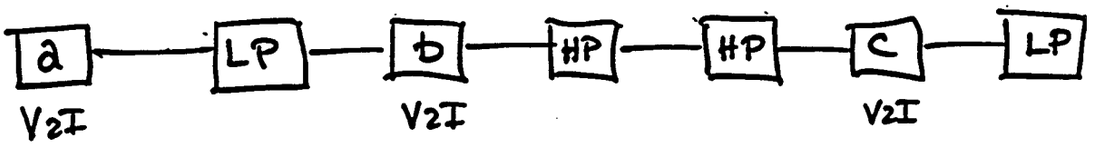
Vpeak = 128.9mv

58mV

88ns

120ns

NOISE PERFORMANCE / OPTIMIZATION



1. We have 3 free parameters: interstage V2I gains "a", "b", "c"

2. For a fixed overall gain product a·b·c is fixed

3. Noise of each shaper stage is dominated by collector shot noise but many other sources contribute.

4. From SPICE models we can get an empirical expression for noise vs. stage current. Empirical fit is linear:

   (i_{rms} vs. I_{bias})

   (shot noise alone would produce $i_n \propto \sqrt{I_{bias}}$)

∴ Bias currents in stages are determined by interstage V2I gains.

$$I_{bias} > I_{signal}$$

We have set $I_{bias} = (1 + 25\%) \cdot I_{signal_{max}}$

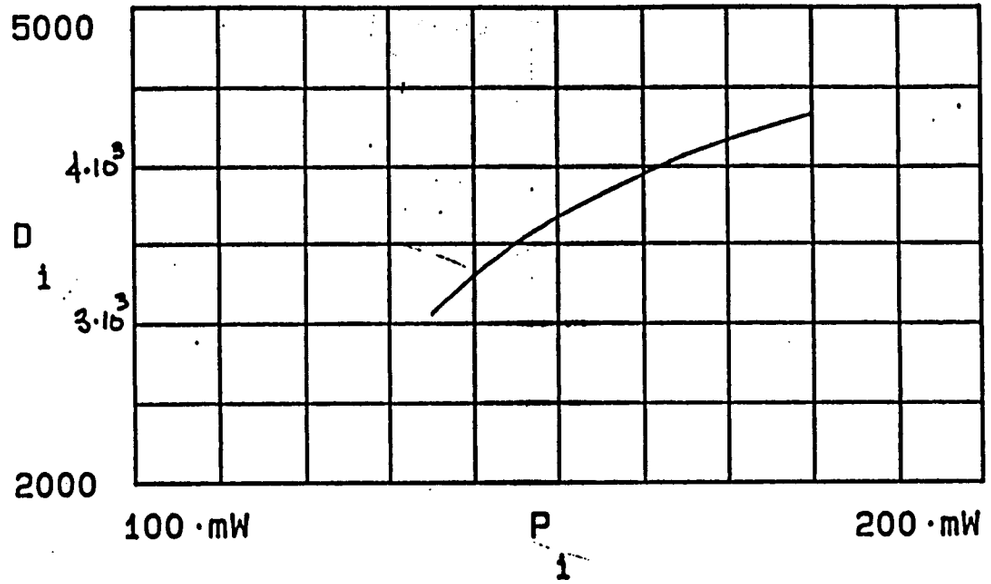
6. Total device power is a function of "a" & "b"

7. Total device noise is a function of "a", "b"

∴ At fixed power, choose "a" & "b" which minimize noise.

Optimum Dynamic Range
vs
Power Dissipation

GAIN = 0.4 Iin = 625·μa Vout (a, b) = 4 Volts



CONCLUSIONS based on SPICE & test circuits.

1. $\leq \frac{1}{4}\%$ non-linearity

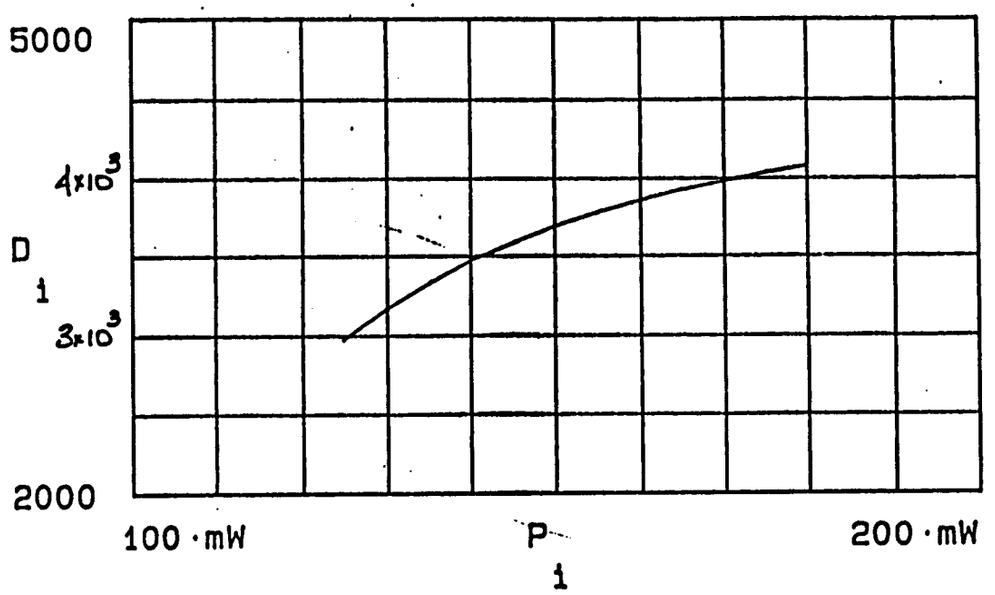
2. Power dissipation is function of required dynamic range (SNR)
   $\Rightarrow \approx$ 200mW @ 12 bits

3. Tuning range ≥ 3
   (high speed operation limited by slew rate)

4. Can trade tuning range for
   (a) lower power
   (b) lower noise
   by adding fixed capacitance.

Optimum Dynamic Range
vs
Power Dissipation

GAIN = 0.625 Iin = 400·μa Vout (a, b) = 4 Volts

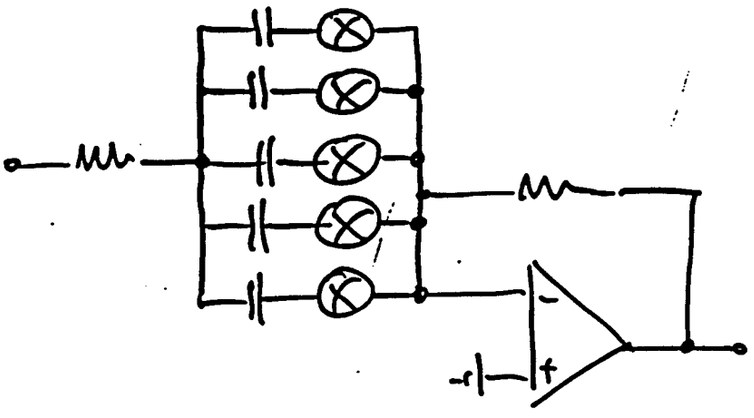


Bi CMOS - shapers

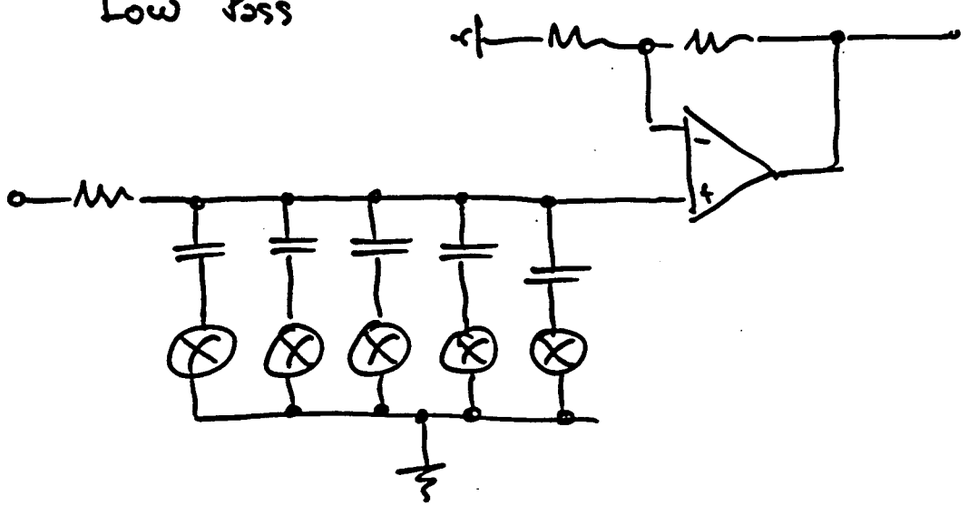
1. Use CMOS switches to select capacitance or resistance in traditional RC shaper circuits.

eg.

High pass



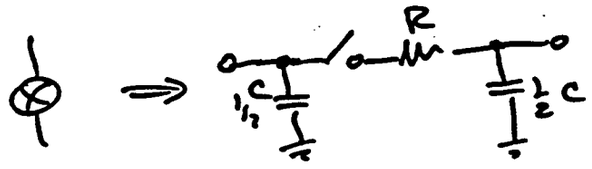
Low Pass



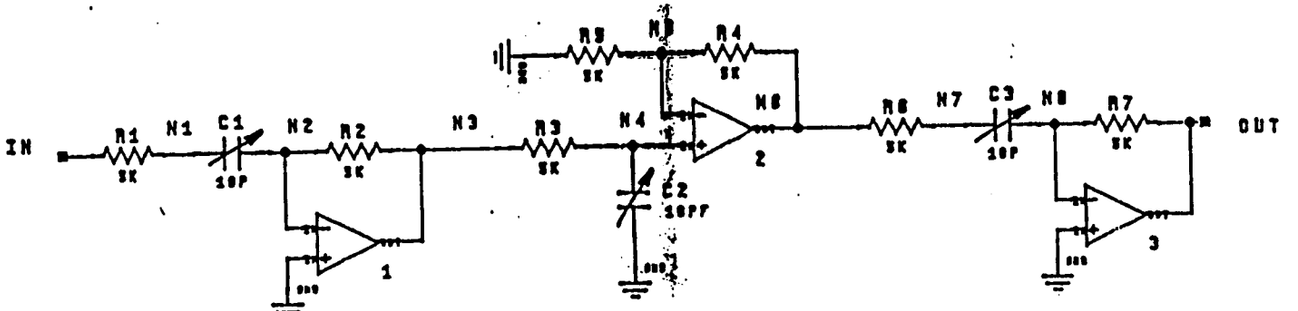
<u>observations</u> so far, using Westinghouse "workhorse" BiCMOS process, & high speed EKS proces

1. Op amp used for simulation is current feedback type (Z_t = 5Meg‖ 1pf) @ 5mW
2. 3 pole shaper design HP - LP - HP
3. Non linearity ≈ 0.1 % SNR ≈ 10,000
4. Tuning range ≈ 2-3 : 1
5. "Workhorse" BiCMOS process has CMOS switches which are too large - C_{ds} too high

   — EKS process has much smaller CMOS transistors
6. Serious simulations using EKS <u>pending</u> Westinghouse design seminar
7. semi-idealized switches used for simulation

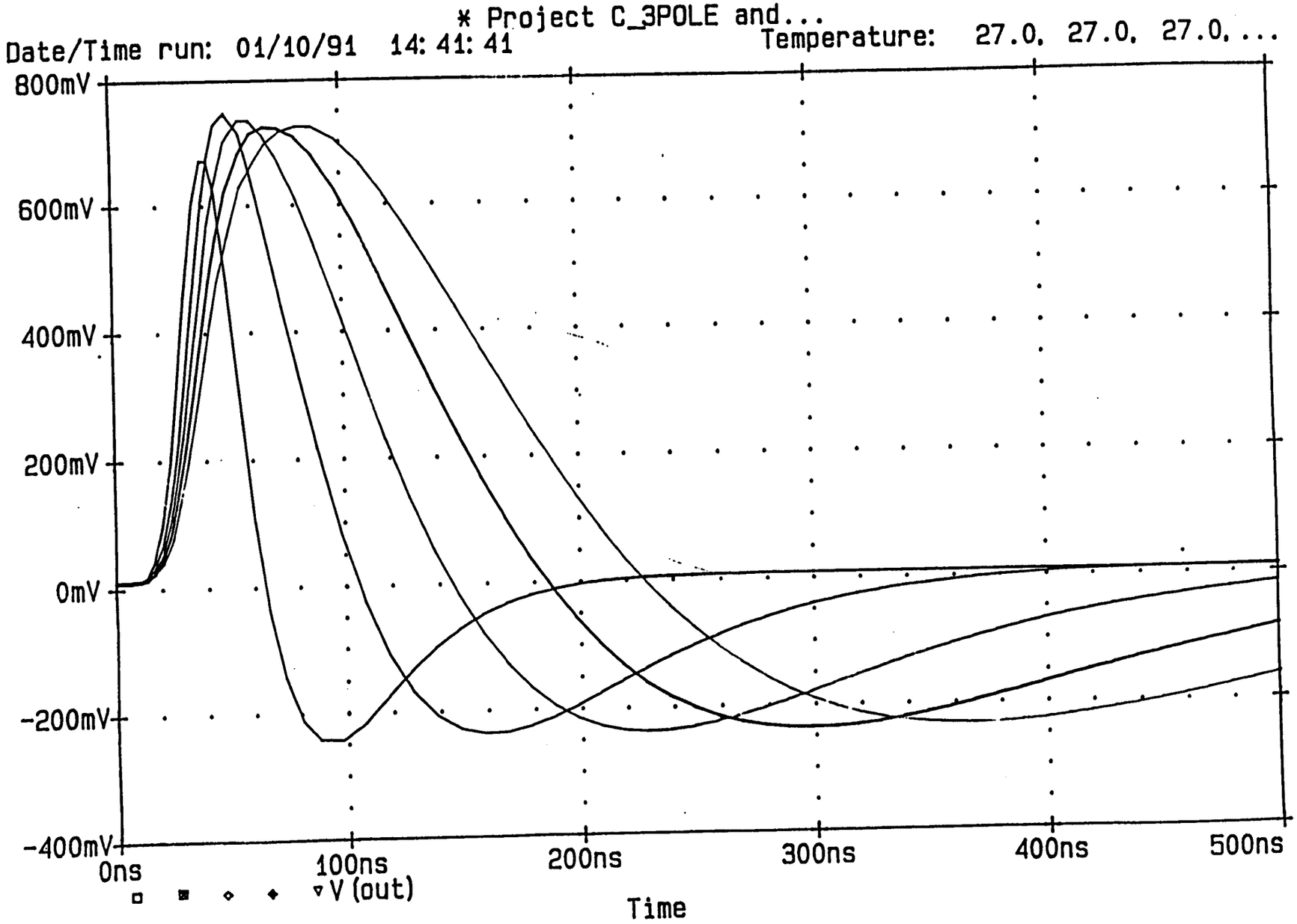


eg. 3-pole bipolar shaper



C_3pole
Variable capacitor shaper
1-10-91 J.O.

P=15 mW



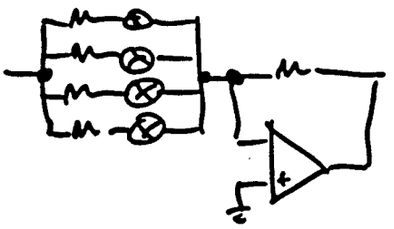
23.

$T_{peak} \cong 30 - 90$ ns

57

Conclusions - With BiCMOS process we can incorporate

1. Shaping
2. Fine gain adjust
3. Programmable gain



4. 8 bit bus interface with internal registers for 1. - 3.

5. $\approx \leq 5$mW per op-amp + higher power stage at output

   $\approx$ 75 mW/channel (a guess)

Fast Variable Pulse Shaping

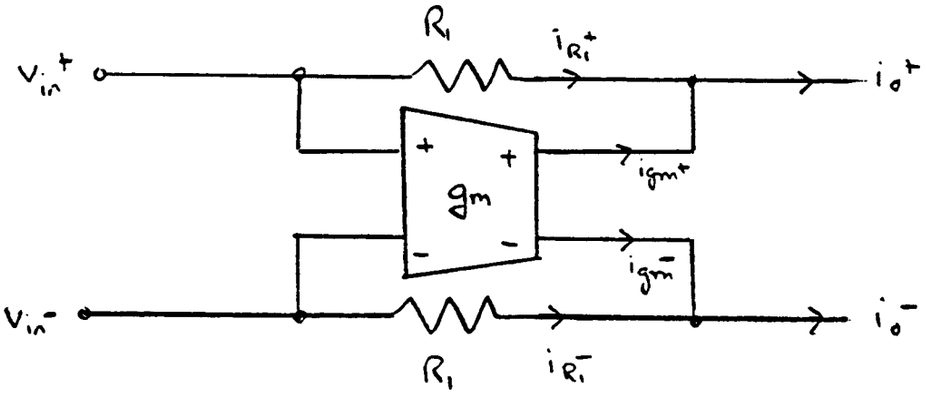
P. O'Conner (BNL)

ELECTRONICALLY CONTROLLED CONDUCTANCE FOR MONOLITHIC SHAPER

In most monolithic silicon processes, passive components have absolute tolerances no better than ± 20%.

Most shaping amplifiers rely on an RC product to set the peaking time. Straightforward implementation in a monolithic process could result in 2X variation in τ_p.

A variable resistance can be obtained by placing a small, variable transconductance in parallel with a passive resistance.



The outputs are attached to low impedance virtual ground

$$g_m = \frac{i_{gm}^+ - i_{gm}^-}{V_i^+ - V_i^-}$$

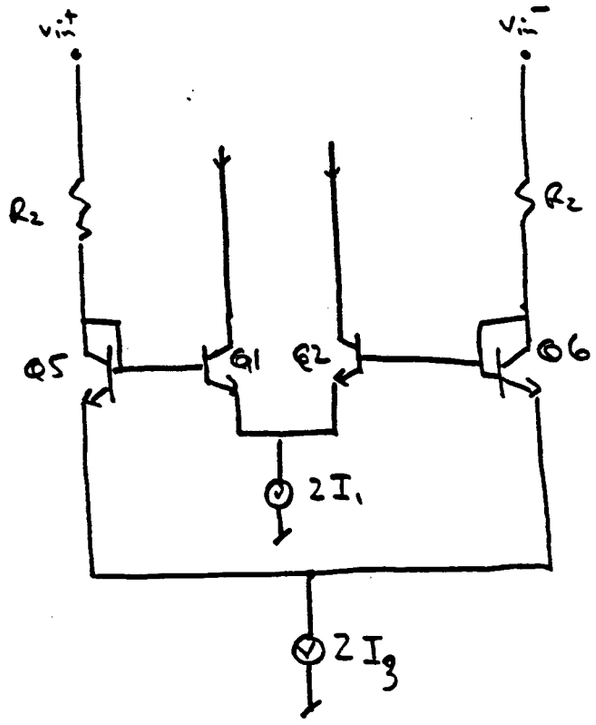
$$i_o^+ - i_o^- = i_{R_1}^+ - i_{R_1}^- + i_{gm}^+ - i_{gm}^-$$

$$G = \frac{i_o^+ - i_o^-}{V_i^+ - V_i^-} = \frac{i_{R_1}^+ - i_{R_1}^-}{V_i^+ - V_i^-} + \frac{i_{gm}^+ - i_{gm}^-}{V_i^+ - V_i^-}$$

$$= \frac{1}{R_1} + g_m$$

By making g_m variable we can correct for the process spread of R_1. Since g_m can be small compared to $1/R_1$, most of the signal current flows in the passive resistor. Hence g_m has reduced impact on high-frequency, linearity, and noise behavior.

Variable ~~transconductance~~ active conductance



For small signals

$$i_5 - i_6 = \frac{v_{in}^+ - v_{in}^-}{R_2}$$

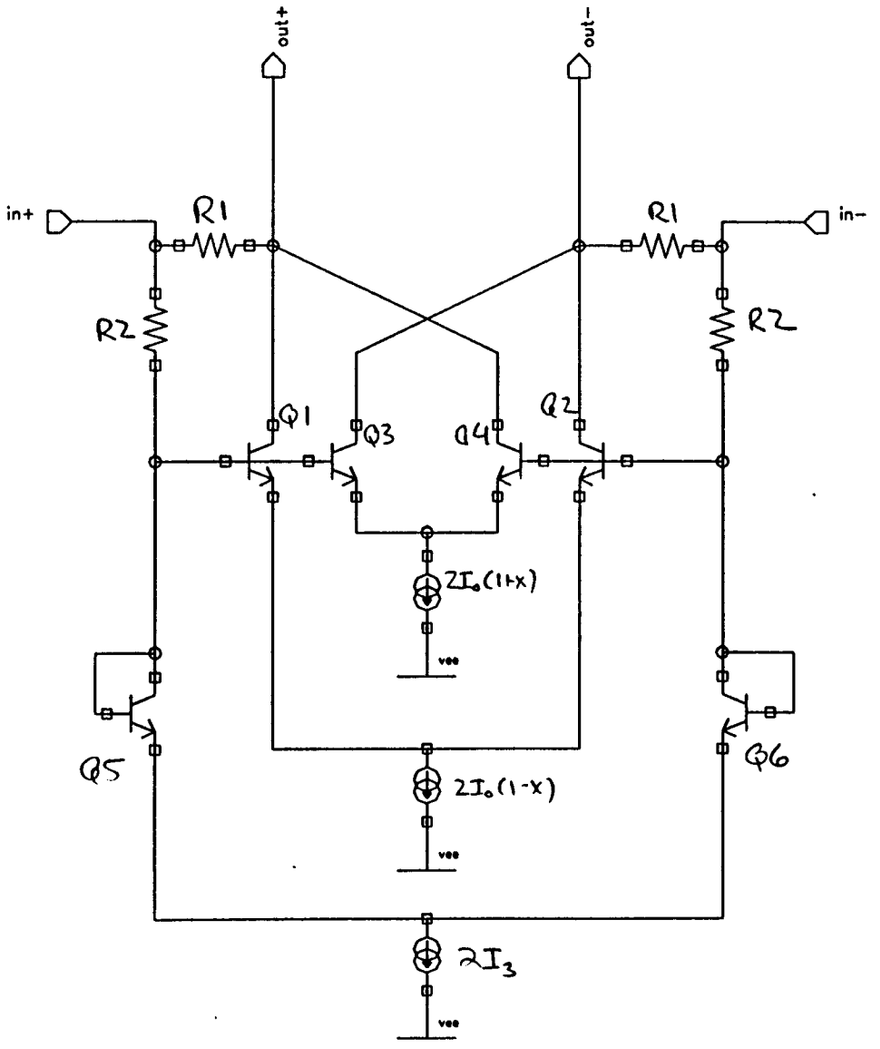
By translinear principle

$$\frac{i_1 - i_2}{i_5 - i_6} = \frac{I_1}{I_3}$$

So

$$g_m \equiv \frac{i_1 - i_2}{v_{in}^+ - v_{in}^-} = \frac{1}{R_2} \cdot \frac{I_1}{I_3}$$

which can be varied by changing the ratio I_1/I_3



$$G = \frac{1}{R_1} + \frac{1}{R_2}\,\chi\left(\frac{I_0}{I_3}\right)$$

fixed variable

Tradeoffs with this circuit:

— linear input range

$$V_{in,max} \sim 2 I_3 R_2 \qquad (1\%)$$

— tuning range

$$\frac{\Delta G}{G} = \frac{R_1 I_0}{R_2 I_3}$$

— power

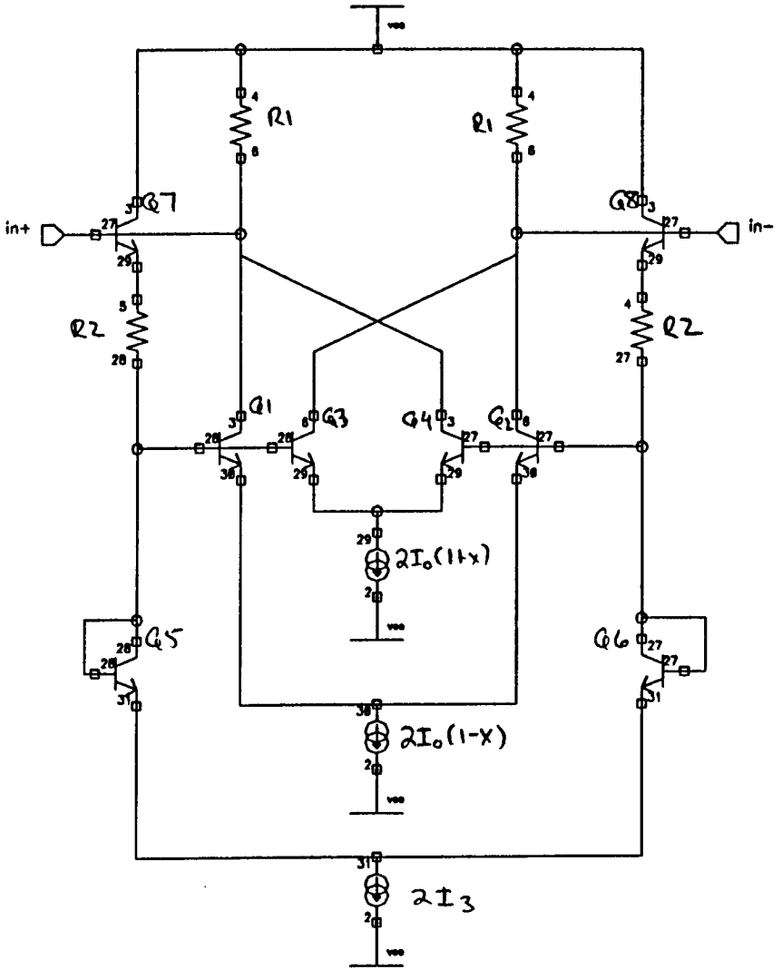
$$(V_{cc} - V_{ee})(2I_3 + 2I_0)$$

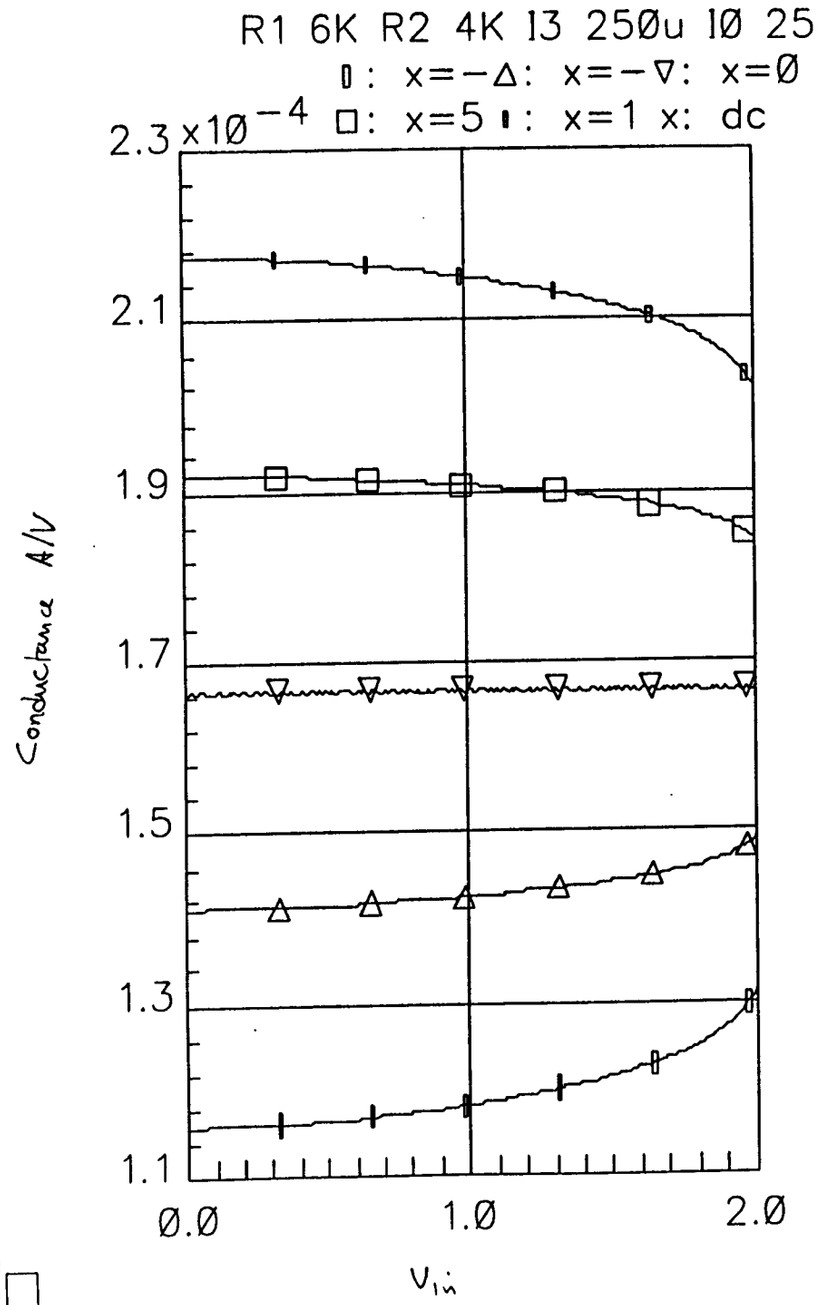
— noise - dominated by Q1-Q4

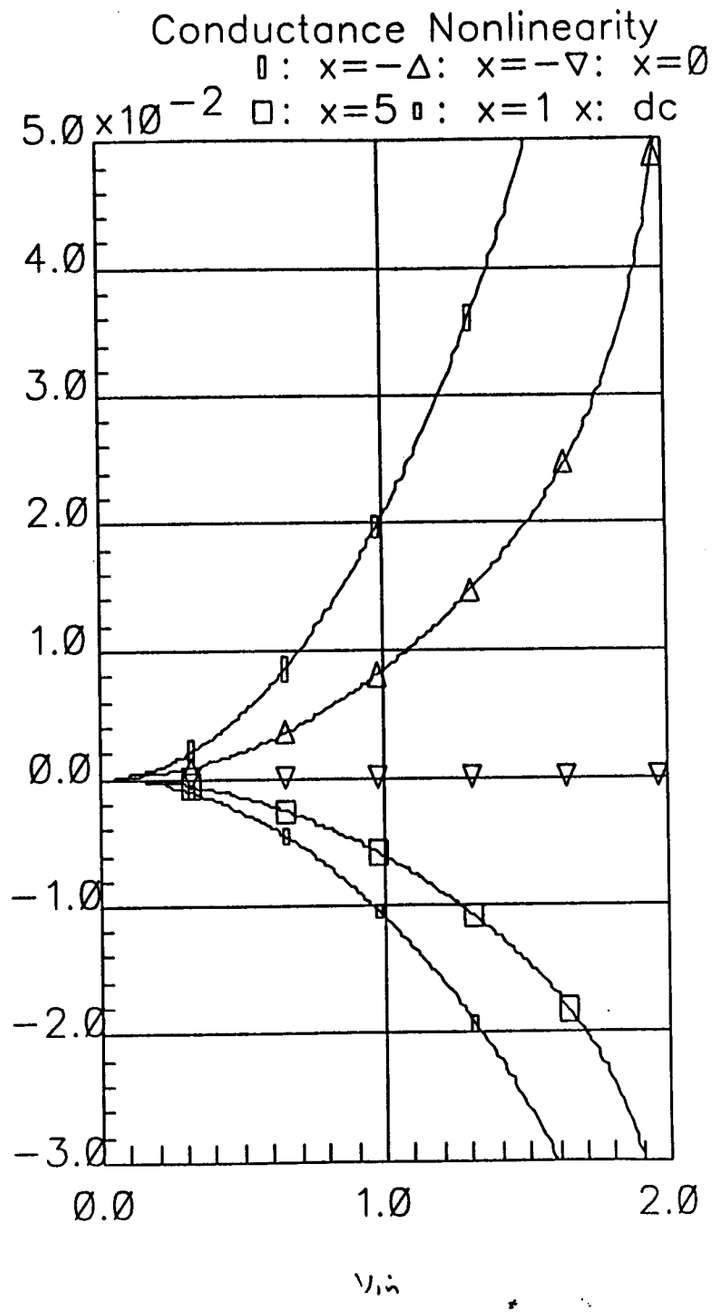
$$\frac{\text{noise contributed by tuning ckt.}}{\text{noise of } R_1} = \sqrt{\frac{q I_0 R_1}{kT}}$$

vregnd

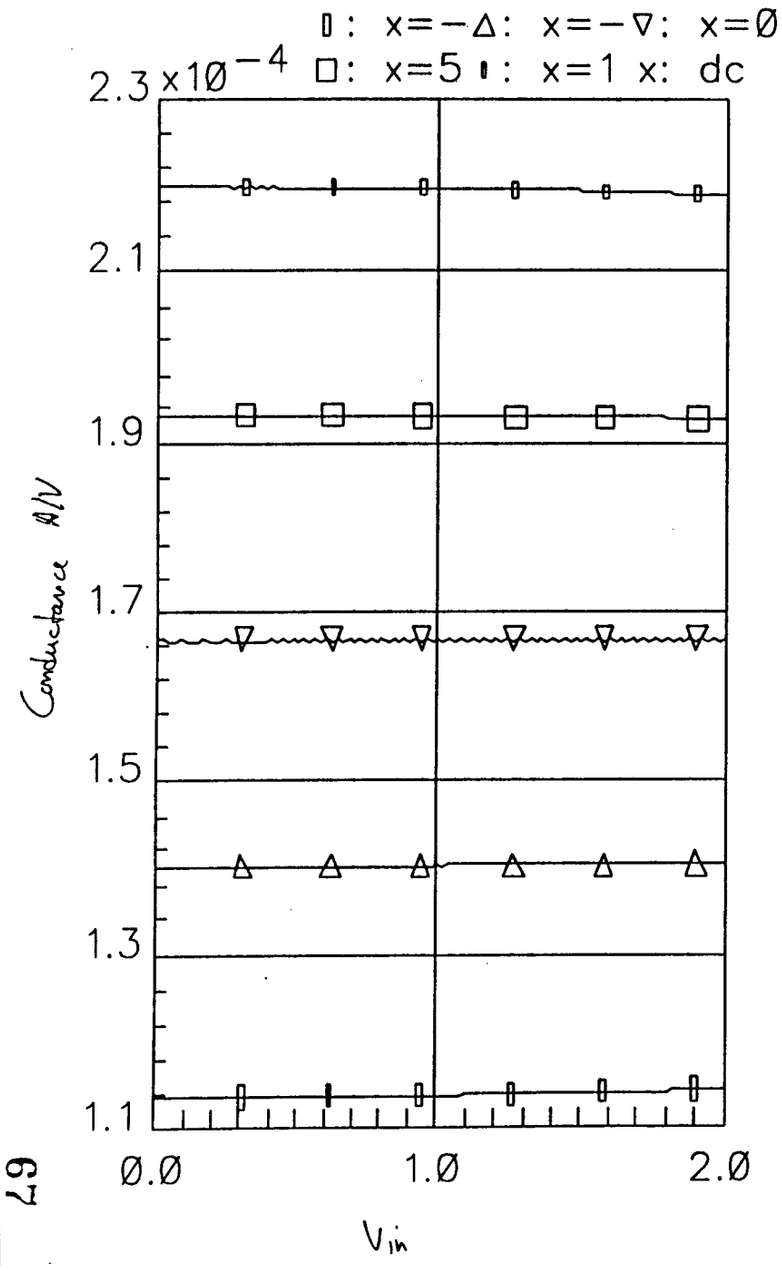
5/6/91

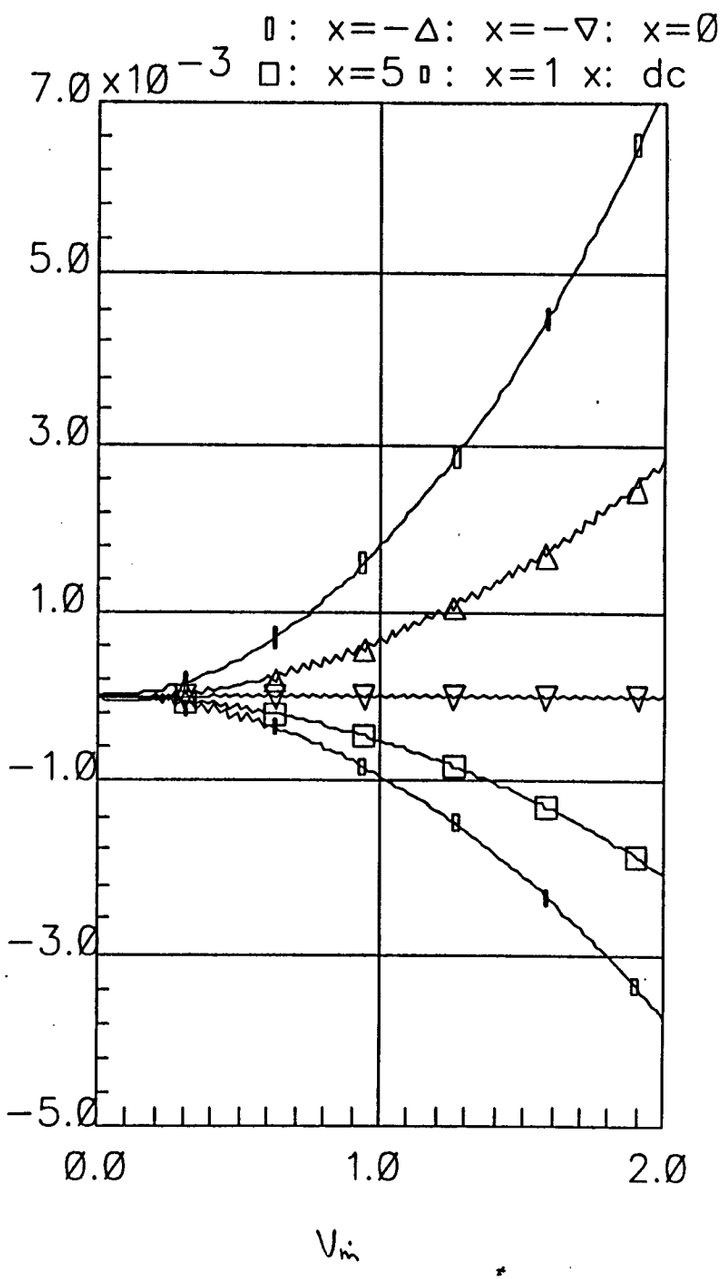



R1 6K R2 4K I3 250u I0 25u
▯: x=−Δ: x=−∇: x=Ø
□: x=5 ▮: x=1 x: dc
2.3 x10^−4
2.1
1.9
1.7
1.5
1.3
1.1
Conductance A/V
Ø.Ø
1.0
2.Ø
V_in

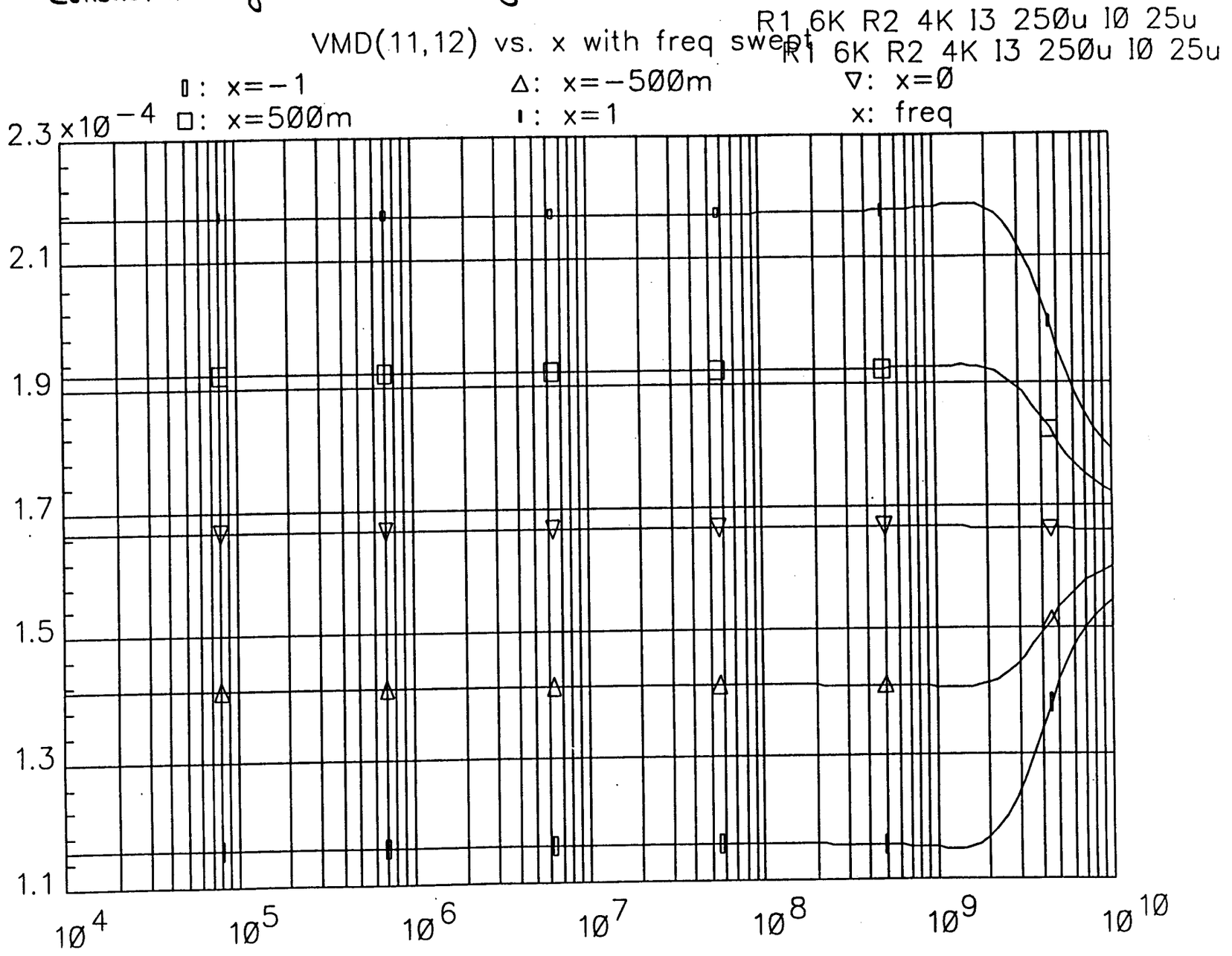

Conductance Nonlinearity
▯: x=−Δ: x=−∇: x=Ø
□: x=5 ▯: x=1 x: dc
5.Ø x10^−2
4.Ø
3.Ø
2.Ø
1.Ø
Ø.Ø
−1.Ø
−2.Ø
−3.Ø
Ø.Ø
1.Ø
2.Ø
V_in

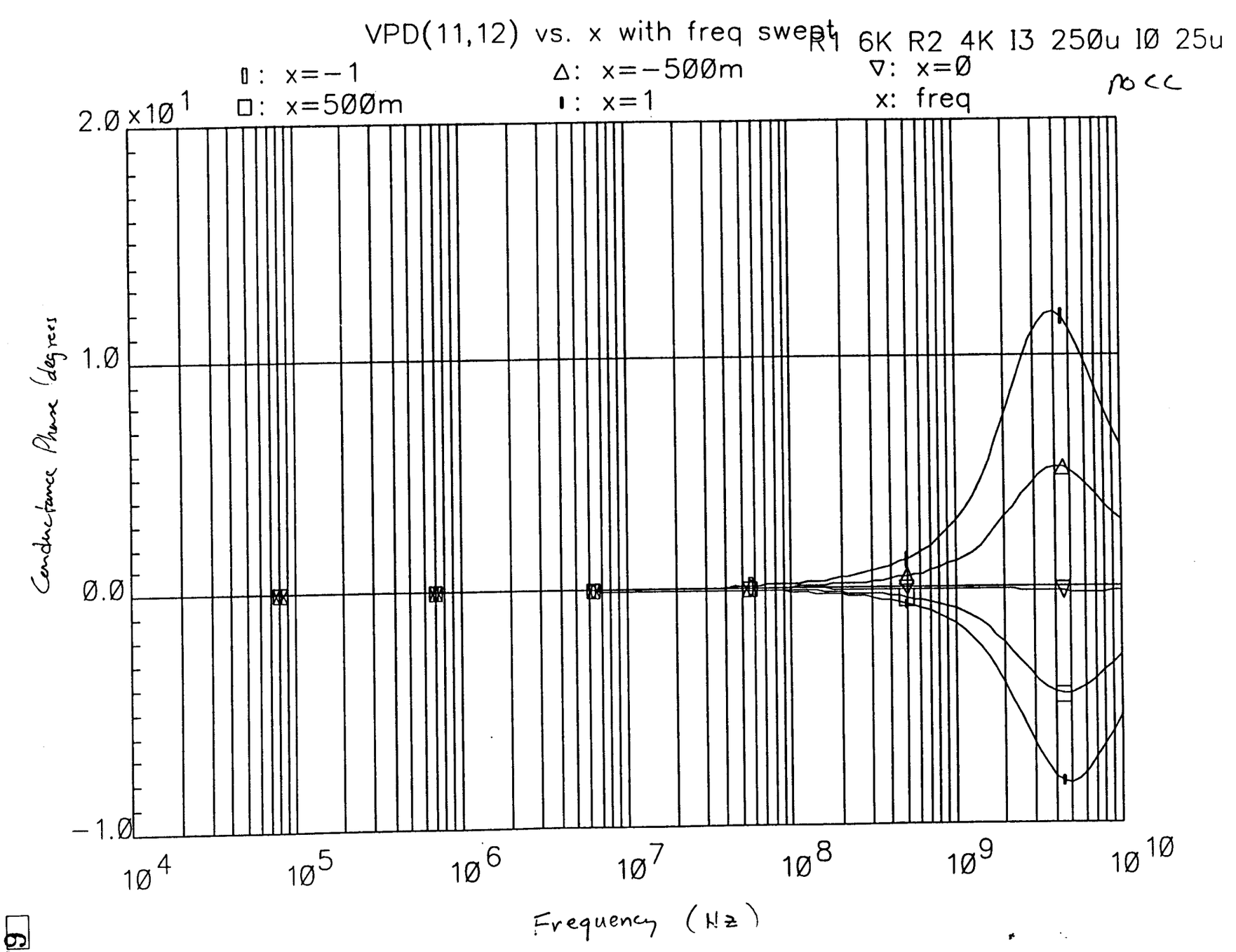
R1 6K R2 8K I3 500u I0 100u



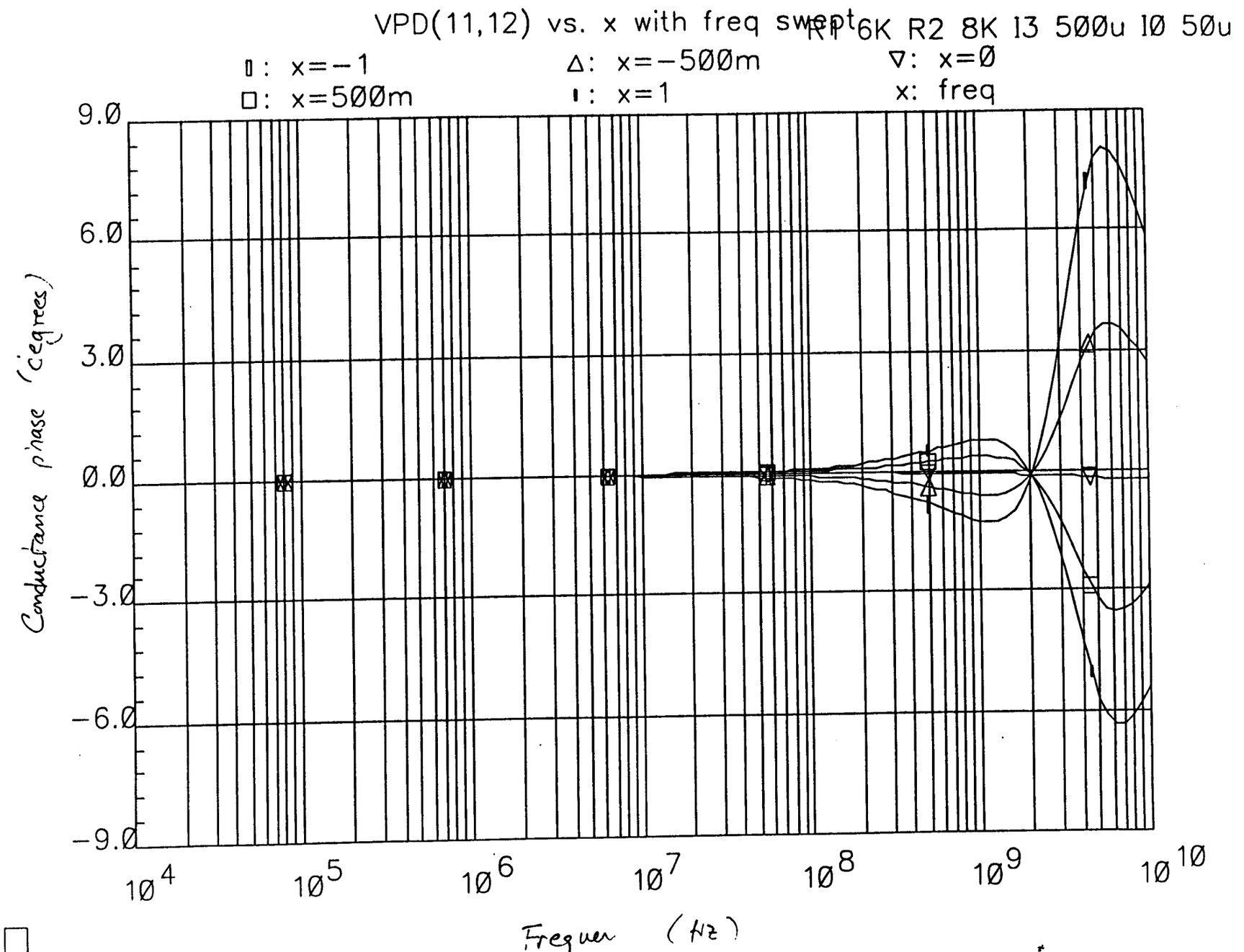


Conductance magnitude vs frequency

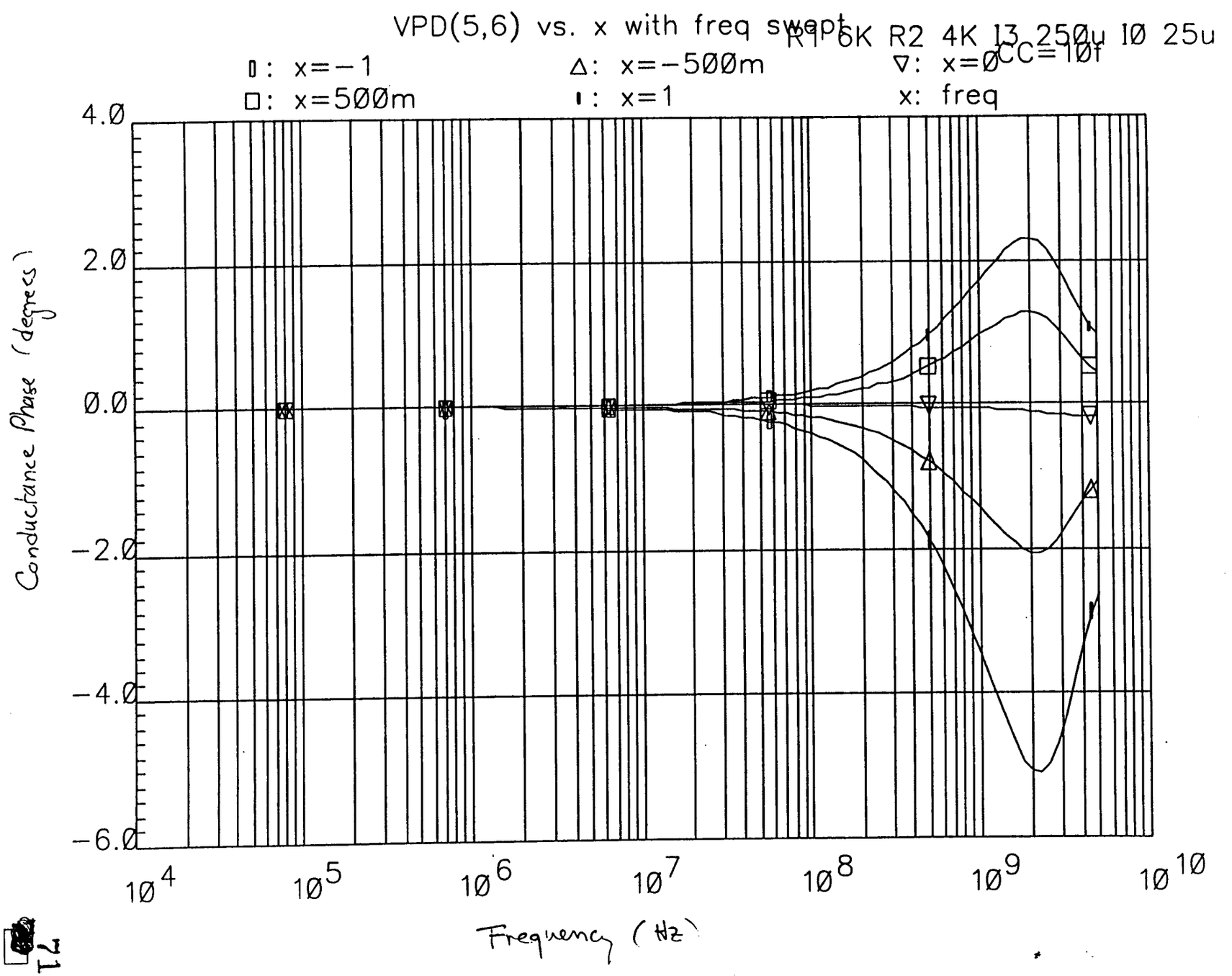



VPD(11,12) vs. x with freq swept
R1 6K R2 4K I3 250u I0 25u
▯: x=−1
□: x=500m
Δ: x=−500m
▮: x=1
▽: x=0
x: freq
2.0 x10^1
1.0
0.0
−1.0
Conductance Phase (degrees)
10^4
10^5
10^6
10^7
10^8
10^9
10^10
Frequency (Hz)

Phase


VPD(11,12) vs. x with freq swept
R1 6K R2 8K I3 500u I0 50u
▯: x=−1
△: x=−500m
▽: x=0
□: x=500m
▮: x=1
x: freq
9.0
6.0
3.0
0.0
−3.0
−6.0
−9.0
Conductance phase (degrees)
10^4
10^5
10^6
10^7
10^8
10^9
10^10
Frequency (Hz)

0L□

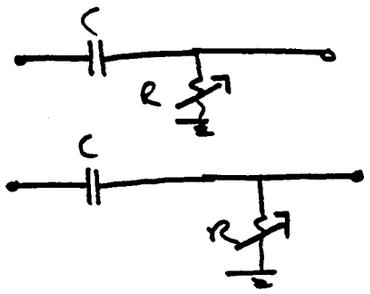


VPD(5,6) vs. x with freq swept
R1 6K R2 4K I3 250u I0 25u
CC=10f
▯: x=−1
□: x=500m
△: x=−500m
▮: x=1
▽: x=0
x: freq
4.0
2.0
0.0
−2.0
−4.0
−6.0
Conductance Phase (degrees)
10^4
10^5
10^6
10^7
10^8
10^9
10^10
Frequency (Hz)

71

Making a shaper with this circuit

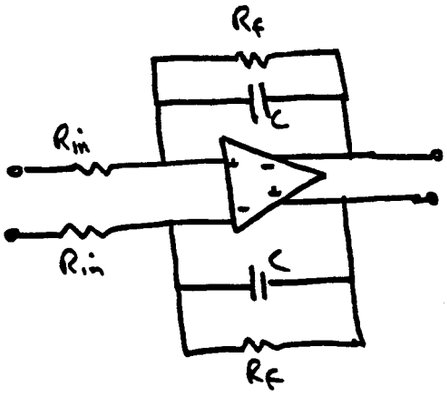
High pass element



$$H(s) = \frac{s\tau}{1+s\tau} \qquad \tau = RC$$

- the variable resister has to be modified slightly to be used in this configuration

Low pass

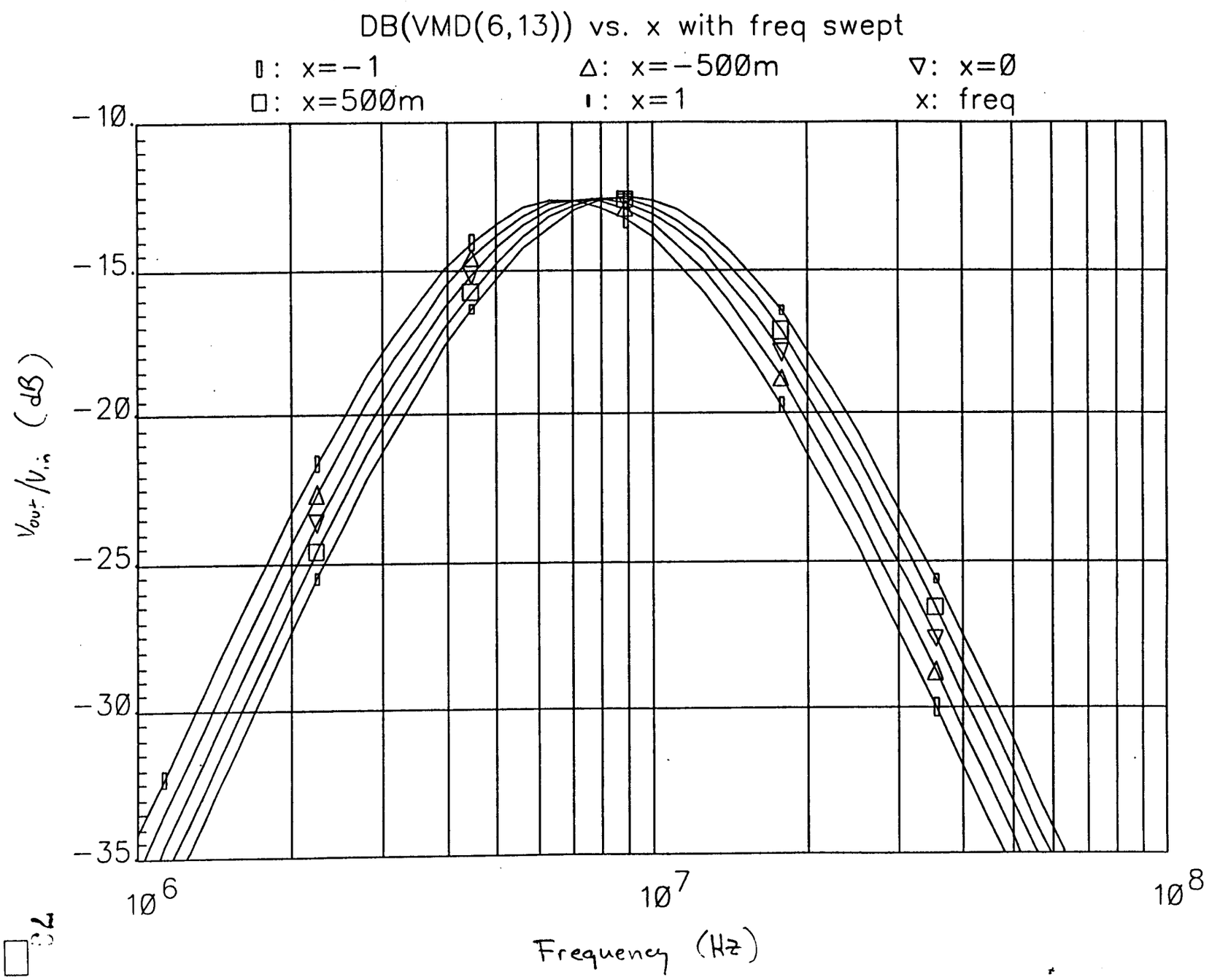


$$H(s) = \frac{Rf/Ri}{1+s\tau} \qquad \tau = R_f C$$

Time constant can be varied by changing only R_f, but then gain will vary. Can make R_{in} + R_f vary together to keep gain constant, at the expense of power + noise etc.

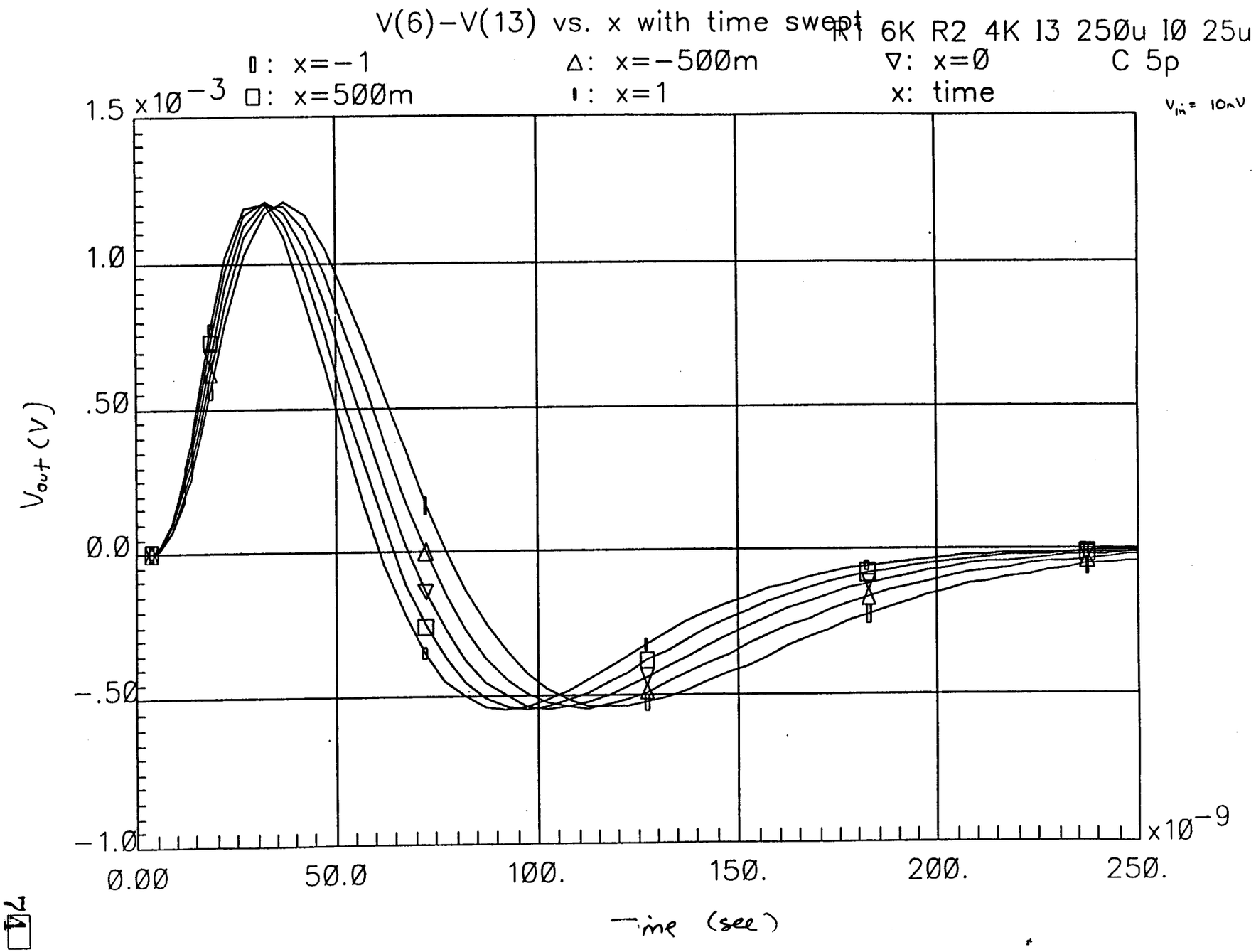
6/24/91

$(CR)^2-(RC)^2$ variable shaper

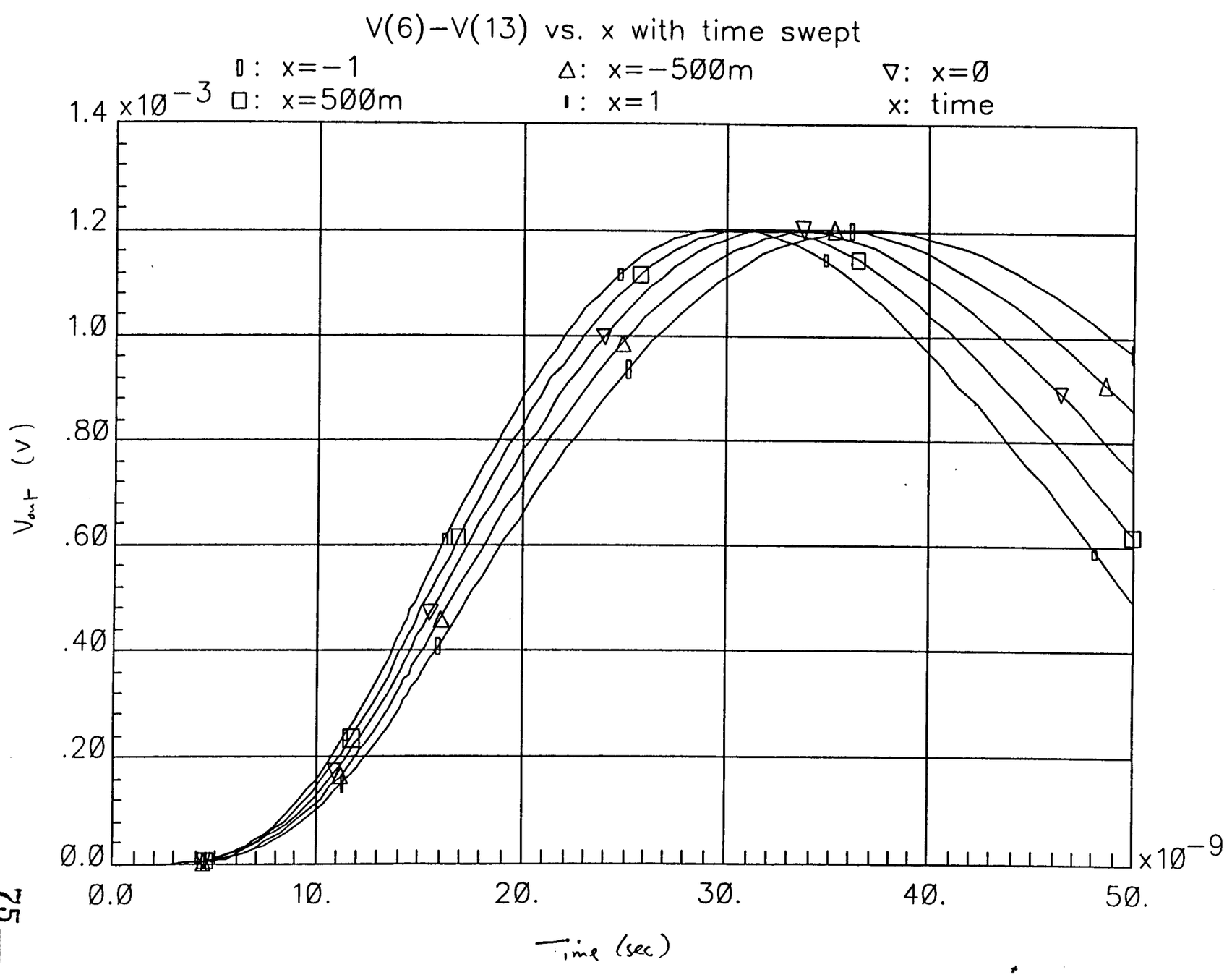


6/27/11

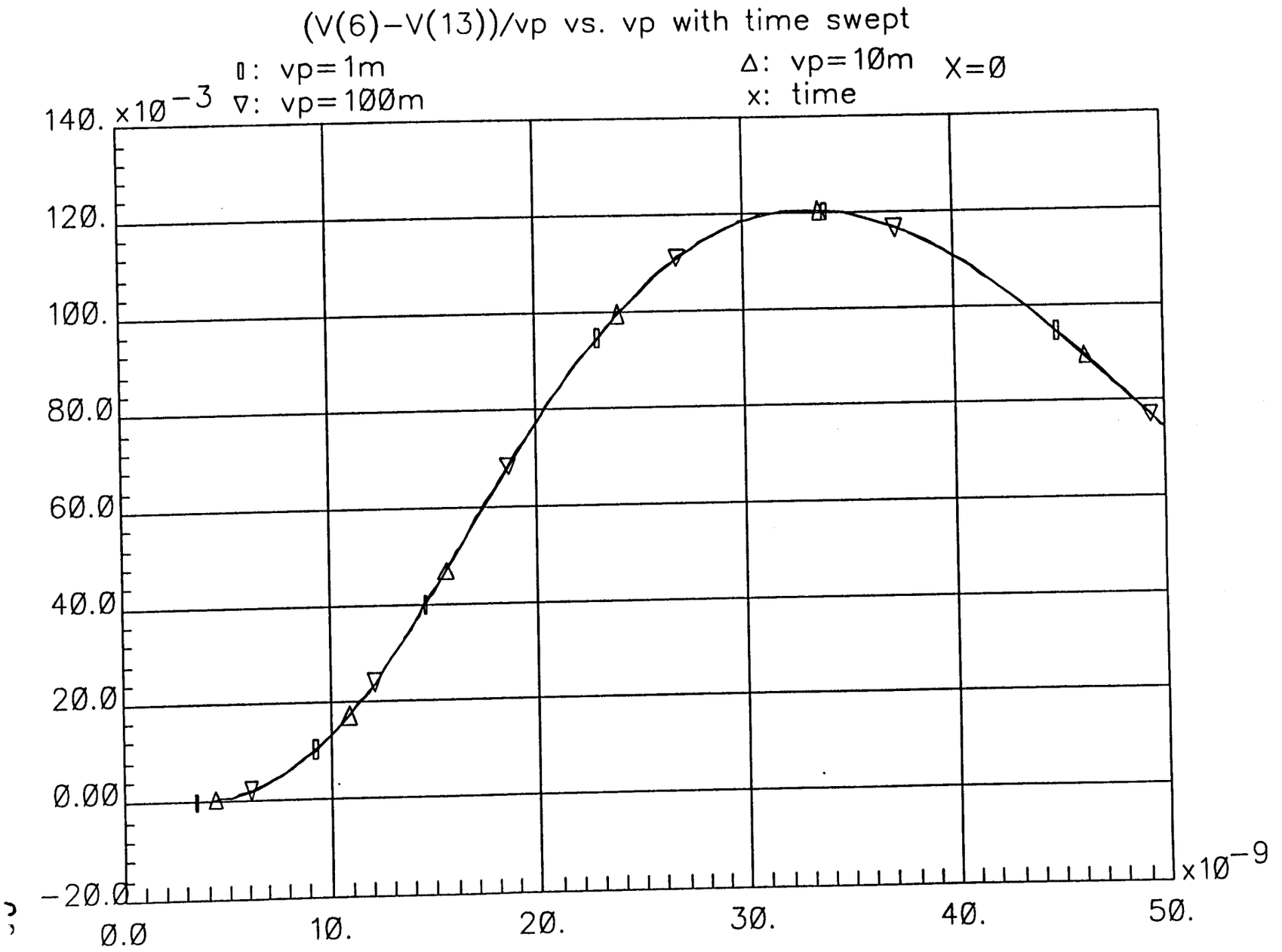
$(CR)^2-(RC)^2$ variable shaper

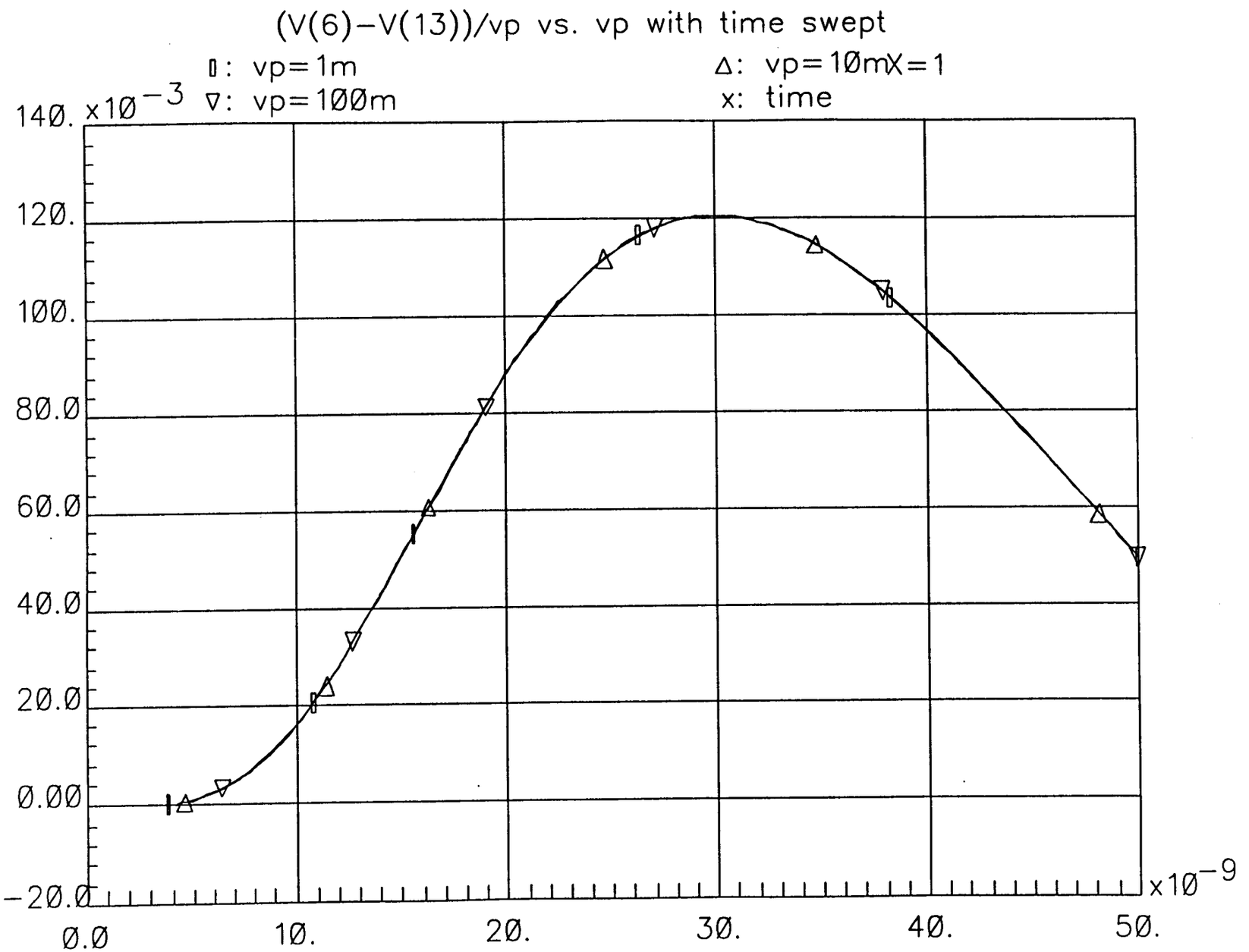


(CR-(RC)^2 variable shaper



(CR)² - (RC) variance shaper




(V(6)−V(13))/vp vs. vp with time swept
▯: vp=1m
▽: vp=100m
Δ: vp=10mX=1
x: time
140. x10^-3
120.
100.
80.0
60.0
40.0
20.0
0.00
-20.0
0.0
10.
20.
30.
40.
50.
x10^-9

Status of Noise Performance of GaAs Devices

P. O'Connor (BNL)

6/6/91
Front End Electr.
LBL mtg.

GaAs MESFETs as Front End Device for Low Noise Charge Sensitive Preamps

- MESFET Technology
- Noise measurements
- Preamp measurements
- Radiation effects.

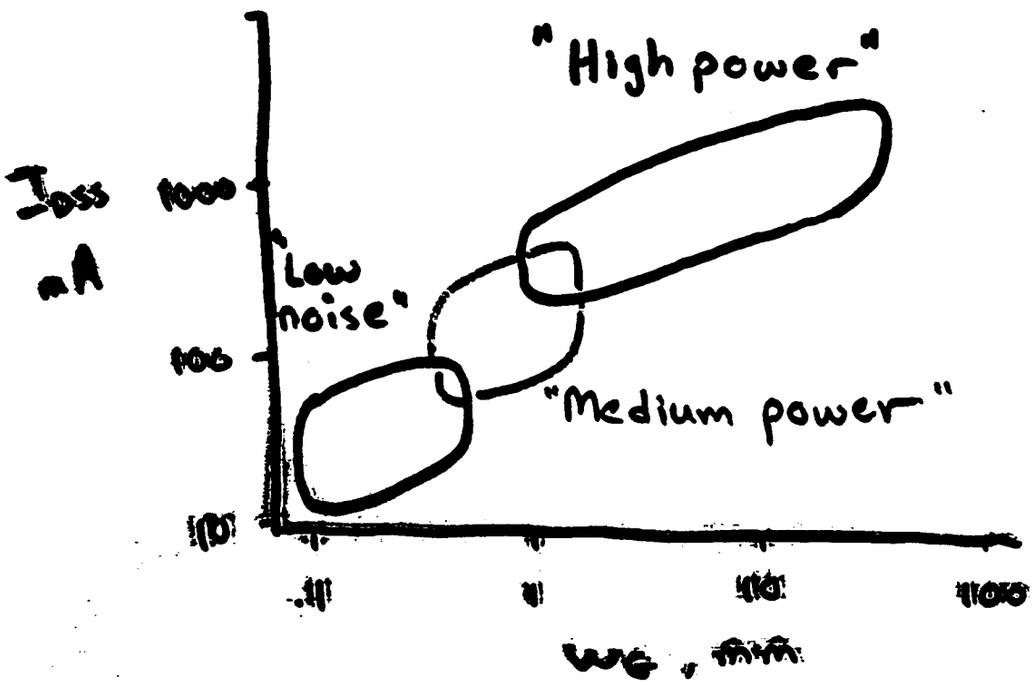
FET noise sources

		JFET	MOS	GaAs
Series thermal	$e_{ns}^2 = \frac{4kT\Gamma}{g_m}$ $\Gamma =$	0.7	≥ 1.0	1.0-1.5
1/f	$e_{nf}^2 = \frac{A_f}{f} = \frac{K_f}{C_{iss} f}$ $K_f =$	10^{-26}-10^{-27}	10^{-24}-10^{-25}	10^{-22}-10^{-2}
Parallel gate current	$e_{np}^2 = 2qI_G$ $I_G =$	10^{-10}-10^{-11}	10^{-14}	10^{-8}-10^{-10}

Technological and electrical characteristics

Gate length	L_g	(1.1) 0.8	-	0.5 (0.2)	μm
Chan. doping	N_D	5e16	-	5e17	cm^{-3}
Cutoff freq.	f_T	4	-	25	GHz
Breakdown	BV_{GD}	12	-	5	V
Transconductance	g_m	80	-	250	mS/mm
Capacitance	C_{GS}	1.5	-	0.3	pF/mm
Pinchoff	V_p	0.3	-	3	V
Sat. current	I_{DSS}	25	-	250	mA/mm

Availability



Preamp Noise

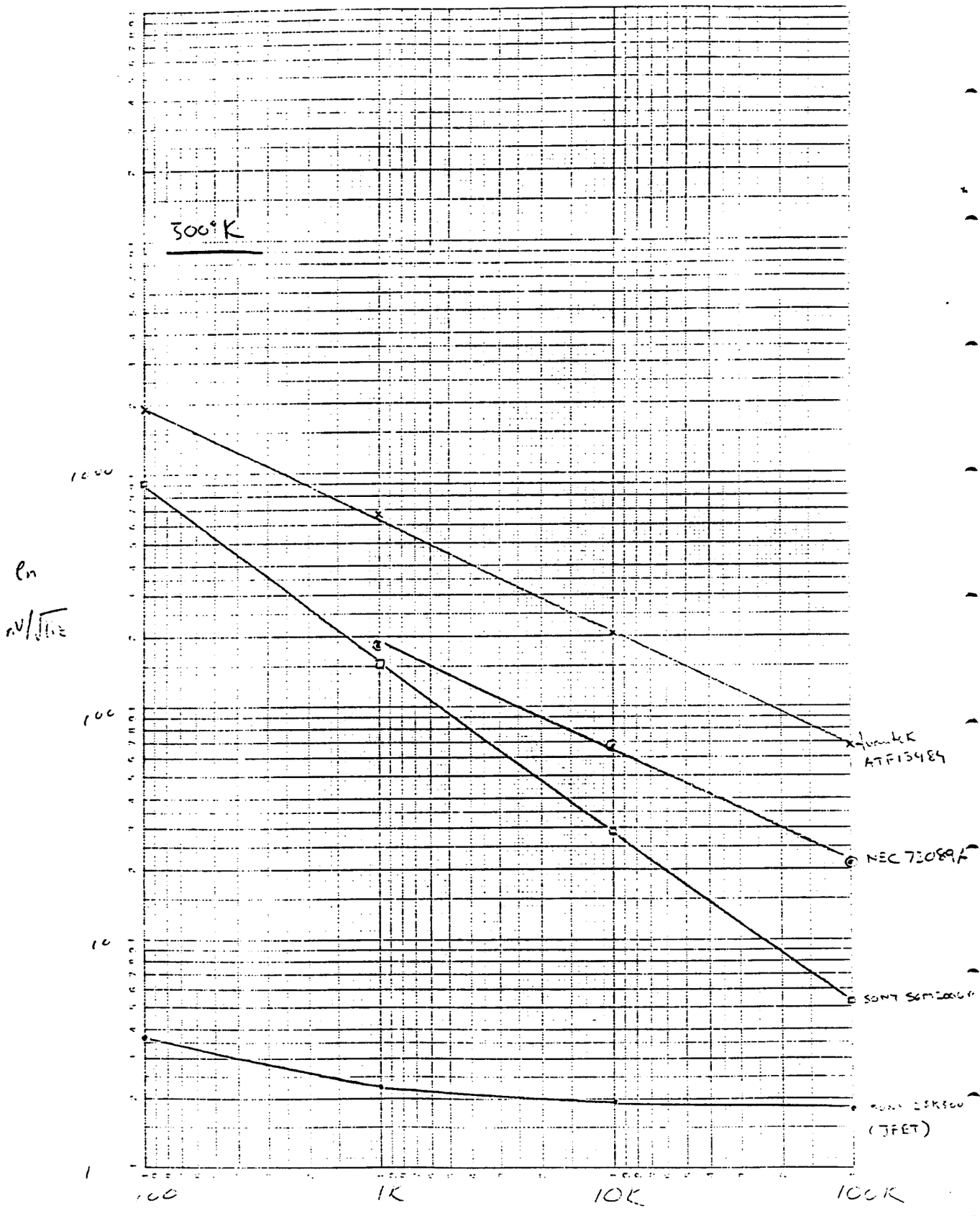
$$ENC^2 = \left(\frac{a_1 e_{ns}^2}{\tau_p} + a_2 f e_{nf}^2 \right) C_t^2 + a_3 e_{np}^2 \tau_p$$

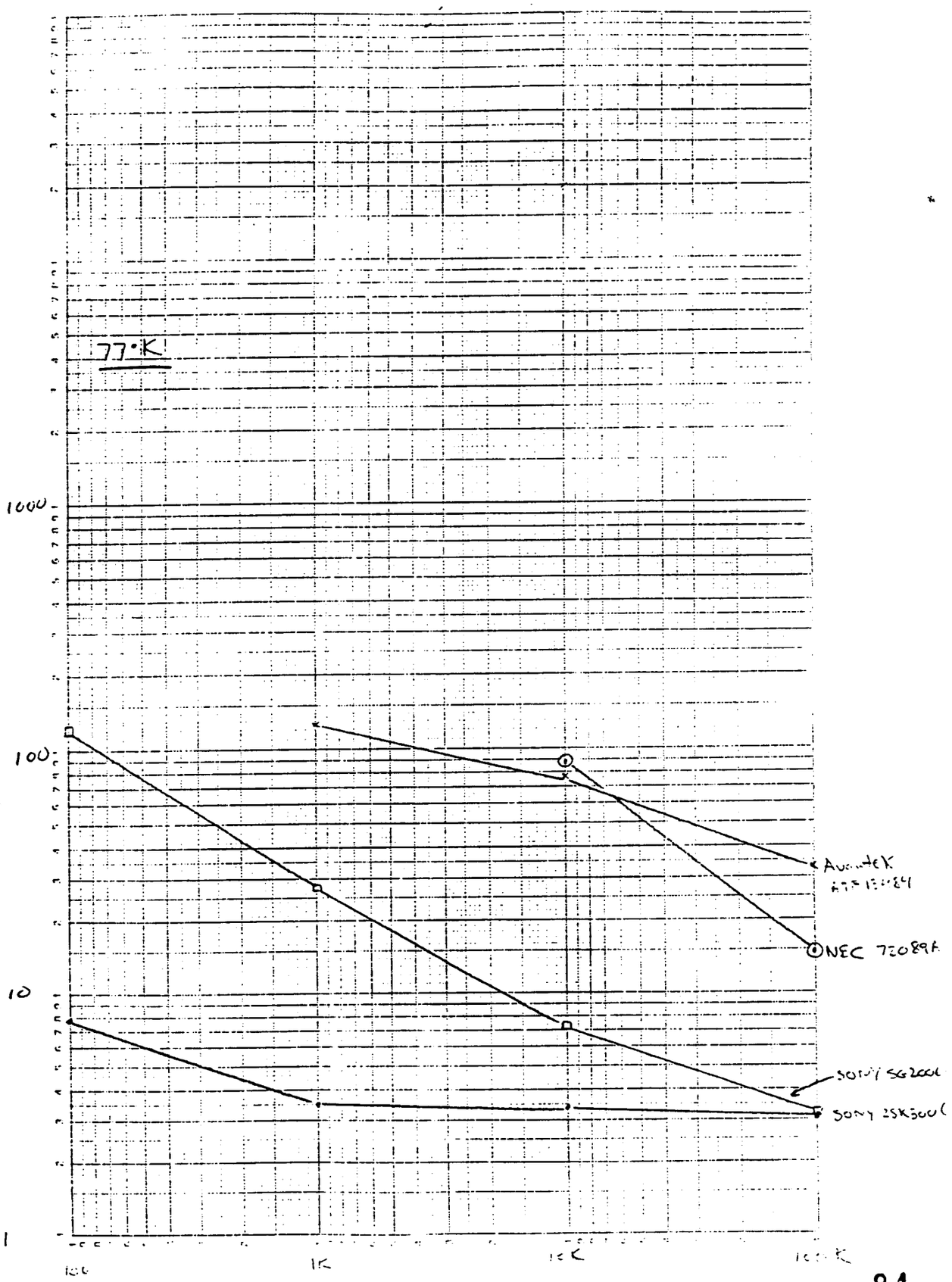
equal when $\tau_p \sim \frac{4KT}{K_f \omega_T}$

5 nsec fn JFET
70 nsec GaAs 300 K
170 " " 77 K

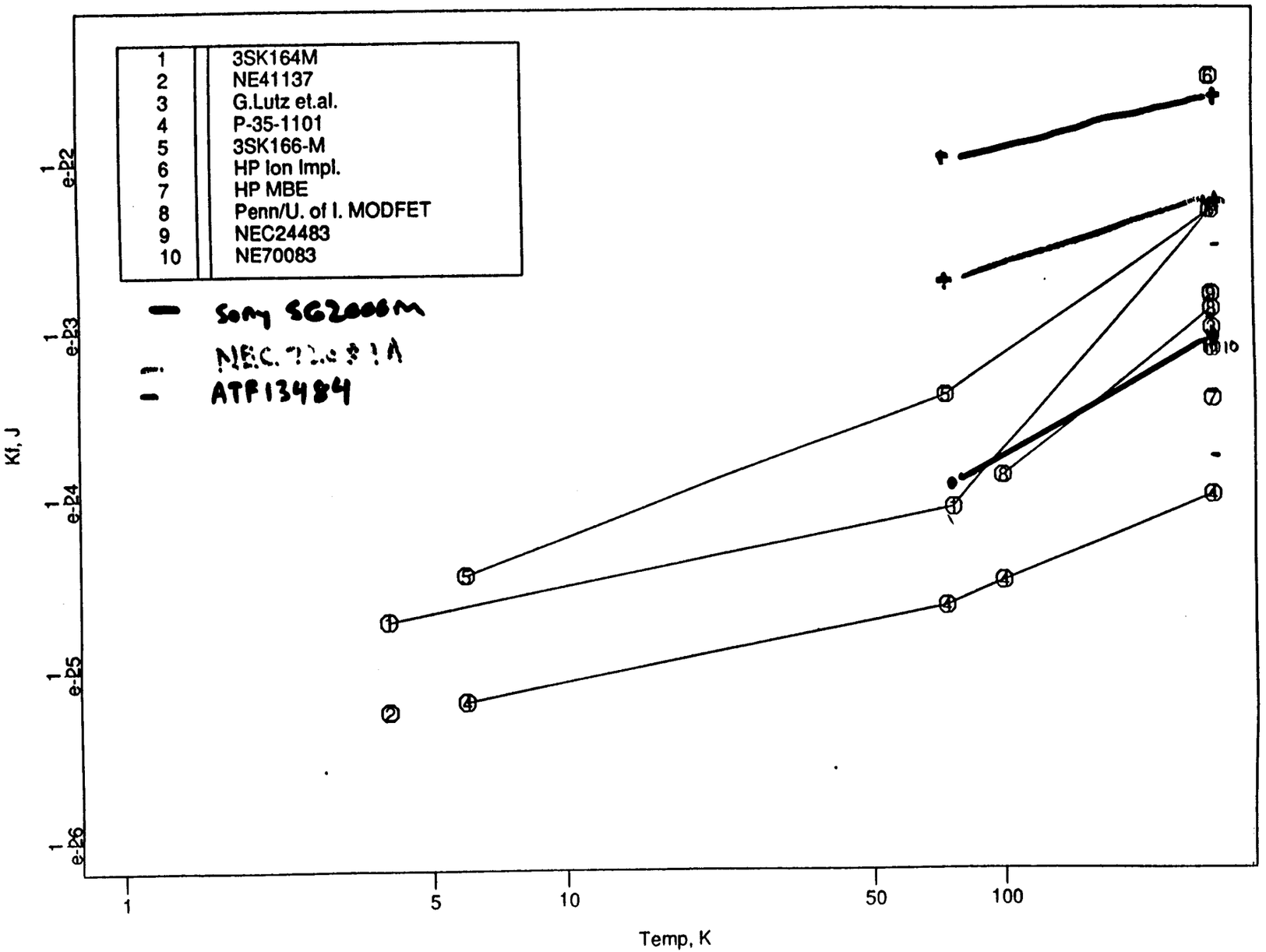
for $C_D = C_{iss}$

$$ENC^2 \propto \frac{a_1 4KT\Gamma}{\tau_p \omega_T} + a_2 K_f$$


300°K
1000
100
10
1
100
1K
10K
100K
en
nV/√Hz
NEC 72089A
SONY SCM2000
(JFET)


77°K
1000
100
10
1
NEC 72089A
SONY 2SK300(

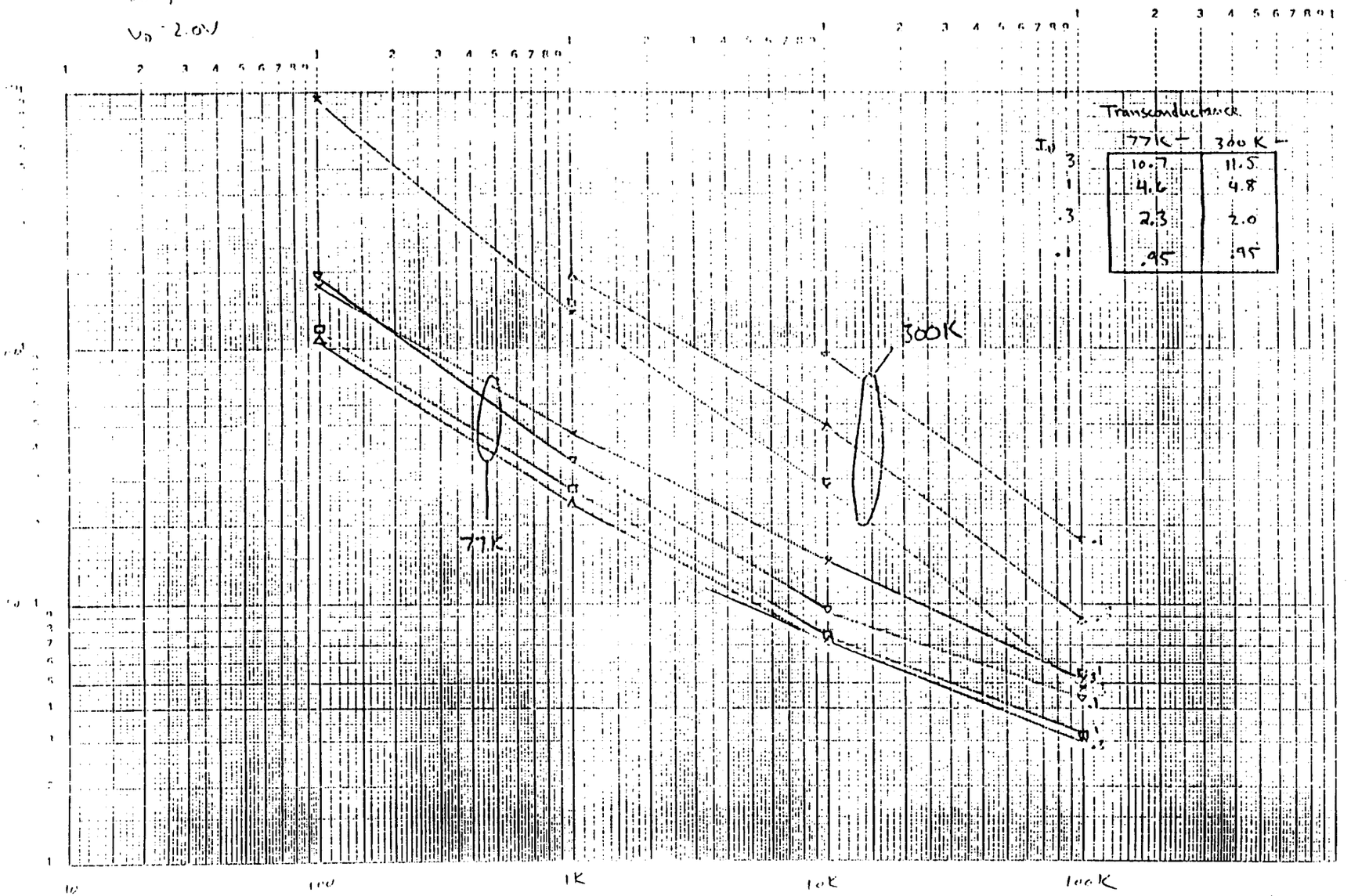
GaAs MESFET 1/f Noise vs. Temperature

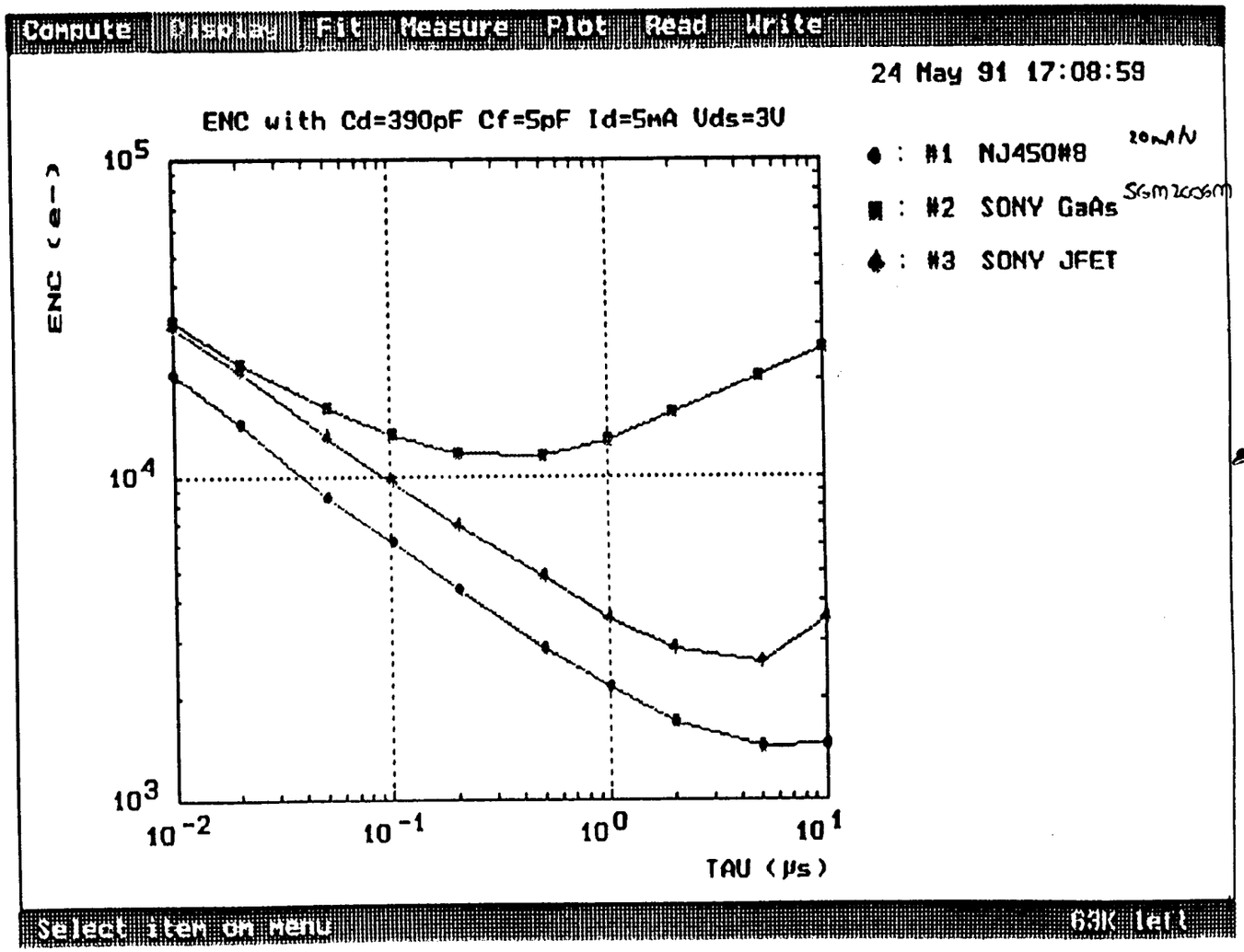


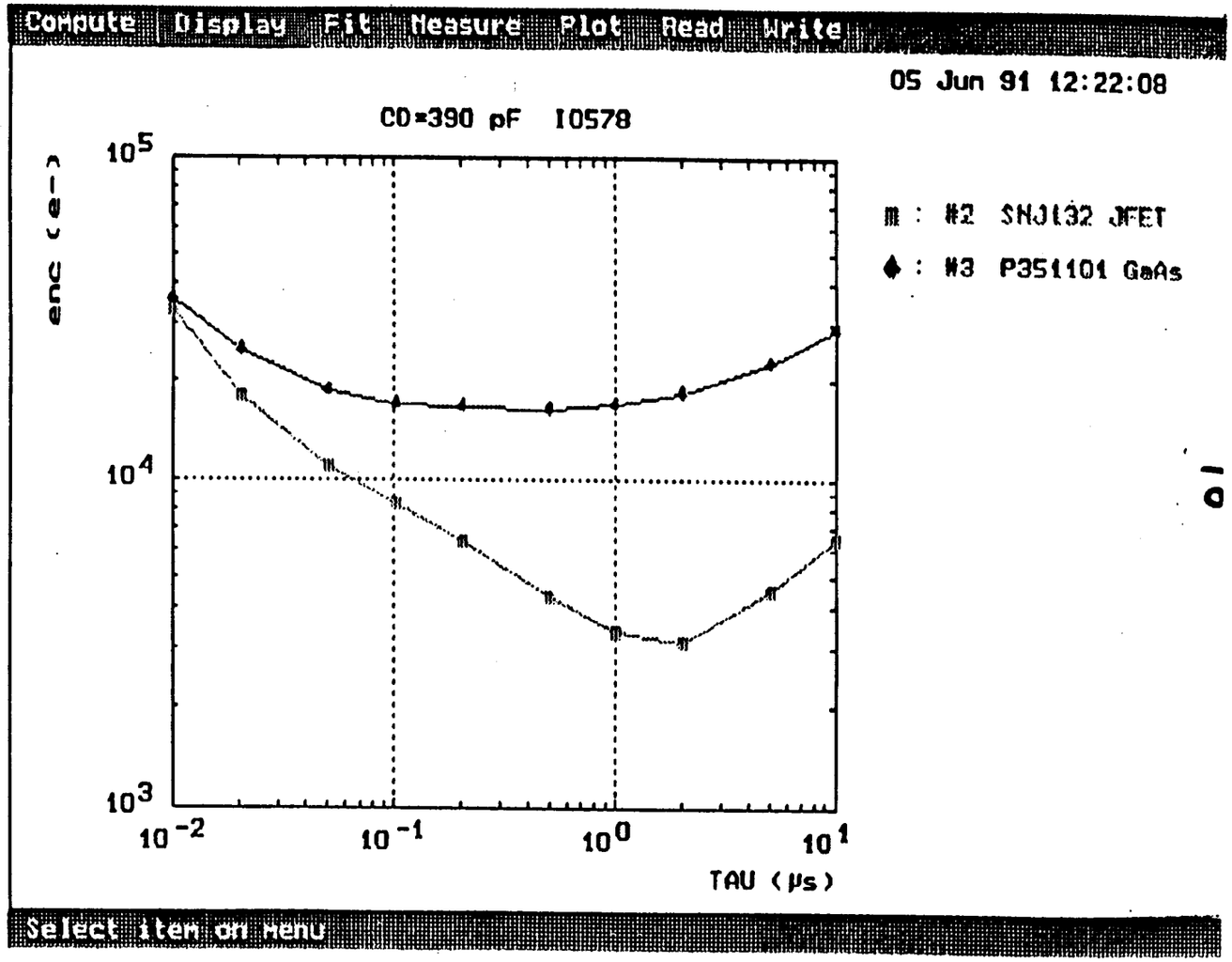
K+E LOGARITHMIC 3 x 5 CYCLES
KEUFFEL & ESSER CO. MADE IN U.S.A.
46 7520

Sony SGM 2006m (#2)

V_D = 2.0V




Compute Display Fit Measure Plot Read Write
24 May 91 17:08:59
ENC with Cd=390pF Cf=5pF Id=5mA Vds=3V
ENC (e-)
10^5
10^4
10^3
10^{-2}
10^{-1}
10^0
10^1
TAU (μs)
● : #1 NJ450#8
■ : #2 SONY GaAs
◆ : #3 SONY JFET
Select item on menu
63K left


Compute Display Fit Measure Plot Read Write
05 Jun 91 12:22:08
CO=390 pF I0578
enc (e-)
10^5
10^4
10^3
10^{-2}
10^{-1}
10^0
10^1
TAU (µs)
■ : #2 SNJ132 JFET
♦ : #3 P351101 GaAs
Select item on menu

Radiation tolerance

GaAs

77°K measurements (Camin, et. al.)

10 Mrad gamma

g_m 7% decrease

I_{dss} 10% decrease

K_f 380% increase

Neutron

	10^{13}/cm²	10^{14}/cm²
	-5%	-19%
g_m		
I_{dss}	-5%	-16%
e_n @ 100 KHz	0	0
e_n @ 100 Hz	10%	50%

AlGaAs HEMT (Krantz et. al.)

Room temp. meas. after neutrons

	10^{14}/cm²	10^{15}/cm²
	-6%	-30%
g_m		

UTMC cmos

< 15% increase in 1/f noise after 10 Mrad and 2×10^{14}/cm² ne-

Fast Summing and Shaping Amplifiers

S. Rescia (BNL)

New Understanding of Long Transmission Lines Between Electrodes and Preamplifiers in Ionization Calorimeters

C. de la Taille (Orsay)

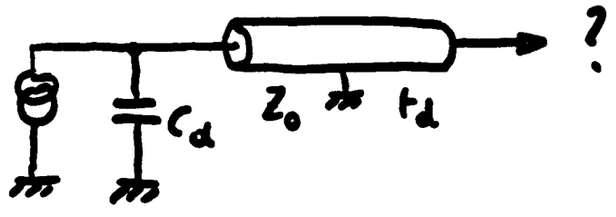
TRANSMISSION LINES

BETWEEN ELECTRODES AND FRONT END ELECTRONICS FOR LAr CALORIMETRY

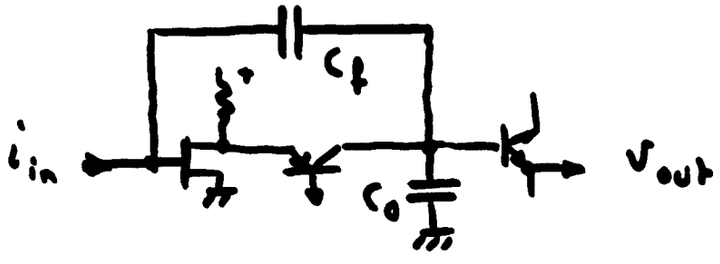
C. de LATAILLE

Advantages :
- No power limitation
- No dissipation in LAr
- No radiation damage
- No technology limitation
- Maintenance

Drawbacks : Noise increase ?



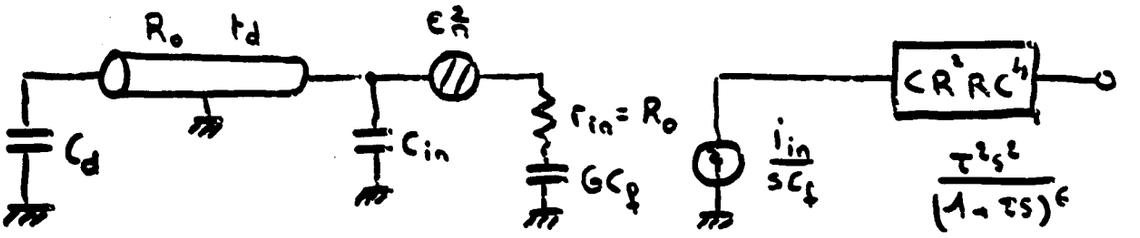
Low noise ⇒ line termination on an active resistor
→ charge preamp.



$$Z_{in} = \frac{1}{g_m}\frac{C_0}{C_f} \quad \in \mathbb{R}$$

→ adjust C_0 to match line impedance

NOISE DUE TO THE LINE



we transform e_n in a current generator i_n :

$$i_n^2 = \frac{e_n^2}{|r_{in} + Z|^2}$$ Z : impedance seen in the l

$$Z = j R_0 \frac{\omega R_0 C_0 \tan \omega t_d - 1}{\omega R_0 C_0 + \tan \omega t_d}$$

rms noise at the output :

$$V_n^2 = \int_0^\infty \frac{e_n^2}{|R_0 + Z|^2} \frac{1}{\omega^2 C_f^2} |H(j\omega)|^2 \frac{d\omega}{2\pi}$$

$$= \frac{e_n^2 \tau}{2\pi R_0^2 C_f^2} \int_0^\infty \frac{x^2}{(1+x^2)^6} \frac{dx}{1 + \left(\frac{\frac{x R_0 C_d}{\tau} \tan \frac{x t_d}{\tau} - 1}{\frac{x R_0 C_d}{\tau} + \tan \frac{x t_d}{\tau}} \right)^2}$$ (x =

ENC at the input ?

$Q_0 \delta(t)$ on input gives $V(s) = \frac{Q_0}{sC_f(1+sR_0C_d)} \frac{\tau^2 s^2}{(1+\tau s)}$

Inverse Laplace Transf → v(t)

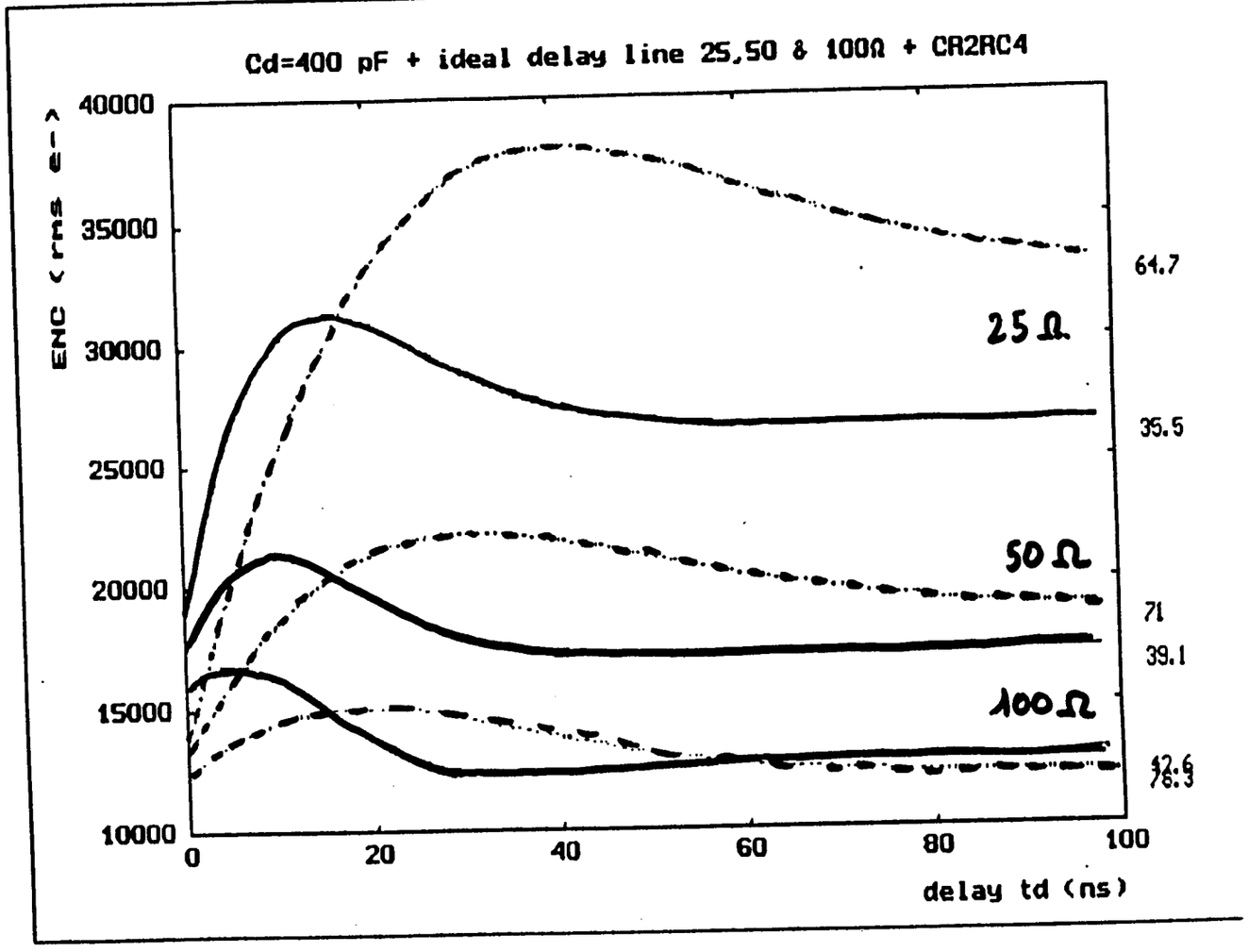
$$ENC^2 = \frac{Q_0^2 V_n^2}{\ldots}$$

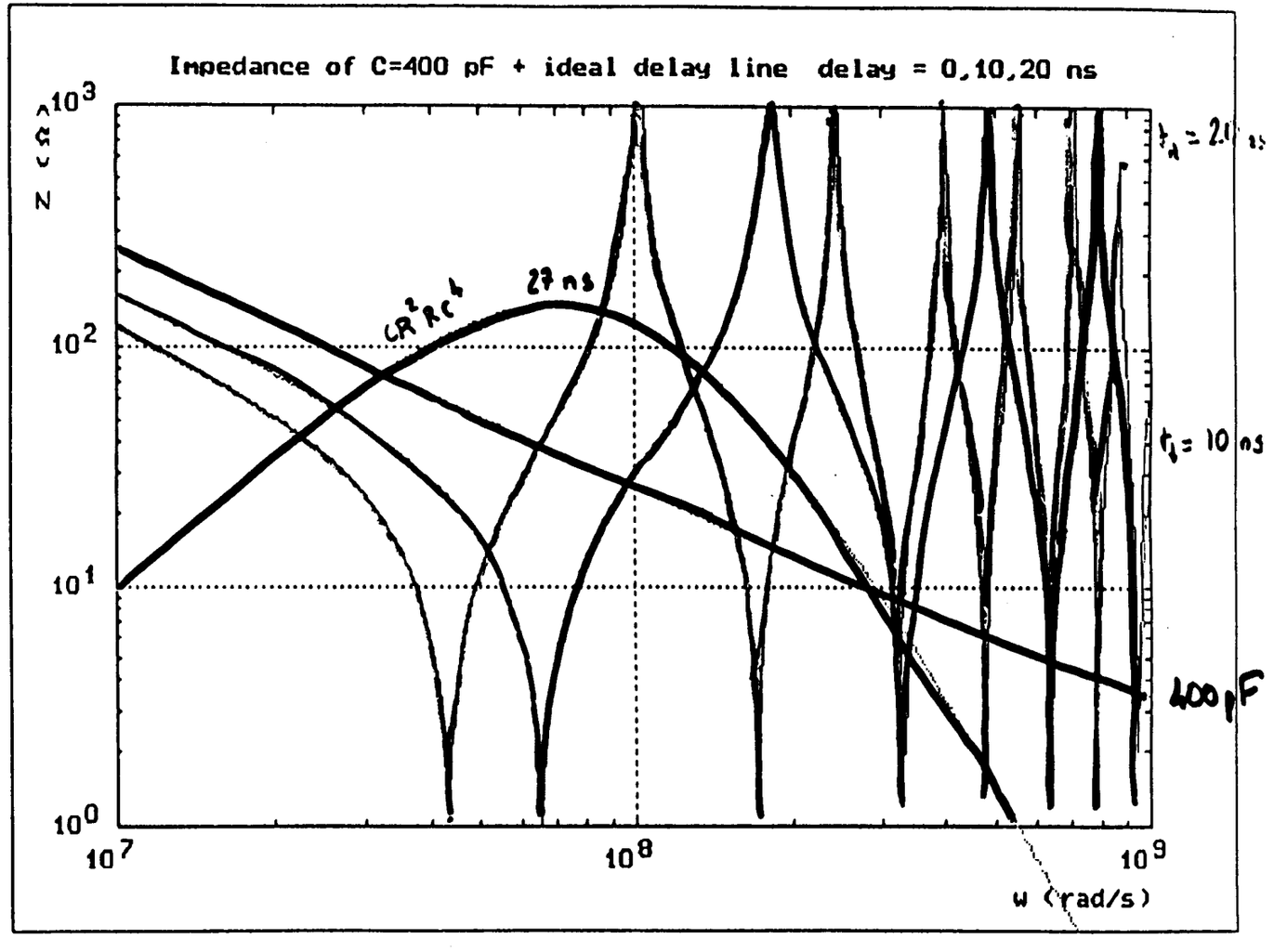
filter CR^2RC^4

— pkg time : 27 ns

-- pkg time : 54 ns

$e_n = 1nV/\sqrt{Hz}$

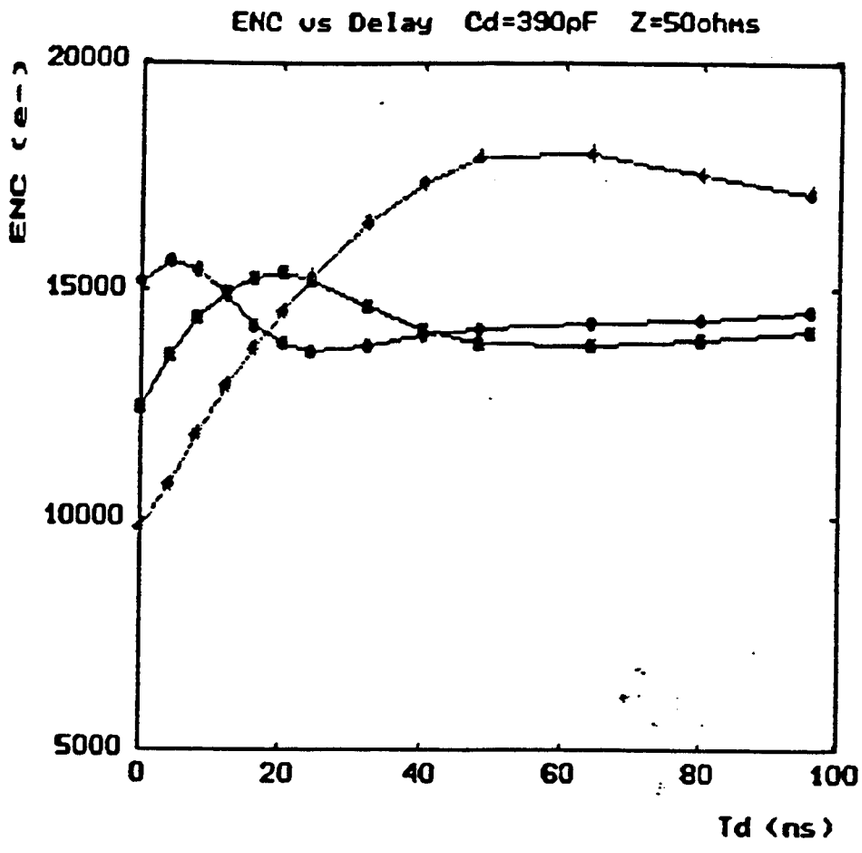



Impedance of C=400 pF + ideal delay line delay = 0,10,20 ns
Z (Ω)
10^3
10^2
10^1
10^0
10^7
10^8
10^9
w (rad/s)
CR^2RC^4
27 ns
t_d = 20 ns
t_d = 10 ns
400 pF

Z

Cd=100 pF + ideal delay line 50 & 100Ω + CR2RC4
ENC (rms e-)
delay td (ns)
50 Ω
100 Ω
59.3
32.3
64.7
35.5
20000
15000
10000
5000
0
0
20
40
60
80
100

Cd=1 nF + ideal delay line 25 & 50Ω + CR2RC4
25Ω
50Ω
72.9
40.3
43.6
80.6
ENC (rms e-)
delay td (ns)
50000
45000
40000
35000
30000
25000
20000
0
20
40
60
80
100



♦ : curve 1 25 n
■ : curve 2 50 n
▲ : curve 3 100 n

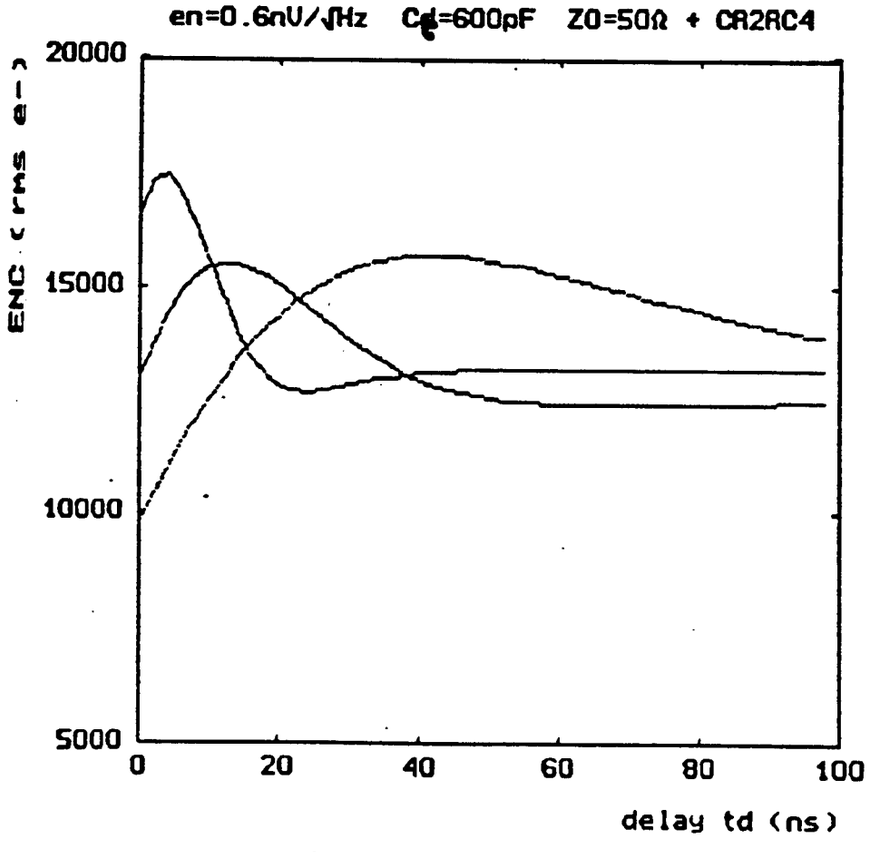
Experimental measurements

FET : NJ 450

$e_n \simeq 0{,}6$ nV/$\sqrt{Hz}$

C_d = 400 pF

RG58 cable

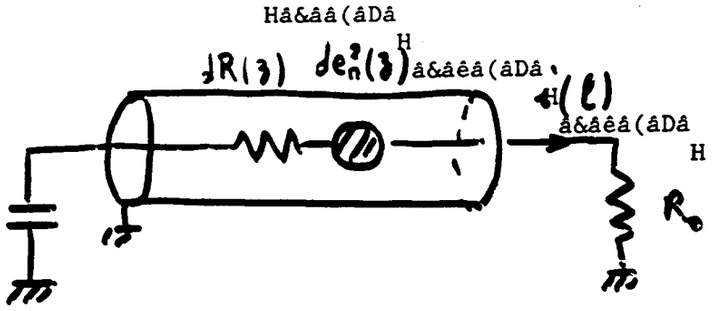


Theoretical Curves

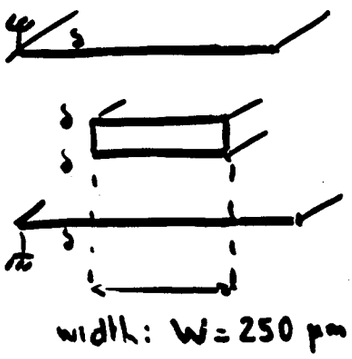
(for some peaking time)

99.4
30
55.2

SKIN EFFECT (S. Rescia)



Computation done for a strip line



skin depth: $\delta = \frac{1}{\sqrt{\pi f \sigma \mu_0}}$

$R_{sq} = \frac{1}{\sigma \delta} = \sqrt{\pi f \rho \mu_0} \simeq 2.6 \cdot 10^{-9} \sqrt{f}$ for copper

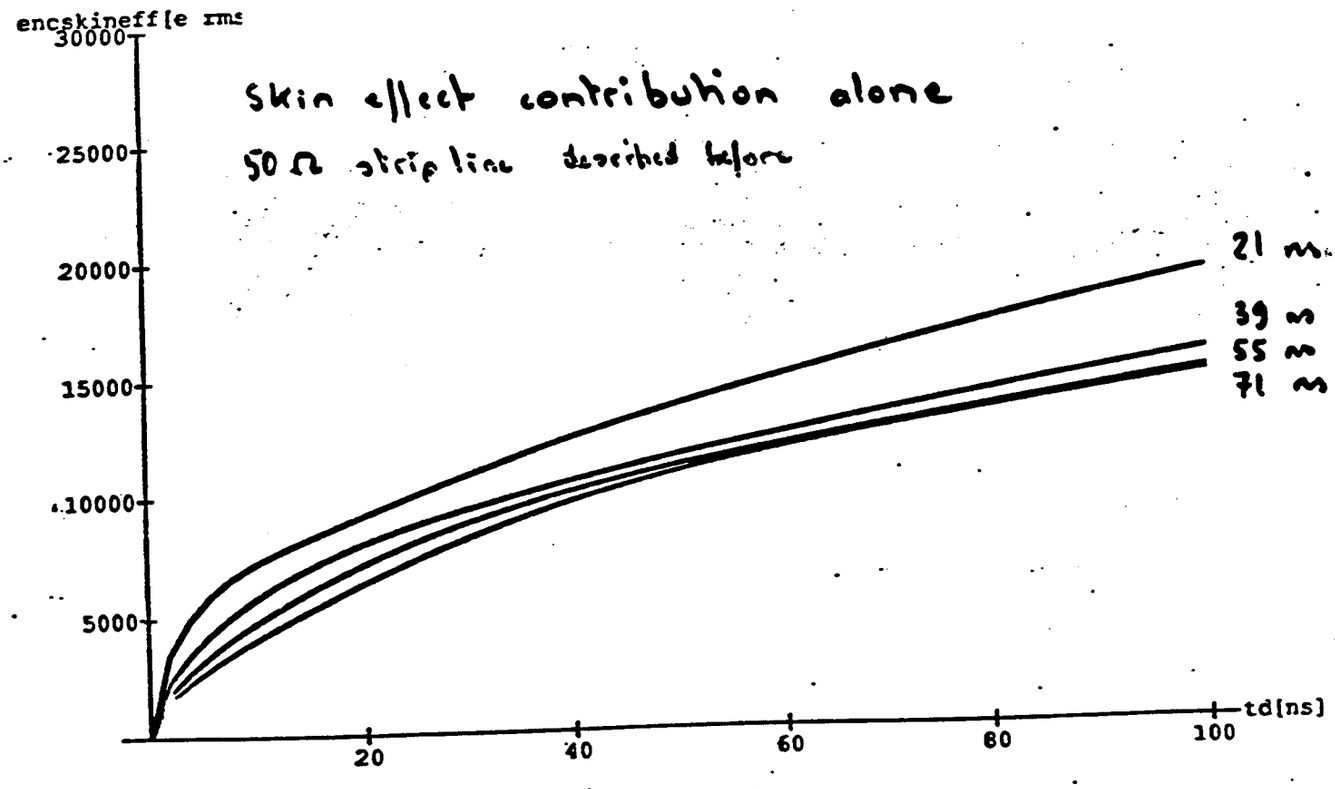
$de_n^2 = \frac{4kT}{W} \sqrt{\pi f \rho \mu_0}\, dz \sim \sqrt{f}$

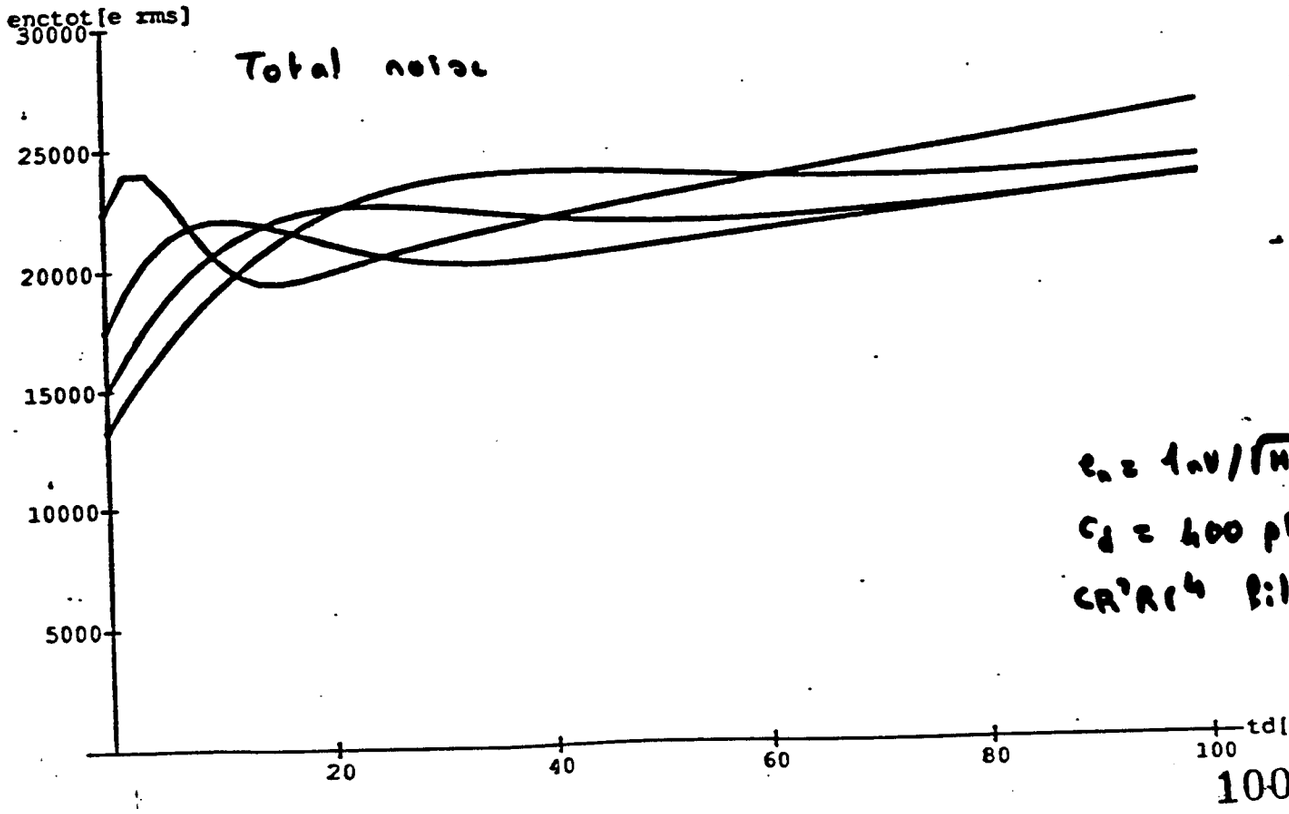
rms noise due to skin effect:

$$V_n^2 = \int_0^\infty I(e_n, t_s, \omega) \frac{1}{\omega^2 C_j^2} \frac{\omega^4 \tau^4}{(1+\omega^2\tau^2)^6} \frac{d\omega}{2\pi}$$

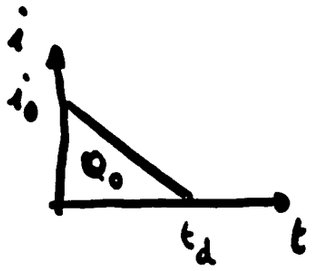
we calculate ENC as before

SKIN EFFECT (ctd)





LINEARITY



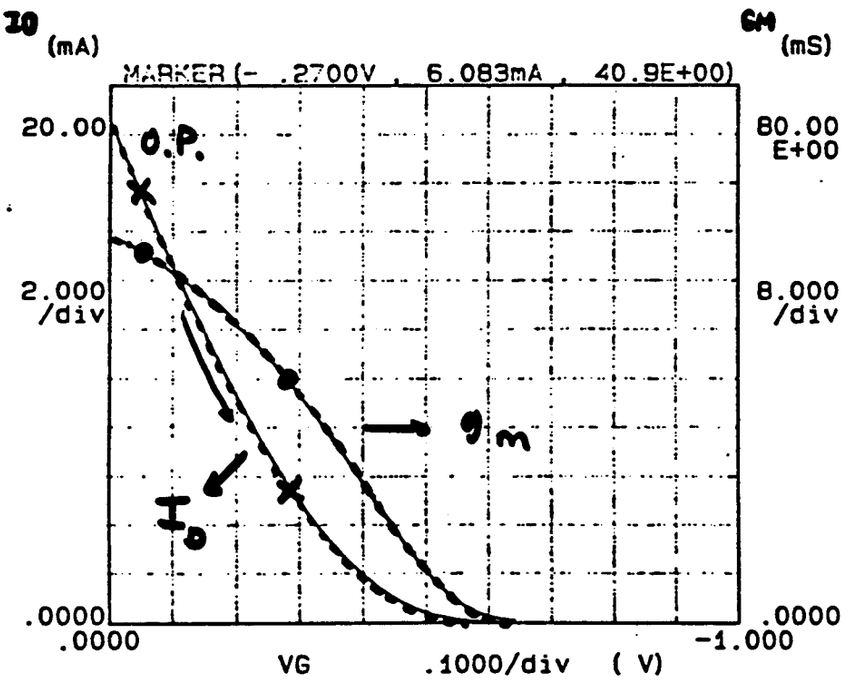
in LA. 1,5 T.V → 850 pC → 4,5 mA in 40C

voltage on the input $\Delta V = R_0 i_0$

↳ 225 mV

This ΔV_{GS} changes g_m and therefore R_{in}

→ limits Z_0



Variable1:
VG -Ch2
Linear sweep
Start .0000V
Stop -1.0000V
Step - .0100V

Constants:
VS -Ch1 .0000V
VD -Ch3 5.0000V

GM (mS) = (ID/ VG) *1000

Interfet L50

$\frac{\Delta g_m}{g_m} \leq 30\%$

Use of a second feedback to stabilize g_m ?

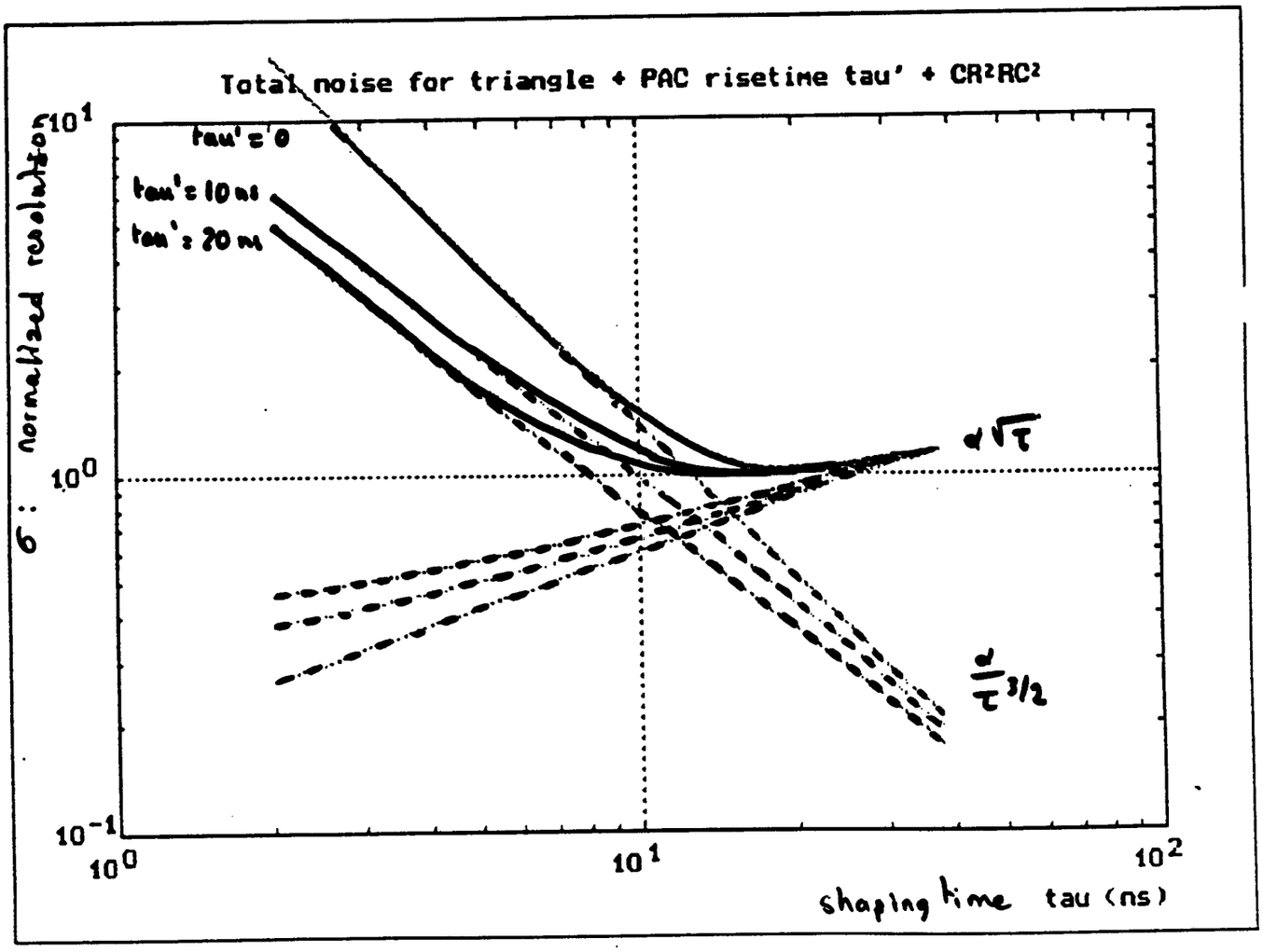
(F. Manfredi

MATCHING PENALTY

matching the line increases R_{in} of preamp

→ slows the preamp with a pole $R_{in} C_D$

what happens to ballistic deficit ?



Preamp/Shaper Circuits

I. Kipnis (LBL)

CMOS Preamplifier / Shaper

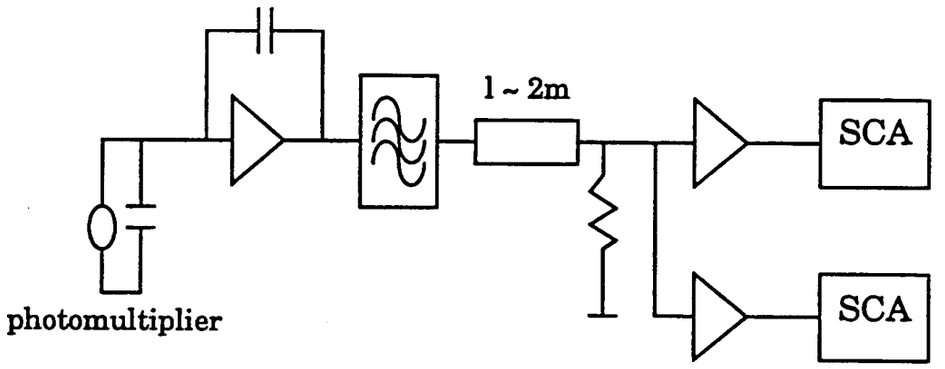
Calorimeter Front-End Electronics for the SSC

Issy Kipnis

Lawrence Berkeley Laboratory

June 1991

Preamplifier / Shaper



Major Objectives

- High Dynamic Range: 1×10^5 (100dB)
- Settling to within 1% in < 16 nsec

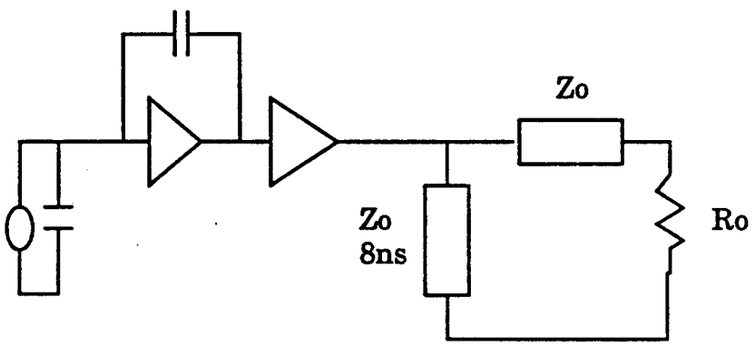
Minor Goals

- Low Noise
- "Low" Power Dissipation

Shaper

- Flat top
- Fast return to baseline

One solution: delay-line filter



Photomultiplier Characteristics
(Hamamatsu R580-15)

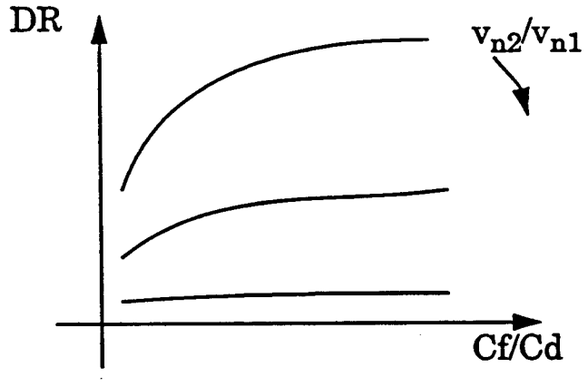
- Anode capacitance: 3 pF
- Rise time: 2.7 ns
- Transit time spread: 2ns

Dynamic Range

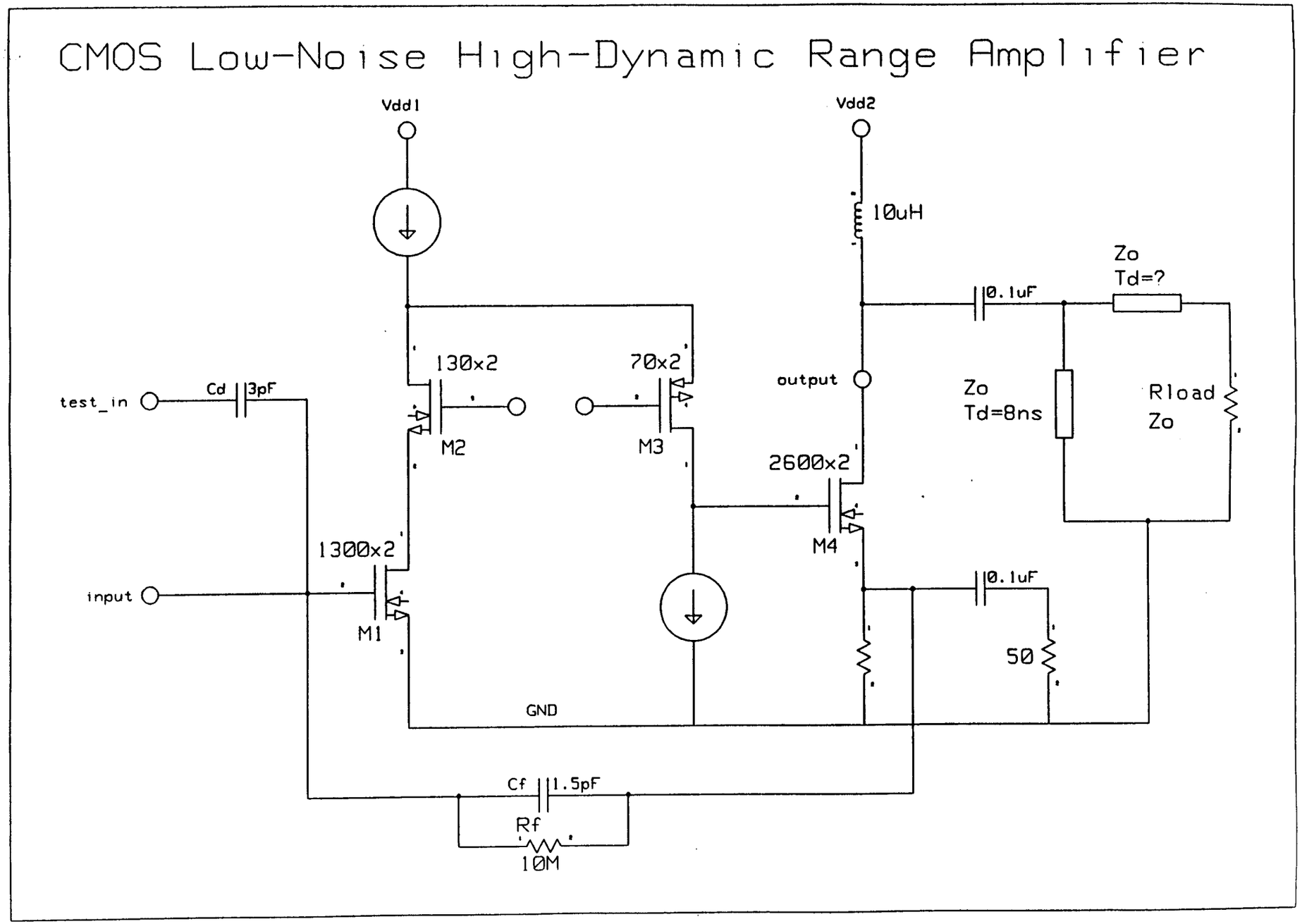
High dynamic range ⟶ large Cf

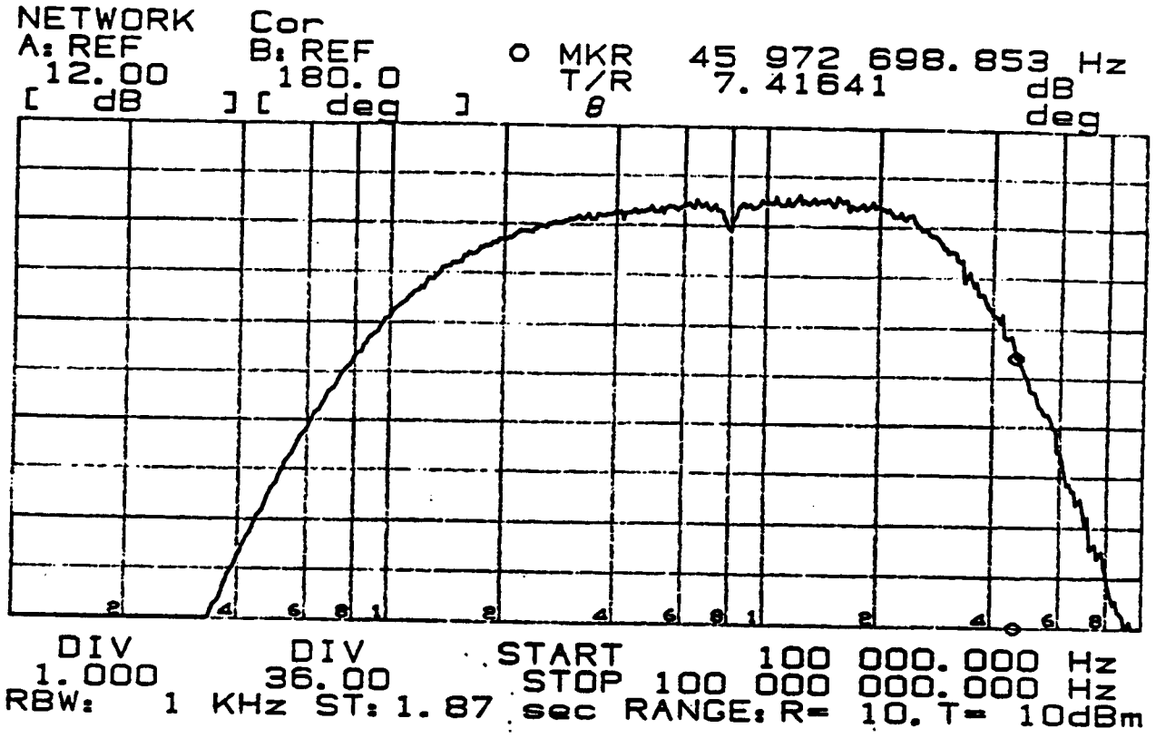
Disadvantages of large Cf

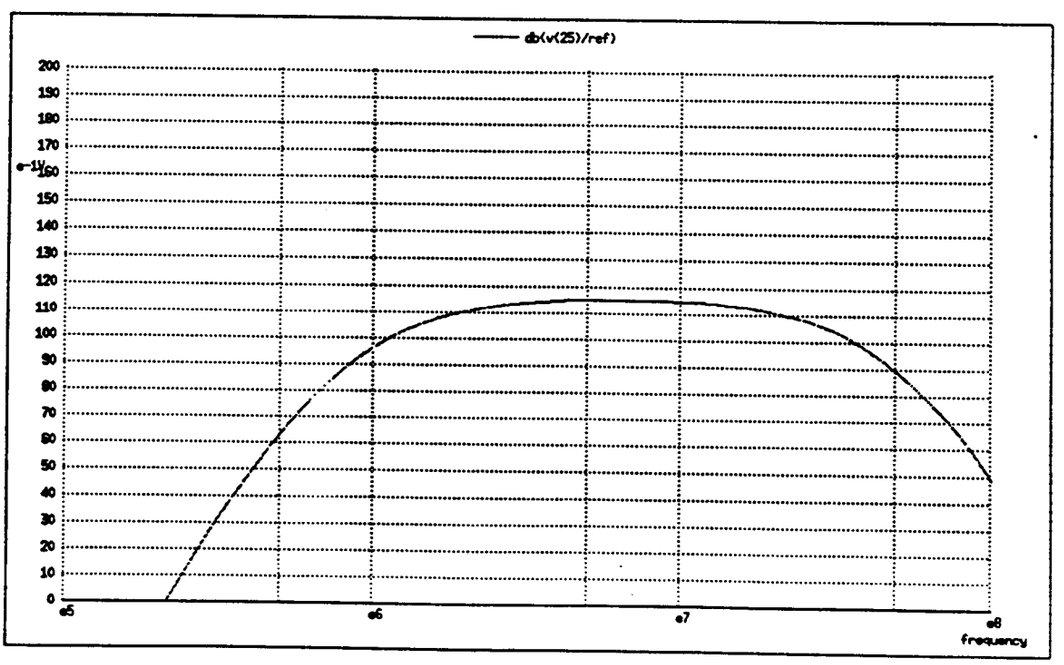
- higher noise
- second stage noise contribution
- higher power dissipation

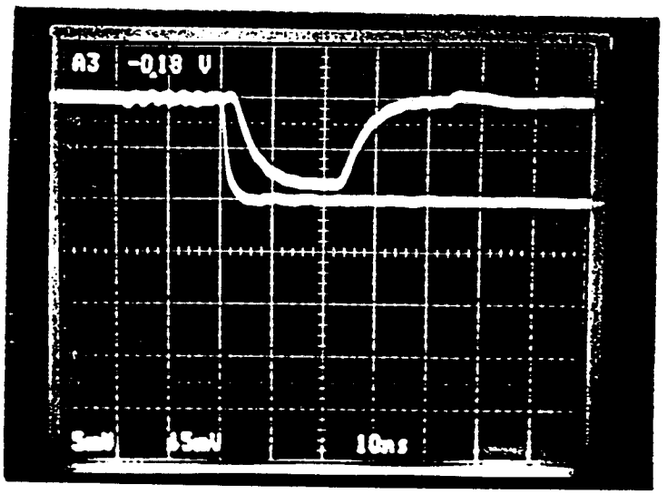


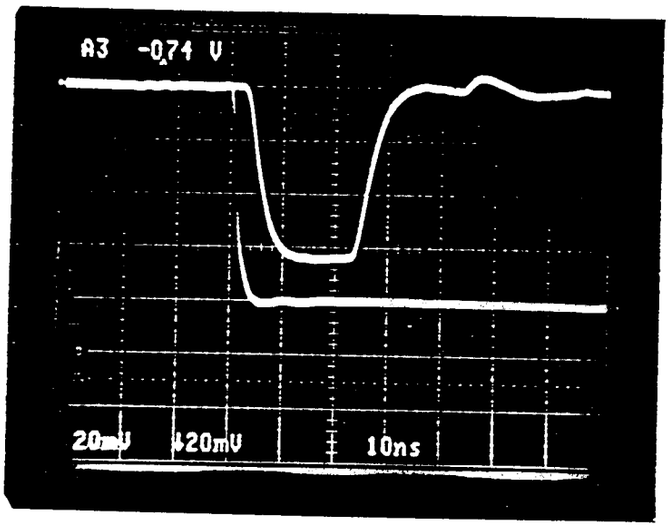
use smallest Cf that satisfies the dynamic range requirements

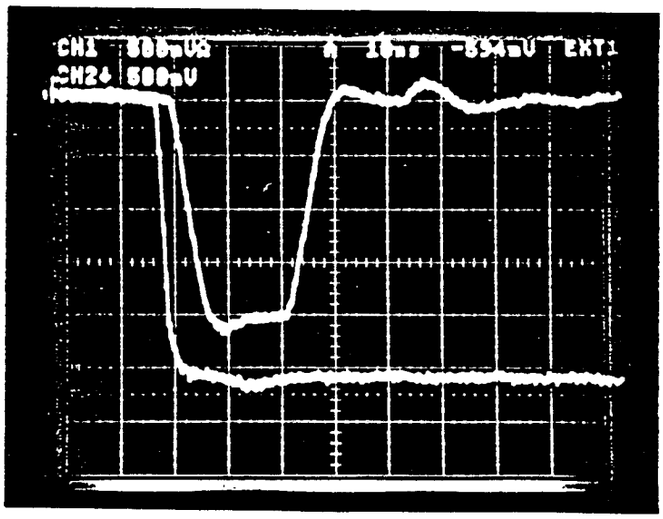

CMOS Low-Noise High-Dynamic Range Amplifier
Vdd1
Vdd2
10uH
Zo
Td=?
0.1uF
130x2
70x2
output
Zo
Td=8ns
Rload
Zo
test_in
Cd
3pF
M2
M3
2600x2
M4
1300x2
input
M1
0.1uF
50
GND
Cf
1.5pF
Rf
10M

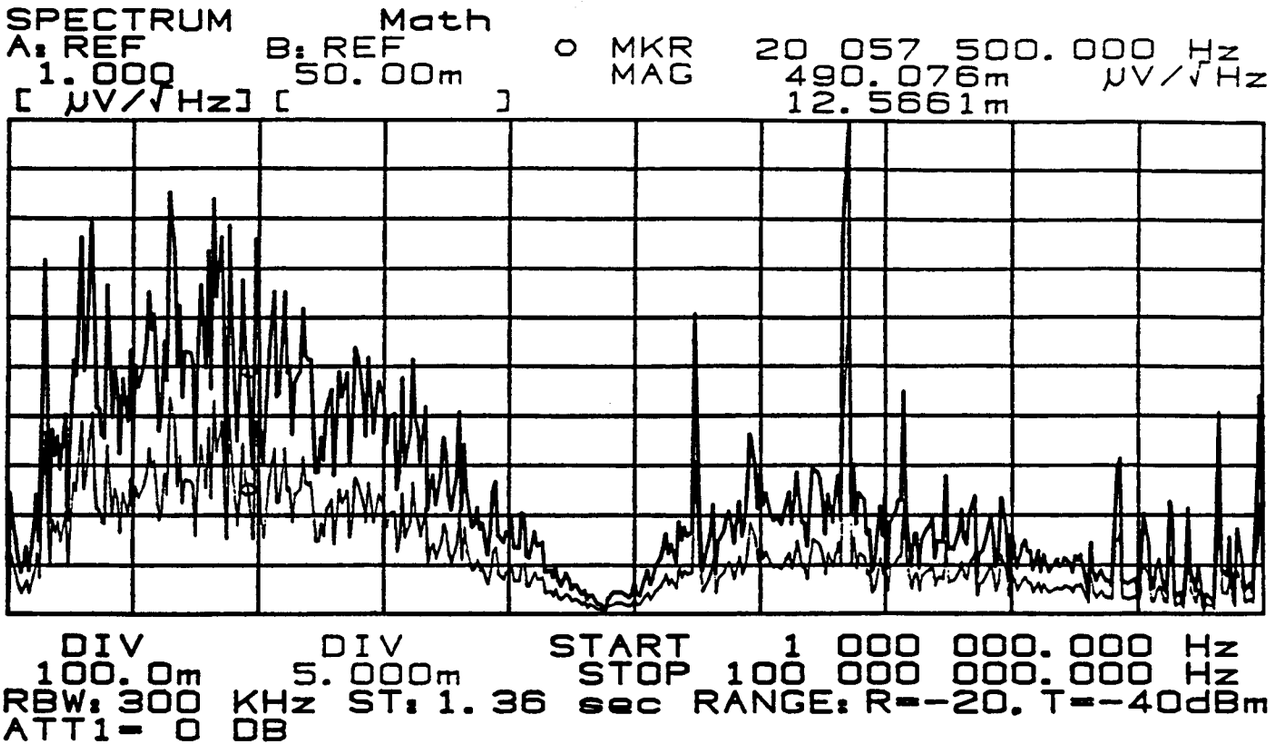

NETWORK Cor
A: REF B: REF
12.00 180.0
[dB] [deg]
MKR 45 972 698.853 Hz
T/R 7.41641 dB
θ deg
DIV DIV START 100 000.000 Hz
1.000 36.00 STOP 100 000 000.000 Hz
RBW: 1 KHz ST: 1.87 sec RANGE: R= 10. T= 10dBm

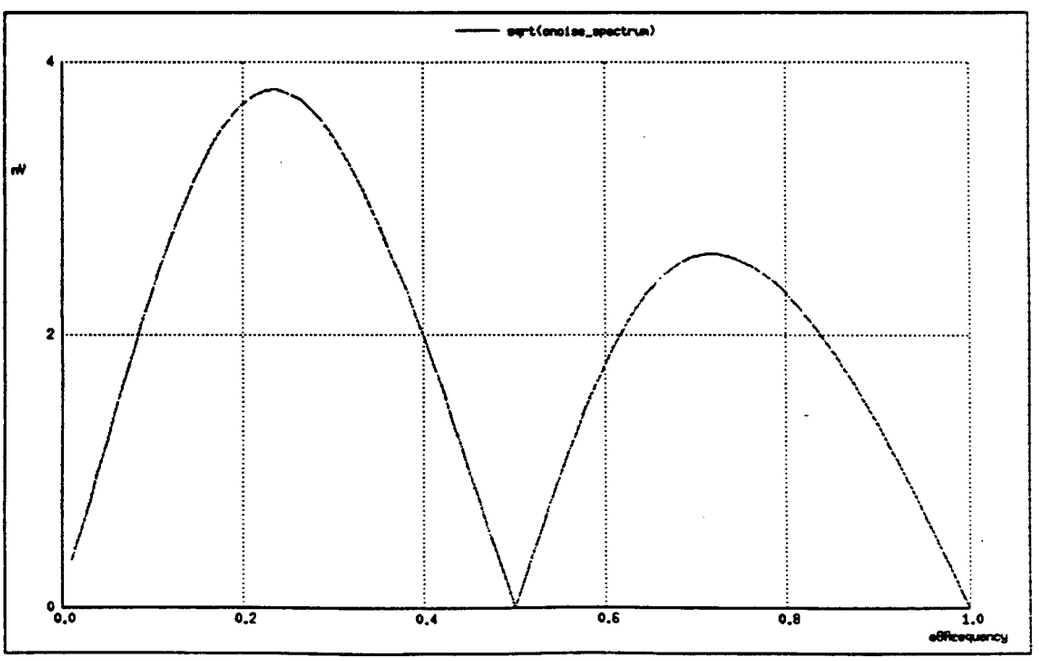

db(v(25)/ref)
frequency


A3 -0.18 V
10ns


A3 -0.74 V
20mV
20mV
10ns


CH1
CH2
500mV
10ns
EXT


SPECTRUM
Math
A: REF
B: REF
MKR
20 057 500.000 Hz
1.000
50.00m
MAG
490.076m
µV/√Hz
[µV/√Hz] [
]
12.5661m
DIV
DIV
START
1 000 000.000 Hz
100.0m
5.000m
STOP
100 000 000.000 Hz
RBW: 300 KHz ST: 1.36 sec RANGE: R=-20. T=-40dBm
ATT1= 0 DB


sqrt(noise_spectrum)
mW
4
2
0
0.0
0.2
0.4
0.6
0.8
1.0
efficiency

CMOS Preamplifier / Shaper

2 μm n-well CMOS Amplifier IC

Design Parameters: (Cd=3 pF)	Specifications	Measured
Dynamic range	$1x10^5$	$2x10^4$
Settling to 1%	< 16 ns	< 12 ns
	Simulation	
3 dB bandwidth	50 MHz	50 MHz
Output voltage noise SD @20 MHz	4 nV/√Hz	12 nV/√Hz
Output voltage noise	25 μV rms	75 μV rms
Transfer gain	320 mV/pC	280 mV/pC
Equivalent input noise charge	500 e rms	1700 e rms
Output swing into 25 Ω	2.5 Vp-p	2 Vp-p
Power consumption	75 mW	75 mW

Most problems can be explained by
hot-electron effects

Work on them!

Noise performance of NMOS device in Orbit's 2μm n-well process

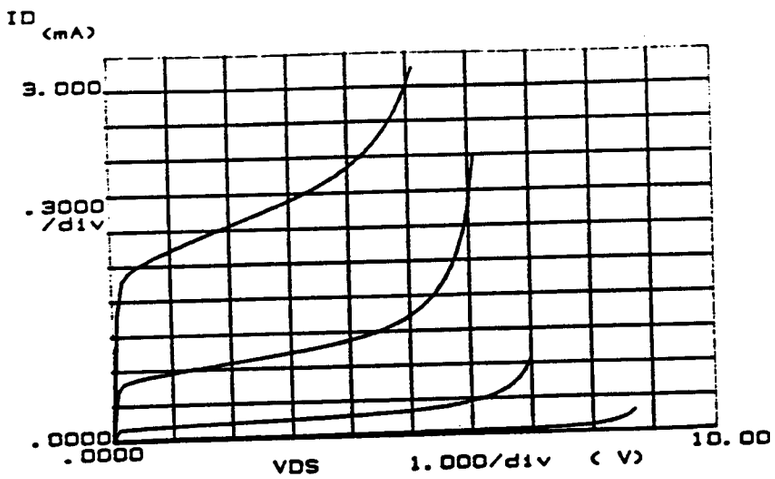
W/L= 1500/2, Ci~ 1.9 pF, Vds= 3 V, Rg= 15 Ω

Id	gm	Id/W	measured current	measured voltage	ideal voltage	√γ	γ	Γ
mA	mmhos		pA/√Hz	nV/√Hz	nV/√Hz			
0.1	2	.07	7	3.5	2.4	1.5	2.2	1.5
1	10	.7	28	2.8	1.2	2.3	5.4	3.6
10	30	7	65	2.2	0.8	2.8	7.6	5.0

W/L= 1300/2, Ci~ 1.6 pF, Vds= 0.5 V, Rg= 15 Ω

Id	gm	Id/W	measured current	measured voltage	ideal voltage	√γ	γ	Γ
mA	mmhos		pA/√Hz	nV/√Hz	nV/√Hz			
0.3	3.7	.23	10.5	2.9	1.8	1.6	2.6	1.7
1	7.3	.77	16.7	2.3	1.3	1.8	3.1	2.1
3	13	2.3	25.1	1.9	1.0	1.9	3.6	2.4

****** GRAPHICS PLOT ******
2600/2

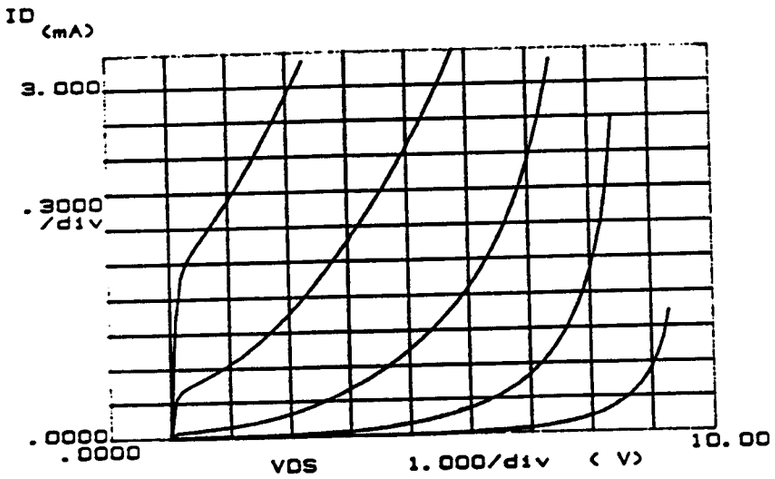


Variable1:
VDS -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .1000V

Variable2:
VG -Ch3
Start .6000V
Stop .8000V
Step .1000V

Constants:
VS -Ch1 .0000V

****** GRAPHICS PLOT ******
2600/2

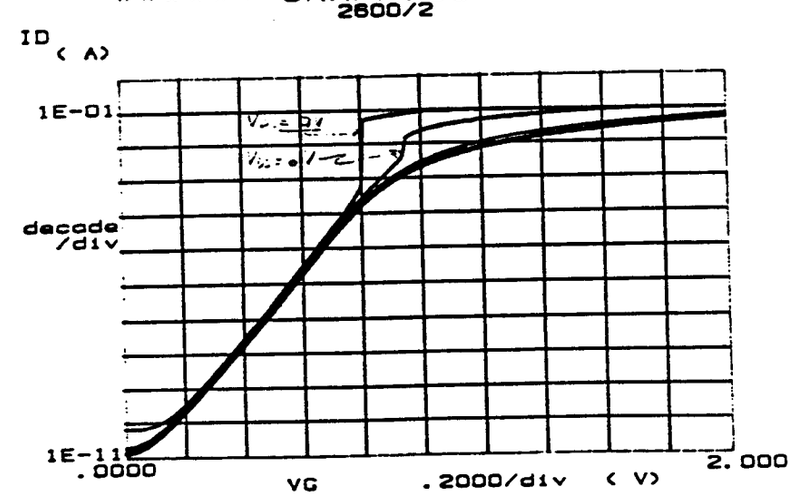


Variable1:
VDS -Ch2
Linear sweep
Start 1.0000V
Stop 10.000V
Step .1000V

Variable2:
VG -Ch3
Start 1.8000V
Stop 2.2000V
Step .1000V

Constants:
VS -Ch1 1.0000V

****** GRAPHICS PLOT ******
2600/2



Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop 2.0000V
Step .0100V

Variable2:
VD -Ch2
Start 3.0000V
Stop 7.0000V
Step 1.0000V

Constants:
VS -Ch1 .0000V

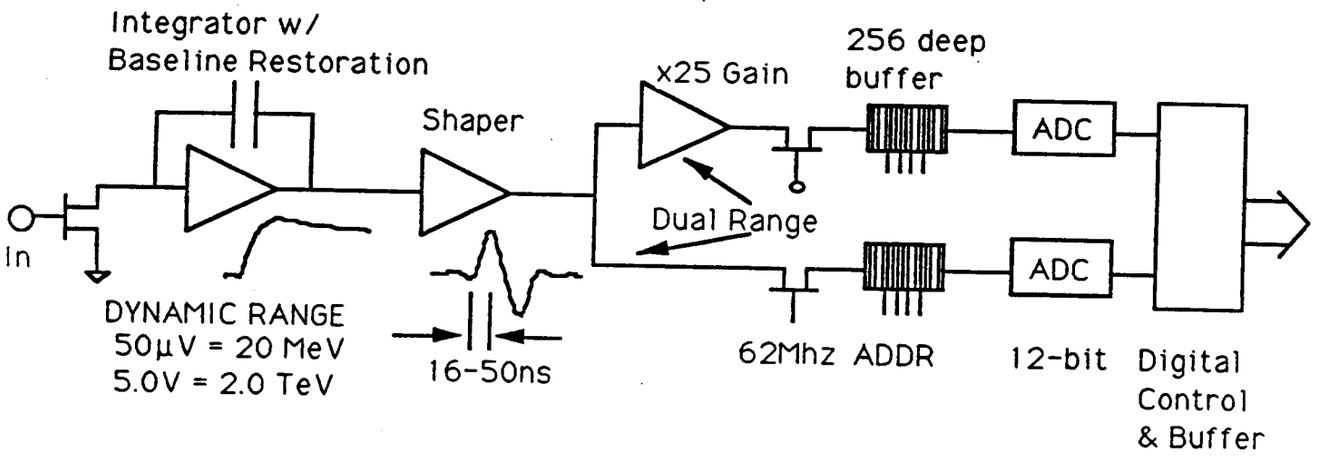
Switched Capacitor Memory/Address List Processor

M. Levi (LBL)

Front-End Electronics for the SSC

Participants: R. Ely, R. Jared, I. Kipnis, F. Kirsten,
S. Kleinfelder, M. Levi, T. Merrick, O. Milgrome

Task: Development of Analog Readout Circuits for Calorimetry



Requirements:

1) High Speed -- 62.5 Mhz
2) Large Dynamic Range -- 18 bits Constructed from Dual Range of 12 bits each
3) 256 Storage Locations (4 μsec Memory)
4) Digitize Data After Trigger Decision
5) Store Signal Transient
6) Random Access Analog Memory
7) Simultaneous Read & Write
8) Hold Data Pending Trigger Decision
9) On Chip ADC
10) Digital Storage Buffer

STANDARD [illegible] ARCHITECTURE

ACCEPTS L1 / L2 / READOUT STRIBES

MANIPULATES STORED DATA UNTIL READOUT

UP TO 4 μSEC CAN BE STORED PENDING L1

BUFFERS DATA IN SAME STORAGE FOR L2.

[illegible]

[illegible]

[illegible]

[illegible]

TRIGGER CHAIN OPERATES ON REDUCED SET OF INFO

TRIGGER GRANULARITY ≤ 0.2 ADEQUATE → SAVES

GRANULARITY 0.1 x 0.1 ASSUMED HERE

FULL READOUT [illegible] AFTER [illegible] ACCEPT

C.I. FOR SHOWER MAX

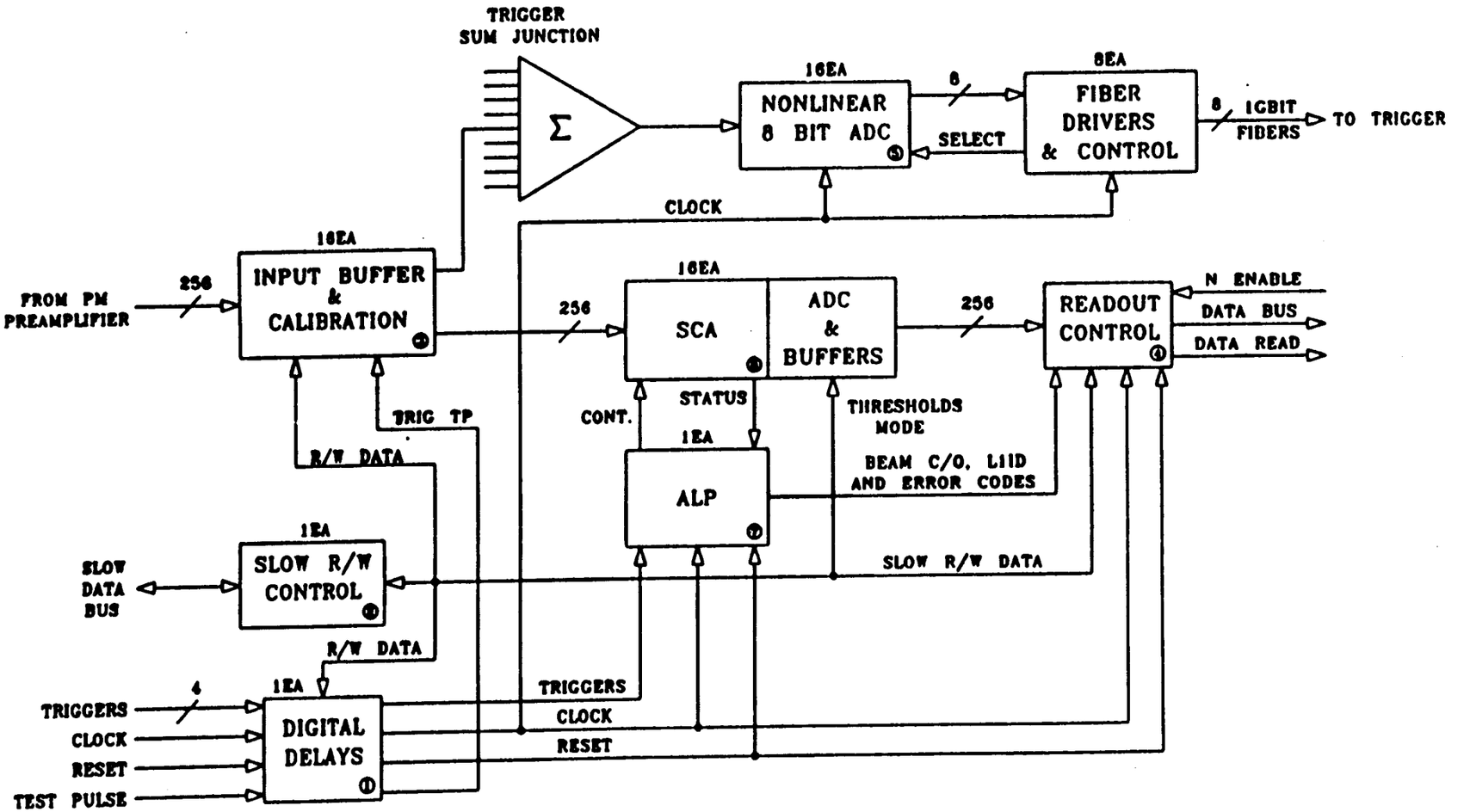
[illegible]

[illegible]

[illegible]

[illegible]

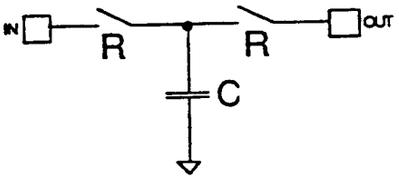
SCA READOUT, CALIBRATION & ZERO SUPPRESSION

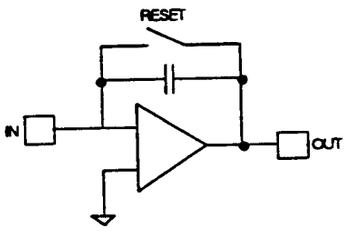


Noise in a Capacitive Sampling Device

Thermal noise will limit the maximum attainable dynamic range in the signal sampling device. Thermal noise arises from any dissipative element both active or passive i.e. transistor, resistor.

A transistor switch is a common element in ADC's, sample & holds (SCA's), and integrators.





Equivalent noise voltage of sample and hold is given by,

$$e_n^2 = 2 \times \{ 4kTR \times f \}$$
$$= 2 \times \{ 4kTR/(4RC) \}$$
$$= 2kT/C$$
$$= 2kT\gamma/C \quad \gamma \geq 1 \text{ for non-ideal devices}$$

e.g. for C = 1 pF and $\gamma = 4$,

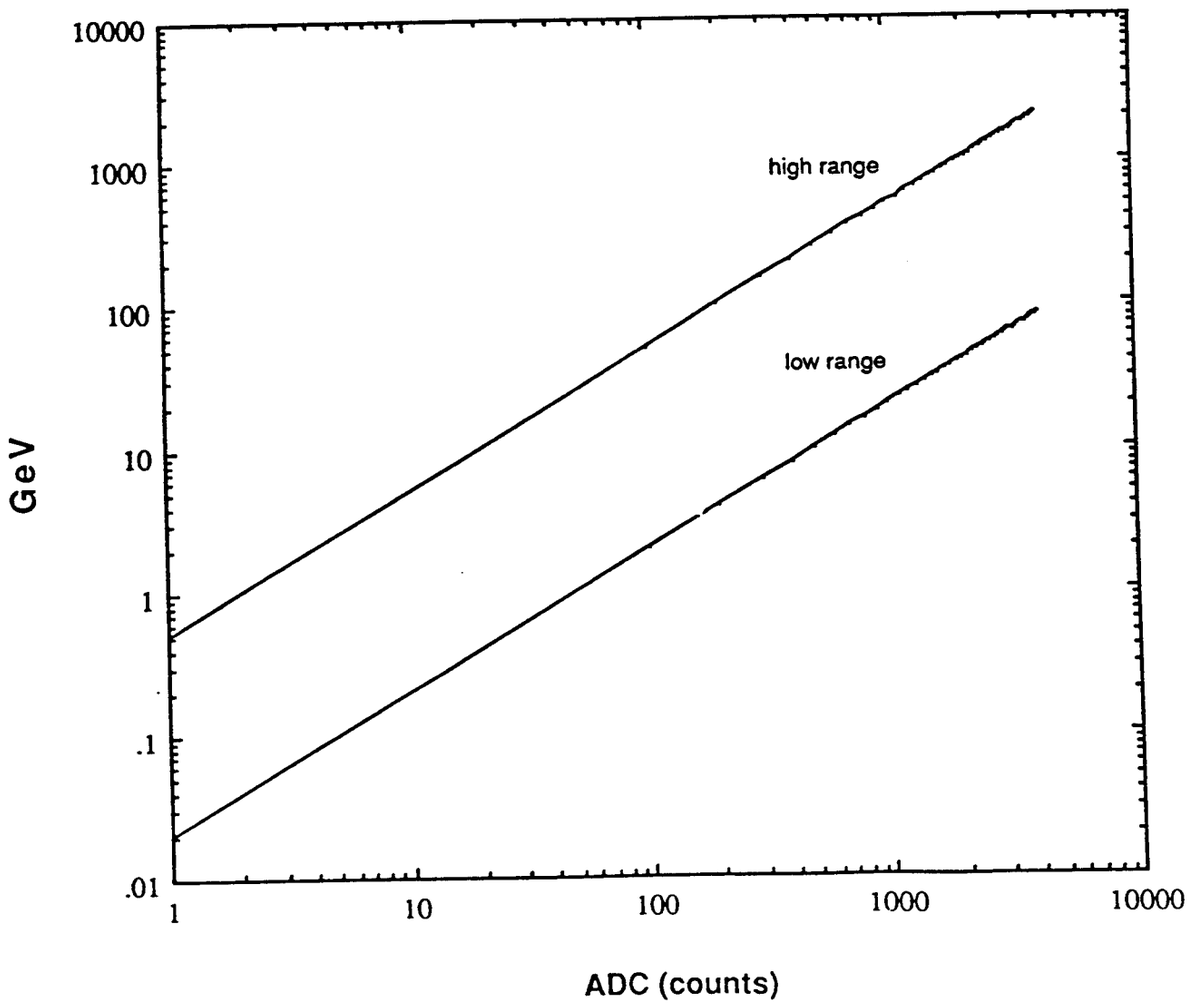
$$e_n \approx 180\ \mu V$$

For a 5V swing, maximum dynamic range is: 1::27000

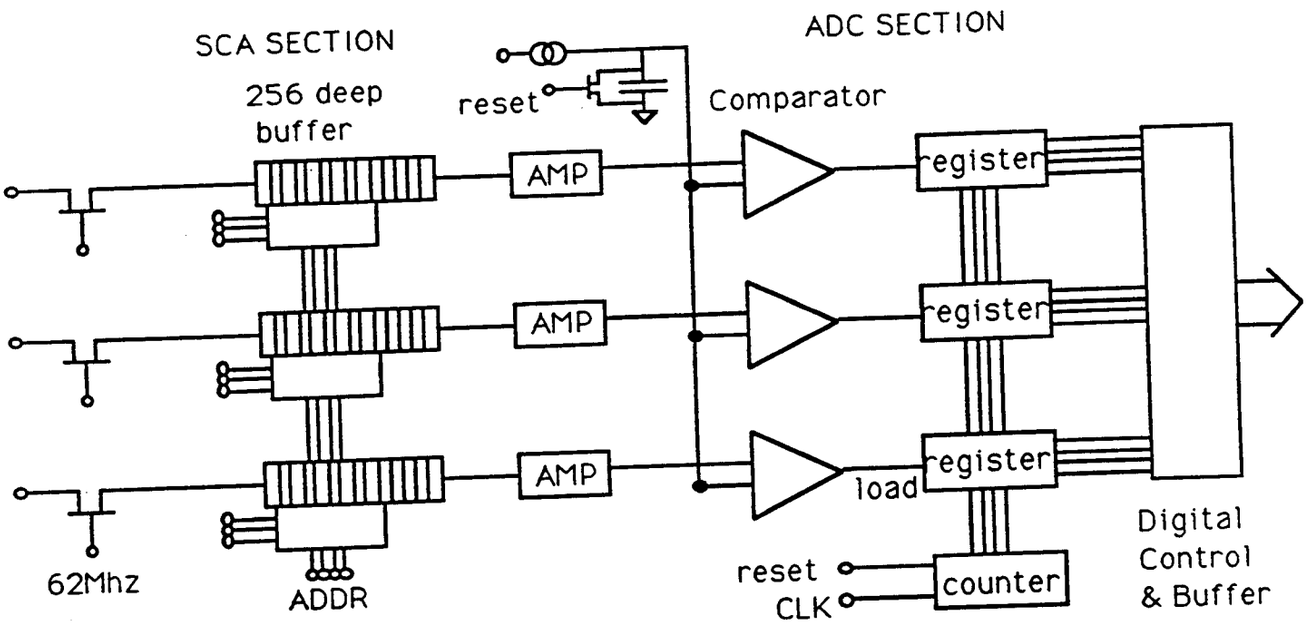
To achieve larger dynamic range must use two or more ranges

Dynamic Range

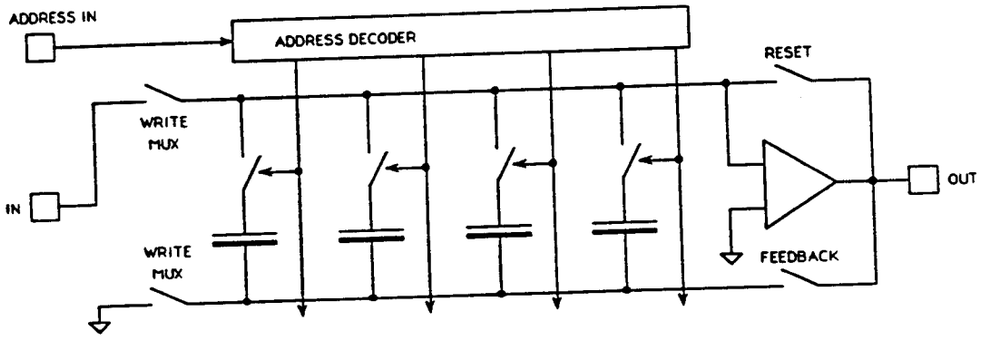
- Two 12-bit ranges (1:4096)
- Dual range extends the dynamic range to 1:100000
- Least count is 20 MeV
- Greatest count is 2 TeV
- Fractional Accuracy is always « 1%



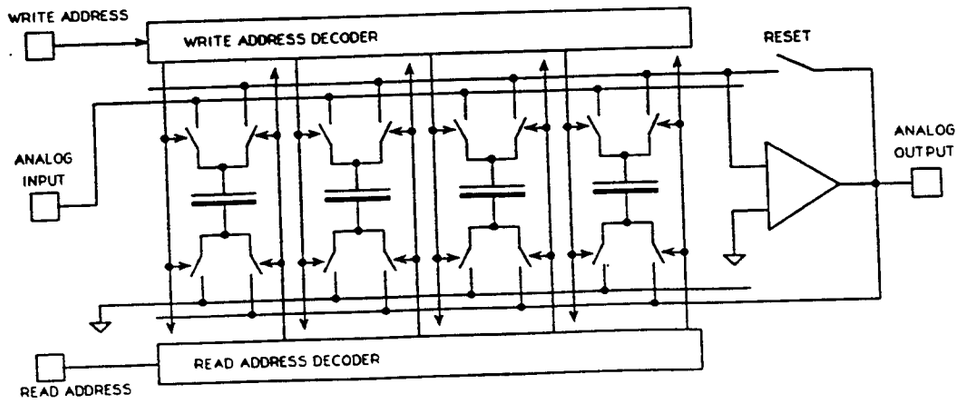
A 256 Element 16 Channel Switched Capacitor Array With a 12-bit Single Slope ADC



Basic Cell of Switched Capacitor Array:



Basic Cell with Simultaneous Read/Write Capability:



SCA Pedestal Variation

⇒ Multiple shots averaged showing capacitor & switch variation

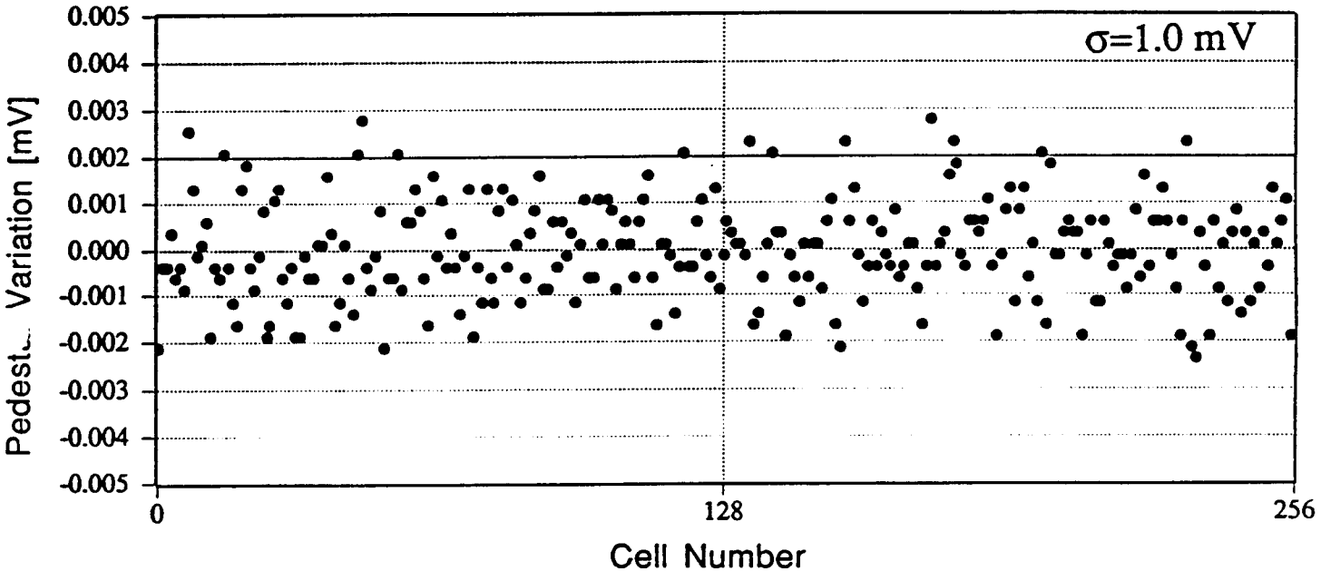
⇒ Differential inputs with 10 volt effective input swing.

⇒ Pedestal variation must be ≤ 1.2 mV rms in a 5V range to achieve 12-bit dynamic range (1:4096).

SCA Pedestal Variation

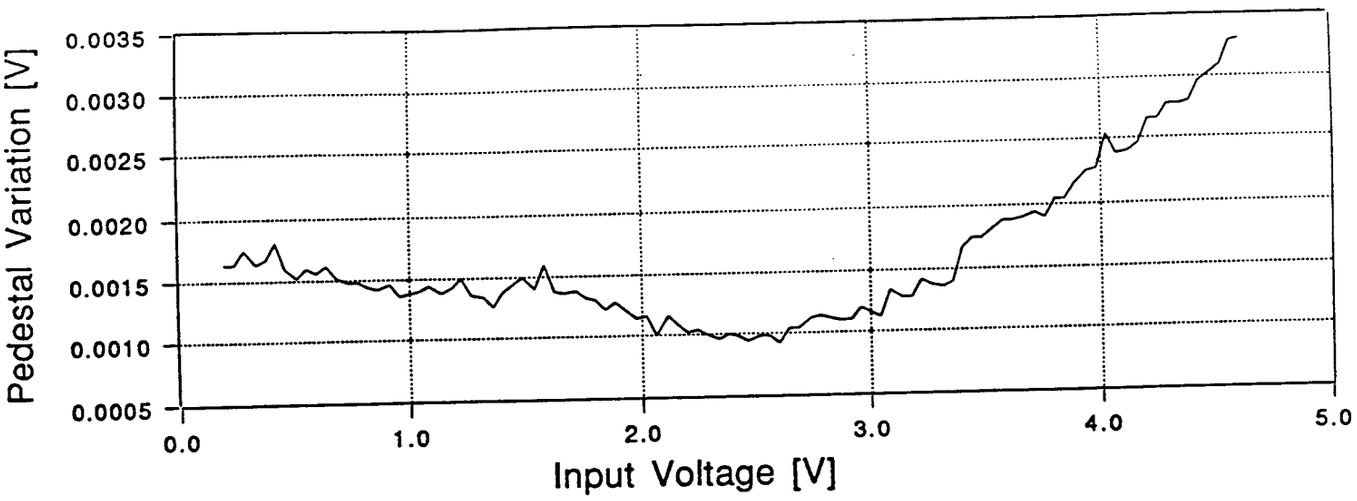
⇒ Single shot variation dominated by kT+1/f noise

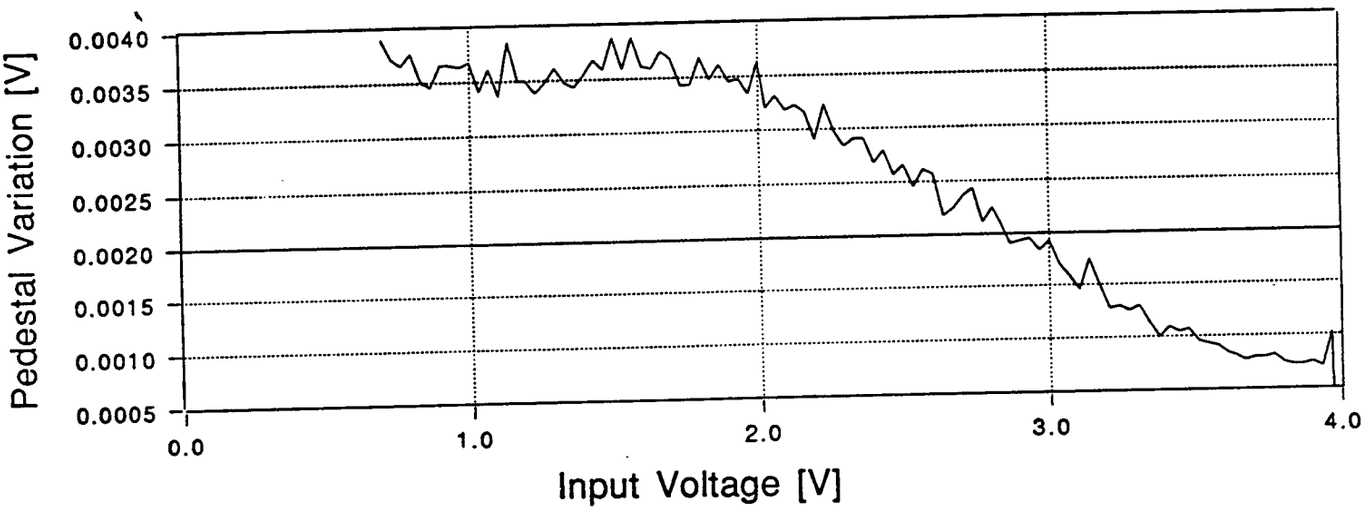
⇒ Differential inputs with 10 volt effective input swing.

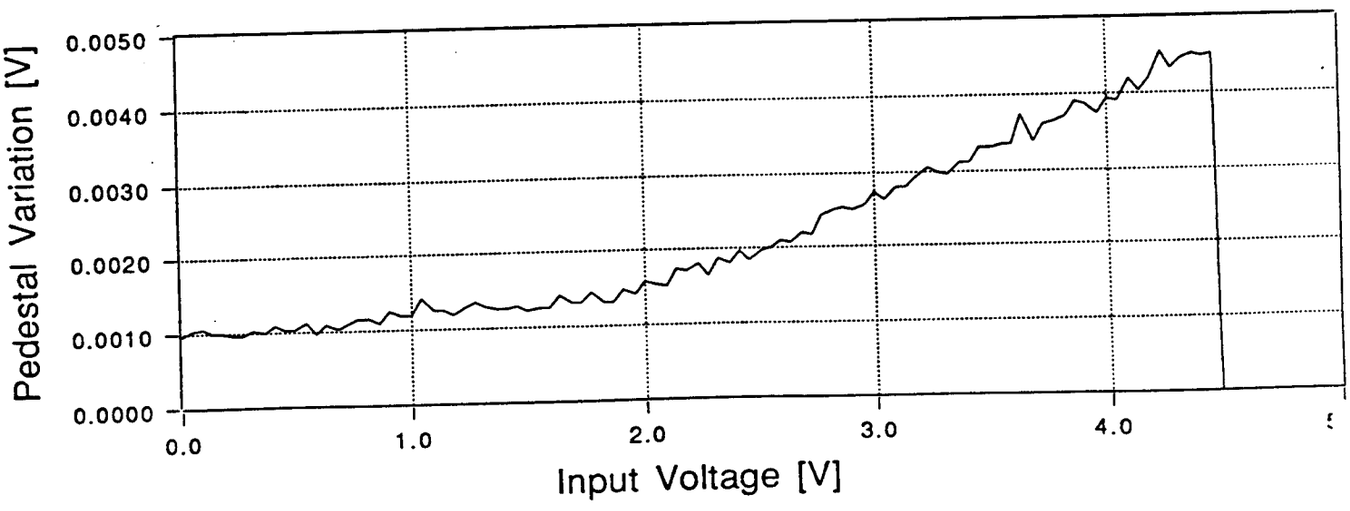


⇒ Pedestal variation must be ≤ 1.2 mV rms in a 5V range to achieve 12-bit dynamic range (1:4096).

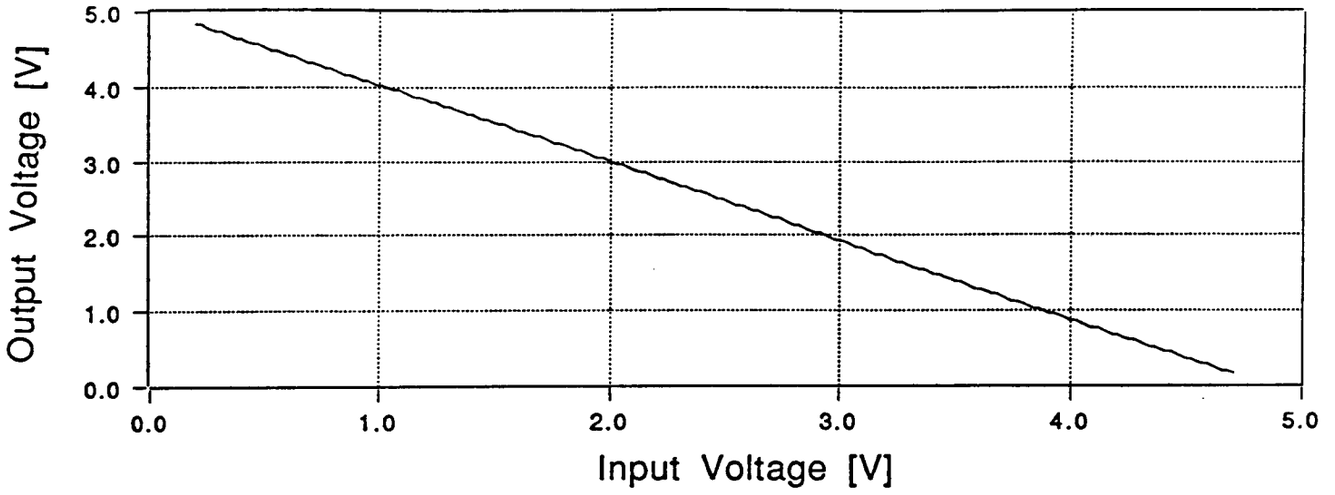
SCA Pedestal Variation

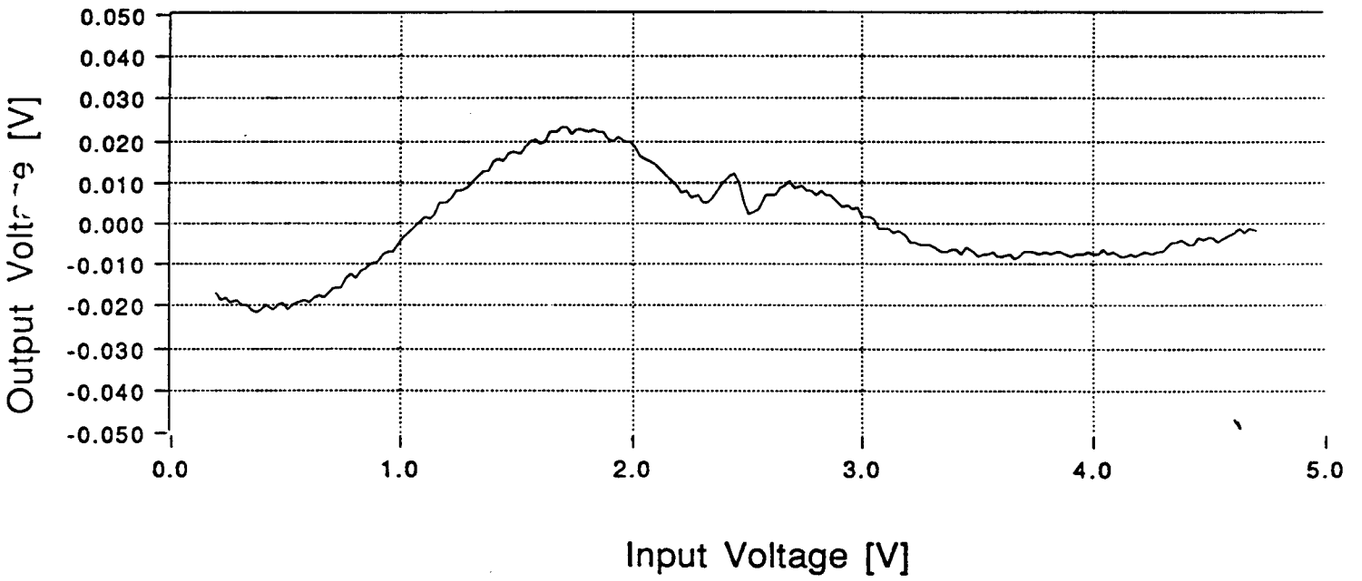






SCA Linearity





Chip Parameters:

SCA Parameters	Achieved Performance
No. channels/chip	16
No. of elements/channel	256
Power/channel	10 mW
Non-linearity	+/- 0.1%
Pedestal variation	0.5 mV rms
Charging time constant	1.5 ns
Channel dynamic range	5000
Maximum sample rate	90 MHz
Maximum readout rate	200 KHz
Noise floor	0.7 mV rms
Input voltage range	0.2-4.8 Volts
Capacitor droop rate	0.1 mV/msec
Output Settling Time	1.2 μsec (to 0.02%)

Current Status:

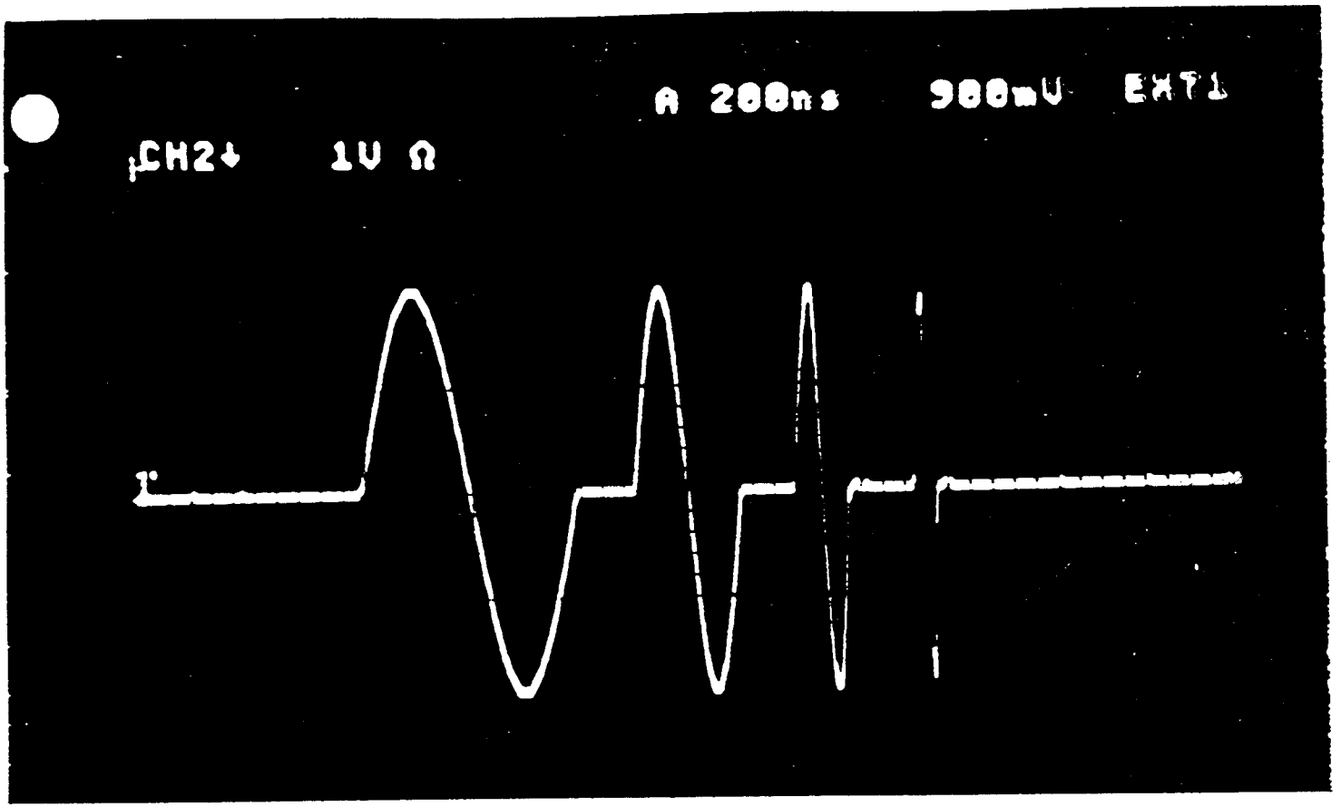
Work continuing on maintaining large dynamic range.

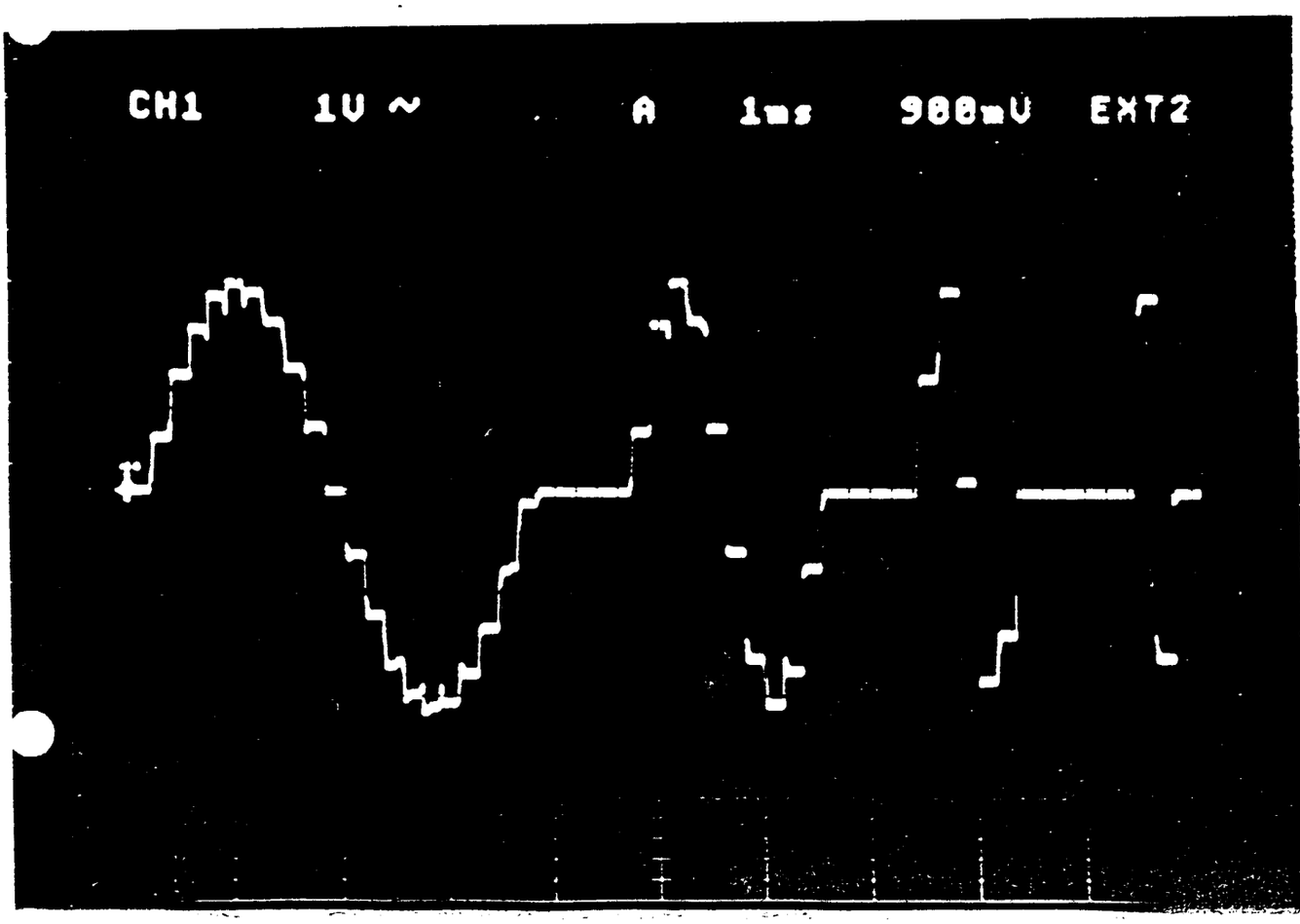
Learning how to reduce effects of digital noise.

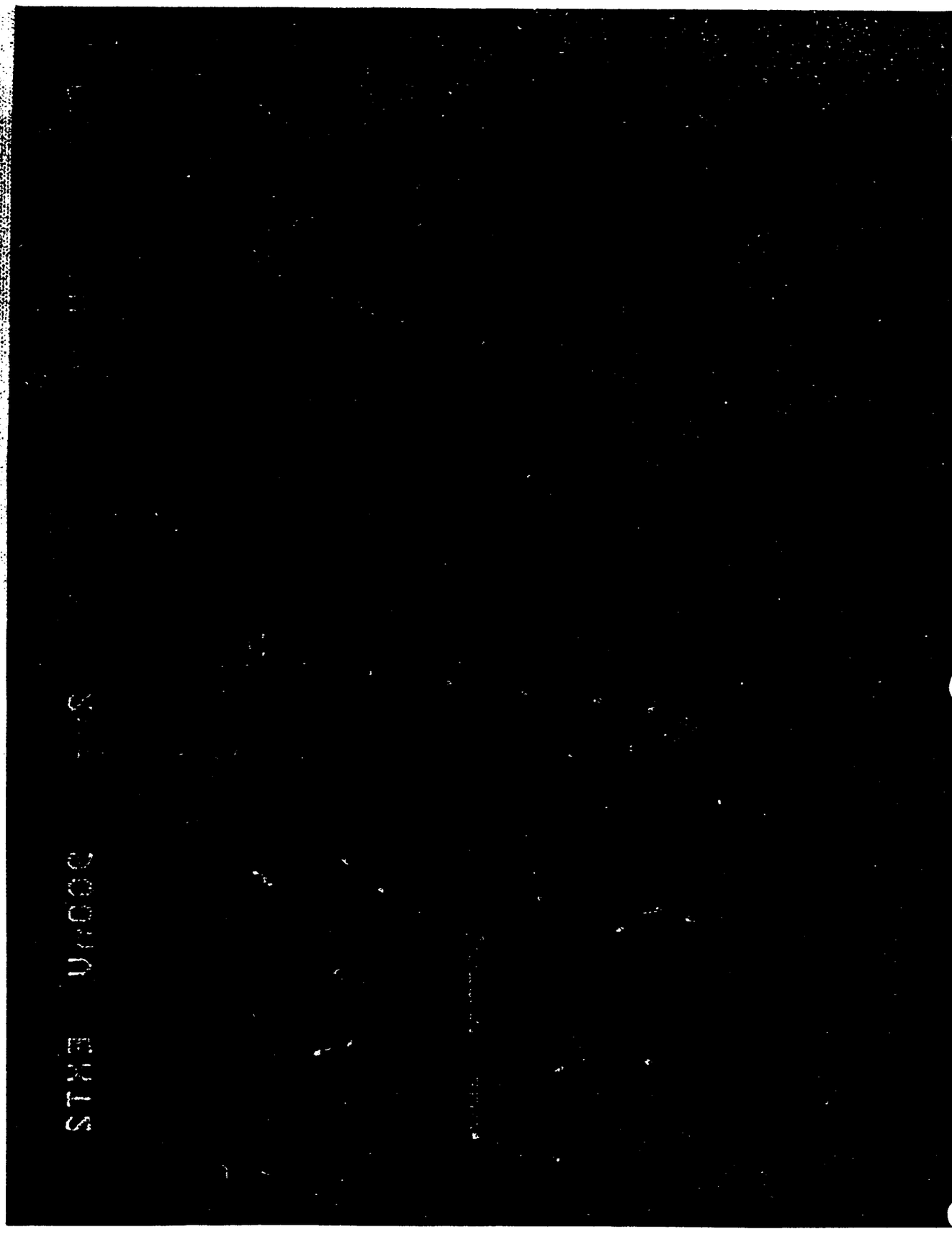
ADC being integrated with SCA.

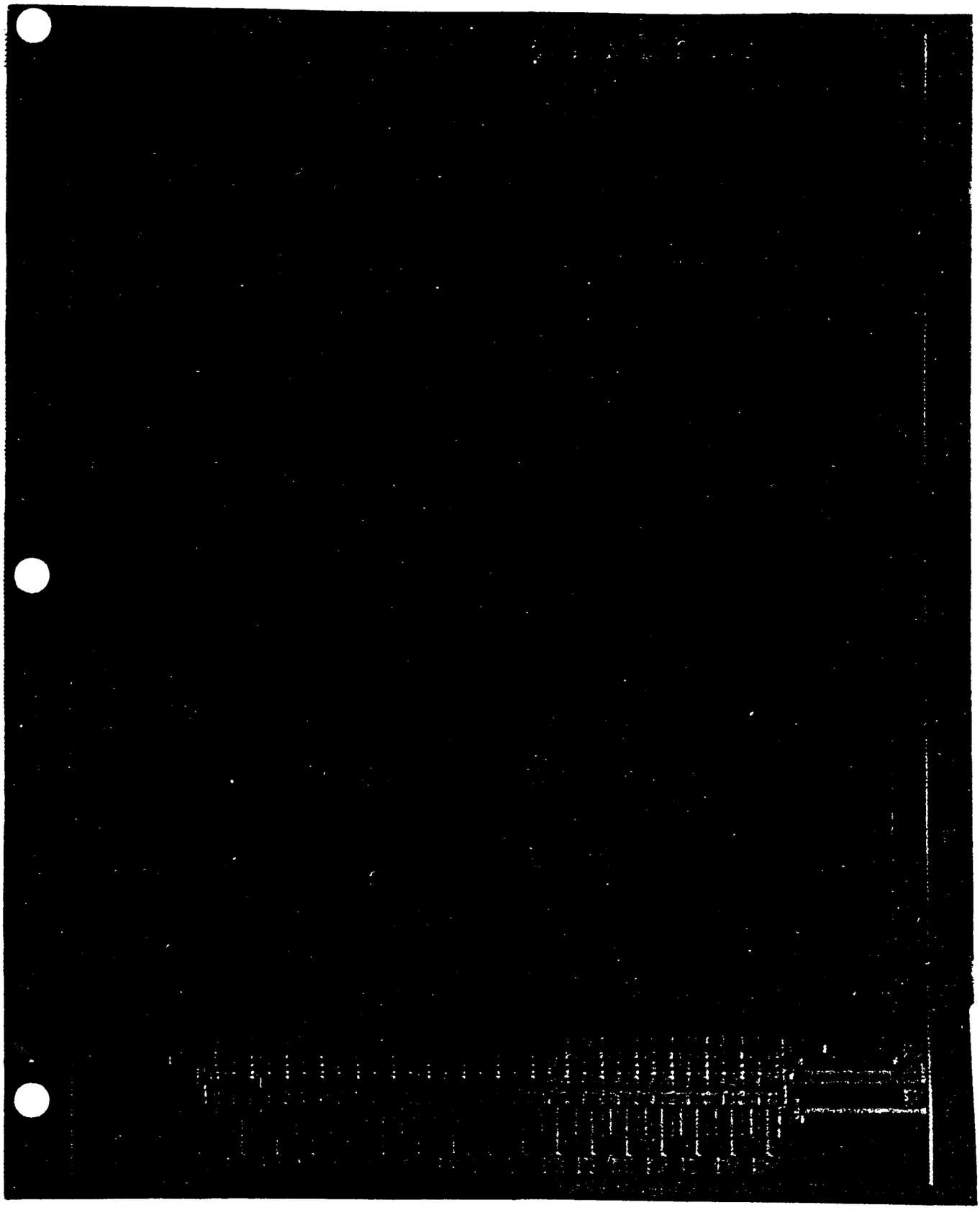
Design Work in Progress:

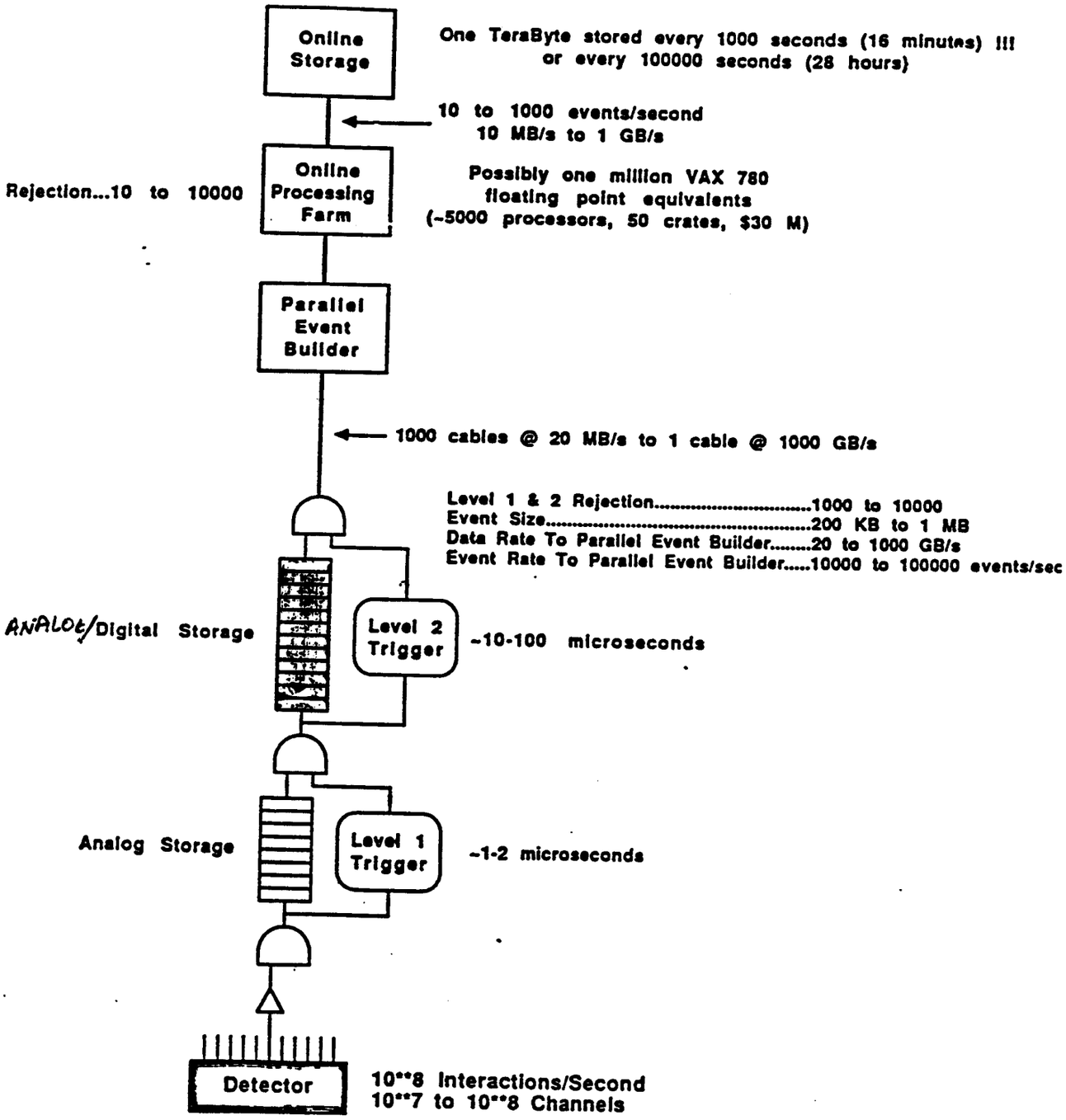
1) Design an Analog Store with 5 volt Differential Inputs
2) Address Generation & Pointer Manipulation
3) High Speed Preamp & Shaper


A 200ns 900mV EXT1
CH2↓ 1V Ω


CH1 1V ~ A 1ms 900mV EXT2



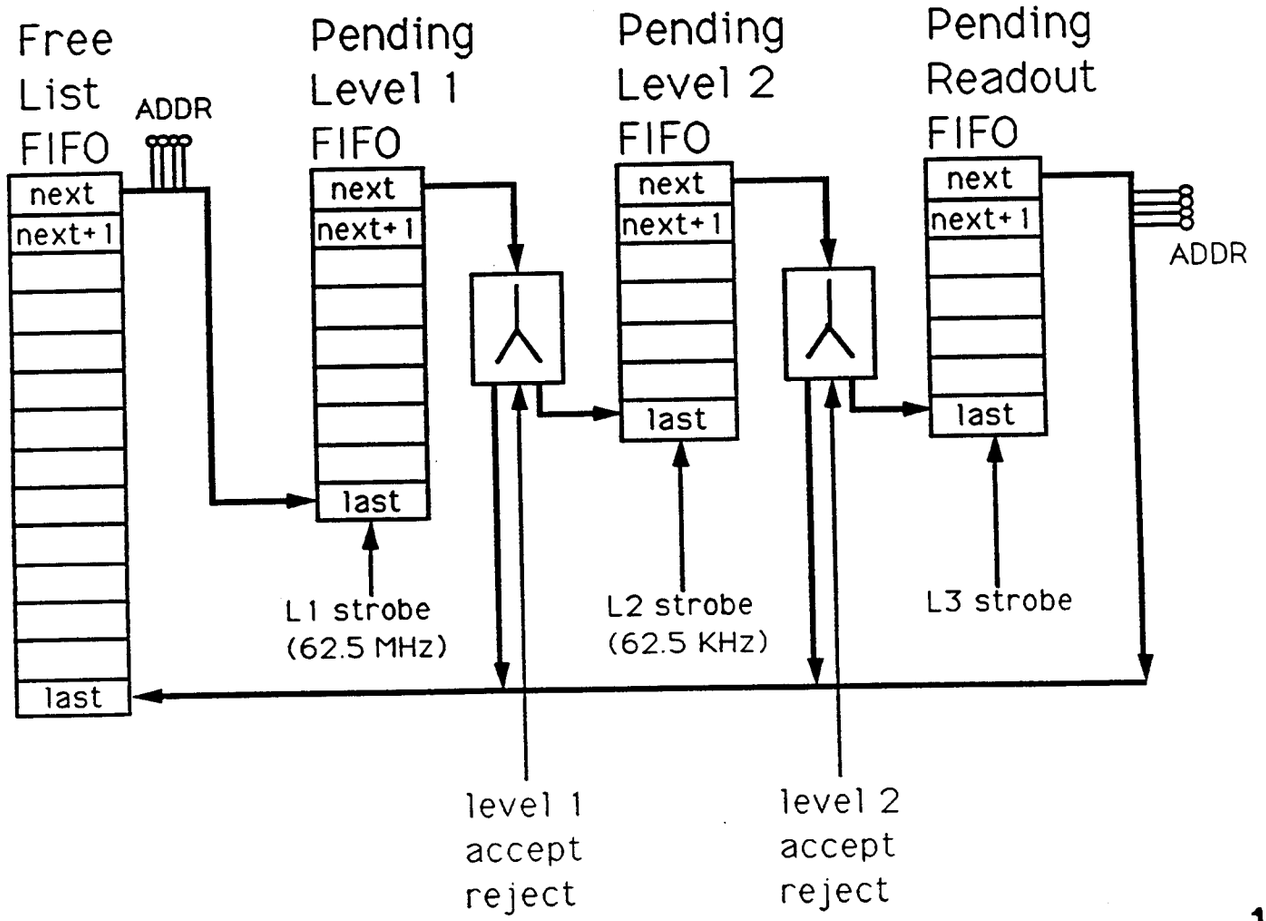


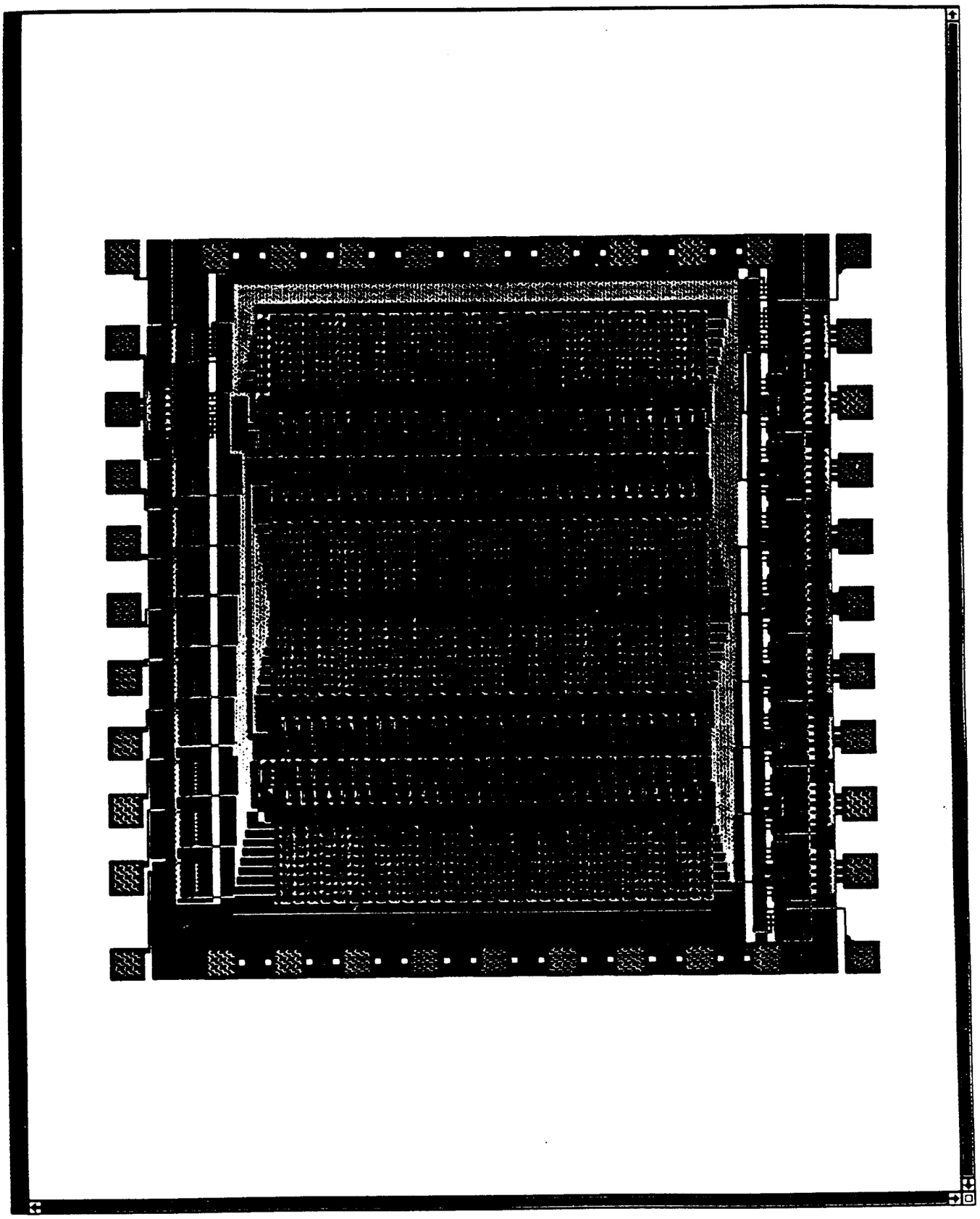

Online Storage
One TeraByte stored every 1000 seconds (16 minutes) !!!
or every 100000 seconds (28 hours)
10 to 1000 events/second
10 MB/s to 1 GB/s
Online Processing Farm
Rejection...10 to 10000
Possibly one million VAX 780
floating point equivalents
(~5000 processors, 50 crates, $30 M)
Parallel Event Builder
1000 cables @ 20 MB/s to 1 cable @ 1000 GB/s
Level 1 & 2 Rejection.....1000 to 10000
Event Size.....200 KB to 1 MB
Data Rate To Parallel Event Builder.....20 to 1000 GB/s
Event Rate To Parallel Event Builder.....10000 to 100000 events/sec
ANALOG/Digital Storage
Level 2 Trigger
~10-100 microseconds
Analog Storage
Level 1 Trigger
~1-2 microseconds
Detector
10**8 Interactions/Second
10**7 to 10**8 Channels

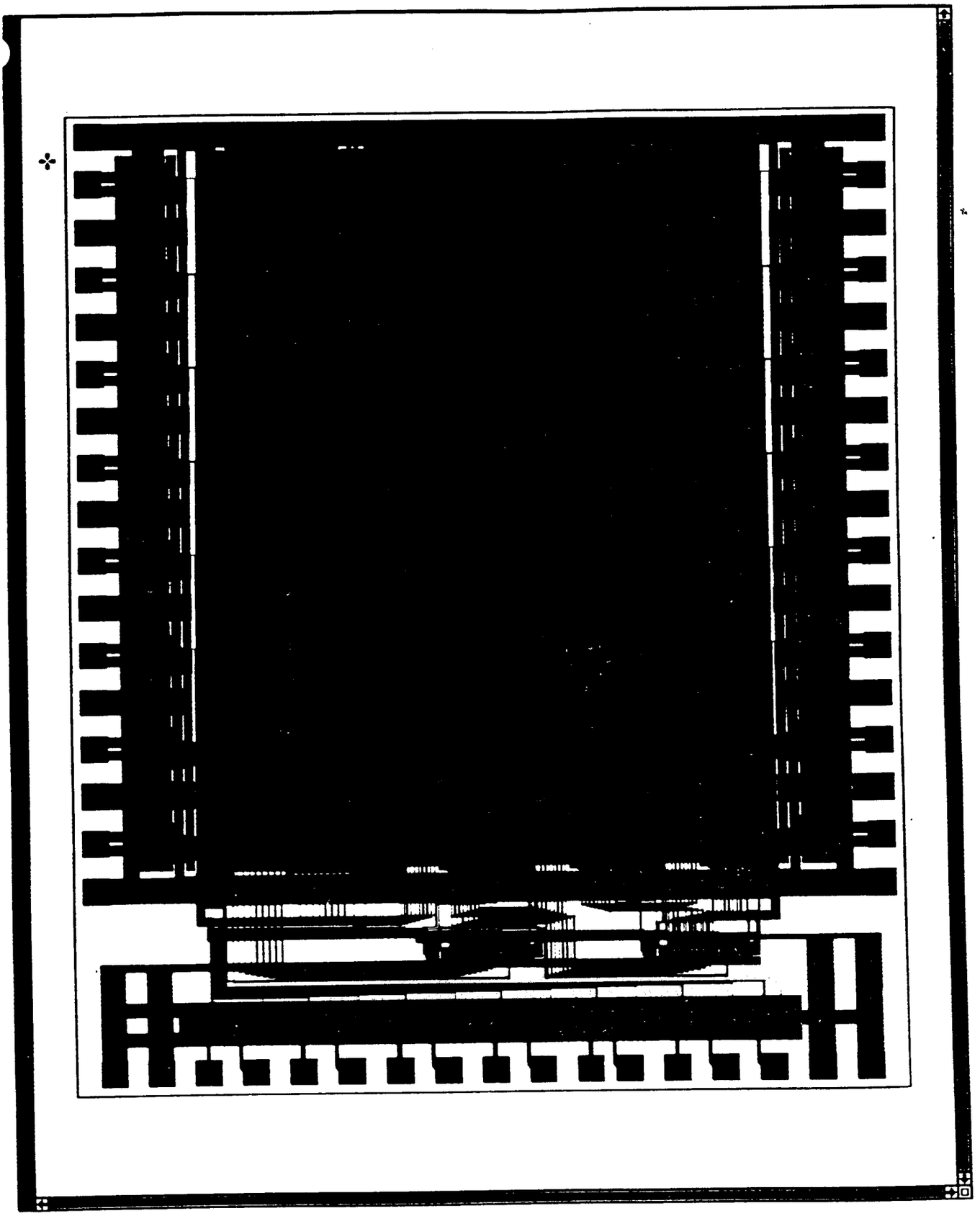
Address List Processor

Address Generation & Pointer Manipulation:

1) Generates input storage locations for the SCA at 62.5 MHz.
2) Maintains a list of saved data until trigger decision is complete.
3) Propagates the list of pointers through the multi-tiered trigger decision chain.
4) Generates addresses for SCA readout.
5) Consists of four high-speed First-In First-Out memories.







Conclusions

1) Completed conceptual and baseline design for calorimeter front-end electronics based on switched capacitor readout.

   Design is compatible with a variety of calorimetric detectors (*e.g.* barrel, end-cap, shower max.), and a variety of calorimetric technologies (*e.g.* scintillator or liquid argon).

2) First version of 12-bit ADC functional.
   - 32 μsec conversion time at 2 mW in 2μm CMOS.
   - 16 μsec conversion time with faster clock.

3) SCA moved to advanced technology 1.2 μm CMOS process. Version with 256 elements/channel just fabricated.

4) L1/L2/Readout Architecture chip (ALP) layout completed in 1.2 μm CMOS.
   - FIFO memory fabricated in 2 μm CMOS and tested at speeds up to 330 MHz.

5) Design of preamp for low gain scintillator PMT initiated.

6) Design of multi-channel board begun.

- Decision point later this year for SDC electronics
- Barrel/Endcap Calorimeter Electronics
- Detector at EM Shower Maximum

ADC/Op-Amp/Comparator

O. Milgrome (LBL)

12 BIT MULTICHANNEL ANALOG TO DIGITAL CONVERTER

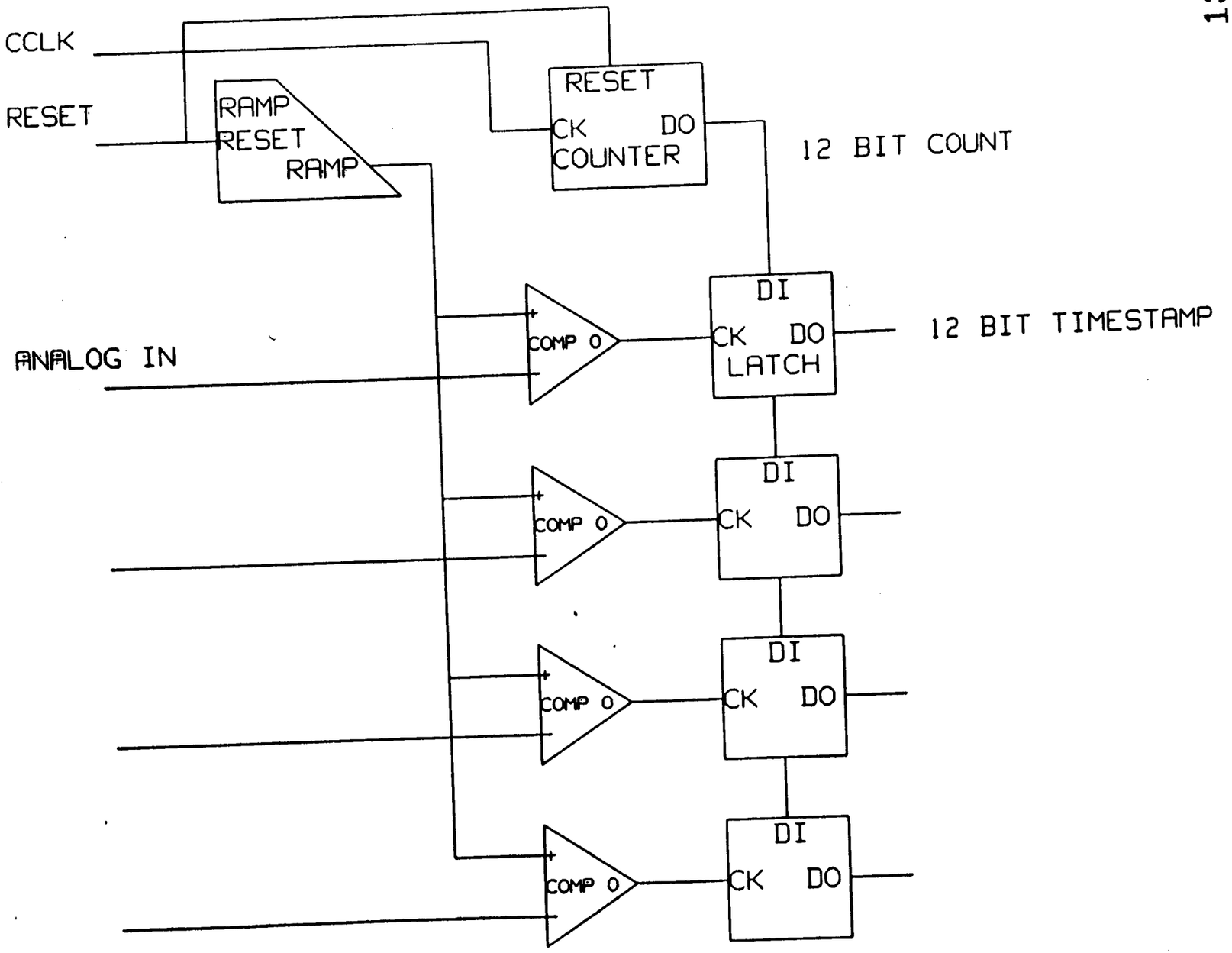
O. MILGROME, S. KLEINFELDER, M. LEVI

LAWRENCE BERKELEY LABORATORY

PURPOSE: READOUT SCA AFTER TRIGGER

TARGET SPECS	RESULTS ACHIEVED
RESOLUTION > 1/4096	1/4096
LINEARITY > 1/128	1/4096
CONVERSION SPEED < 64US	< 32US
POWER PER CHANNEL < 10MW	5MW

MULTICHANNEL SINGLE SLOPE ADC



ADC

Counter

12-bit pipelined gray code counter.
Counts on every edge of 125 MHz clock (250 MHz effective rate).
5 MW

Analog Ramp

5V ramp in 32 µsec.
Excellent linearity due to improved error amplifier
4 MW

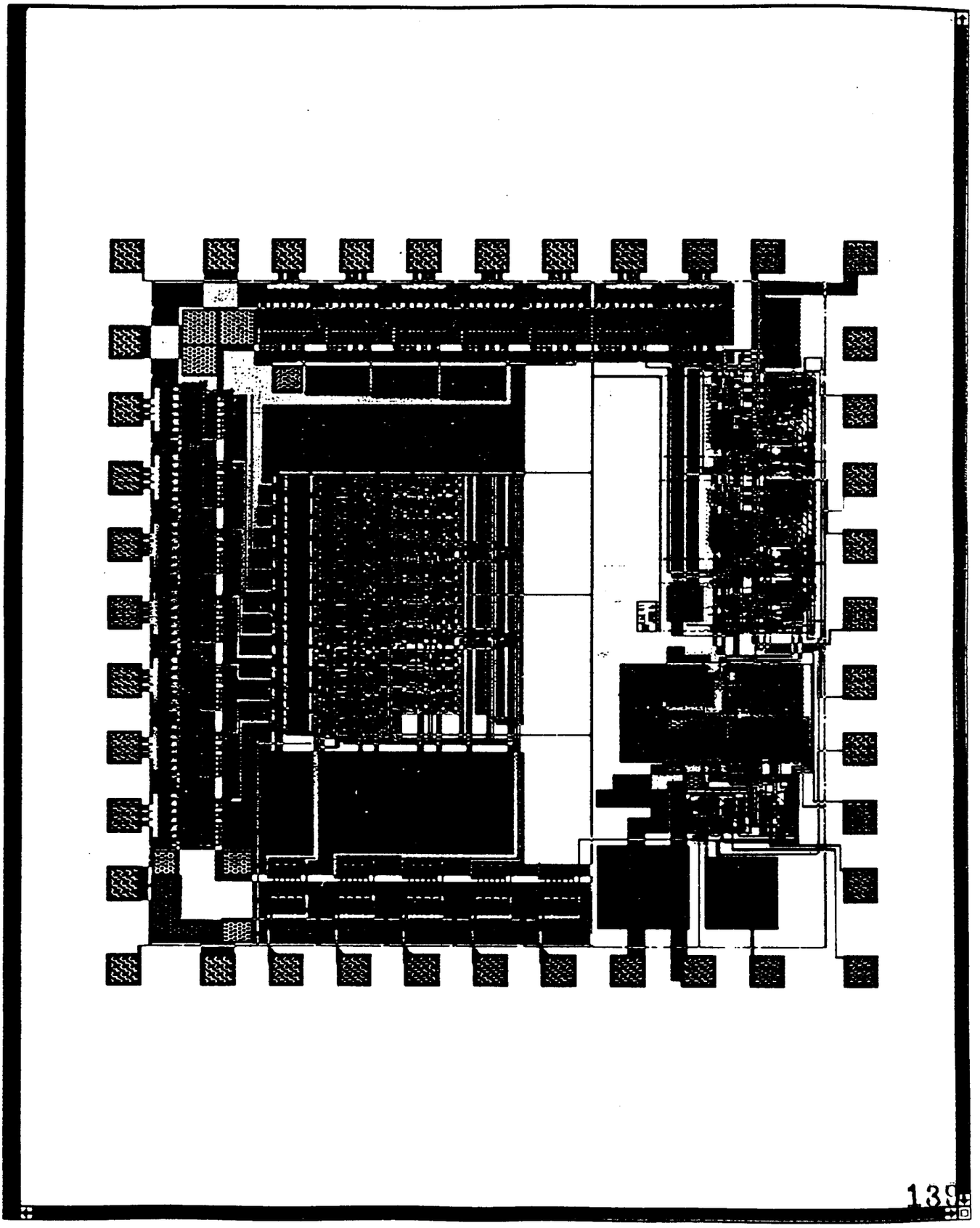
Comparator

5 stage linear amplifier with hysteresis
DC gain of 10^8
sensitivity ≤ 1 mV
5 mW/channel

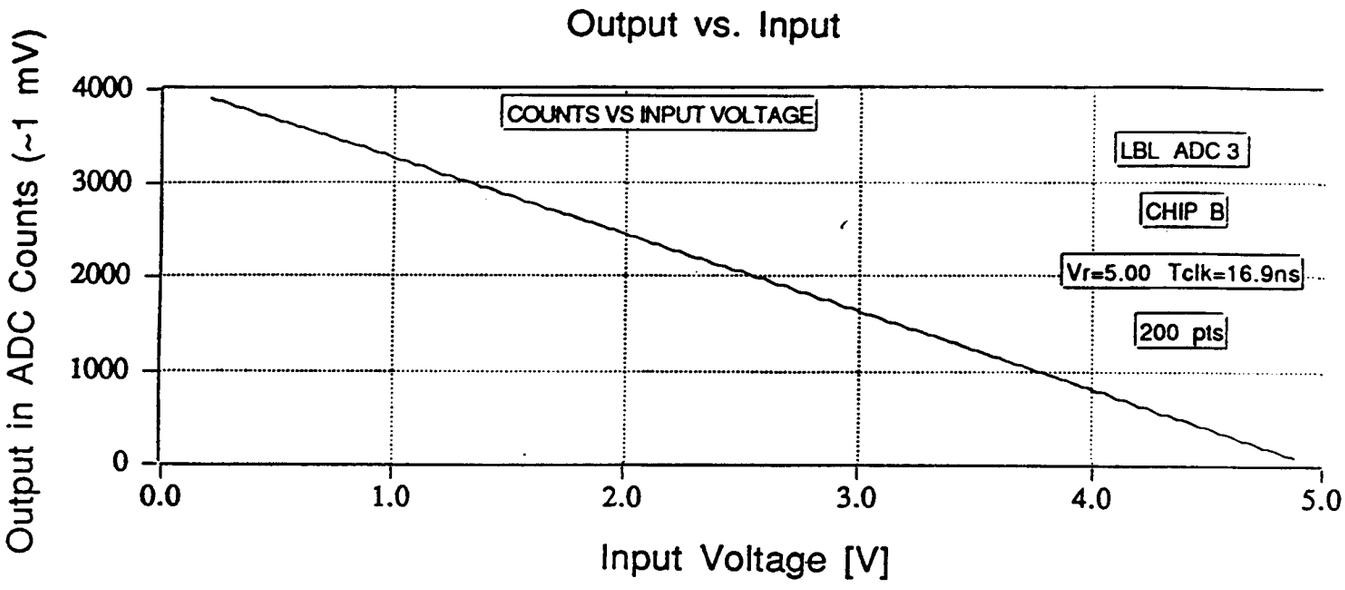
Operation

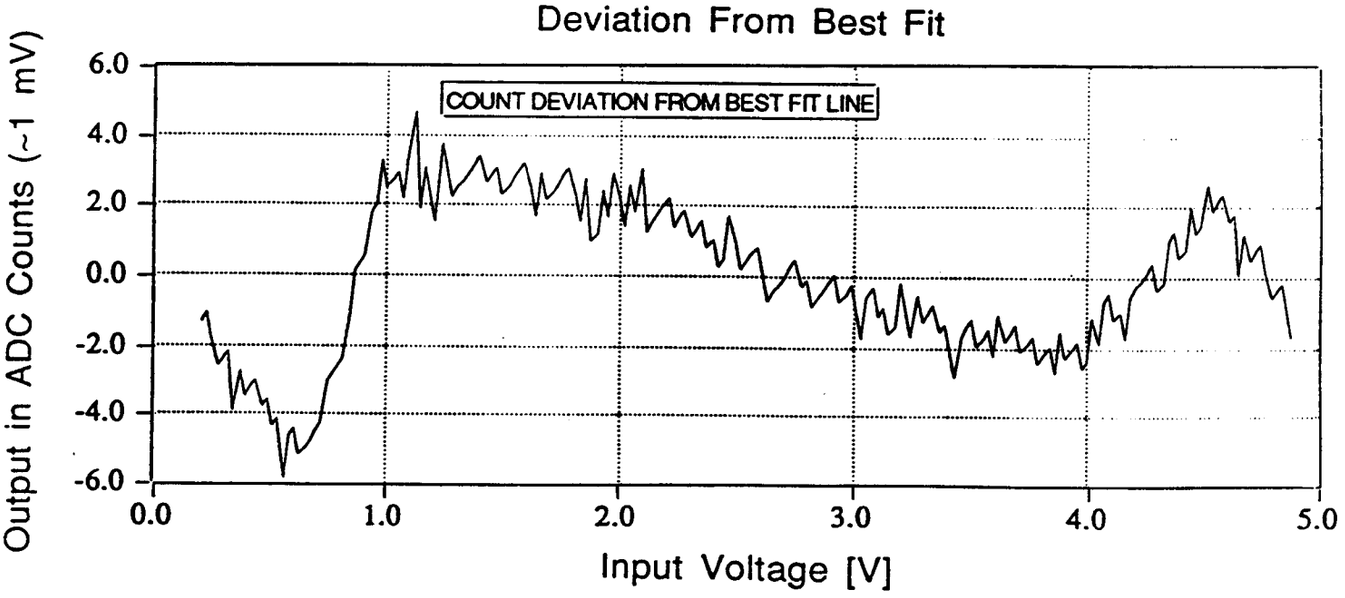
12 bit conversion with 32 kHz throughput.

Integrated circuit successfully combines high speed CMOS f_{clk} = 62 MHz with analog signals smaller than 1 mV

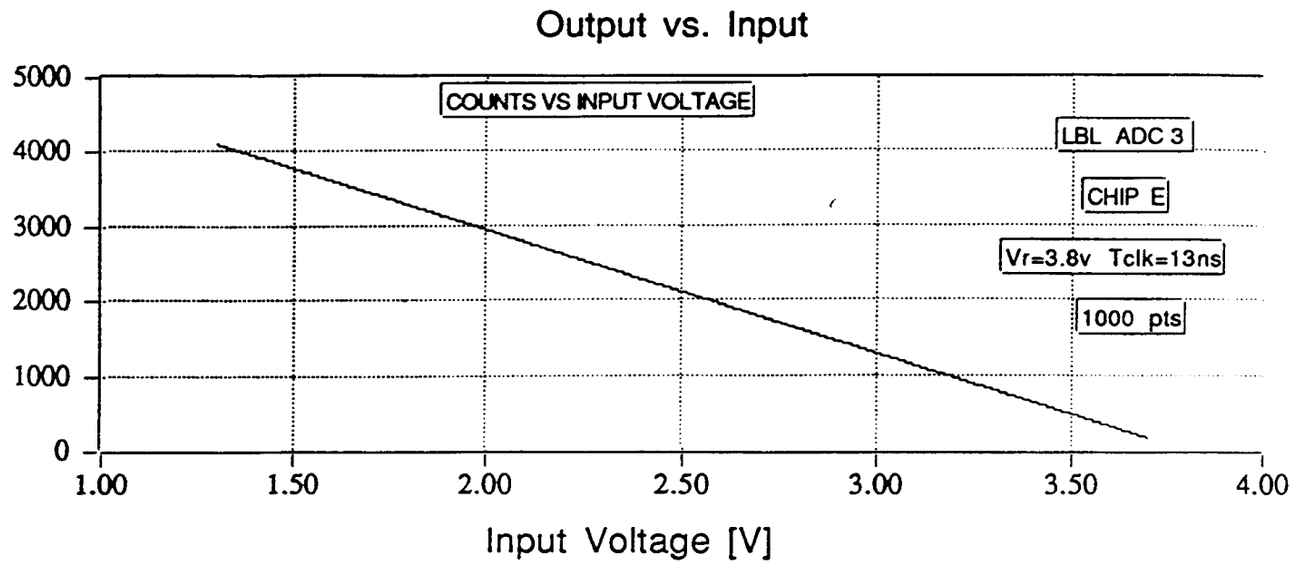


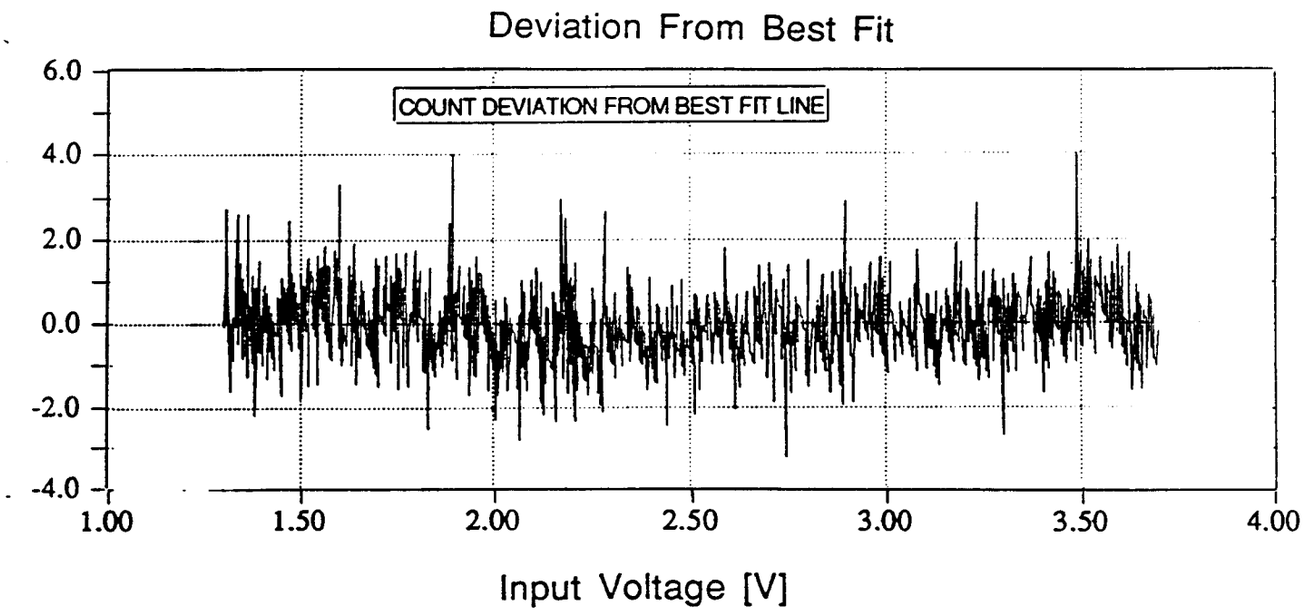
ADC Linearity



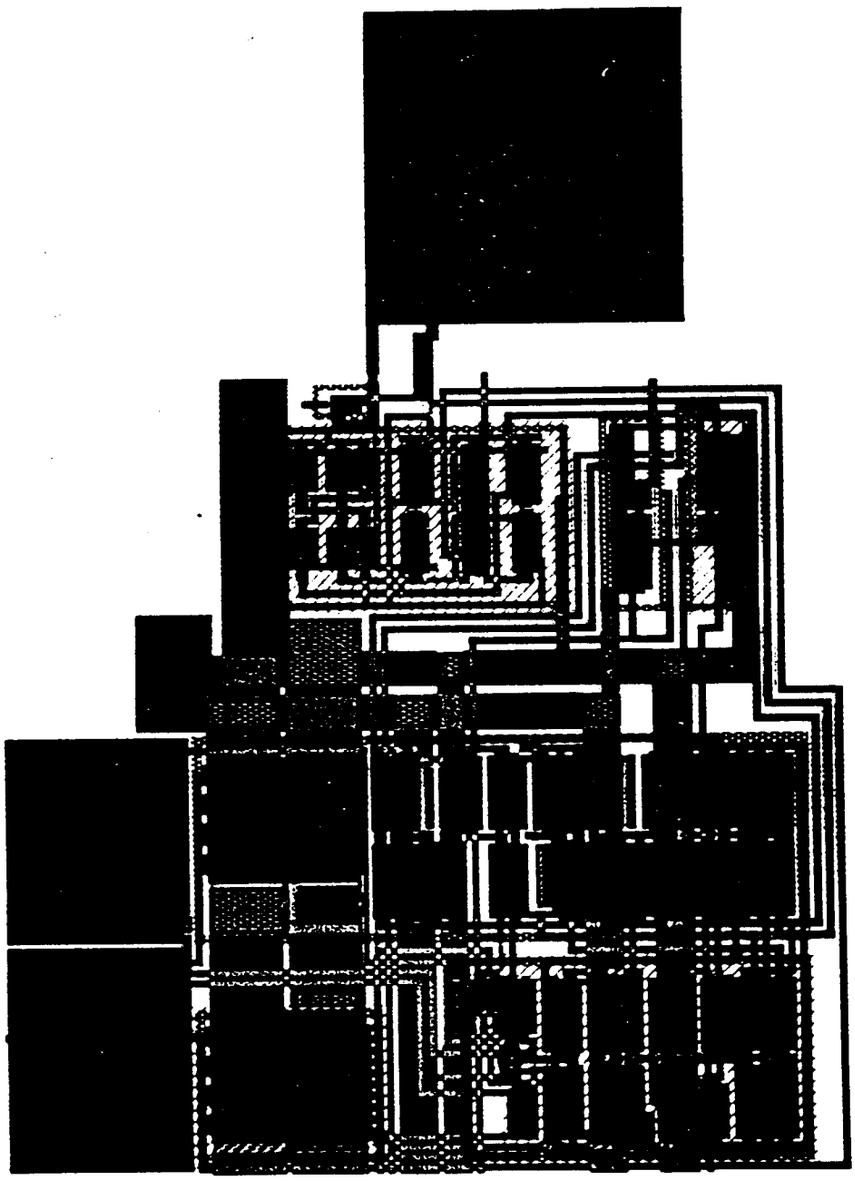


ADC Linearity





RAMP SCHEMATIC
C-CHARGE
C2
5X5
M6
8X8
M3
VOUT
SENSE
REFERENCE
M5
M1
M4
M2
VDD
GND
D
C
B
A
E
RAMP START
RAMP OUTPUT
R-BIAS
M5



```
AMP LINEARITY 25PF 4UA 4.7 -> 0.3 V IN 32 US

>>>> #pts, slope, yintercept
3,-1.631586e+05 4.993798e+00
> x, y, yfit, y-yfit
.761900e-06 4.707960e+00 4.706329e+00 1.631149e-03
.401900e-06 4.603346e+00 4.601907e+00 1.438657e-03
.041900e-06 4.498736e+00 4.497486e+00 1.250165e-03
.681900e-06 4.394130e+00 4.393064e+00 1.065673e-03
.321900e-06 4.289530e+00 4.288643e+00 8.871810e-04
.961900e-06 4.184935e+00 4.184221e+00 7.136889e-04
.601900e-06 4.080345e+00 4.079800e+00 5.451969e-04
.241900e-06 3.975761e+00 3.975378e+00 3.827049e-04
.881900e-06 3.871182e+00 3.870957e+00 2.252128e-04
.521900e-06 3.766610e+00 3.766535e+00 7.472078e-05
.161900e-06 3.662045e+00 3.662114e+00 -6.877126e-05
.801900e-06 3.557487e+00 3.557692e+00 -2.052633e-04
.441900e-06 3.452937e+00 3.453271e+00 -3.337553e-04
.008190e-05 3.348396e+00 3.348849e+00 -4.532474e-04
.072190e-05 3.243864e+00 3.244428e+00 -5.637394e-04
.136190e-05 3.139340e+00 3.140006e+00 -6.662315e-04
.200190e-05 3.034827e+00 3.035585e+00 -7.577235e-04
.264190e-05 2.930324e+00 2.931163e+00 -8.392156e-04
.328190e-05 2.825832e+00 2.826742e+00 -9.097076e-04
.392190e-05 2.721353e+00 2.722320e+00 -9.671996e-04
.456190e-05 2.616887e+00 2.617899e+00 -1.011692e-03
.520190e-05 2.512437e+00 2.513477e+00 -1.040184e-03
..584190e-05 2.408004e+00 2.409056e+00 -1.051676e-03
..648190e-05 2.303586e+00 2.304634e+00 -1.048168e-03
..712190e-05 2.199183e+00 2.200213e+00 -1.029660e-03
..776190e-05 2.094793e+00 2.095791e+00 -9.981519e-04
..840190e-05 1.990415e+00 1.991370e+00 -9.546439e-04
..904190e-05 1.886050e+00 1.886948e+00 -8.981360e-04
..968190e-05 1.781700e+00 1.782527e+00 -8.266280e-04
2.032190e-05 1.677364e+00 1.678105e+00 -7.411201e-04
2.096190e-05 1.573043e+00 1.573684e+00 -6.406121e-04
2.160190e-05 1.468739e+00 1.469262e+00 -5.231041e-04
2.224190e-05 1.364453e+00 1.364841e+00 -3.875962e-04
2.288190e-05 1.260186e+00 1.260419e+00 -2.330882e-04
2.352190e-05 1.155940e+00 1.155998e+00 -5.758026e-05
2.416190e-05 1.051716e+00 1.051576e+00 1.399277e-04
2.480190e-05 9.475158e-01 9.471546e-01 3.612357e-04
2.544190e-05 8.433421e-01 8.427331e-01 6.090436e-04
2.608190e-05 7.391972e-01 7.383115e-01 8.856516e-04
2.672190e-05 6.350839e-01 6.338900e-01 1.193860e-03
2.736190e-05 5.310056e-01 5.294685e-01 1.537067e-03
2.800190e-05 4.269666e-01 4.250470e-01 1.919575e-03
2.864190e-05 3.229717e-01 3.206255e-01 2.346183e-03
```

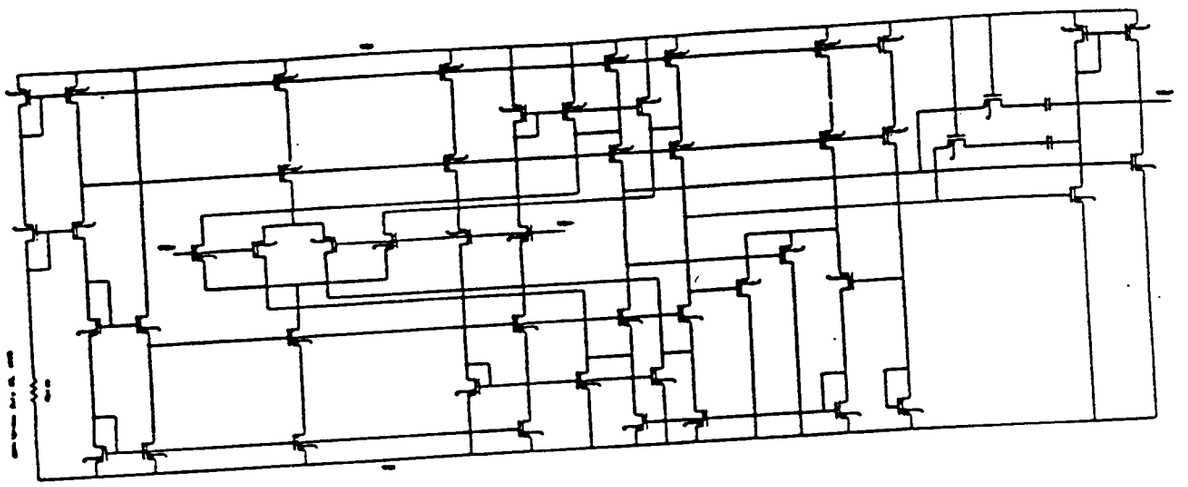
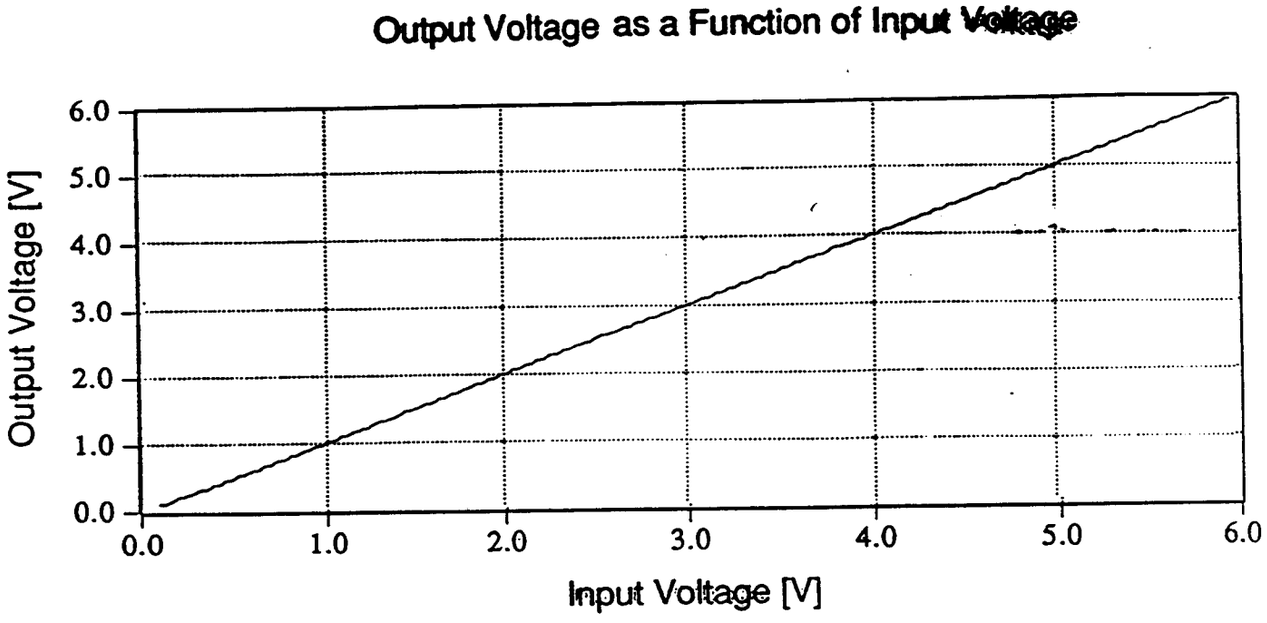


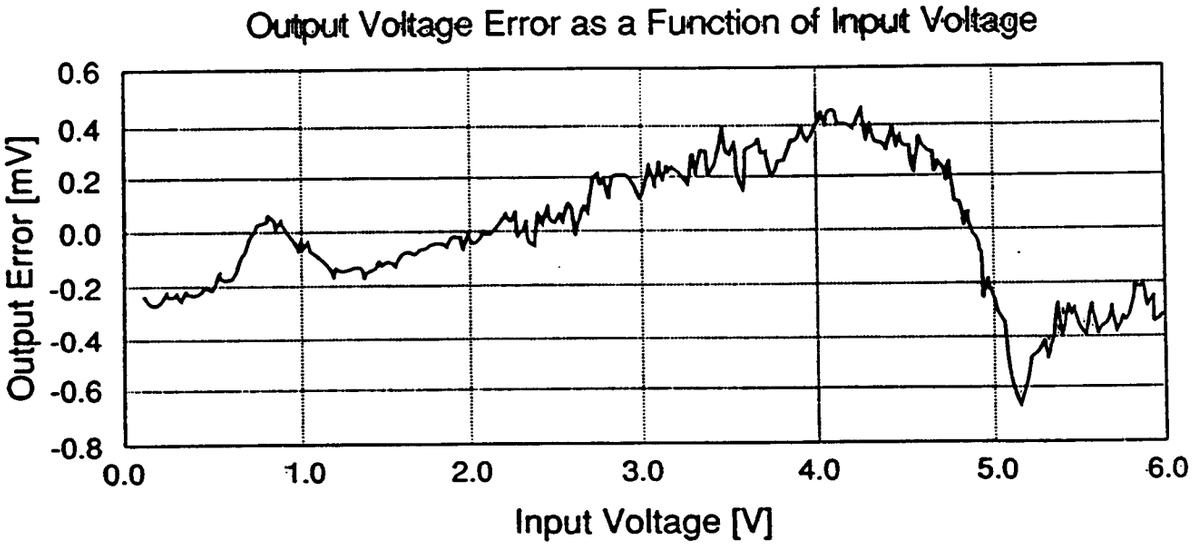
Figure 28: Rail to Rail Folded Cascode Op Amp Schematic

Op Amp Parameters	Performance
Offset voltage	$\pm 1.5mV$ (rms)
max. deviation from linearity	$< 3.0mV$
noise voltage	$150nV/\sqrt{Hz}$
Calc. gain bandwidth (unloaded)	250 MHz
Gain bandwidth (compensated)	2.8 MHz
Max. load capacitance	$< 1000pF$
power consumption/channel	2 mW
settling time (0.02%)	$4\mu seconds$
open loop gain	120 db
slew rate	$2.5V/\mu second$

Table 5: Achieved performance parameters for a new rail-to-rail operational amplifier for the switched capacitor array readout reconstruction.

Op-Amp Linearity





COMPARATOR

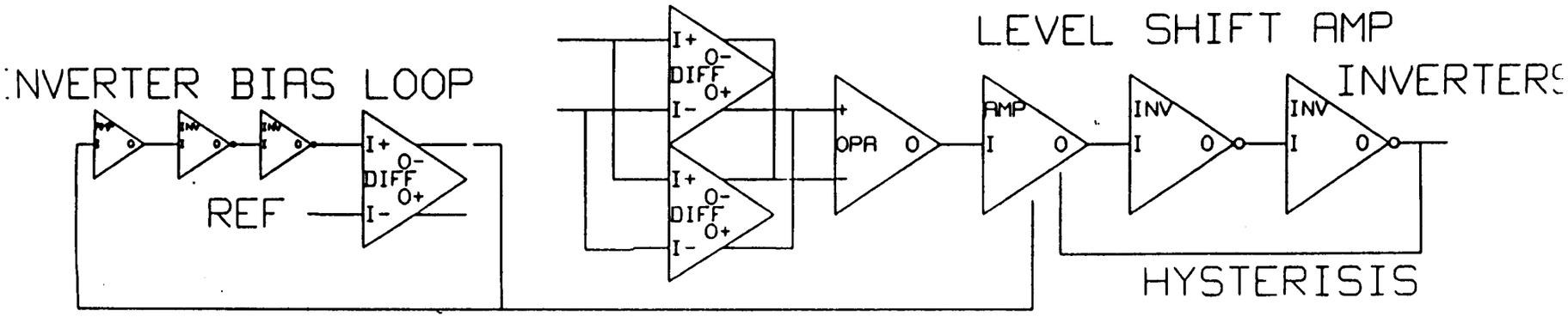
RAIL TO RAIL V->I

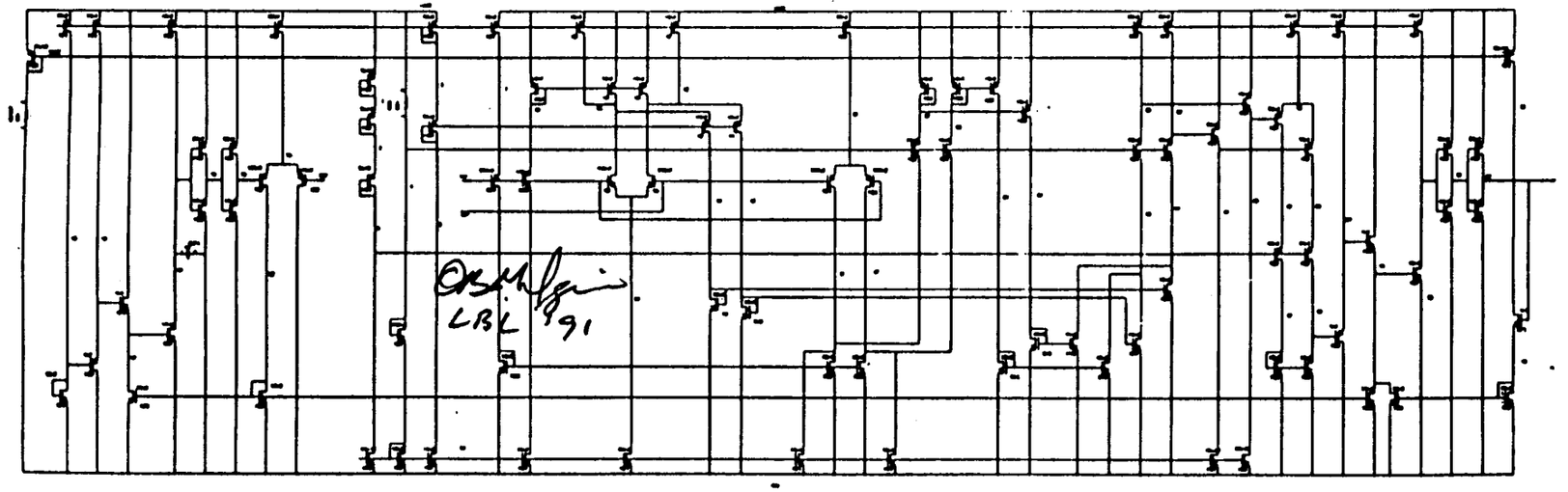
SUMMING AMP

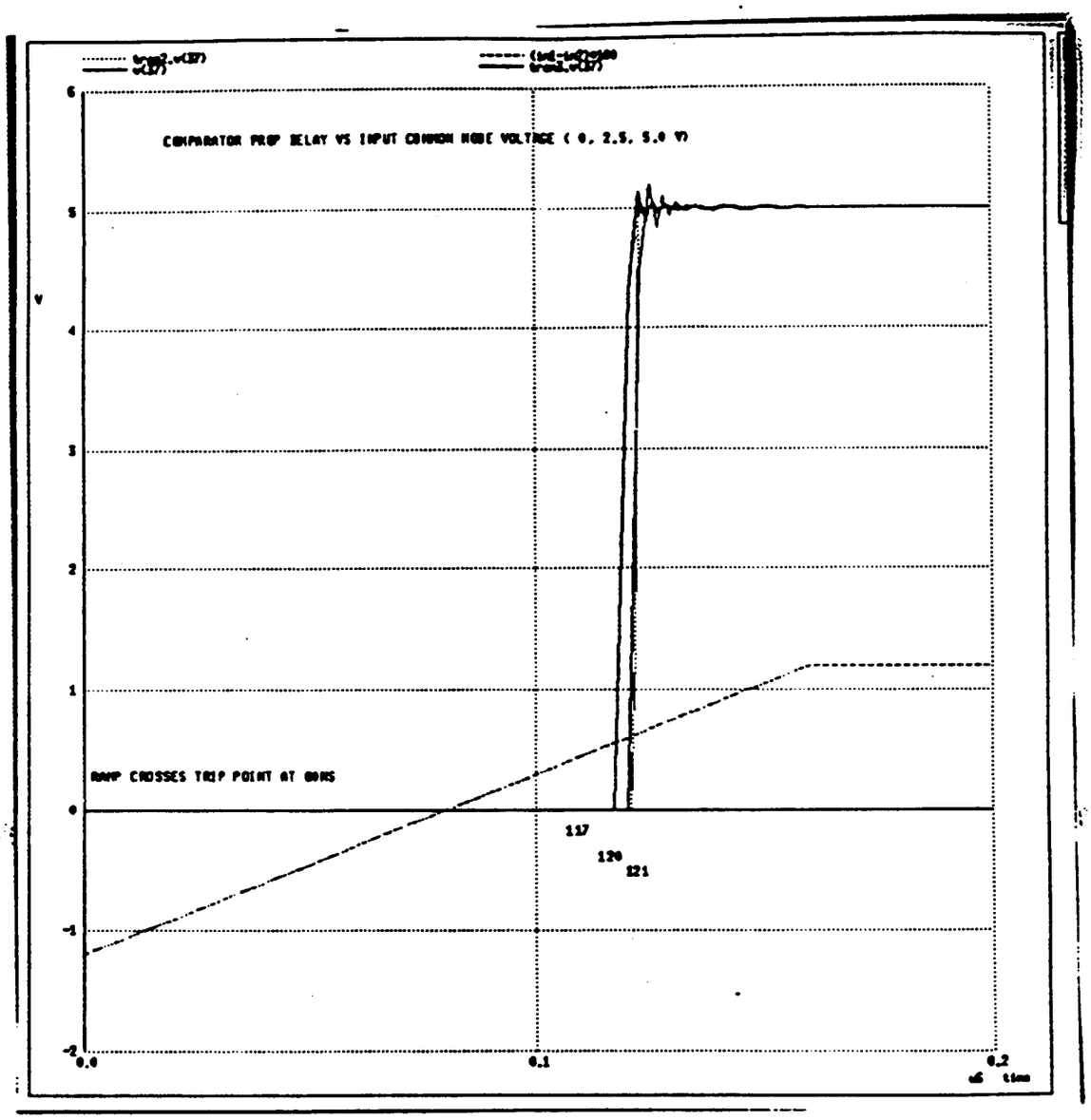
LEVEL SHIFT AMP

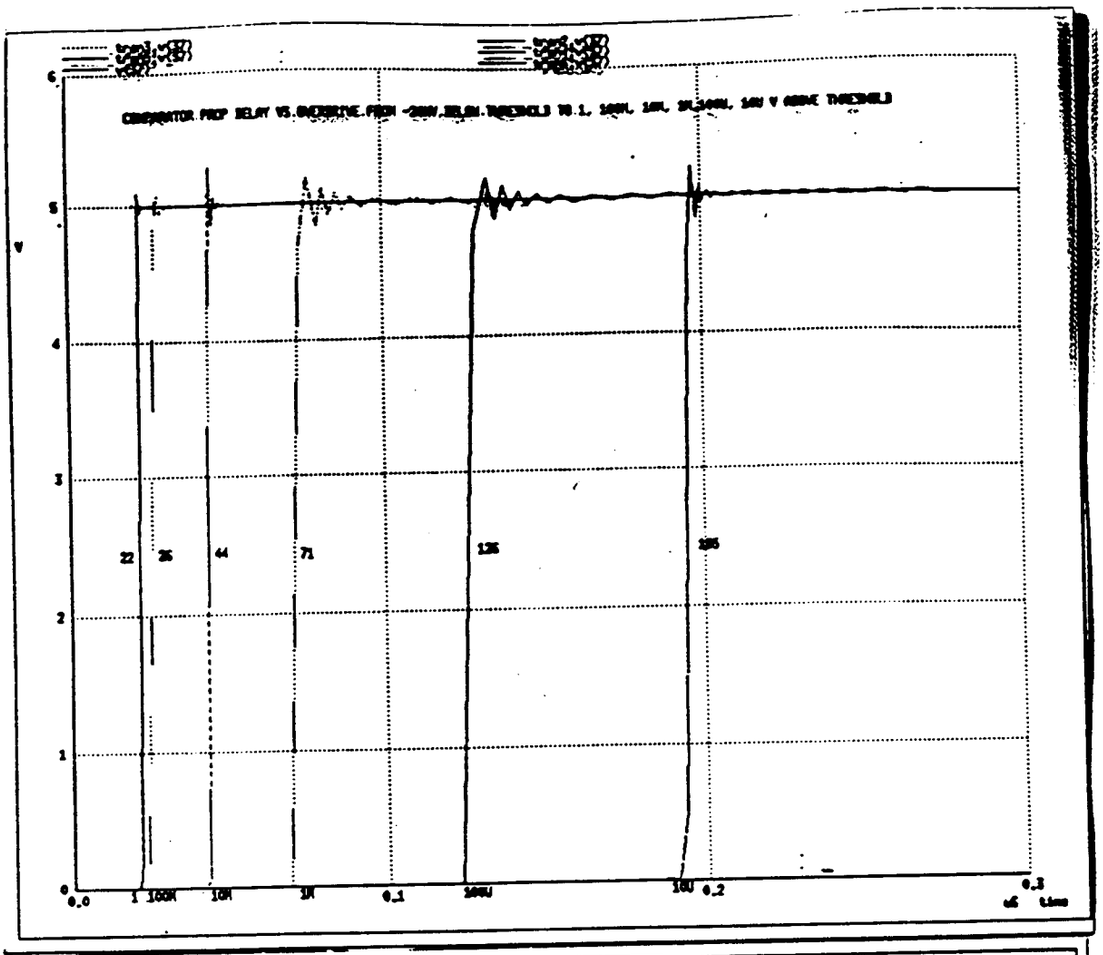
INVERTER BIAS LOOP

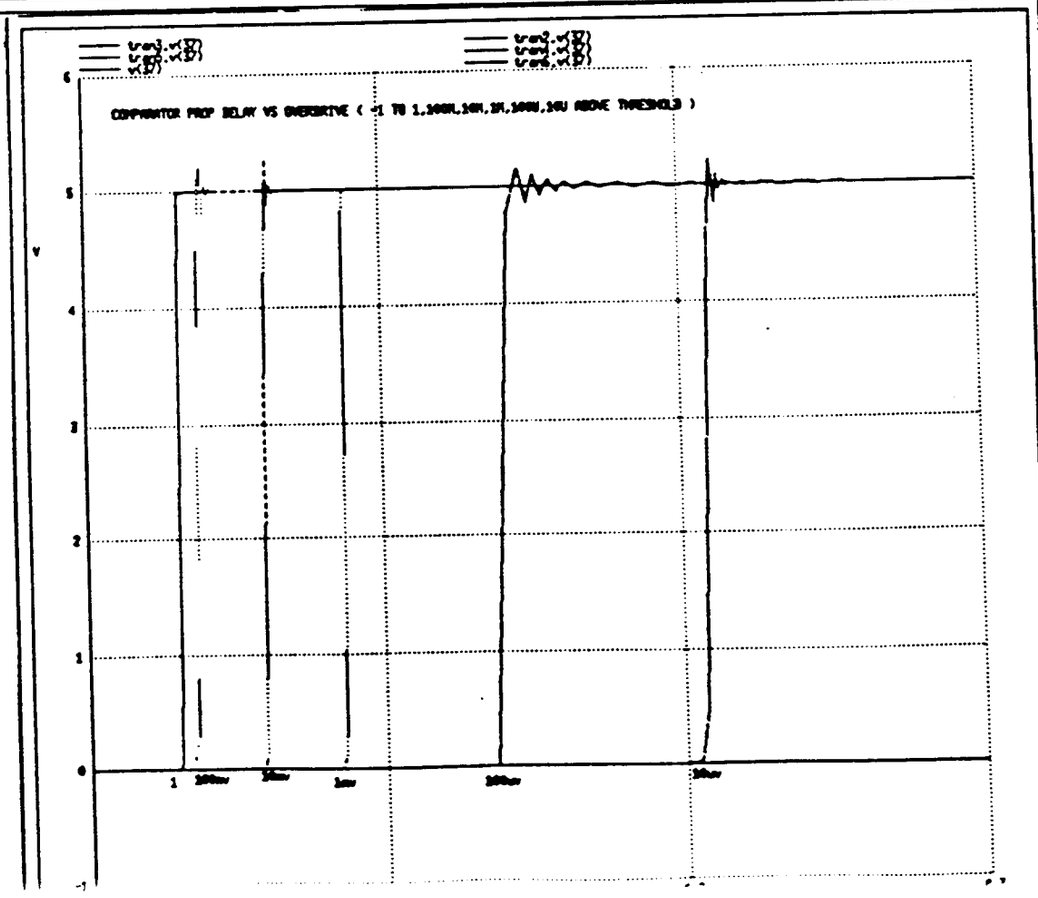
INVERTERS

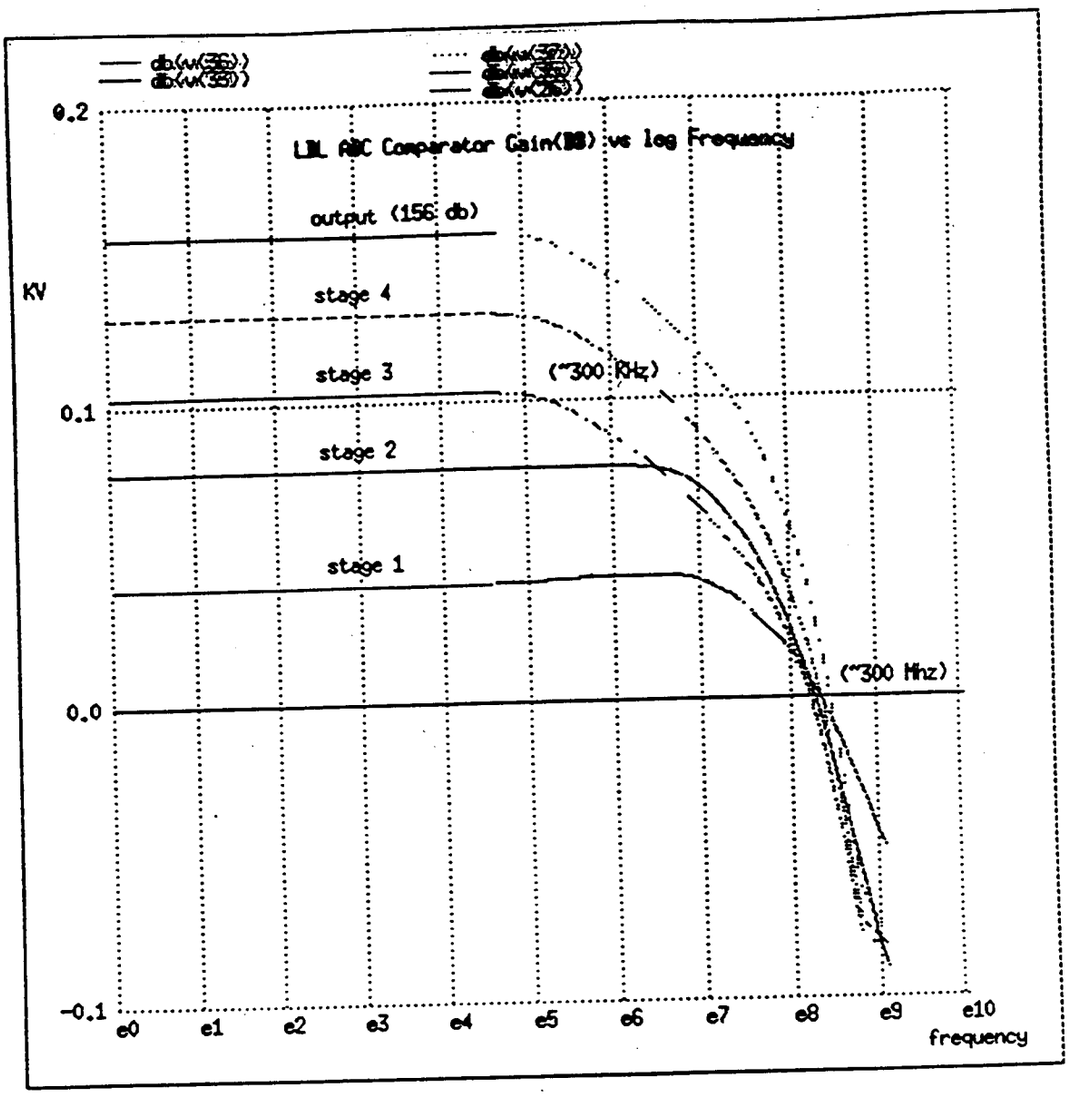





COMPARATOR PROP DELAY VS INPUT COMMON MODE VOLTAGE (0, 2.5, 5.0 V)
V
6
5
4
3
2
1
0
-1
-2
0.0
0.1
0.2
RAMP CROSSES TRIP POINT AT 00NS
117
120
121

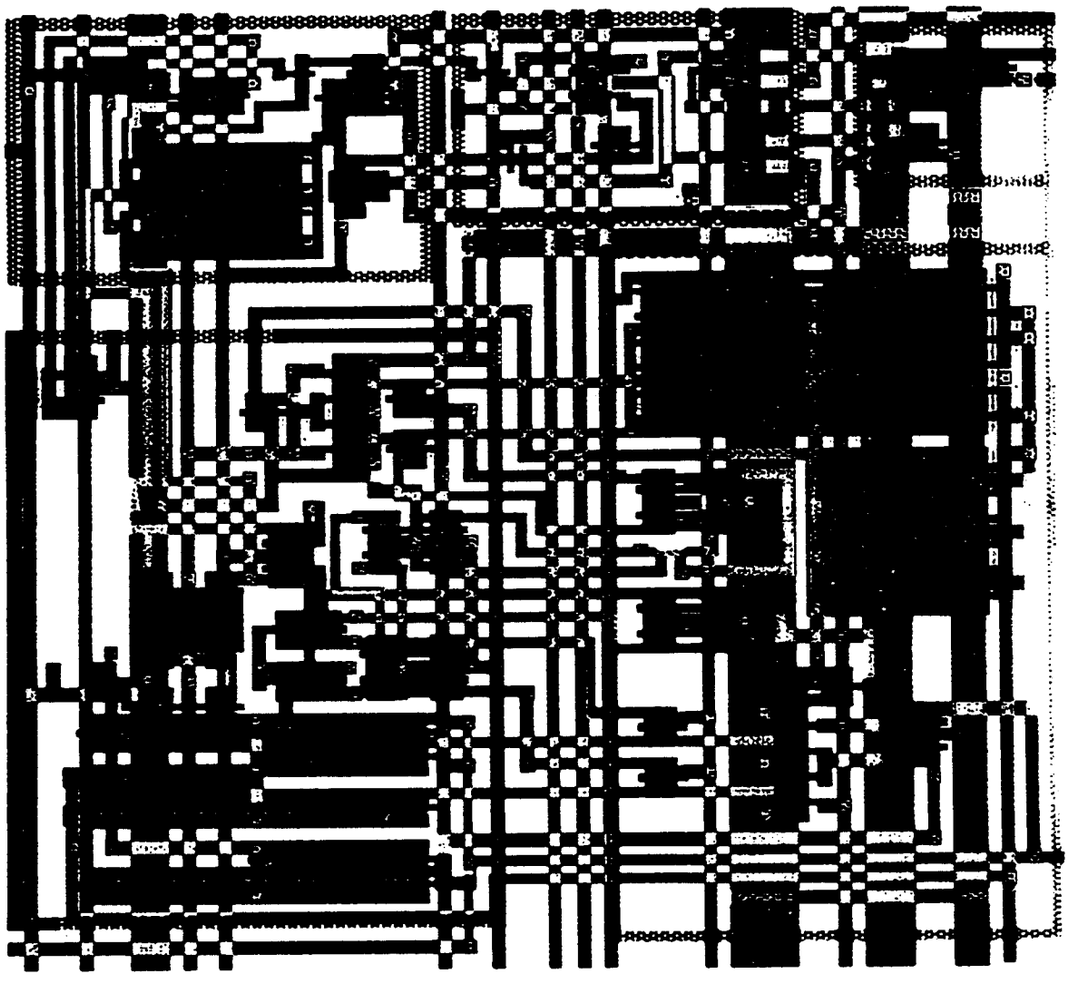

V
6
5
4
3
2
1
0
22
35
44
71
135
195
0.0
1
100N
10N
1N
0.1
100U
10U
0.2
0.3

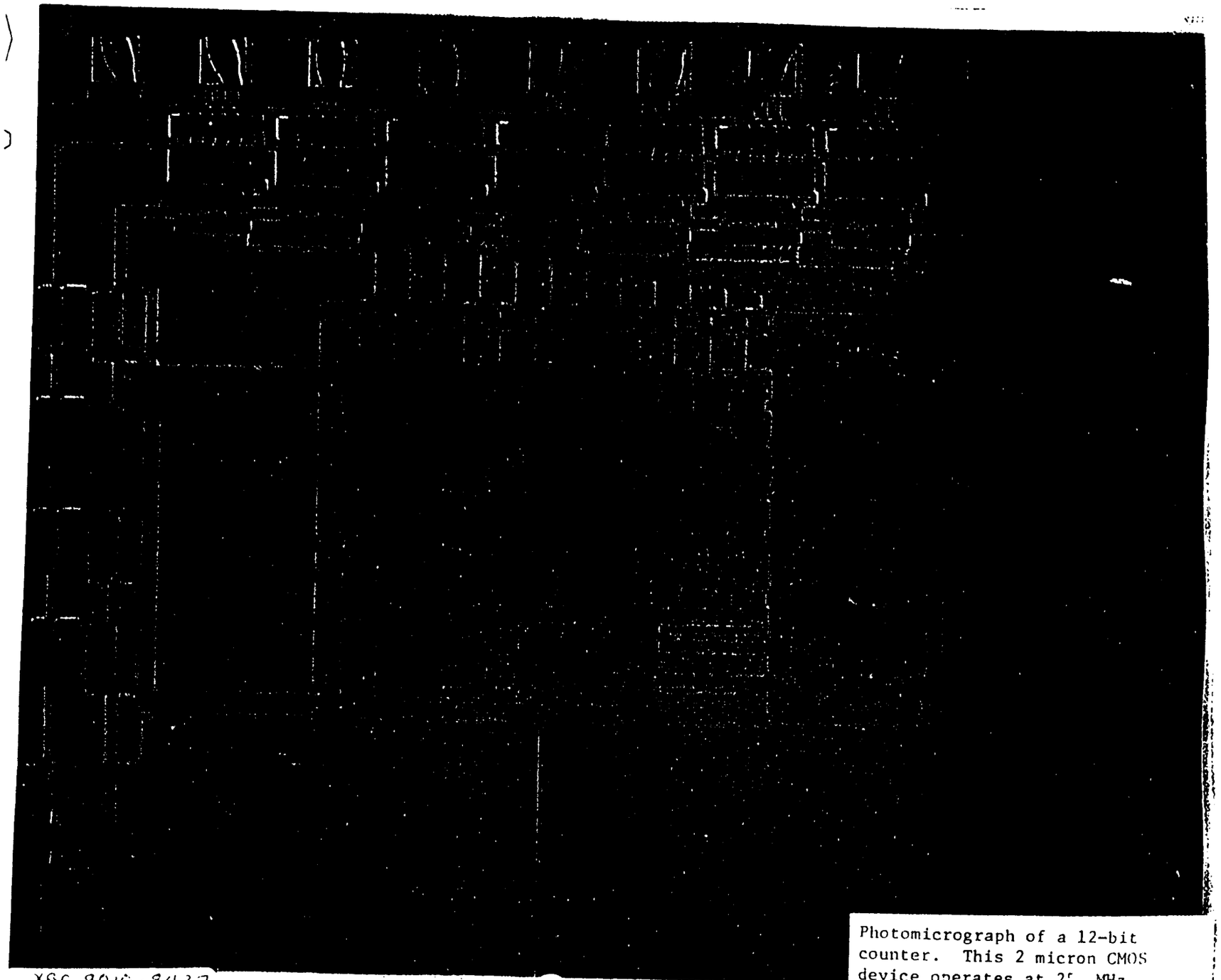

V
6
5
4
3
2
1
0
-1
1
1m
100m



COMPARATOR GAIN-BANDWIDTH = 300 MHz

DC OPEN LOOP = 65×10^6



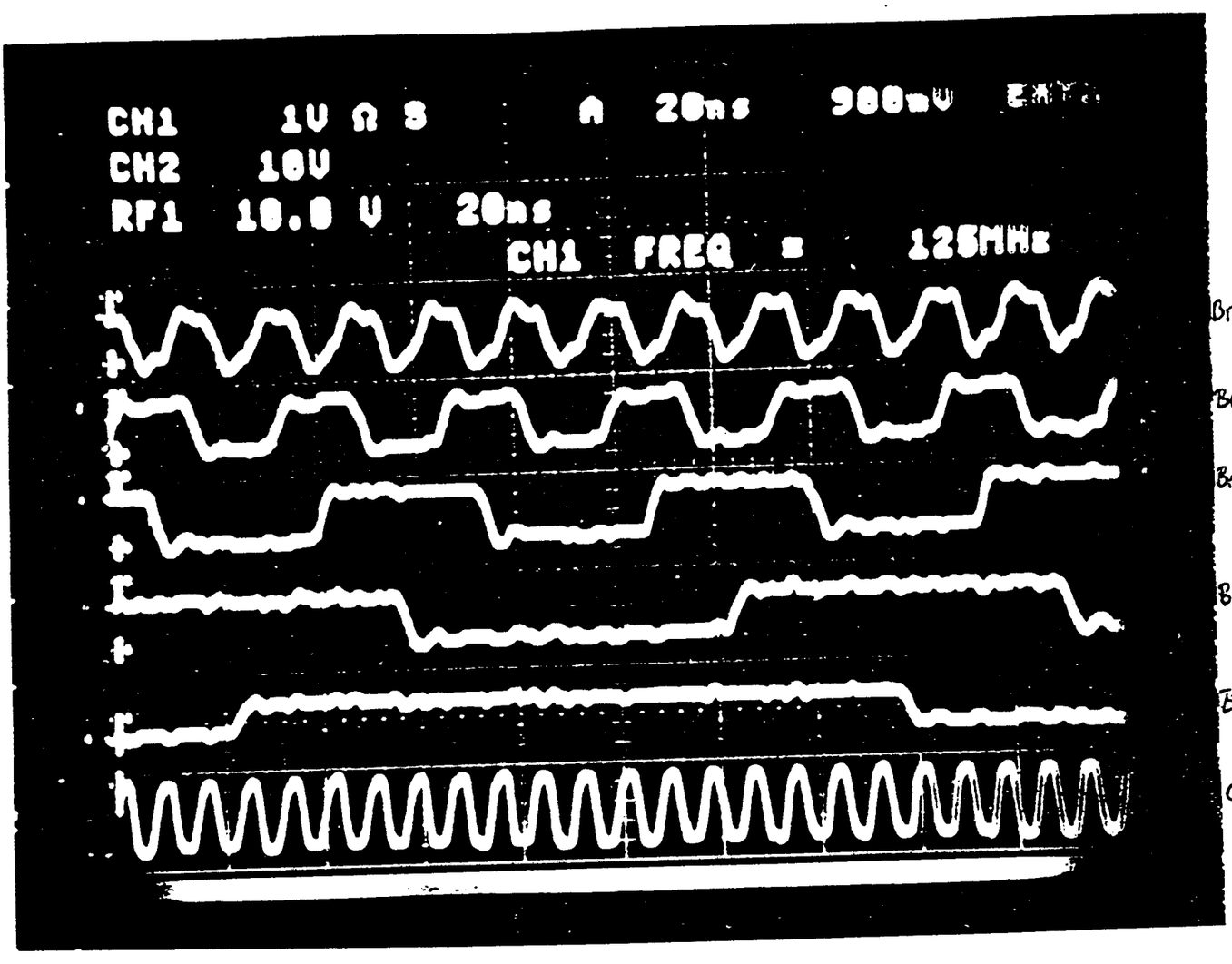


XBC 9010-8427

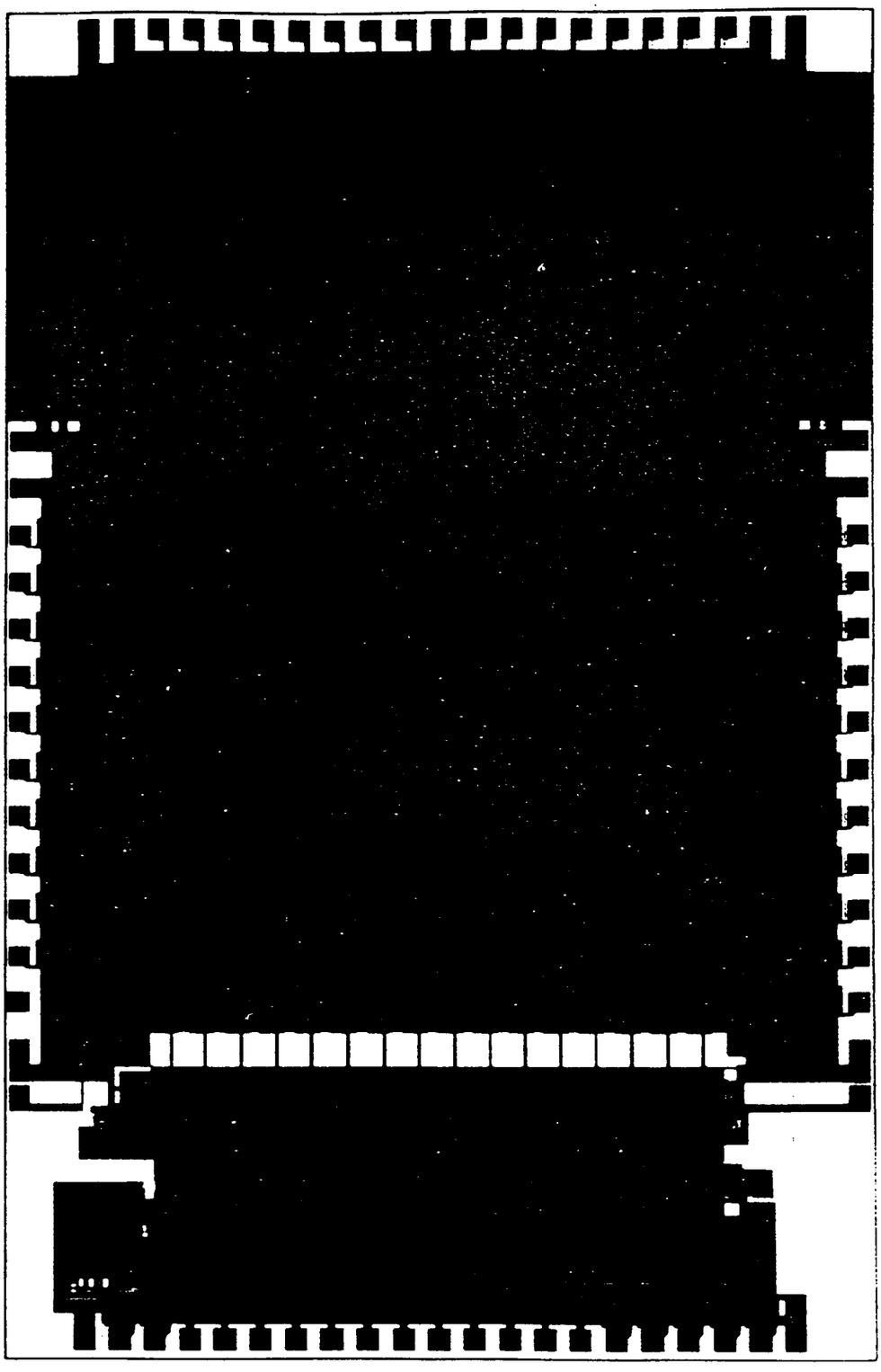
Photomicrograph of a 12-bit counter. This 2 micron CMOS device operates at 2[illegible] MHz.

```
RSIM simulation of GRAY CODE COUNTER

*** RSIM Version 6.1 ***
150 nodes, transistors: n-channel=144 p-channel=175
data=0XXXXXXXXXXX cout=000000000000 rb=0 phi1=0  -----
time = 100.0ns
data=000000000000 cout=X00000000000 rb=0 phi1=1  RESET
time = 200.0ns
data=000000000000 cout=000000000000 rb=0 phi1=0  -----
time = 300.0ns
data=000000000000 cout=100000000000 rb=1 phi1=1  COUNT
time = 400.0ns
data=000000000000 cout=110000000000 rb=1 phi1=0
time = 500.0ns
data=000000000000 cout=010000000000 rb=1 phi1=1
time = 600.0ns
data=000000000000 cout=011000000000 rb=1 phi1=0
time = 700.0ns
data=100000000000 cout=111000000000 rb=1 phi1=1
time = 800.0ns
data=110000000000 cout=101000000000 rb=1 phi1=0
time = 900.0ns
data=010000000000 cout=001000000000 rb=1 phi1=1
time = 1000.0ns
data=011000000000 cout=001100000000 rb=1 phi1=0
time = 1100.0ns
data=111000000000 cout=101100000000 rb=1 phi1=1
time = 1200.0ns
data=101000000000 cout=111100000000 rb=1 phi1=0
```



125 MHz INPUT CLOCK, BIT COUNTS ON EVERY CLOCK EDGE



[redacted]

SPEC	ADC601	ADC603	ADC80	[redacted]
TYPE	SAR	FLASH	SAR	COUNTER
BITS	12	12	12	12
RATE	100NS	1US	25US	32US
POWER	6W	1.5W	500MW	
COST	1045	95	50	
/CHANNEL				
POWER	20MW	60MW	500MW	5MW
COST	4.00	3.80	50.00	0.50
/BOARD				
CHIPS	1	10	256	0

Overall Calorimeter System Design/Costs

R. Jared (LBL)

SCINTILLATING TILE BARREL AND ENDCAP CALORIMETER ELECTRONIC COST ESTIMATE

Robert Ely, Jack Frank, Richard C. Jared, Issy Kipnis,
Frederick Kirsten, Stuart Kleinfelder
Michael Levi, Thomas Merrick, Oren Milgrome,
Robert Minor, Leverett Pope, Paul Salz,
Edward Theil and Jack Zelver

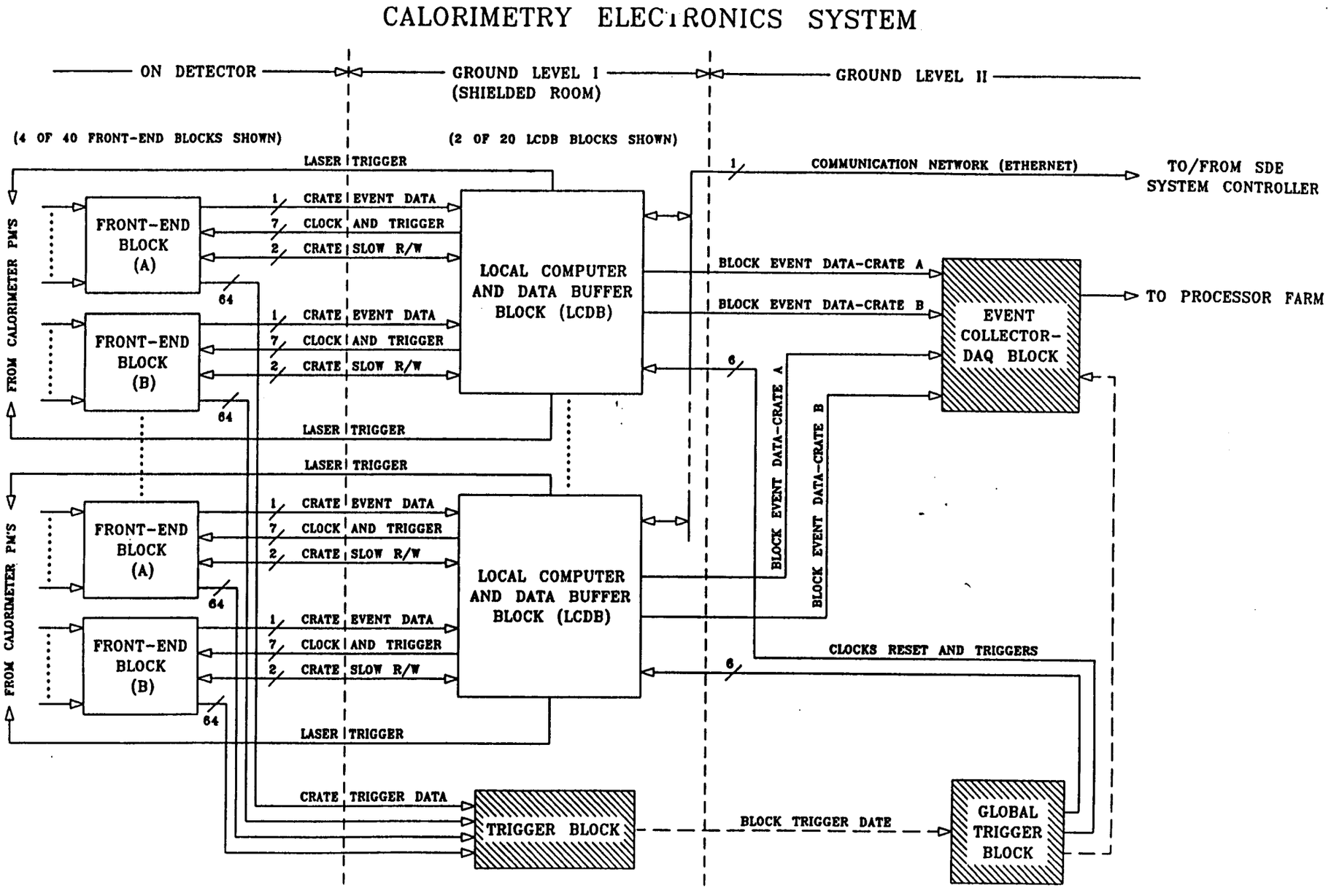

CALORIMETRY ELECTRONICS SYSTEM
ON DETECTOR
GROUND LEVEL I
(SHIELDED ROOM)
GROUND LEVEL II
(4 OF 40 FRONT-END BLOCKS SHOWN)
(2 OF 20 LCDB BLOCKS SHOWN)
LASER TRIGGER
FROM CALORIMETER PM'S
FRONT-END BLOCK (A)
FRONT-END BLOCK (B)
1 CRATE EVENT DATA
7 CLOCK AND TRIGGER
2 CRATE SLOW R/W
64
LOCAL COMPUTER AND DATA BUFFER BLOCK (LCDB)
1 COMMUNICATION NETWORK (ETHERNET)
TO/FROM SDE SYSTEM CONTROLLER
BLOCK EVENT DATA-CRATE A
BLOCK EVENT DATA-CRATE B
EVENT COLLECTOR-DAQ BLOCK
TO PROCESSOR FARM
6
BLOCK EVENT DATA-CRATE A
BLOCK EVENT DATA-CRATE B
CLOCKS RESET AND TRIGGERS
CRATE TRIGGER DATA
TRIGGER BLOCK
BLOCK TRIGGER DATE
GLOBAL TRIGGER BLOCK

Figure 4.1

FRONT END BLOCKS FOR CALORIMETER
(1 OF 40 CRATES SHOWN)

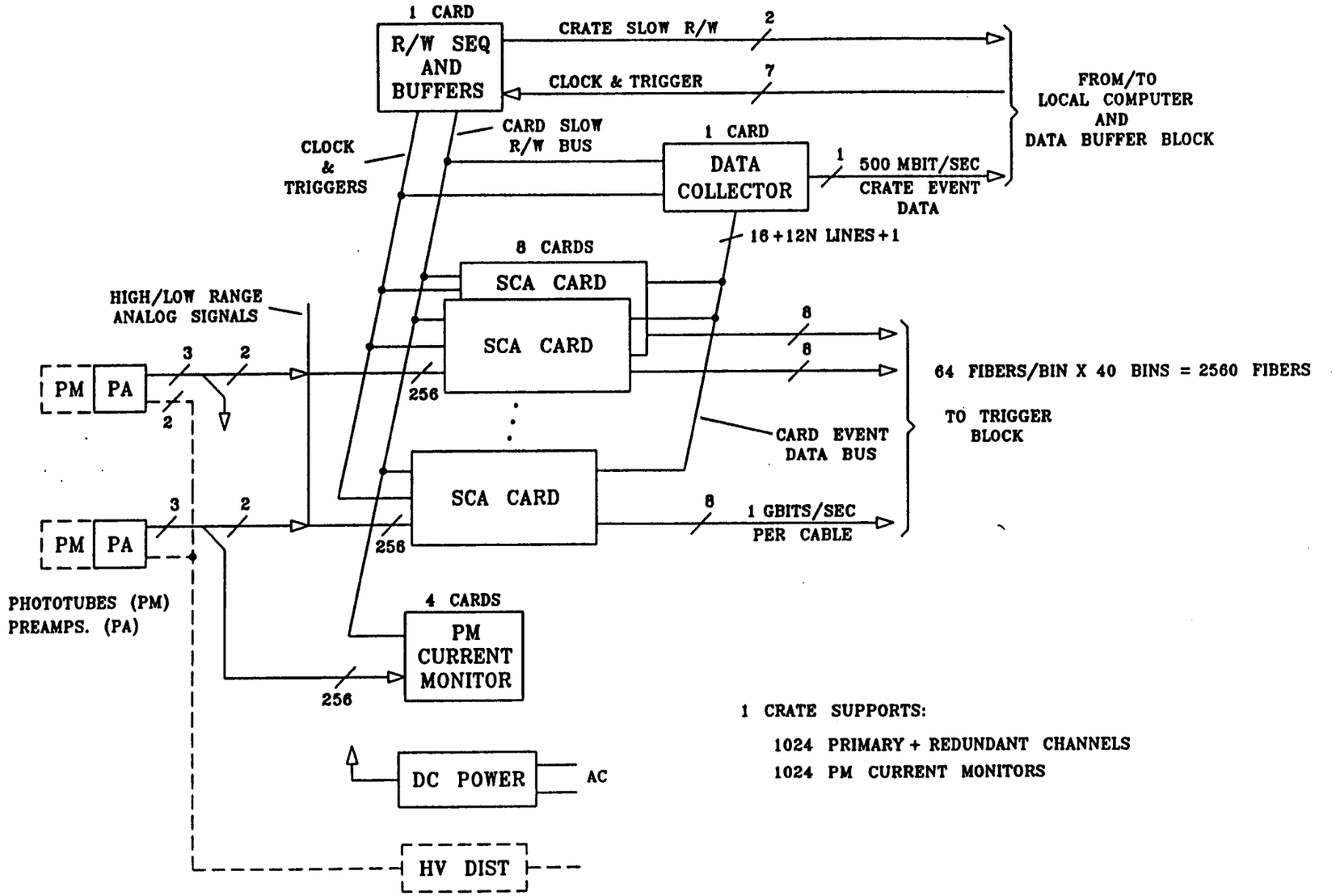


Figure 4.3

PHOTOMULTIPLIER AND PREAMPLIFIER CARD

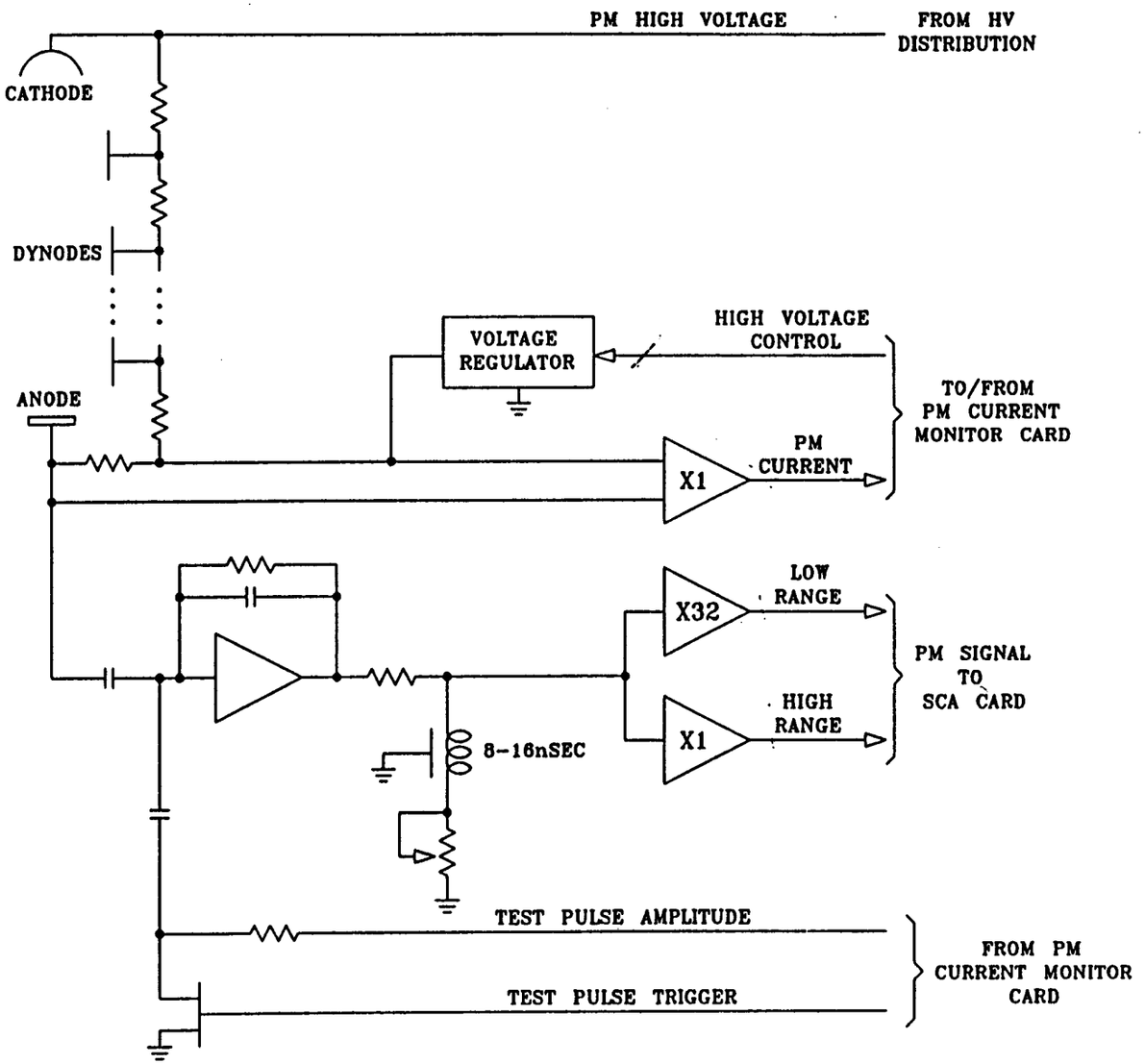


Figure 4.4

SCA CARD

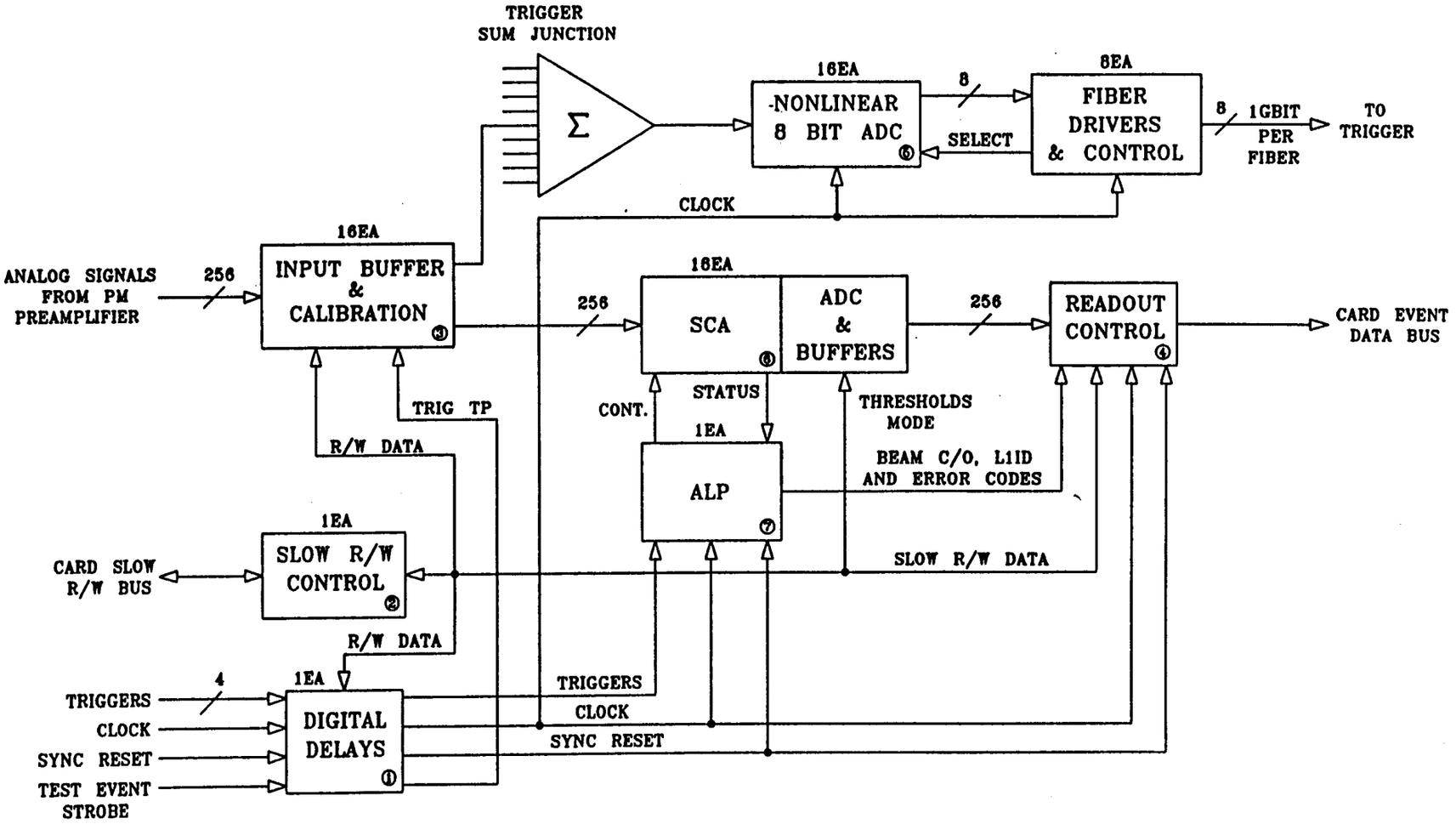


Figure 4.6

PM CURRENT MONITOR CARD

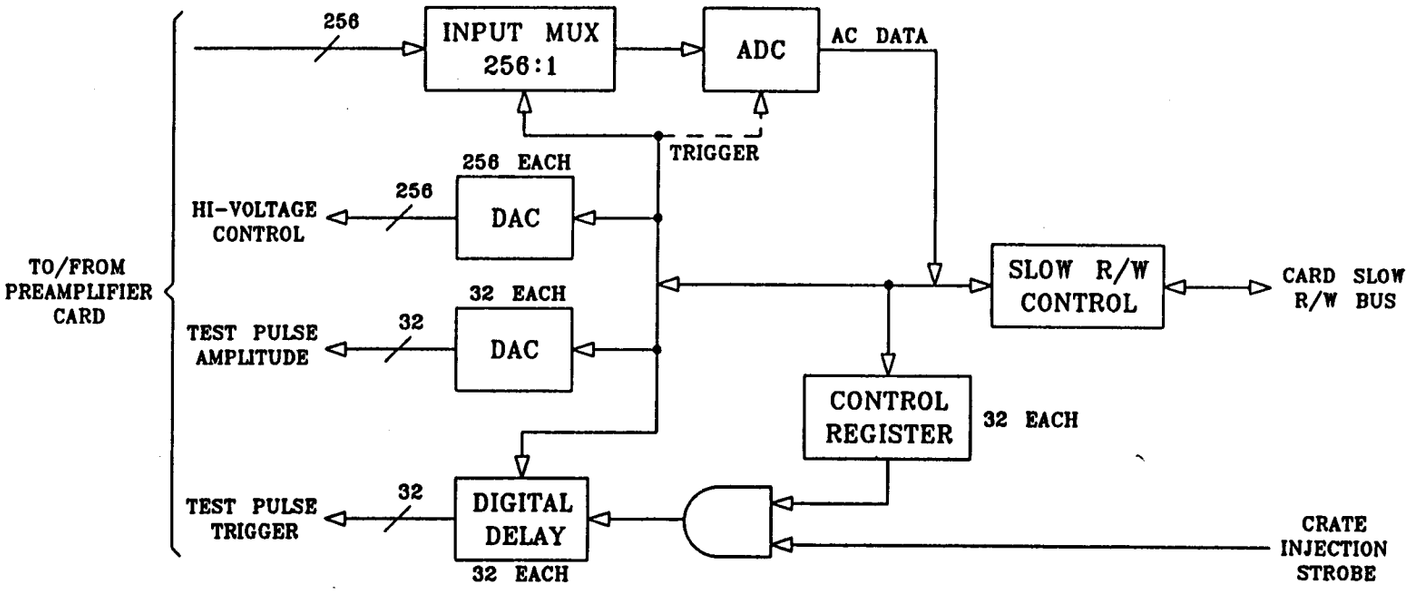


Figure 4.7

DATA COLLECTOR CARD

ALL PERT DATA (3 + (259)8)16 = 33K BITS
NORMAL EVENT (3 + (259)8)16X.1 = 3.3K BITS

3 X ALL PERTINATE DATA 3 X 33K BITS/SEC X 10^4 = 990M BITS/SEC
NOMINAL DATA RATE 3.3K BITS/SEC X 10^4 = 33M BITS/SEC

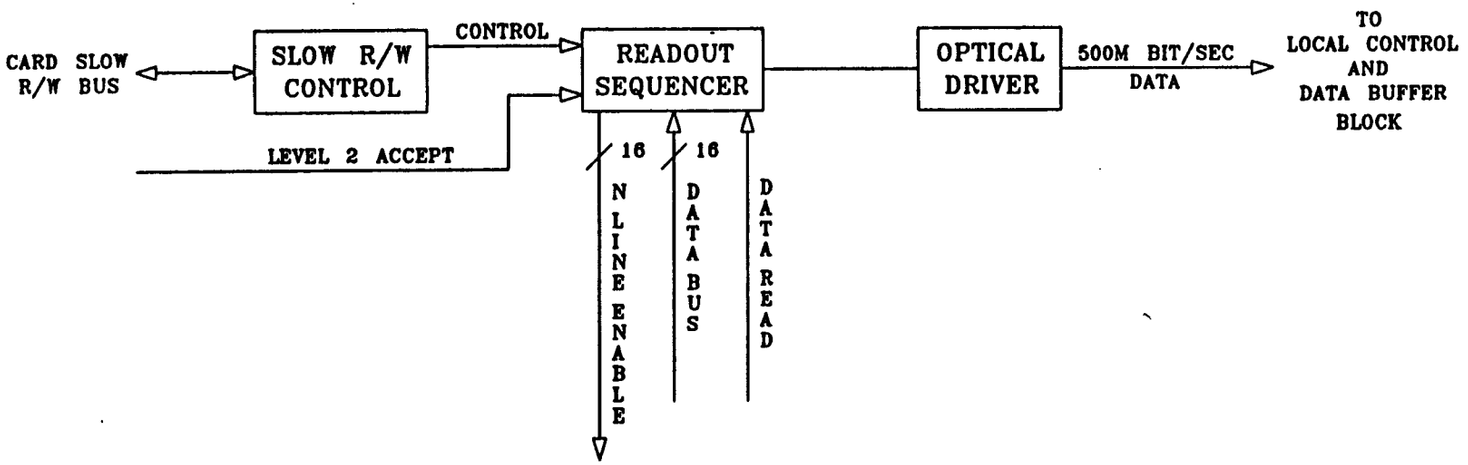


Figure 4.8

R/W SEQUENCER CARD

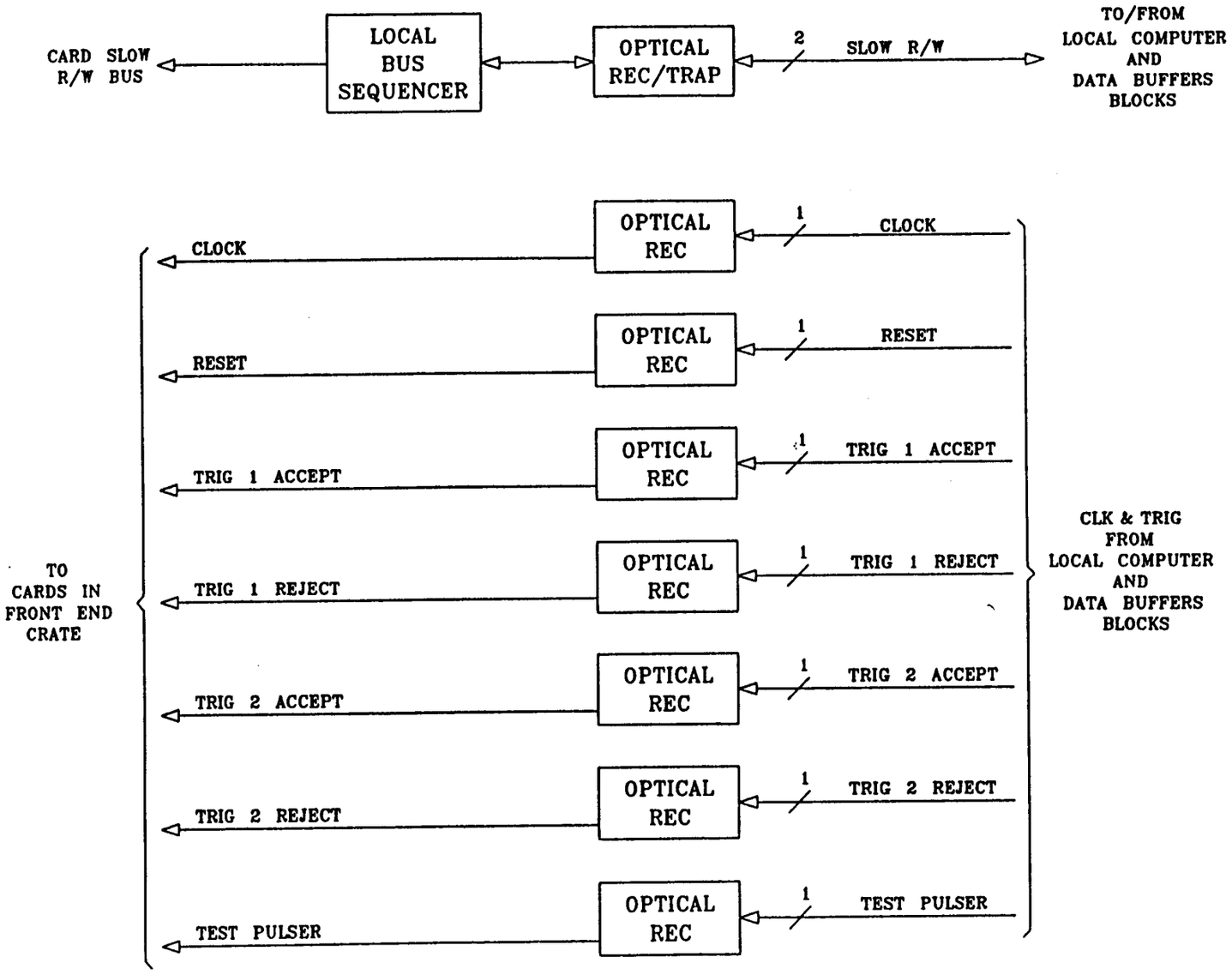


Figure 4.9

LOCAL COMPUTER AND DATA BUFFER (LCDB BLOCKS)

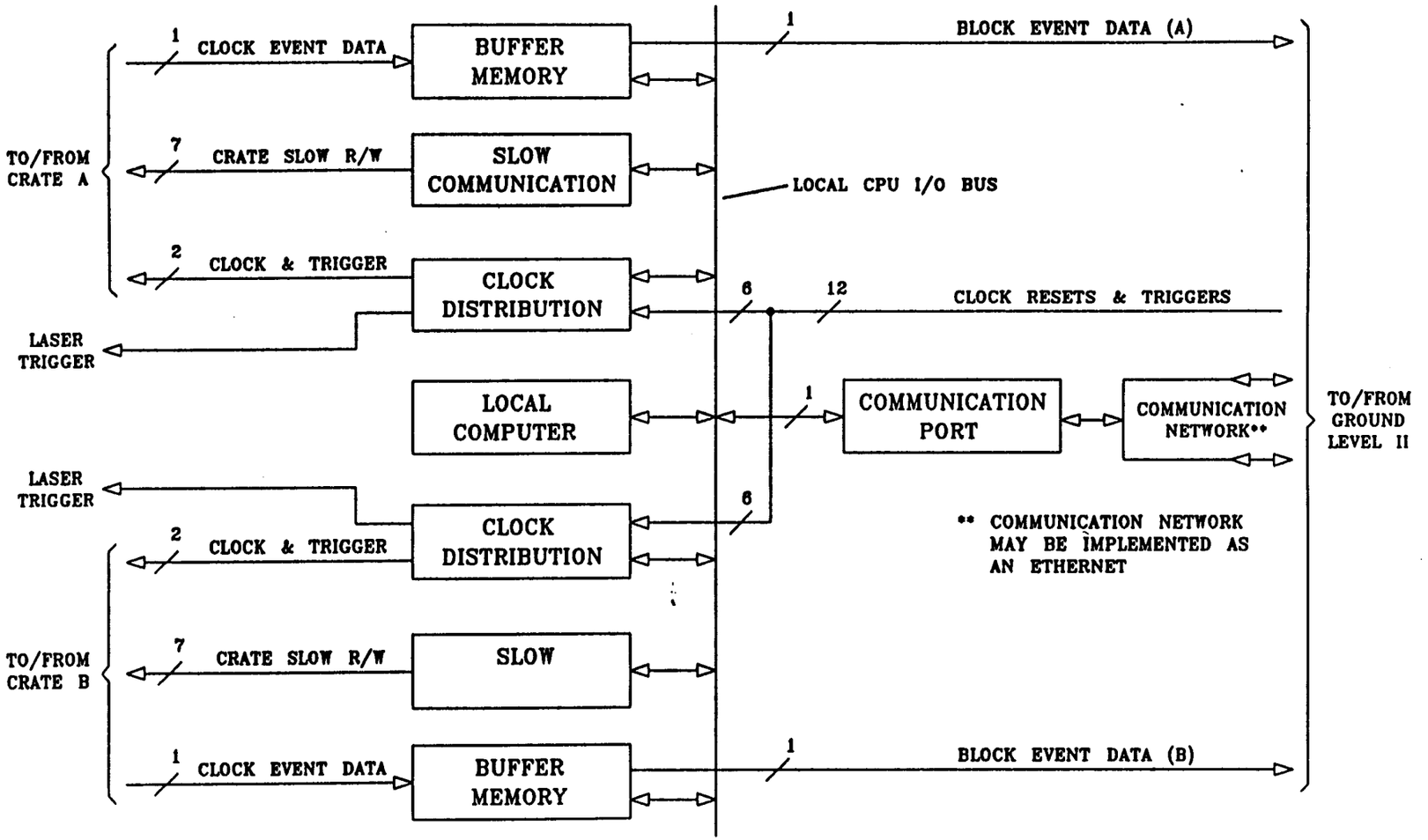
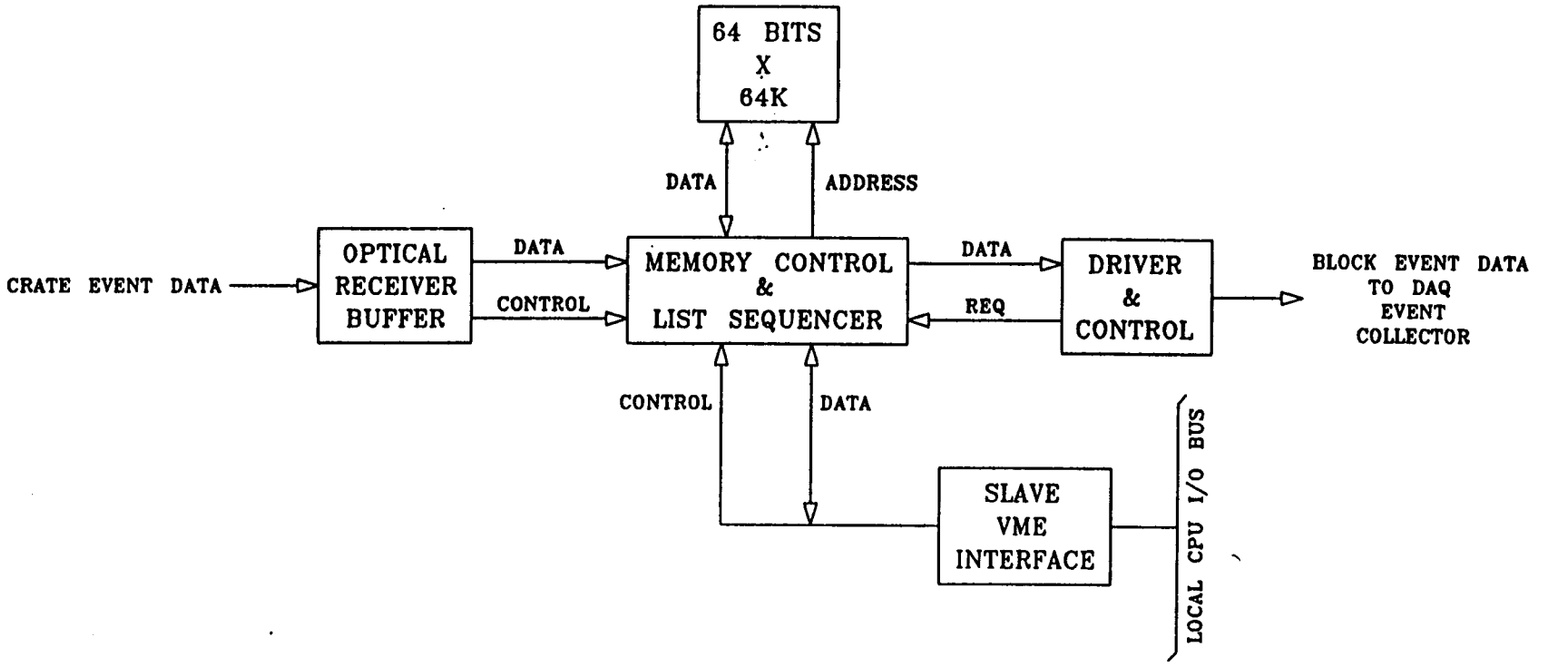


Figure 4.10a

BUFFER MEMORY CARD



SLAVE VME INTERFACE CONTROLS MODES OF DATA FLOW:

A. NORMAL, INPUT DATA IS DERANDOMIZED AND TRANSMITTED TO DAQ.

B. NORMAL DATA FLOW AND CAN PASSIVELY TRAP AN EVENT

C. ACCEPT AND STORE DATA ONLY.

D. LOAD FROM VME EVENT TO BE TRANSFERRED TO DAQ.

Figure 4.10b

CLOCK DISTRIBUTION
AND LOCAL CONTROL FOR TESTING CARD

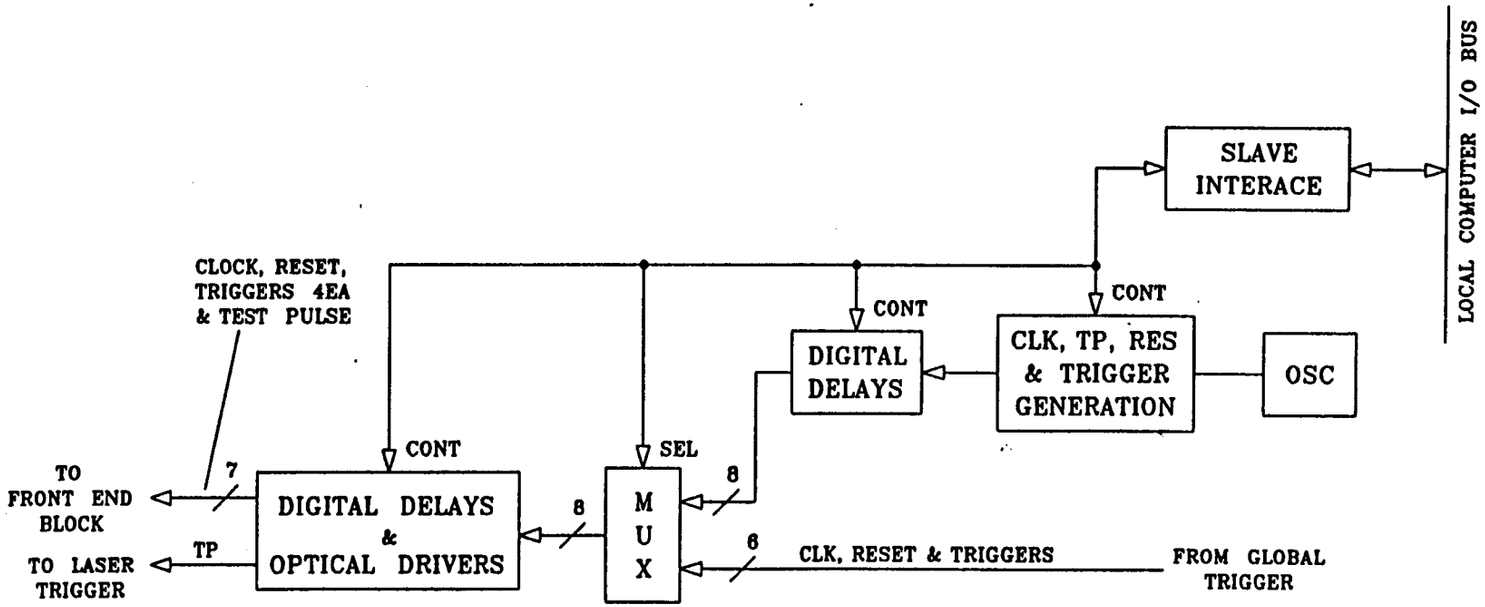


Figure 4.10c

SLOW R/W CARD

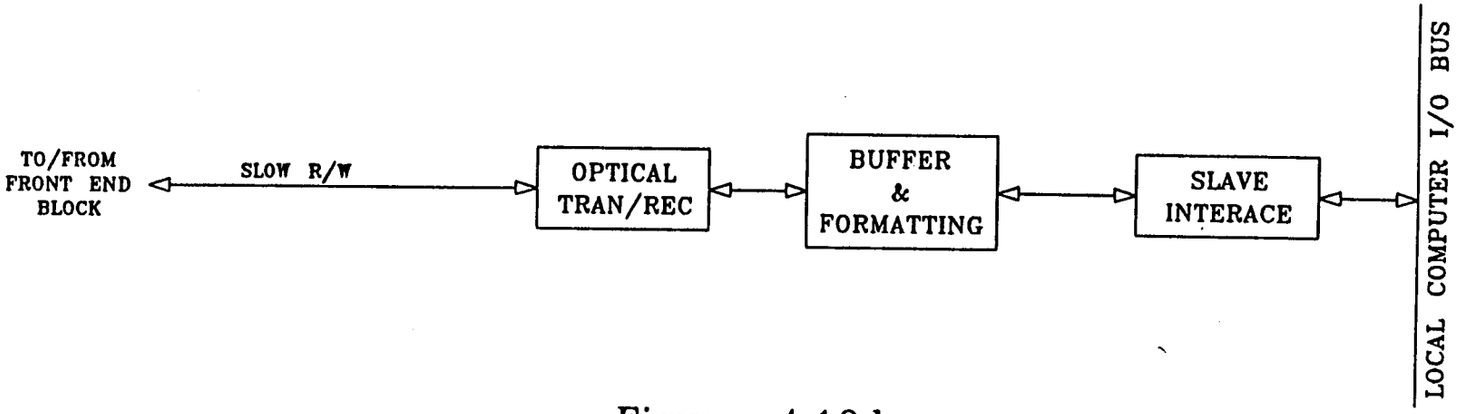


Figure 4.10d

LEVEL 1 SCHEDULE WITH MAJOR MILESTONES

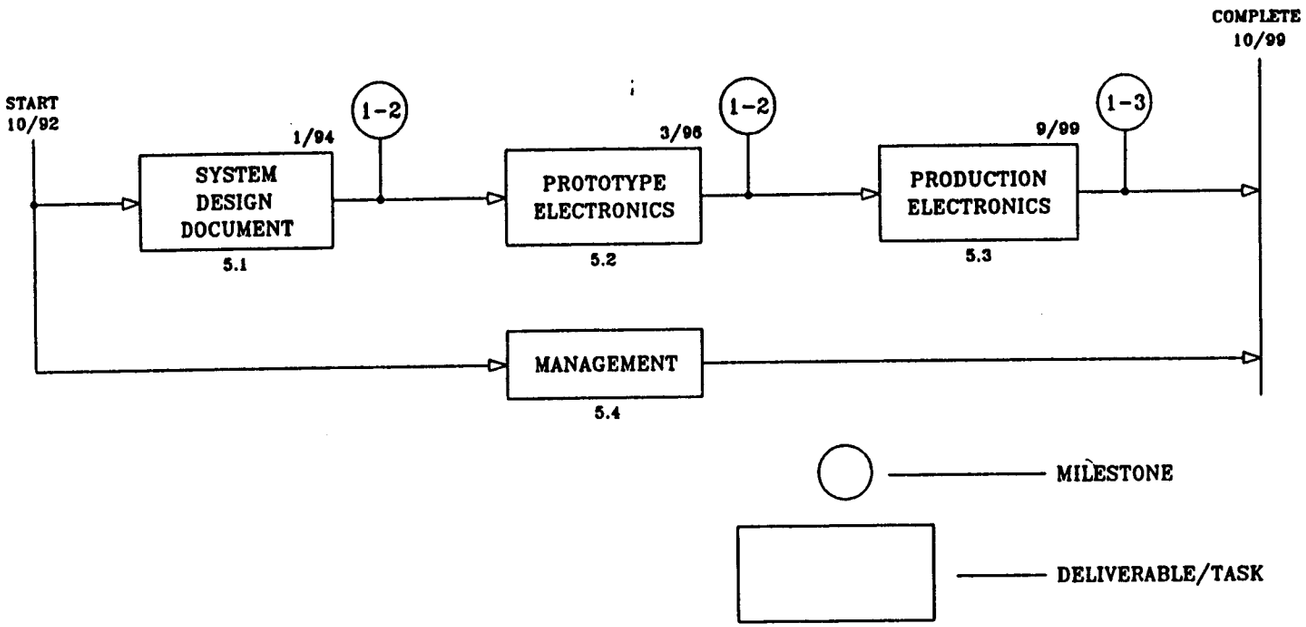


Figure 7.1a

LEVEL 2 SCHEDULE WITH MAJOR AND MINOR MILESTONES

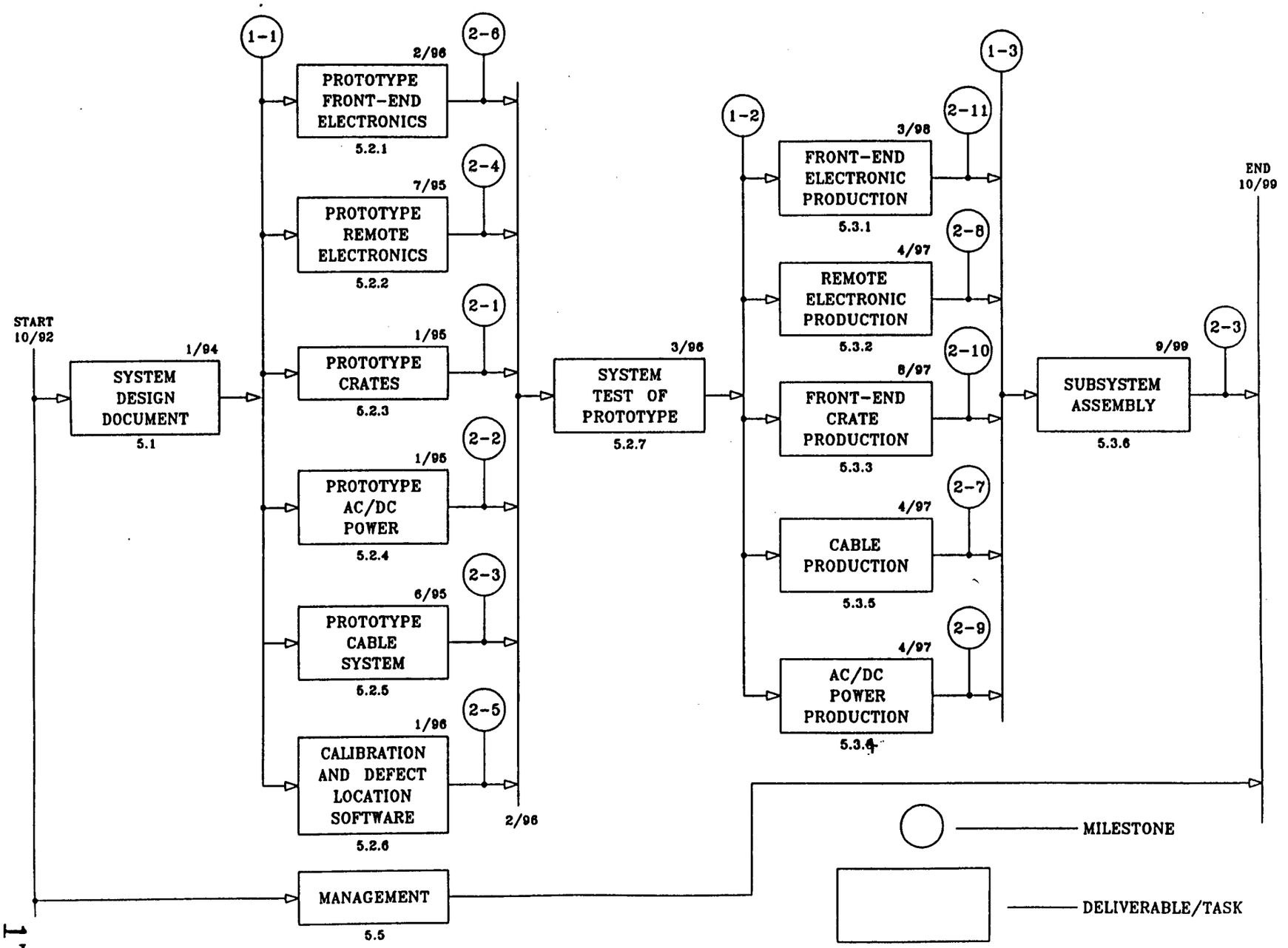


Figure 7.1b

Gated Integrator ASIC for All Digital Readout

W.Foster

WHY YOU WANT AN ALL-DIGITAL

PHOTOTUBE READOUT SYSTEM

(Bill Foster May '91)

Main Selling Points:

- Get out of Analog ASAP
- Minimize Parts Count (R&D $$)
- Simplest Cabling and Ground
- Same Readout for Trigger & DAQ ... & SIMPLER!
- 100% Testability Before Beam
- Digital Collaborations Work Better than Analog Collaborations

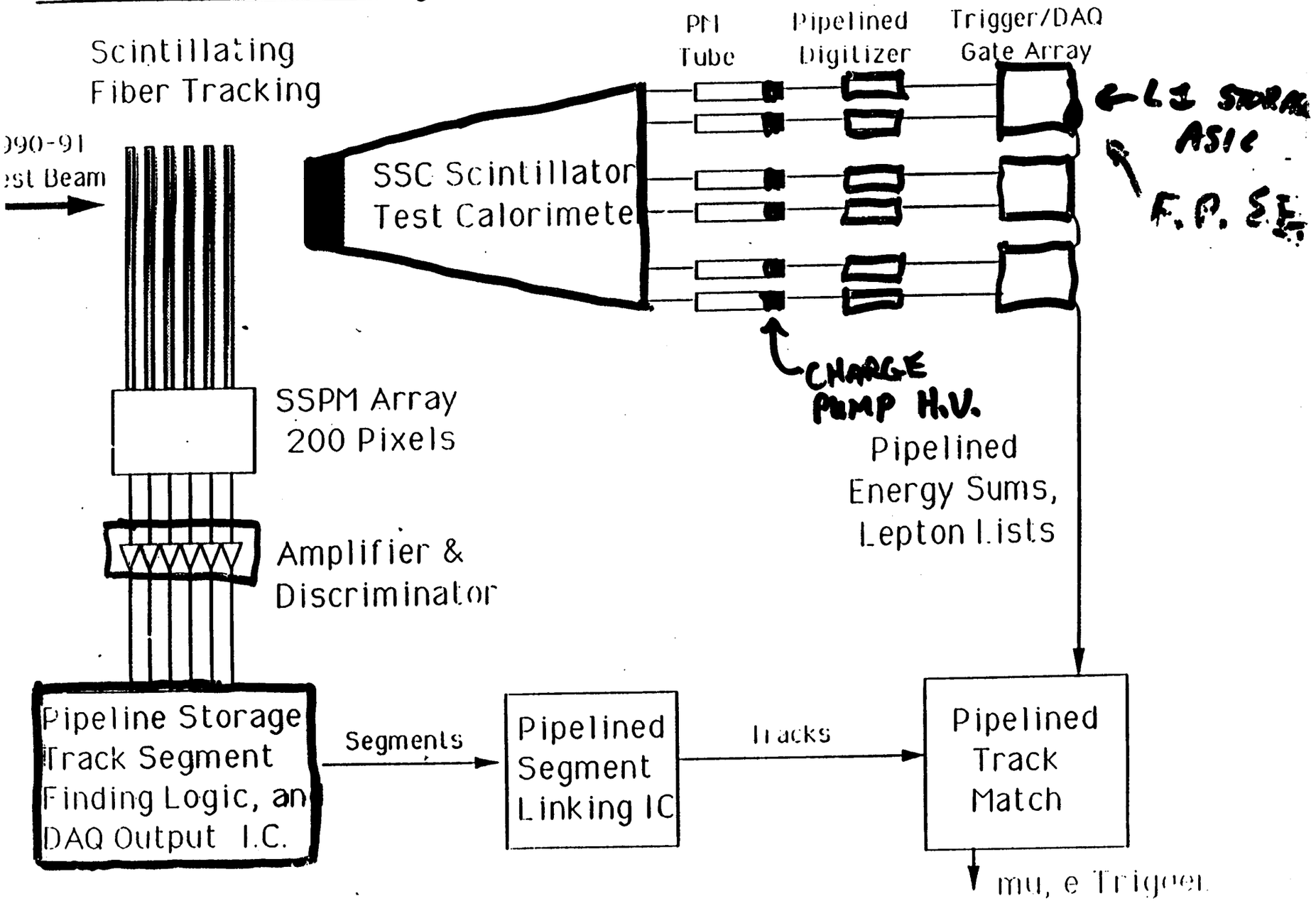
Main Negatives:

- No Separate Empires for Trig & DAQ ==> many natural enemies
- Possibility of Egg on SSC's Face for using no components from "front-end" subsystem collab.

++ ➡ Beam Test device

++ ➡ ORBIT NPN characterization (BiCmos looks OK...)

FNAL Pipelined Digitization/Trigger/DAQ Project



DYNAMIC RANGE OF PMT DIGITIZATION

HIGH END: Space-Charge Current Limit

$\sim 100\,ma \cdot 10\,ns = 1\,nc$ ($\equiv$ 10 TeV Full Scale)

LOW END: ELECTRONICS NOISE

$\sim 1500\ e^-$ in 16ns gate
for 10pf anode capacitance

$= 1/4$ f.c.

DYNAMIC RANGE LIMIT

$$\frac{1\,nc}{1/4\,fc} = 4 \times 10^6 \quad \left(= \frac{10\ TeV\ Full\ Scale}{2.5\ MeV\ least\ co}\right.$$

.... without playing the dynode card...

PRACTICAL LIMITS TO DYNAMIC RANGE

CABLE NOISE $\approx$ 1 mv in practical situat

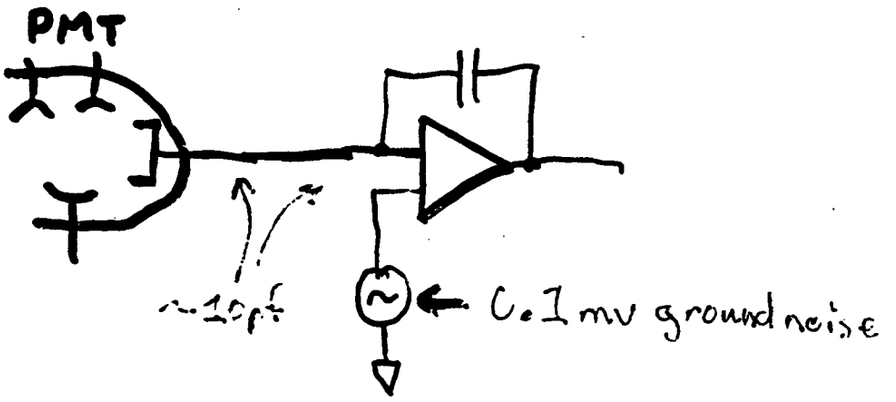
$$\frac{1\,\text{mv}}{50\,\Omega} \cdot 16\,\text{ns gate} = 320\ \text{fc} \quad \left(\begin{array}{l}1000\times \\ \text{noise} \\ \text{limit}\end{array}\right.$$

$$\boxed{\Rightarrow \text{DON'T USE A CABLE}}$$

CLOCKING NOISE (inside a metal can)

(0.1 mv ground noise) $\cdot$ (10 pf anode cap.)

= 1 fc ← This is our target



WE ARE SHOOTING FOR:

$$\frac{\text{FULL SCALE}}{\text{LEAST COUNT}} = \frac{1\,\text{pc}}{1\,\text{fc}} = \frac{10\,\text{TeV}}{10\,\text{MeV}} = 10^{6}$$

... or a 4x worse than electronic ...

? WHY GATED INTEGRATOR ?

⇒ Resets the Integrating capacitor every cycle! D.C. Coupled like PMT. (no problems w/ pileup or integrator hitting supply ...)

⇒ IDEAL SQUARE-BOX INTEGRATOR RESPONSE

? What rate of hits to design for?

$$\langle occ \rangle = \frac{dN}{d\eta} \cdot \Delta\eta \cdot \frac{\Delta\phi}{2\pi} \cdot \left\langle \frac{16/\text{crossing}}{@10^{34}} \right\rangle \cdot (\sim 2 \text{ for } \pi^0 \pi^+ \text{ splitting})$$

(plug)

$$= 8 \cdot (0.1) \cdot \left(\frac{0.1}{2\pi}\right) \cdot 16 \cdot 2$$

$$= \boxed{40\%}$$

? ENERGY FLOW ?

(EM fraction)

$$\langle E \rangle = \frac{dN}{d\eta} \cdot \Delta\eta \cdot \frac{\Delta\phi}{\sim\pi} \cdot \langle 1/\text{cross} \rangle \; \frac{0.6 \text{ GeV}}{\sin\theta} \cdot (\frac{1}{3}$$

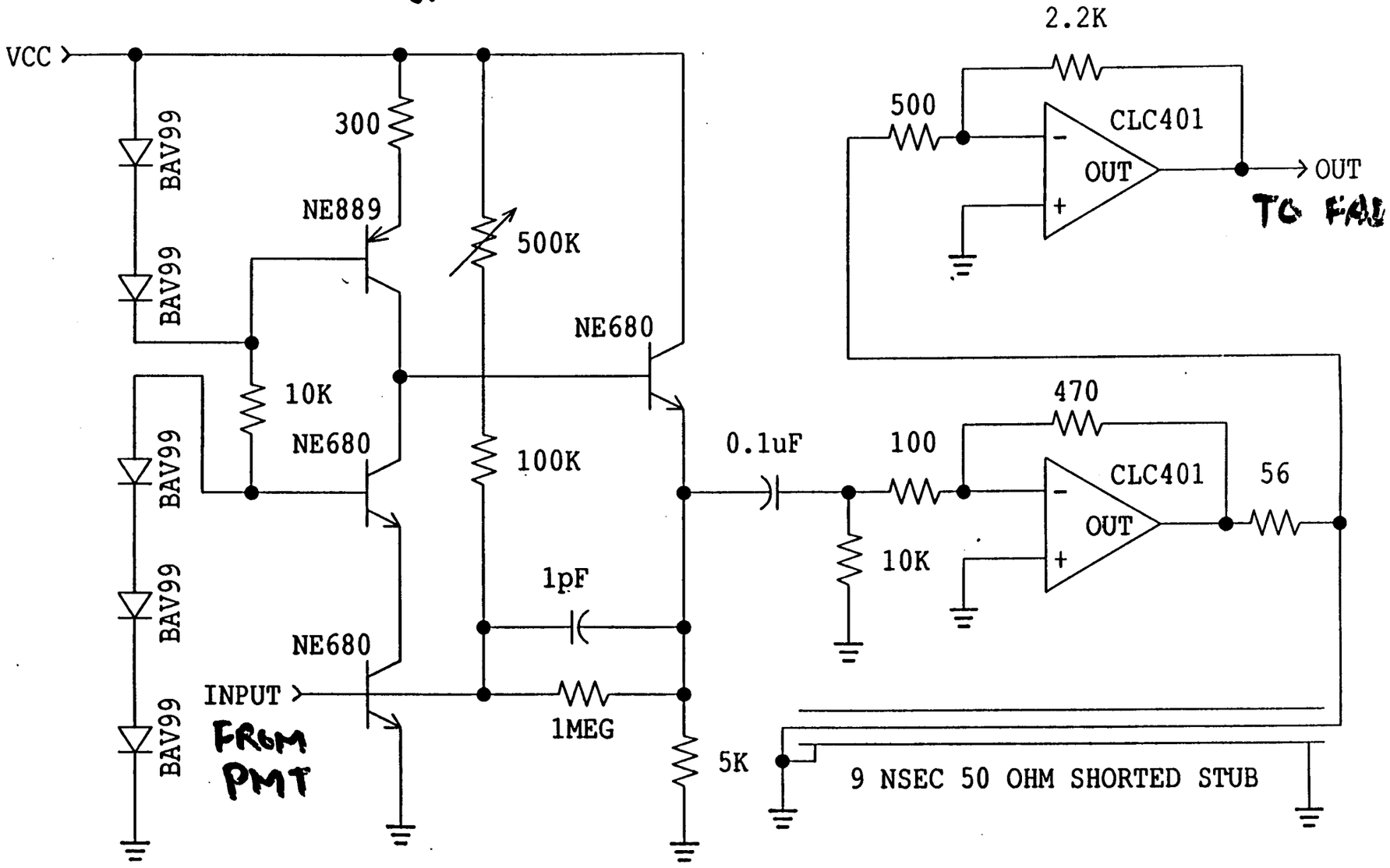
$$= (8)(0.1)\left(\frac{0.1}{2\pi}\right) \cdot 16 \cdot \frac{0.6}{0.15}$$

$$\approx 4 \text{ GeV/crossing/PMT}$$

16-CHANNEL "PROOF OF PRINCIPLE" FOR FAST + LOW-GAIN PMT (C. Rivetta)

1 CHANNEL INTEGRATOR

(PMT CLIP AMP FOR TEST BEAM)



A Fast PMT Digitization Circuit

- Part of a pipelined digitization / trigger / DAQ system for SDC being developed at FNAL

Goals for the PMT Digitization Circuit

- 20 bit dynamic range
  10 MeV least count → 10 TeV full scale

- Digitize in 16 nsec.

- 3 bit accuracy
  signal should be known to $\lesssim$ 0.5 %
  (1% const. term in calorimeter resolutio

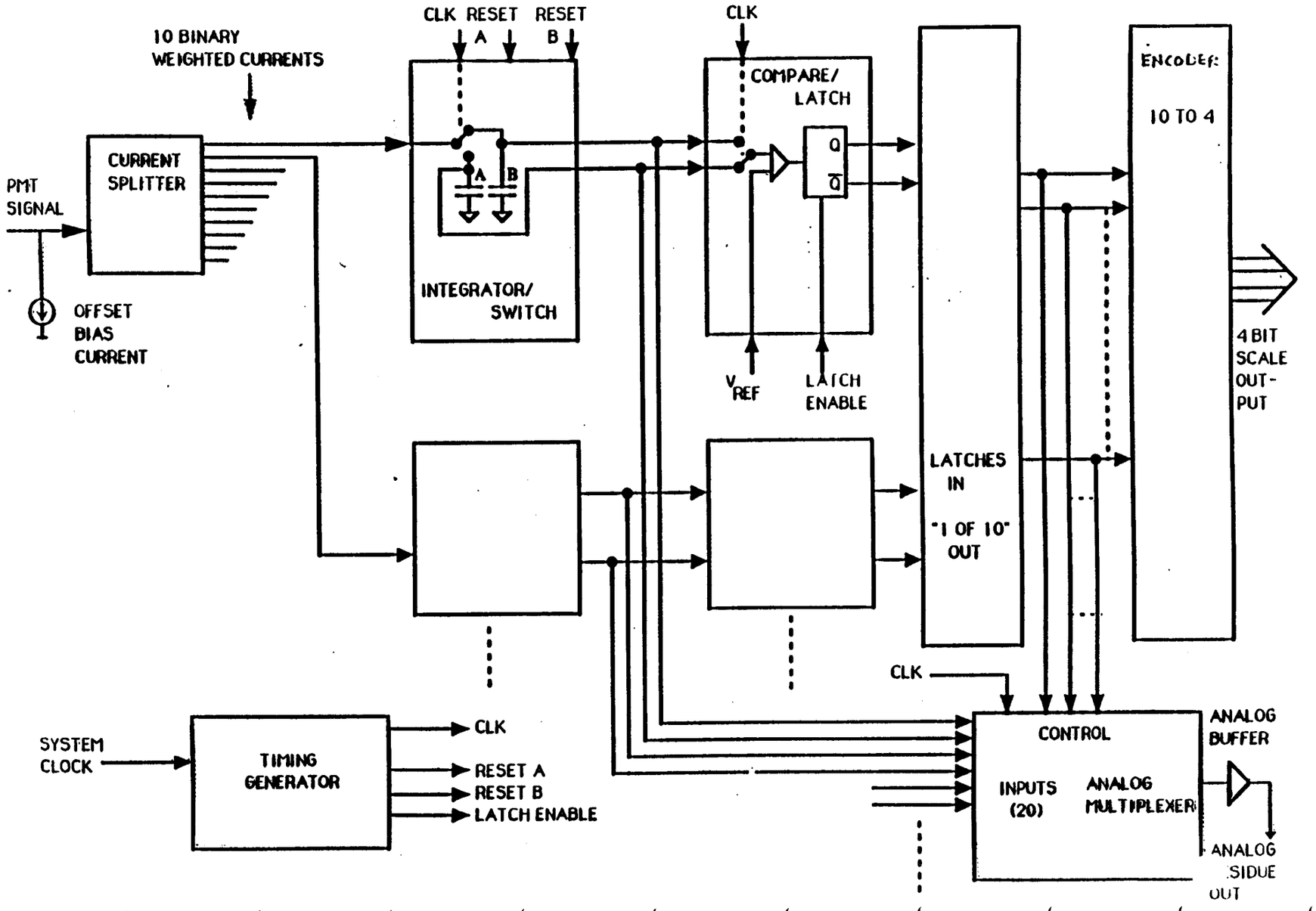
How to get large dynamic range

- Split current by factors of 2 ($I/2$, $I/4$ ...)
  only digitize voltage which is between half and full scale.
- Lowest 8 bits from a commercial FADC (mant
- Higher bits correspond to (binary weighted) scale factors. (exponent)

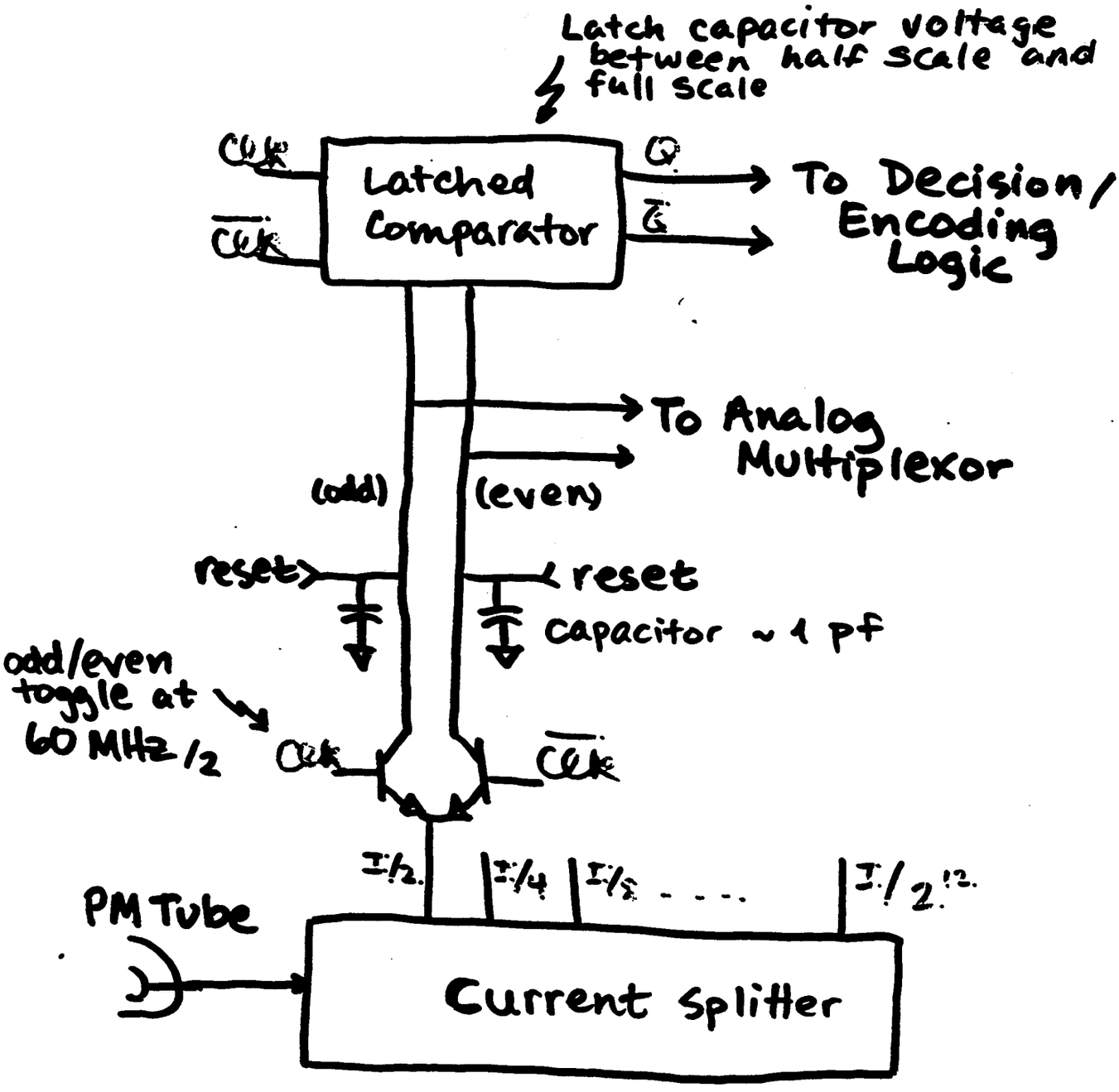
1ST PASS PMT DIC
CIRCUIT LAYOUT

TOM ZIMMERMAN
5/25/90

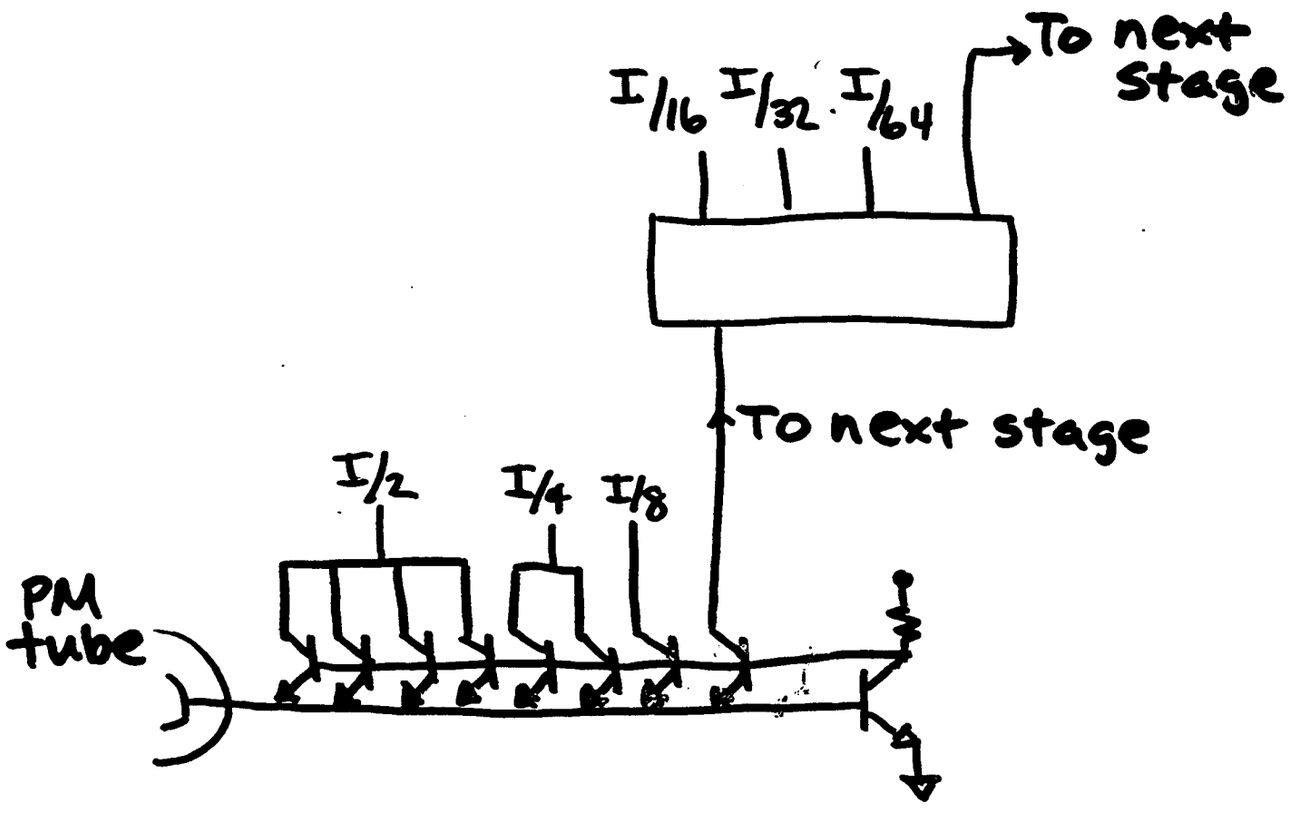
PHOTO TUBE DIGITIZER



PMT Digitization Circuit



Current Splitter



- Large Dynamic range (~ 10^4)
- Fast PMT charge collection
  (< 3 ns over full dynamic range)
  WITH Tek Bipolars

Circuit Operation

Every 16 ns:

1 capacitor is collecting charge

Other capacitor:

- Comparator, latch
- determine which capacitor is between half and full scale
- Encode scale bits (parallel)
- Switch relevant cap. voltage to FADC (analog multiplexor)
- Reset capacitor

Circuit will be on a chip

ASIC - application specific integrated circuit

We are currently using Tektronix Quick-chip design package (TekSpice) to design the chip.

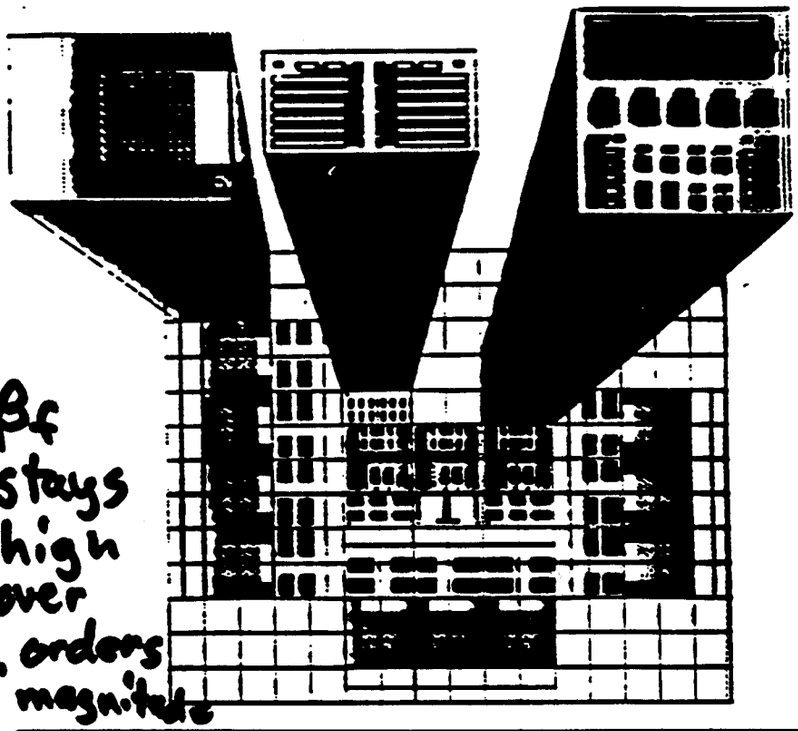
Decision Encoding Logic

Determining which cap voltage is between half and full scale

(5 successful designs already in use in RF-clocked systems @ FNAL...)

QUICKTILE™ IC DESIGN

- Speed, analog precision, and density of full custom design
- Fast development time and convenience of QuickChip design
- High speed analog process (SHPi):
  - 3x density of SH3 (QC2 family)
  - Sidewall oxide isolation
  - f_t ~ 8.5GHz, f_{max} ~ 11GHz
  - P-channel JFETs ($g_m/2\pi C_{iss} \geq$ 600 MHz)
  - Improved breakdown ($LV_{CEO} \geq$ 8V)
  - 2 layer Au metal on 4 um pitch
  - Schottky diodes (guarded & unguarded)
  - Low power (f_t peak at 1mA for N2 device)
- QuickCustom design tools integrated with QuickKic graphics editor:
  - Guided user layout
  - Design rule checks (DRC)
  - QuERC electrical rule checker
  - Connectivity checks
  - Passive component design
  - Interconnect parasitic calculation
- Integration levels up to:
  - 225 equiv. full tiles in array core
  - 60 pads on a .144" X .144" die
- Forward compatibility of QuickChip 6 designs for circuit expansion.
- Expandable library of 16 standard tiles



Bf stays high over 7 orders of magnitude Ic

General Description

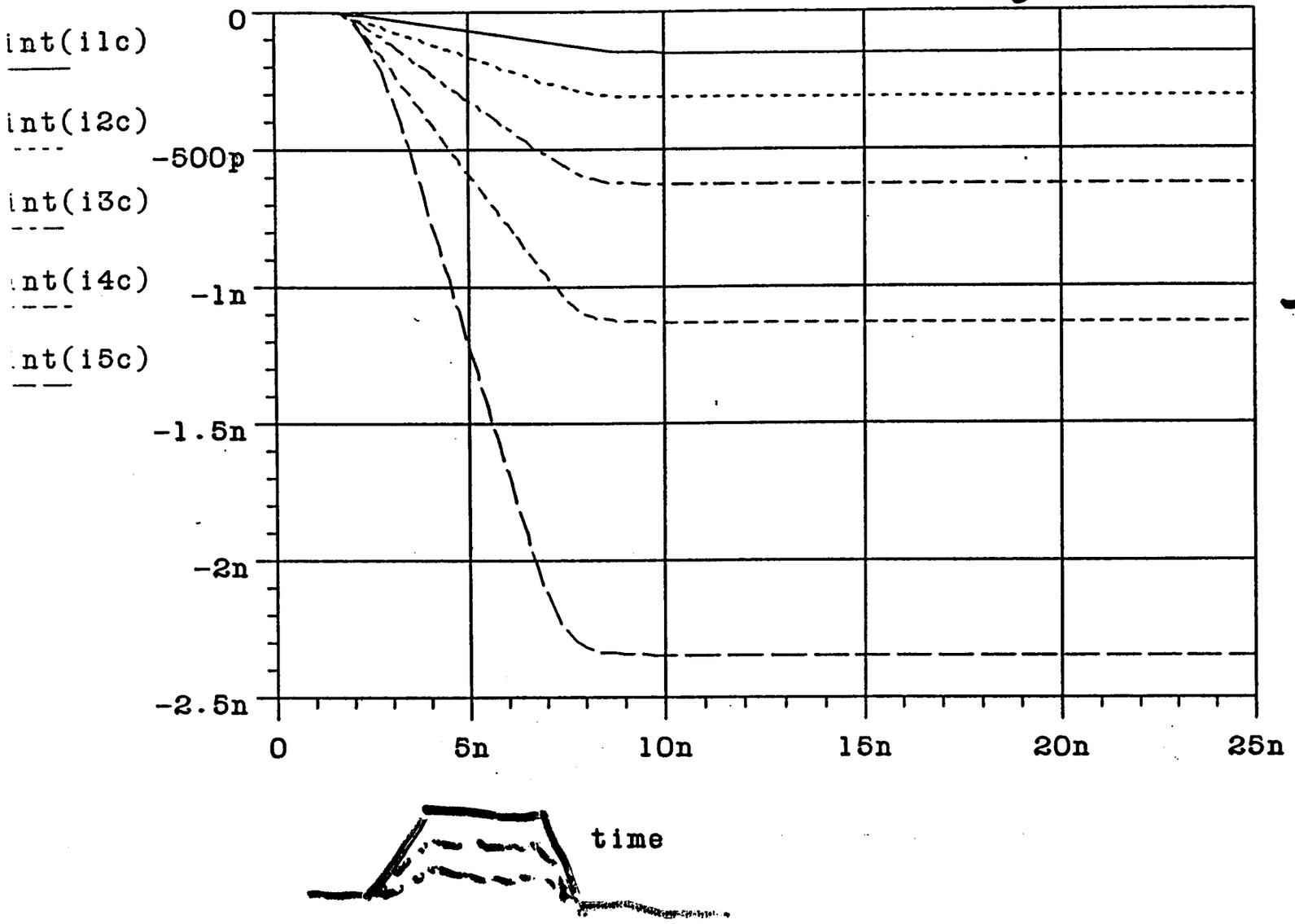
The *QuickTile™* approach to integrated circuit design combines a new, higher performance wafer fabrication process with our *QuickCustom™* design system giving the ASIC designer a powerful tool that easily produces custom arrays. Extending from the successful *QuickChip™* family of analog arrays, the QuickTile method brings a new dimension of configurability to the designer. It enables greater flexibility in device count and placement which is necessary for higher performance and more functionality. These characteristics, previously available only in full custom design, are now available to the QuickTile designer with the design and layout ease associated with QuickChips.

The QuickTile design method is based on the use of "standard tiles." Each tile is composed of a fixed set of unconnected devices that are arranged for convenient interconnection to provide a functional increment to a larger integrated circuit design. The devices on the standard tiles are precharacterized and modeled, significantly simplifying circuit design. The tiles are all exactly the same size (or submultiples thereof.) These tiles are placed by the designer in a way that best accomodates the circuit needs. This design method requires that masks be generated for all layers, the same as full custom. However, unlike full custom, which requires each device to be placed on the IC individually, the QuickTile design method "snaps" standard tiles together on a grid, thus

Tektronix

Full Splitter, IVAL=76.8m 07/23/90 10:13:02

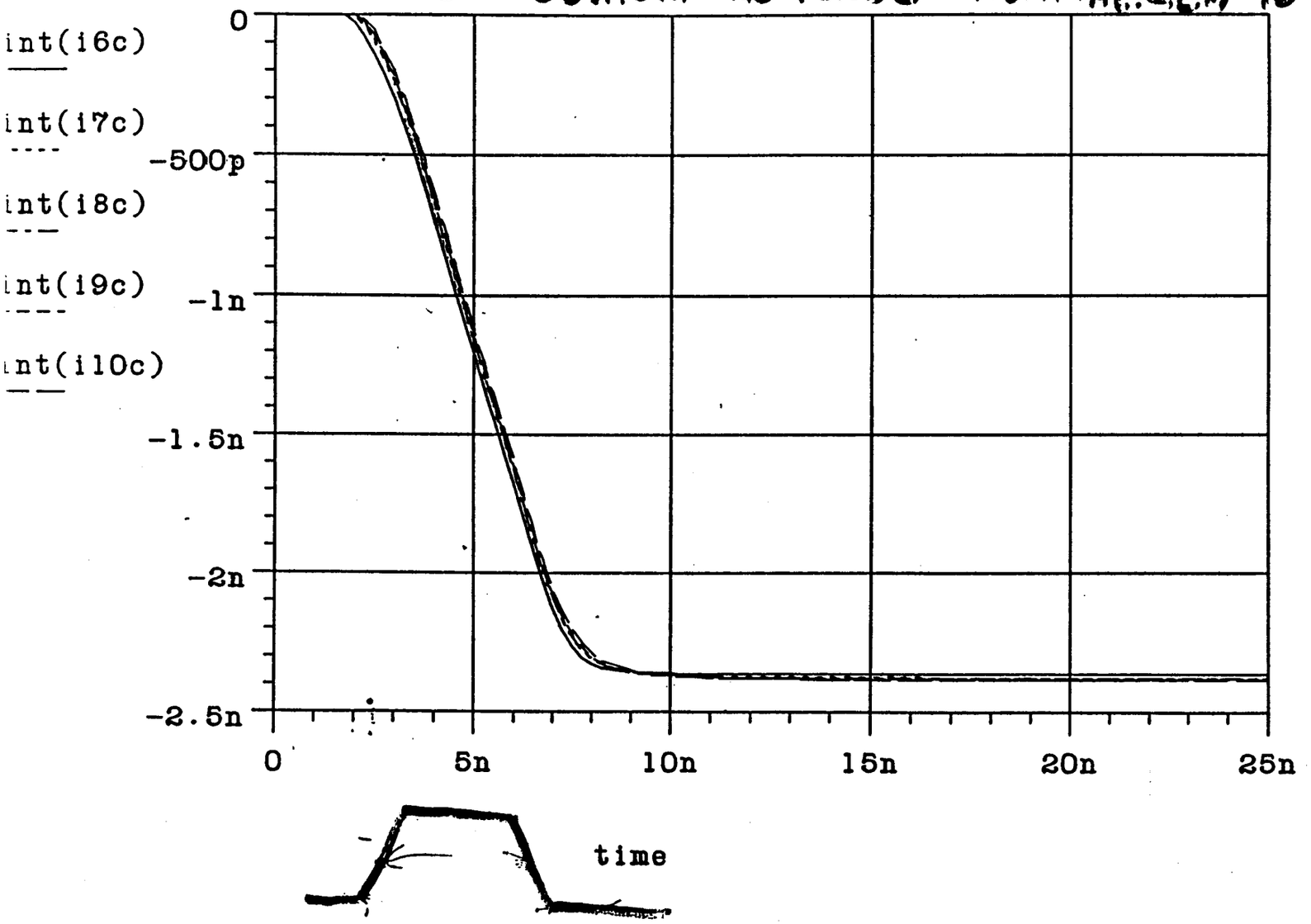
GATED INTEGRATOR WAVEFORMS



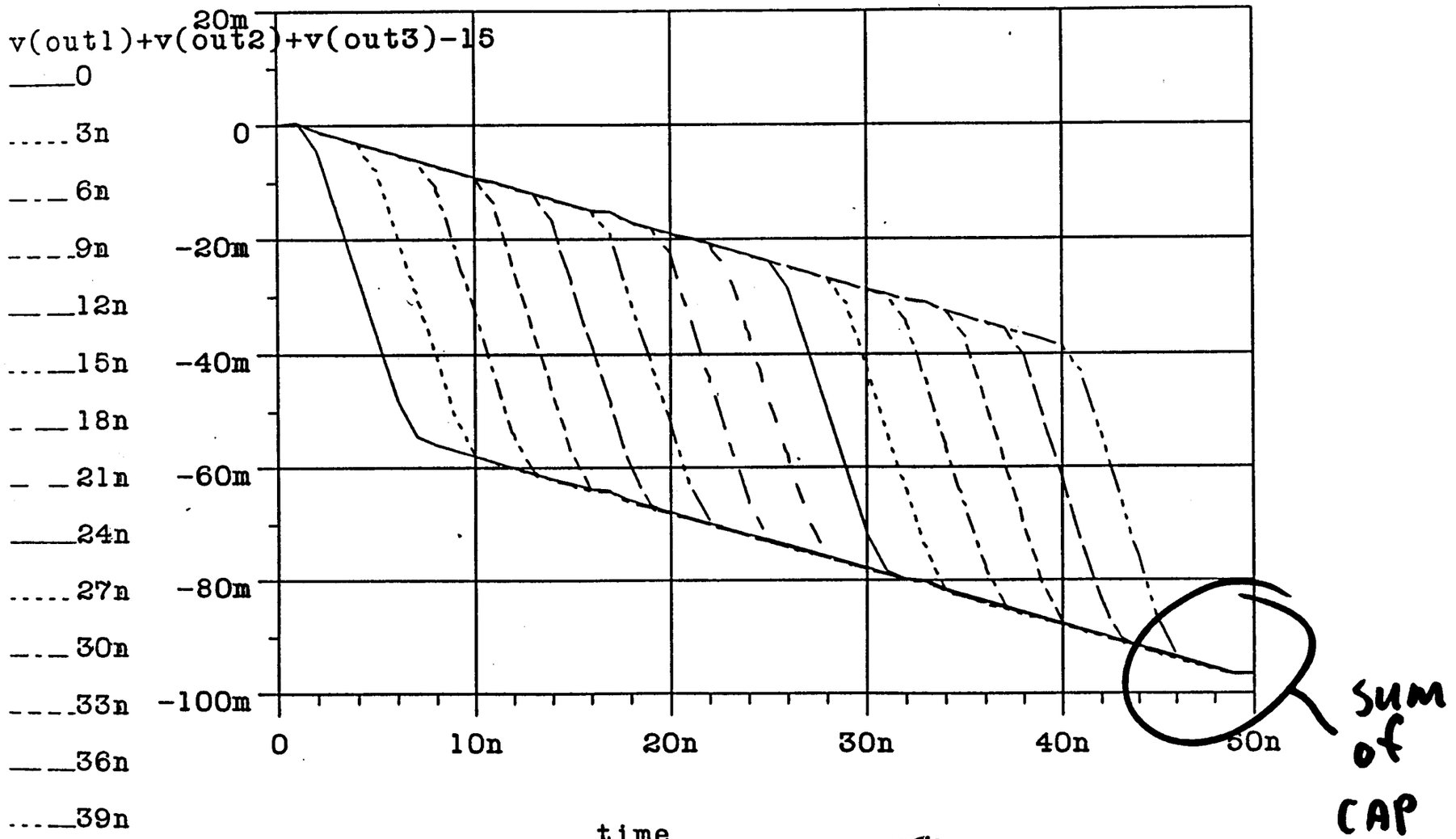
FADC R
8 BIT
use dy
range
betwe
½ and
full sc

Full Splitter, IVAL=76.8m 07/23/90 10:13:03

INTEGRATOR RESPONSE NORMALIZED TO PULSEWIDTH



Current Switch test circuit tzero 01/30/90 13:30:27



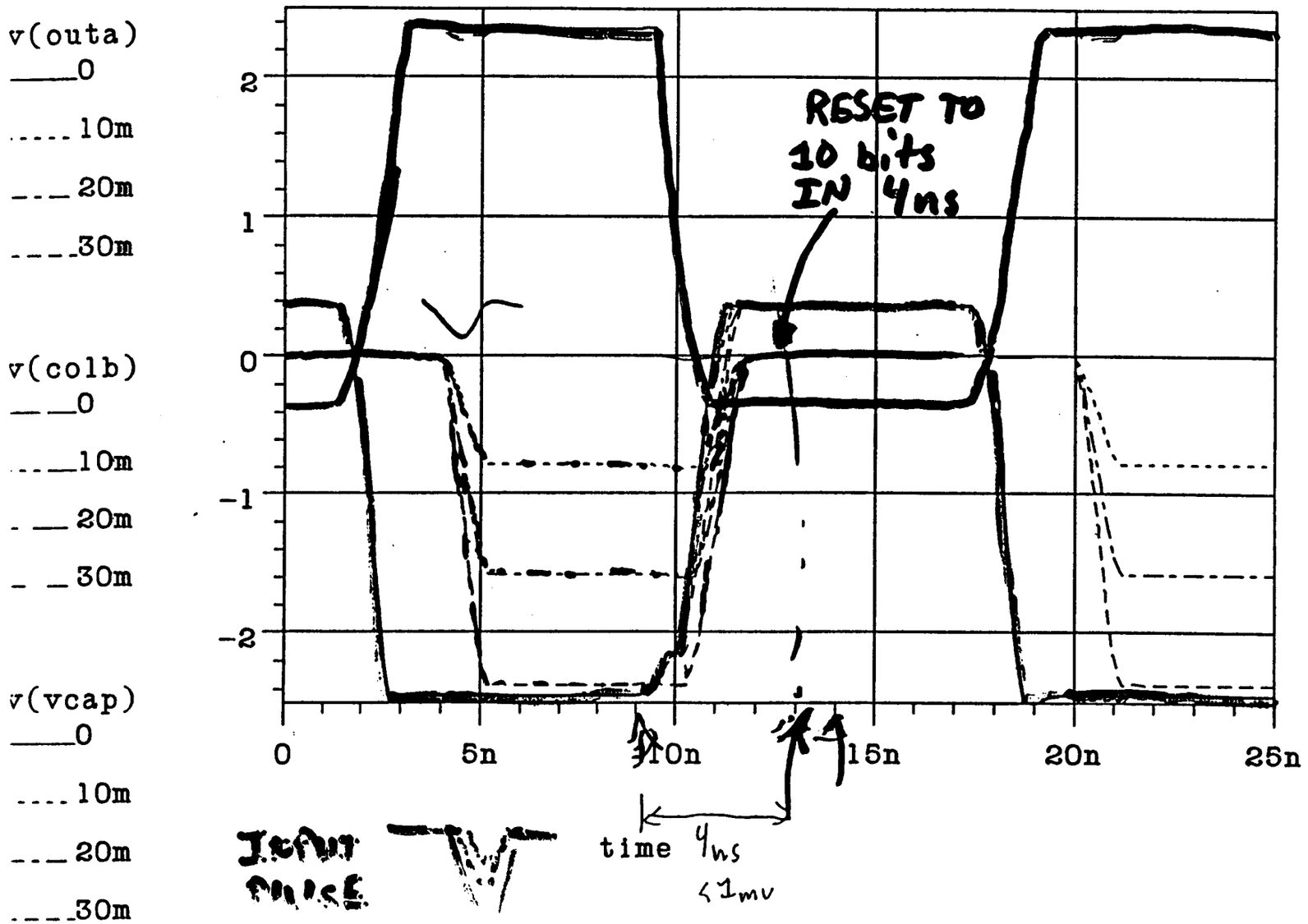
sum of CAP VOLTAGE

PMT

TRUE: "GATED INTEGRATOR" PERFORMANCE is indep of pulse

shottkey bridge reset driver

03/01/90 10:02:57



Target Specifications for Phototube Digitization System

Unit Cost:

Using 1989 parts costs in high quantities: $60/channel. This is broken down as follows: $10 for the analog ASIC, $40 for the commercially-purchased Flash ADC, and $50 for a Trigger/DAQ gate array chip which is shared among 5 Phototubes in a tower ($10/PM tube).

For an SSC calorimeter with 50,000 PM tubes, this is $3M.

Power dissipation:

Using 1989 commercially available parts: 650 mw/channel. This is broken down as follows: 100 mw for the analog ASIC, 250 mw for the commercially-purchased Flash ADC, and 1W for a Trigger/DAQ gate array chip which is shared among 5 Phototubes in a tower (200 mw/tube).

For an SSC calorimeter with 50,000 PM tubes, this is 32 kw. All of this power is dissipated on the outside of the detector, so this poses no particular problem.

Least Count Sensitivity: = 1 fC
= 1 millivolt on a 1 pf capacitor
= 0.1 ua * 10 nsec current pulse from phototube
= 10 MeV for a calorimeter with 100 Photoelectrons/Gev and a Phototube gain of ~10**4

Full Scale Sensitivity: = 1 nC
= 1 volt on 10 pf after 1/100 current attenuation
= 100 ma * 10 nsec current pulse from phototube
= 10 TeV for a calorimeter with 100 Photoelectrons/Gev and a Phototube gain of ~10**4
= 10**6 Least Counts (20-bit dynamic range)

Binary Output:

- 4-bit scale code (floating point exponent) produced by ASIC. The scale code has a range of 0-11, corresponding to the twelve binary-weighted scale factors.
- 8-bit Mantissa produced by Flash ADC. Since the flash ADC will only be used to digitize voltages between 1/2 scale and full scale, the Flash ADC output codes of 0-255 will actually correspond to 256-511. Thus, the value of the digitized charge will be:

  Charge (in fC) = (FADC Mantissa + 256) x 2**(scale code)

  Thus, the signal will be digitized to an accuracy of between 1/256 and 1/511 of itself, depending on where it lands on the ADC range. This compares well with a calorimeter resolution of ~15%/sqrt(E) + 1%, since the digitization error would be about 0.2%.

Input Characteristics:

- Large-Signal Recovery Time Constant of < 1 nsec. Note that this will not allow recovery to full 20-bit accuracy within 16 ns following a full-scale hit.

- The analog ASIC would be optimized for placement in close proximity to the Phototube (i.e. no cable). The input stage (probably a single

Theory of Operation

Input Stage: This is a low-impedance amplifier which functions to drain the charge off of the annode capacitance (~15 pf) of the PM tube. It consists of a common-base NPN transistor amplifier with feedback to lower the input impedance. The input stage basically passes the Phototube current through with a gain of ~1, and serves to isolate the current-splitting stage from the annode capacitance.

Current Splitting Stage: The instantaneous phototube current is split onto a number of binary-weighted outputs using bipolar current-splitting techniques (i.e. multiple collectors, etc.). These binary-weighted outputs are used to generate the different scales for the floating-point result.

Current Switching Stage: This is a standard emitter-coupled current switch which routes the scaled phototube currents to one of 2 sets of integrating capacitors each 16 nsec. Current switching times of < 100 psec are be obtained, generating a very sharply defined gate. Simulations indicate that nearly ideal "gated integrator" behavior is obtained: the total charge registered by the circuit is independent of the pulse position within the gate, and the total charge registered by a pulse which traddles a gate is equal (to within 1%) to the charge registered when the pulse is centered in the gate.

The circuit toggles between the two sets of capacitors each RF bucket.

During the 16-ns period that charge is being integrated on one set of capacitors, the following operations are performed on the other set:

i) Each binary-weighted capacitor signal has an individual latched comparator on it. This is used to identify which one of the capacitors is between 1/2 scale and full scale. This capacitor voltage is the one that will be chosen to be routed off-chip to the commercial FADC. The comparator outputs are valid 2ns after the end of the ADC gate.

ii) The comparator outputs are latched, and and a single level of ECL logic is used to identify the capacitor of interest. This process is completed 4ns after the end of the ADC gate.

iii) This signal is used to enable an analog multiplexor (a shottkey-diode sampling bridge) which selects the correct capacitor voltage for routing to the Flash ADC. Simulations indicate that the analog multiplexor settles to 9-bit accuracy in within 3ns, or 7ns after the end of the ADC gate. At the end of this period, the sampling bridge is opened. This "freezes" the analog signal at the output of the multiplexor and allows most of the 16-ns clock period as settling time for routing the analog signal off-chip to the FADC.

iv) The digital range selection bits are encoded to produce a 4-bit scale code which is routed off-chip. This happens in parallel with the settling of the analog signal to the FADC.

iii) Finally, the capacitors are reset in preparation for the next gate. This takes < 4ns, so that the complete readout & reset cycle is finished 11 ns after the end of the gate. The capacitors remain idle

common-base NPN transistor) must have a low enough input impedance to drain off the charge from the annode (~15 pf) with the 1 nsec RC recovery time mentioned above.

- The input will be compatible with a passive phototube pulse-clipping network, either delay-line or R-C. Such clipping techniques (which effectively subtract off the exponential tail of the scintillation light pulse) have been used to bring the pulse from a PM tube back to baseline within ~10ns. This enables one to completely reject energy deposited in adjacent RF buckets. This technique is most effective in EM calorimeters for which the energy deposition is essentially instantaneous, and for hadron calorimeters such as Iron/Scintillator which have a very small delayed neutron component & can be made compensating inside a 16-ns gate.

- The unit will be DC-coupled throughout to eliminate rate-dependent pedestal effects, gain saturation, etc. This is especially important at the SSC where hundreds of GeV are being dumped into the calorimeter every crossing -- and with the abort gaps producing a cyclical pulsation of the average energy deposition.

CHARACTERIZATION OF ORBIT NPN's (T. Zimmerman)

(spice models derived from measurements of naked devices)

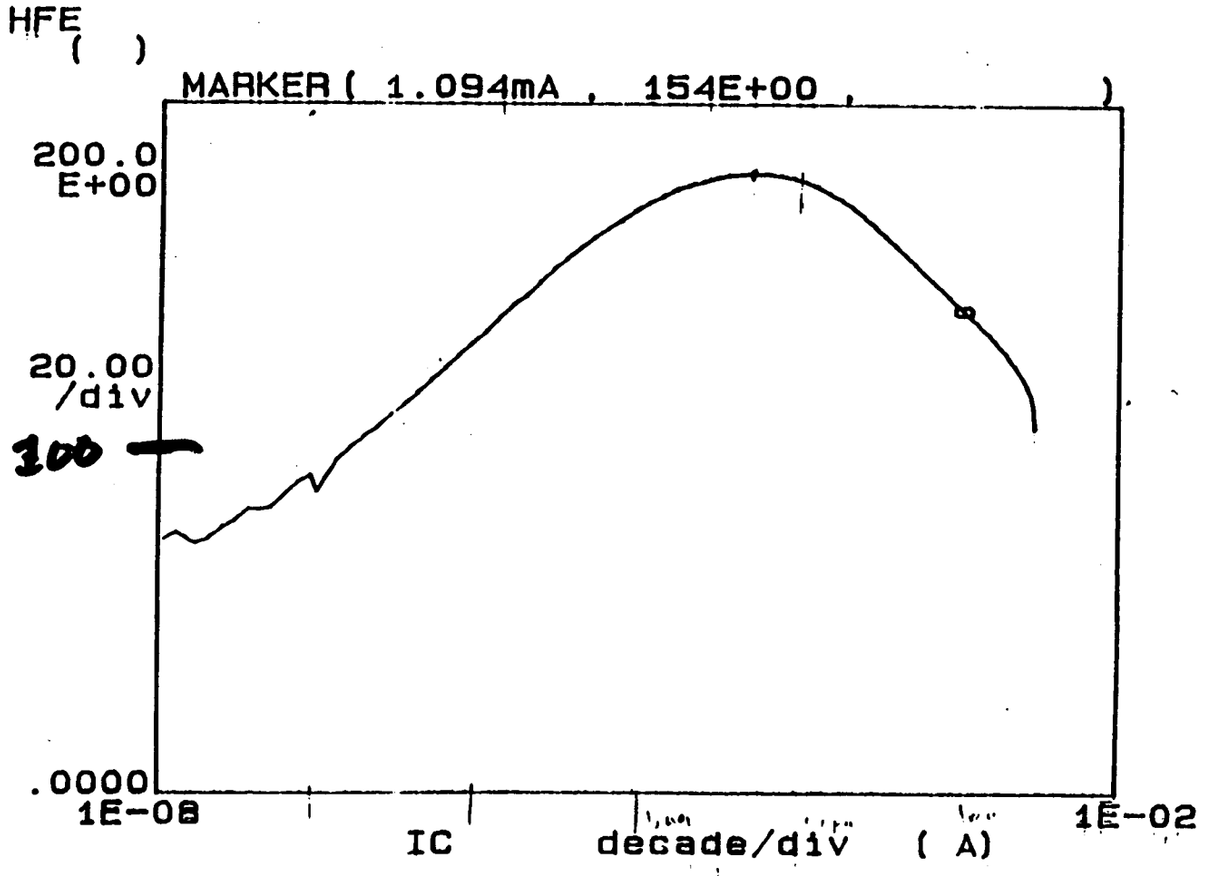
⇨ ORBIT LOOKS O.K. TO FAB PASSABLE SPLITTER.
...LAYOUT OF SUBCIRCUITS IN PROGRESS...

```
*ORBIT small NPN (X1)
.model npn1 npn is=6.7e-17 vaf=35 bf=141 rc=800 rb=300 re=14.7 ne=1.46 ise=2.6
+tf=60e-12 cje=.1p cjc=.1p ccs=.22p mje=.333 vje=.75 mjc=.5 vjc=.75
+mjs=.5 vjs=.75 fc=.67

*ORBIT big NPN (X32)
.model npn32 npn is=2e-15 vaf=35 bf=143 rc=65 rb=25 re=3 ne=1.46 ise=2.6
+tf=60e-12 cje=3.2p cjc=2.1p ccs=2.0p mje=.333 vje=.75 mjc=.5 vjc=.75
+mjs=.5 vjs=.75 fc=.67

******* NPN8 model NOT measured; this is a guess! ***********
*ORBIT medium NPN (X8)
.model npn8 npn is=5e-16 vaf=35 bf=143 rc=240 rb=75 re=5 ne=1.46 ise=2.6
+tf=60e-12 cje=.8p cjc=.56p ccs=.65p mje=.333 vje=.75 mjc=.5 vjc=.75
+mjs=.5 vjs=.75 fc=.67
```

****** GRAPHICS PLOT ******

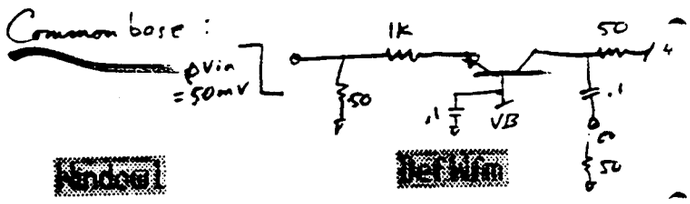


Variable1:
VB -Ch3
Linear sweep
Start .400
Stop .880
Step .005

Constants:
VE -Ch1 .000
VCE -Ch2 10.00
VSUB -Ch4 .000

SA 602 DIGITIZING SIGNAL ANALYZER
date: 24-APR-91 time: 15:00:09

Common base :

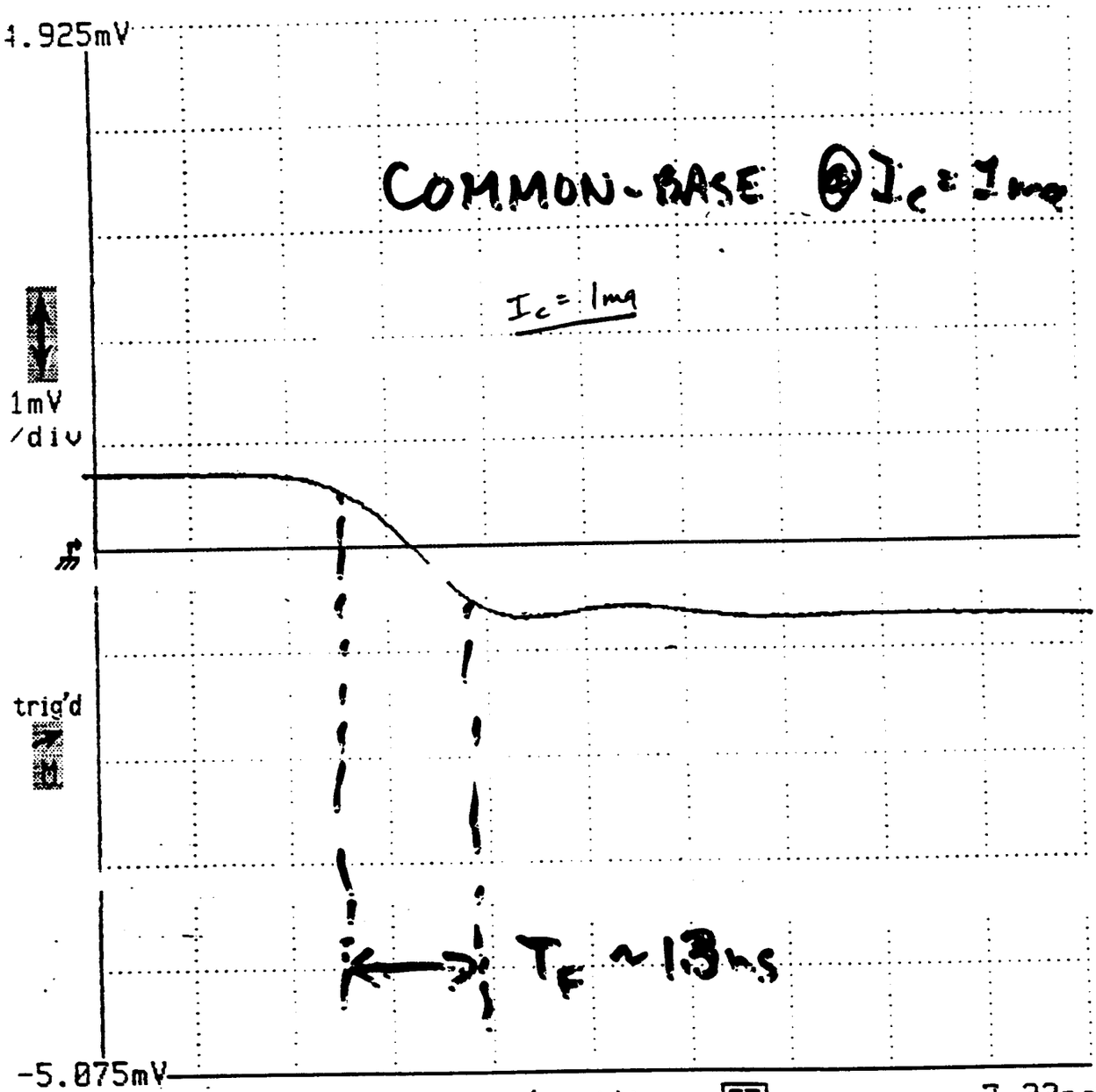


Tek

Cursors

Window1

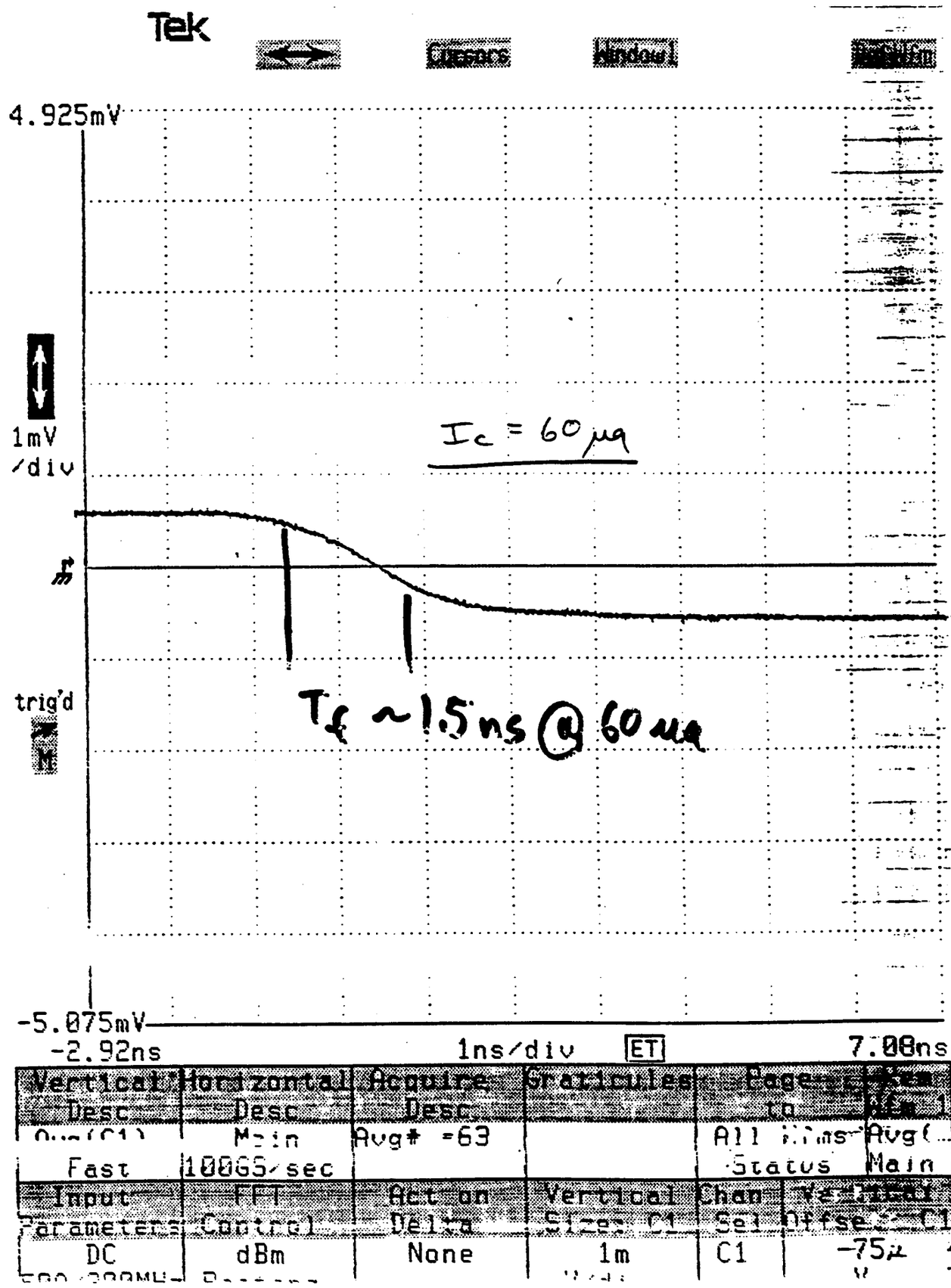
DefWfm



1:Avg(C1) Main				Page To	Rem Wfm-1
1mV 1ns				Single Waveform	Avg(... Main
			Main Size	Pan/ Zoom	Main Position
			1n	Off	-2.8n

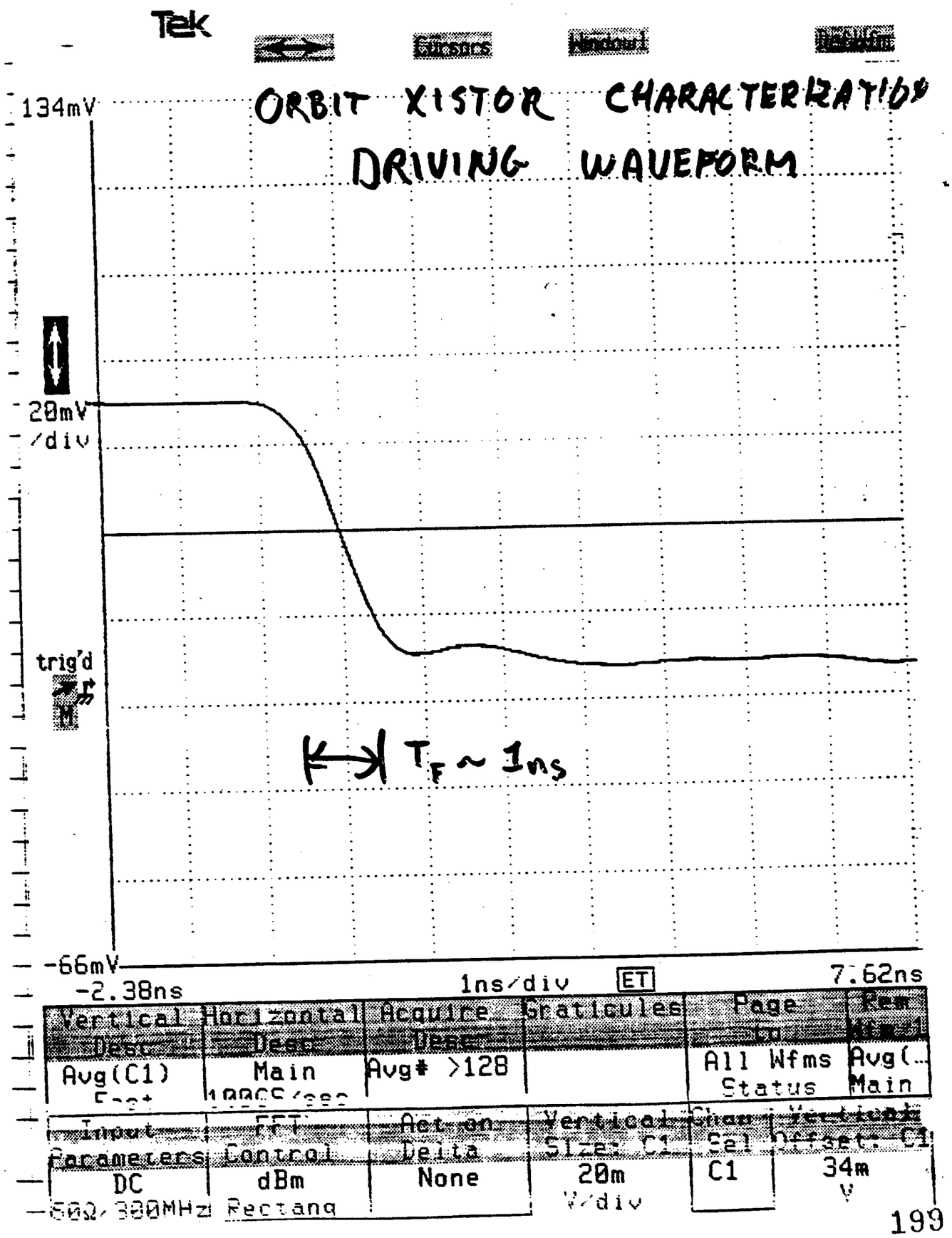
DSA 602 DIGITIZING SIGNAL ANALYZER
date: 04-APR-91 time: 13:10:40

(Common base)

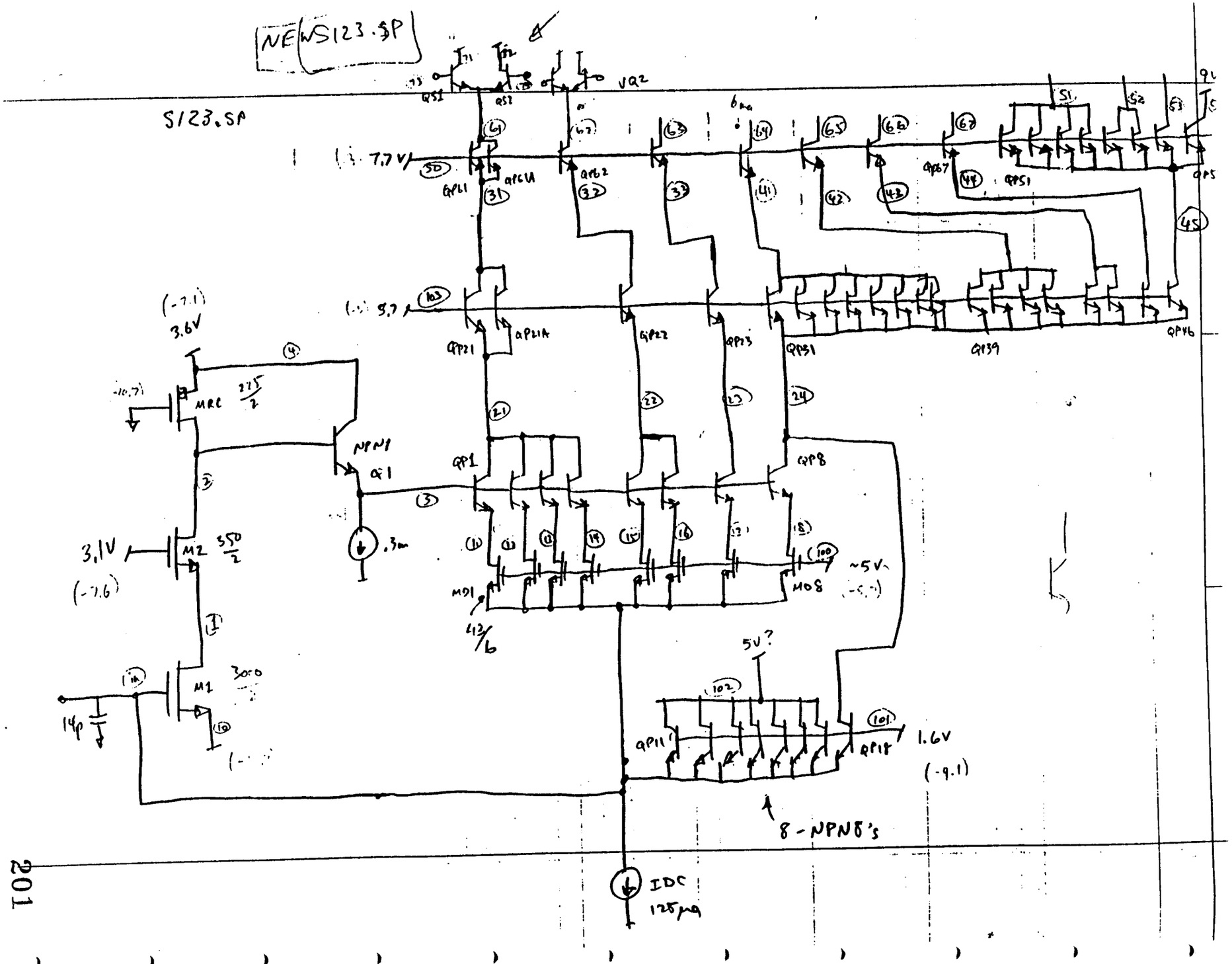


Vertical Desc	Horizontal Desc	Acquire Desc	Graticules	Page to	Meas
C1	Main	Avg# =63		All ms	Avg(
Fast	100GS/sec			Status	Main

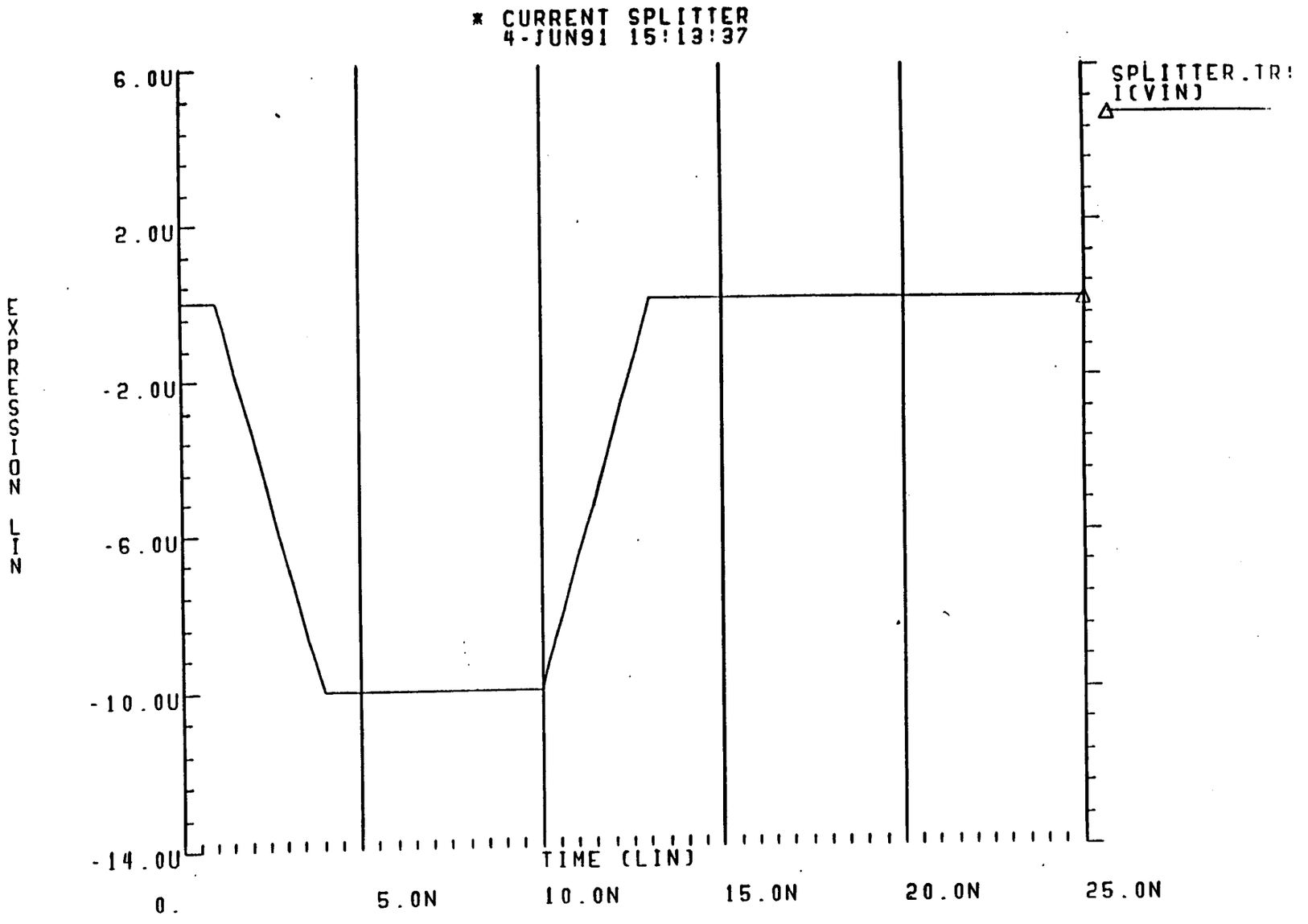
Input Parameters	FFT Control	Action Delta	Vertical Size C1	Chan Sel	Vertical Offset C1
DC	dBm	None	1m	C1	-75μ


DSA 602 DIGITIZING SIGNAL ANALYZER
Tek
Cursors
Window1
ORBIT XISTOR CHARACTERIZATION
DRIVING WAVEFORM
134mV
20mV
/div
trig'd
M
$T_F \sim 1ns$
-66mV
-2.38ns
1ns/div
ET
7.62ns
Vertical Desc
Avg(C1)
Horizontal Desc
Main
Acquire Desc
Avg# >128
Graticules
Page to
All Wfms Status
Rem Wfm1
Avg(...
Main
Input Parameters
DC
50Ω/300MHz
FFT Control
dBm
Rectang
Act on Delta
None
Vertical Size: C1
20m
V/div
Chan Sel
C1
Vertical Offset: C1
34m
V

Orbit Splitter Design (Bi-CMOS)

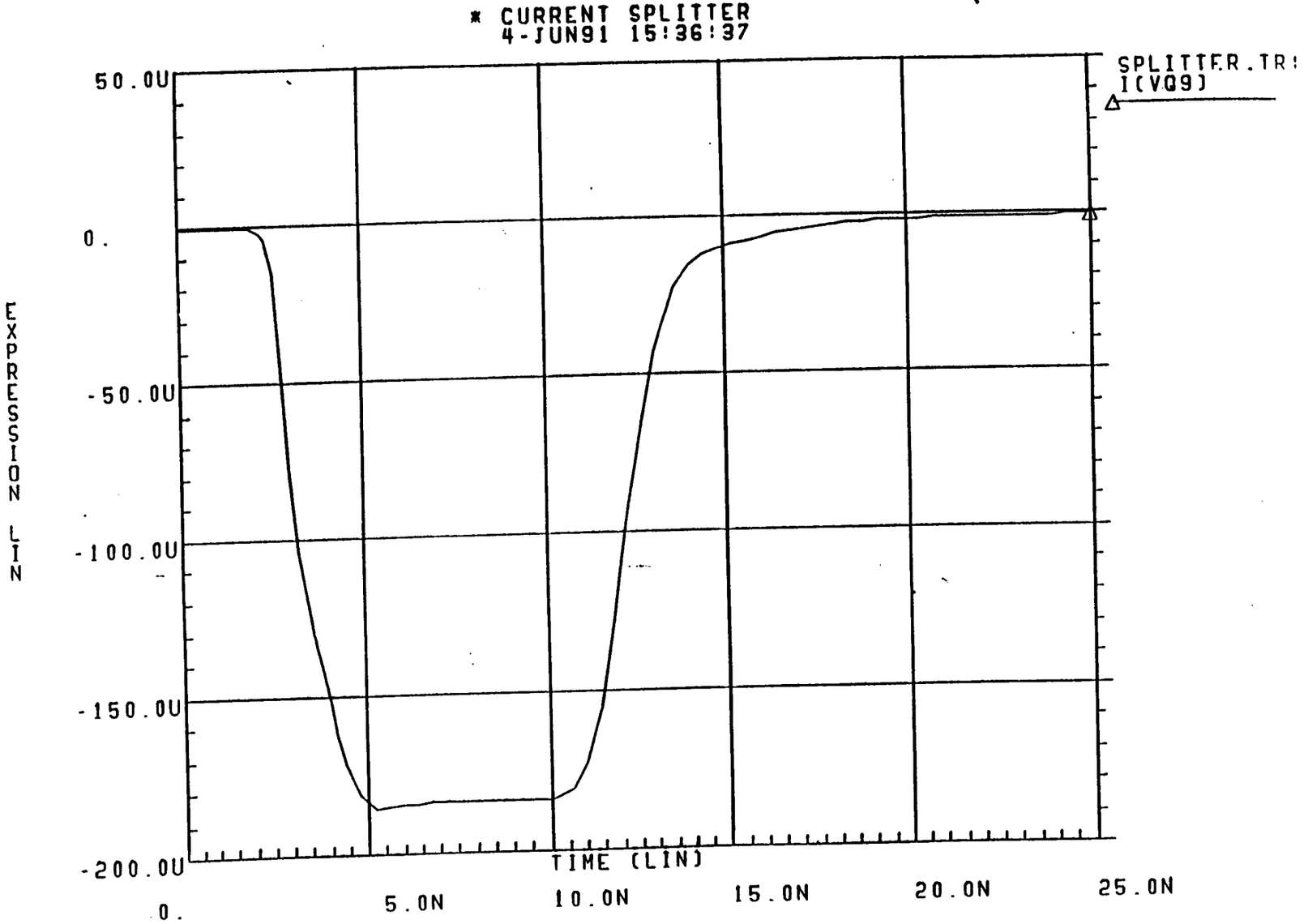

NEWS123.SP
S123.SP
VQ2
QS1
QS2
7.7V
QP61
QP61A
QP62
QP67
QP51
QP5
5.7
QP21
QP21A
QP22
QP23
QP31
QP39
QP46
3.6V
MRC
NPN1
Q1
QP1
QP8
3.1V
M2
.3m
M01
M08
~5V
M1
14p
5V?
QP11
QP18
1.6V
8-NPN8's
IDC
125μa

SPICE DRIVING WAVEFORM FOR ORBIT SPLITTER

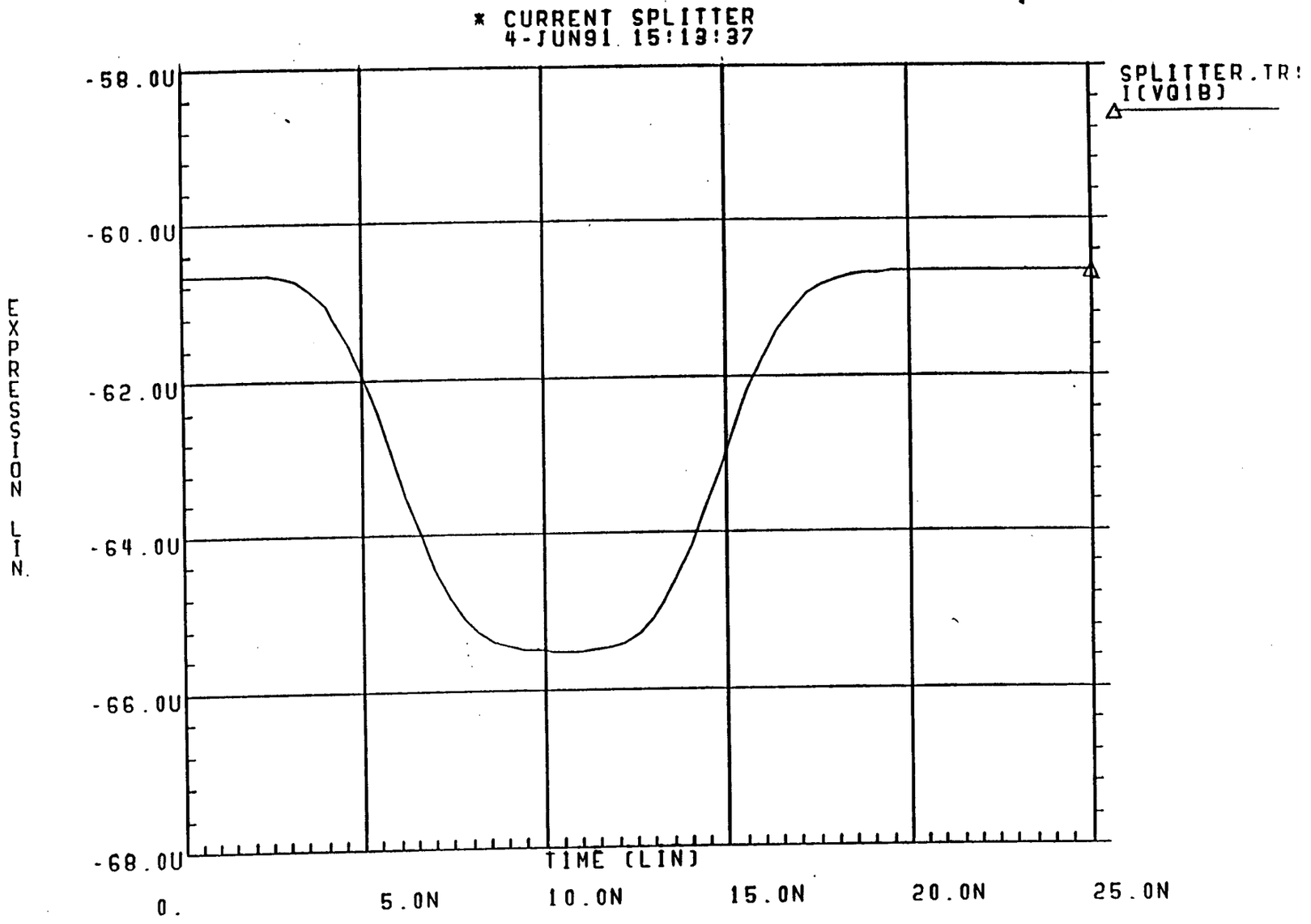


Spice Output waveform for 0.1A input pulse

Input : 100mA



Sp e. output waveform for Wave Input pulse



NEAR-TERM PLANS

(1) Test Beam PROOF-OF-PRINCIPLE FADC + AMP

(2) FAB ORBIT SPLITTER + GATED INT.
layout now; "final" device by test beam?

(3) IMPORT FADC (2-stage flash, ~70 mw)

(4) SMALL RAM [redacted] IMPORTED ON-CHIP

↳ Download MC events to PMT base!
(full-speed test of trigger, cables, & DA

Status of Electro-optical Modulators

V. Radeka

Papers presented at the Symposium on
Detector Research and Development for
the Superconducting Super Collider,
Fort Worth, TX, October 15-18, 1990

BNL–45393

A STUDY OF ELECTRO-OPTICAL MODULATORS FOR TRANSFER OF DETECTOR SIGNALS BY OPTICAL FIBERS*

T. Tsang, V. Radeka, T. Srinivasan-Rao, and W. J. Willis†

Brookhaven National Laboratory, Upton, NY 11973

†BNL and Columbia University, New York 10027

October 1990

*This research was supported by the U. S. Department of Energy:
Contract No. DE-AC02-76CH00016.

T. Tsang, et al.

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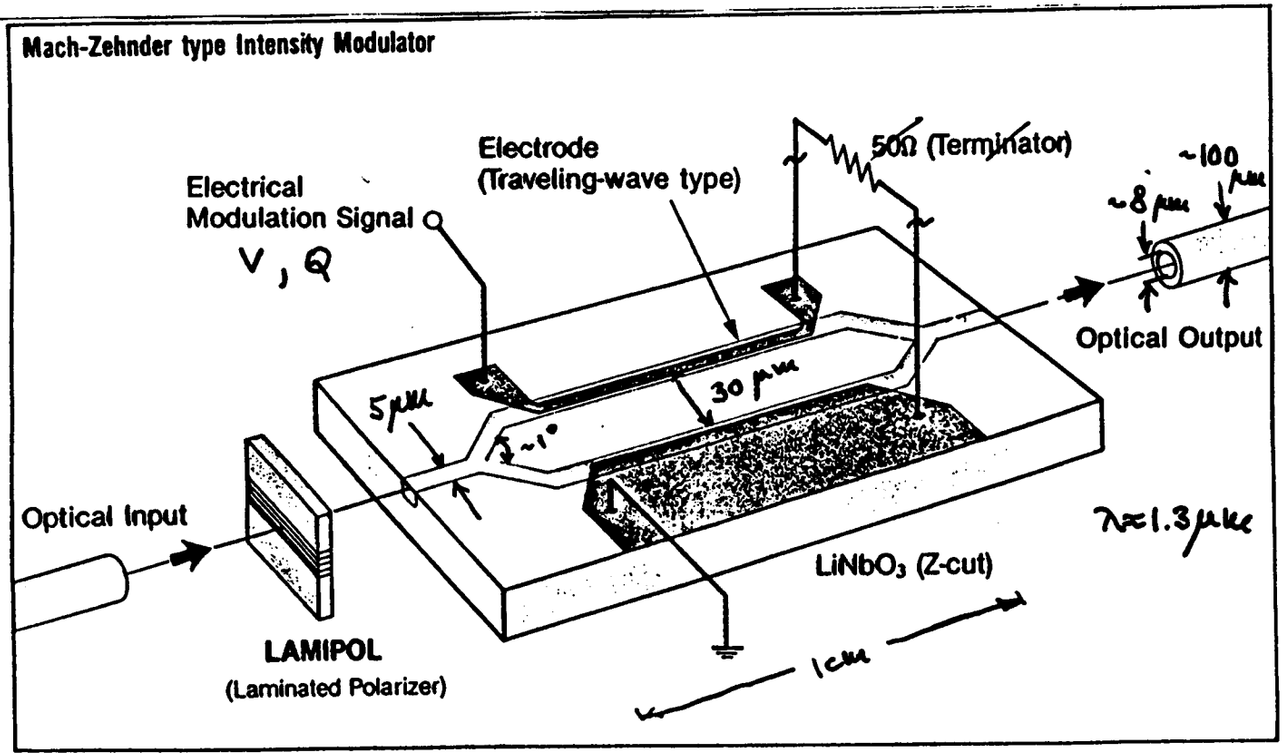
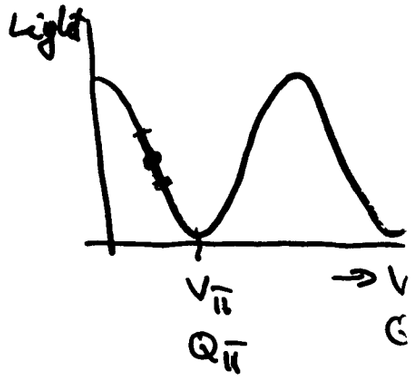
Electro-optical modulators





$V_{\pi} = 2-5$ volts

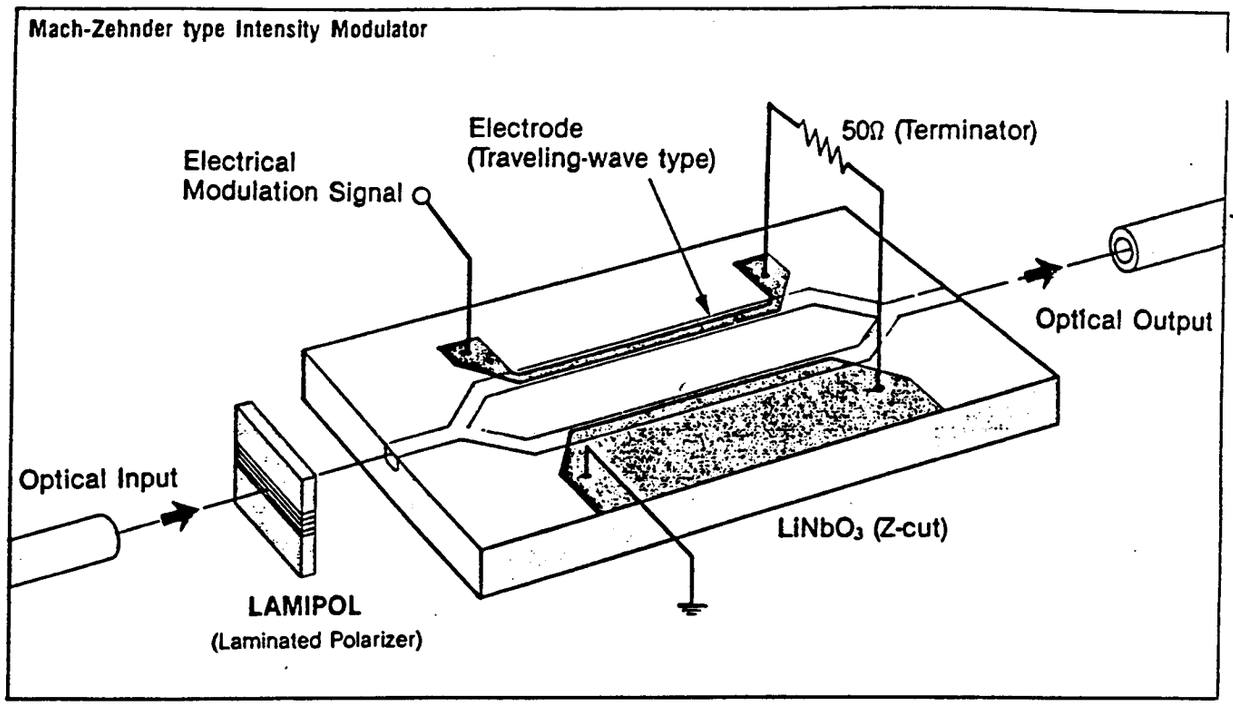
$Q_{\pi} \approx 20-40$ pico coulo

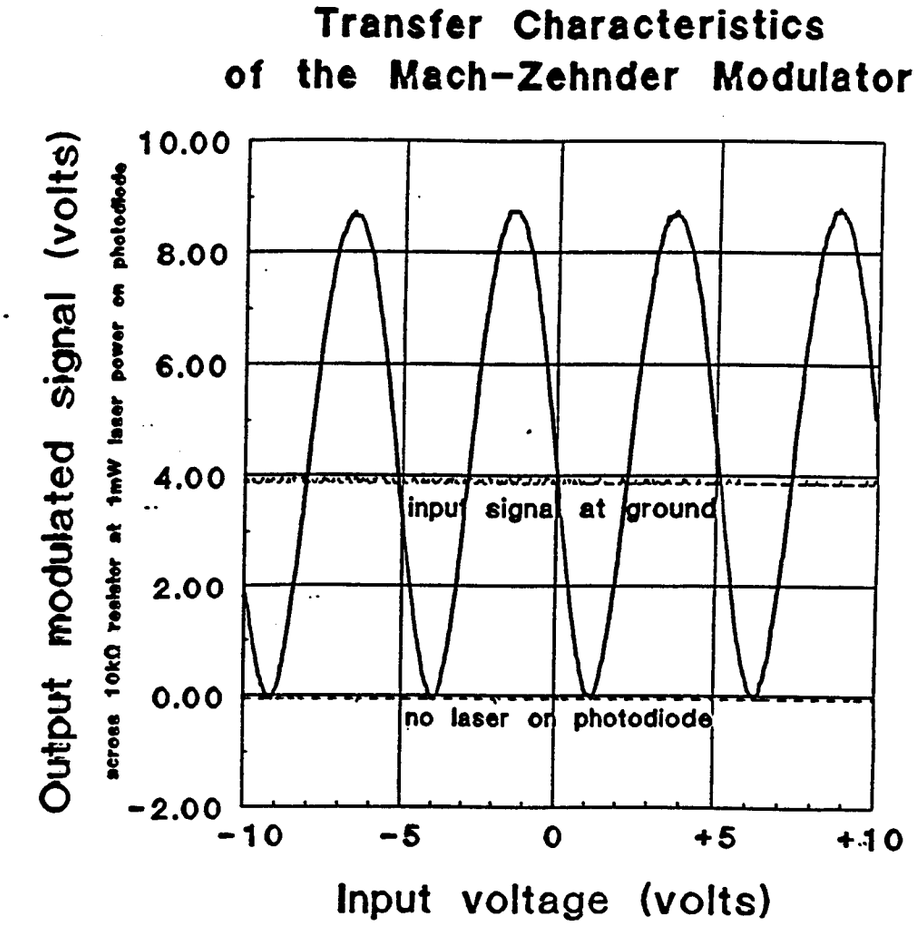
Noise ≈ 1fC − 4f

Dynamic range: $\sim 1-5 \times 10^3$

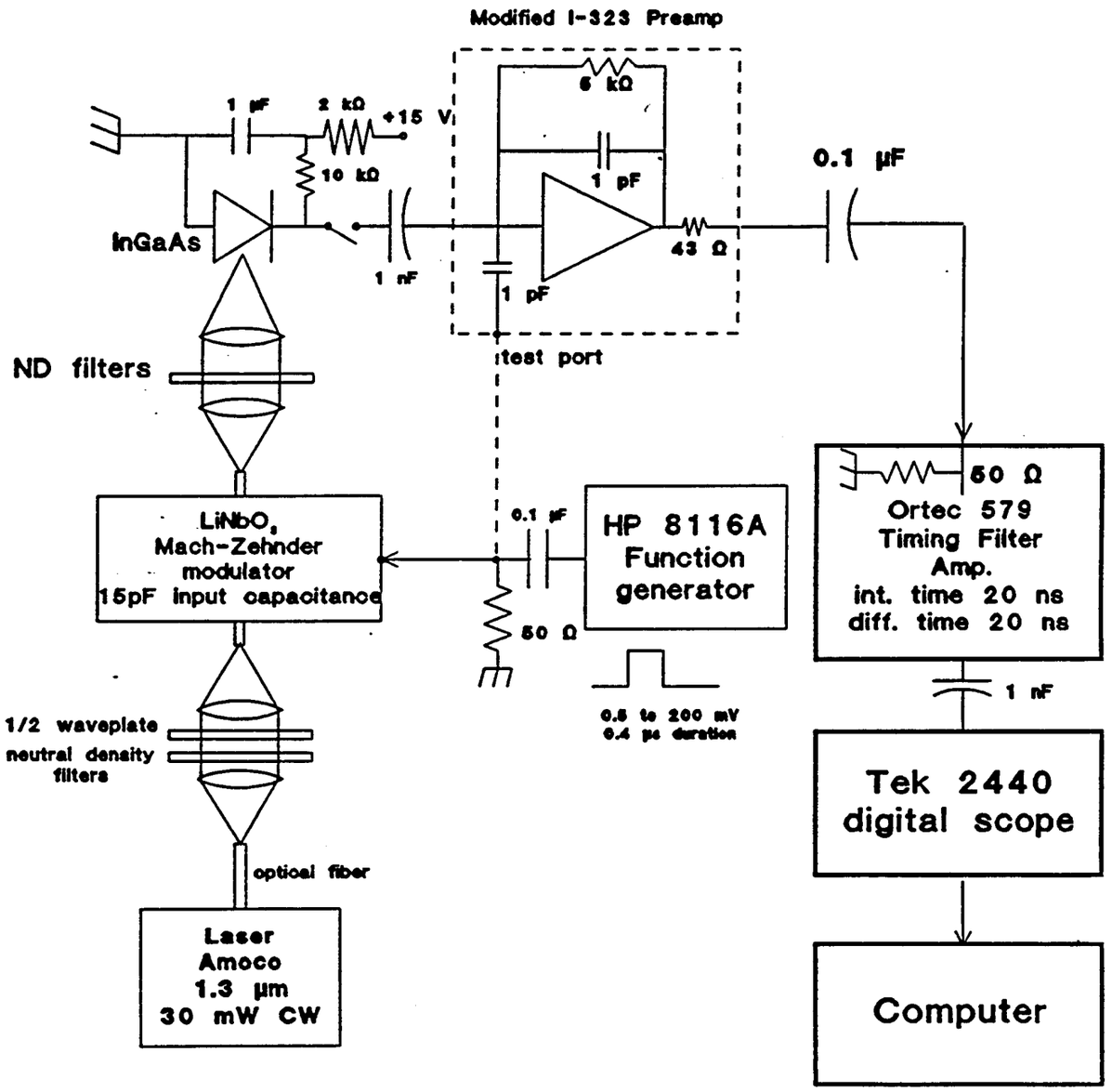
Index of refraction $\Delta n \propto E$

Phase shift $\Delta\phi \propto E$


Mach-Zehnder type Intensity Modulator
Electrical
Modulation Signal
Electrode
(Traveling-wave type)
50Ω (Terminator)
Optical Output
Optical Input
LiNbO3 (Z-cut)
LAMIPOL
(Laminated Polarizer)

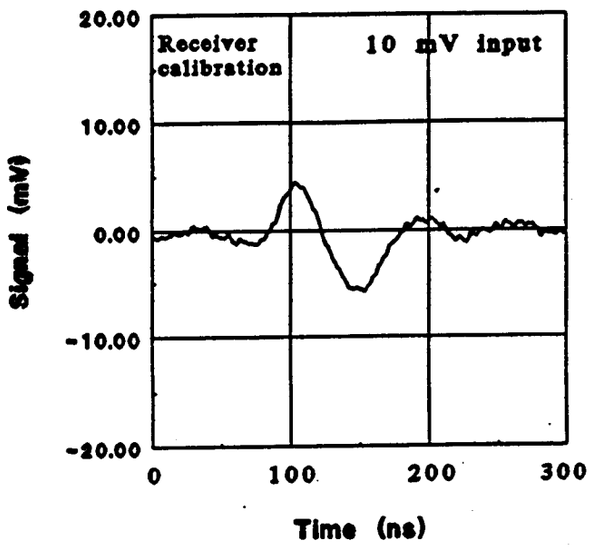

Transfer Characteristics
of the Mach-Zehnder Modulator
Output modulated signal (volts)
across 10kΩ resistor at 1mW laser power on photodiode
10.00
8.00
6.00
4.00
2.00
0.00
-2.00
input signal at ground
no laser or photodiode
-10
-5
0
+5
+10
Input voltage (volts)

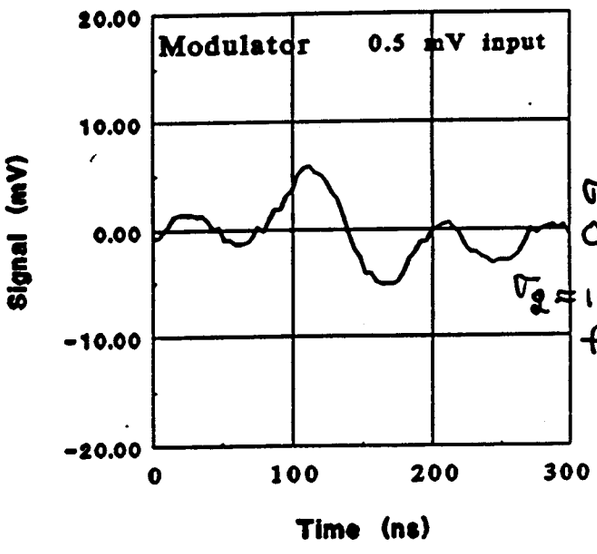
Experimental setup for noise measurements
Pulse shaping technique



Modulator-Receiver Response

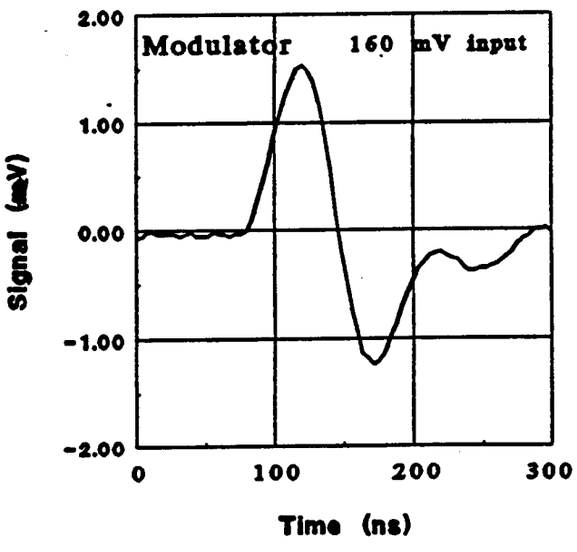
Pulse shaping: Ortec 579, $\tau_i = \tau_d = 20$ ns

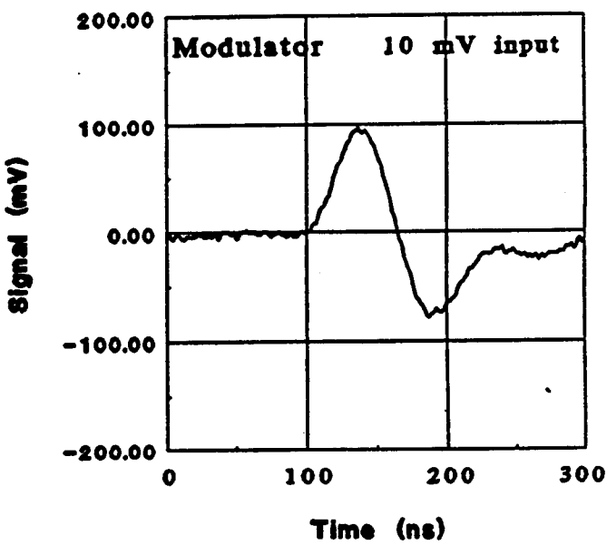




$\sigma =$ 0.1 mV

$\sigma_Q = 1-2$ fC

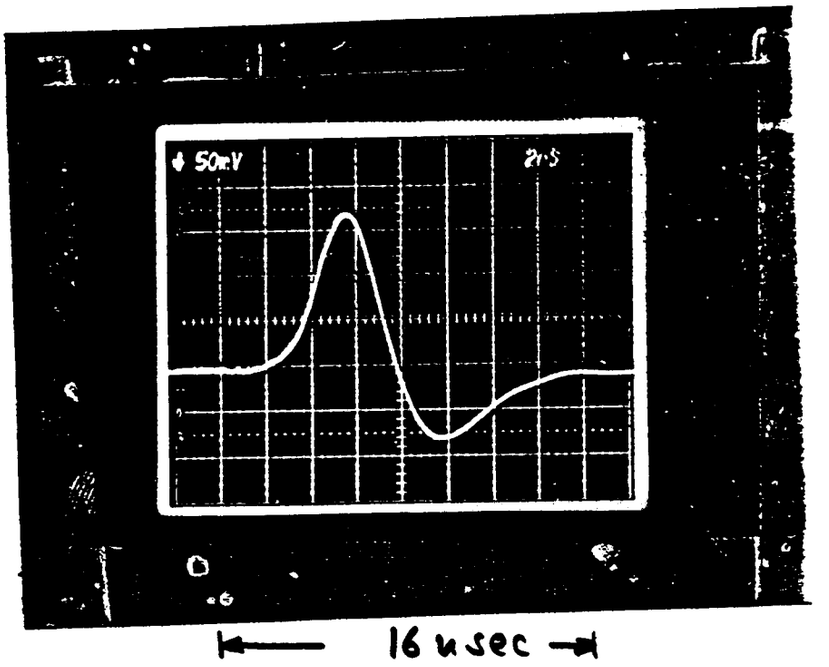




Modulator–Receiver Response

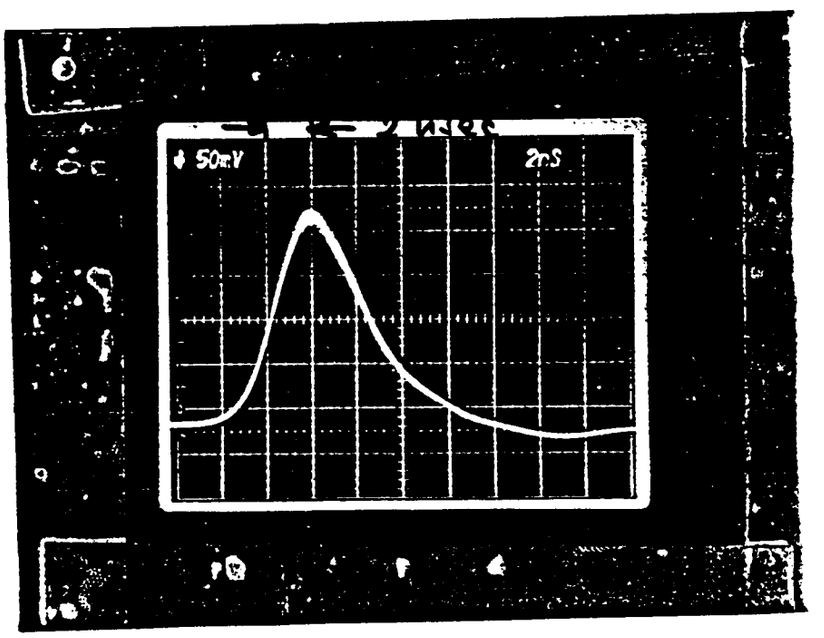
Fast pulse shaping, $T_i = T_d = 3$ ns

Receiver calibration −50 mV input



16 μsec

−50 mV, 6 μs pulse input to the modulator



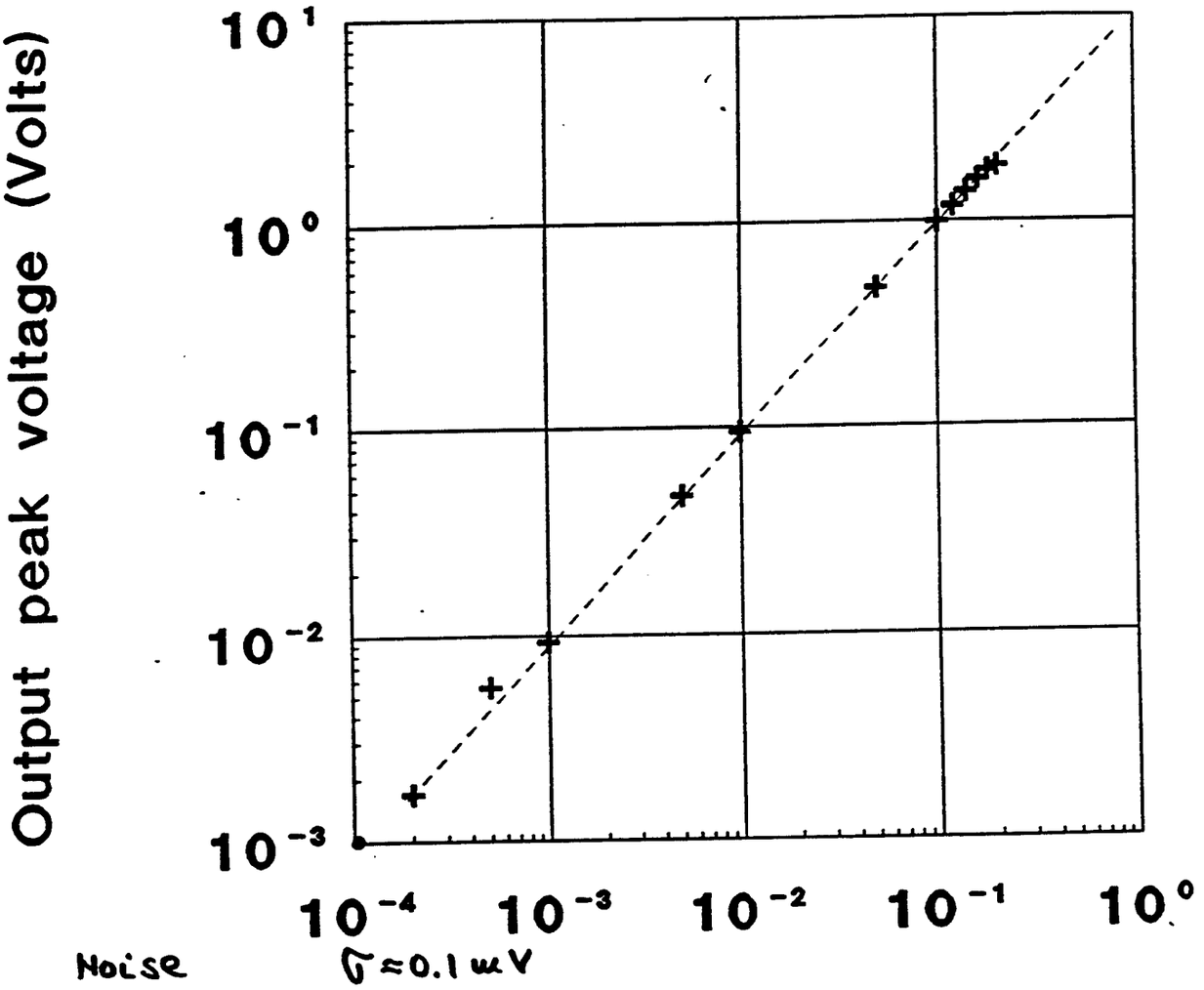
$\sigma_{in}(v) \approx 0.2\ mV$

$\sigma_{in}(q) \approx 4\ fc$

for $C_M \approx 10\ pF$

$C_D \approx 10\ pF$

Mach–Zehnder Modulator
Linearity at −3 dB bias point

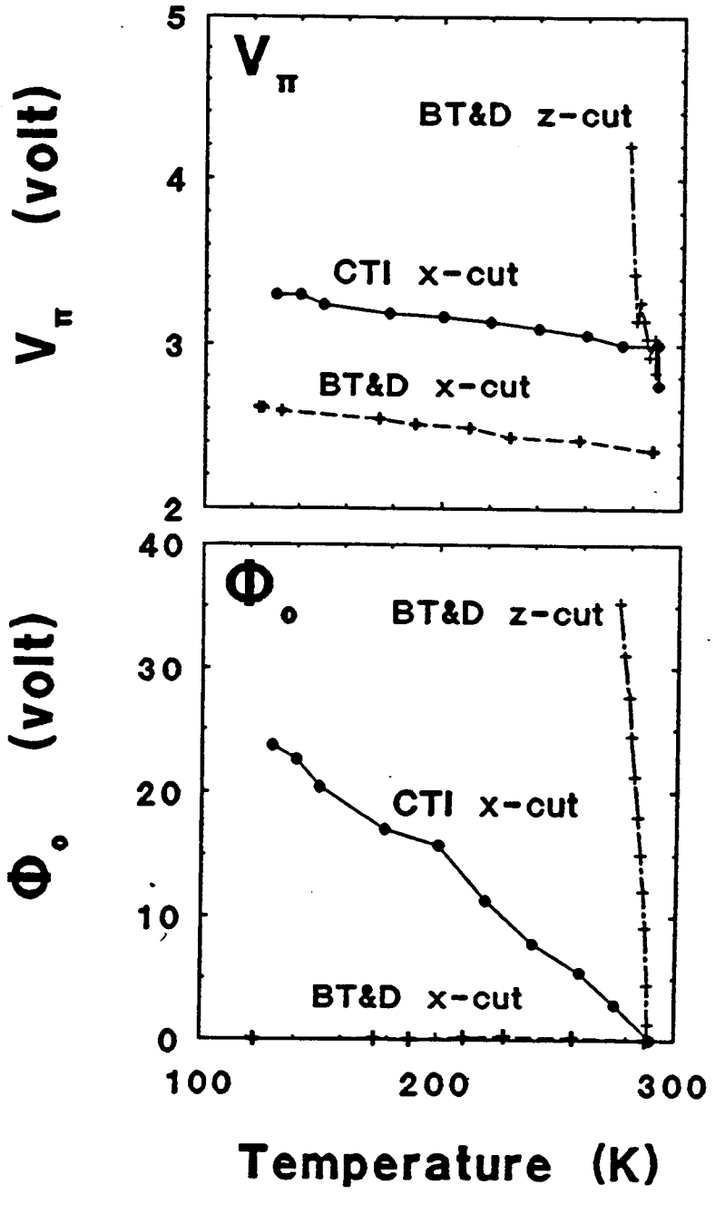


For 1% nonlinearity:

Dynamic range : $1-3 \times 10^3$ for $t_m = 35$ nsec

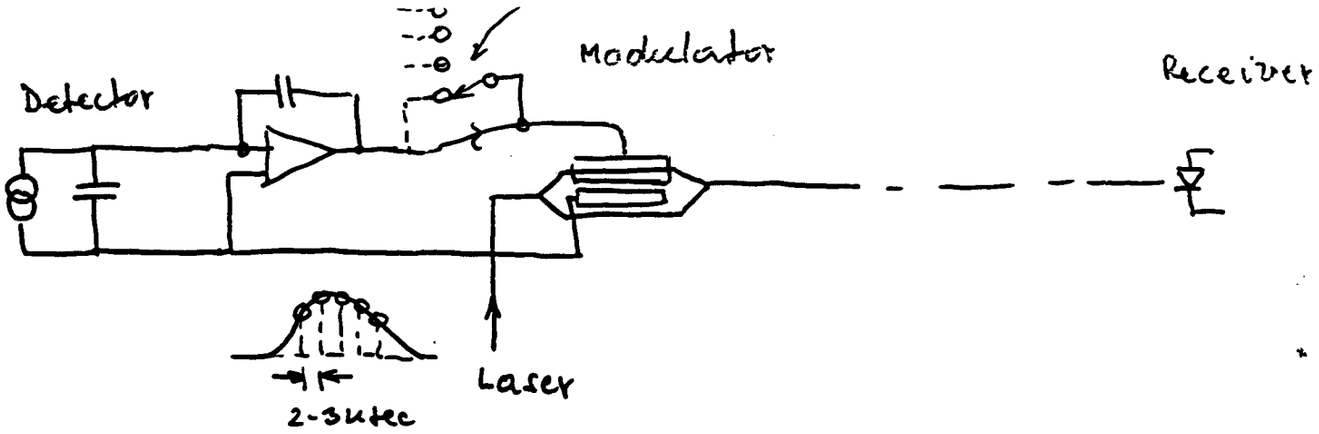
$$\frac{v_{max}}{\sigma_{in}(v)} = \frac{Q_{max}}{\sigma_{in}(q)} \approx 0.18 \sqrt{t_m \cdot n_0}$$

t_m: integration time; n_0: photoelectron rate

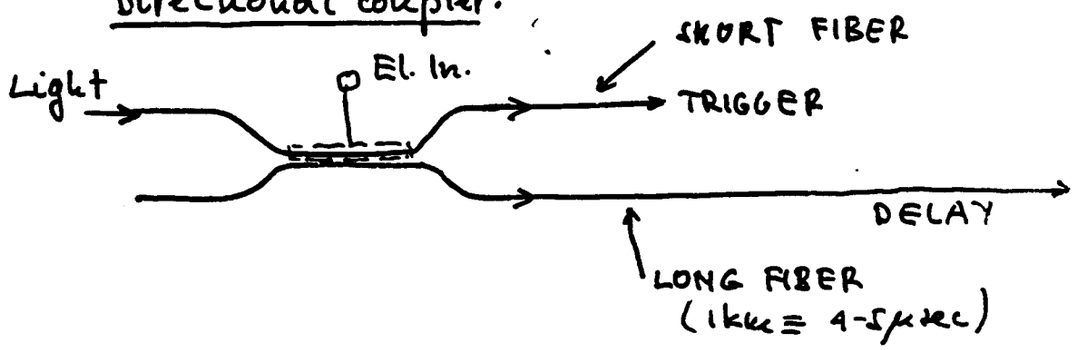


CLEO'91 Fig2.tc

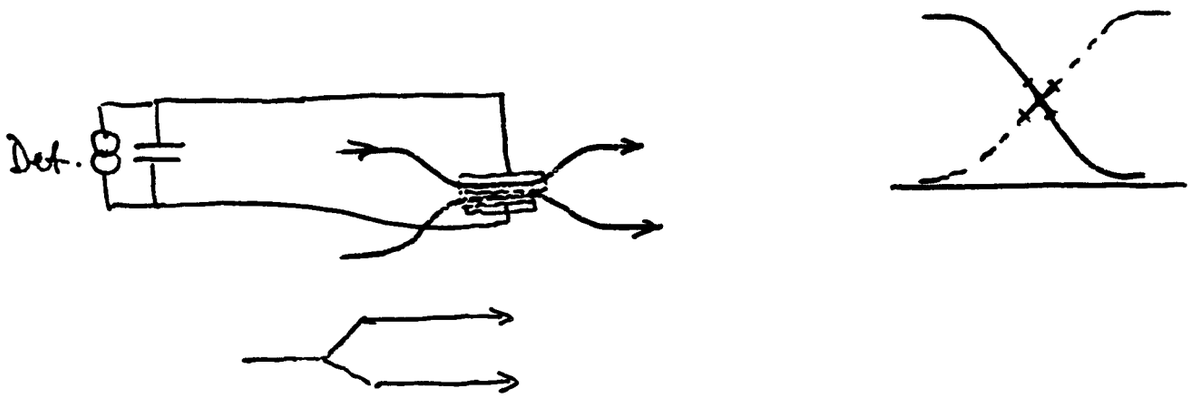
5/91 T.T.



Directional coupler:

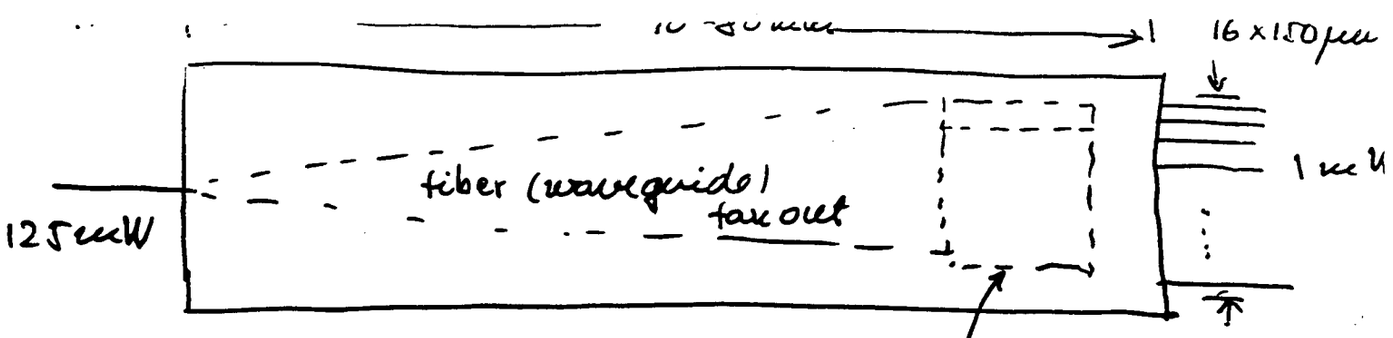


The ultimate:



Questions:

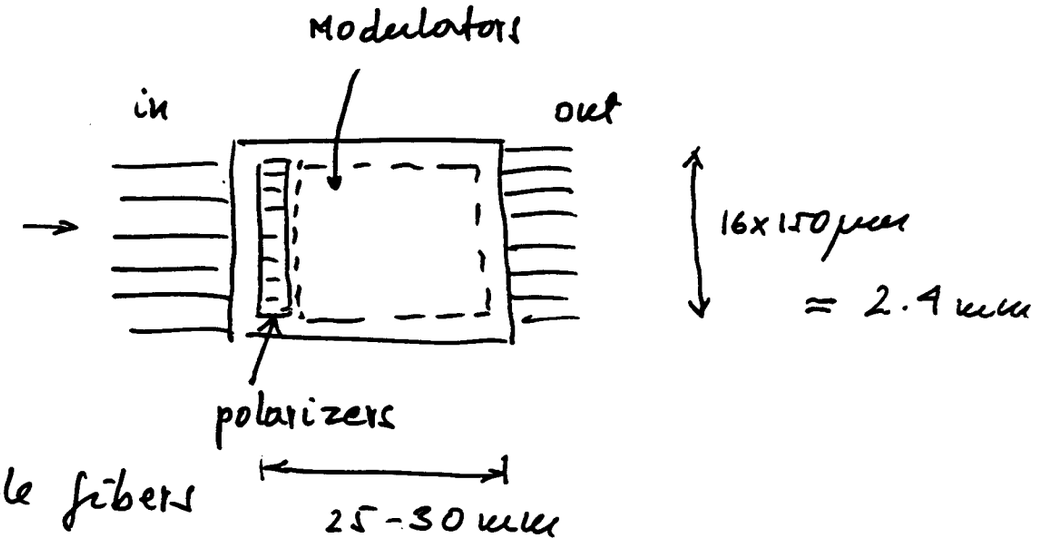
- stability of the bias point, process control
- fiber connections
  - rad. damage (neutrons), γs OK
  - power dissipation, (less of a problem)
- light generation and distribution



1 fiber in single mode polarization preserving

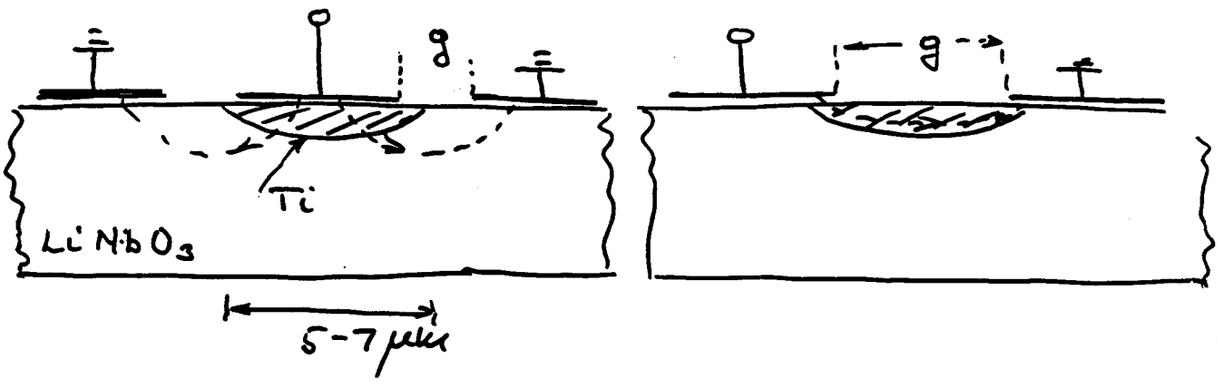
"on the chip light distribution"

2.



"off the chip light distribution"

Modulator Wave Guide

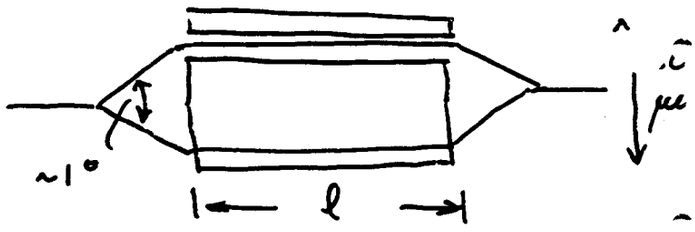


$$V_{\pi} = \lambda \frac{g}{\Gamma \ell} \frac{1}{n_e^3 r_{33}} \qquad E = \frac{V}{g\Gamma}$$

Γ = 0.2 – 0.3 E-field, Opt. field overlap

$r_{33} \approx 3 \times 10^{-11}$ m/V

$n_e \approx 2.2$



$V_{\pi} \approx 2.6$ V

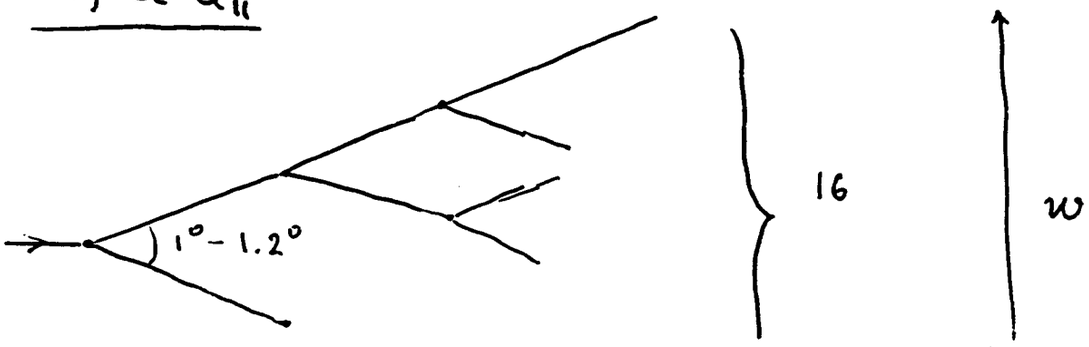
ℓ = 14 mm

$V_{\pi} \propto \frac{1}{\ell}$

$C_M \propto \ell$

Q_{π} independent of ℓ

$\Delta f \propto Q_{\pi}$



1) 16-channel modulator development
(AT&T)

2) Recent measurements:
- temperature dependence of the bias (BNL)

3) Future measurements:
- Finer points in noise measurements
- Long fibers and noise (BNL)

4) Questions to be solved:
- light generation and distribution
- fiber connections and handling

5) Connections and matching to the detector:
- minimum circuits between detector and modulator.

6) Bias point as processing in multi-channel devices (NRL)

Overall System Design/Cost of FNAL CAL Readout

W. Foster

FNAL Work on a Pipelined Digitization/Trigger System for the SDC

G. WILLIAM FOSTER October 30, 1990

Morris Binkley, John Elias, G. William Foster, Catherine Newman-Holmes, Dave Christian
Al Bambaugh, Jim Hoff, Ray Yarema, Tom Zimmerman

① GENERAL APPROACH
- DIGITAL PIPELINE
- SINGLE-LEVEL TRIGGER

② FIBER TRACKER
- LOGIC DESIGN
- PACKAGING & COST

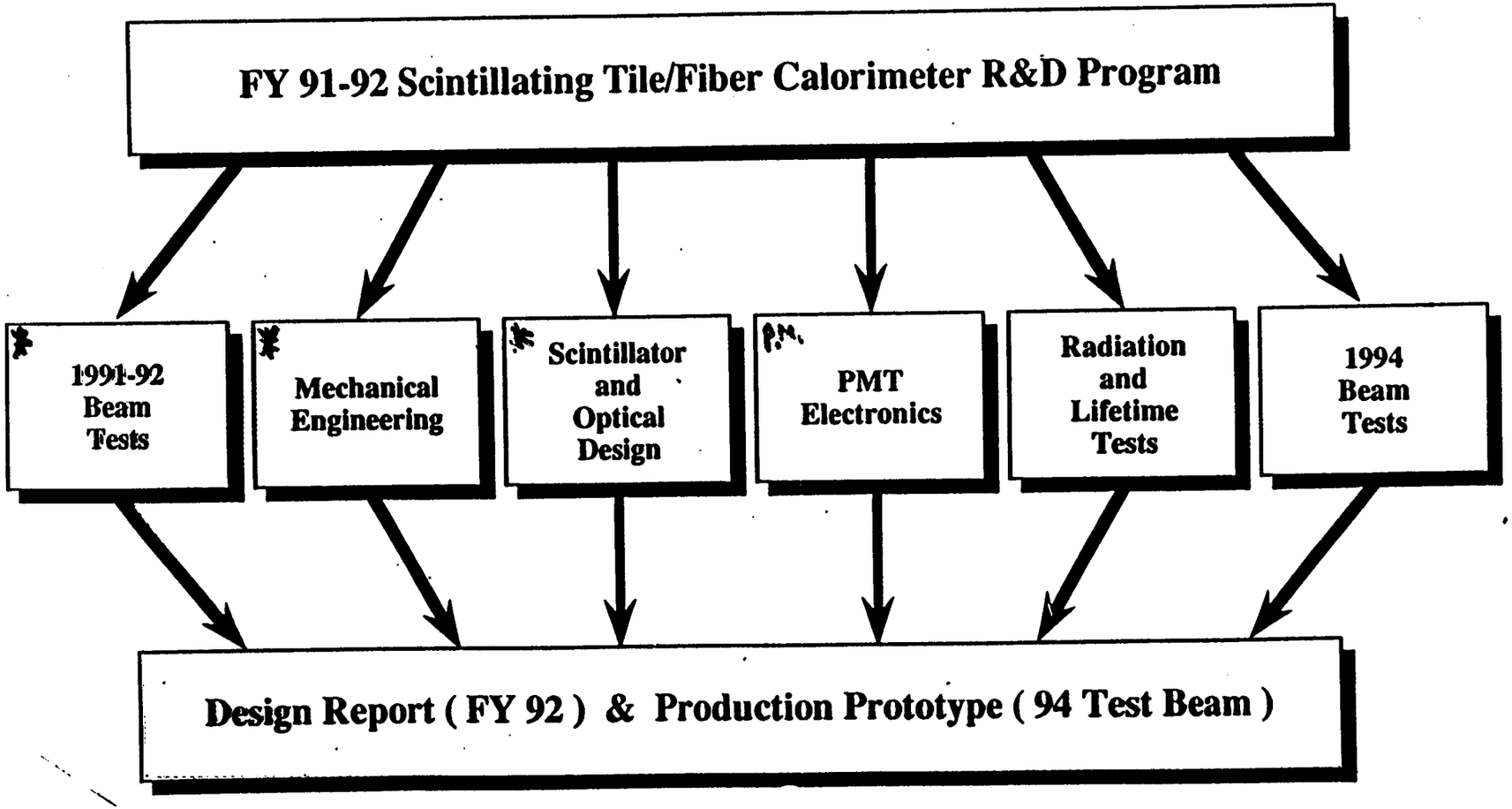
③ PHOTOTUBE DIGITIZER
- GATED 16ns INTEGRATOR
- COMMERCIAL FADC
- FLOATING-POINT OUTPUT EACH CROSSING

④ PIPELINED TRIGGER
- FLOATING-POINT E_T SUMS
- FULL ELECTRON I.D. (TRACK, $\frac{EM}{HAD}$, ISOLATION

⑤ I.C.'S & SYSTEM ENGINEERING IN PROGRESS AT

Fermilab

SDC



Fermilab

Phototube Testing and Procurement Program

SDC

FY-91

Beam tests and digitization/base design using existing PM Tubes. Tests of currently available PMT's which approximately meet our requirements (e.g. Phillips XP1922). Preliminary specifications written and circulated to vendors.

FY-92

Obtain samples from vendors, (Burle, Phillips, EMI, Hamamatsu, USSR). Establish testing procedures and apparatus. Revise specification on basis of sample lots.

FY-93

Obtain approximately 500 PMT's each from four vendors. Begin burn-in (500 device years/vendor). Setup production test apparatus. Finalize bid specification.

FY-94

Select final vendor. Begin delivery and testing of 40K PMT's.

Low gain 19 mm (3/4") diameter tube

XP1922

MECHANICAL DATA

Dimensions in mm

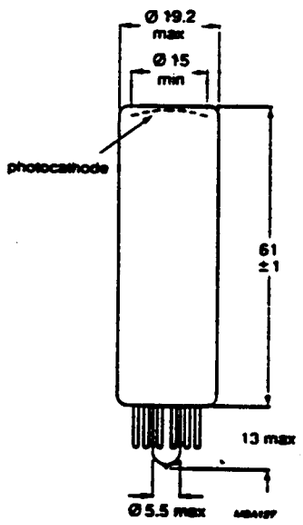
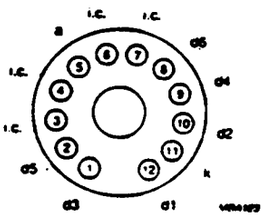


Fig.5 Mechanical outline.



i.c. = internally connected

Fig.6 Pin connections.

Base 12-pin all glass
Net mass 16 g

ACCESSORIES

Socket	FE1004
Mu-metal shield	56689

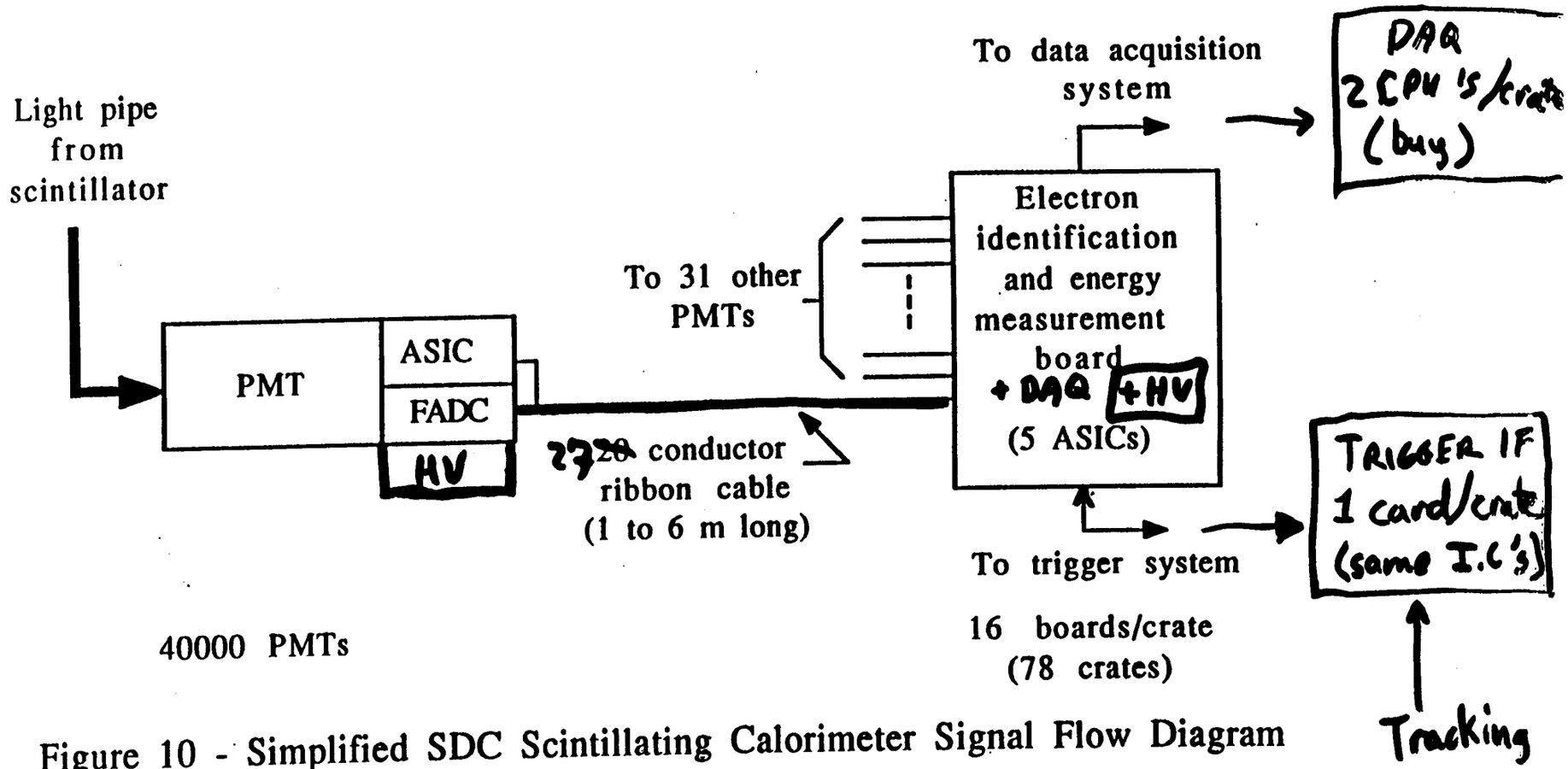


Figure 10 - Simplified SDC Scintillating Calorimeter Signal Flow Diagram

TEST STAND (& system debug)

In the all-digital system, there are essentially two (2) components:

- a modular PMT Base/readout assembly
- an all-digital Trig/DAQ/HV control board

"change the PMT/base and solve the problem"
OR
"swap the readout card"

You don't have problems like:

"well, the tube looks OK in the trigger sums but the readout and calibrations look fritzed....."

Fermilab

PMT High Voltage/Distribution and Base Mechanics R&D Program

SDC

FY-91

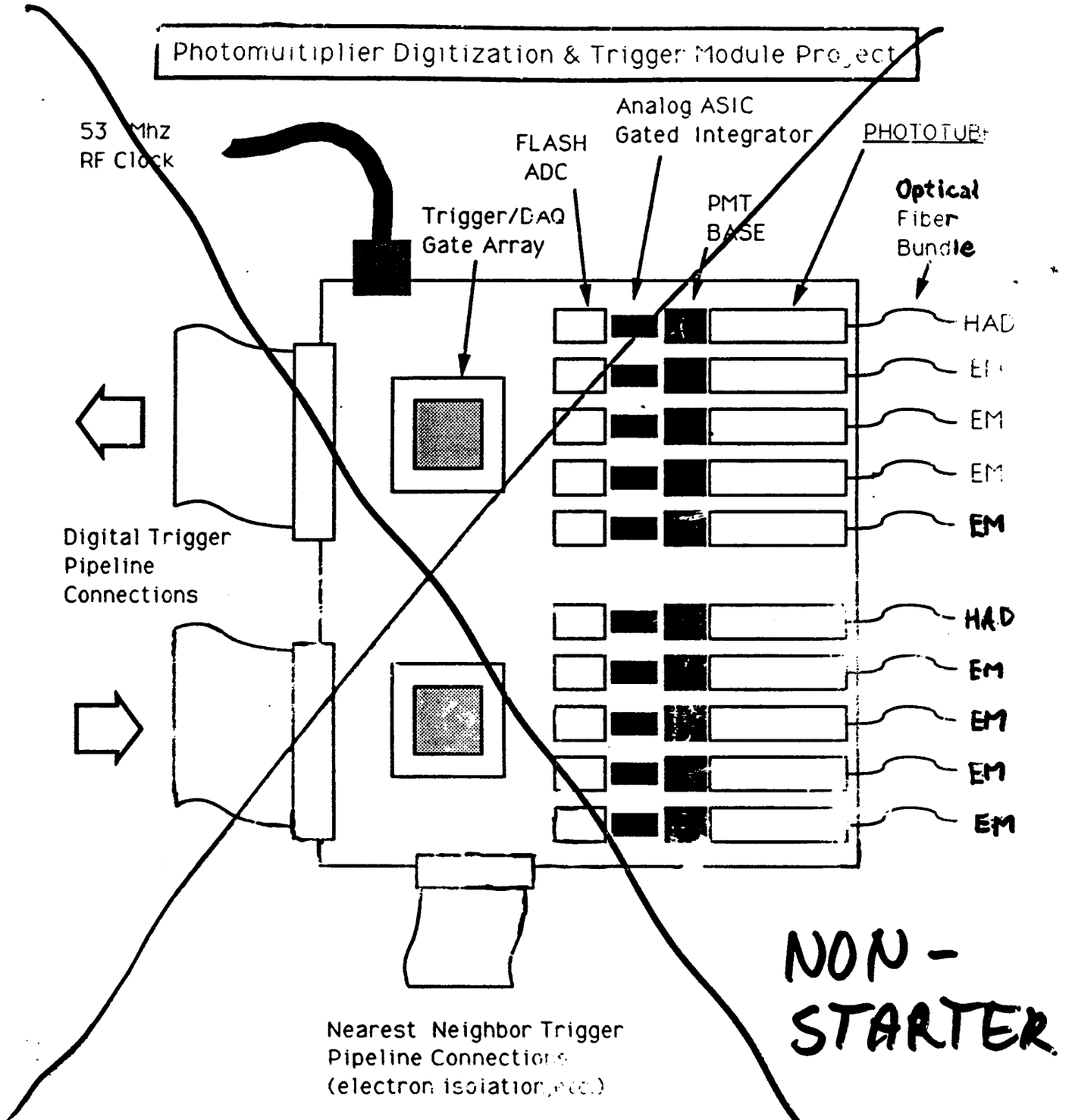
Prototype both "Standard" and "Charge Pump" base designs, to be used in test beam. Test noise performance with low gain PMT's (~5000 electrons/LSB). Test feasibility of charge pump transients during beam abort gap.

Establish system costs for:

1. "Standard" base design with bulk HV (CDF Model)
2. "Standard" base design with distributed HV (Le Croy Model)
3. "Charge Pump"base/HV supply. (Zeus Model)

Assemble wedge PMT/Electronics mockup to study fiber routing, PMT mechanics, PMT replacement, cable routing, board connections, cooling, etc.

Photomultiplier Digitization & Trigger Module Project



Design Goals:

Dynamic Range: 20 Bits Cost: < $200 / Channel
Accuracy: 9 Bits Power: 600 mw/Channel

⇨ ALL-DIGITAL TRIGGER BASED ON SAME INFO AS OFFLINE ⇦

Fermilab

PMT High Voltage/Distribution and Base Mechanics R&D Program

SDC

FY-92

Prototype and burn-in testing of 100~1000 PMT charge pump bases. Revise charge pump base design based on burn-in. Evaluate performance of charge pump and resistive bases with "SDC" PM Tubes. Finalize base mechanical design to optimize ease of replacement (Quick connects for optical, electronics, and cooling) working with the Scintillating Tile/Fiber Calorimetry group.

FY-93

Base/HV design decision. Begin burn-in of ~2000 channels of final design in conjunction with PMT burn-in testing.

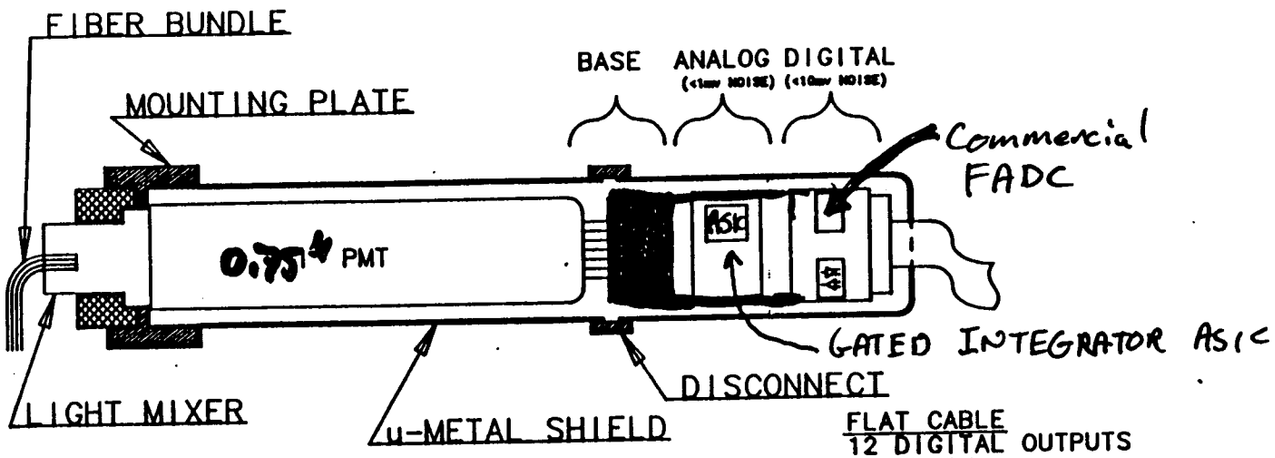
FY-94

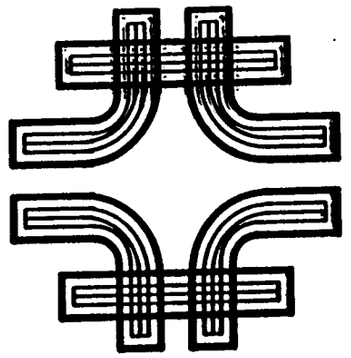
Begin procurement and testing of 40K PMT HV and bases.

REV.	DESCRIPTION	DRAWN	DATE
		APPD.	DATE

229

PHOTOTUBE MECHANICS
(20,000 PCS. TOTAL)



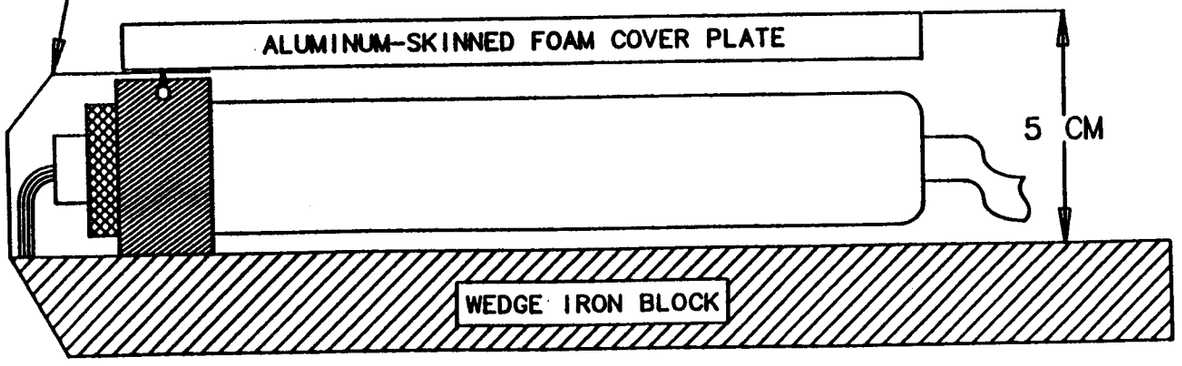


FLAT CABLE

12	DIGITAL OUTPUTS
1	CLOCK
3	POWER
2	CALIB
2	SPARE
20	

+7 HV CONTROL
27 conductors

.05" WIDE .025" PITCH



ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY. REQ.

PARTS LIST

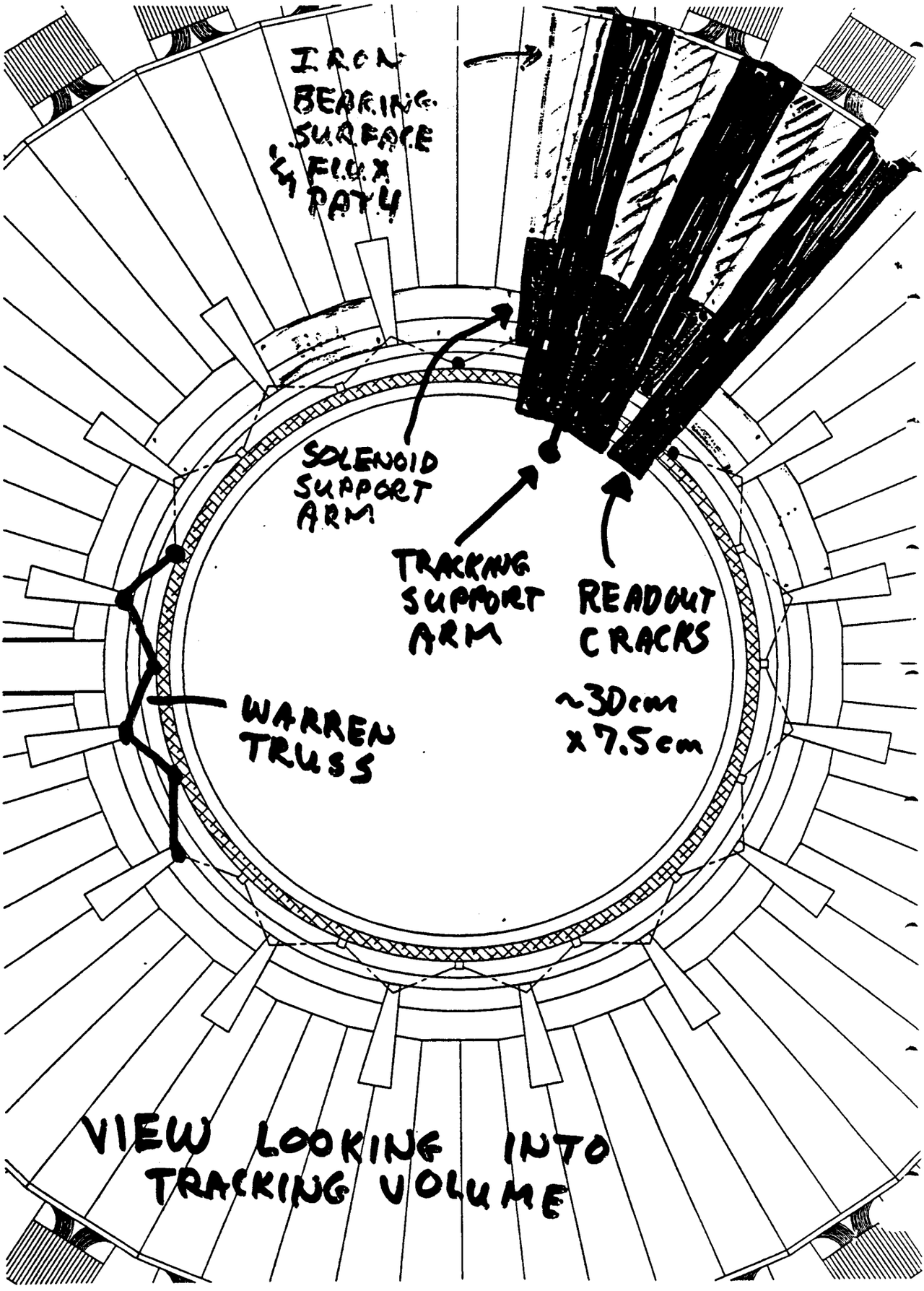
UNLESS OTHERWISE SPECIFIED	ORIGINATOR	G W FOSTER
FRACTIONS DECIMAL ANGLES	DRAWN	BRIAN LEE HAHN 10/18/9
	CHECKED	
1. BREAK ALL SHARP EDGES 1/64 MAX.	APPROVED	
2. DO NOT SCALE DWG.	USED ON	
3. DIMENSIONING IS ACCORD WITH ANSI Y14.5 STD'S	MATERIAL-	
MAX. ALL MACHINED SURFACES		

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

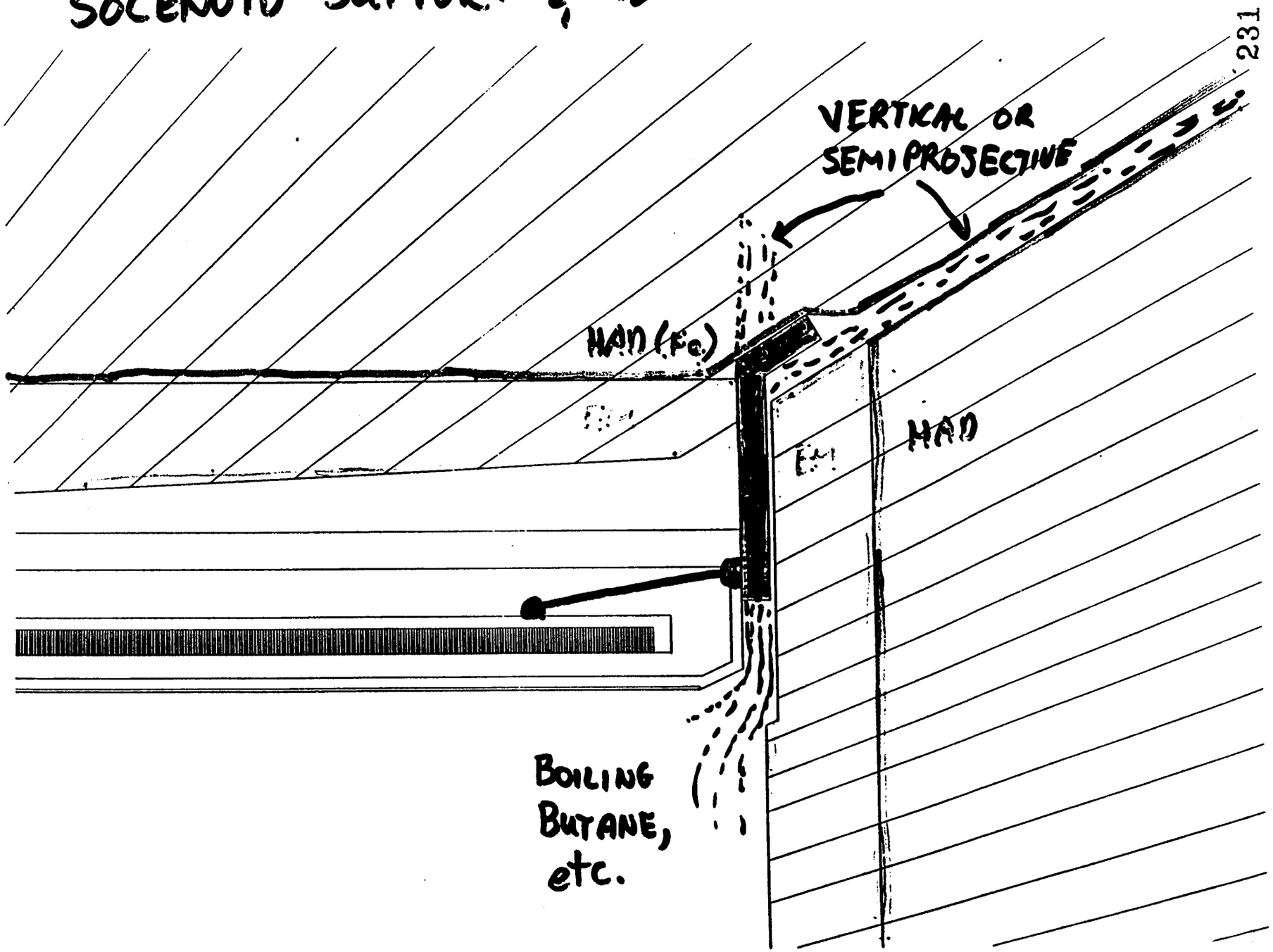
PHOTOTUBE MECHANICS

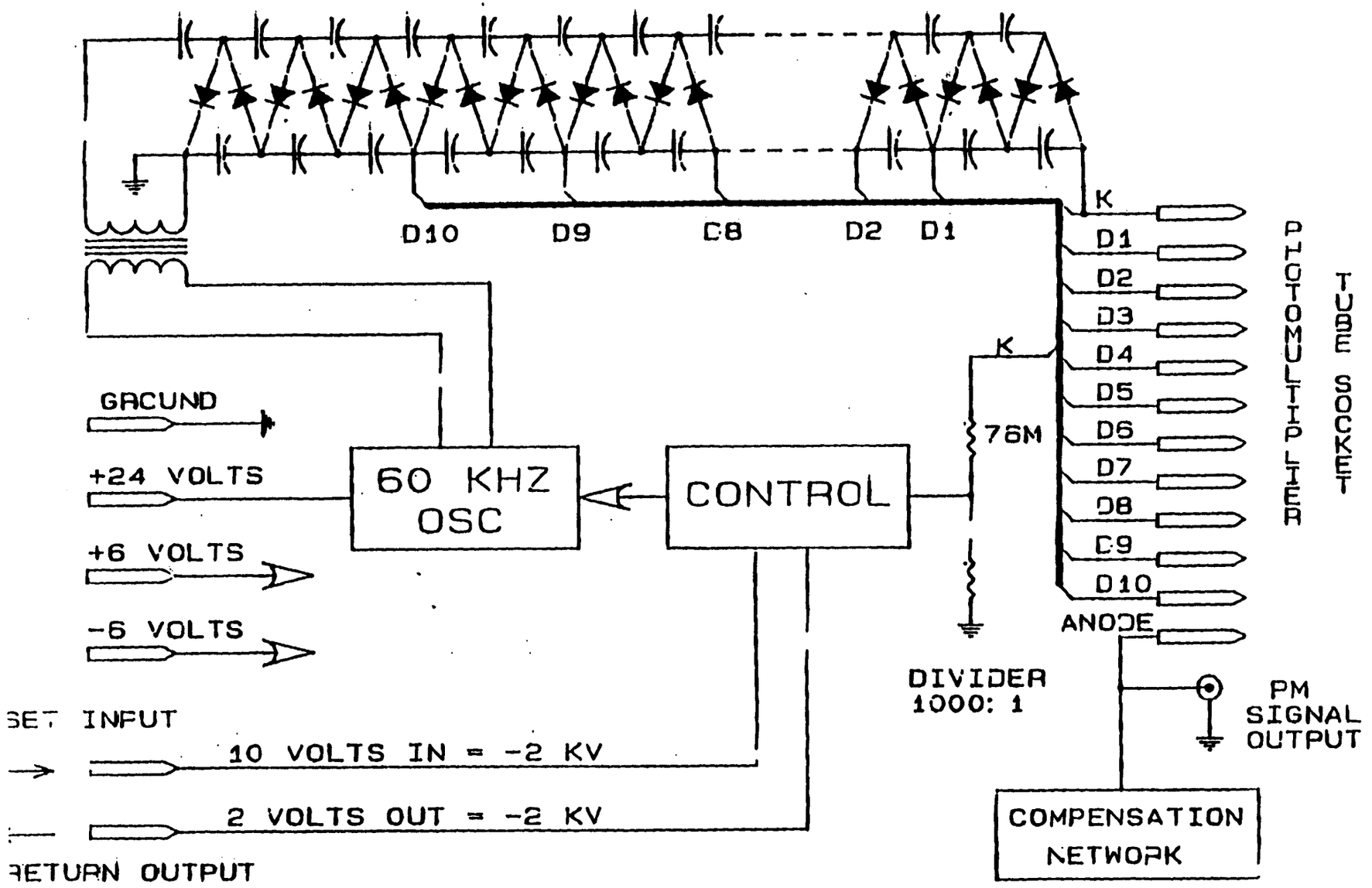
SCALE	DRWG SIZE	DRAWING NUMBER	REV.
3/2	C		

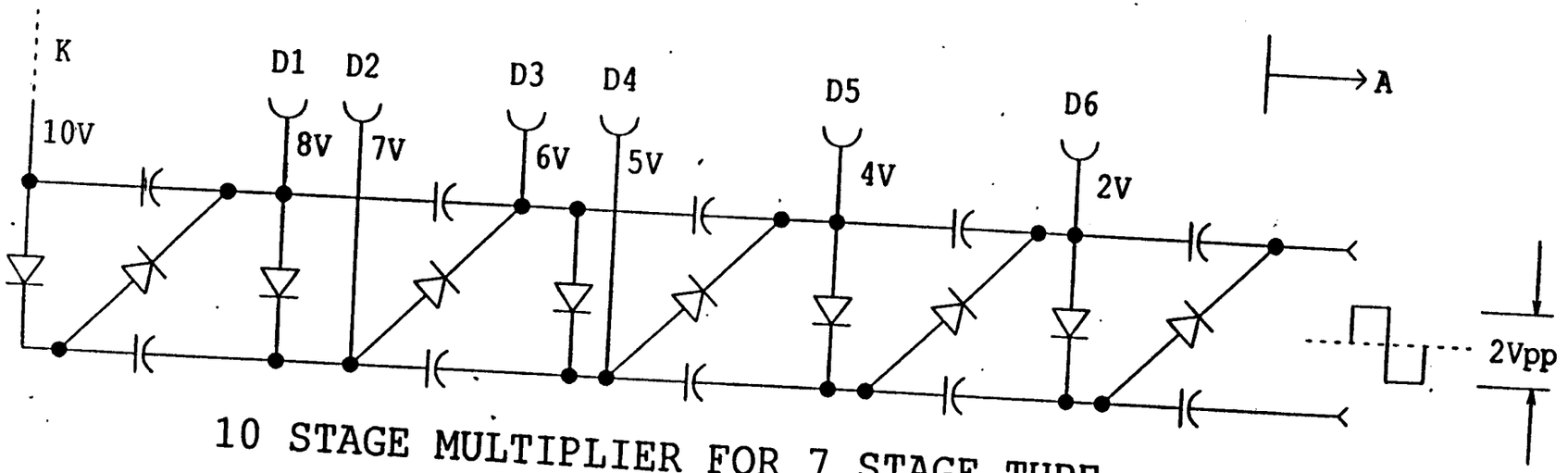
IDEAS LEVEL 4.0 USER:


IRON BEARING SURFACE & FLUX PATH
SOLENOID SUPPORT ARM
TRACKING SUPPORT ARM
READOUT CRACKS
~30cm x 7.5cm
WARREN TRUSS
VIEW LOOKING INTO TRACKING VOLUME

SOLENOID SUPPORT & REMOVAL

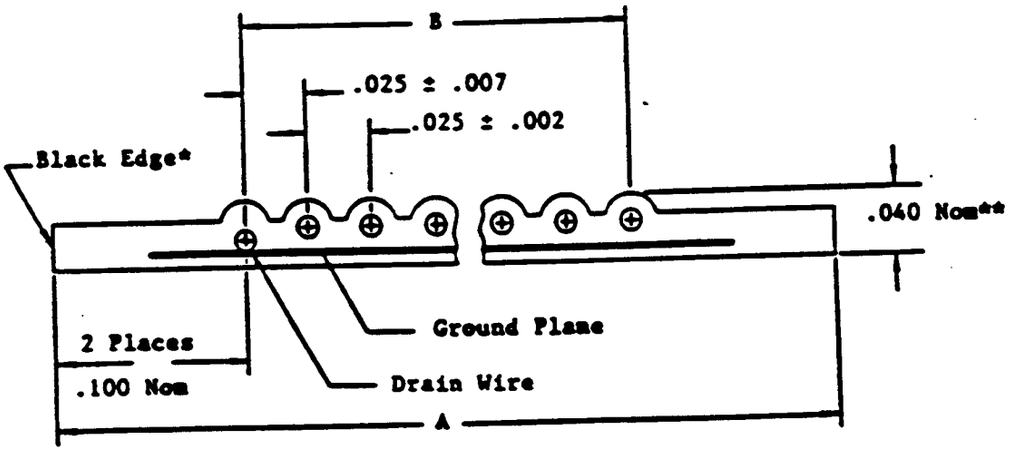



K
D10
D9
C8
D2
D1
D1
D2
D3
K
D4
D5
GRCUND
76M
D6
+24 VOLTS
60 KHZ
OSC
CONTROL
D7
D8
+6 VOLTS
C9
D10
-6 VOLTS
ANODE
DIVIDER
1000: 1
PM
SIGNAL
OUTPUT
SET INPUT
10 VOLTS IN = -2 KV
2 VOLTS OUT = -2 KV
RETURN OUTPUT
COMPENSATION
NETWORK
PHOTOMULTIPLIER TUBE SOCKET



10 STAGE MULTIPLIER FOR 7 STAGE TUBE
(BLEEDER RESISITORS NOT SHOWN)

.025" CENTER GROUND PLANE CABLE	November 17, 1987
PART NUMBER 133-30XX-XXX	
PRELIMINARY PRODUCT SPECIFICATION	Page 2 of 2



Product shown above is with a drain wire.
* Red edge for product without a drain wire.
** .045 nom for Qwik Strip.

3.0 Order Information

PART NUMBER	NO COND	WIDTH 'A' INCHES	SPAN 'B' INCHES
133-3012-020	20	.675	.475 ± .005
133-3012-026	26	.825	.625 ± .005
133-3012-034	34	1.025	.825 ± .005
133-3012-040	40	1.175	.975 ± .006
133-3012-050	50	1.425	1.225 ± .006
133-3012-060	60	1.675	1.475 ± .006

Above Table — Series 133-3012-0XX: Product with a drain wire as shown above.
Series 133-3011-0XX: Product without a drain wire.
Qwik Strip — Series 133-3014-0XX: Product with a drain wire.
Qwik Strip — Series 133-3013-0XX: Product without a drain wire.

01061

CABLE TEST SUMMARY

January 23, 1989

R. Yarema

A compact, flexible, 64 conductor, flat cable with a 25 mil pitch is needed to bring signals from a preamplifier card on a detector to an amplifier-shaper-discriminator card. A flat cable is desired for ease of stacking and routing. To provide maximum density, all conductors in the cable are to be used as differential pairs (no grounds). Flat cable characteristics are not typically specified for SSS (signal-signal-signal) applications. A series of tests were performed to measure and compare cables driven in a differential mode without interleaved ground conductors.

All cable samples tested were 10' long. A pair of conductors were driven differentially and crosstalk was measured differentially on an adjacent pair. Conductor pairs were near the center of the cable. The driven pair receiving end, and the crosstalk forward and backward ends were terminated in the cable characteristic impedance. If a ground plane was present, it was connected to the scope ground at the receiving end. The cable impedance, attenuation, and crosstalk were measured with a 2 volt input pulse that had a rise time and fall time (10-90%) of 5ns, and a flattop of 5ns. The cable rise time measurement was made at the receiving end with a 50 ns wide, 2 volt input pulse that had a rise time of 1.7 ns.

Cable Type	Impedance	Attenuation••	Forward Crosstalk◊	Reverse Crosstalk	Risetime	Cost (5000')
1	140 ohms§	9%	2.3%	5.1%	3.7 ns	1.16/ft*Δ
2	116	6%	3.0%	3.8%	2.9 ns	1.76/ft*
3	105	10%	2.0%	3.2%	2.7ns	2.36/ft*
4	92	23%	7.5%	1.9%	6.6ns+50ns tail	2.16/ft*
5	139§	6%	2.8%	5.8%	3.2ns	.77/ft
6	115	6%	3.8%	4.4%	2.8ns	2.28/ft
7	105	11%	3.1%	4.2%	3.0ns	1.89/ft
→ 8	100	11%	0.7%	4.2%	2.0ns	1.94/ft
9	142	5%	0.6%	2.2%	2.0ns	15.36/ft
10#	100	12%	0.2%	0.1%	1.8ns	9.54/ft*
11#	127	7%	1.2%	1.6%	3.0ns	.90/ft
12#	158	6%	3.6%	4.8%	2.5ns	≈5.00/ft

Notes:
- * Prices are for cables with less than 64 conductors.
- Δ Cable #5 with 64 conductors is a less expensive choice.
- # These cables do not have a 25 mil pitch.
- ◊ Forward crosstalk is directly proportional to cable length and increases with faster signal rise times.
- •• Attenuation is directly proportional to cable length.
- § Impedance changes with proximity to other cables and ground plane.

Cable Types Tested

1) CW Industries, 25 mil pitch, 50 cond., PVC, #30 AWG, stranded, unshielded
2) CW Industries, 25 mil pitch, 50 cond., PVC, #30 AWG, stranded, Cu tape 1 side
3) CW Industries, 25 mil pitch, 50 cond., PVC, #30 AWG, stranded, Cu tape 2 sides
4) CW Industries, 25 mil pitch, 50 cond., PVC, #30 AWG, stranded, CHO-FLEX 2 sides
5) Spectra-strip, 25 mil pitch, 64 cond., PVC, #30 AWG, solid, unshielded, #1913003-064
6) Spectra-Strip, 25 mil pitch, 64 cond., PVC, #30 AWG, solid, Cu CHO-JAC #022-26
7) Spectra-Strip, 25 mil pitch, 64 cond., PVC, #30 AWG, solid, Al CHO-JAC #021-26
→ 8) Spectra-Strip, 25 mil pitch, 64 cond, PVC,#30 AWG, solid,w/gnd plane #133-3013-064
9) Gore, 25 mil pitch, 50 cond., Teflon, #30 AWG, stranded, w/gnd plane
10) Gore, 40 mil pitch, 22 twisted pairs, Teflon, #30 AWG, stranded, #A04B060/24
11) Belden Vari-Twist, 50 mil pitch, 32 twisted pair, PVC, #28 AWG, stranded, #9V28064
12) Ansley (Nevis style), 33 mil pitch, 64 cond., polyethalene, #30, solid (normally used with interleaved and end ground wires to control cable characteristics).

The Spectra-Strip cable is particularly attractive for detector signals from E-771 for several reasons. First the cable has relatively good high frequency characteristics. Second the cost of $2.00/foot is reasonable. Third, the imbedded ground plane provides controlled cable impedance and shielding. Fourth, the cable is quite flexible and is relatively small. And last, the cable is easily mass terminateable with standard connectors from several different manufactures. Therefore several additional tests were done.

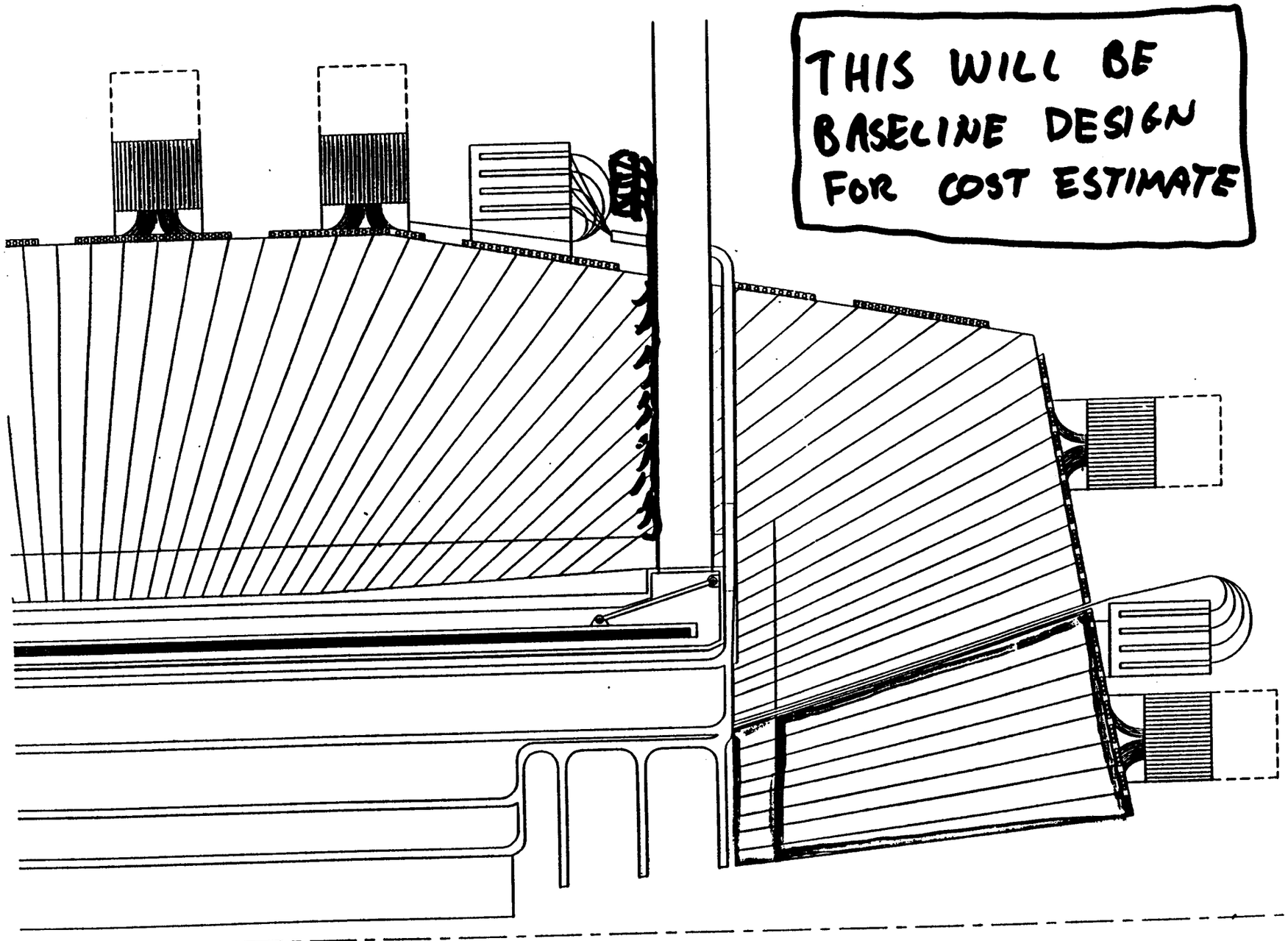
A test was done with 2 Spectra-Strip ground plane cables stacked to investigate multiple cable bundles. With 2 cables, the forward crosstalk dropped to from 0.7% to 0.4%, while all of the other reported characteristics remained unchanged.

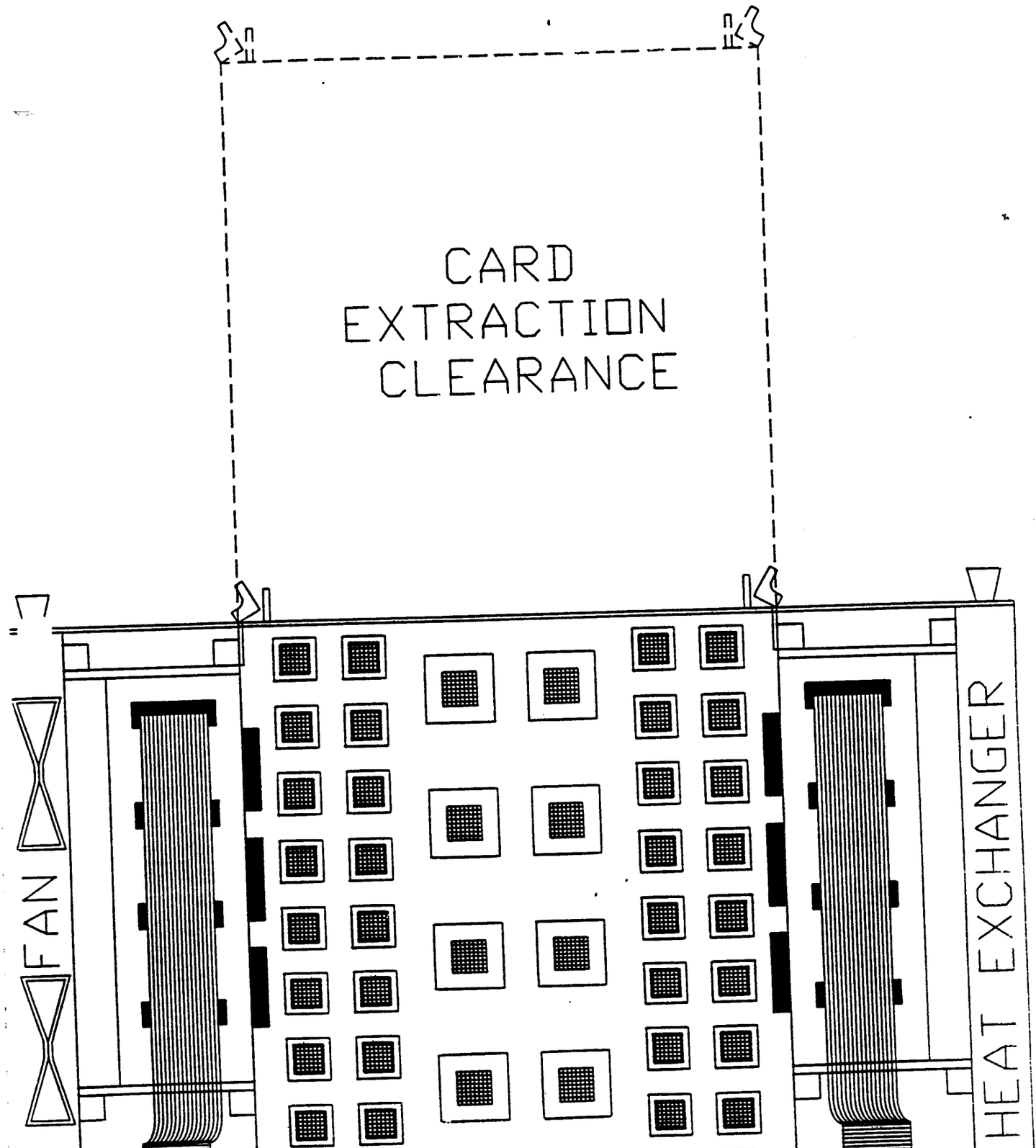
Another test was performed in which the differential output from a E-771 preamp prototype was used as the test pulse into a single piece of Spectra-Strip ground plane cable. The pulse was about 30ns baseline to baseline with a rise time of about 10ns and a fall time of about 15ns. With the preamp input, attenuation over 10 feet of cable was 7.4%, forward crosstalk was 0.4%, and reverse crosstalk was 4.2%.

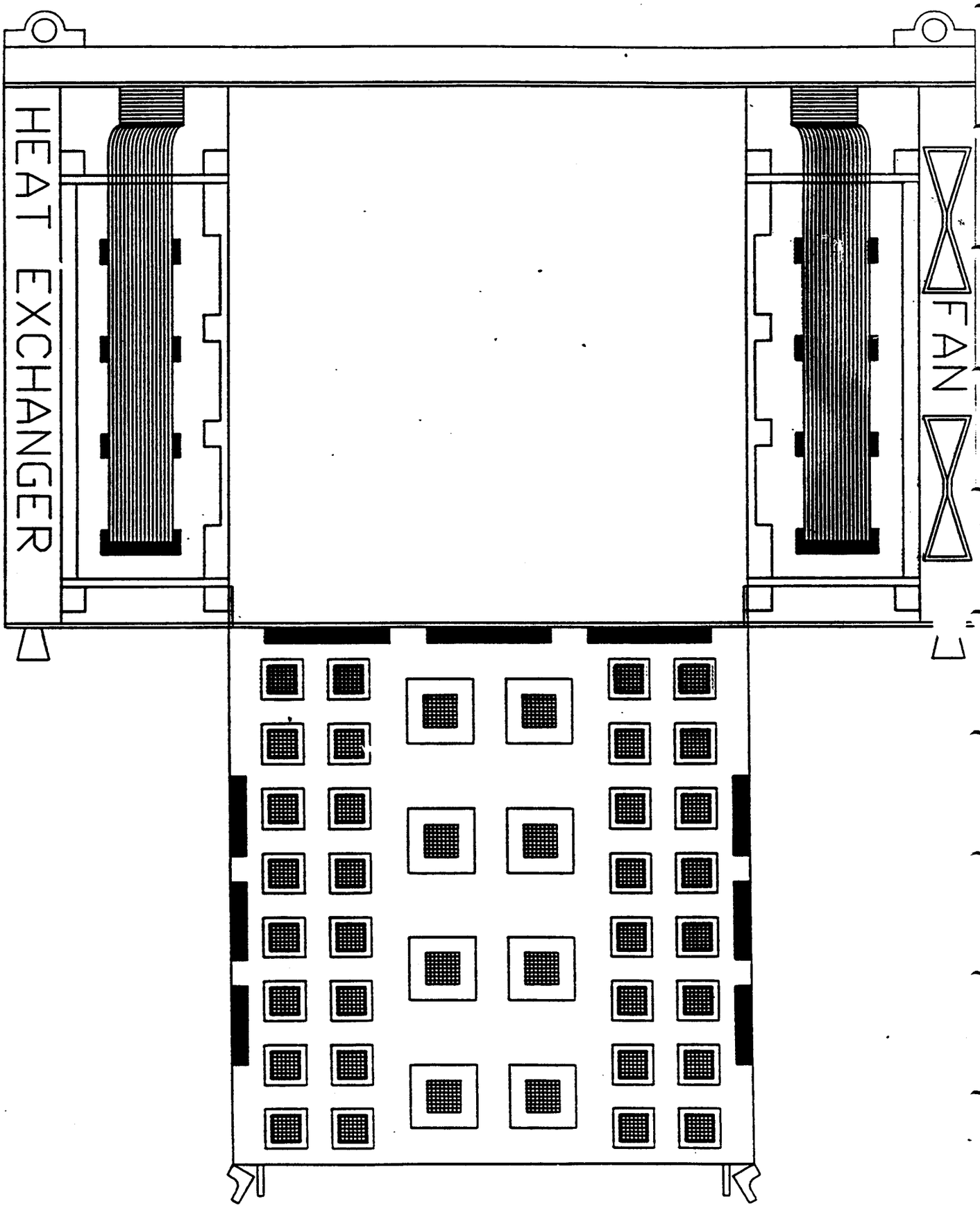
A third test was done on the Spectra-Strip ground plane cable to examine end channel effects (pairs of conductors at the edge of the flat cable). The cable characteristics for end channels were found to be the same as those for middle channels. If a cable is used without an extended ground plane or appropriate interleaved ground conductors, the characteristics of end channels can be expected to be different than those of middle channels.

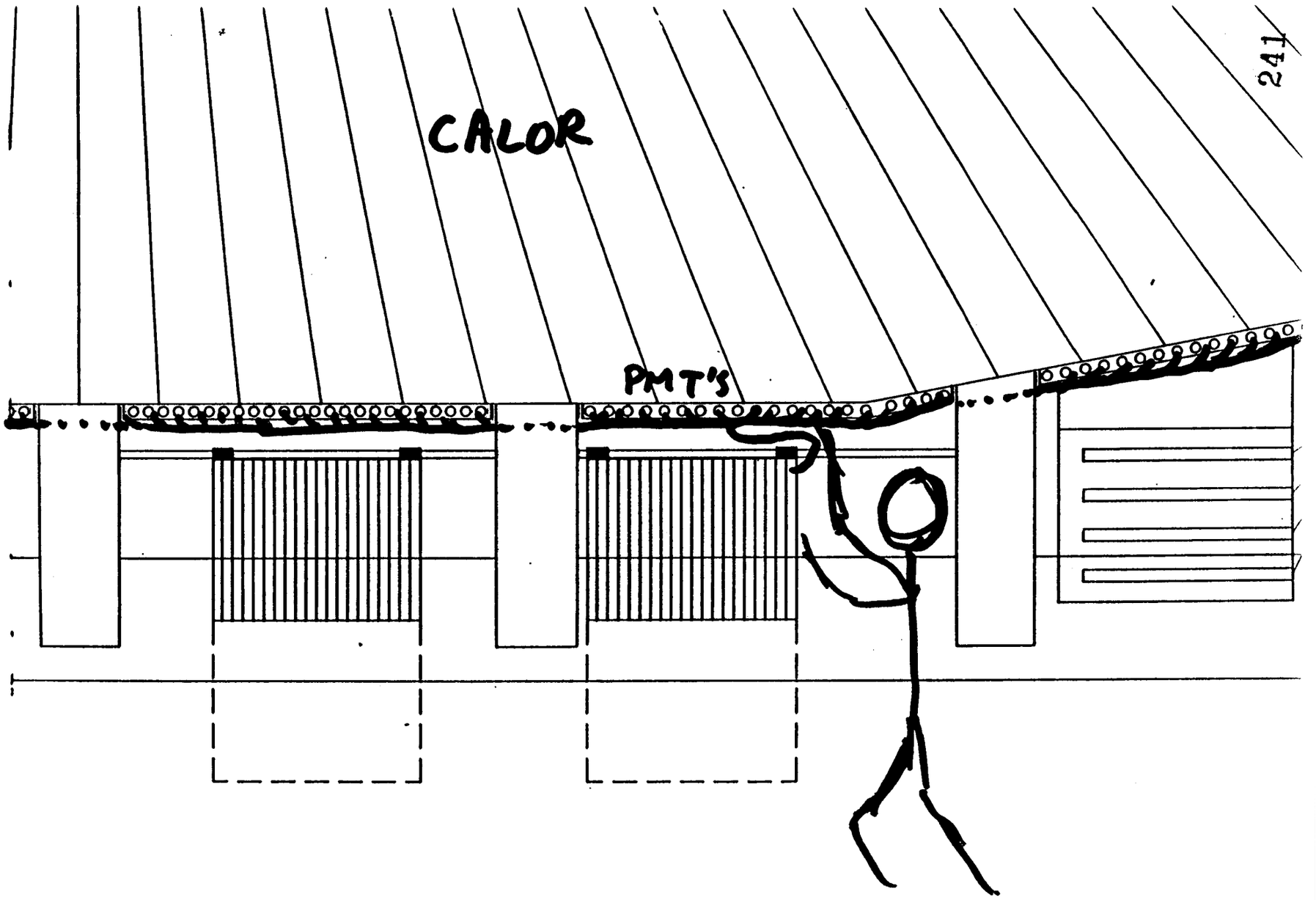
At the present time, the Spectra-Strip cable with imbedded ground plane appears to be an excellent choice for E-771 detector signals. Ultimately this cable could find use in many other similar installations.

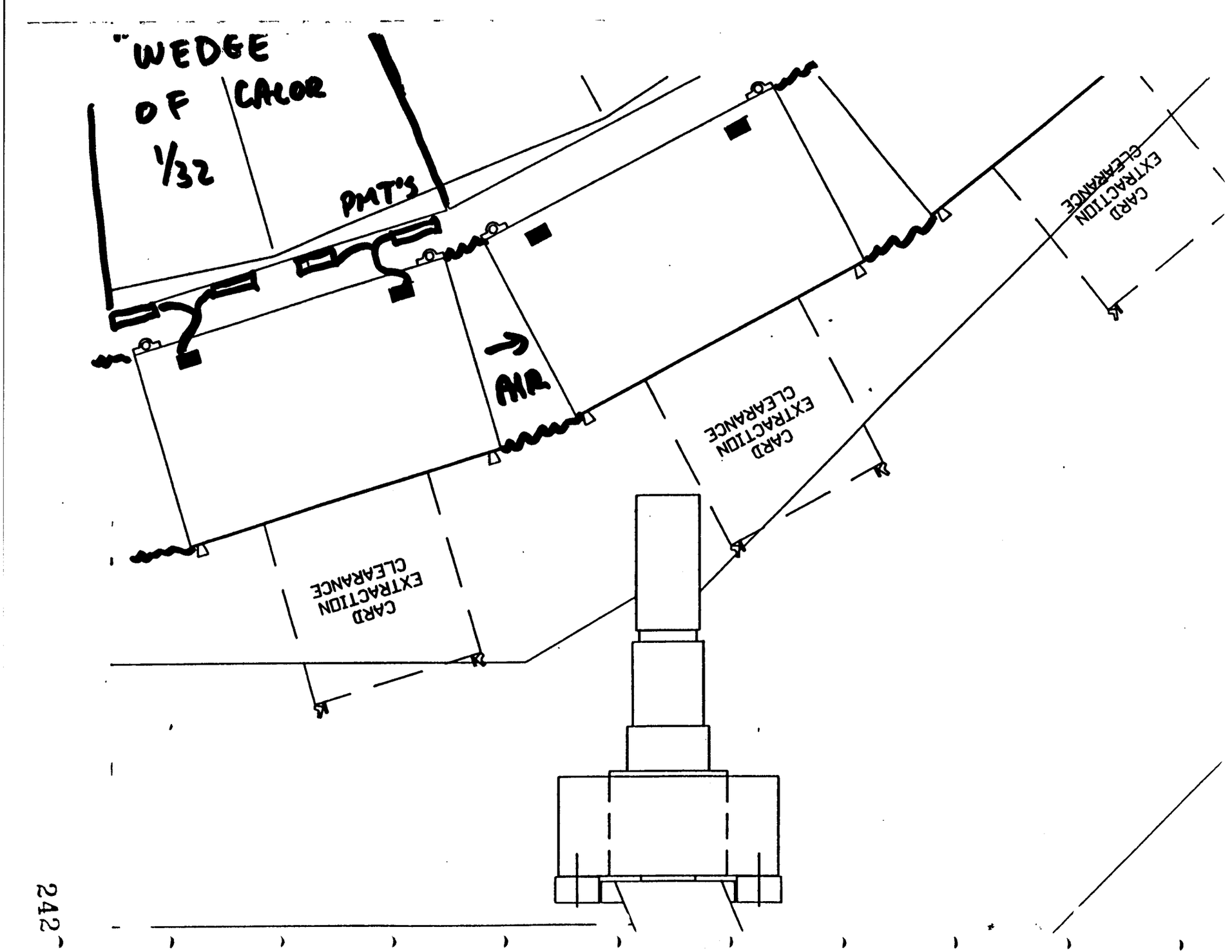
CHIMNEY IS EASIER FOR VERTICAL CRACK DESIGN




CARD
EXTRACTION
CLEARANCE
FAN
HEAT EXCHANGER


HEAT EXCHANGER
FAN


CALOR
PMT'S


"WEDGE
OF CALOR
1/32
PMT'S
AIR
CARD
EXTRACTION
CLEARANCE
CARD
EXTRACTION
CLEARANCE
CARD
EXTRACTION
CLEARANCE

CALOR ELECTRONICS DEPLOY & DEBUG SCENARIO:

(All-Digital Readout/Trig/DAQ)

- Test Bench: Debug the Analog
- Test Stand: Modular Assembly & Test
- Test Crates: Standalone 1-wedge testing
- Test Beam: Several Wedge testing

(ship to Dallas & Assemble in Pit...)

- Test of MC Events: Full-speed Clocking
- CR testing in Pit: PMT Gate Positions
- Beam-on tests:
  - PMT Gate phasing to RF
  - Trigger Thresholds
- Datataking

- Verify Analog Performance of Base-Digitizer

    - H.V. Regulation, noise
    - Digitizer Noise, Linearity
    - Toleration of Different Digital Cable lengths

    **--> REJECTION OF EXTERNAL NOISE

**** we are now out of the Analog Business ***

IT IS A CHARACTERISTIC OF ANALOG SYSTEMS THAT THE WHOLE SYSTEM OFTEN BEHAVES DIFFERENTLY THAN THE SUM OF THE PARTS (coherent noise pickup, oscillations, groundloops, etc...)

WITH ANALOG SYSTEMS, YOU MUST HOLD YOUR BREATH EVERY TIME YOU PLUG TOGETHER 10x MORE COMPONENTS THAN YOU HAVE EVER TESTED BEFORE. All-Digital systems go together with much less agony.

4,000 fake events can be downloaded
to calibration/lookup RAM

==> Full 63MHz testing of trigger
and interconnects w/o beam

Smaller number can be downloaded to PMT bases
(BiCMOS digitizer ASIC)

==> full-speed testing of PMT cables

Glitch Hunting
1) Download Fake Data to all ~64 Crates
2) Trigger if any crate disagrees

-->(impossible w/analog trigger!)

3) Complete dump of pipeline history
tells you where the ball got dropped

4) Full Binary trigger simulation via CPU

Test Vectors - RAMS can be accessed:
- Sequentially, to generate repetitive waveforms
and reproduce glitches
- Quasi-randomly (but deterministically!)
via random sequence generator circuits

==> generate effectively huge test vectors
to excite low-probability error modes

Fermilab

Digital Storage & Gain Correction ASIC for PMT Readout

SDC

FY-91

A prototype of the delay portion (called SIRO) of the ASIC has been designed and is being fabricated. A CAMAC test board has been designed and fabricated to test the SIRO chip. Performance of the SIRO chip will be evaluated and another chip submitted if necessary in FY91. A VME based version of the SIRO board is being designed and built for use in the test beam.

FY-92

Fabricate complete prototype IC, including calibration lookup RAM, L1/L2 storage, and readout FIFO. Iterate design to optimize performance, power, and diagnostic features.

TRIGGER DESIGN

- All-Digital Trigger
  - Based on same information as offline
  - No "Trigger Efficiency" curves !

* Make all possible cuts in the lowest level trigger
  - energy sums, isolation, track match, etc.
  - CDF experience indicates that this will get down to the "physics" rate
  - no need for 2nd-level trigger processors, etc.
  - no need to buy the (Mega-Vax) Farm!

* Straight "Fall-thru" digital pipeline
  - easy to debug
  - deadtimeless

* Built into same front-end digital gate arrays as DAQ/readout system: Saves $$$

* Can be fully debugged in advance by using front-end digital storage to exercise trigger logic at full clock speed.

Fermilab

Floating-Point Adder Tree ASIC (for Scint. Calorimeter Energy Sums)

SDC

(Includes Quad Adder and Total Energy Sum circuits)

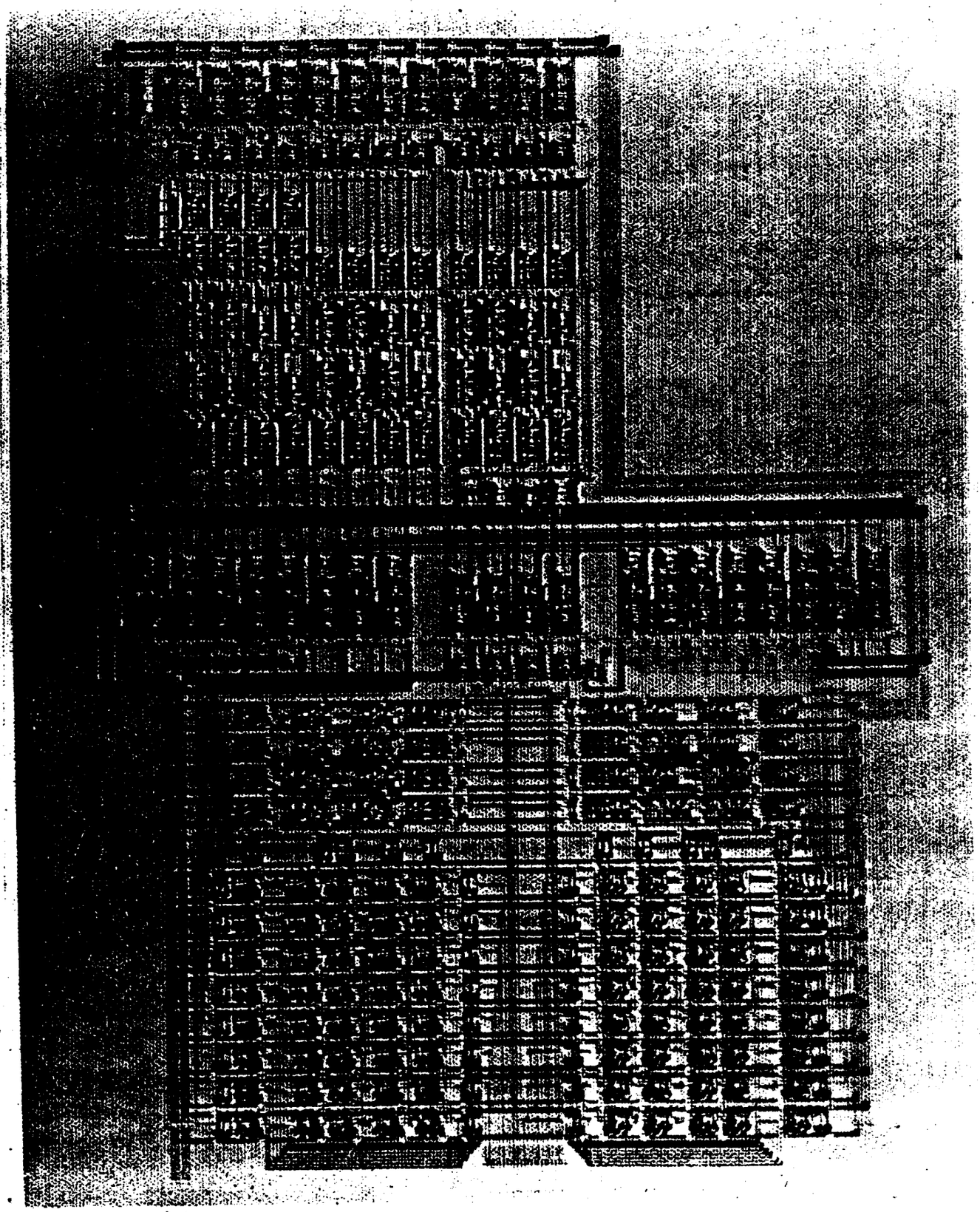
FY-91

Fabrication and test of a floating point adder for two numbers with an 4 bit exponent and an 8 bit mantissa. Layout has been completed and the chip submitted for fabrication. Performance evaluation of the first chip and a second submission is expected in FY91.

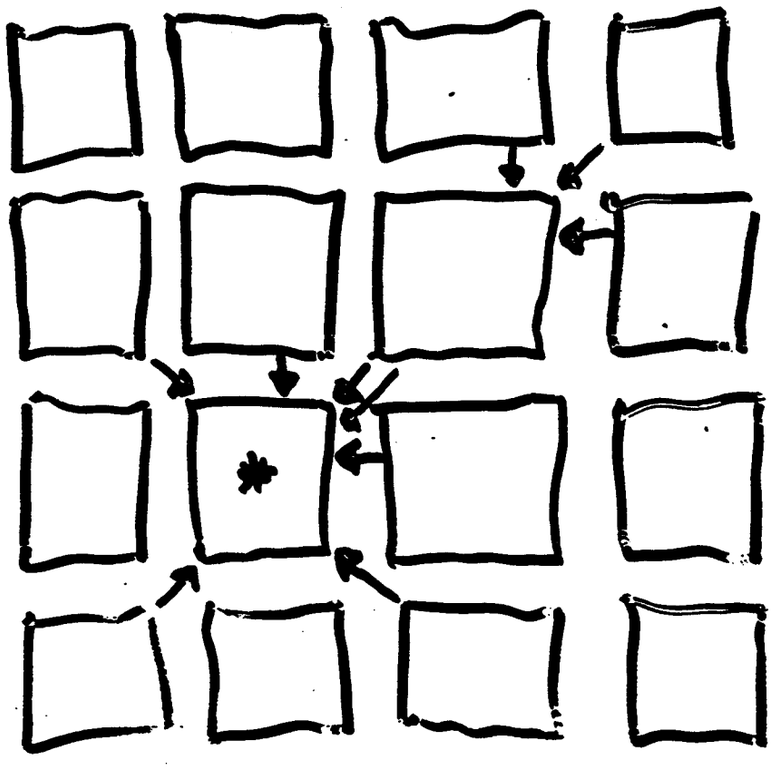
FY-92

First layout of a complete chip is expected. Allowance is made for multiple fabrication runs to test design principles.

91-495-2



EXAMPLE: ELECTRON TRIGGER



□ SIGNAL TOWERS

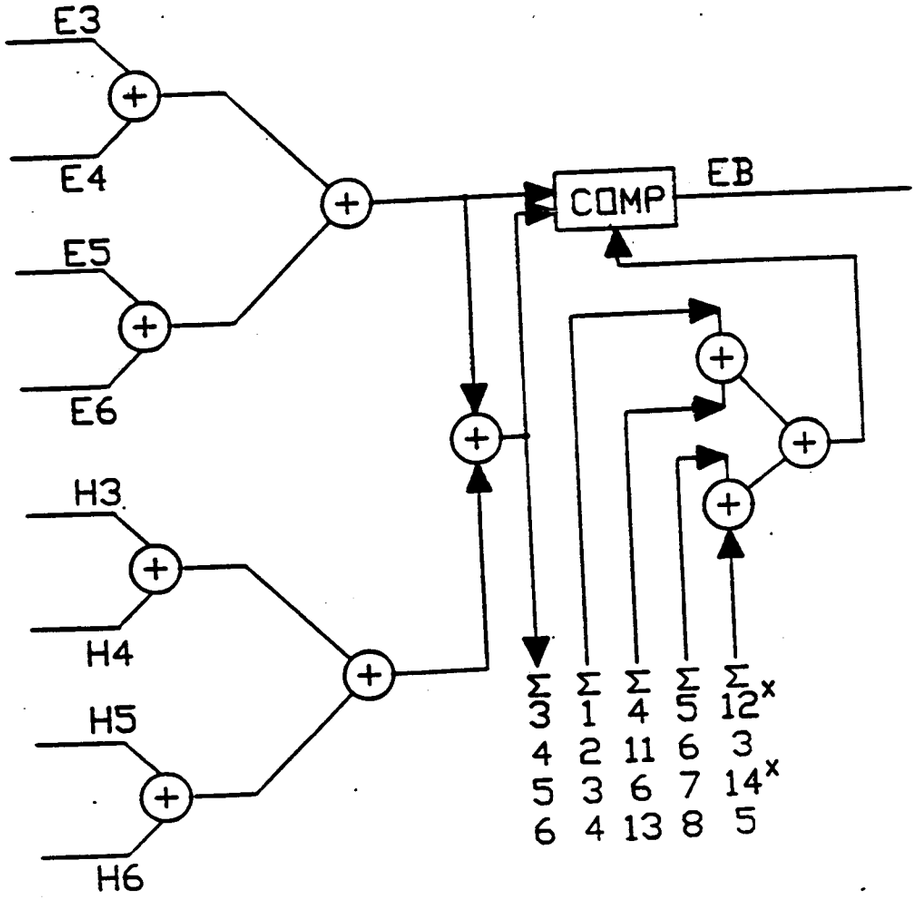
□ ISOLATION TOWERS

(1) PERFORM 2x2 OVERLAPPING SUMS FOR EM and HADRON SIGNAL TOWER

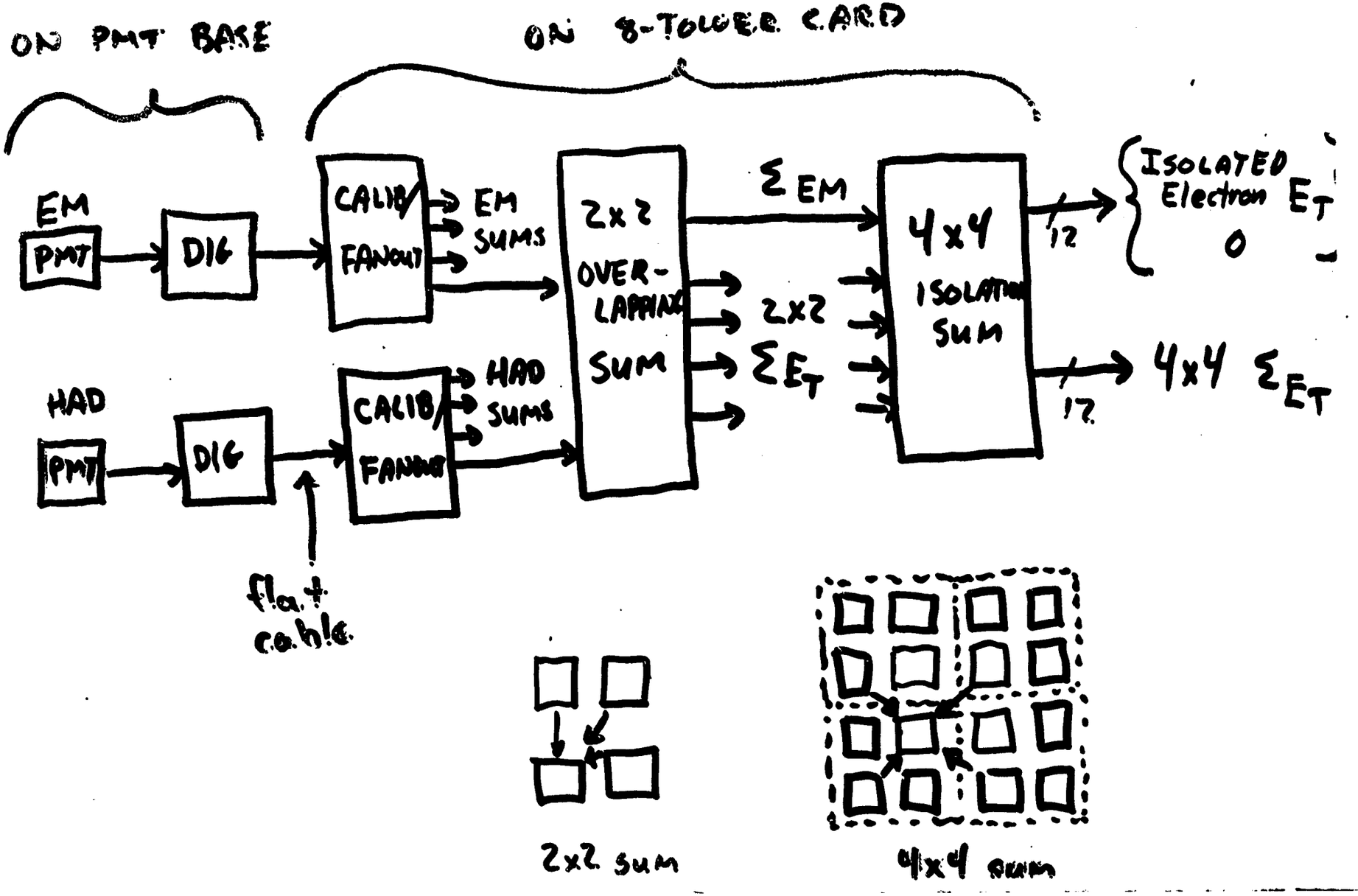
⇒ CUT: $\frac{\text{HADRIN}}{\text{EM}}$

(2) ADD 2x2 SUMS to get 4x4 SUM FOR ELECTRON/PHOTON ISOLATION

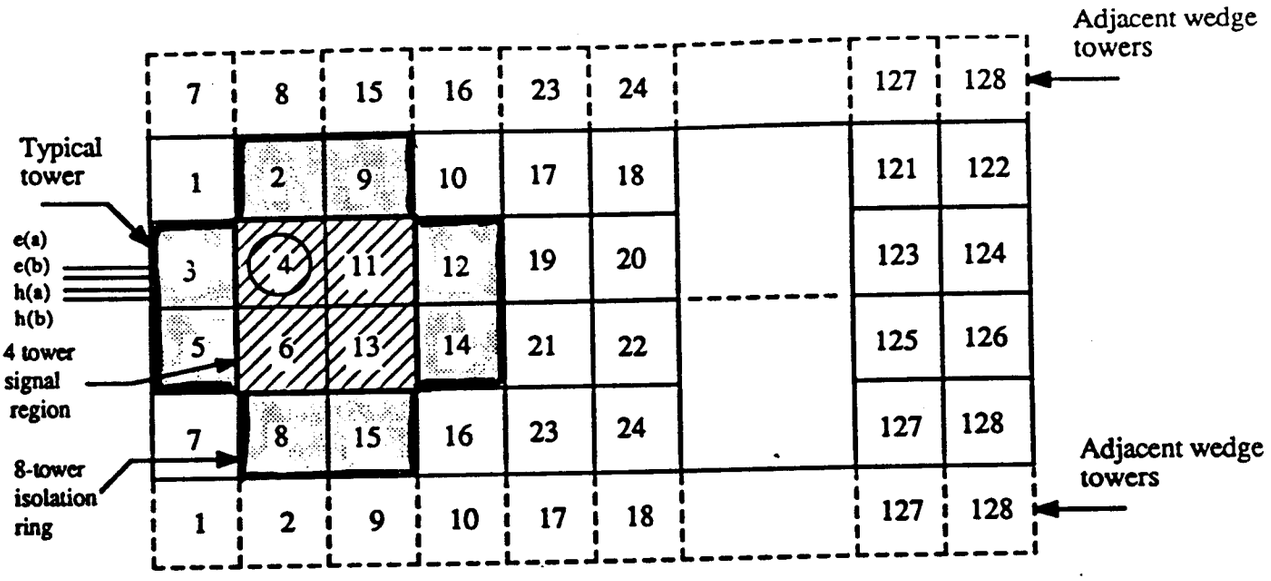
⇒ CUT: EM ISOLATION


E3
E4
E5
E6
H3
H4
H5
H6
COMP
EB
Σ 3 4 5 6
Σ 1 2 3 4
Σ 4 11 6 13
Σ 5 6 7 8
Σ 12x 3 14x 5

TOWER LOGIC PIPELINE



SDC Scintillating Calorimeter
Electron Identification



An electron is identified in the following manner:

Electron Energy Sums Each group of 4 adjacent towers is examined to determine if an electron was present. This includes all possible adjacent towers which includes overlapping groups of 4 on the same wedge such as 1-2-3-4 and 2-9-4-11 as well as groups of 4 which cross wedge boundaries. Thus, there are 128 groups of 4 towers (neglecting end effects)/wedge or 8 groups of 4 towers/readout board.

Each group of 4 towers is represented by the tower number in the upper left hand corner of the group. Towers 4-11-6-13 are represented by the circled number 4.

The two electron PMT signals and the two hadron PMT signals are added to provide an electron sum and a hadron sum for each tower. The sum signals are referred to as the electron and hadron signals.

Had/Em Two conditional tests are used to identify an electron.

In the first test, the electron energy sum from 4 towers is compared to the total electron and hadron energy sum for the 4 towers. If the ratio is greater than X%, the test is passed. For the 4 towers shown inside the heavy line box (4,11,6,13), the test is as follows:

$$\frac{E(4,11,6,13)}{E(4,11,6,13) + H(4,11,6,13)} > X\% \qquad X \text{ is programable (eg 88\%)}$$

Isolation

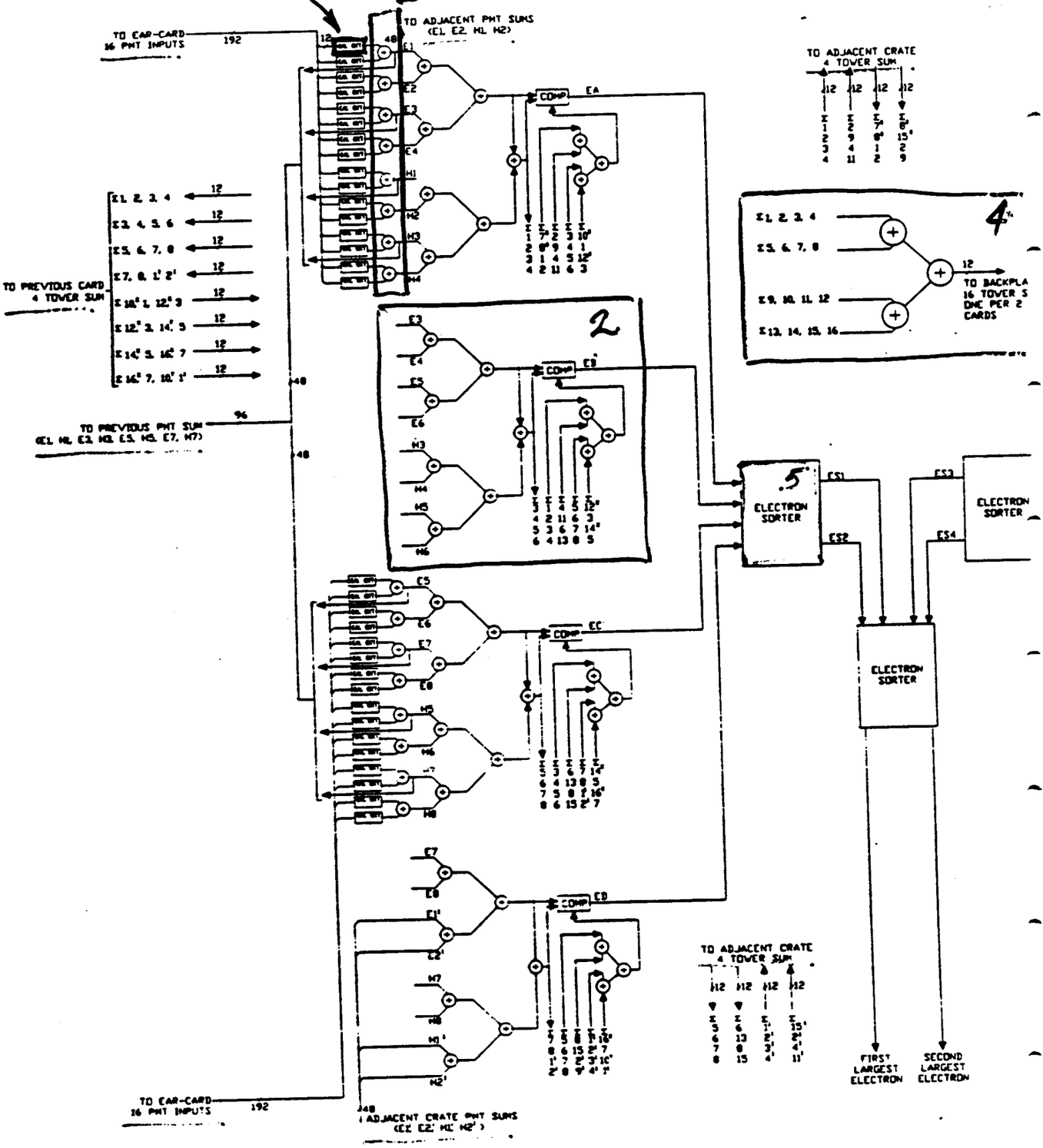
In the second test, the electron energy sum from 4 towers is compared to the total electron and hadron energy sum from four 4 tower sums. If the ratio is greater than Y%, the test is passed. For the 4 tower sum identified by the circled #4, the 4 tower sums to be used are shaded.

$$\frac{E(4,11,6,13)}{E(2,9,4,11,11,12,13,14,6,13,8,15,3,4,5,6)+H(2,9,4,11,11,12,13,14,6,13,8,15,3,4,5,6)} > Y\%$$

An alternate test which may be used is the ratio of the electron energy sum from 4 towers to the total energy from four non-overlapping 4 tower energy sums (eg 1-16).

Electron sorting If the two tests are passed, the electron energy sum (eg E(4,1,6,13)) is passed along with an address location to a series of sorter circuits to identify the largest and next largest electron signals.

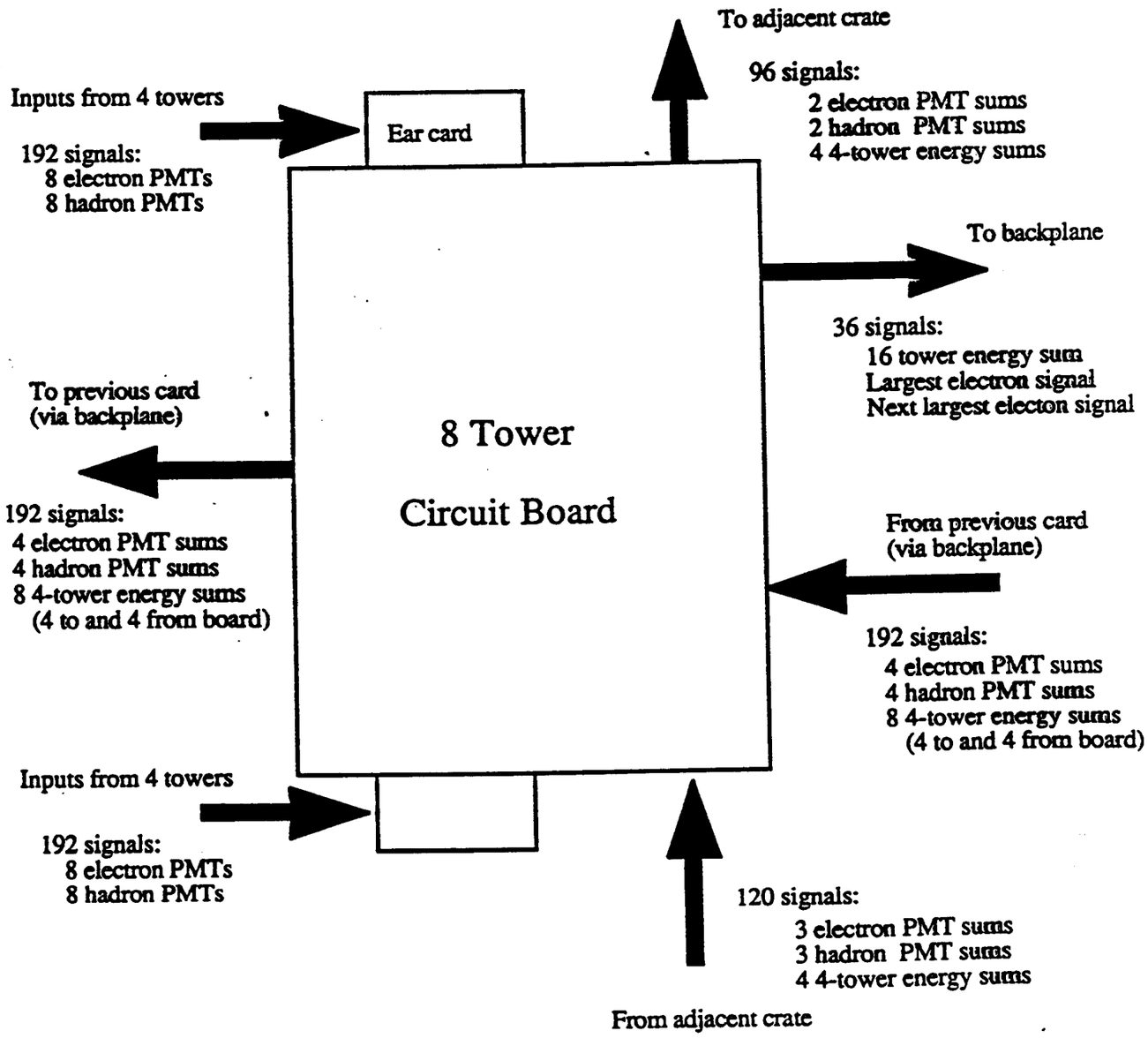
ENERGY SUMS & ELECTRON I...



SDC Scintillating Calorimeter 8-Tower Readout Board

The trigger logic on the tower circuit board performs the following functions:

1) Finds electron sums from two electron PMTs on a tower
2) Finds hadron sums from two hadron PMTs on a tower
3) Finds four tower energy sums
4) Finds the largest and next largest electron signal
5) Finds the total energy for 16 towers



Each PMT input and PMT sum is a 12 bit floating point signal bus.

Total number of PMT signal lines entering and leaving board = 1020
(does not include power, clock or other control signals)

RJY
2/25/91

SDC Scintillating Calorimeter Crate
Circuit Board Organization

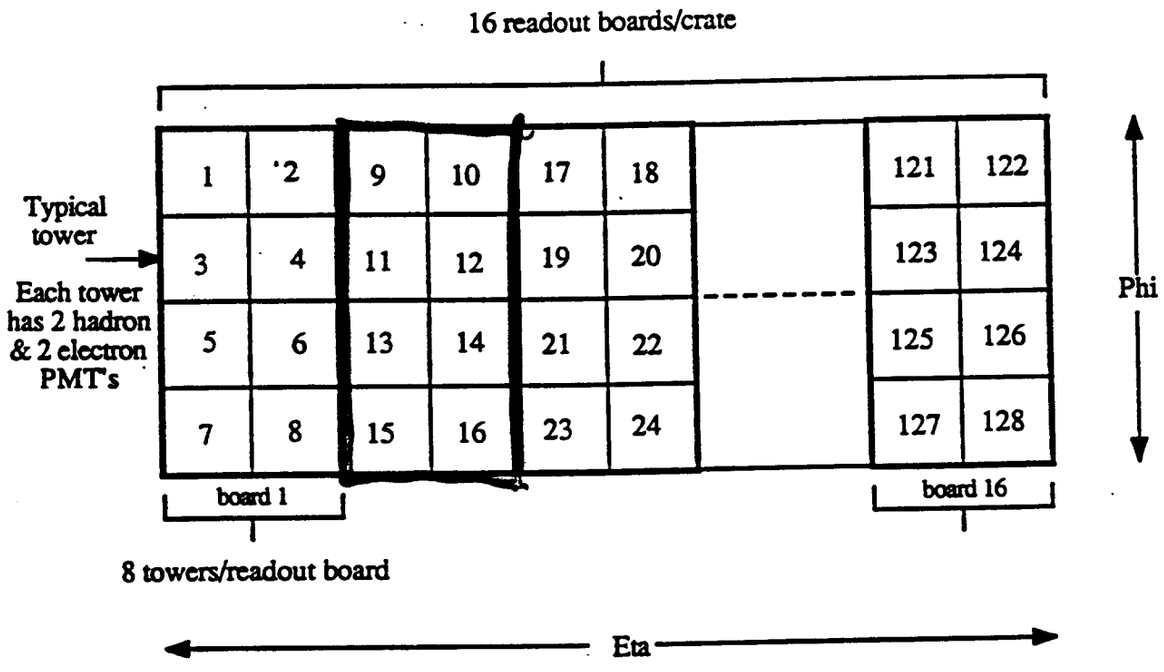
Each wedge has 128 towers (512 PMTs).

There is 1 crate of electronics associated with each 128 towers (wedge).

Each crate has 16 calorimeter readout boards.

Each readout board handles signals from 8 towers (eg 1-8, 9-16, etc)

Each tower has two electron and two hadron PMTs.



FNAL design of full local electron trigger
- 2x2 overlapping sums
- EM/Hadron
- 4x4 Isolation Sums
- sums cross card, crate & wedge boundaries
- Track Match
- electron sorting

leads to a lot of nearest-neighbor digital interconnects
- ~20/PMT (incoming flat cable from PMT)
- ~25/PMT (trigger interconnects)

most of these are not "mission critical":

- masking out a single dead nearest-neighbor interconnect will negligibly effect trigger eff. (we turn off trigger channels in CDF all the time)

- only the crate-wide energy sums are critical (these are 2-fold redundant in our design)

**** If you design in nearest-neighbor interconnects,
- the cost is small ~~$400k
- you have 10 years to optimize their usage by changing the digital login on each tower
- they may save your butts on trigger rate.

(if CDF had them, we could write ~pure electrons onto tape).

Pipeline Timing Sequence of Operations

- **Clock Cycles 1-6:** Time-of flight, Optical Fiber and Phototube Propagation Delays
- **Clock Cycles 7-10:** Phototube Digitization and Cabling Delay to Trigger Crate
- **Clock Cycles 10-13:** Calibration and E_T weightings of Phototube energies (pipelined lookup table).
- **Clock Cycles 13-17:** Exchange of Nearest-neighbor energies to form overlapping 2x2 and 4x4 Energy Sums.
- **Clock Cycles 17-31:** Identification of $e/\gamma/\mu$ candiates in the calorimetry by placing threshold and ratio cuts on local sums.

  [Note: Pipelined Track processing complete at this point].
- **Clock Cycles 31-43:** Wedge-level E_T sums and lists of $e/\gamma/\mu$ candidates in each wedge completed.
- **Clock Cycles 43-49:** Pipelined Track Match of $e/\gamma/\mu$ candiates; identification of largest, 2nd largest e, μ in each wedge.
- **Clock Cycles 49-63:** Cable Delay and Re-synchronization for data transport from wedges to Trigger Platform located outside of muon steel.
- **Clock Cycles 63-78:** Calculation of global Sum E_T, Missing E_T, and Biggest, 2nd biggest e, μ in event.
- **Clock Cycles 78-94:** Final Yes/No Trigger Decision
- **Clock Cycles 94-112:** Cable Delay and Fanout of Trigger Decision Bit to front-end chips.

⇨ COMPLETE TRIGGER DECISION (EQUIVALENT TO MOST HIGHER-LEVEL TRIGGER) IN LOWEST-LEVEL (2μsec) PIPELINE.

Cost for Scintillating Calorimeter Readout with Flash Encoders

	Unit cost	NRE	Cost/PMT
Phototube digitizer (40000)			
Quicktile gated integrator ASIC	15.30	94K	17.65
FADC- Signetics TDA8713 or eq. 50 Mhz, 8 bit	18.00?	----	18.00
Electronics calibration circuit	5.00	----	5.00
Assembly	20.00	----	20.00
Test assembly	2.00	4K	2.10
Power supply and fusing (No HV)	----	----	3.10
Phototube to tower crate cabling (20000)			
Cable (15', 20 conductor with ground plane, 0.025" pitch)	6.75	----	6.75
Sockets (845-C0205-ALA00)	1.78	----	3.56
Assemble and 100% test	3.44	----	3.44
Mating headers (2)	1.71	----	3.42
Tower circuit board (8 towers/board, 32 PMT/board, 1250 boards)			
Calibration RAM & delay FIFO ASIC (40000, 32/board)	6.65	72K	8.45
Adder tree ASIC(10000, 8/board)	16.50	72K	5.92
Electron sorter ASIC (3/card)	9.54	72K	3.00
Circuit board (18"x12", 6-8 layer)	240.00	----	7.50
Misc logic & special connectors	----	----	20.00
Assembly	128.00	----	4.00
Test	32.00	20K	1.50
Master Summation Board (1/crate)			
Includes: 14 electron sorter ASIC's circuit board, misc parts, assembly, and test	900.00	----	1.75
Crate & Enclosure (16 Adder boards/crate, 16 PMT/board, 78 crates)			
Includes: crate, power supplies, backplane, heat exchanger, blower, alarms, and ductwork	10000	----	19.53
Total/PMT			154.67
Contingency - 20%			30.00

Total system cost = $7,360,000

Perspectives on Calorimeter Triggering

W. Smith (Wisconsin)

Calorimeter Triggering

T. Gorski, J. Lackey, W. Smith, W. Temple

U. Wisconsin

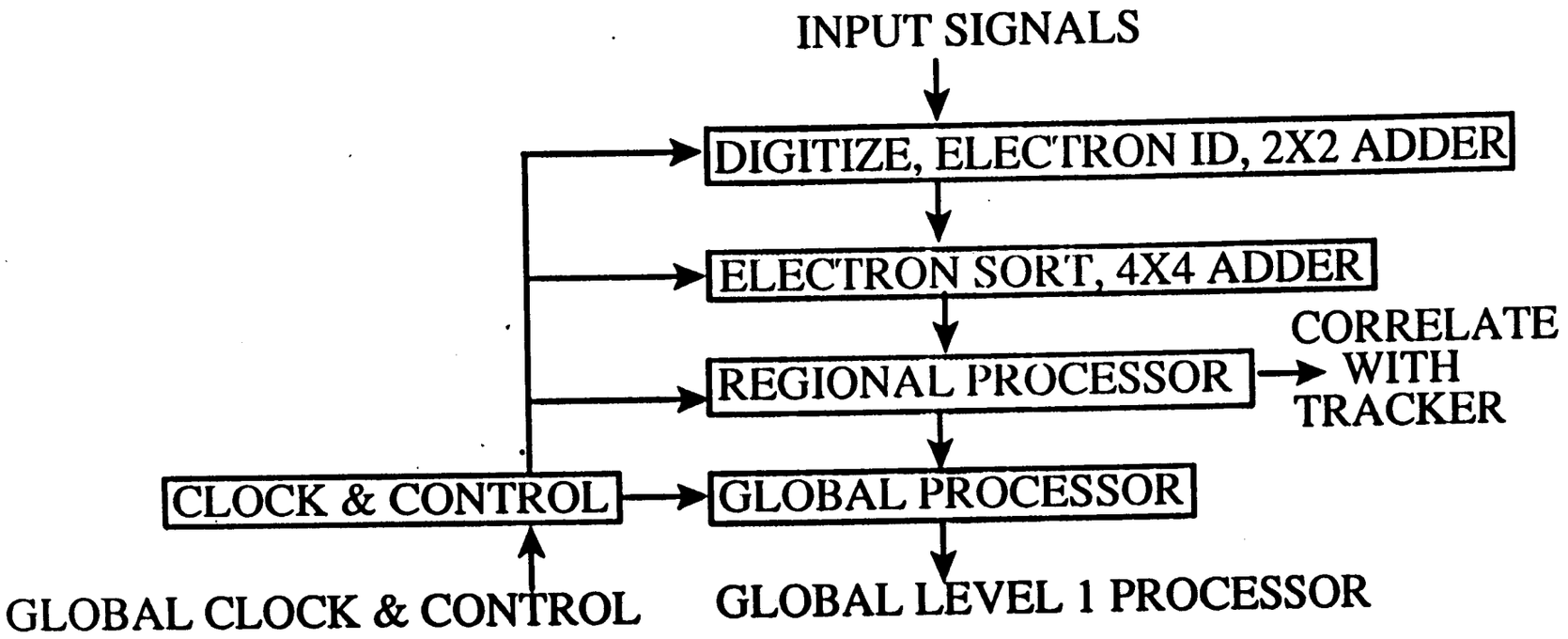
I. General Organization
   Cal. Trigger Functional Blocks
   Interface to Global Trigger

II. Isolated Electron Pattern Logic
   Circuit Design

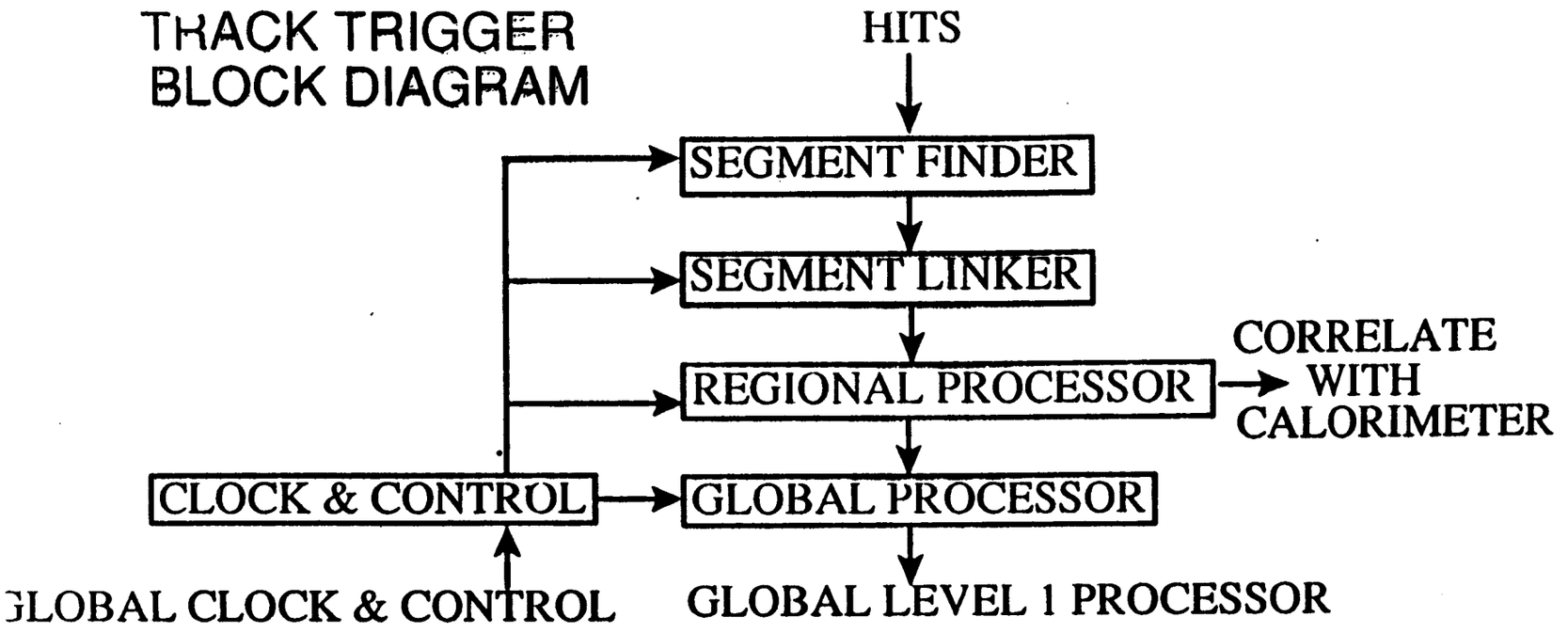
III. Comments on Cal. Triggering
   Major Issues
   (see talk by G. Sullivan)

Advertisement:
Madison Trigger Meeting: July 17-19
1. Establish baseline design(s)
2. Pipeline Length
3. Interfaces to FE/DAQ
4. Simulation Review
5. R+D Plan Review

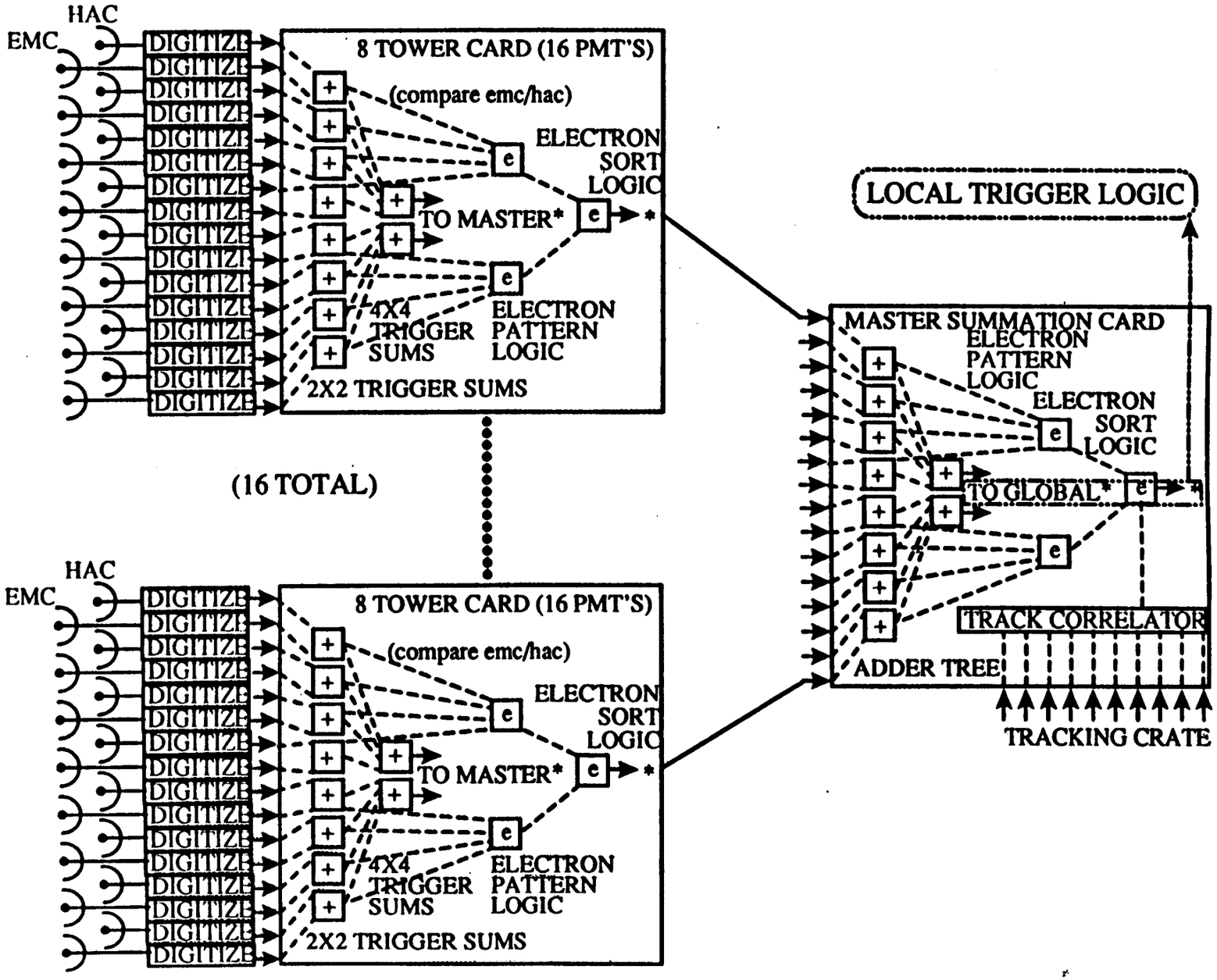
DIGITAL CALORIMETER TRIGGER BLOCK DIAGRAM



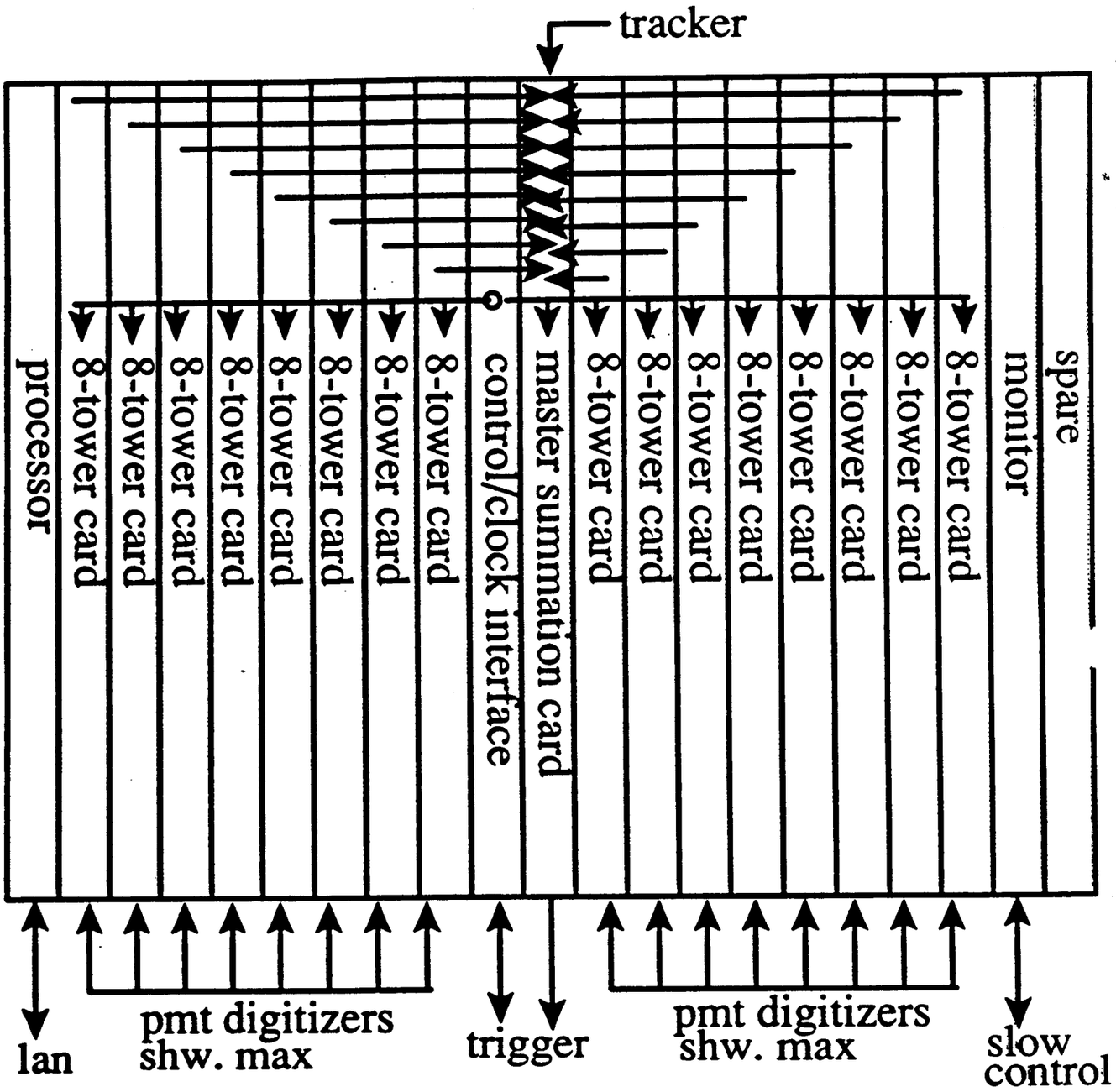
TRACK TRIGGER BLOCK DIAGRAM



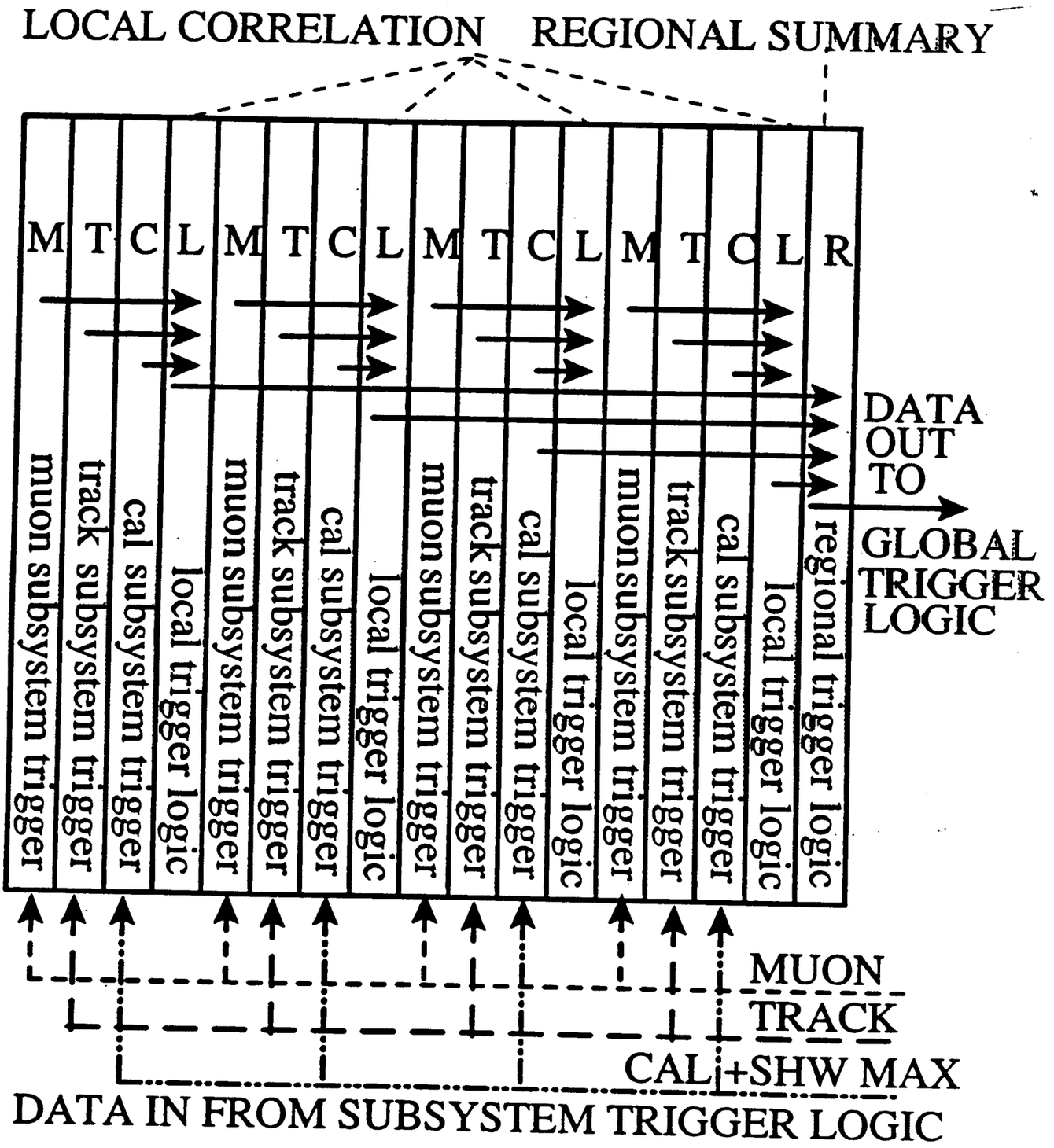
CALORIMETER FIRST LEVEL TRIGGER:
WEDGE CRATE (1 OF 78): SERVICES 512 TOWERS

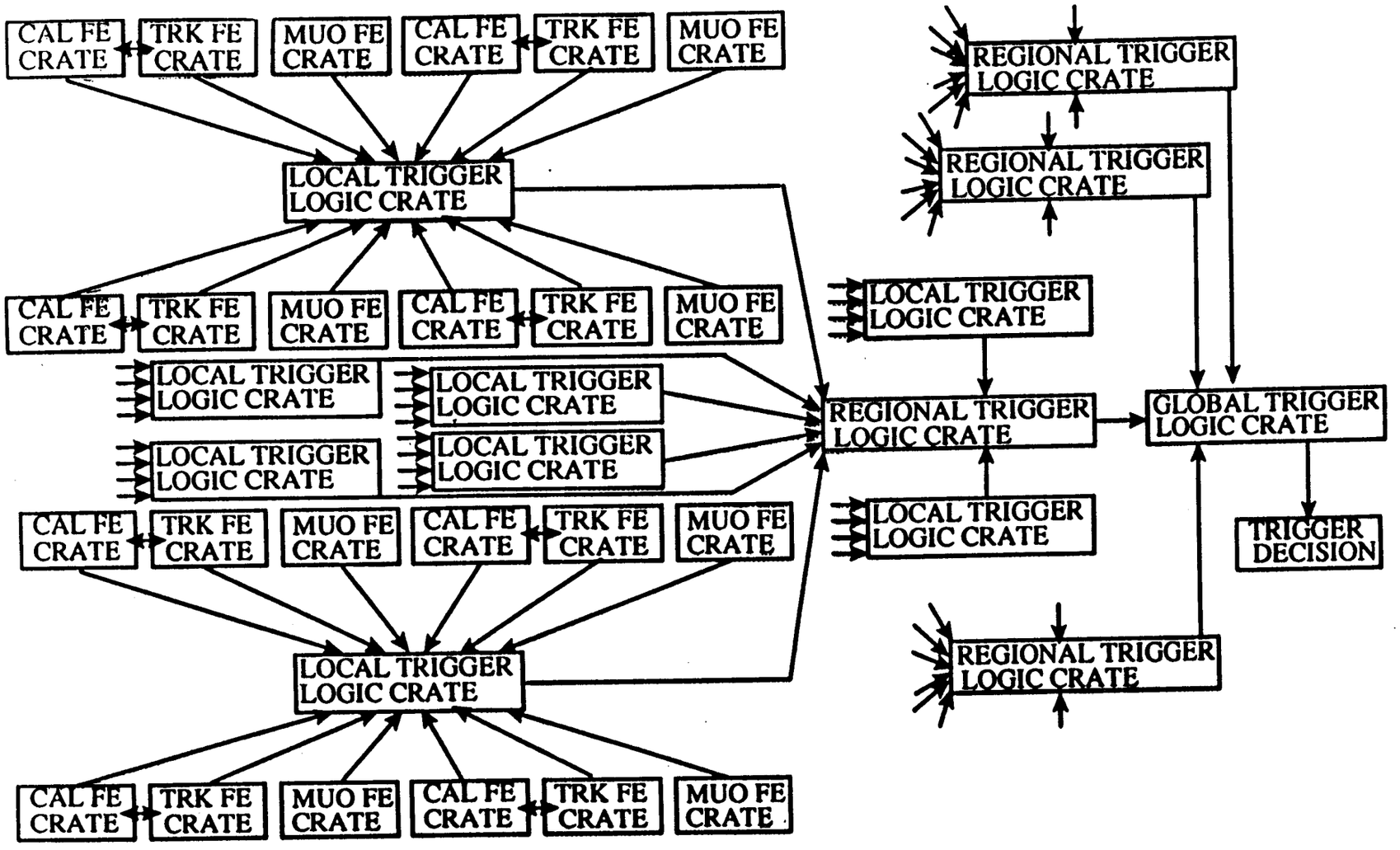


CALORIMETER FRONT END CRATE



LOCAL TRIGGER LOGIC




CAL FE CRATE
TRK FE CRATE
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CAL FE CRATE
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LOCAL TRIGGER LOGIC CRATE
CAL FE CRATE
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LOCAL TRIGGER LOGIC CRATE
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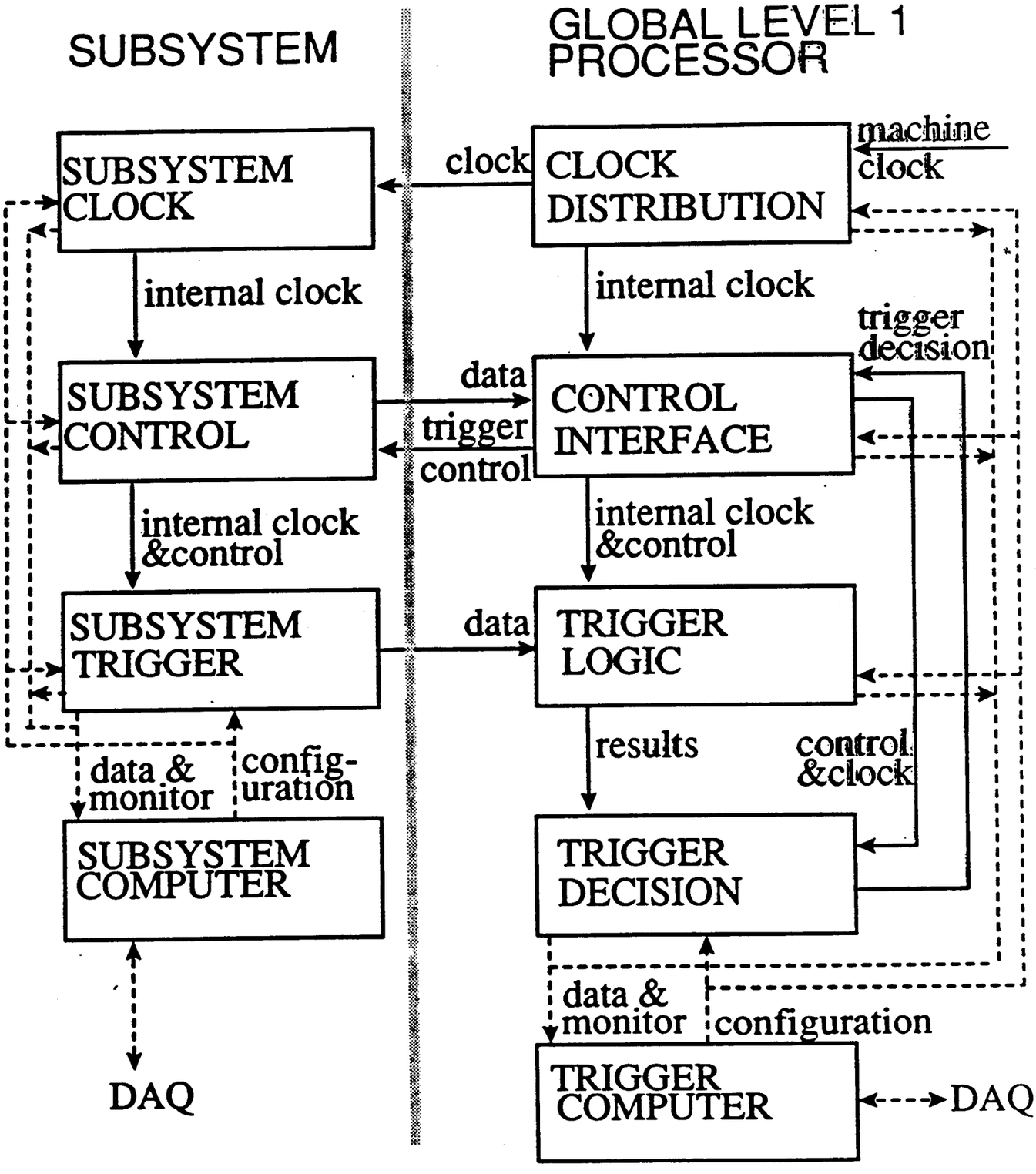
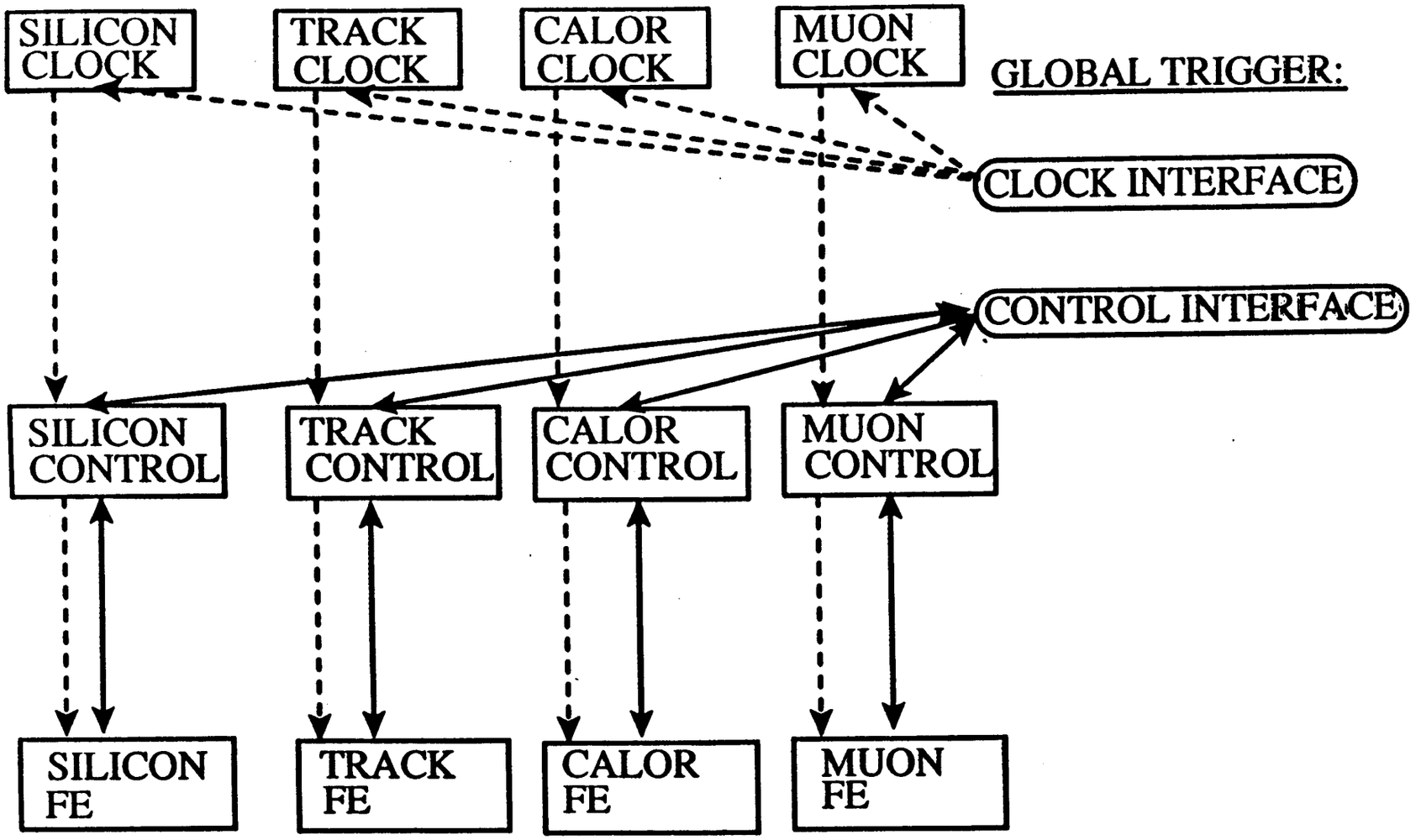
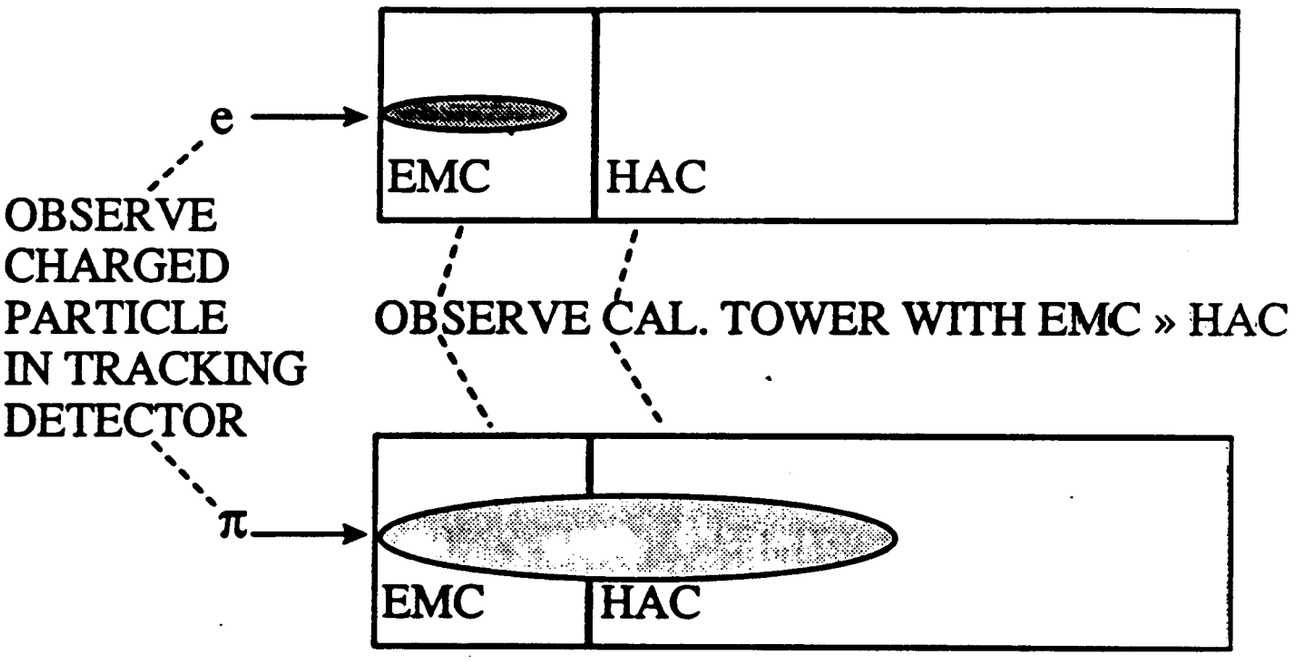
MUO FE CRATE
CAL FE CRATE
TRK FE CRATE
MUO FE CRATE
REGIONAL TRIGGER LOGIC CRATE
REGIONAL TRIGGER LOGIC CRATE
LOCAL TRIGGER LOGIC CRATE
REGIONAL TRIGGER LOGIC CRATE
GLOBAL TRIGGER LOGIC CRATE
LOCAL TRIGGER LOGIC CRATE
TRIGGER DECISION
REGIONAL TRIGGER LOGIC CRATE


SUBSYSTEM
GLOBAL LEVEL 1 PROCESSOR
SUBSYSTEM CLOCK
clock
CLOCK DISTRIBUTION
machine clock
internal clock
internal clock
trigger decision
SUBSYSTEM CONTROL
data
trigger control
CONTROL INTERFACE
internal clock &control
internal clock &control
SUBSYSTEM TRIGGER
data
TRIGGER LOGIC
results
control &clock
data & monitor
config-uration
SUBSYSTEM COMPUTER
TRIGGER DECISION
data & monitor
configuration
TRIGGER COMPUTER
DAQ
DAQ

SUBSYSTEM ELECTRONICS



FIRST LEVEL TRIGGER PIPELINE
ELECTRON IDENTIFICATION



OBSERVE THAT "ELECTRON" TOWER IS ISOLATED:

Use Pattern logic technique that avoids interconnects and overlapping sums. (Reduced Information set)

QUIET	QUIET	QUIET
QUIET	EMC » HAC	QUIET
QUIET	QUIET	QUIET

SDC Calorimeter Trigger
Isolated Electron Detection

Statement of Problem:

Find a method by which to locate calorimeter towers which contain energy depositions consistent with the passage of electrons. Examine adjacent towers to thus determine the presence of isolated electrons with two independent energy thresholds for the purpose of generating a first level trigger.

Perform this detection on 8x8 physical regions of towers, while at the same time minimizing the number of latteral interconnectons necessary between electronics crates.

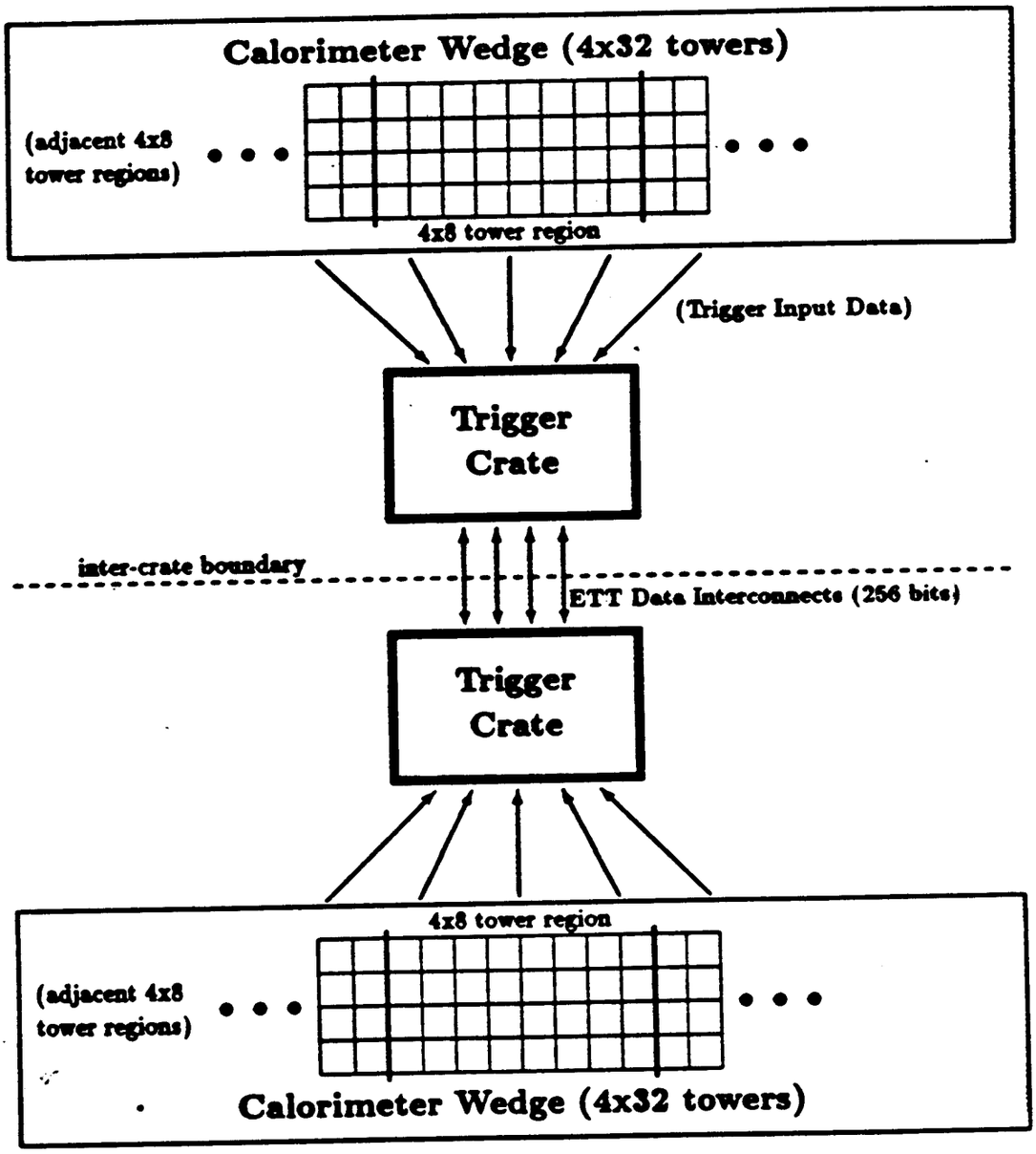


Figure 1: Interconnection of Two Wedges to Form 8x8 Grids. Total of 4 grids formed from pairing of 4x32 wedges.

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63

Upper Wedge

Lower Wedge

Figure 2: Tower Numbering Assignments in 8x8 Grid.
Each tower provides a 2-bit ETT data code.

ETT Code		State Definition	Q_L	E_L	Q_H	E_H
0	0	Quiet Tower	●		●	
0	1	Low-Energy Electron		●	●	
1	1	High-Energy Electron		●		●
1	0	Non-Electron				

Figure 3: ETT Codes and Q/E Bit Definitions.

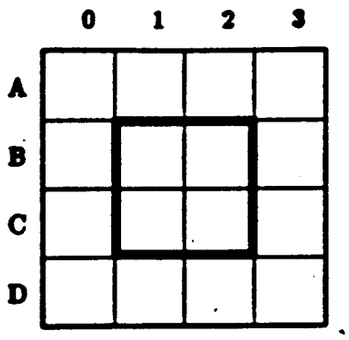


Figure 4: Blank Template Showing Inner 2x2 region.
Active E bits must be found in the inner 2x2 region, completely surrounded by Q bits.

Evaluation Function:

Definition: F **is TRUE if the template contains an isolated electron centered within the inner 2x2 region.**

$F = C_1 \cdot C_2 \cdot C_3 \cdot C_4 \cdot \overline{D} \cdot \overline{N}$, where:

$$C_1 = (Q_{A0} \cdot Q_{A1} \cdot Q_{B0}) + (\overline{E_{B1}} \cdot Q_{A1} \cdot Q_{B0}) + (\overline{E_{B1}} \cdot Q_{A1} \cdot \overline{E_{C1}}) + (\overline{E_{B1}} \cdot Q_{B0} \cdot \overline{E_{B2}}) + (\overline{E_{B1}} \cdot \overline{E_{B2}} \cdot \overline{E_{C1}})$$

$$C_2 = (Q_{D0} \cdot Q_{D1} \cdot Q_{C0}) + (\overline{E_{C1}} \cdot Q_{D1} \cdot Q_{C0}) + (\overline{E_{C1}} \cdot Q_{D1} \cdot \overline{E_{B1}}) + (\overline{E_{C1}} \cdot Q_{C0} \cdot \overline{E_{C2}}) + (\overline{E_{C1}} \cdot \overline{E_{C2}} \cdot \overline{E_{B1}})$$

$$C_3 = (Q_{D2} \cdot Q_{D2} \cdot Q_{C3}) + (\overline{E_{C2}} \cdot Q_{D2} \cdot Q_{C3}) + (\overline{E_{C2}} \cdot Q_{D2} \cdot \overline{E_{B2}}) + (\overline{E_{C2}} \cdot Q_{C3} \cdot \overline{E_{C1}}) + (\overline{E_{C2}} \cdot \overline{E_{C1}} \cdot \overline{E_{B2}})$$

$$C_4 = (Q_{A2} \cdot Q_{A2} \cdot Q_{B3}) + (\overline{E_{B2}} \cdot Q_{A2} \cdot Q_{B3}) + (\overline{E_{B2}} \cdot Q_{A2} \cdot \overline{E_{C2}}) + (\overline{E_{B2}} \cdot Q_{B3} \cdot \overline{E_{B1}}) + (\overline{E_{B2}} \cdot \overline{E_{B1}} \cdot \overline{E_{C2}})$$

$$D = (Q_{B1} \cdot Q_{C1} \cdot \overline{BOTTOM}) + (Q_{B1} \cdot Q_{B2} \cdot \overline{RIGHT}) + (Q_{B1} \cdot Q_{B2} \cdot Q_{C1} \cdot Q_{C2})$$

$$N = (\overline{E_{B1}} \cdot \overline{Q_{B1}}) + (\overline{E_{B2}} \cdot \overline{Q_{B2}}) + (\overline{E_{C1}} \cdot \overline{Q_{C1}}) + (\overline{E_{C2}} \cdot \overline{Q_{C2}})$$

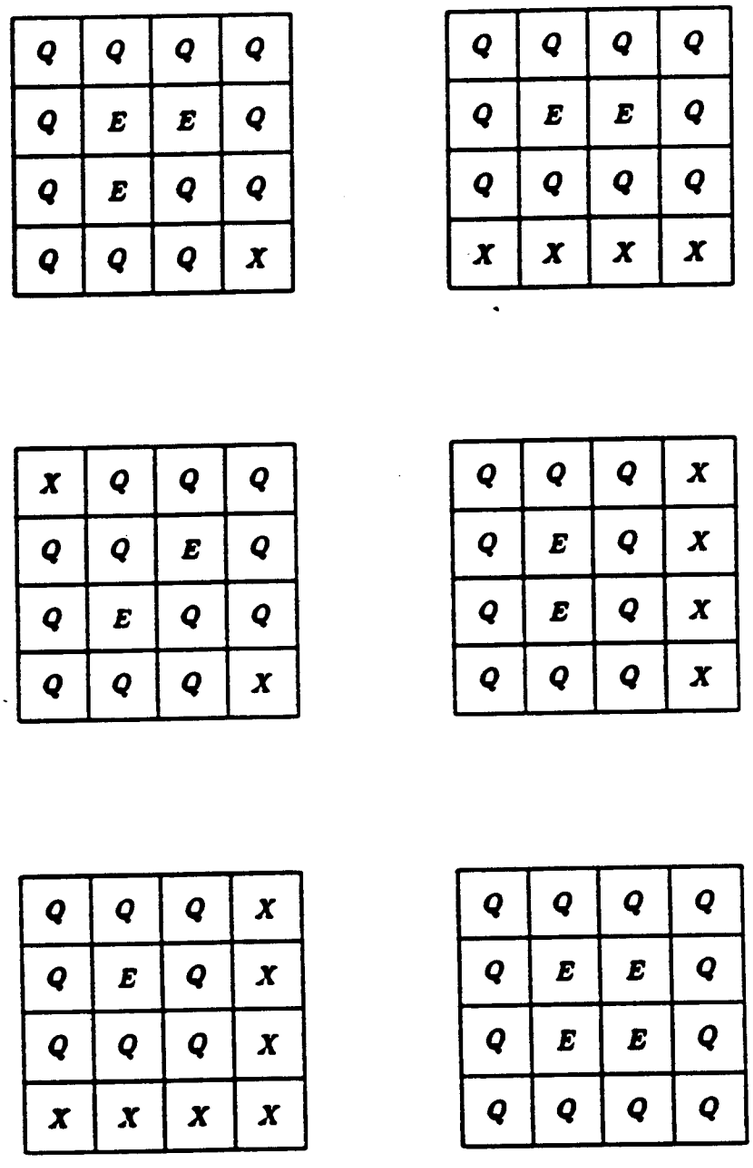


Figure 5: Examples of Isolated Electrons.
"X" denotes towers for which state is a "don't care."

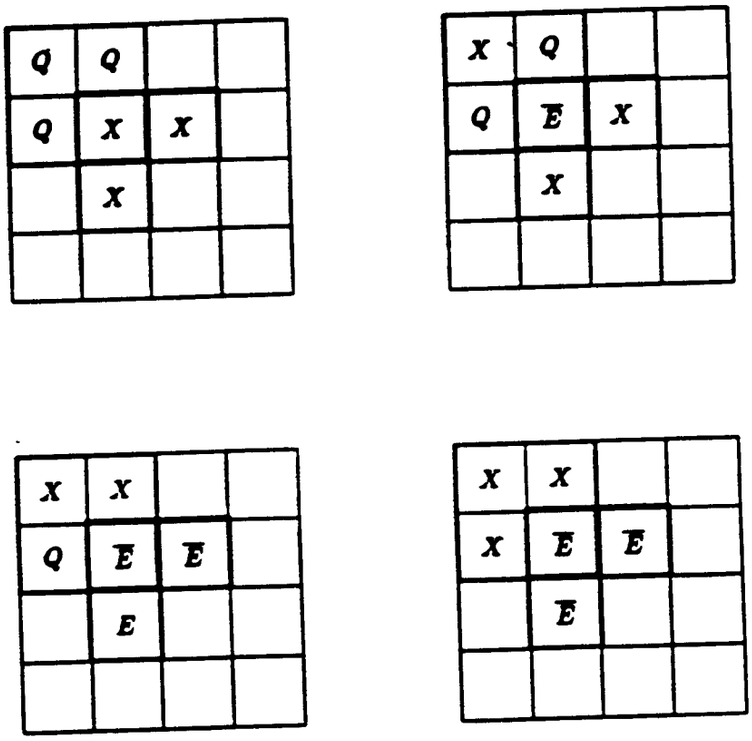
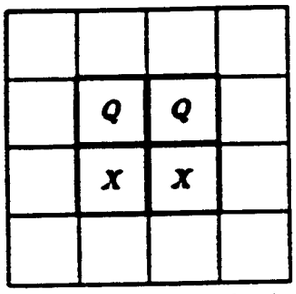
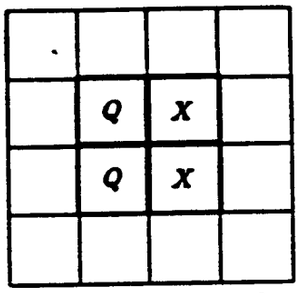


Figure 6: Region Operated on by $C1$ Corner Subfunction. Example cases for which subfunction is TRUE are shown. "X" denotes towers for which state is a "don't care." Other subfunctions obtained by rotating the template.



[Except bottom edge.]



[Except right edge.]

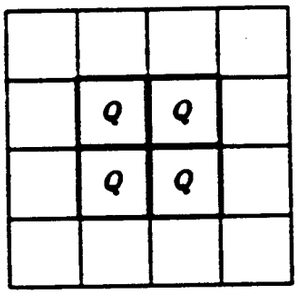


Figure 7: Region Operated on by *D* Defer Subfunction.
Cases for which subfunction is TRUE are shown.
"X" denotes towers for which state is a "don't care."

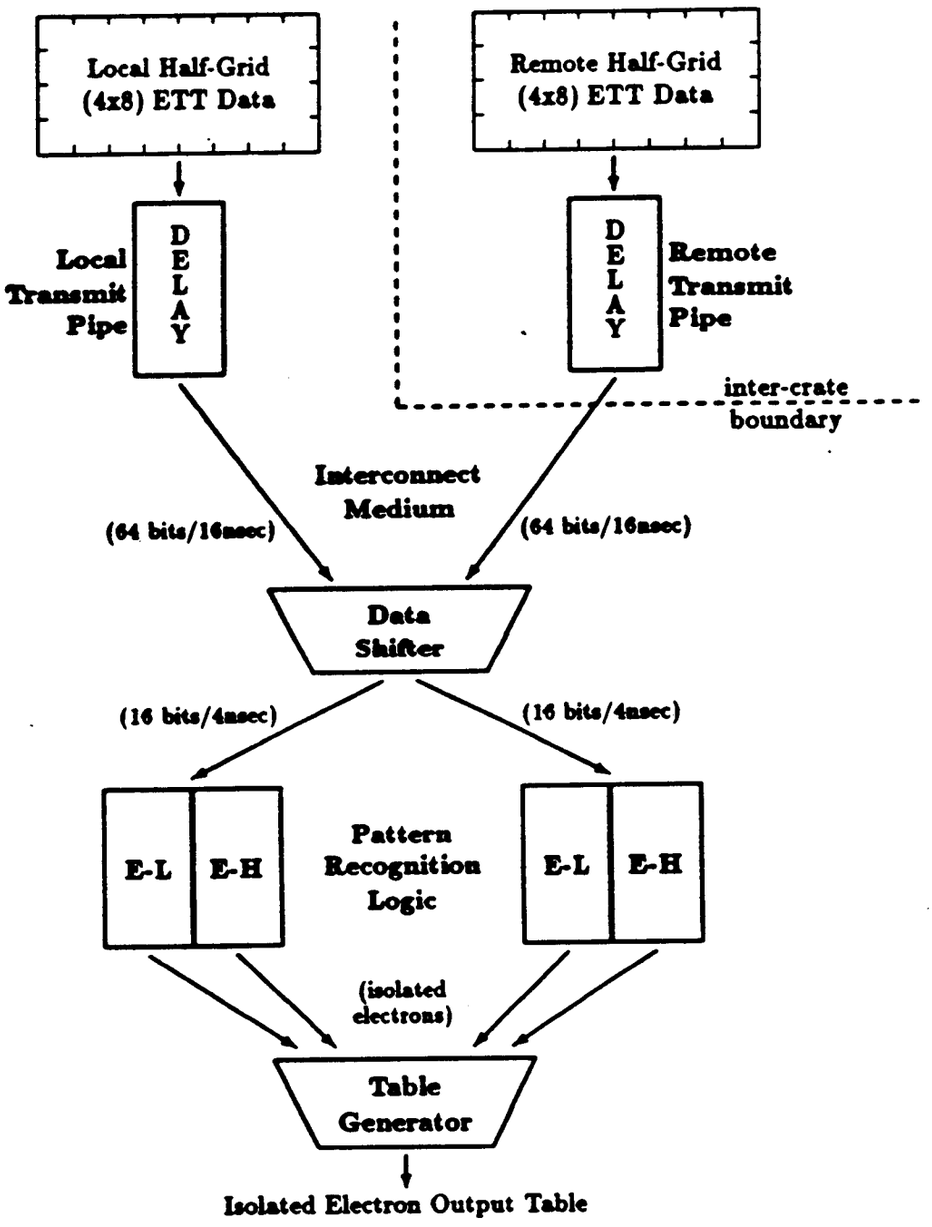


Figure 8: Isolated Electron Detection Hardware for one 8x8 Grid.

Isolated Electron Detection Hardware

KEY FEATURES:

- Pairs up trigger crates to form 8x8 tower regions.
- Low inter-crate interconnect count (1 bit/tower).
- Independent E-L/E-H thresholds for detection.
- Provides {X,Y} location for up to 4 electrons.
- "Drop-In" function into existing crates.
- Robust self-test capabilities.
- Max Clock Rate: 250 MHz.
- Built-in compensation for inter-crate delay.
- Technology currently available.

Calorimeter Triggering: Important Issues

Upstairs / Downstairs:

Do we do minimal calculations on detector and ship 8-fold sums (.05x.05x2long → .1x.1x11long) of EM + HAC to Counting house upstairs? (Jared/Levi's Talk)
Or do we do all Calculations/correlations on detector on full tower granularity of Calorimeter and ship (for example) "electrons" upstairs? (Foster's Talk)

Sparse / Synchronous:

Does each wedge send trigger information for every crossing (every 16 ns) whether there is something or not?
Or does a wedge only send trigger information with a bunch crossing tag when there is something

Correlation w/ other Subsystems, Global system.
Define an overall structure that can be placed either:

- On detector with minimal (or nothing) upstairs
- Upstairs where the entire detector η-ϕ space is mapped onto racks.

Correlating Tracking with Calorimetry:

Electrons: (.1 x .1)
$|\eta| < 1.5$: 64 ϕ x 32 η Towers w/ EM + HAC Energy
$1.5 < |\eta| < 3.0$: 64 ϕ x 6 η Towers w/ EM + HAC Energy
Shower Max: Barrel: 1024 x 2 halves, Each end: 1024
Preshower: 1024 x 2 halves $\Rightarrow \sim$ 1 kHz/wedge of electron triggers

Jets: Fixed Towers .4x.4
Sum Towers over threshold
Get 12 x 16 Towers: Barrel: 8x16, Each End: 2x16.

Totals: (4864 Total)
Calorimeter Electrons: 2432 HAC + 2432 EM
(Shower Max: 4096
Preshower: 2048)
x 8 bits Energy

Calorimeter Jets 192 Towers

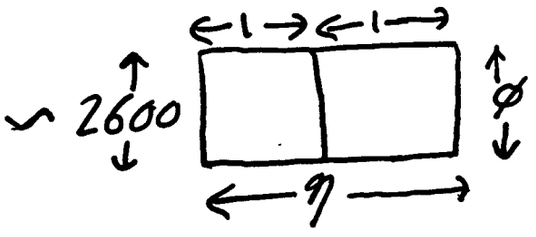
Average Occupancy $\sim$ ½% per Cal channel
x 8 fold Sum = 4%.

Central Tracking Triggers:

Fiber Tracker:

4 bits P_T: 1024 ϕ bins x 2 η bins = **2048 bins x 4 bits P_T**
from 32 Crates (16 on each half)
Rate: 1 track >10 GeV / 6 Crossings at 10^{33}

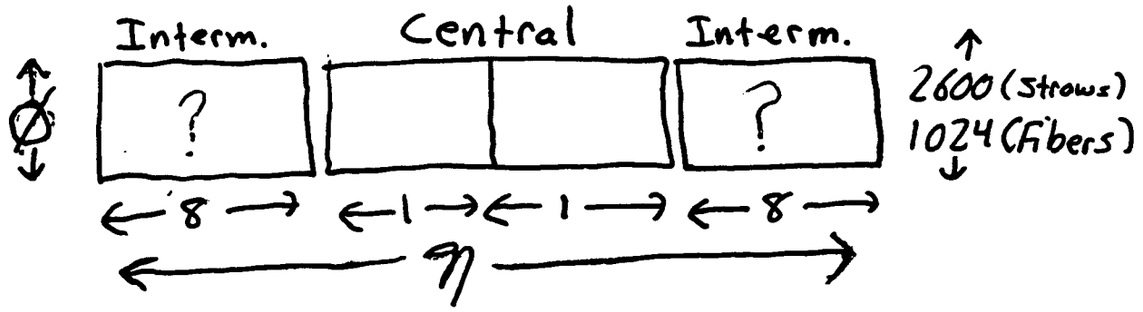
Straw Tube Tracker



2600 ϕ x 2 η bins = **5200 bins over P_T thr.**

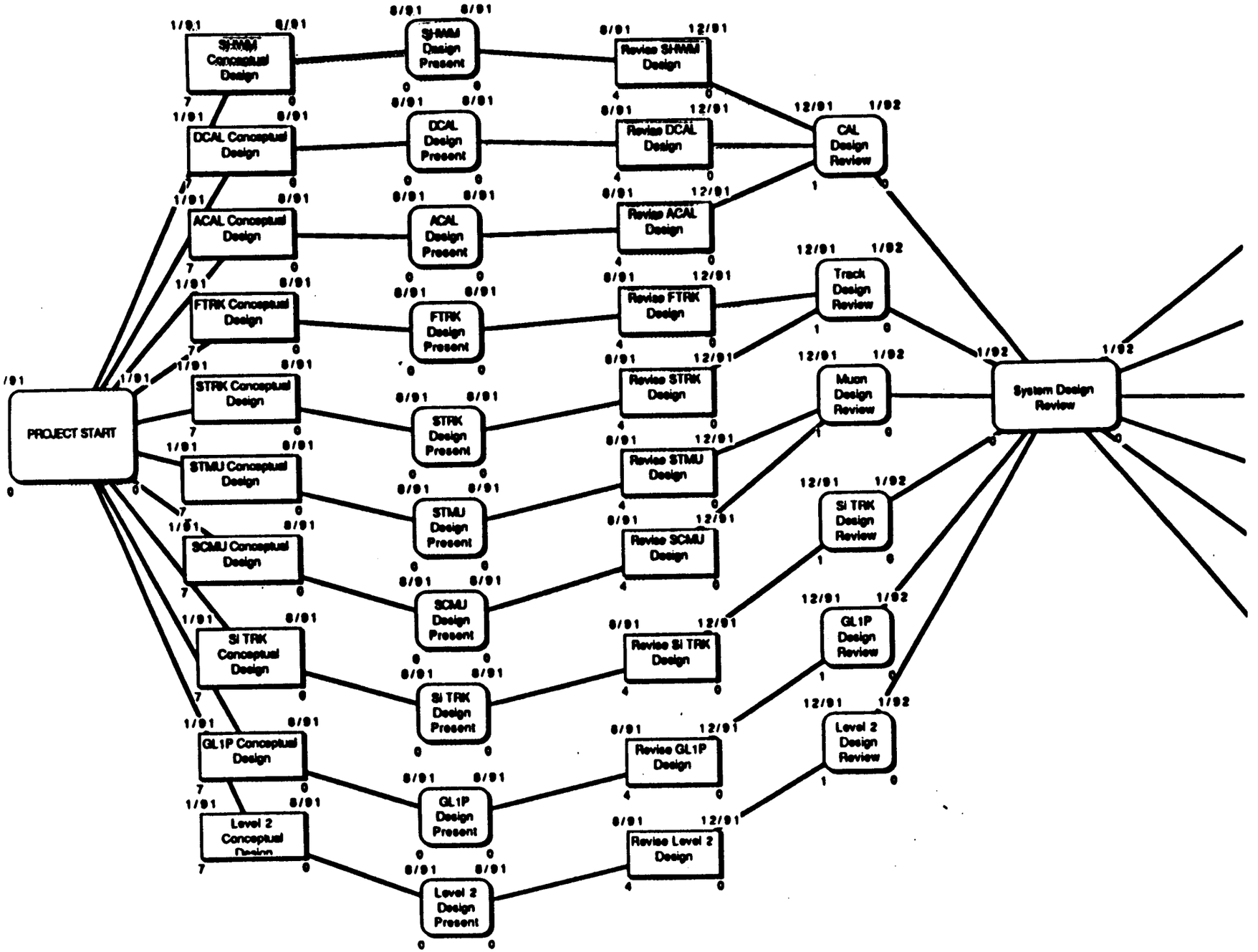
straw tube occupancy $\lesssim$ 4% at 10^{33}

Total Track Trigger Granularity



Total Bins:

Straws: 26k = 5k Central + 21k Intermediate
Fibers: 10k = 2k Central + 8k Intermediate


PROJECT START
SI-HMM Conceptual Design
DCAL Conceptual Design
ACAL Conceptual Design
FTRK Conceptual Design
STRK Conceptual Design
STMU Conceptual Design
SCMU Conceptual Design
SI TRK Conceptual Design
GL1P Conceptual Design
Level 2 Conceptual Design
SI-HMM Design Present
DCAL Design Present
ACAL Design Present
FTRK Design Present
STRK Design Present
STMU Design Present
SCMU Design Present
SI TRK Design Present
GL1P Design Present
Level 2 Design Present
Revise SI-HMM Design
Revise DCAL Design
Revise ACAL Design
Revise FTRK Design
Revise STRK Design
Revise STMU Design
Revise SCMU Design
Revise SI TRK Design
Revise GL1P Design
Revise Level 2 Design
CAL Design Review
Track Design Review
Muon Design Review
SI TRK Design Review
GL1P Design Review
Level 2 Design Review
System Design Review

TRIGGER R&D

Calorimeter Isolated Electron Trigger Logic

- Start with Digitized Tower Energies
- Electron ID MLU:
  - 8 bits EMC Tower Energy
  - 8 bits HAC Tower Energy
  - → Electron ID bit, threshold bit
- Isolation Pattern MLU:
  - Identify EM clusters
  - Check Isolation
  - Count Total vs. Threshold
  - Info. for Correlation w/track
- Progress: Computer Model of Function
- Goal (this year):
  - MC studies
  - Conceptual Design

Global Level 1 Trigger

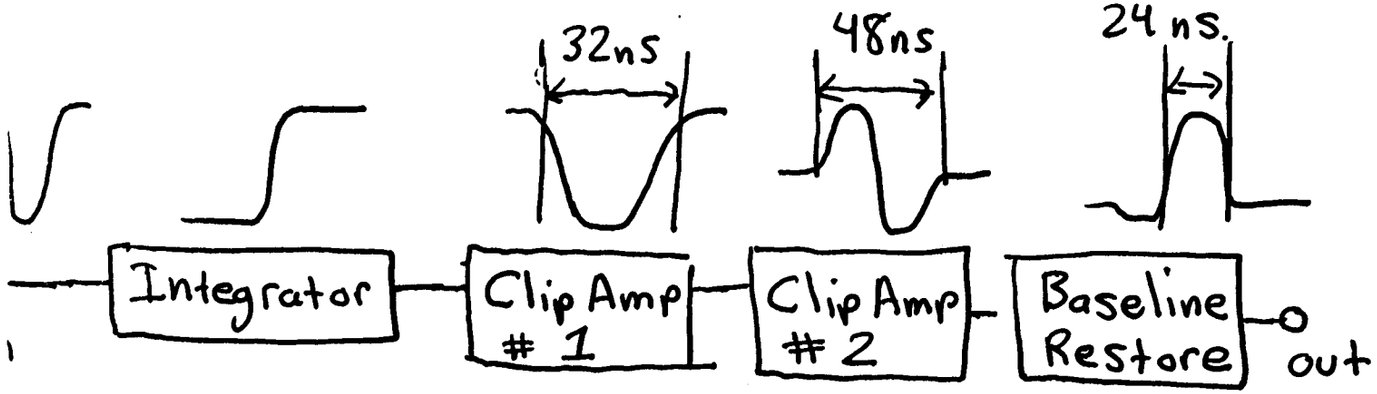
- L1 Clock Distribution to Subsystems
- L1 ⇔ Subsystem Control Interface
- Correlation and Trigger Logic
- Trigger Decision Logic
- Progress:
  - Preliminary Design Document
  - Simulation Module Conceptual Design
- Goal (this year):
  - Simulation Module
  - Conceptual Design

Preamplifier for PMT → SCA

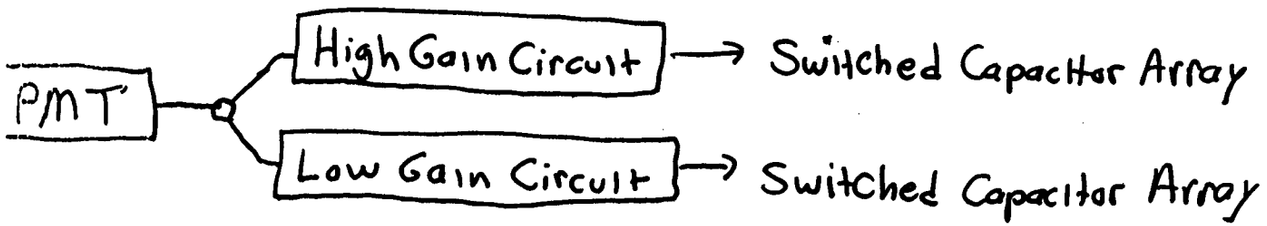
D. Panescu, P. Robl, W. Smith

U. Wisconsin

SSC Calorimeter Integration + Baseline Restoration Circuit:

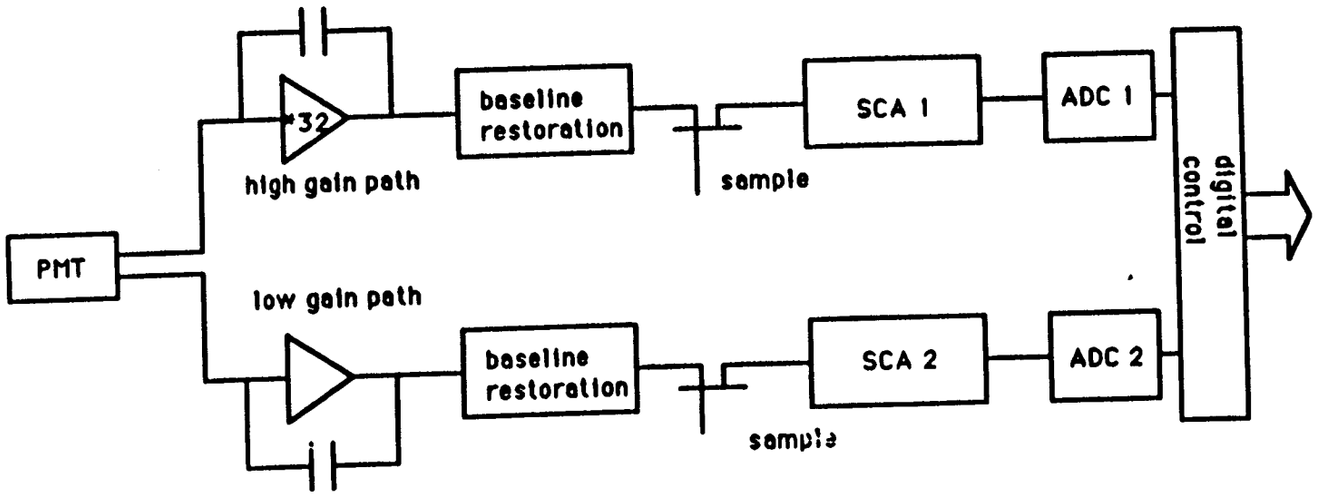


Application:



Able to transfer charge in 16ns

Able to correctly amplify in High gain after pulse on low gain scale (saturates high gain)


PMT
32
high gain path
baseline restoration
sample
SCA 1
ADC 1
digital control
low gain path
baseline restoration
sample
SCA 2
ADC 2

OUTLINE FOR THE INPUT STAGE REQUIREMENTS

1. INTEGRATION OVER A WIDE DYNAMIC RANGE

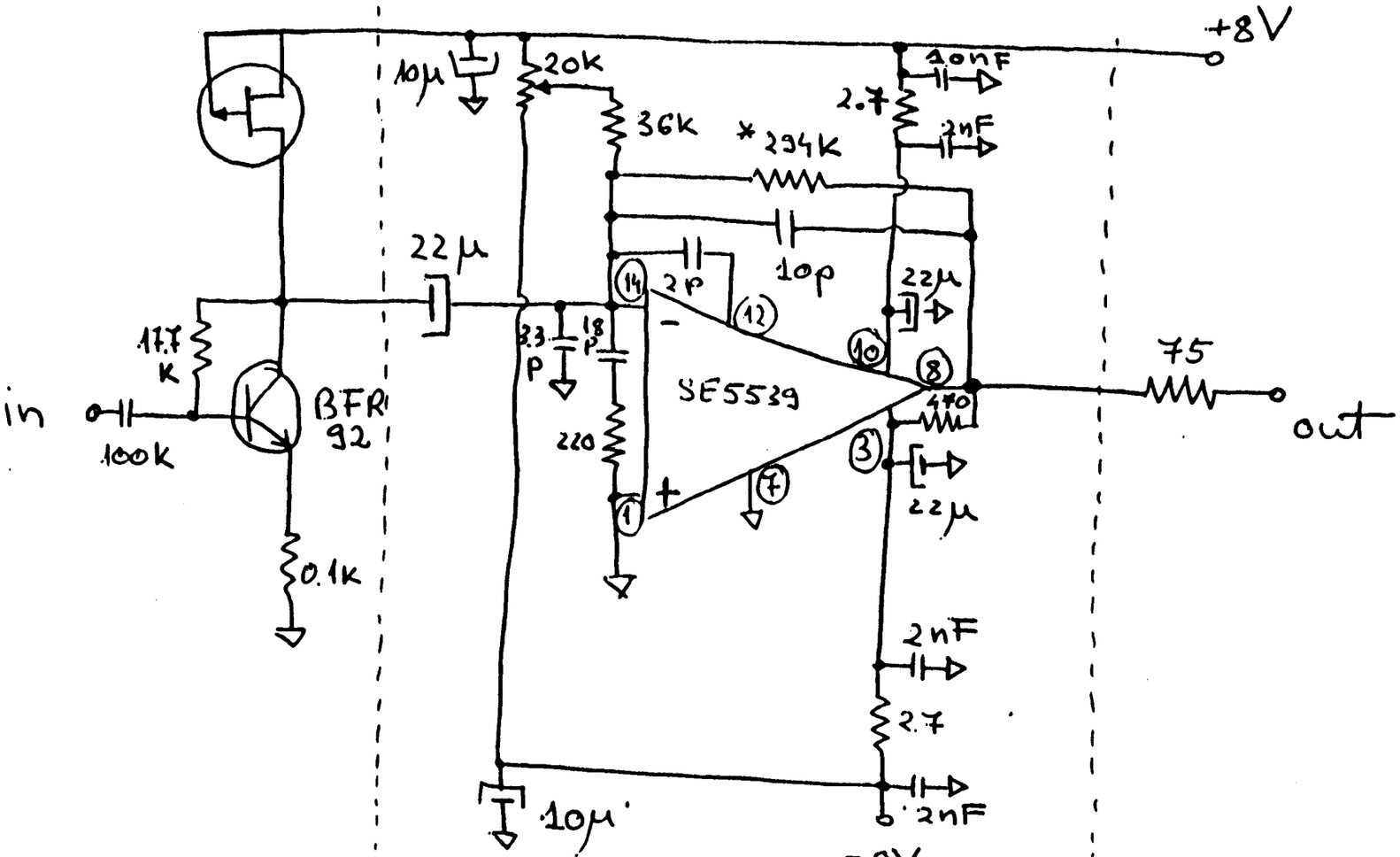
-INPUT SIGNAL DYNAMIC RANGE: 104dB
-DURATION OF THE INPUT SIGNAL: 16nS
-DROOP OVER 4nS : 1LSB OF 12 BITS
-SOLUTION : TO USE A HIGH GAIN AND A LOW GAIN PATH. THE HIGH/LOW GAIN RATIO SHOULD BE 32.

2.BASELINE RESTORATION

-IF A HIGH LEVEL INPUT PULSE IS FOLLOWED BY A LOW LEVEL ONE THE DYNAMIC RANGE MIGHT BE AFFECTED BY THE SATURATION OF SOME OF THE DEVICES WITHIN HIGH GAIN PATH. TO AVOID THIS PHENOMENON THE BASELINE HAS TO BE RESTORED IMMEDIATELY AFTER THE INTEGRATION ENDS. THE CLIP AMP IS USED FOR ACCOMPLISHING THIS REQUIREMENT AND A SOLUTION FOR RESTORATION OF THE BASELINE AT THE INTEGRATOR OUTPUT IS ON THE WAY TO BE TESTED.

3.THE STORAGE OF THE SAMPLED SIGNAL IN A ANALOG MEMORY(SCA)

-USE 2 SEPARATE SCA's-ONE EACH FOR HIGH AND LOW GAIN PATHS. EACH HAS 12 BIT DYNAMIC RANGE. GAIN RATIO IS 1/32.

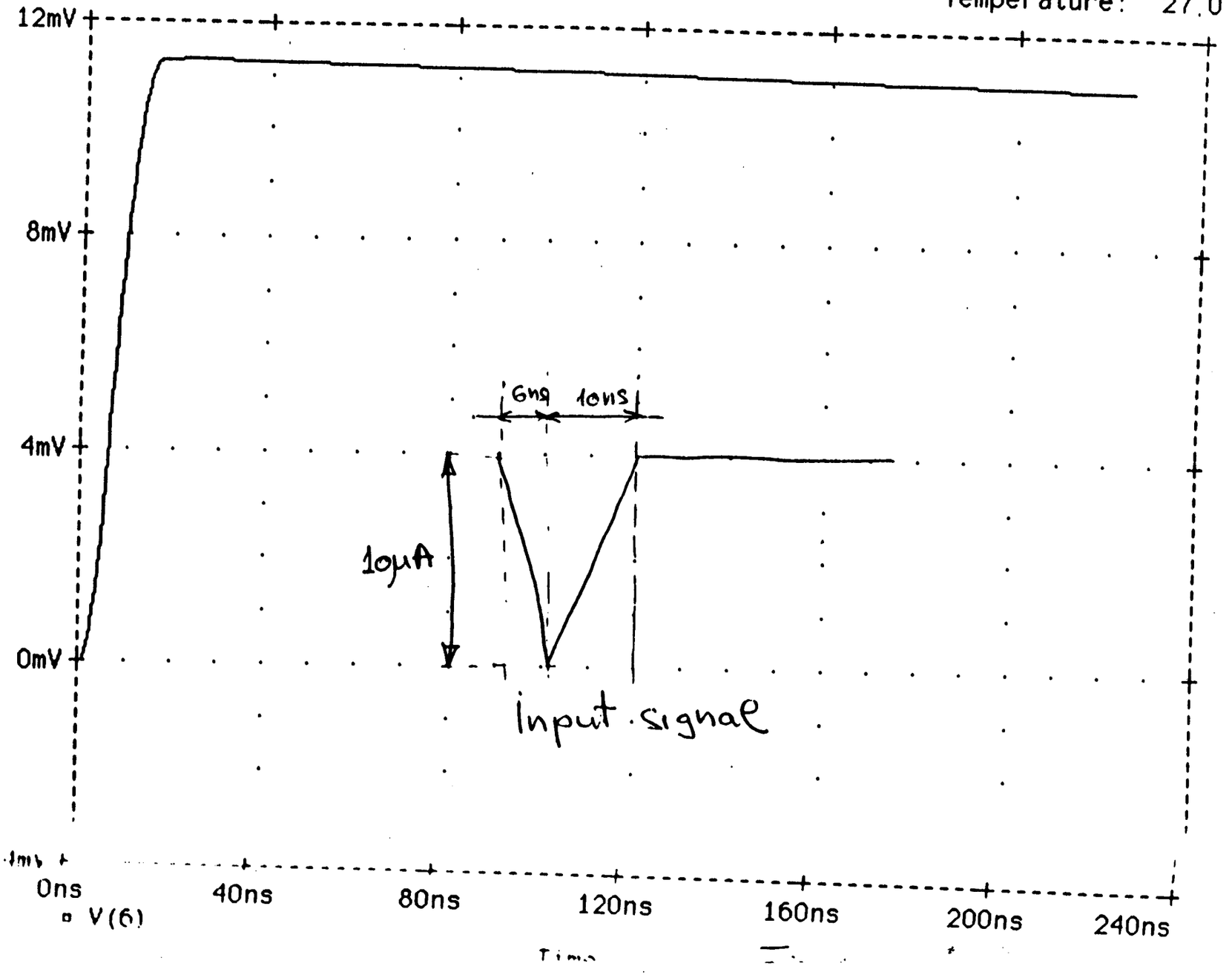


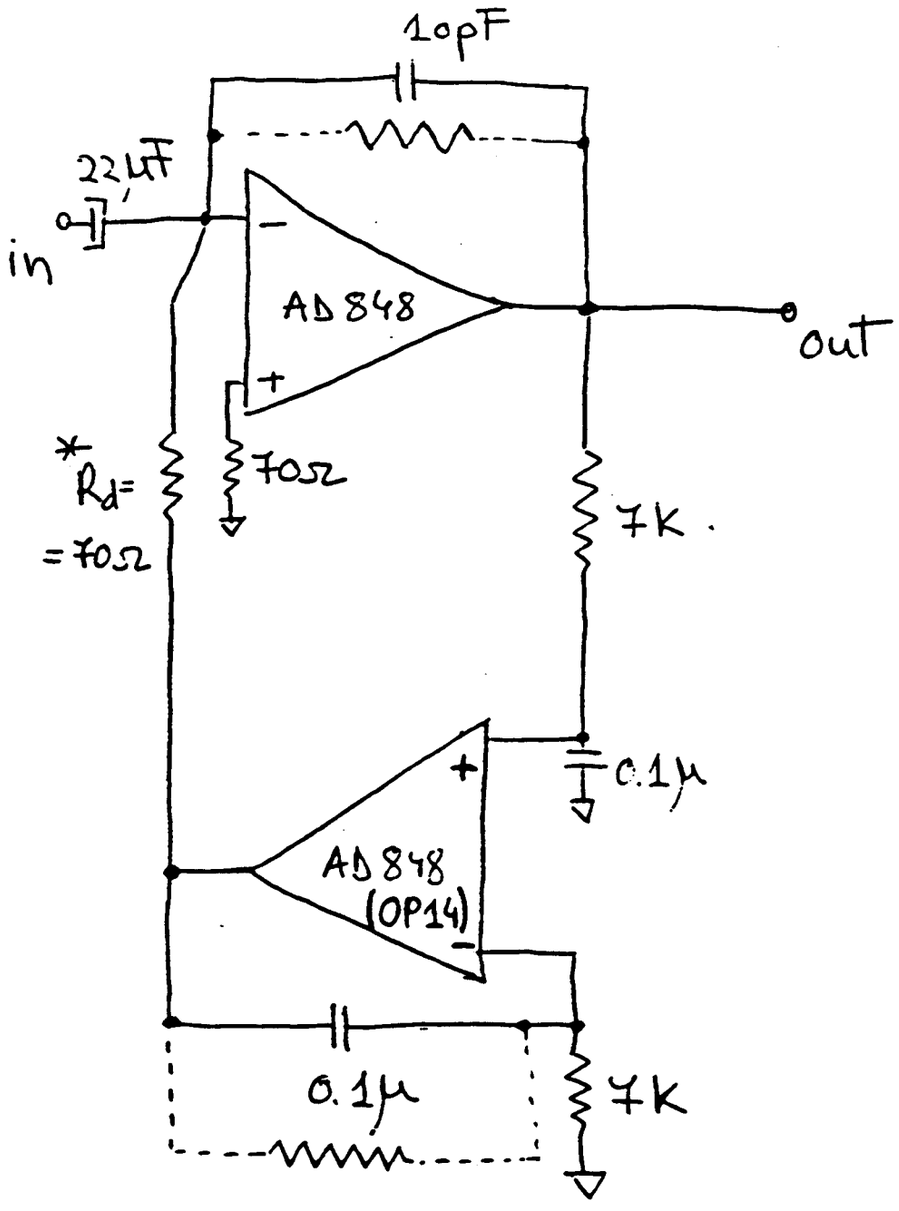
Integrator with NE/SE 5539

Test equipment

Date/Time run: 04/15/91 10:55:43

Temperature: 27.0



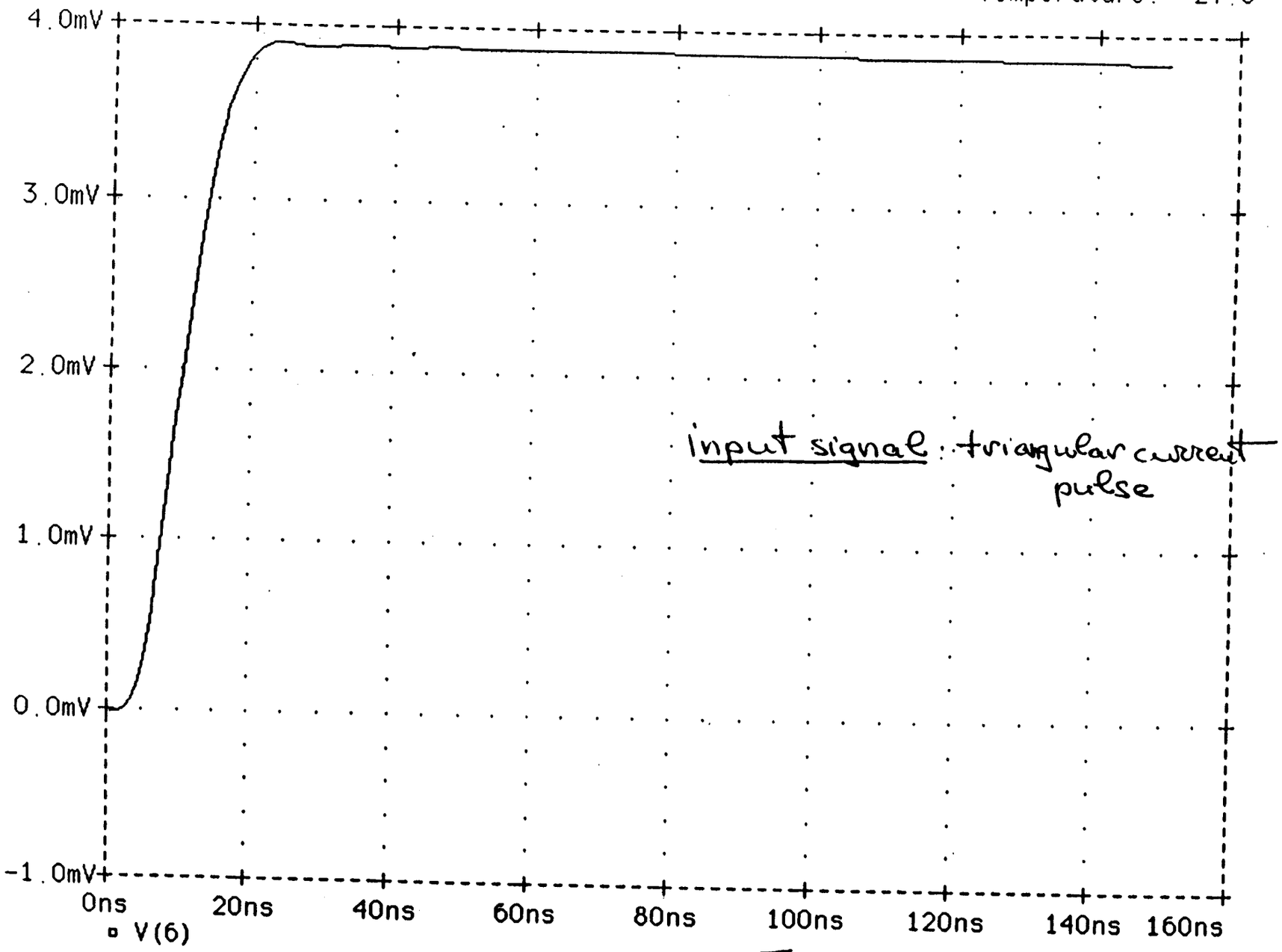


Integrator using AD 848.

$R_g = 50\Omega$

Date/Time run: 04/23/91 10:16:52

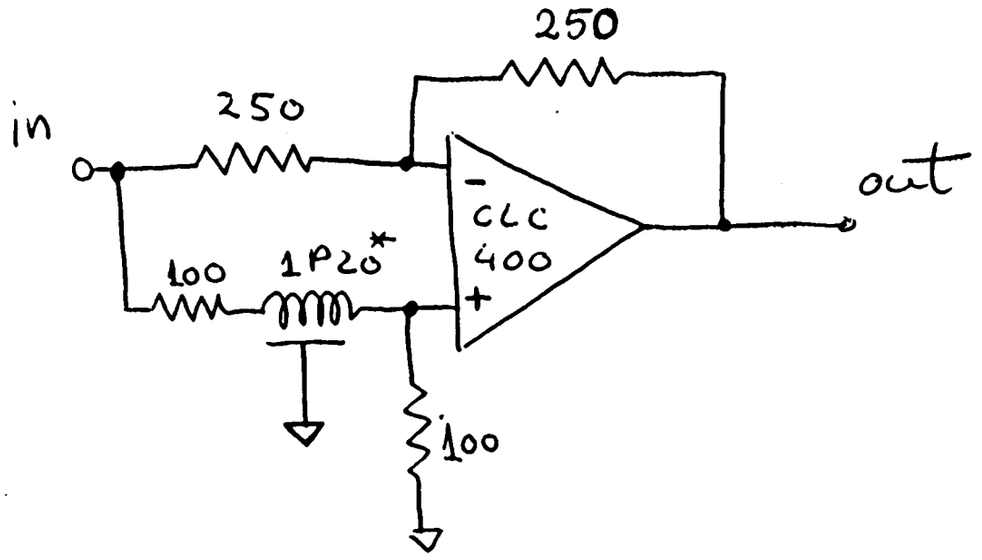
Temperature: 27.0



input signal : triangular current pulse

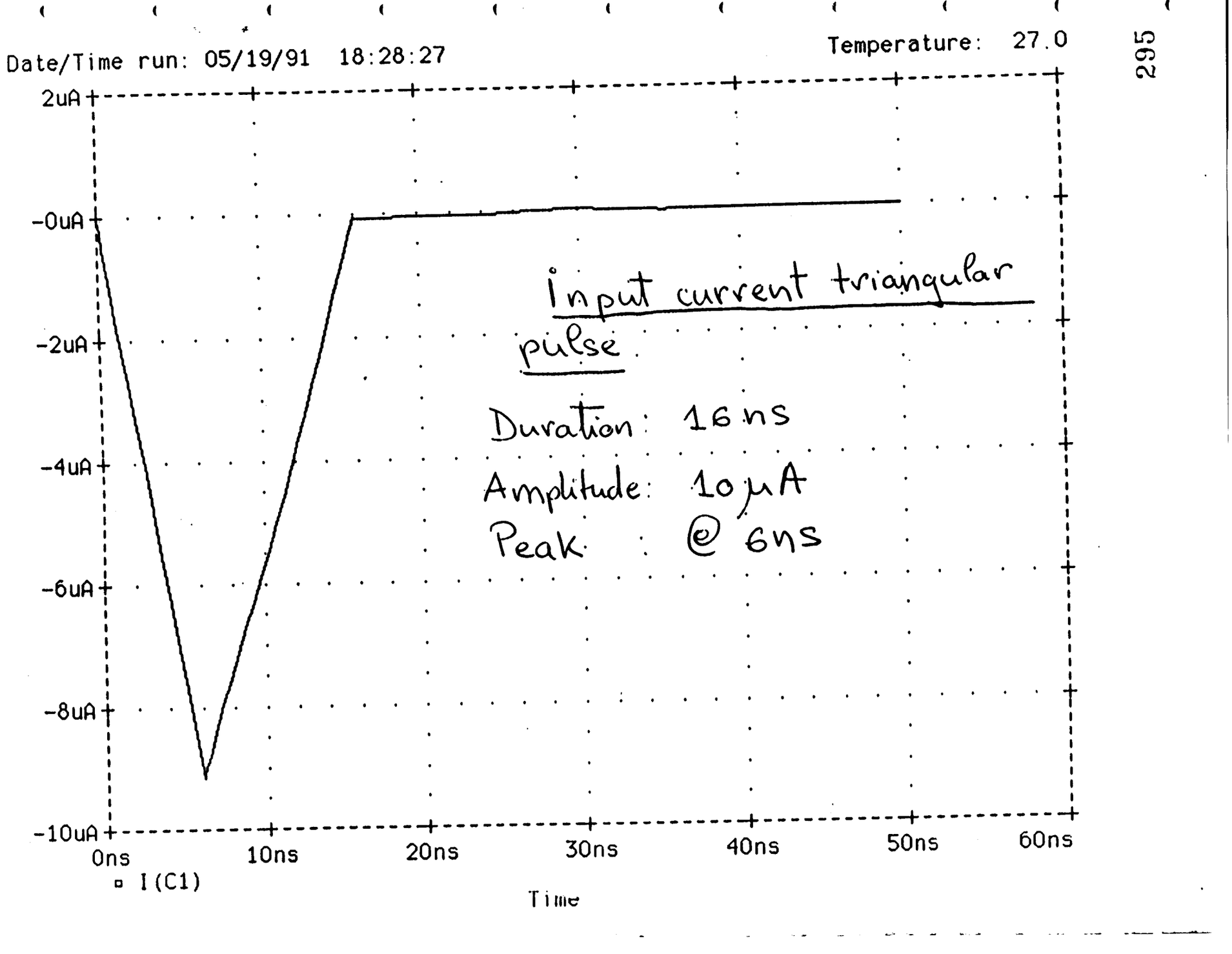
Fig 14

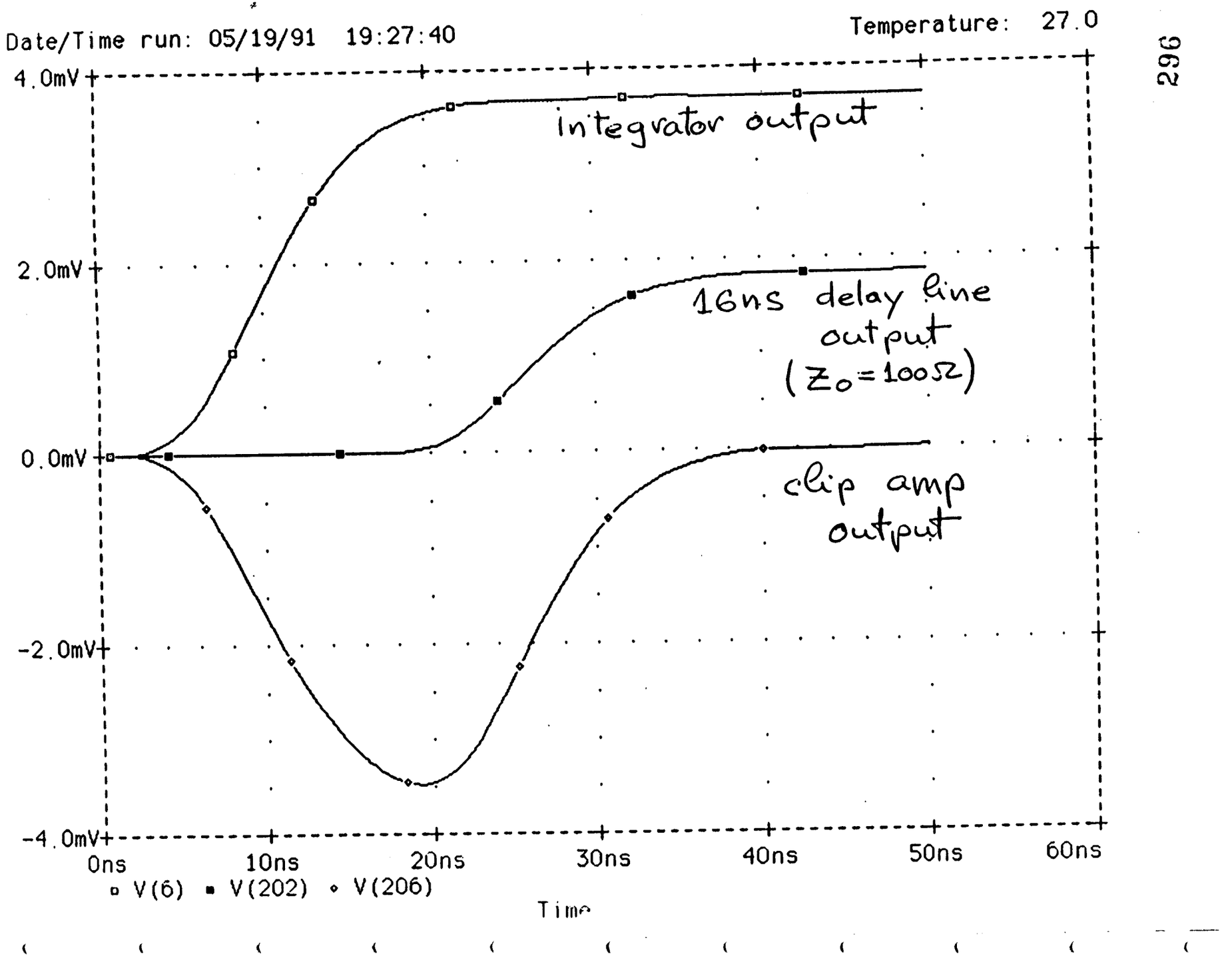
2N2
Inverter
2N2
Clamp and Hold
2N3565
4200
4200
2N2222
V_H
22
.05μF
2N2
$V_{0.2}$ = +3.0V
(Hold and Trigger Pulse)
2N3565

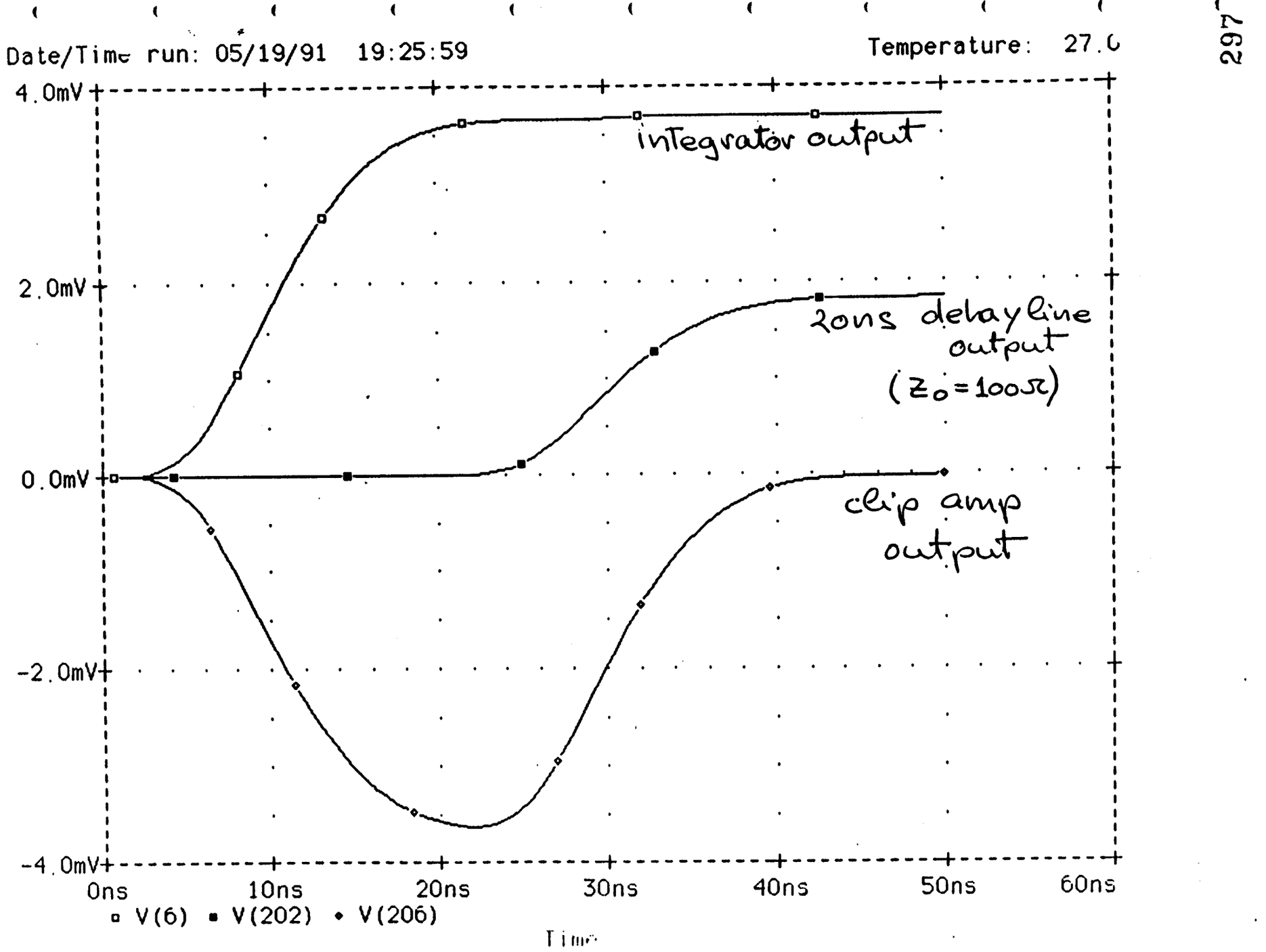


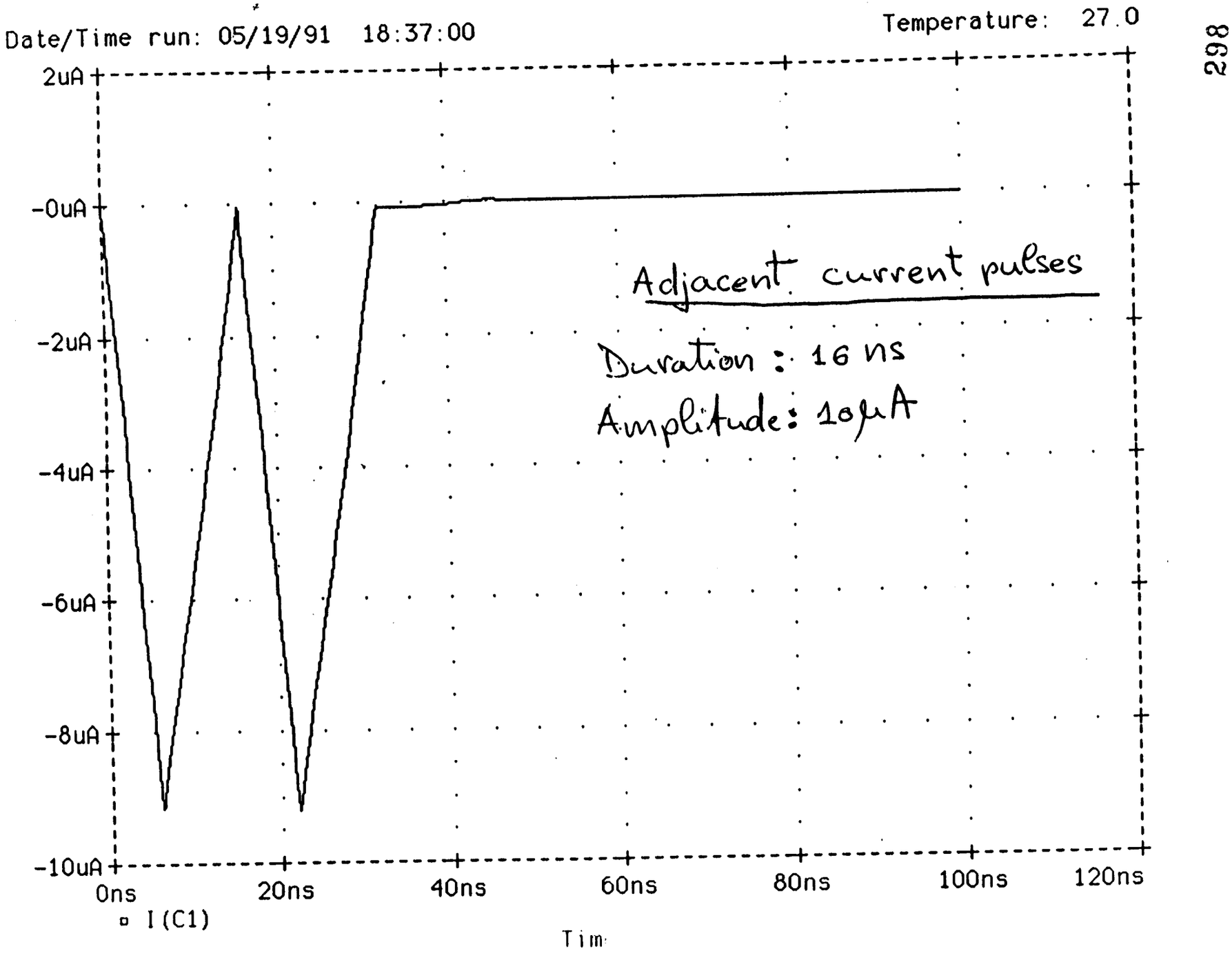
1P20 * → delay line 20ns, 20 taps.

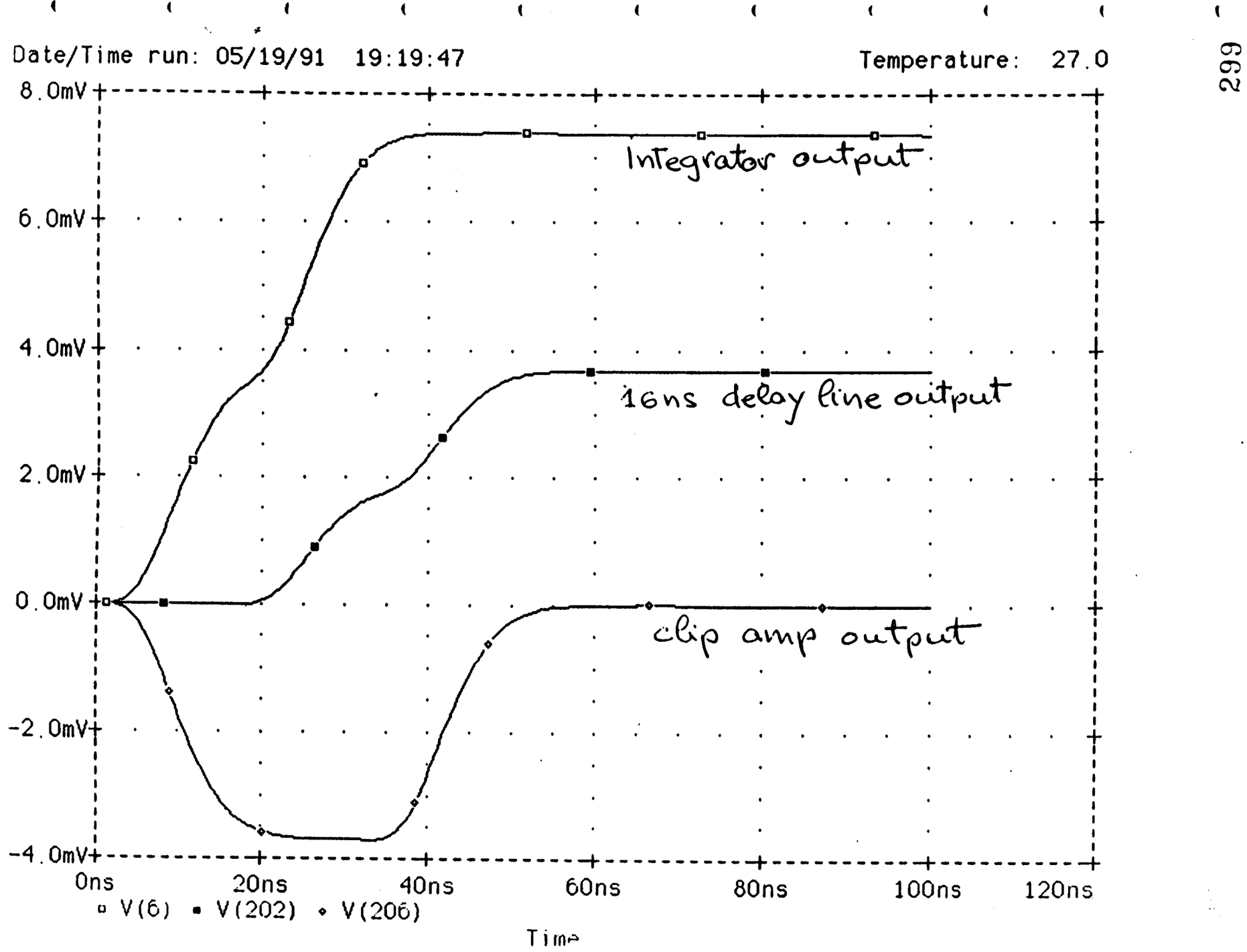
Clip amp using CLC 400

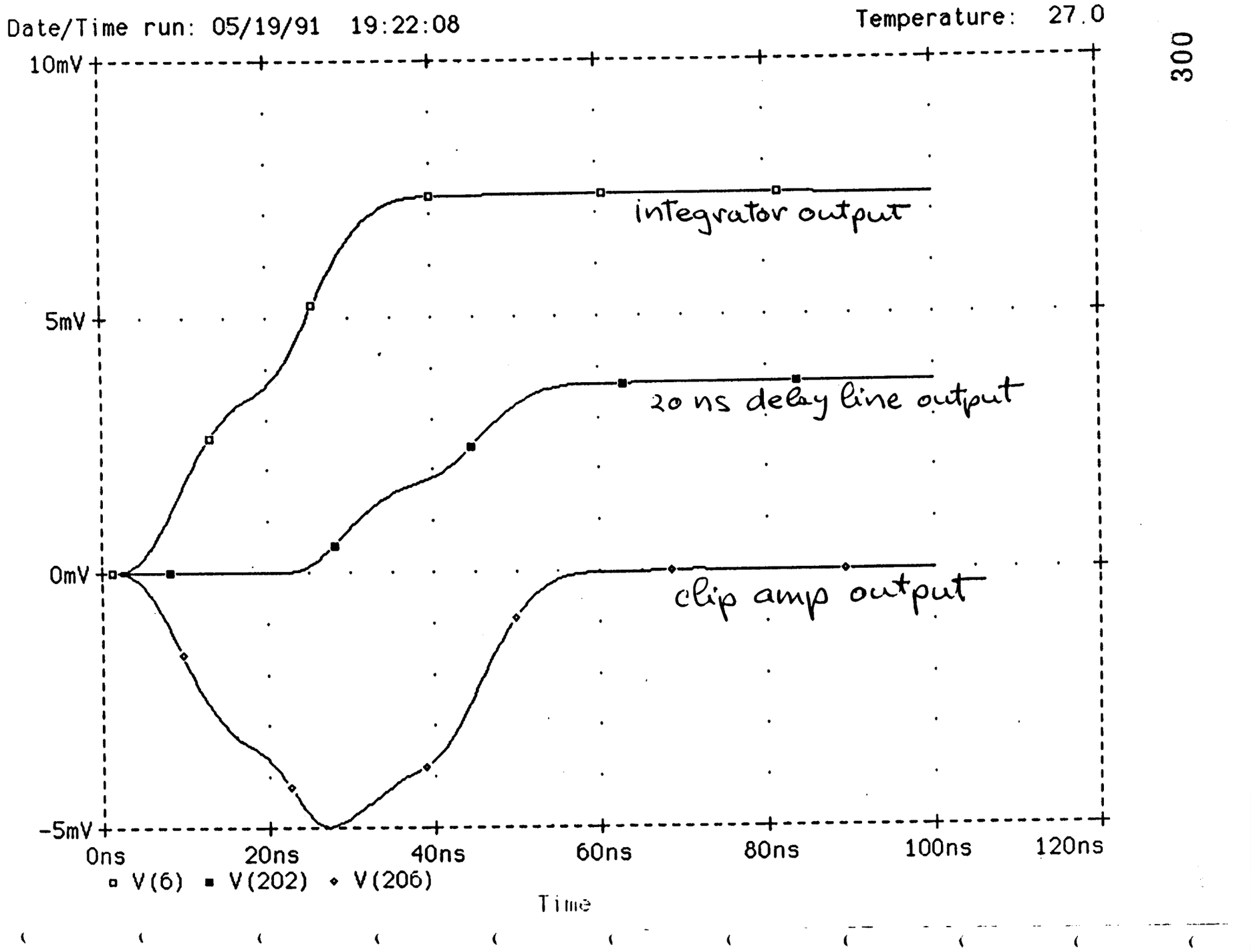

Date/Time run: 05/19/91 18:28:27
Temperature: 27.0
2uA
-0uA
-2uA
-4uA
-6uA
-8uA
-10uA
0ns
10ns
20ns
30ns
40ns
50ns
60ns
I(C1)
Time
Input current triangular pulse
Duration: 16 ns
Amplitude: 10 μA
Peak : @ 6ns

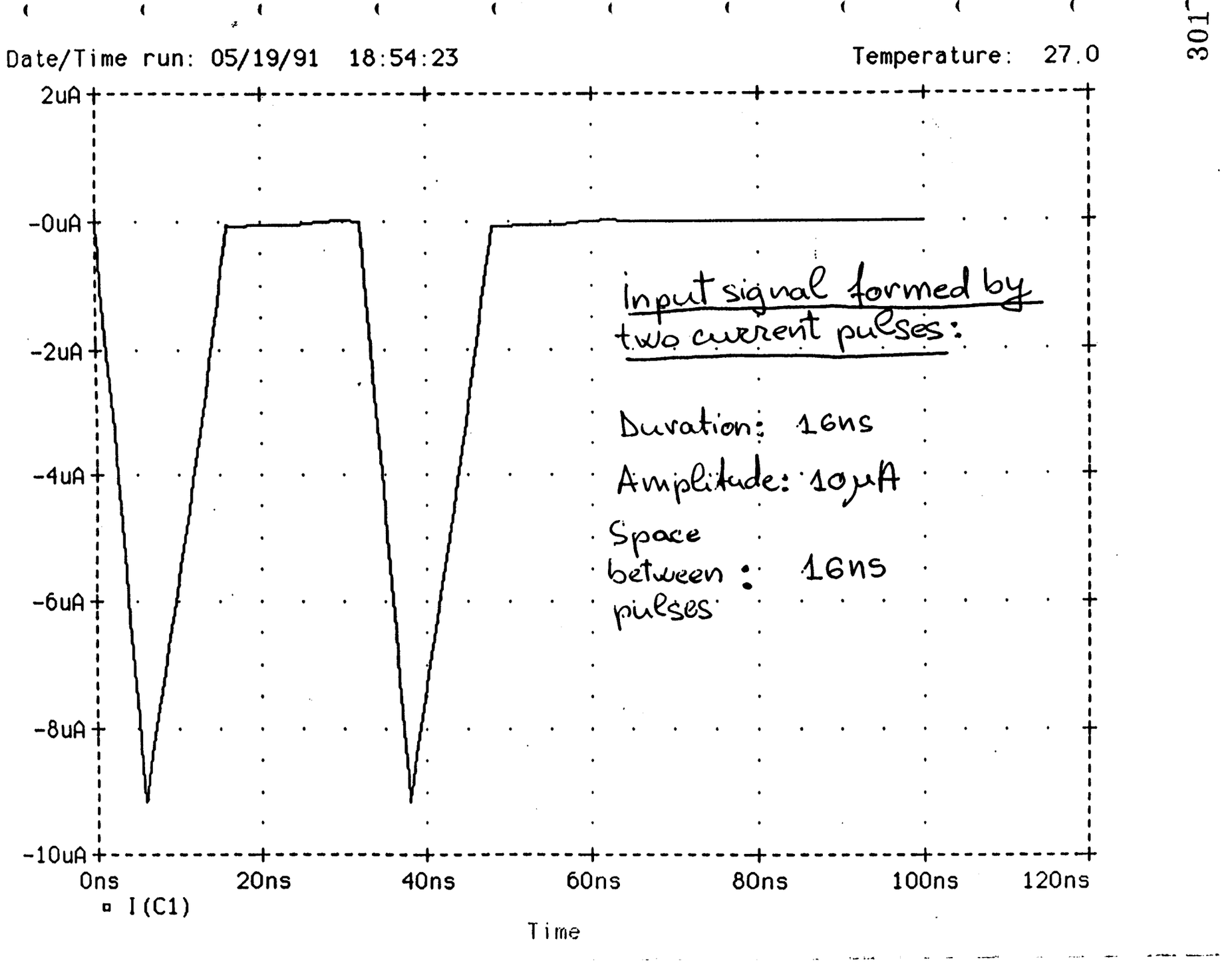

Date/Time run: 05/19/91 19:27:40
Temperature: 27.0
296
4.0mV
2.0mV
0.0mV
-2.0mV
-4.0mV
integrator output
16ns delay line output (Z_o=100Ω)
clip amp output
0ns
10ns
20ns
30ns
40ns
50ns
60ns
▫ V(6) ▪ V(202) ◇ V(206)
Time

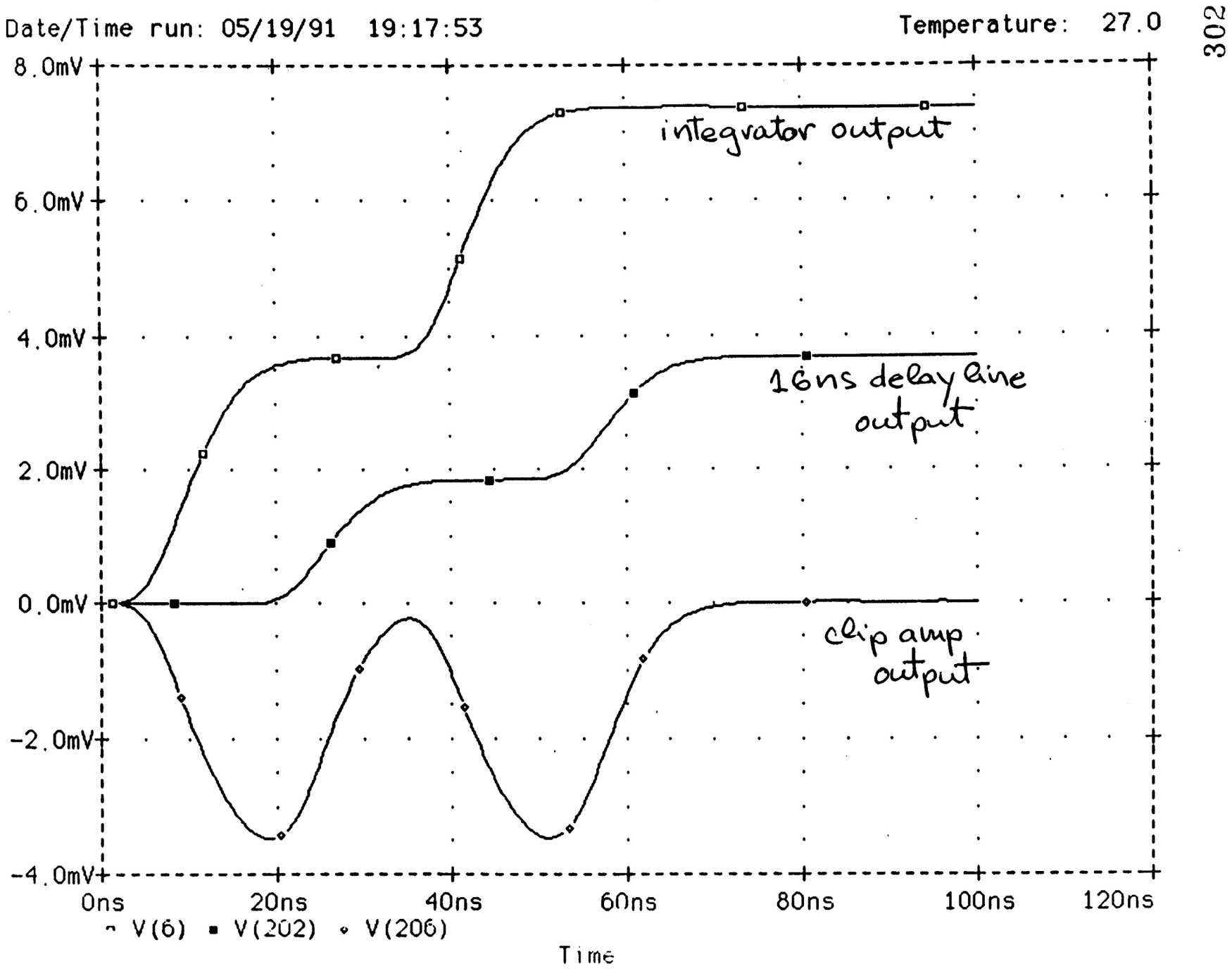

Date/Time run: 05/19/91 19:25:59
Temperature: 27.0
4.0mV
2.0mV
0.0mV
-2.0mV
-4.0mV
0ns
10ns
20ns
30ns
40ns
50ns
60ns
integrator output
20ns delay line output
(Z0=100Ω)
clip amp output
V(6) V(202) V(206)
Time

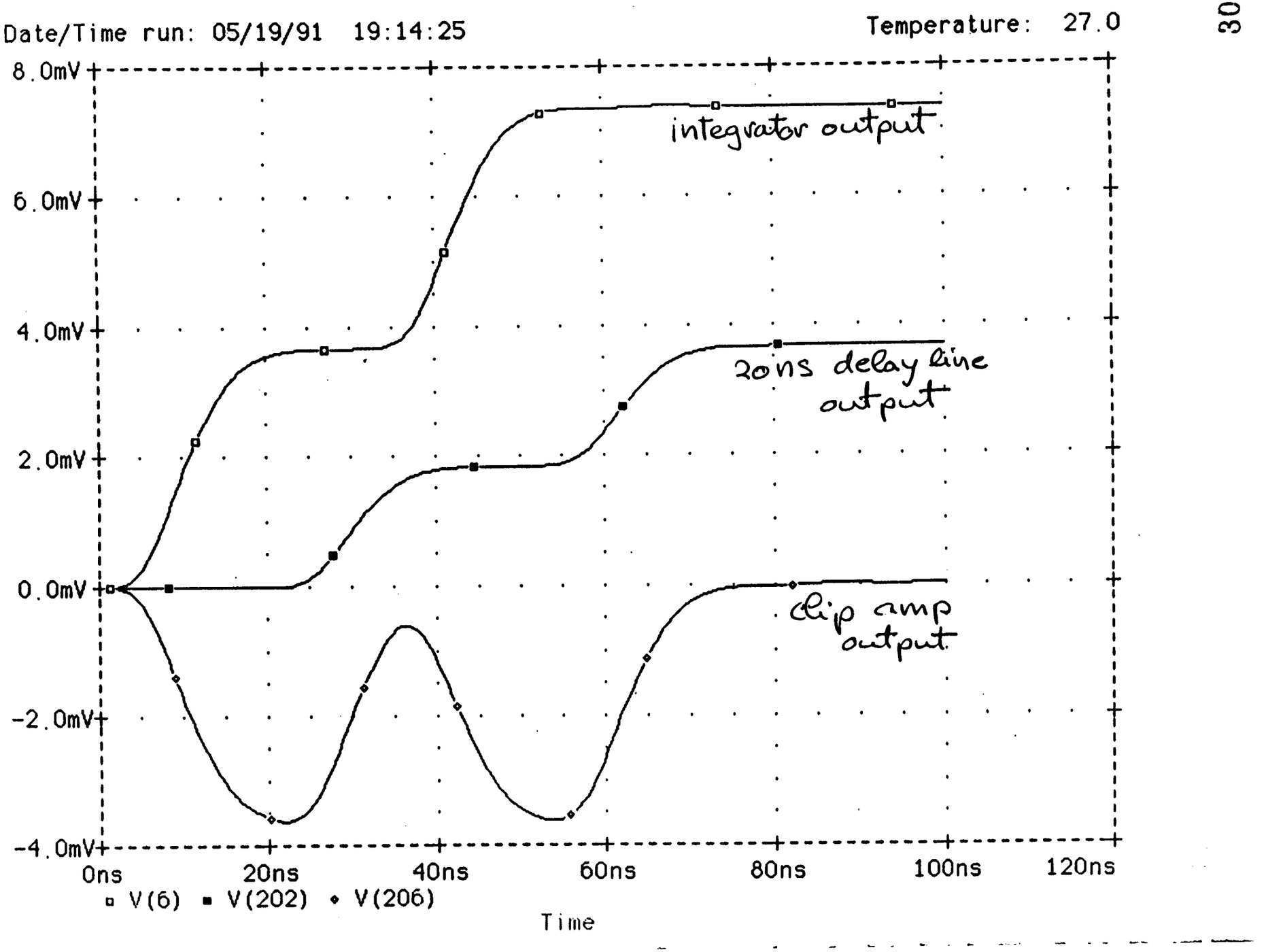

Date/Time run: 05/19/91 18:37:00
Temperature: 27.0
2uA
-0uA
-2uA
-4uA
-6uA
-8uA
-10uA
0ns
20ns
40ns
60ns
80ns
100ns
120ns
I(C1)
Tim
Adjacent current pulses
Duration : 16 ns
Amplitude: 10μA

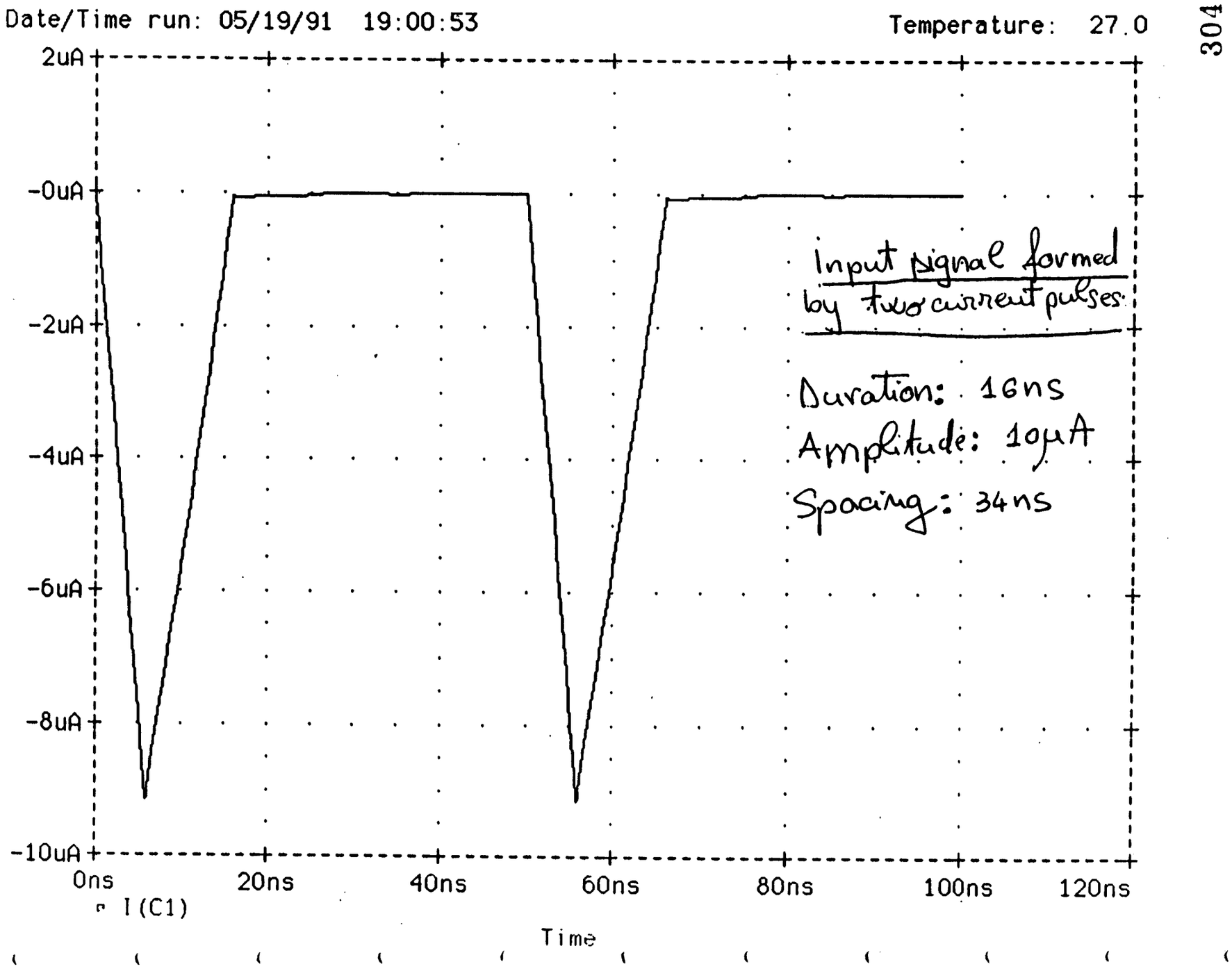

Date/Time run: 05/19/91 19:19:47
Temperature: 27.0
8.0mV
6.0mV
4.0mV
2.0mV
0.0mV
-2.0mV
-4.0mV
Integrator output
16ns delay line output
clip amp output
0ns
20ns
40ns
60ns
80ns
100ns
120ns
V(6) V(202) V(206)
Time

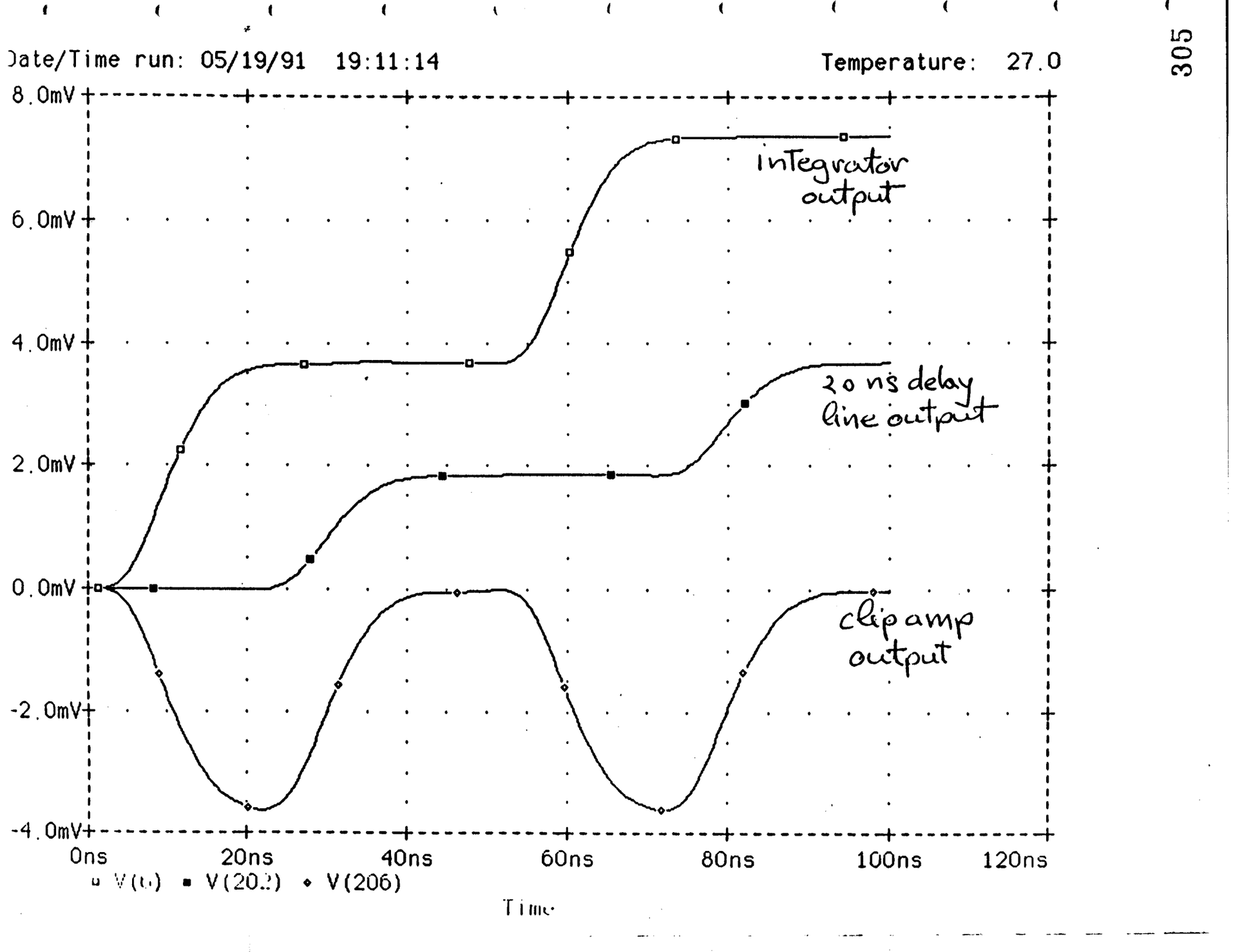

Date/Time run: 05/19/91 19:22:08
Temperature: 27.0
300
10mV
5mV
0mV
-5mV
integrator output
20 ns delay line output
clip amp output
0ns
20ns
40ns
60ns
80ns
100ns
120ns
V(6) V(202) V(206)
Time


Date/Time run: 05/19/91 18:54:23
Temperature: 27.0
2uA
-0uA
-2uA
-4uA
-6uA
-8uA
-10uA
0ns
20ns
40ns
60ns
80ns
100ns
120ns
I(C1)
Time
Input signal formed by two current pulses:
Duration: 16ns
Amplitude: 10μA
Space between pulses: 16ns

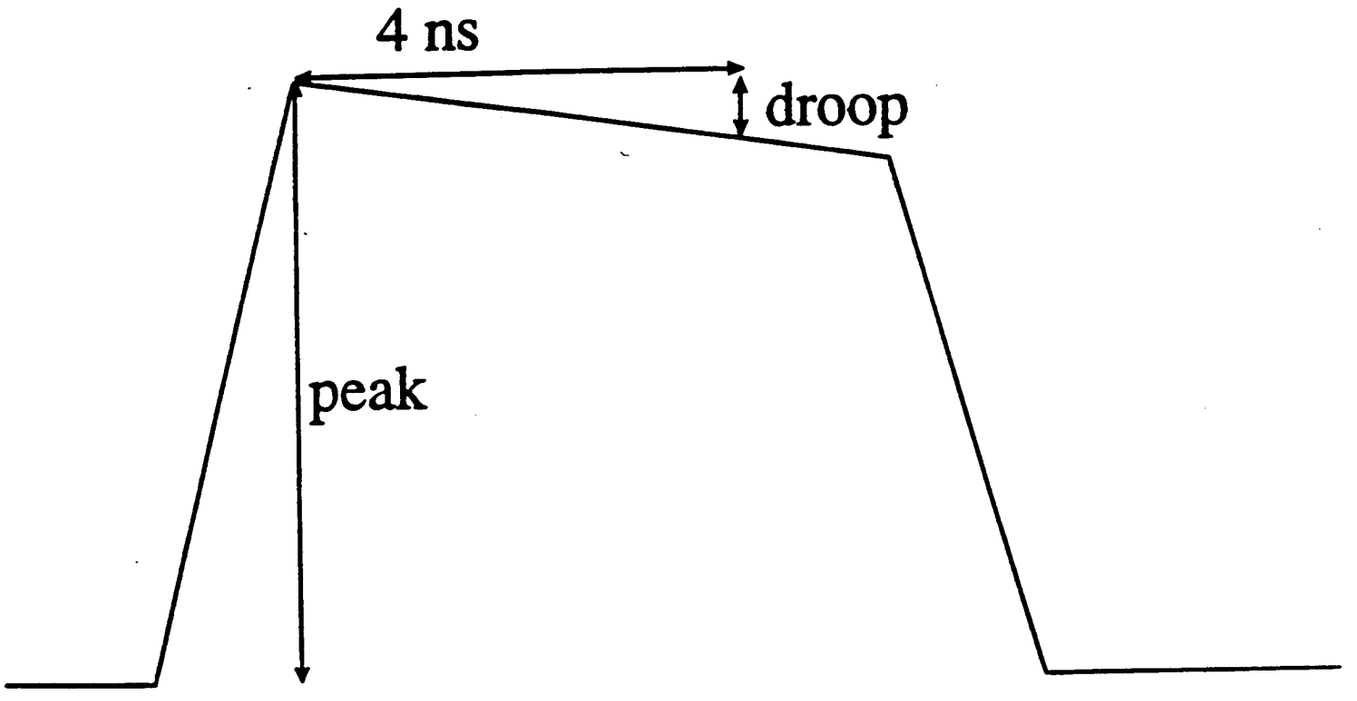

Date/Time run: 05/19/91 19:17:53
Temperature: 27.0
8.0mV
6.0mV
4.0mV
2.0mV
0.0mV
-2.0mV
-4.0mV
0ns
20ns
40ns
60ns
80ns
100ns
120ns
integrator output
16ns delay line output
clip amp output
V(6) V(202) V(206)
Time


Date/Time run: 05/19/91 19:14:25
Temperature: 27.0
8.0mV
6.0mV
4.0mV
2.0mV
0.0mV
-2.0mV
-4.0mV
integrator output
20ns delay line output
clip amp output
0ns
20ns
40ns
60ns
80ns
100ns
120ns
V(6) V(202) V(206)
Time


Date/Time run: 05/19/91 19:00:53
Temperature: 27.0
2uA
-0uA
-2uA
-4uA
-6uA
-8uA
-10uA
0ns
20ns
40ns
60ns
80ns
100ns
120ns
I(C1)
Time
Input signal formed by two current pulses
Duration: 16ns
Amplitude: 10μA
Spacing: 34ns

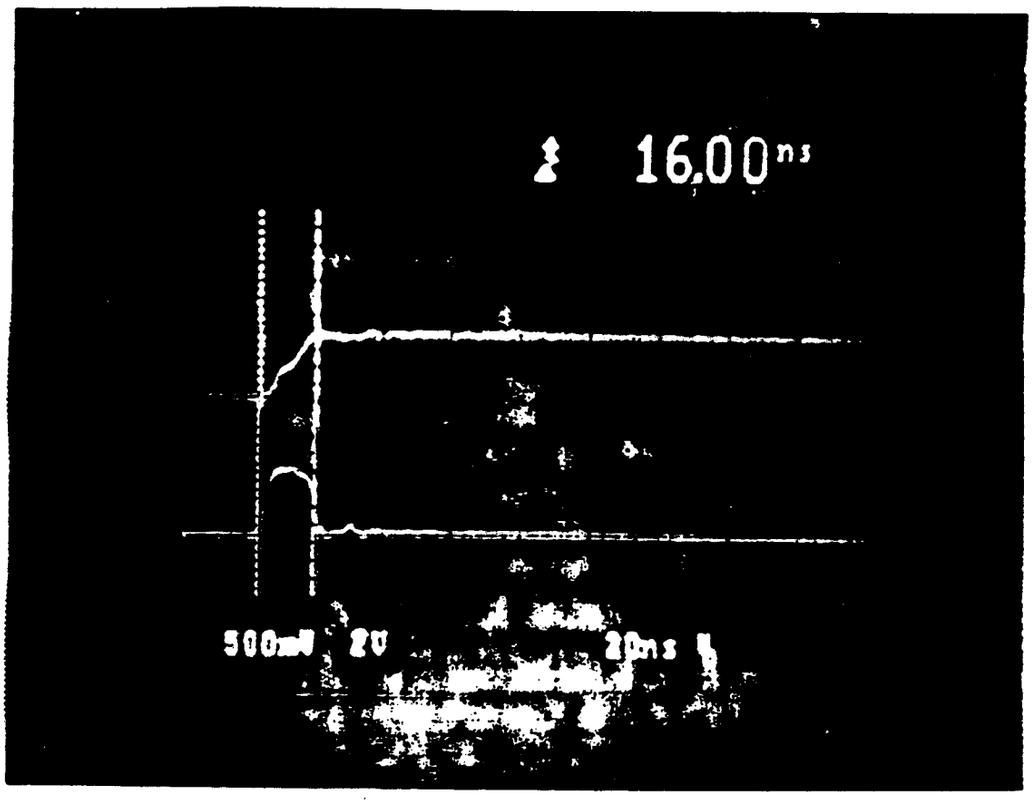

Date/Time run: 05/19/91 19:11:14
Temperature: 27.0
8.0mV
6.0mV
4.0mV
2.0mV
0.0mV
-2.0mV
-4.0mV
0ns
20ns
40ns
60ns
80ns
100ns
120ns
integrator output
20 ns delay line output
clip amp output
V(6)
V(20?)
V(206)
Time

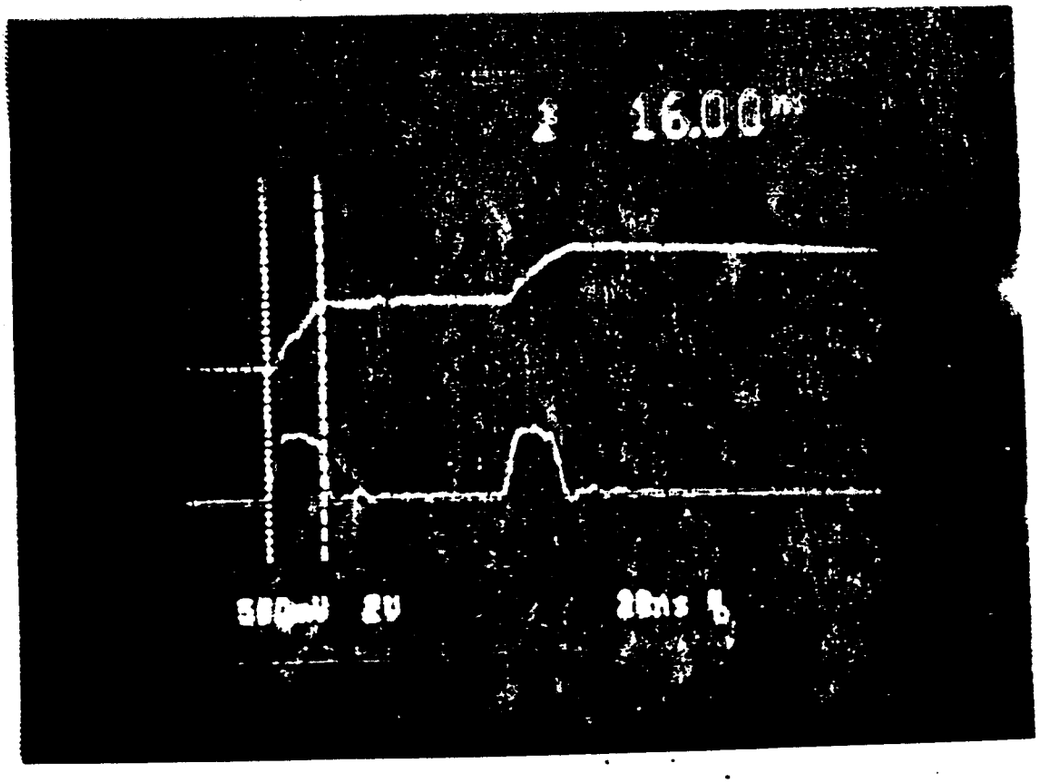
DELAY LINE	DROOP OVER 4NS AFTER THE PEAK
16NS /AD 848	15%
16NS /SE 5539	13%
22NS /AD 848	2.48%
22NS /SE 5539	< 0.1%

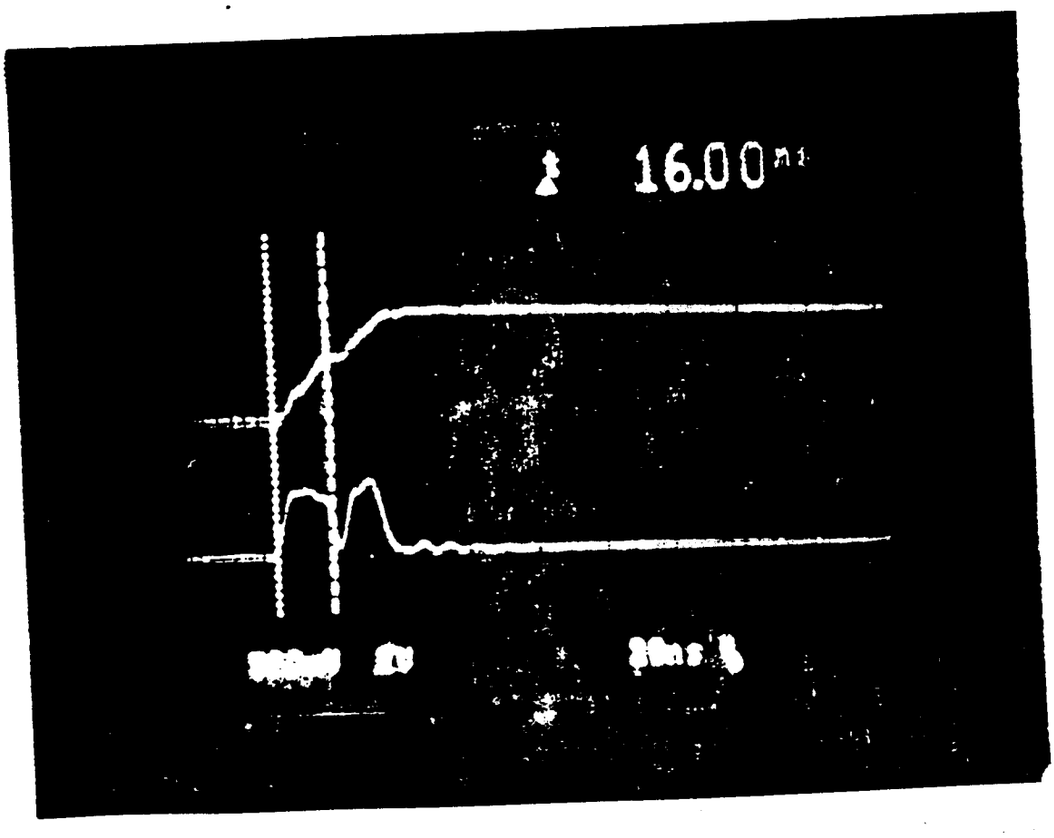


Percentage of Previous Crossing pulse in next crossing pulse

Time lag between peaks	16 ns delay line	20 ns delay line
16 NS	6.26%	18%
32 NS	0.1%	5.34%
50 NS	< 0.1%	< 0.1%


16.00ns
500mV 2V
20ns


16.00


16.00

Perspectives on Calorimeter Triggering

G. Sullivan

G. Sullivan
Chicago
6/7/91

CALORIMETER TRIGGERING

- Different Schemes
- Physics Processes
  Physics Objects (e, μ, jets, γ, ν)
- Simulation of Trigger
- Trigger ↔ Front End

Trigger Schemes

"Local" (Downstairs)

- Process data at front end crates.
  Send physics objects to global trigger.
  * Could use to reduce trigger bandwith
  * Muon and tracking subsystems must process data at front end.
  * Cost is less ??
  * L1 buffer length is smaller

"Central" (Upstairs)

- Send tower energies to central location for Processing.
  * allows access to electronics if "Upstairs"
  * Makes a "clean" break between Cal-Trigger
  * Debugging trigger system is easier
  * No interconnect problem on detector

Note: Upstairs / Downstairs depends on Calorimetry trigger!

Local trigger

- Physics objects (i.e. e, γ, jets) are sent from front-end crates.

- Reduced bandwith sent to global trigger.

  ex: electron bits

E_t	η	ϕ	iso	Shower max
8	4	1	1	?

  ~ 16 bits/electron + 11 bits (time stamp)

- Can be Synchronous (~ 6 fiber/crate) or Asynchronous (< 1 fiber/crate)

Central Trigger

- Digitize every beam crossing
- Transmit data over Fiber (LBL)
- Synchronous data to trigger

  1 Gbit/sec per trigger tower

  (~ 32 fibers/crate)

Benchmark Processes

① Electrons from inclusive W's

② Muons from inclusive W's

Goal: 50% eff for leptons in fiducial volume and not failing offline cuts.

③ High P_t jets

④ High P_t photons

Goal: 1-2 decade overlap with data from present colliders

⑤ Missing E_t

Goal: Measurable signal for new physics

⑥ Low P_t multileptons from B's

Goal: Competitive B physics

Level 1 Strawman Trigger Table

Trigger	Et min (GeV)	η coverage
electron	30	1.5 ?
photon	35	3
muon	15	1.1 (2.5?)
jet	200	3
2 elec	14	1.5?(3 e/γ)
2 muon	10	1.1 (2.5?)
e/μ	14/10	1.5/1.1
$\not{E}_t$	140	.5?
ΣE_t	1000	5?
ΣP_t	?	1.5
2μ + μ or e	5 (μ) ? (e)	
Minbias (pre-scaled)		
elec "	15	1.5
muon "	5-10	1.1 (2.5?)
jet "	100	3

Electrons

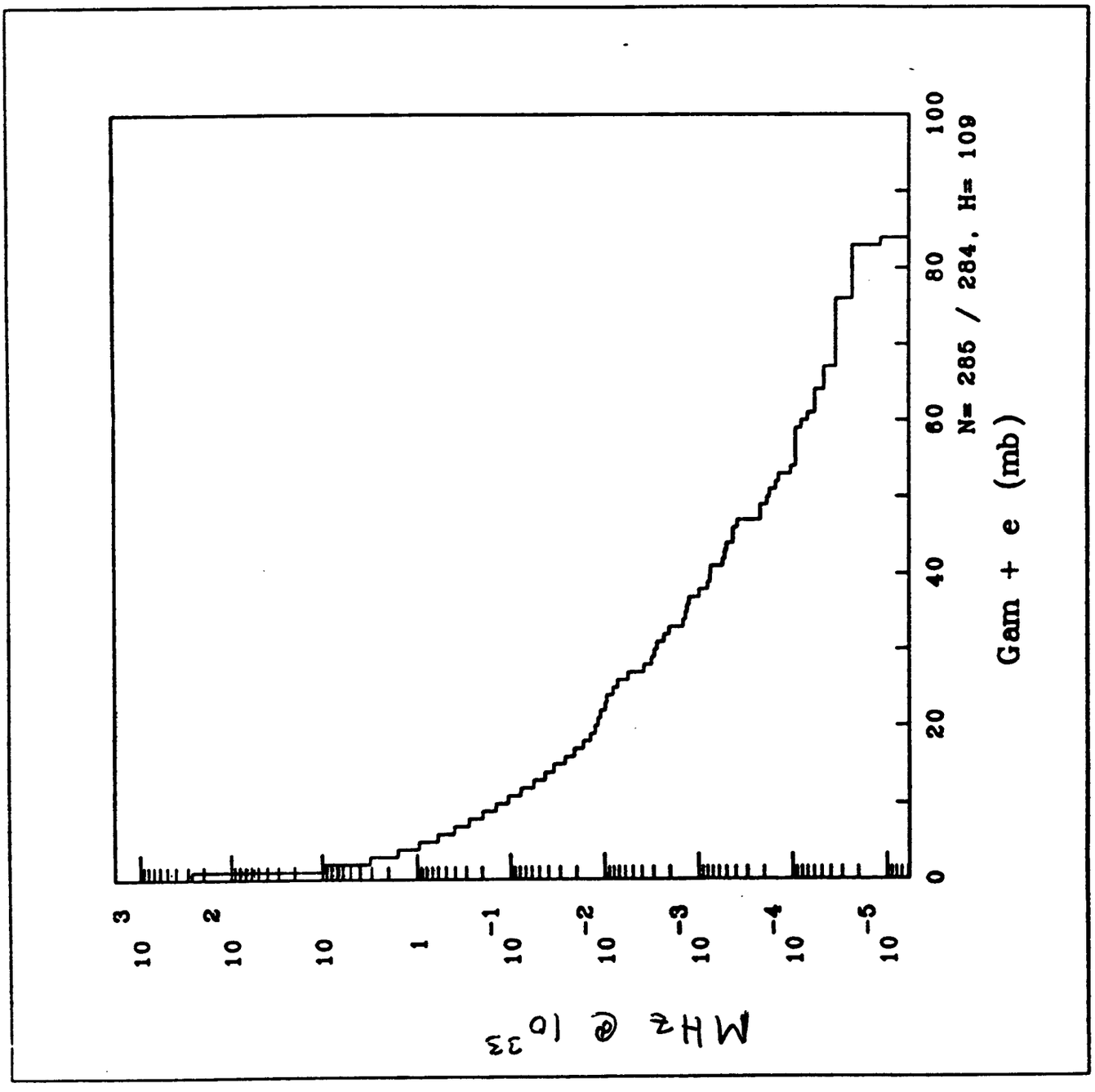
* E_t over threshold
  - what is trigger tower size?
  - need overlapping sums.?

* Had/Em Ratio
  - EM tower > E_t threshold
  - efficiency vs. rejection

* Isolation
  - use EM or Had Isolation?
  - which towers to include?
  - relax for second leg?

* Track pointing to trigger tower
  - How accurat does match have to be (.05 or .1)?
  - is it necessary (i.e. how much does it get you given material in tracking volu

* Track - Shower max position match
  - Do you want it in L1?


Gam + e (mb)
N= 285 / 284, H= 109
0
20
40
60
80
100
MHz @ 10^{33}
10^{3}
10^{2}
10^{1}
1
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}

Jets

* Sum trigger towers $E_t > E_t^{thresh}$

  (0.2×0.2) or

  $(0.4 \times 0.4) \Rightarrow$ overlap wedges!

* use $|\eta| < 3$ only or use forward?

$\sum E_t$, $\not{E}_t$

* Do we need $\not{E}_t$ at L1?
  - what can give you LARGE $\not{E}_t$ with no leptons or jets above L1 thresholds?

  - CDF doesn't use $\not{E}_t$ at L1

Chicago Simulation

Goal: Study calorimeter related triggers → make design decisions

Prob: Electron trigger requires tracking, shower max, and calorimeter info.

Full simulation → too slow

⇒ Write simulation w/ parametrization wherever possible (everywhere at first).

Try to learn where full simulation is necessary.

Use CDF parameters in sim and compare w/ known CDF rates.

! ⇒ Eventually get all parametrizations in SHELL.

Use full sim where needed

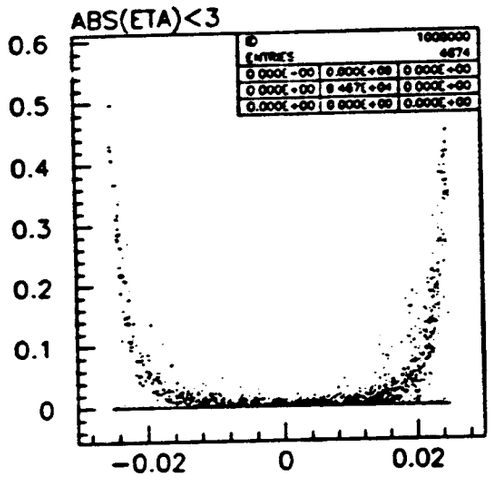
False tracks + tails of dists (E.

Use parametrizations for speed

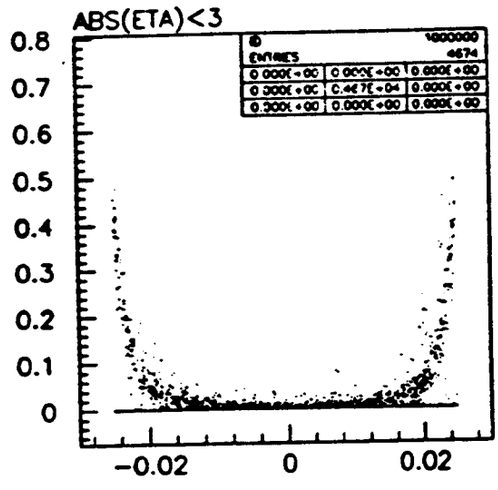
Description of Simulation

- Generate data sets w/ Isajet
  minbias, 2 jet, W, Z, ...
- Use shaping function for energy deposition
- Keep time history of energy in towers
  poisson dist of minbias at every crossi
- Smear vertex
- π, K decays in flight
- conversions
  material inside tracking lumped in one layer.
- Track eff = 1.0, resolution from EOI
- Calorimeter longitudinal, lateral smearing $|\eta| < 3.0$. $|\eta| > 3.0 \rightarrow E = E^{ge}$
- Shower max in bins

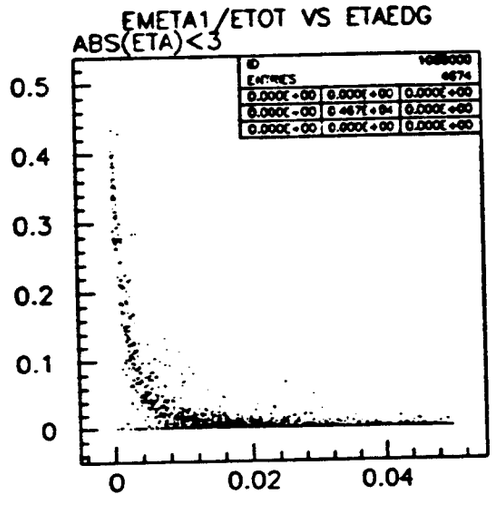
29/05/91 11.17



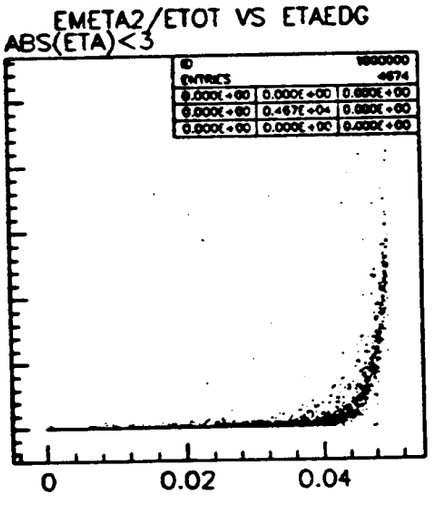
EMETA1/ETOT VS ETAEDG



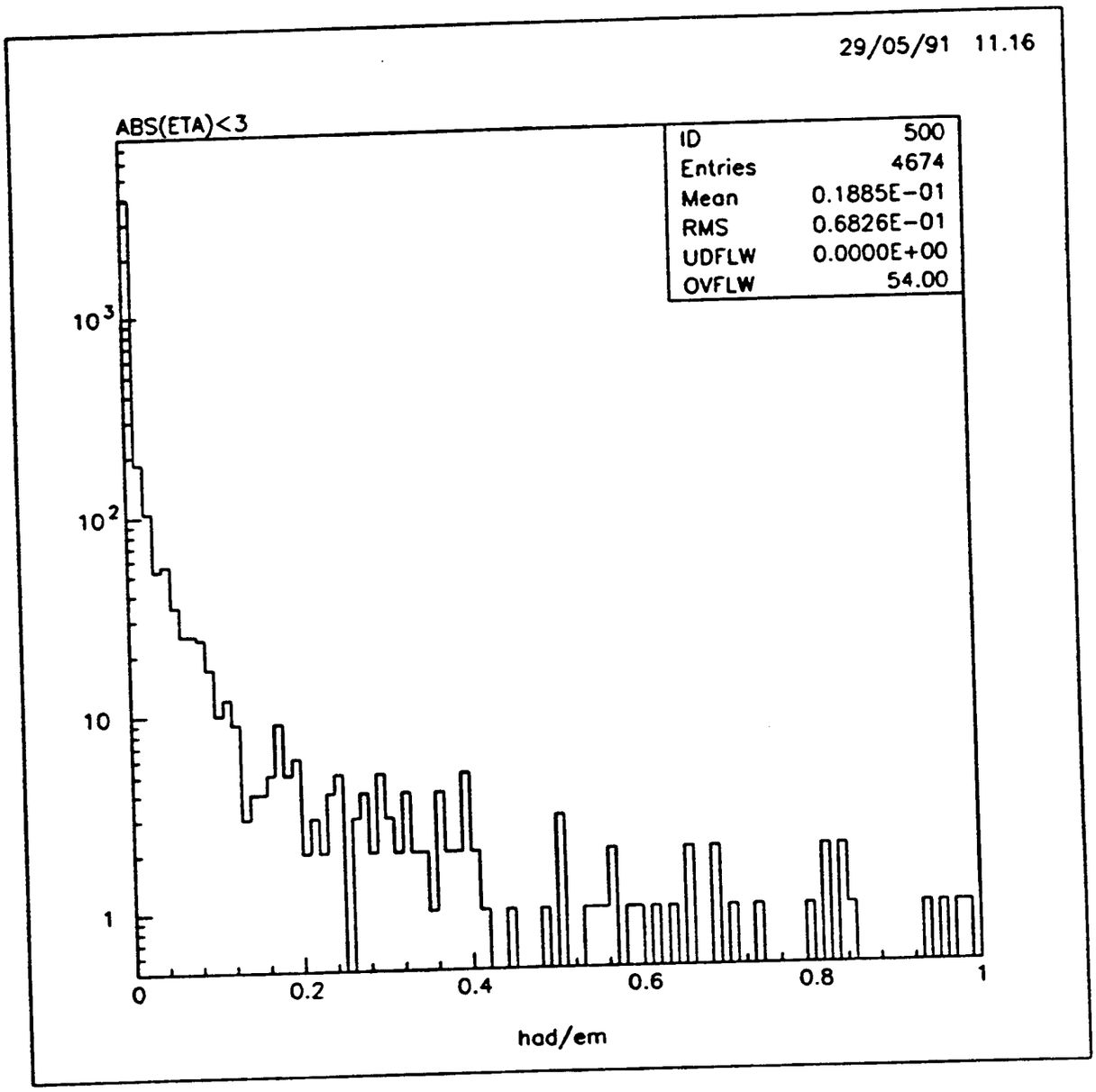
EMETA2/ETOT VS ETAEDG

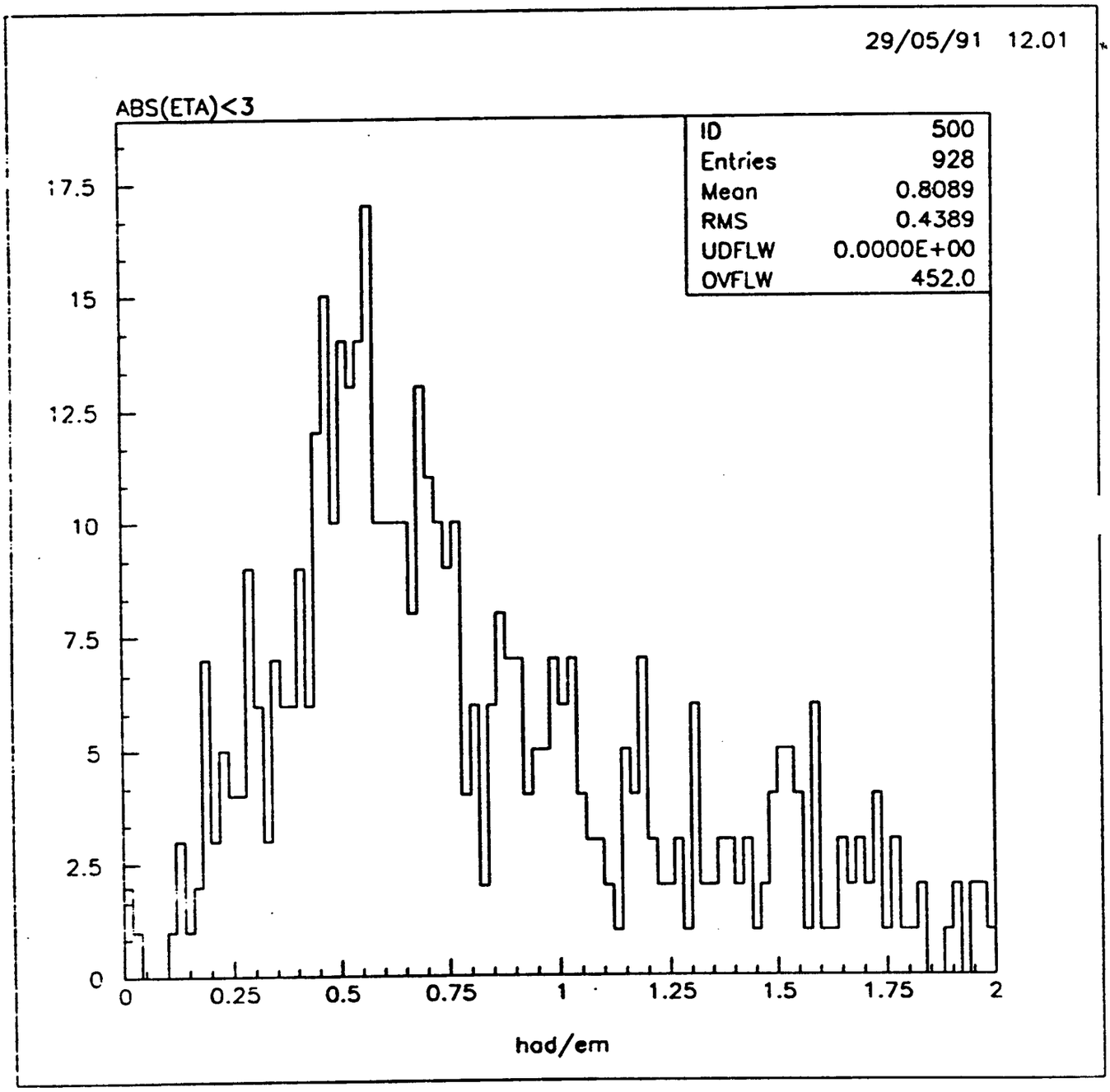


EMPHI1/ETOT VS PHIEDG



EMPHI2/ETOT VS PHIEDG


29/05/91 11.16
ABS(ETA)<3
ID 500
Entries 4674
Mean 0.1885E-01
RMS 0.6826E-01
UDFLW 0.0000E+00
OVFLW 54.00
10^3
10^2
10
1
0
0.2
0.4
0.6
0.8
1
had/em


29/05/91 12.01
ABS(ETA)<3
ID 500
Entries 928
Mean 0.8089
RMS 0.4389
UDFLW 0.0000E+00
OVFLW 452.0
17.5
15
12.5
10
7.5
5
2.5
0
0
0.25
0.5
0.75
1
1.25
1.5
1.75
2
had/em

Problems to Study

Tracking -

- Necessary For L1 ?
- How accurate should matching be ?
- Conversions (i.e. material)

Isolation -

- Which towers are included ?
- Need adjacent wedge info ?
- Both Had and EM info ?

Effect of front end shaping function -

Trigger towers -

- Overlap for EM cluster ?
- Jet size ?

Clearly many others

What do We Know?

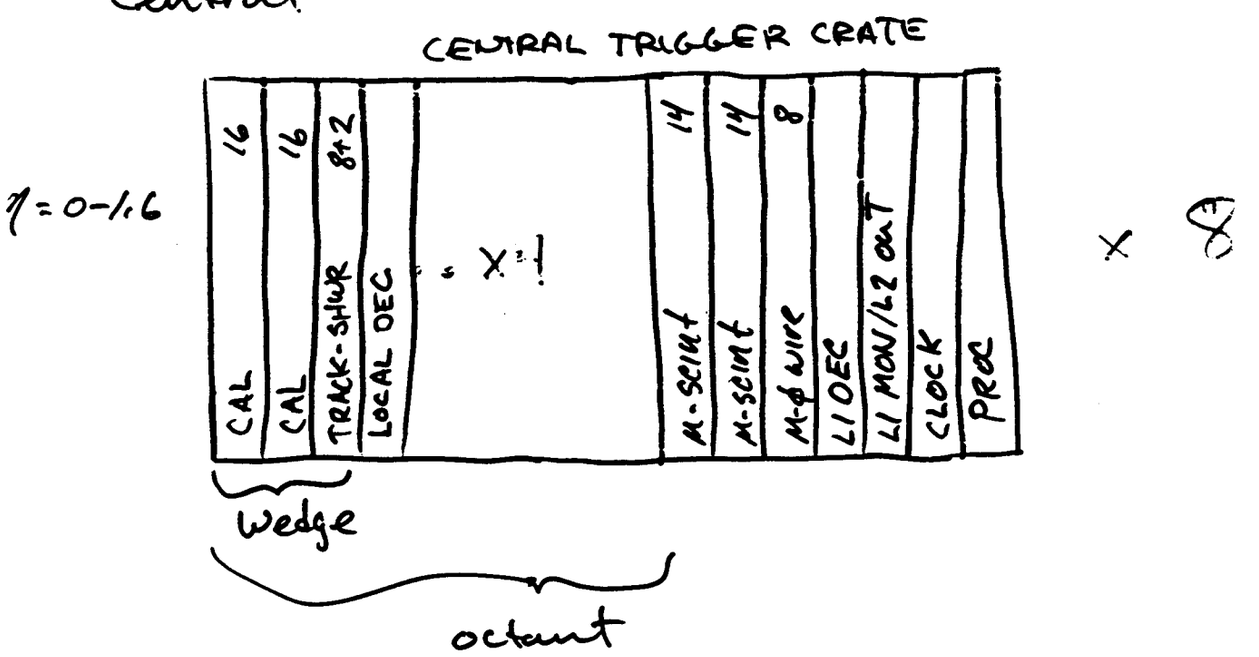
- trigger on electrons, muons, jets, photons, ν
- electrons use: Had/EM
  Isolation
  track match
  E_t
- TRIGGER energies are digital

What we don't know

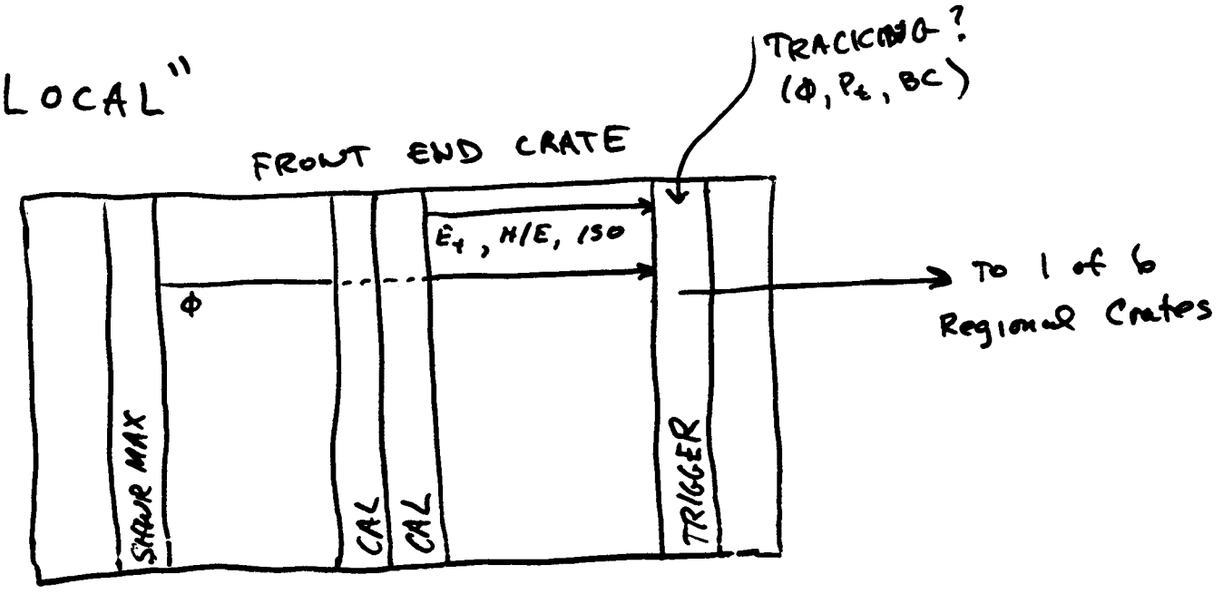
- what the front end electronics are!
- what the forward Calorimeter is.
- what the trigger tower size is.
  (descoping!)
- how finely do we need to match tracks to calorimeter. (tower vs shwr max)
- do we need overlapping tower sums for trigger.
- Can all subsystems live with "upstairs" trigger
  (i.e. 4ms buffer)
-
-

Front end - Trigger interface

"Central"

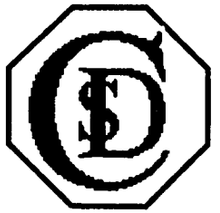


"LOCAL"



Level 2 Triggering

D. Hubbard

The  Level 2 Trigger

A global view of the level 2 trigger
Summary of the Saclay group investigation

P. Bonamy , J.C. Brisson, J. Ernwein , R. Hubbard
O. Gachelin, P. Le Dû , B. Thooris.

Version 0.9

May 91

Edited by P. Le Dû

Presented by Dick Hubband

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Is it necessary ? *What are the main features ?*

■ Redundancy with the level 1:

Quik decision (10 to 50 µsec) to refine the Level 1 selection
use a ---> *a* **finer granularity**
---> *a* **more flexible algorithms** *and thresholds.*

- *check level 1 hardware efficiency ....*
- *solve pile-up events & timing overlaps*

If you remove the signal at Level 1, Level 2 doesn't help !

■ Correlate information between detectors in a global mode.

---> *Tracking + Calorimetry*

■ Add detectors information not availabable at the level 1.

---> *Pixel : better Pt , forward tracking , secondary vertex ?*
---> *Muon : better eta-phi, isolation*
---> *Track : better Pt, z information*
---> *Calorimetry :better E resolution , add ShowerMax ---> isolated Electron / Gamma*

More information ⇒ better cuts for same bandwidth

■ Full energy measurement and topological correlations

----> *Missing Et ... , event topology flag (b,t ?,W, Z , H ? etc.)*

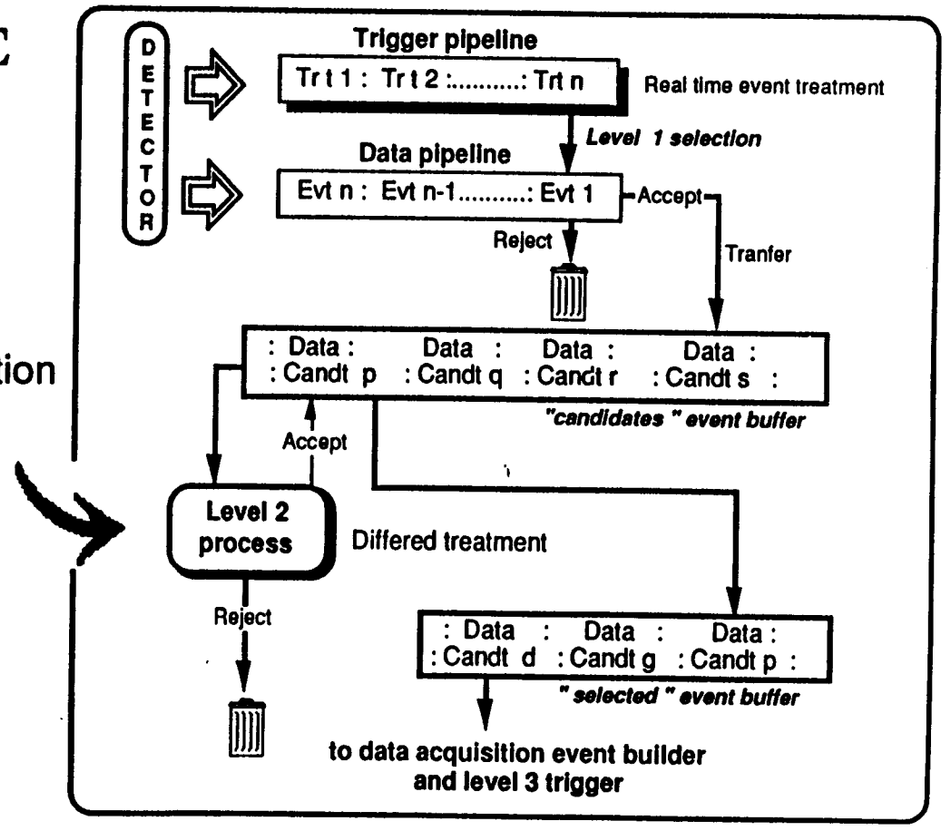
Keep less-isolated electrons at lower E_T.

Architecture

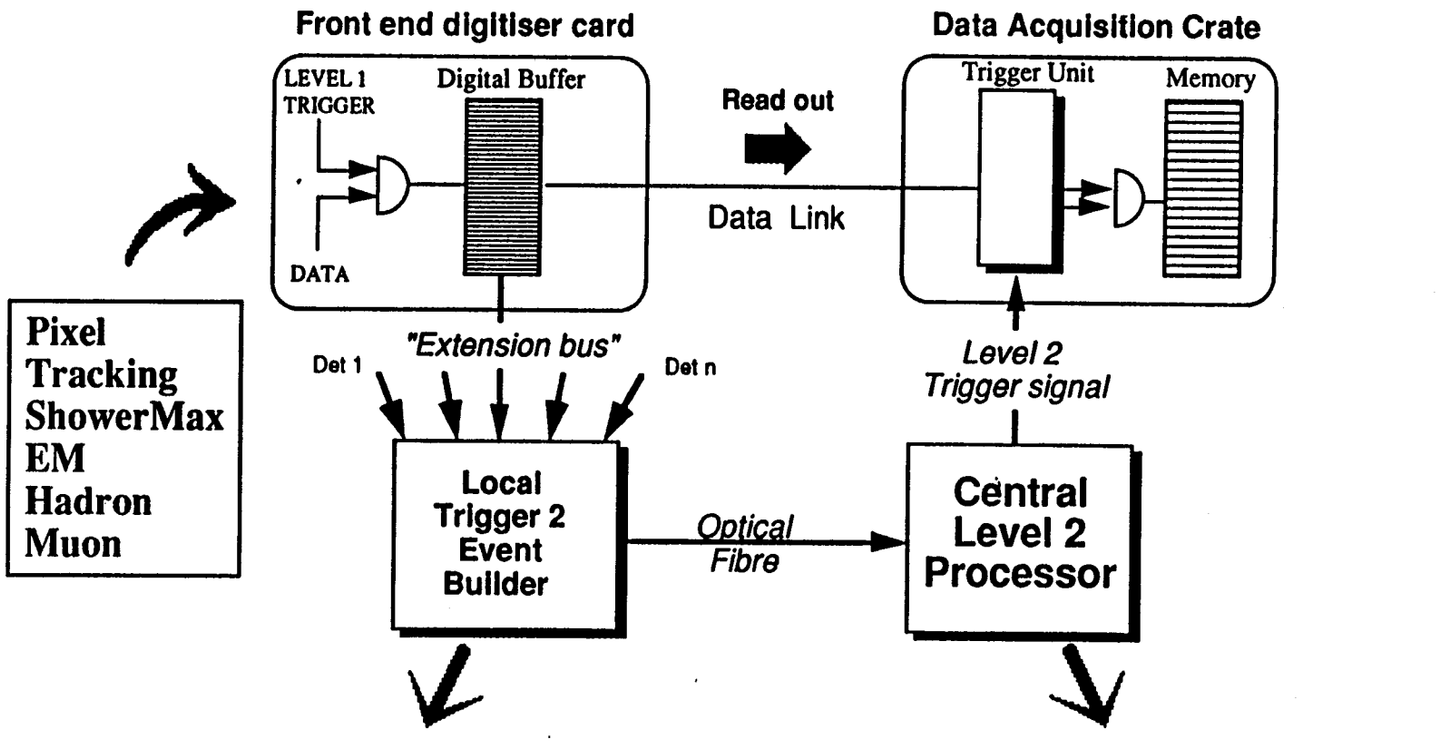
➡ **Full PIPELINE**

The level 2 interacts with

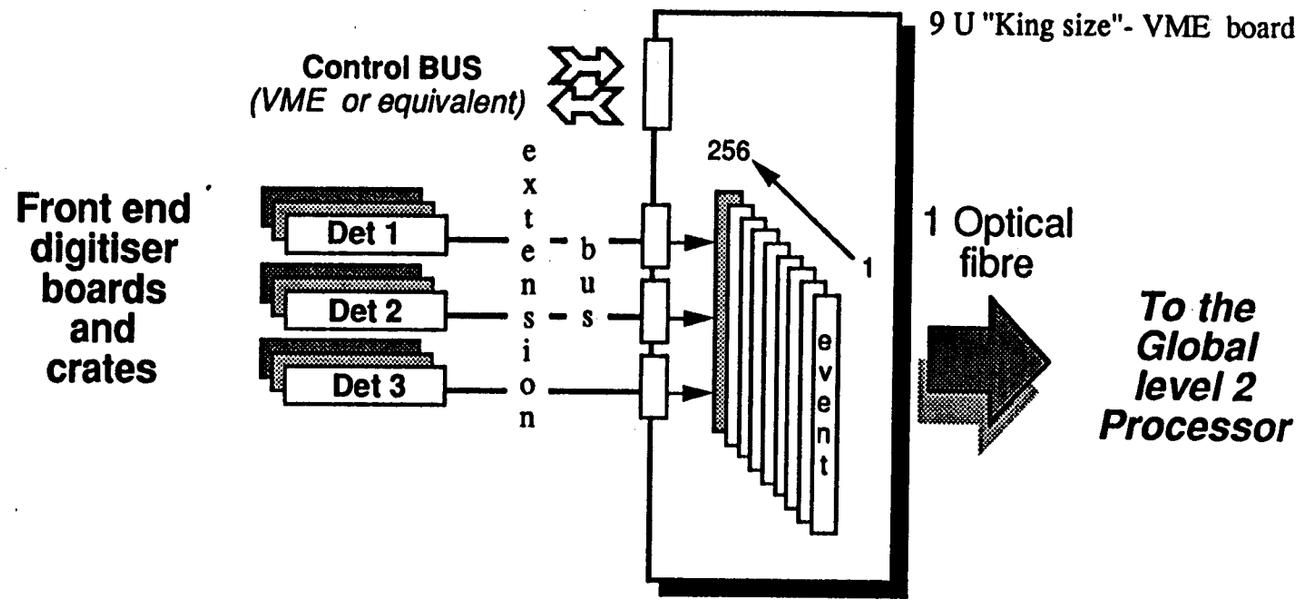
- The front end electronics
- Level 1 trigger synchronisation
- Data Acquisition



Integration & Synchronisation

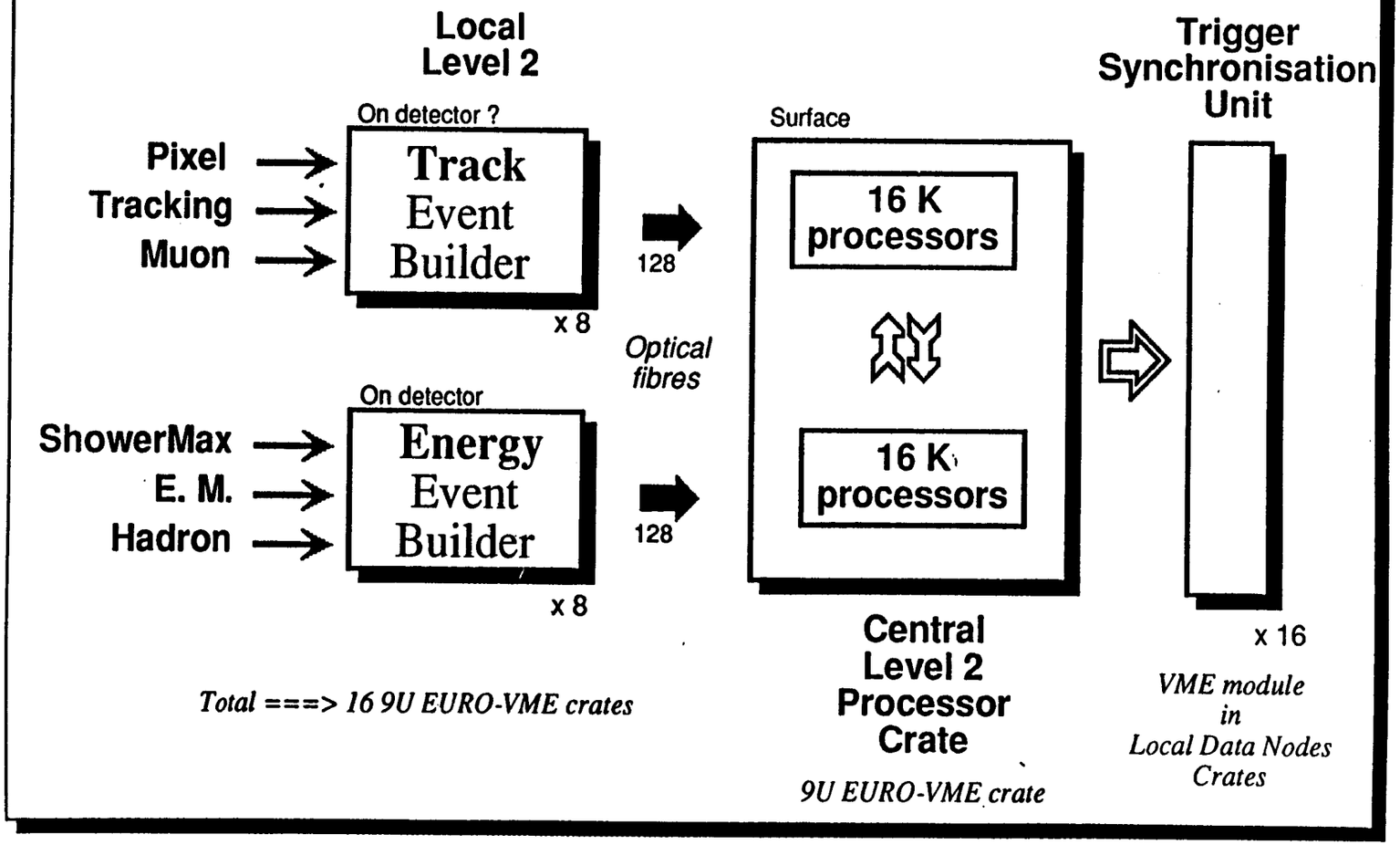


Local Event Builder Board

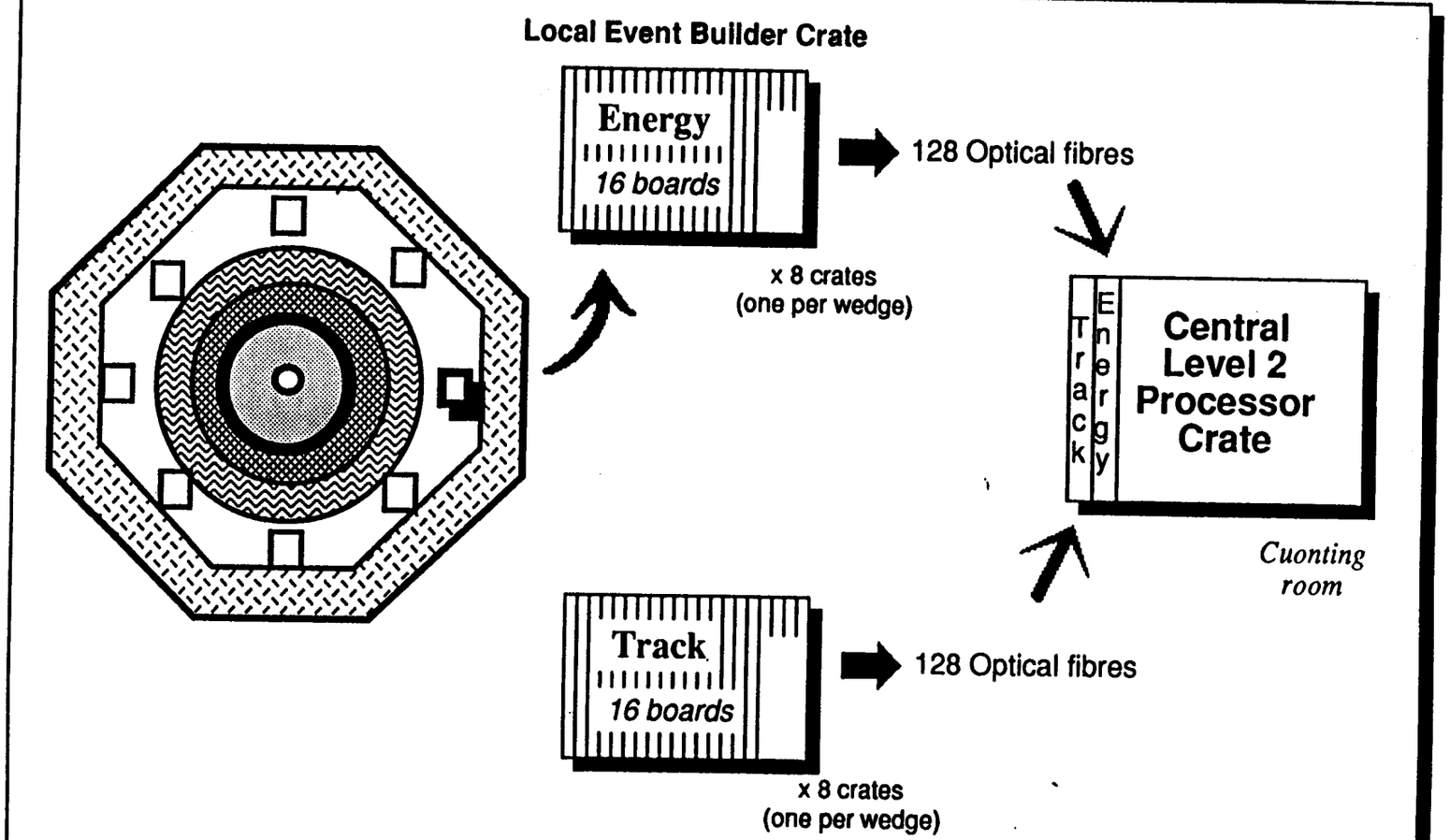


Component		Nb	FF	$	Total (FF)	Total ($)
PC board	6 layers type ?	1	1400	233.3	1400	233
Connectors	VME type	4	60	10	240	40
Static RAM	50 ns - 16 bit x 1024	4	100	16.67	400	67
Control logic	VME + clock ...	1	1000	166.7	1000	167
Cabling & test		1	1500	250	1500	250
Cost per board					4540	757

Level 2 Trigger Layout



Topology



SDC level 2 trigger - DSM Saclay

ASP : Associative String Processor

A short introduction ...

➢ *Basic idea*

- **Suppress memory access**
  ---> *one processor for each data word*
- **Suppress addressing mode**
  ----> *Content addressable memory*
  ----> *associative access to multiple data*

➢ *Basic component* : **APE --> Associative Processor Element**

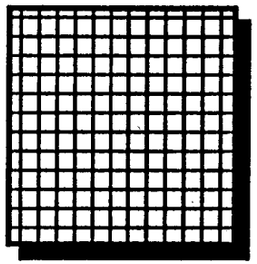
Today ---> ASPEX VASP64

- Clock frequency 20 MHz
- 64 bit data register
- Time slot 30 ns
- 2µm rule technology
- Hybrid with 1024 processors (Polycon-Phoenix)
- 8182 processors per 9U MAXI VME board
- 5 $ per APE
- Power consumption : 100 Watts for 8 K processors

Tomorrow ---> ASPEX + HUGHES
---> *ASP mprovment*

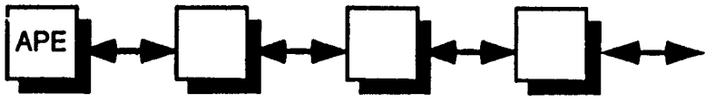
- Clock frequency ≥ 40 MHz
- ≥ 64 bit data register possible (128 ?)
- Vector Data Buffer
- Time slot ≤ 25 ns
- 1 µm rule technology
- SOS : rad hard Silicon On Saphire
- 1 dollar per element ?

ASP Communication & Software



Array of
128 x 128 APE

Linear --> String



- **Communication by shift**
- **Communication by propagation**
- **Network may be segmented by 8,16, 32, 64 (BKL)**

Instructions

- 25 ns per instruction at 20 MHz
  (add, search,clear,write,read,shift,change ..)

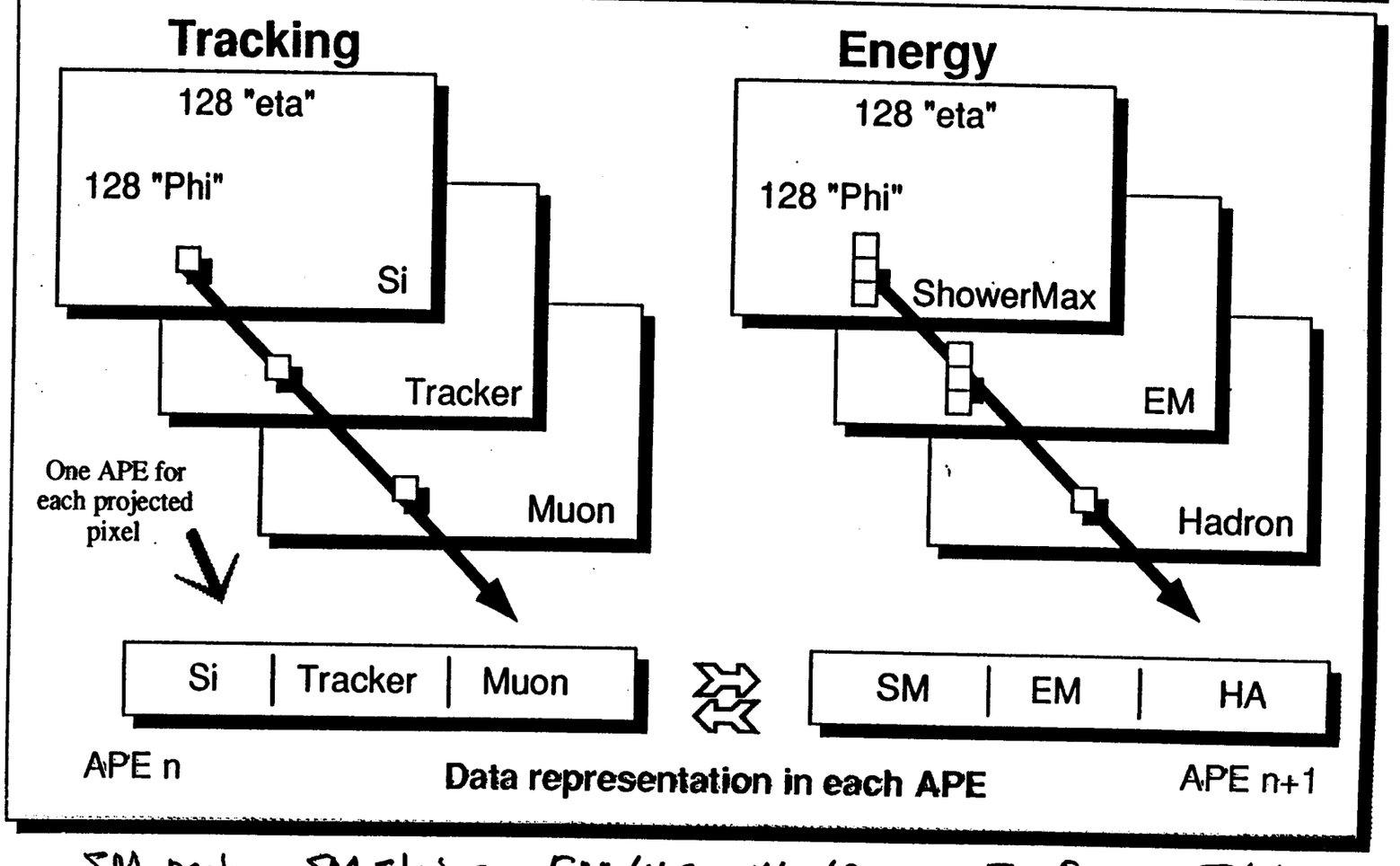
Tools
Software Development System

- ASP simulation & timing analysis
- Application compiler , linker and loader
- Debugger

Performances

- 12 bit addition = 100 GOPS
- In-out bandwidth ~ 2.5 Gbytes /sec
- Power consumption ~ 100 watts

Global Level 2 Processor Principle



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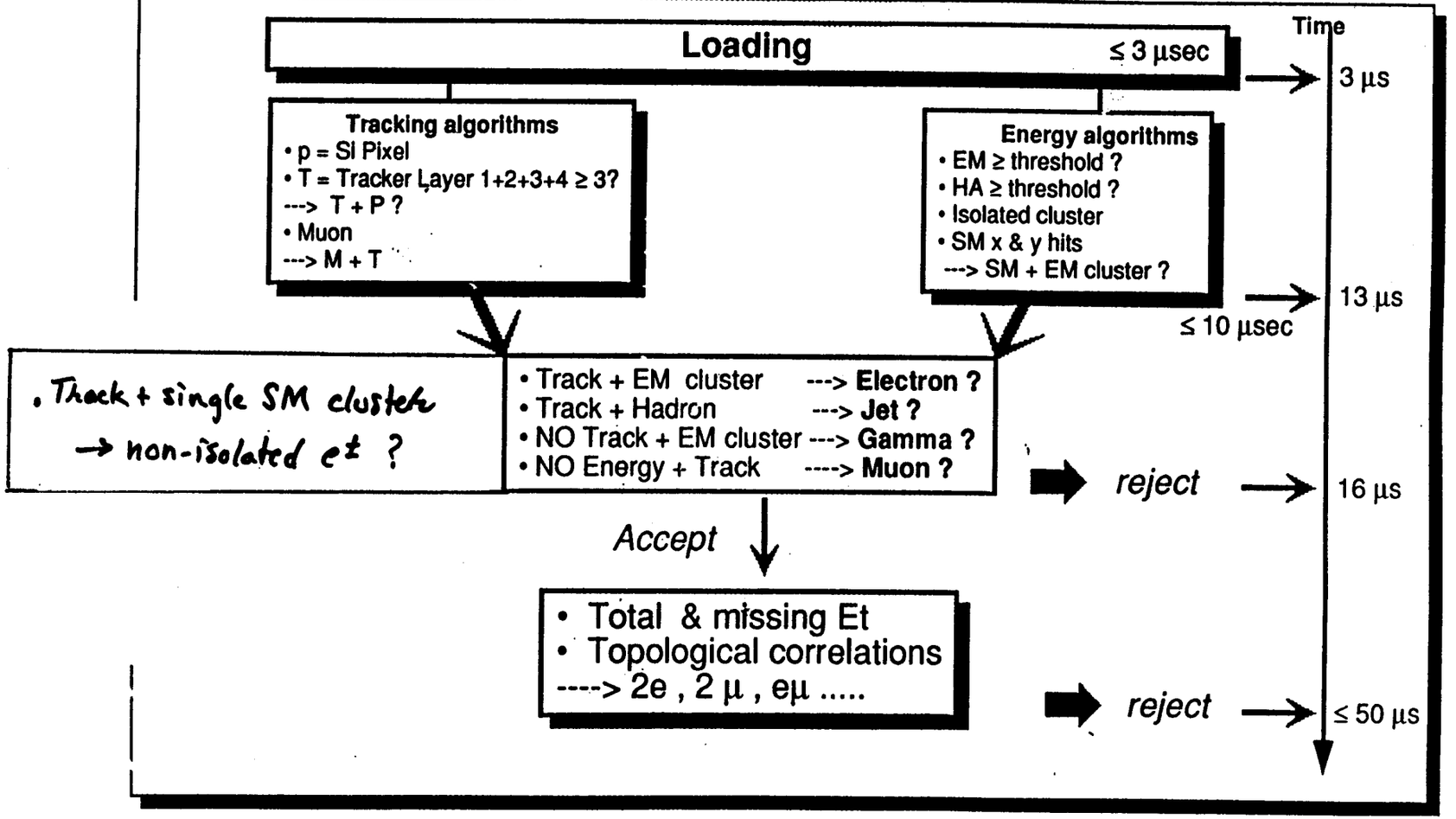
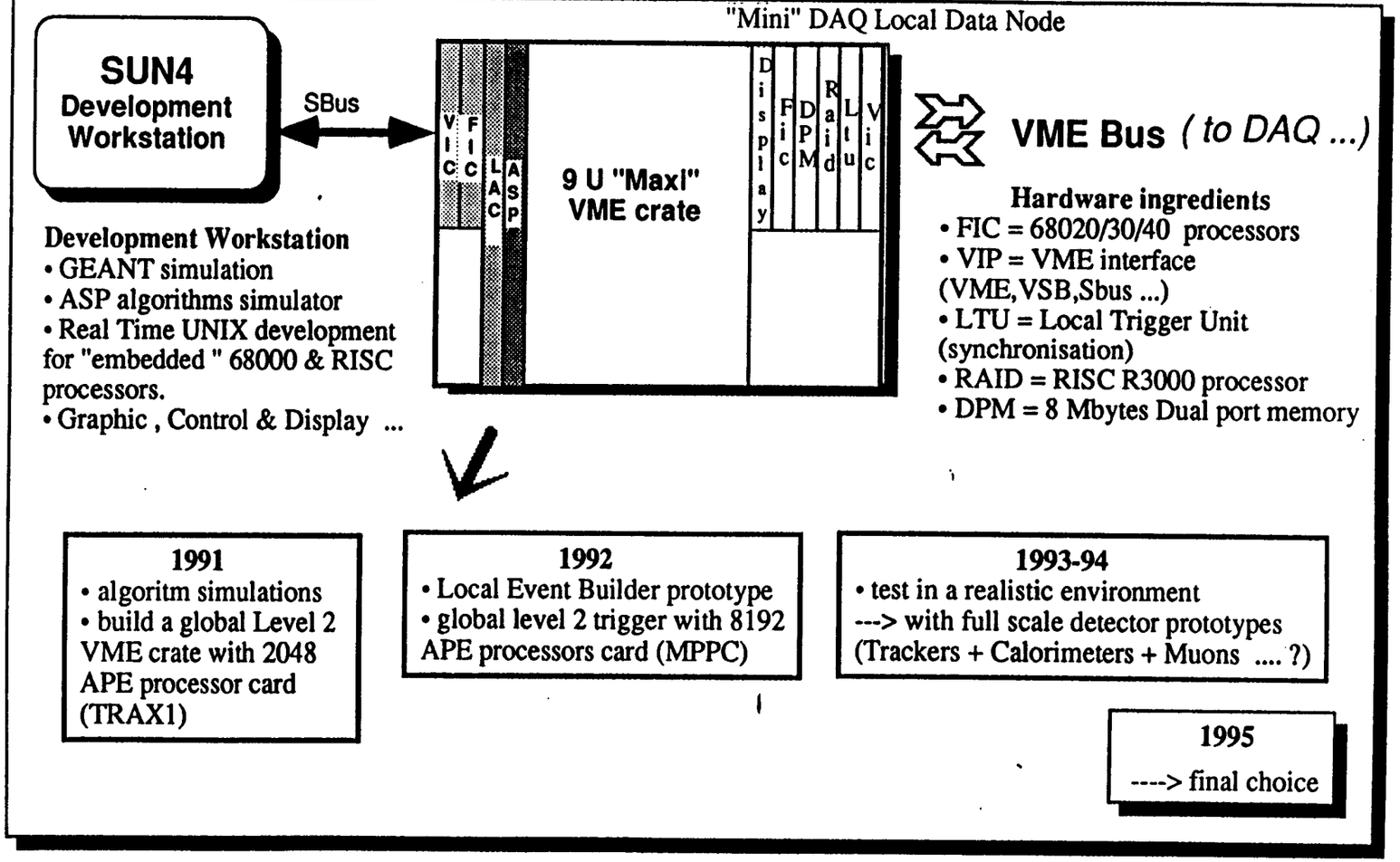
SM peak SM strips EM/HA Up/Down $\sin\theta$ Total

Algorithms flow chart



Saclay Prototype & Test



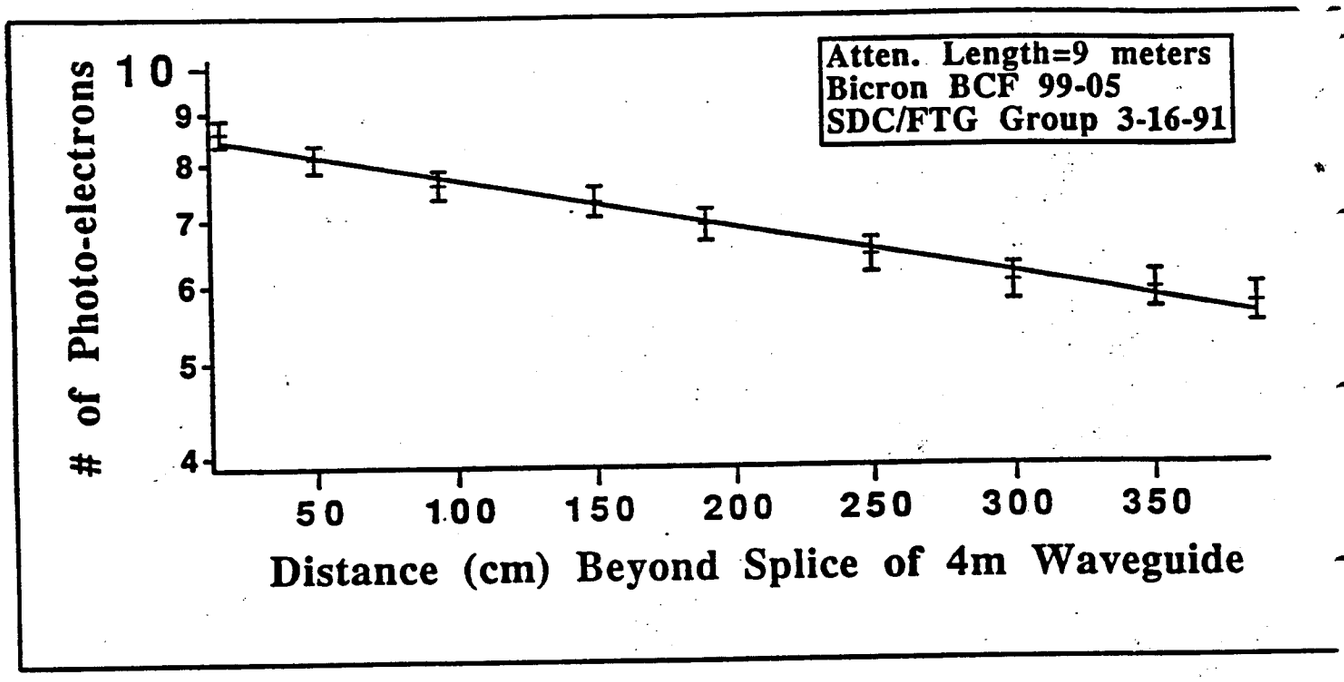
Summary & Cost

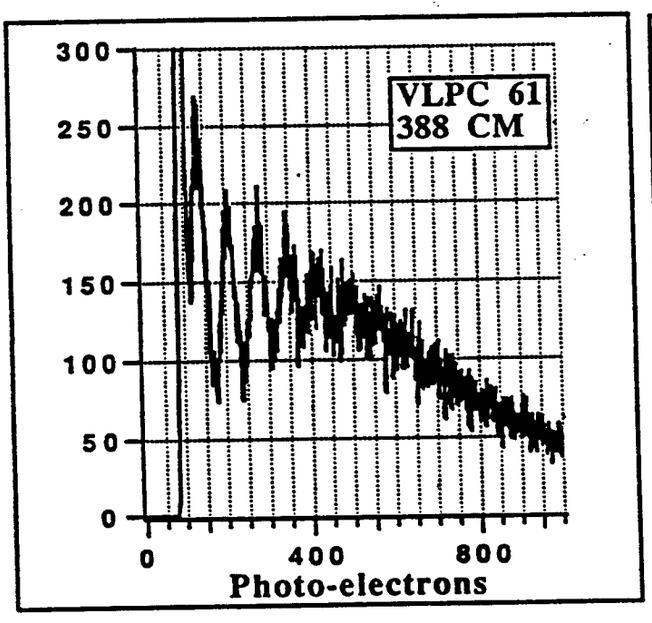
Components	Description or type	Number	cost/ unit KFF	cost/ unit K$	Total MFF	Total M$
Local Event Builder						
Board		256	4.5	0.75	1.152	0.192
Crate	9U Euro-VME	16	18	3.00	0.288	0.048
Processor (Control)	FIC	16	18	3.00	0.288	0.048
Synchro & trigger	LTU	16	8	1.33	0.128	0.021
Crate interconnection	VIC	16	15	2.50	0.240	0.040
Global						
Crate	VME 9 U	2	25	4.17	0.050	0.008
Control card	LAC type	2	50	8.33	0.100	0.017
ASP processor card	8 K APE	6	250	41.67	1.500	0.250
VME Processors	FIC	2	30	5.00	0.060	0.010
Crate interconnection	VIC	4	15	2.50	0.060	0.010
Cables	optical fibres...	1	500	83.33	0.500	0.083
Workstation & Periph.	SUN4..	2	500	83.33	1.000	0.167
DAQ Synchro Unit	LTU	16	8	1.33	0.128	0.021
TOTAL					5.494	0.916
add 10% (protos,spares)					6.043	1.007

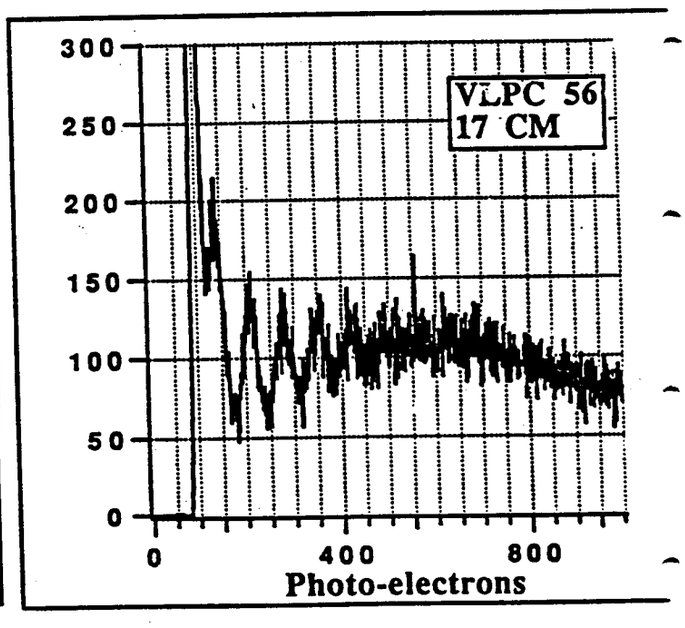
Scintillating Fiber Readout

A. Baumbaugh

A. BAUMBAUGH.





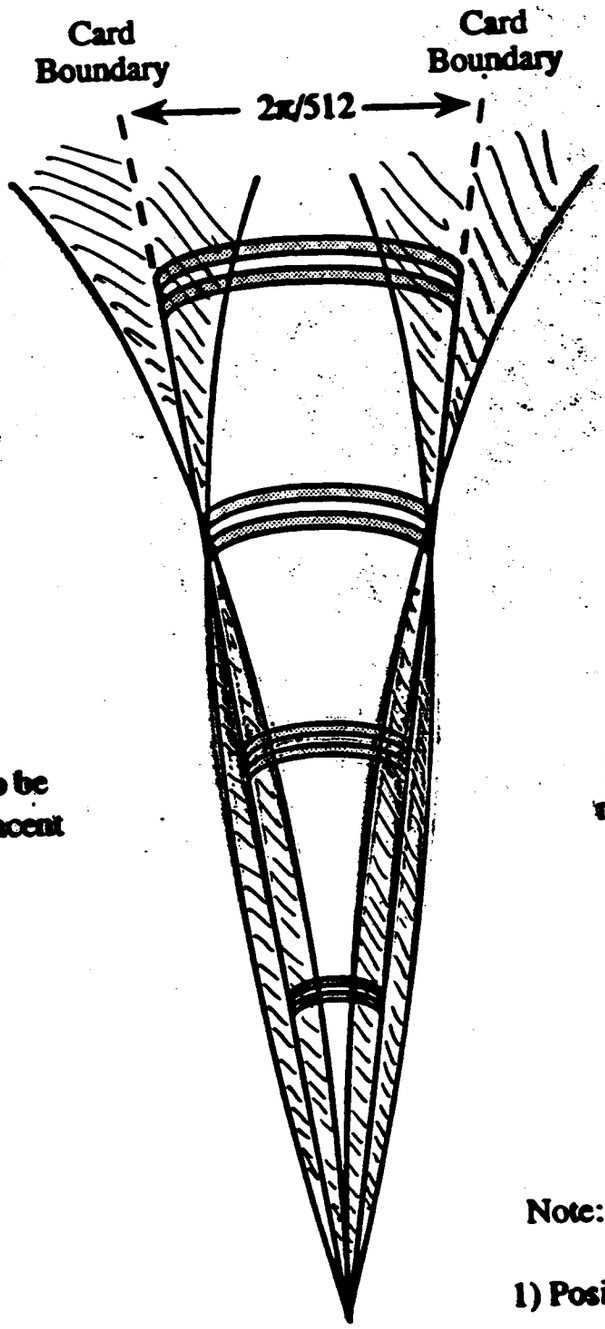


Photon-Statistics From a Full Length SDC Scintillating Fiber Tracking Tes

Key Assumptions

- **Minimum Pt for trigger purposes is 10 Gev**
- **System has full 1 / 512 symmetry**
  (Card to card boundaries are the same as crate to crate)
- **Fiber diameters are adjusted to maintain this symmetry in each layer**
  AND SPACING.
- **Fiber counts in each layer have a convenient least common factor (64)**
- **System redundancy is an important issue**
- **Full digital pipeline running at 62.456762 MHz**
- **One thousand events / sec are read off the detector**
- **Simulated data can be downloaded to test the system**

Boundary Fiber Sharing



Red area needs to be transmitted to adjacent cards

Blue area needs to be received by trackfinder ASIC for this slice

Note: What gets sent is track segment bits
1) Position (1 fiber width bins)
2) Dip (+, 0, -)
In some areas only selected Dip angles need be exchanged

Sci- Fi Tracker - Digital Trigger Card and Crate Connections

- **Digital Inputs**

  15360 Signals from fiber cryostat / crate
  562 Signals from neighboring crates
  40 Signals Clock and Trigger distribution
  64 Signals Pt Code Exchange

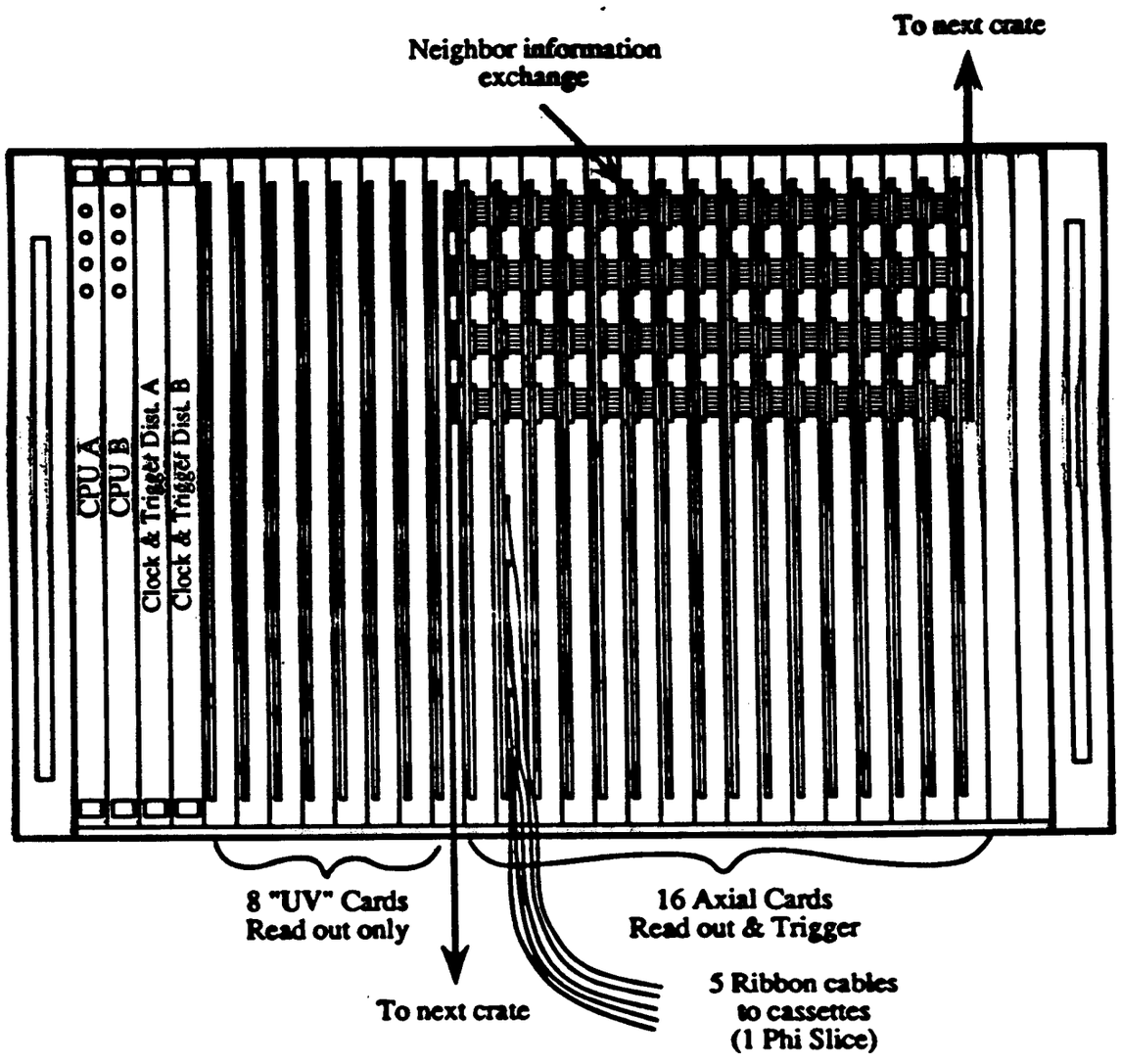
- **Digital Outputs**

  4 x 4 bit Pt Code to calorimetery crate
  (One per tower of calorimeter in phi)
  4 x 4 bits Pt Code to muon crate
  562 Signals from neighboring crates
  2 Ethernet cables

SDC Fiber Tracking Crate

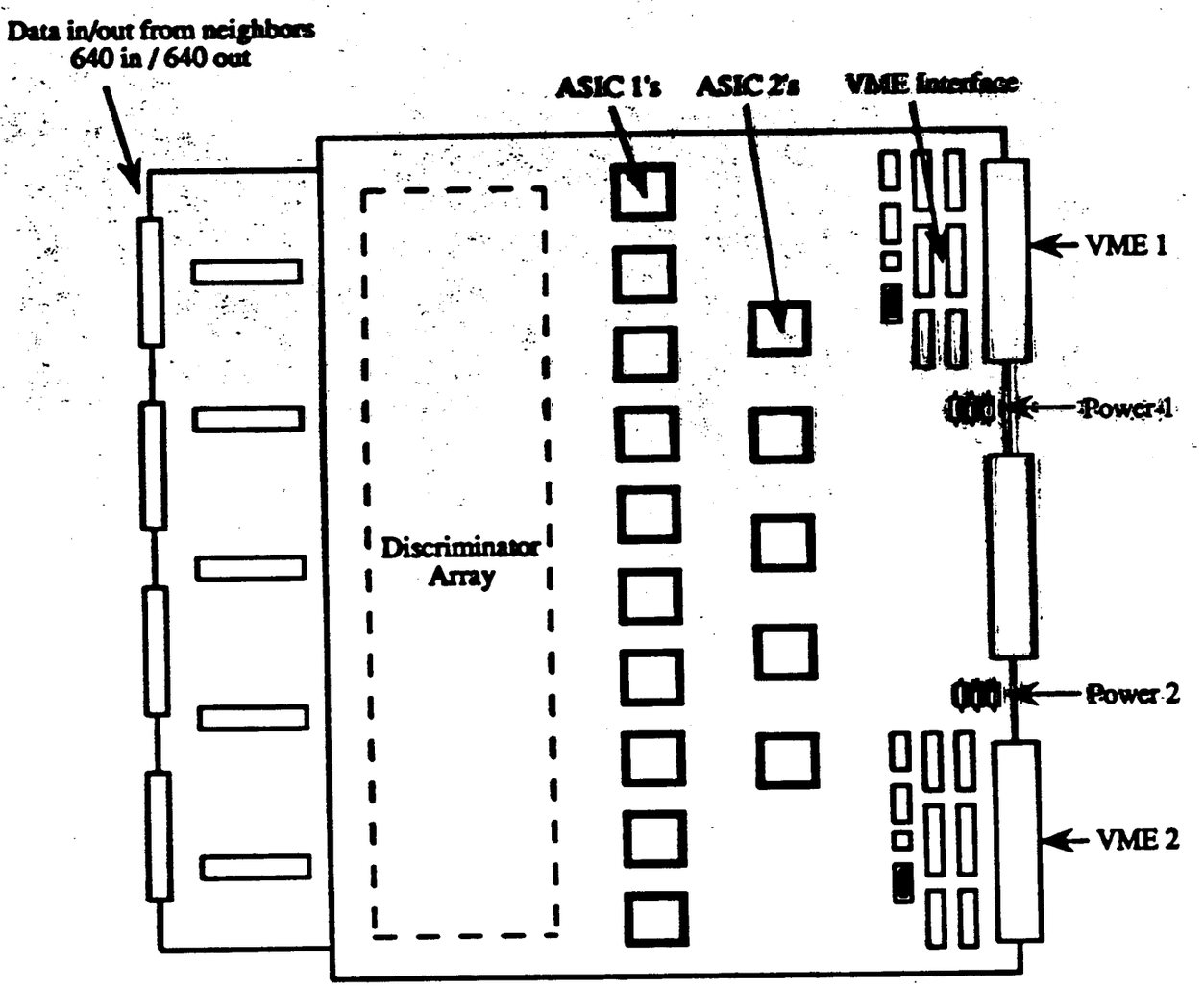
24 Tracking/Readout Cards

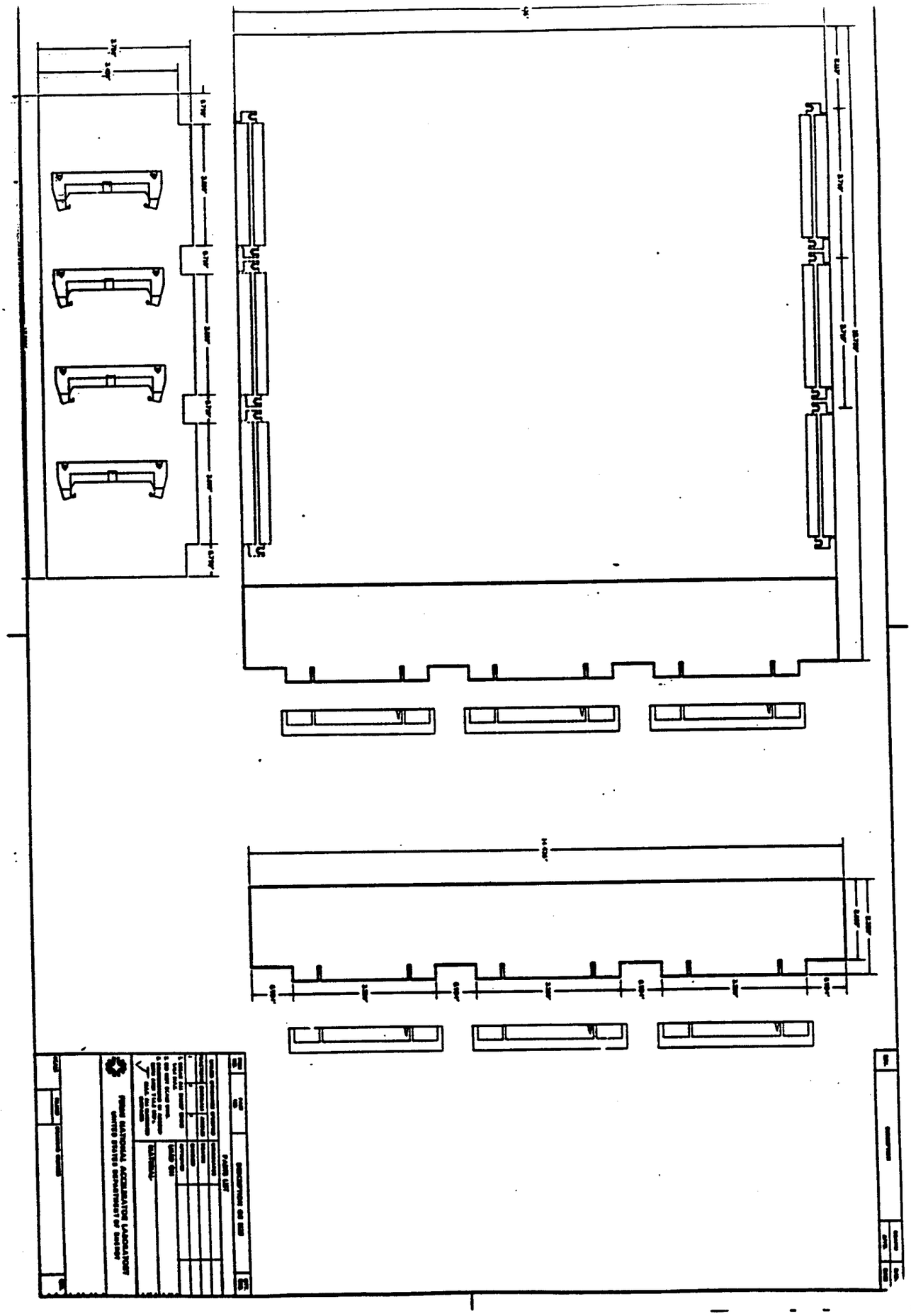
30 Slots @ 1 inch



SDC Fiber Tracker
Reciever Board

9 U x 400mm (14.437" x 15.750") Printed Circuit Board





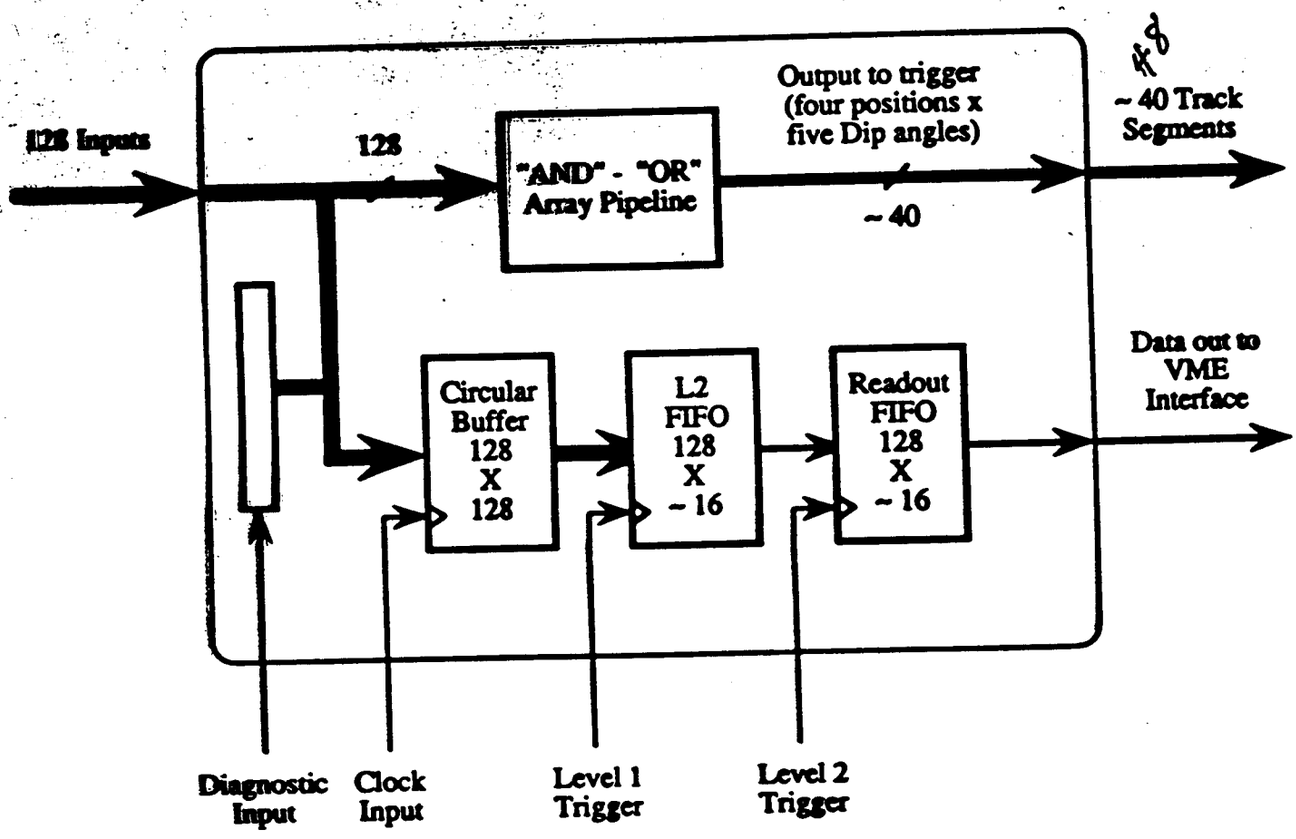
SDC
Tracking/Trigger ASIC 1

(7.0K Required)

Stores all "Hit" information locally while trigger is formed

Provides serial readout of selected events

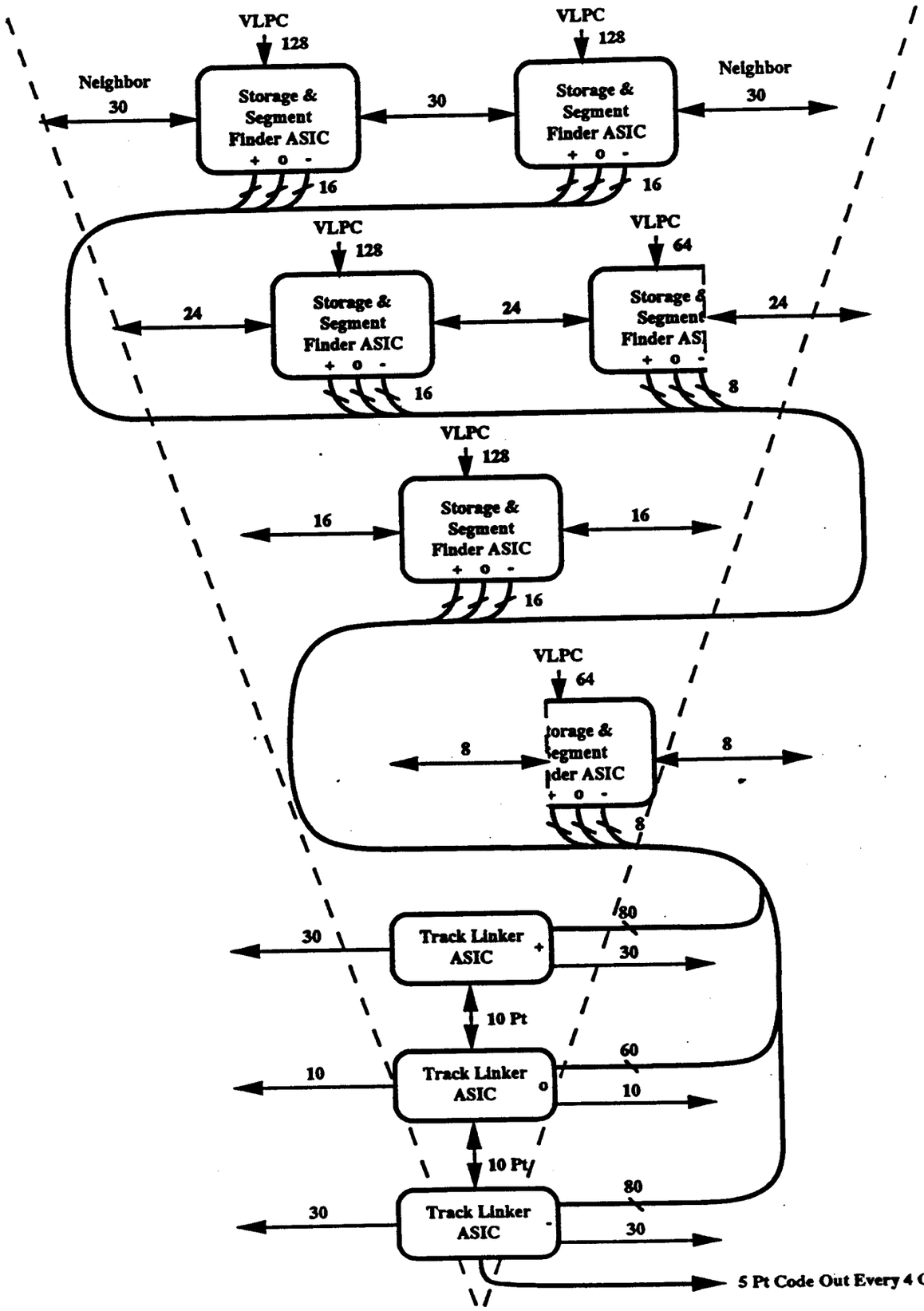
Provides "Track Segments" for trigger



(ASIC 2 is similar for segment linking, 3.5K required)

Level 1 Track Finder

(1 Card ~ 640 Inputs)



Data Acquisition System

Desirable Features:

1) Uniformity as much as possible

2) Commercial hardware as much as possible

3) Need a coherent picture of system:

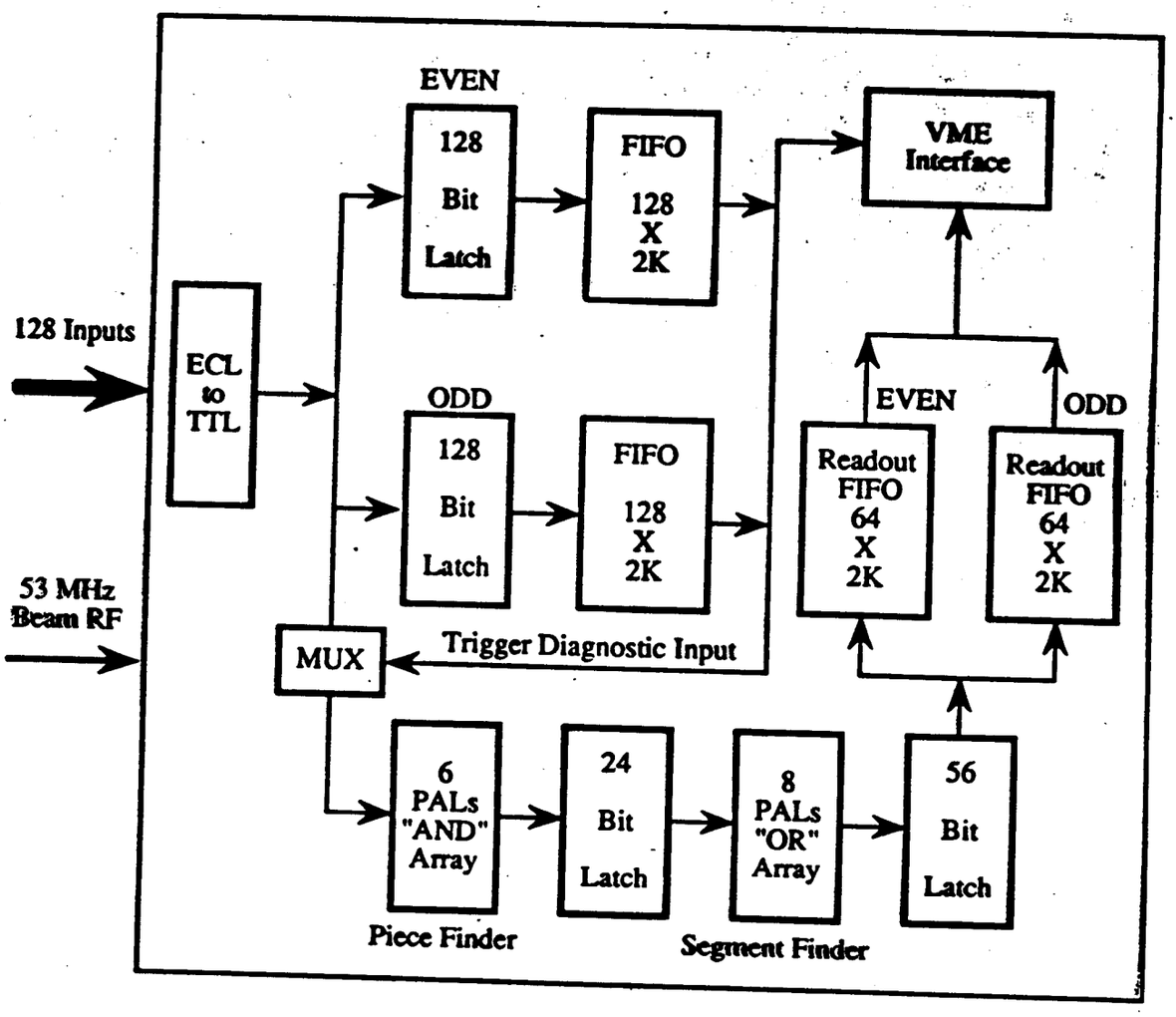
Event sizes
Event rates L1, L2

SDC ASIC 1
Simulation Board

Stores all "Hit" information locally while trigger is formed

Provides readout of events and tracks found

Board size is 9U X 400mm (14.570" X 15.750")



Scintillating Fiber Tracking Test Beam Goals

- 128 to 1024 Channels of VLPC
- 128 to 1024 Channels of Amp / Discriminator
- 128 to 1024 Channels of Pipeline Storage and Track Segment Finder running at 53 Mhz
- Store inputs and Segments found at 53 Mhz for off line comparison

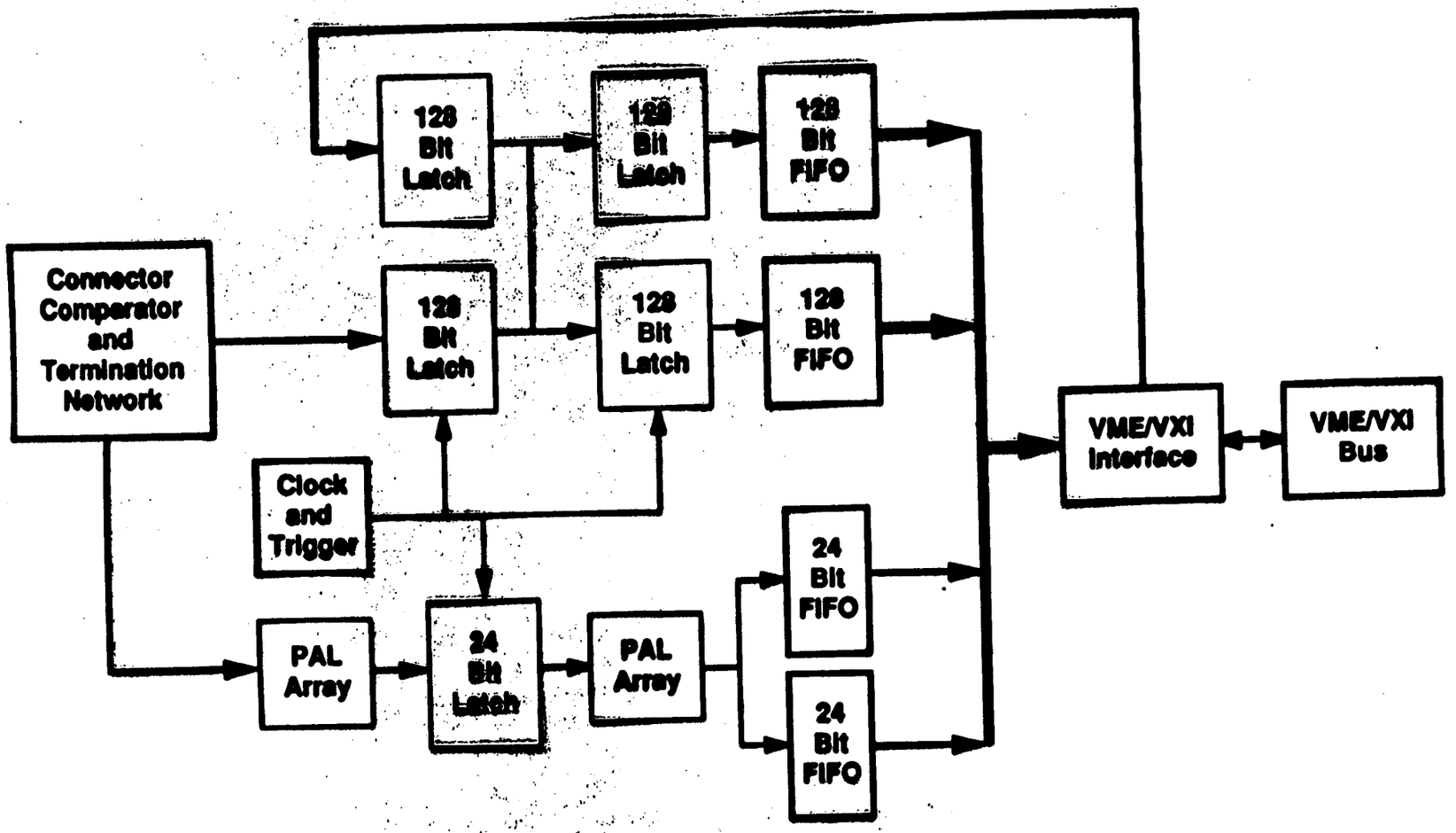
Tracking Storage and Segment Finder Board

- 128 Inputs
- Pipeline FIFO's for storage (4K RF Buckets)
- Pipeline "AND - OR" array for segment finding
- FIFO's to store results of segment finder
- All pipeline operation at 53 Mhz
- VME Interface for readout and diagnostics
- 1024 channels requires 8 boards
- Adder tree requires 3 boards
- Internal / External clocking for test operations

SDC Test Beam Effort

Tracking & Buffer Card

(Baumbaugh)

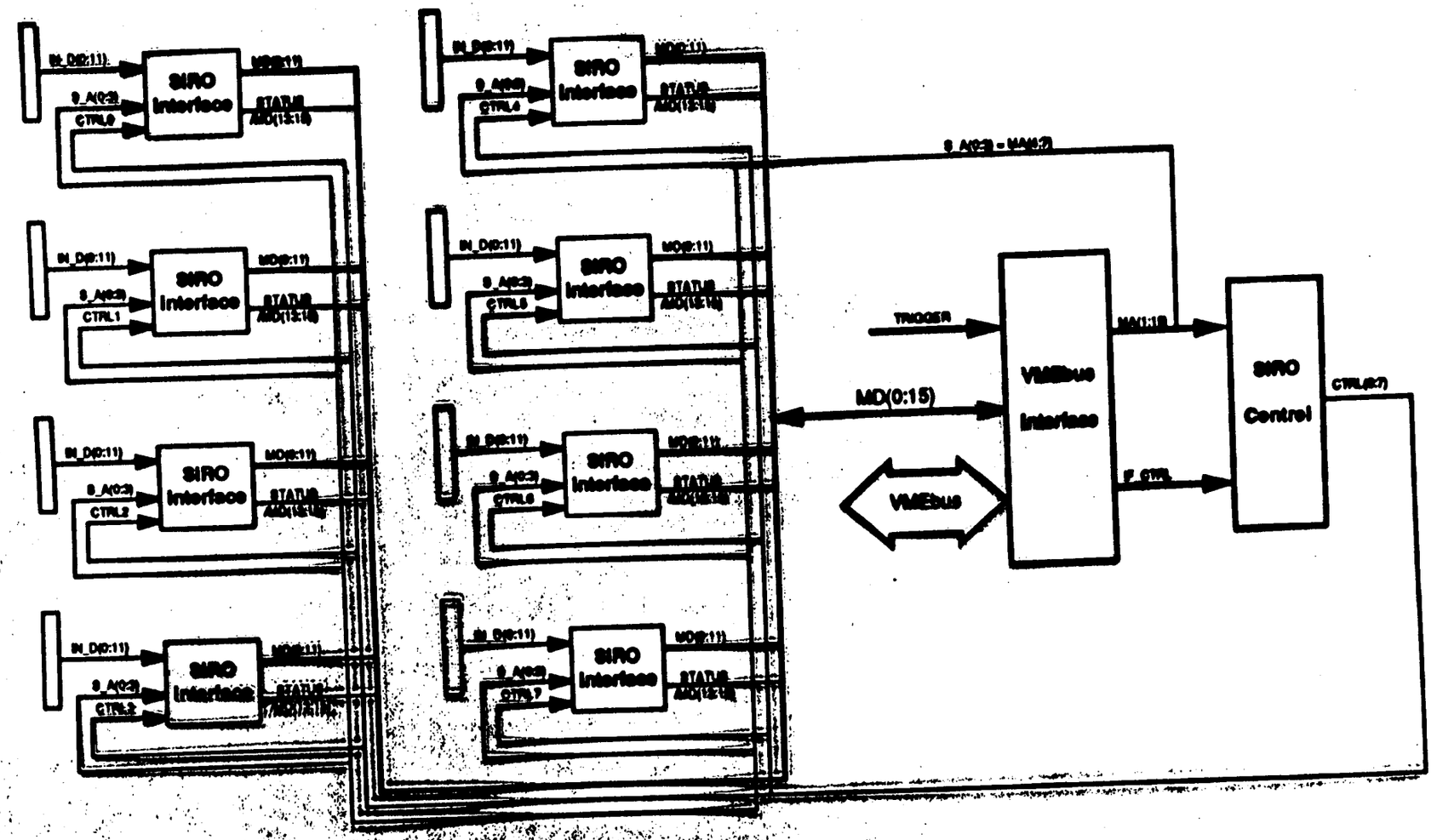


[redacted]

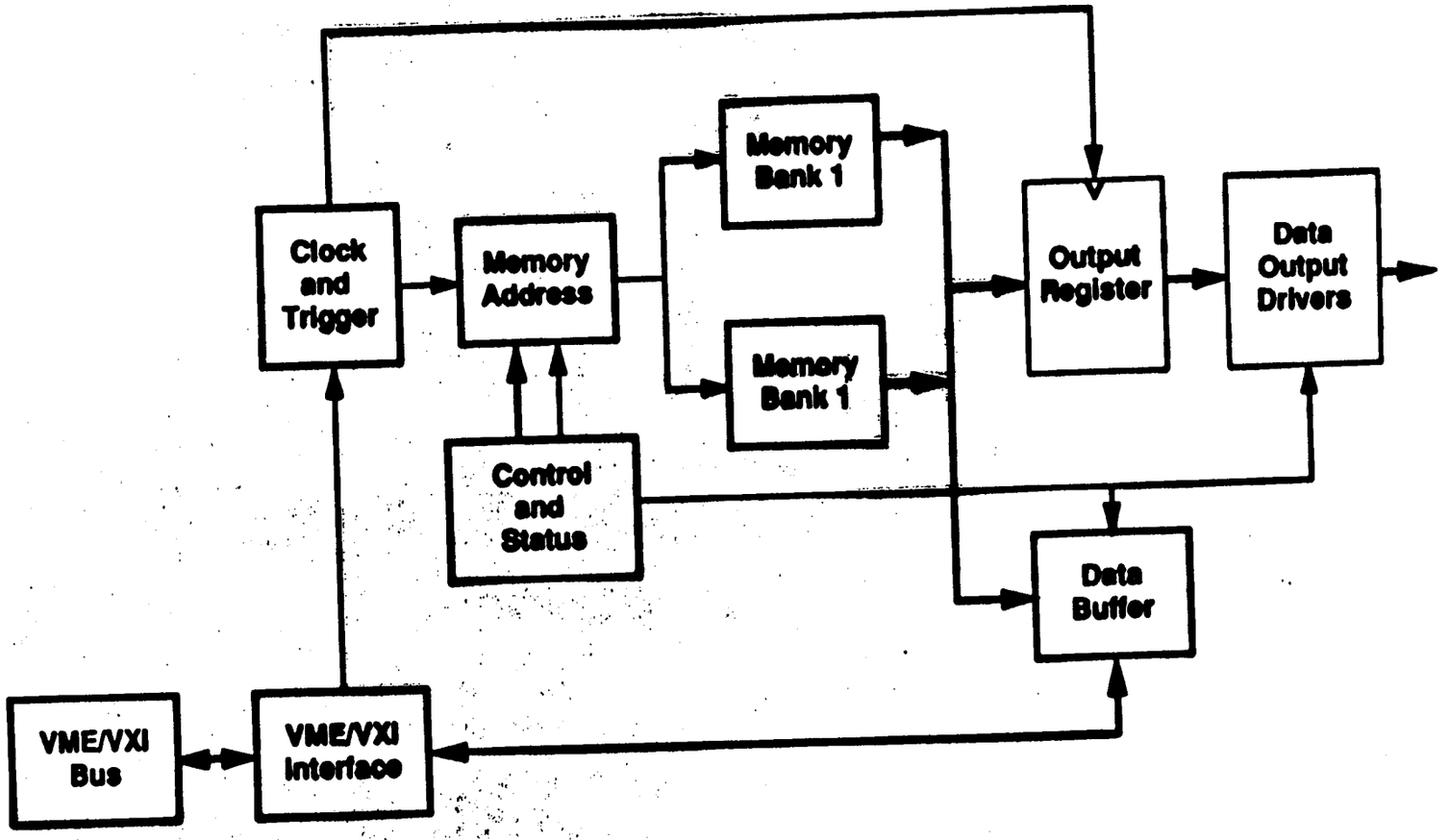
SDC Test Beam Effort

SIRO Card

(Trevizo)



SDC Test Beam Effort
Test Transmitter
(Urish)



Photodetectors for Shower Max Detectors

E Beuville
D. Hubbard ~~(Saclay)~~

CEA Saclay
Microelectronics

1- The ShowerMax Electronics for SDC

Front-end read out scheme

Front-end Amplifier - Noise considerations

Analog Pipeline

2- Rad-Hard Technology: S.O.I.

Results on PJFET

CMOS, JFET and Bipolar

The ShowerMax Electronics

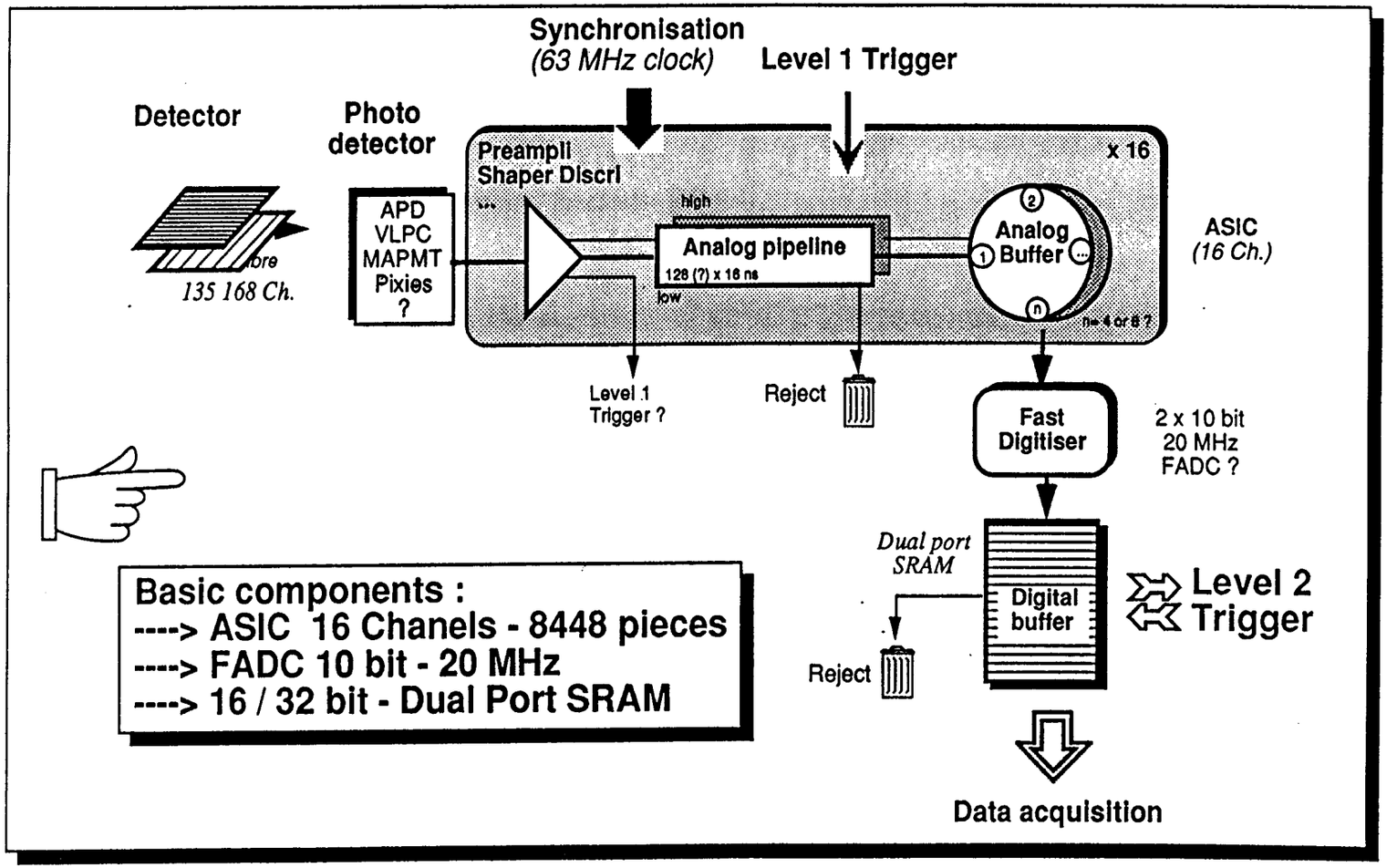
Summary of the Saclay group investigations

P. Bonamy, E.Beuville , JC Brisson , J. Ernwein,
R. Hubbard, J. Lugiez , P. Le Dû,

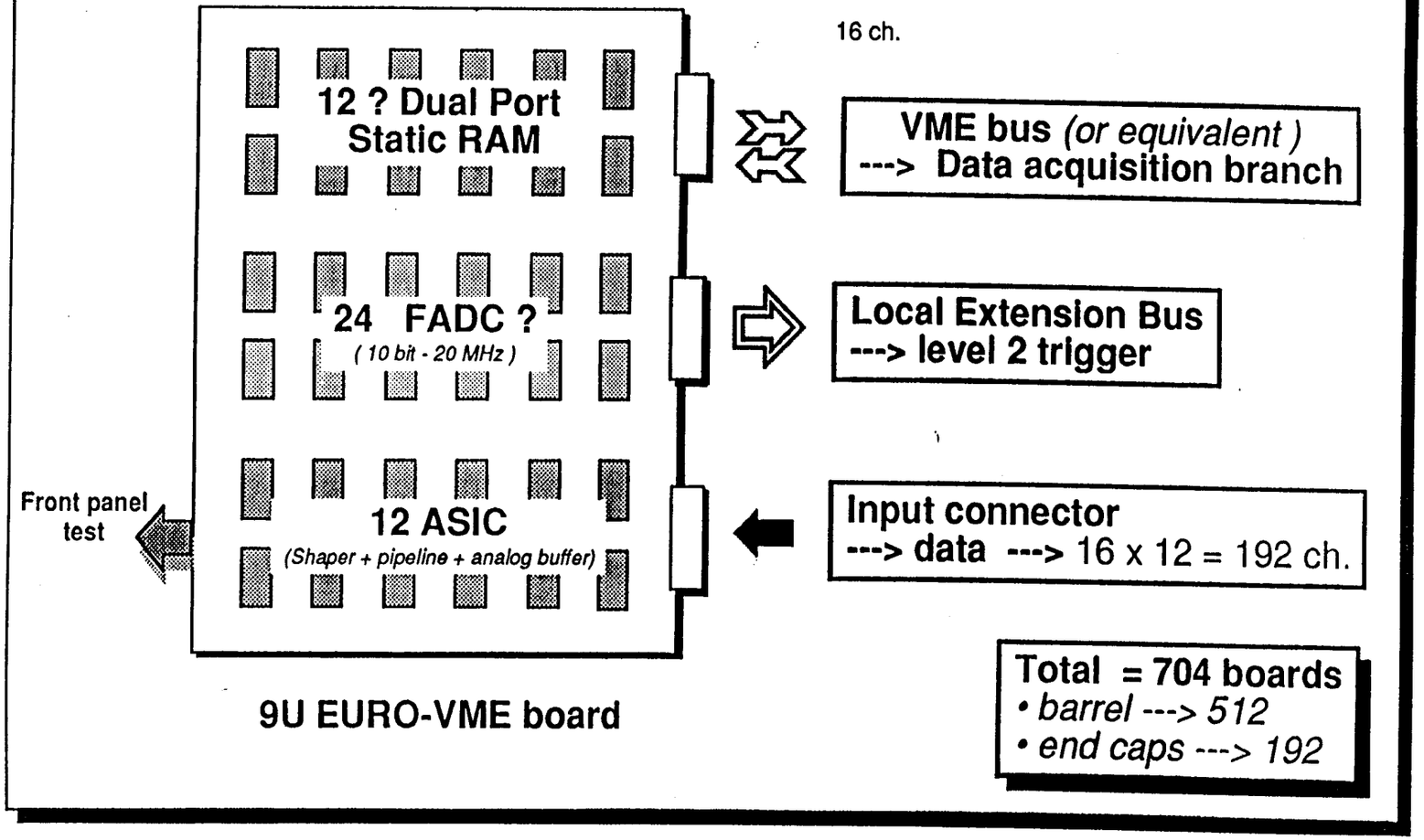
DSM - Saclay

May 1991

Front end read out scheme



Front end board layout



NOISE CONTRIBUTION

SPECIFICATIONS (APD)

$C_{det} \approx 2$ pF
$I_{leak} \approx$ 10 to 50 nA
Shaping time $\leq$ 16ns ?

NOISE CALCULATION FOR AN RC-(CR)^5 FILTER

$$ENC_T^2 = ENC_S^2 + ENC_{//}^2$$

$$= \underbrace{2kT \frac{2n}{3gm} C_{in}^2 \langle N_\Delta^2 \rangle}_{\text{Input transistor}} + q I_{leak} \langle N_s^2 \rangle$$

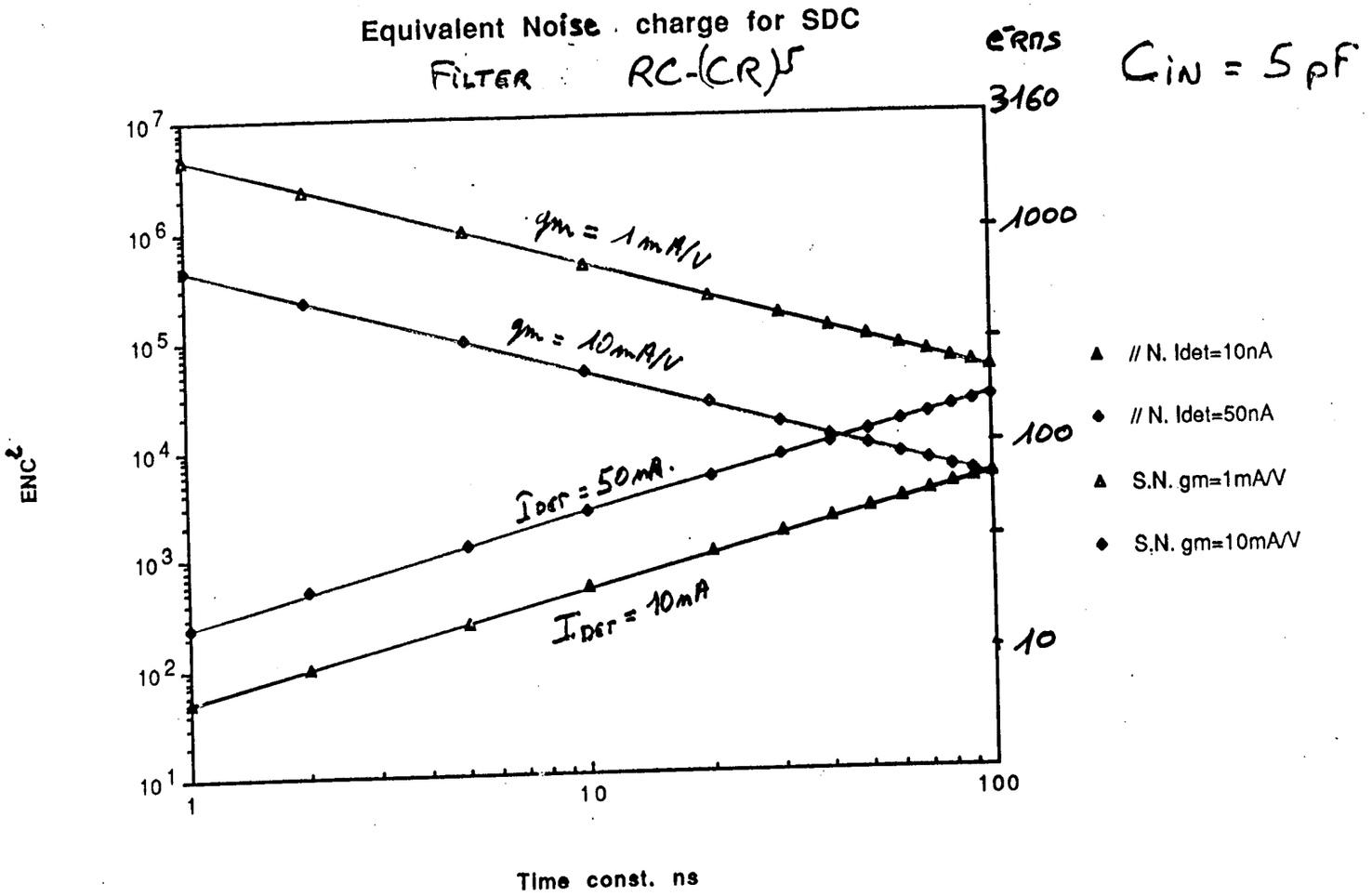
$\langle N_s^2 \rangle = 0.8\,\tau$

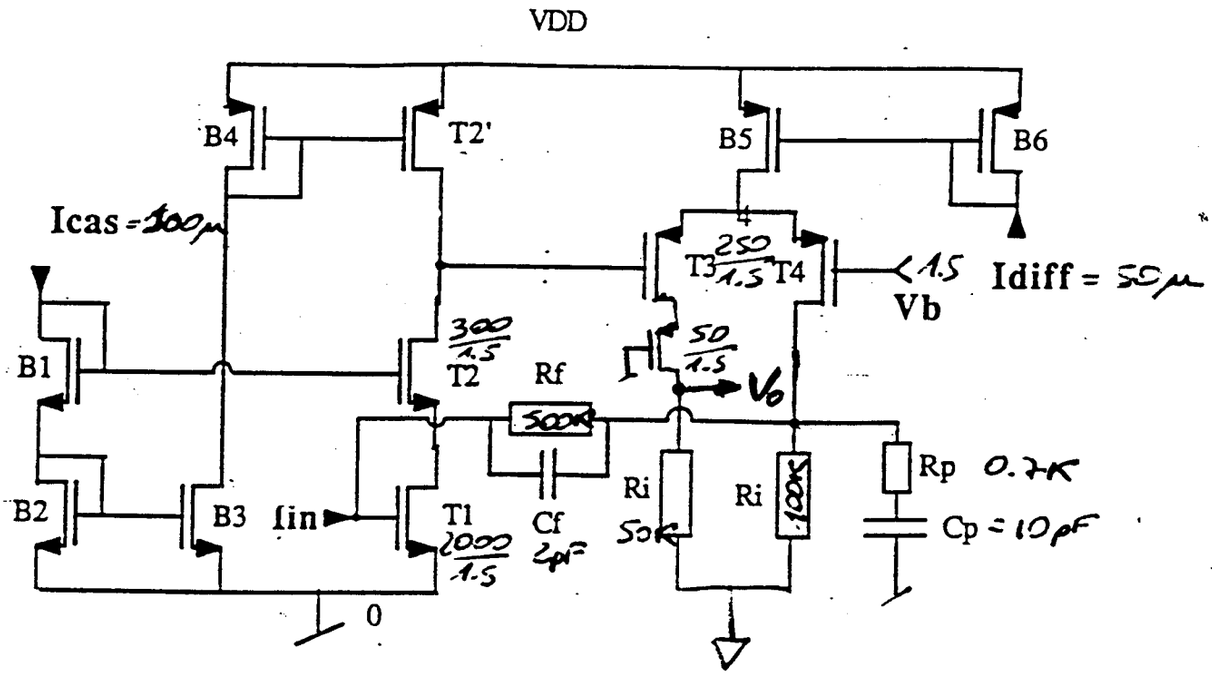
$\langle N_\Delta^2 \rangle = 2.22 / \tau$

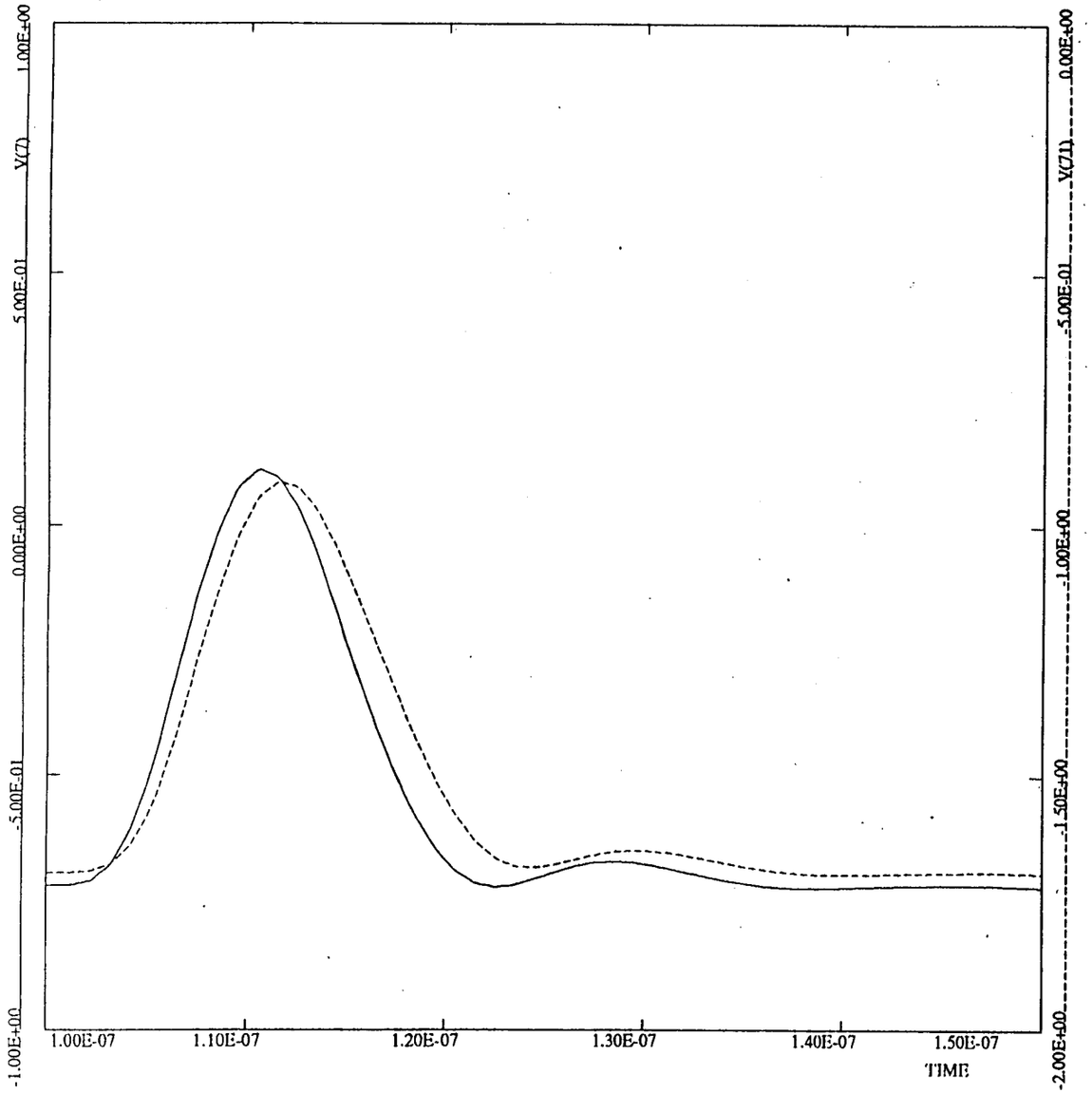
$C_{in} = C_{det} + C_{Tin} \approx 5$ pF

Input transistor : gm $\approx$ 3 mA / V

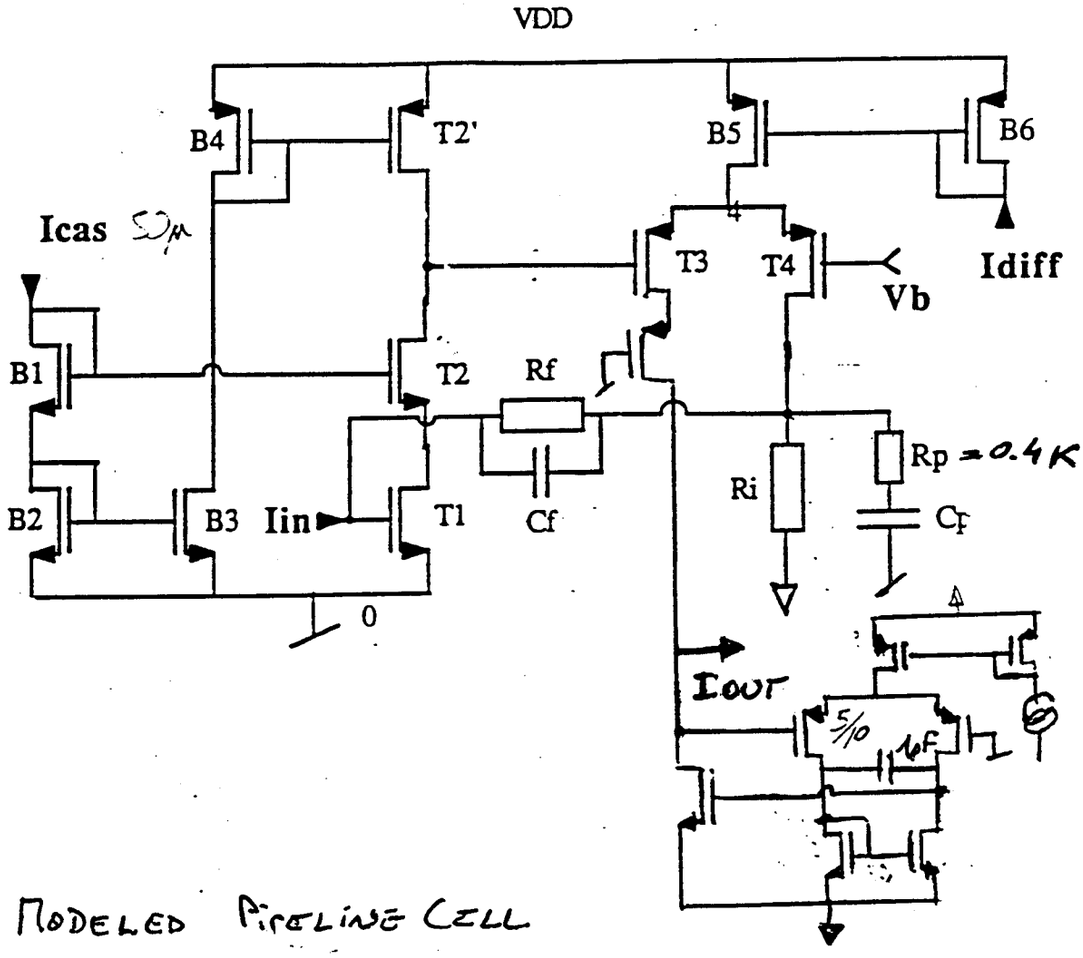
➔ LIMITATION DUE TO THE SERIE NOISE


Equivalent Noise charge for SDC
FILTER RC-(CR)5
eRMS
3160
1000
100
10
C_{IN} = 5 pF
10^7
10^6
10^5
10^4
10^3
10^2
10^1
ENC²
gm = 1 mA/V
gm = 10 mA/V
I_{DET} = 50 mA
I_{DET} = 10 mA
1
10
100
Time const. ns
// N. Idet=10nA
// N. Idet=50nA
S.N. gm=1mA/V
S.N. gm=10mA/V

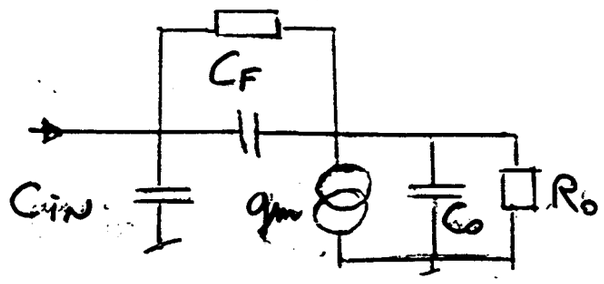

VDD
B4
T2'
B5
B6
Icas = 100µ
T3 250/1.5 T4
1.5
Vb
Idiff = 50µ
B1
300/1.5
T2
Rf
500K
50/1.5
Vo
B2
B3
Iin
T1
1000/1.5
Cf
2pF
Ri
50K
Ri
100K
Rp 0.7K
Cp = 10pF
0

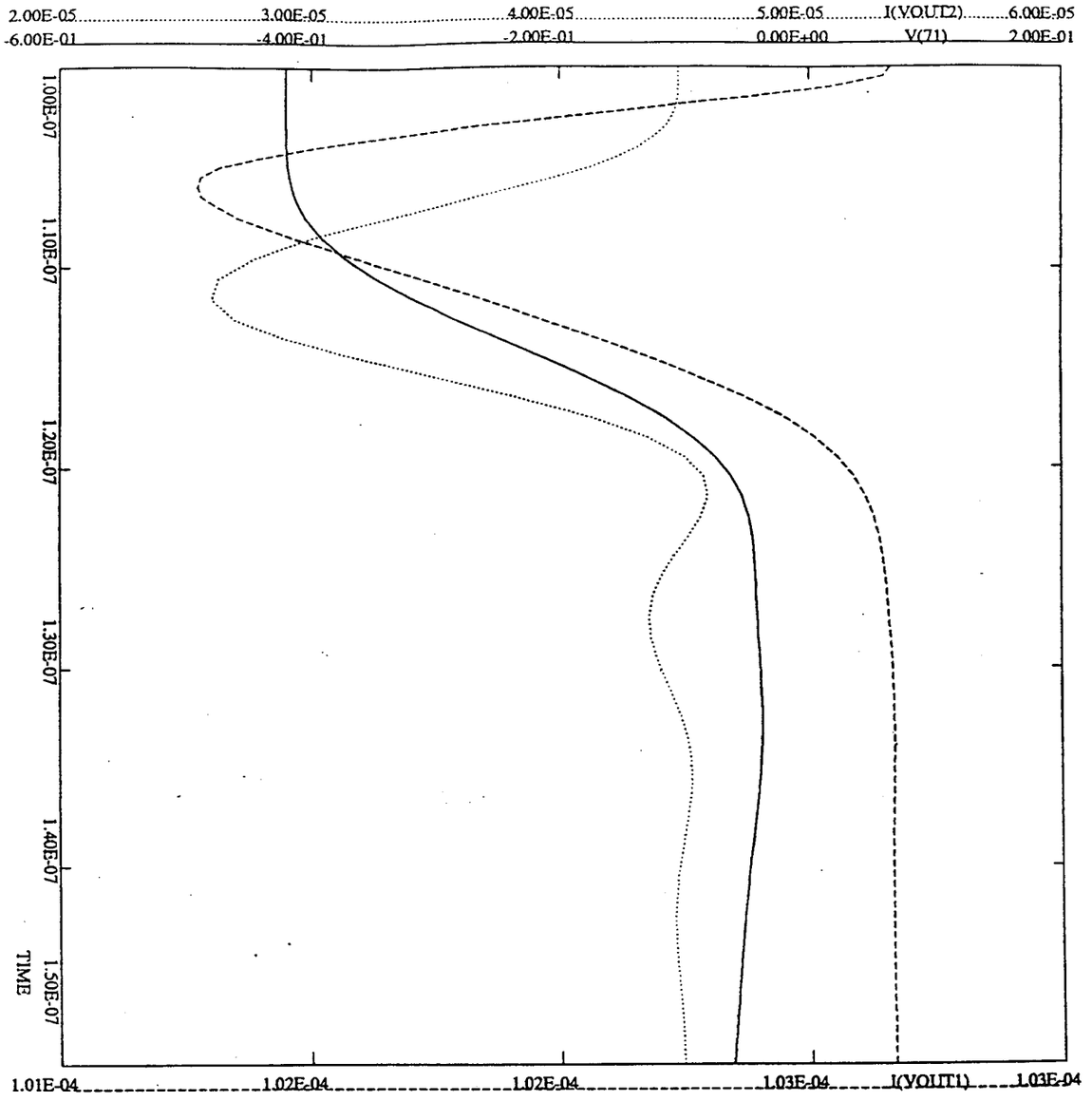


CURRENT AMPLIFIER



MODELED PIPELINE CELL



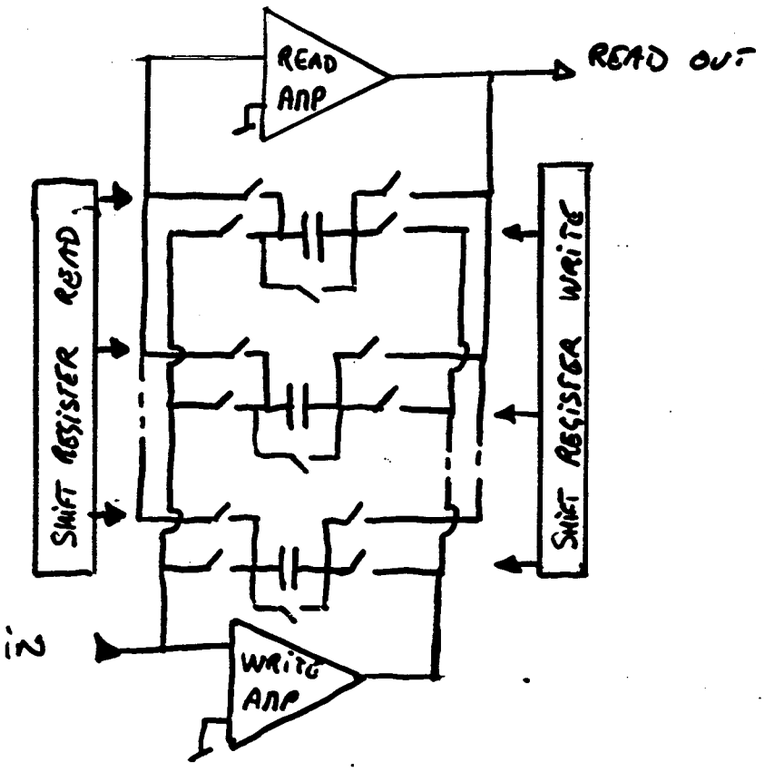


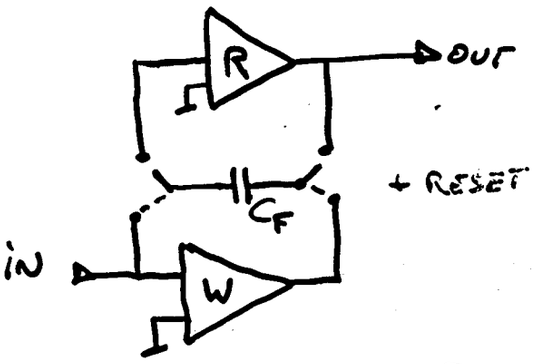
PRESHOWER FRONT-END

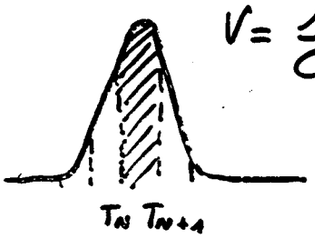
CEA , 26-FEB-91 10-24

PIPELINE

CHARGE INTEGRATOR / VOLTAGE SAMPLI







$$V = \frac{1}{C}\int_{T_N}^{T_{N+1}} i\,dt$$

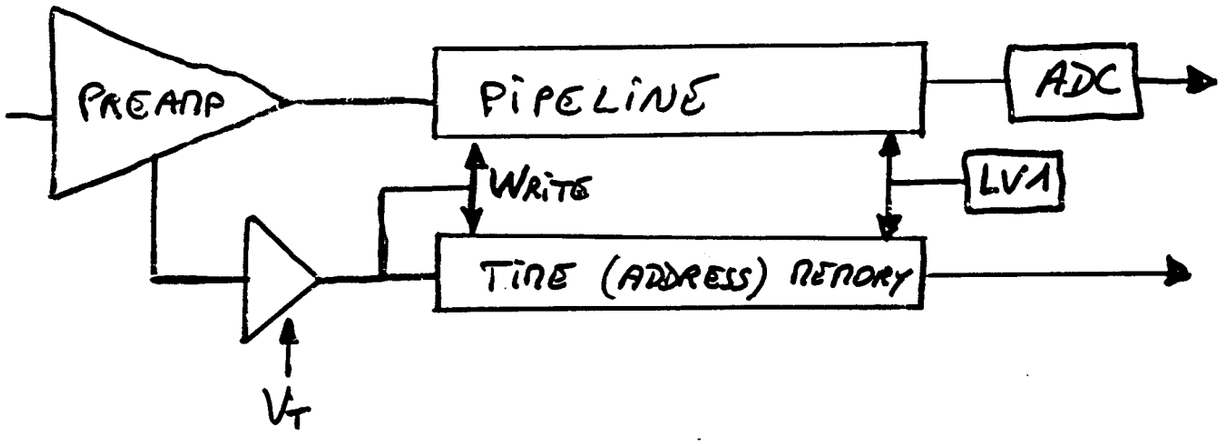
CHARGE INTEGRATOR : $V_{OUT} = \frac{Q_{IN}}{C_F} = \frac{I_{IN} \cdot T}{C_F}$

RISE TIME $\propto \frac{C_0}{g_m} \cdot \frac{C_{IN}}{C_F} = \frac{1pF \; 1pF}{10^{-3} \cdot 0.5pF} \simeq 2ns.$

NOISE = PREAMP / SHAPER NOISE CONVOLUTED WITH THE INTEGRATION TIME.

DELAY $\simeq 2\mu s \Rightarrow$ 128 CELLS

'DATA DRIVEN' PIPELINE



⟹ REDUCTION OF THE PIPELINE LENGTH

TIME (ADDRESS) MEMORY -

DIGITAL : COUNTER + MEMORY

ANALOG : CURRENT SUMMATION ON C.
VOLTAGE AMP.

RAD-HARD TECHNOLOGY

WHAT'S AVAILABLE IN EUROPE ?

ABB CMOS / SOS

MARCONI CMOS / SOS

THORSON CMOS / SOI (DIGITAL)
BIPOLAR / SOI

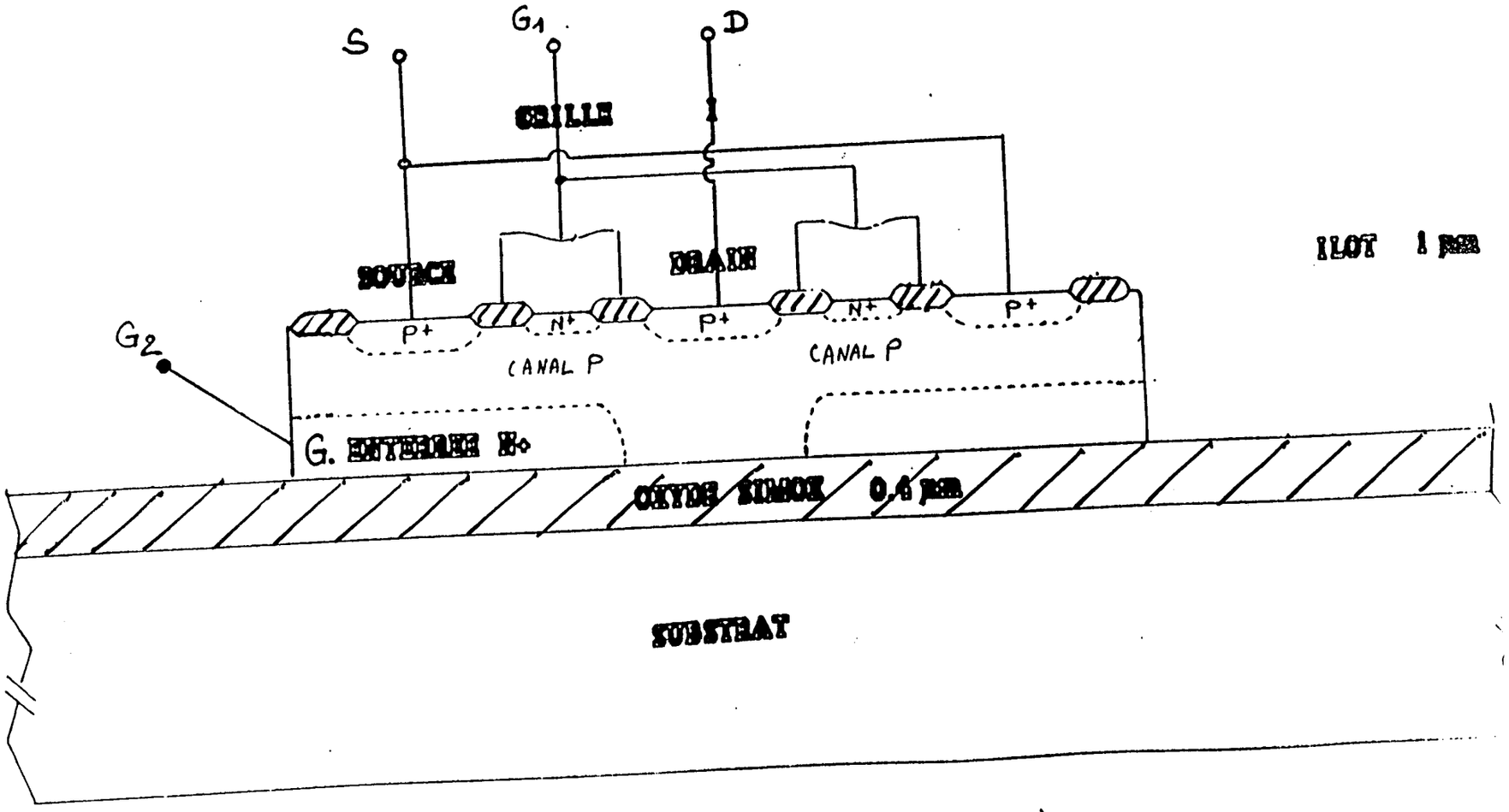
IS GaAs RAD-HARD ENOUGH ?

CEA LETI / DAII / DSII

⇒ NEW S.O.I. CMOS
+ JFETs
+ BIPOLAR
(VERTICAL NPN
PNP)

SPECIFICATION ⇒ 10 Meg RAD / 10 years
$10^{14} - 10^{15}$ n/cm² / 10 year

D. LETI / MEL / S. MSC



GRILLE ENTERREE PARTOUT SAUF SOUS LE DRAIN (VERSION STANDARD)

GRILLE SUPERIEURE

BAR DOSE

GRILLE INF.

D. LETI / MEL / S. MSC

521.1.egr 10/25/89 ocument est la propriete d -DAM et ne peut etre roduit ou communique sans autorisation

PJFET LOT 242 TR9 SR2 P2 L3G2 56/2 mesure 5

GAMMA-

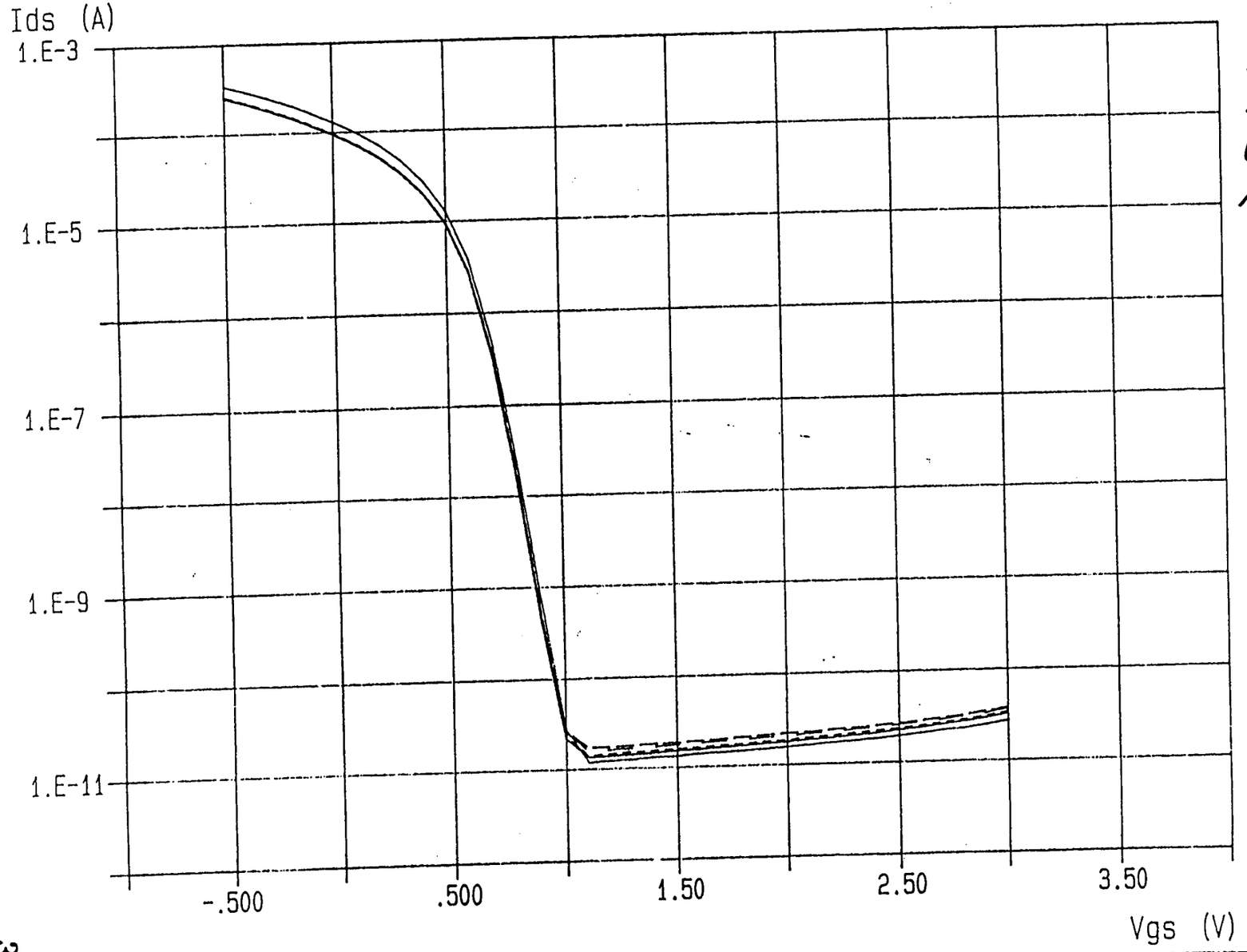
0. krad

30. krad

300. krad

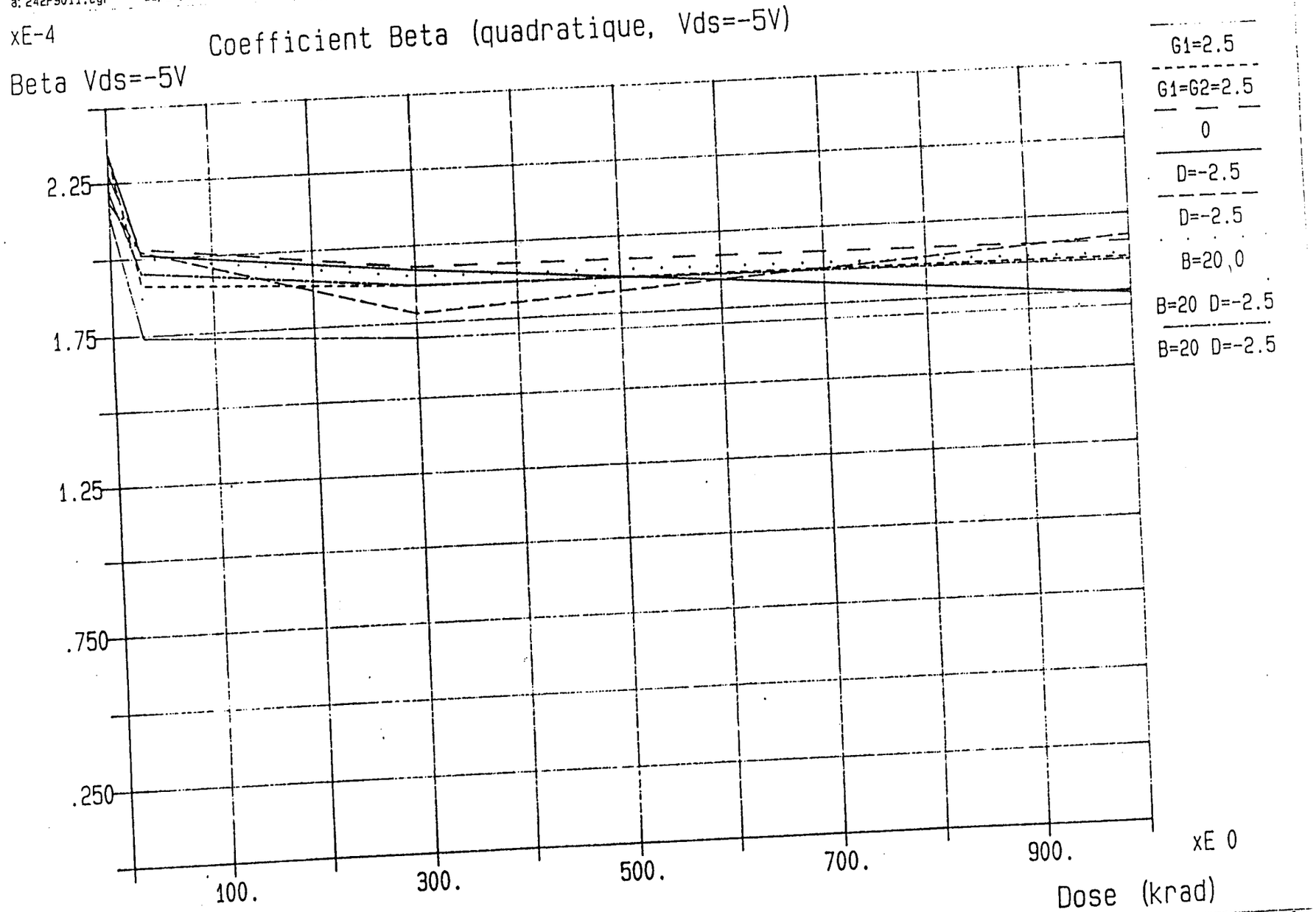
600. krad

1000. krad

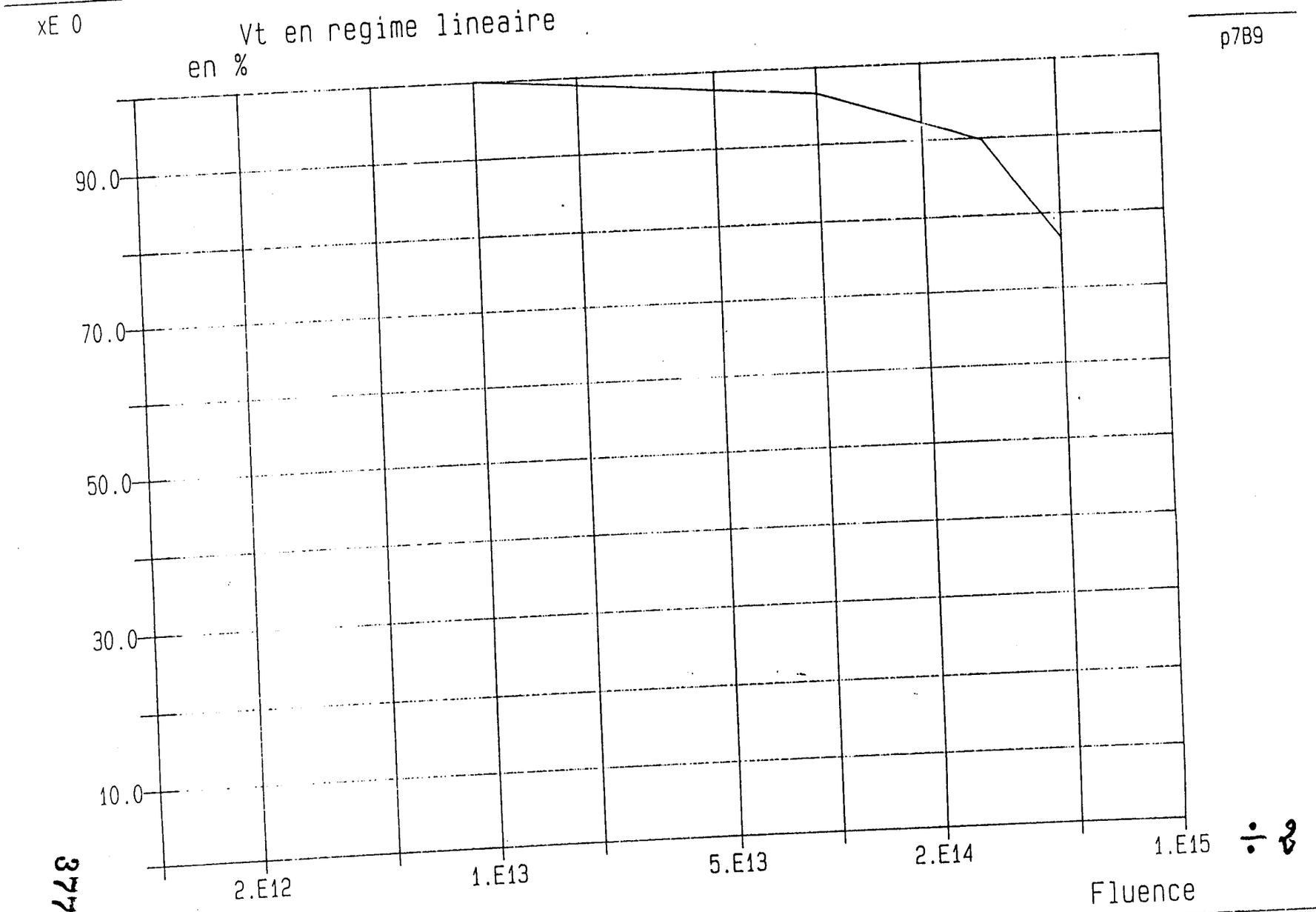


document est la propriété

a:242P9011.egr 11/22/89



242p9016.egr 11/22/89 C. :ument est la propriete du CEA-DAM et ne peut etre . oduit ou communique sans autorisation



÷ 2

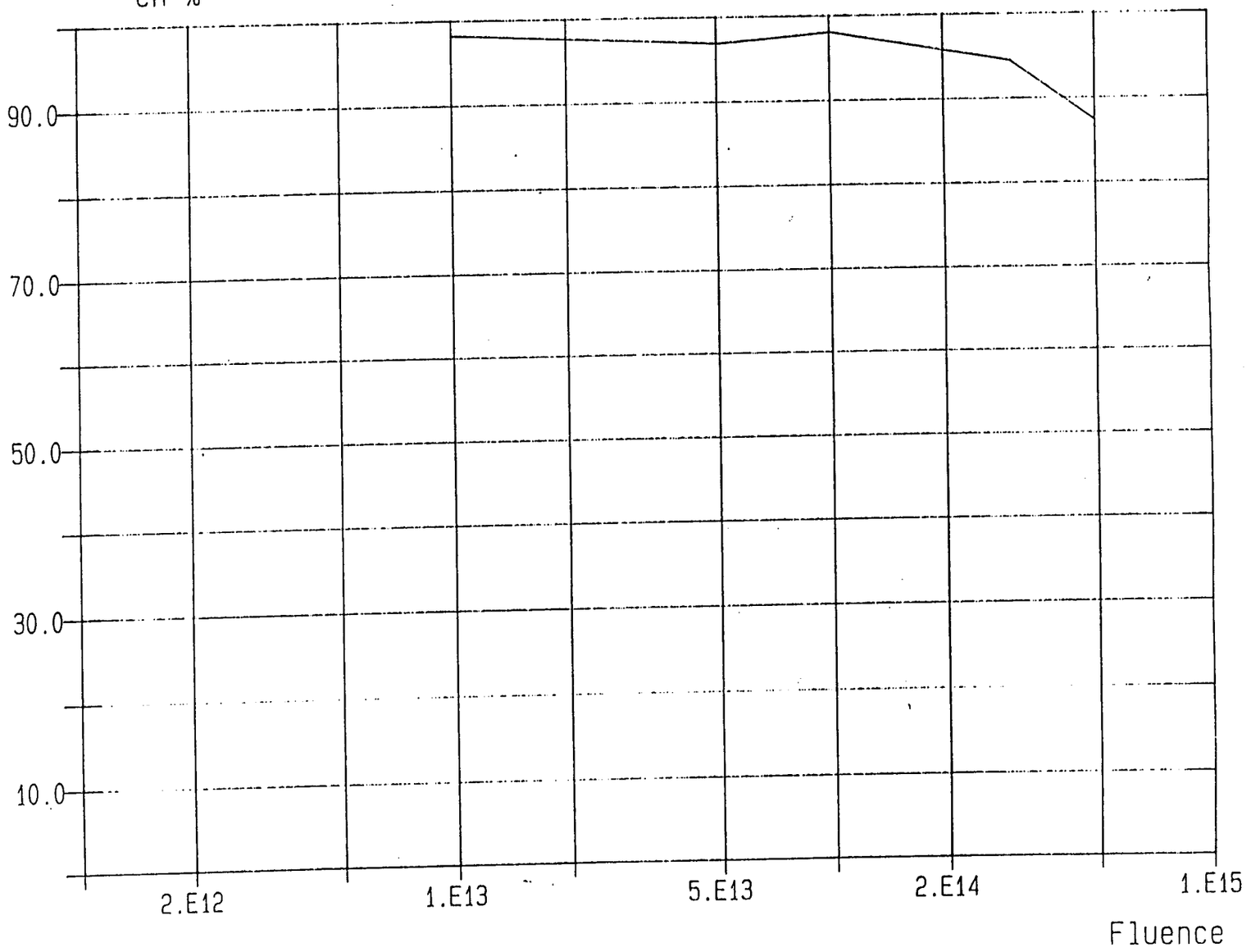
242p9017.egr 11/22/89 document est la propriete du CEA-DAM et ne peut et[illegible]produit ou communique sans autorisation

xE 0

Beta lineaire

en %

p789



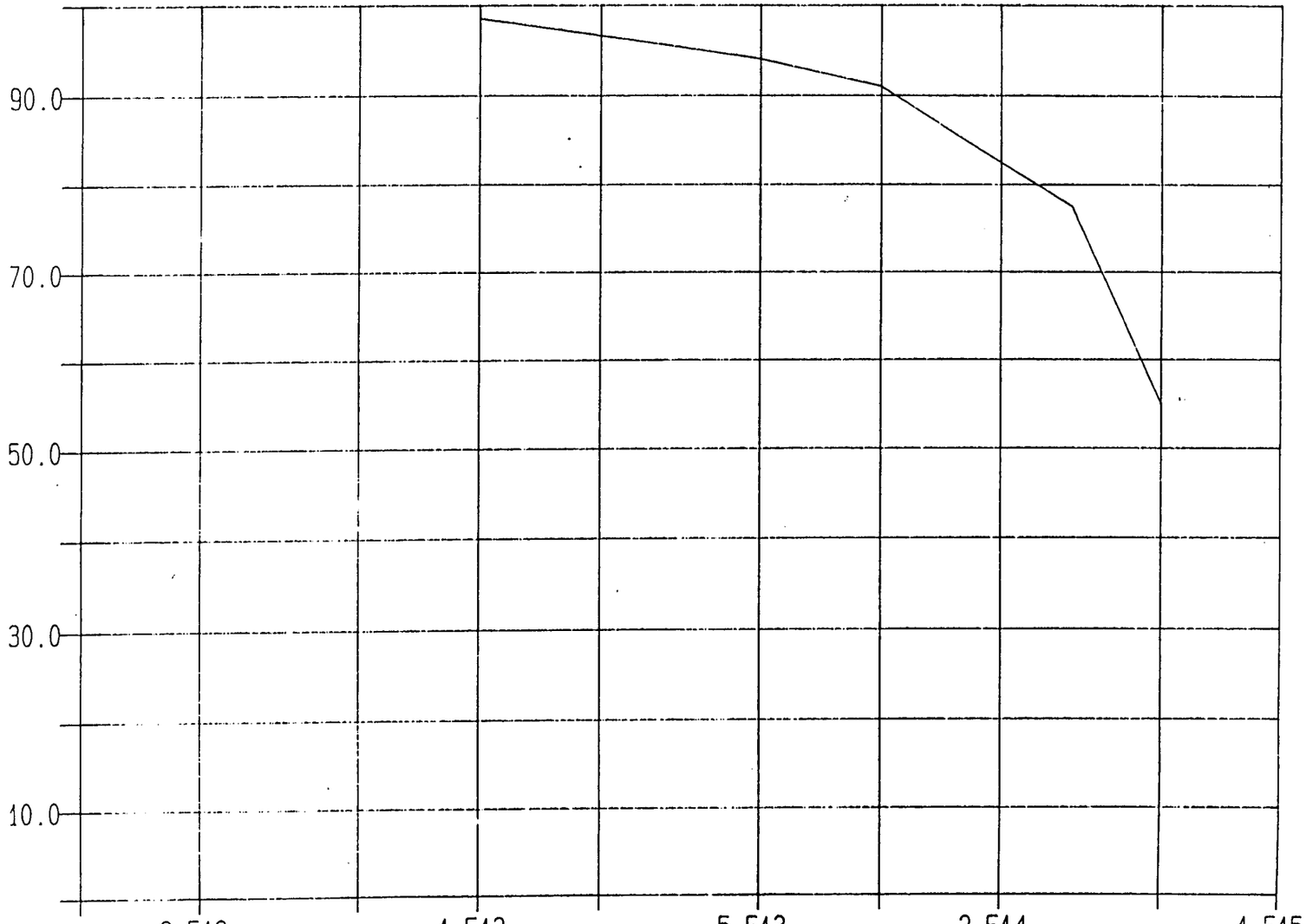
242p9015.egr 11/22/89 Ce ument est la propriete du CEA-DAM et ne peut etre r oduit ou communique sans autorisation

xE 0

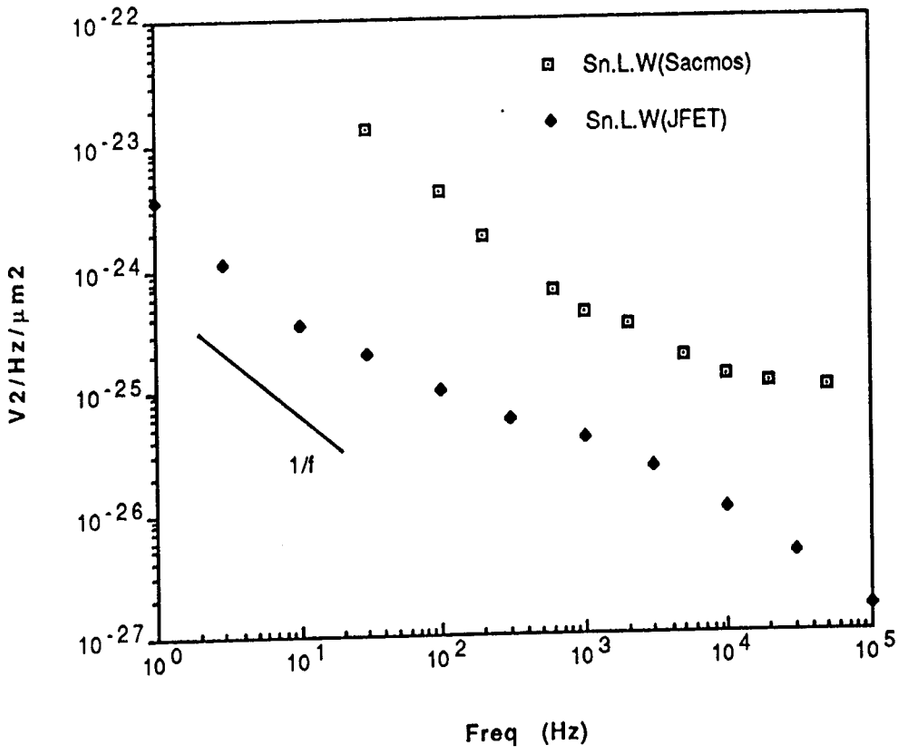
Idss en regime quadratique pjfet

en %

p7B9



Comparison between JFET/SOI and SACMOS p channel.
Input noise Normalised to the gate area



PJFET/SOI ≈ 2N4416

Preamp/Shaper/Disc/TVCAMU

R. Van Berg

STRAW ELECTRONICS

PREAMP / SHAPER / DISCRIMINATOR / TVC AMU

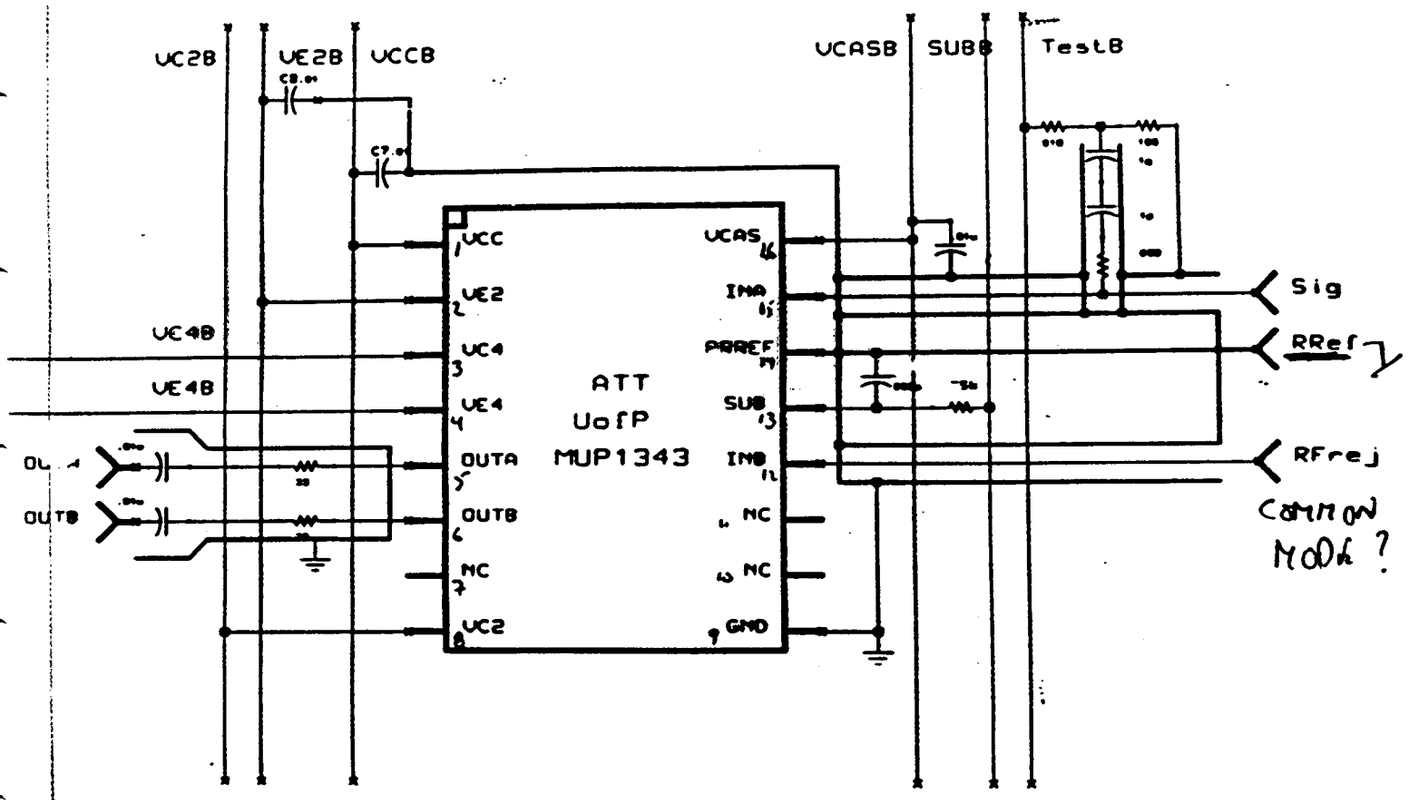
PA/S –
AT&T SINGLE CHANNEL
95% YIELD ON WAFER
90+% PACKAGED

PA/S/D
TEKTRONIX, MULTICHANNEL, QUICKSILE
SEPARABLE
TEK. SPICE CHECK
TEK ERC
LAYOUT ...

TVC AMU
TINY CHIPS
RELAYOUT/SIMULATE

PACKAGING
COLORADO
ORNL
HIGH DENSITY ?
PICKUP NOISE ?

FIGURE 2 Single Channel Circuit



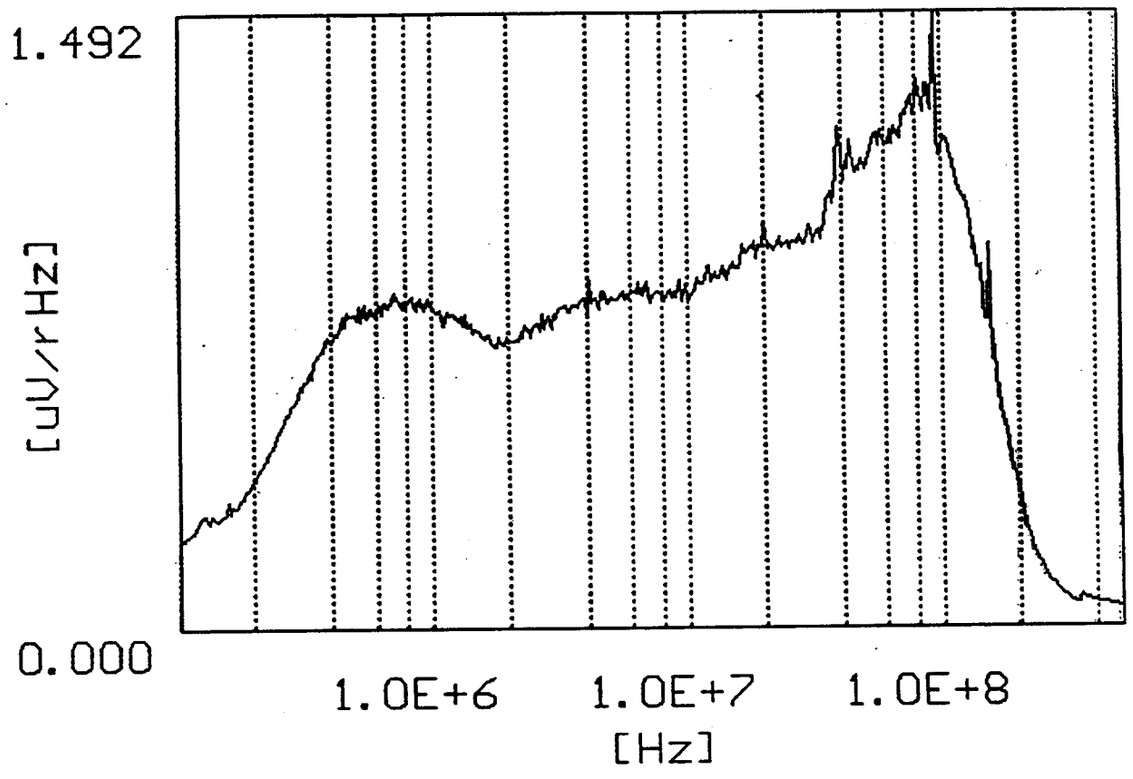
Four Channel Circuit

The circuit diagram of the full board is simply four of the above single chip circuits plus power supply, power distribution and filtering, test pulse distribution, input connector, output connector options, and voltage test points.

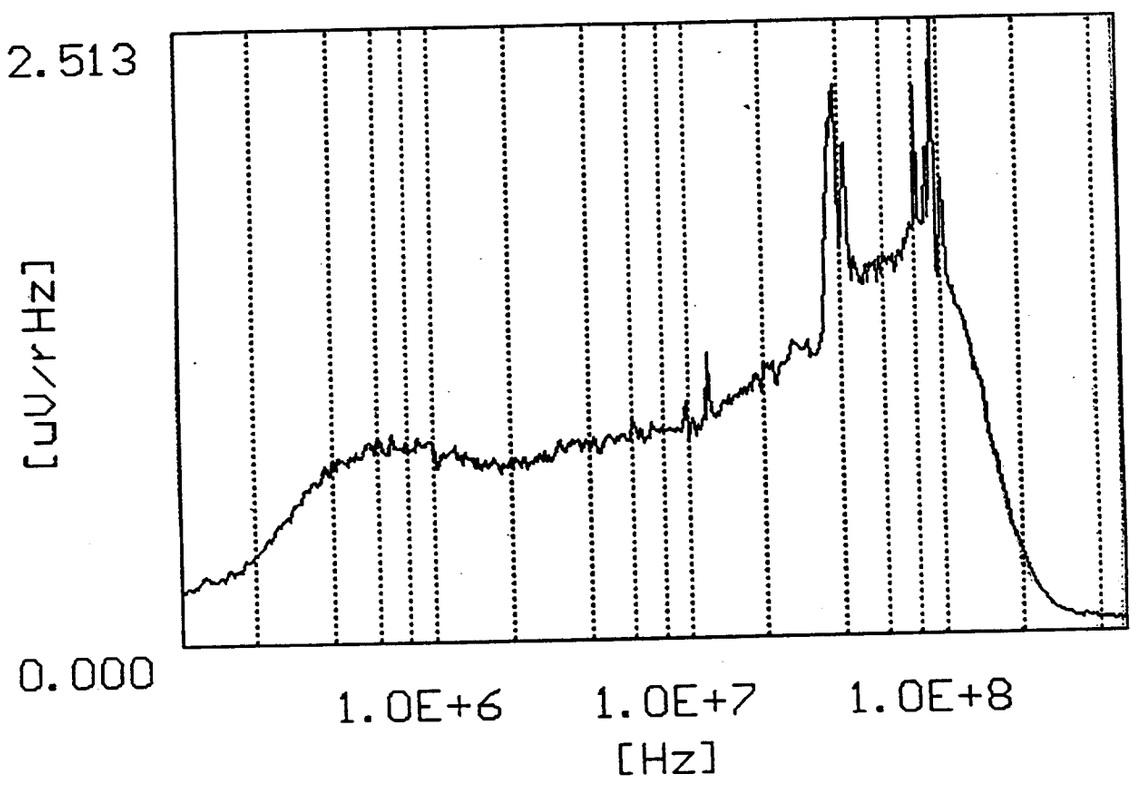
ATT PREAMP / SHAPER
NOISE SPECTRUM

RMS NOISE x10

Integral: 11.084879 mV [a,b] = [1.5e+05 Hz, 9.91e+07 Hz]

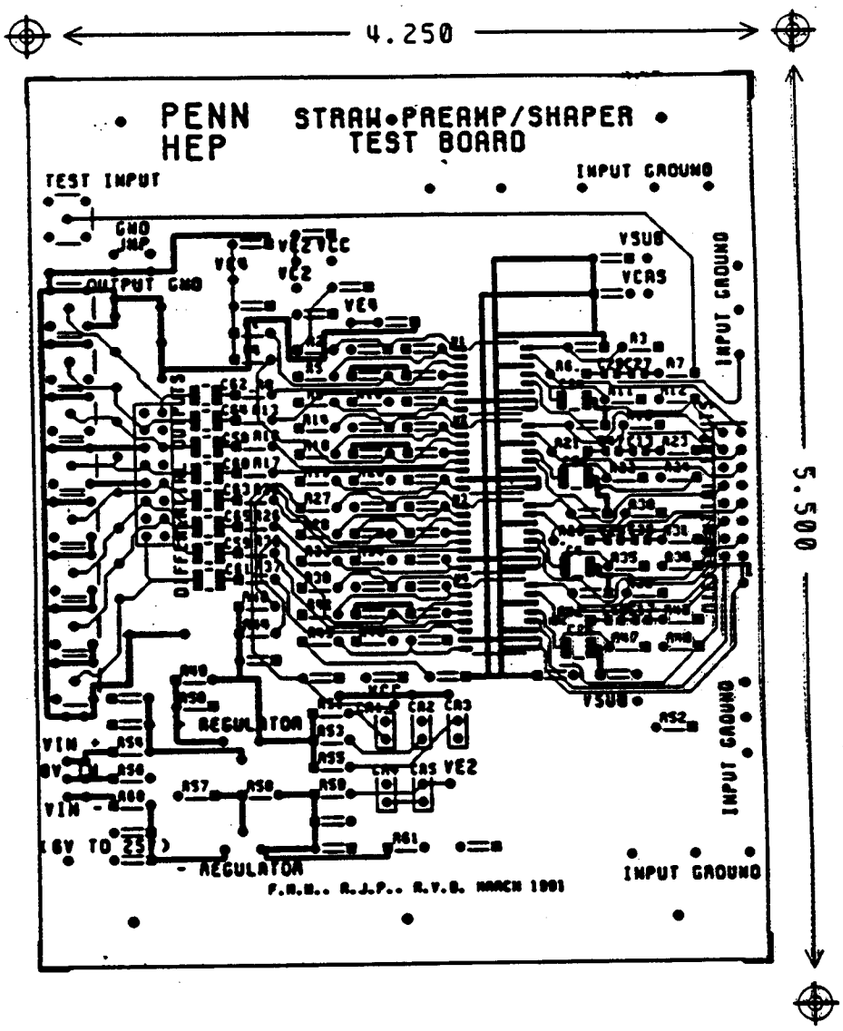


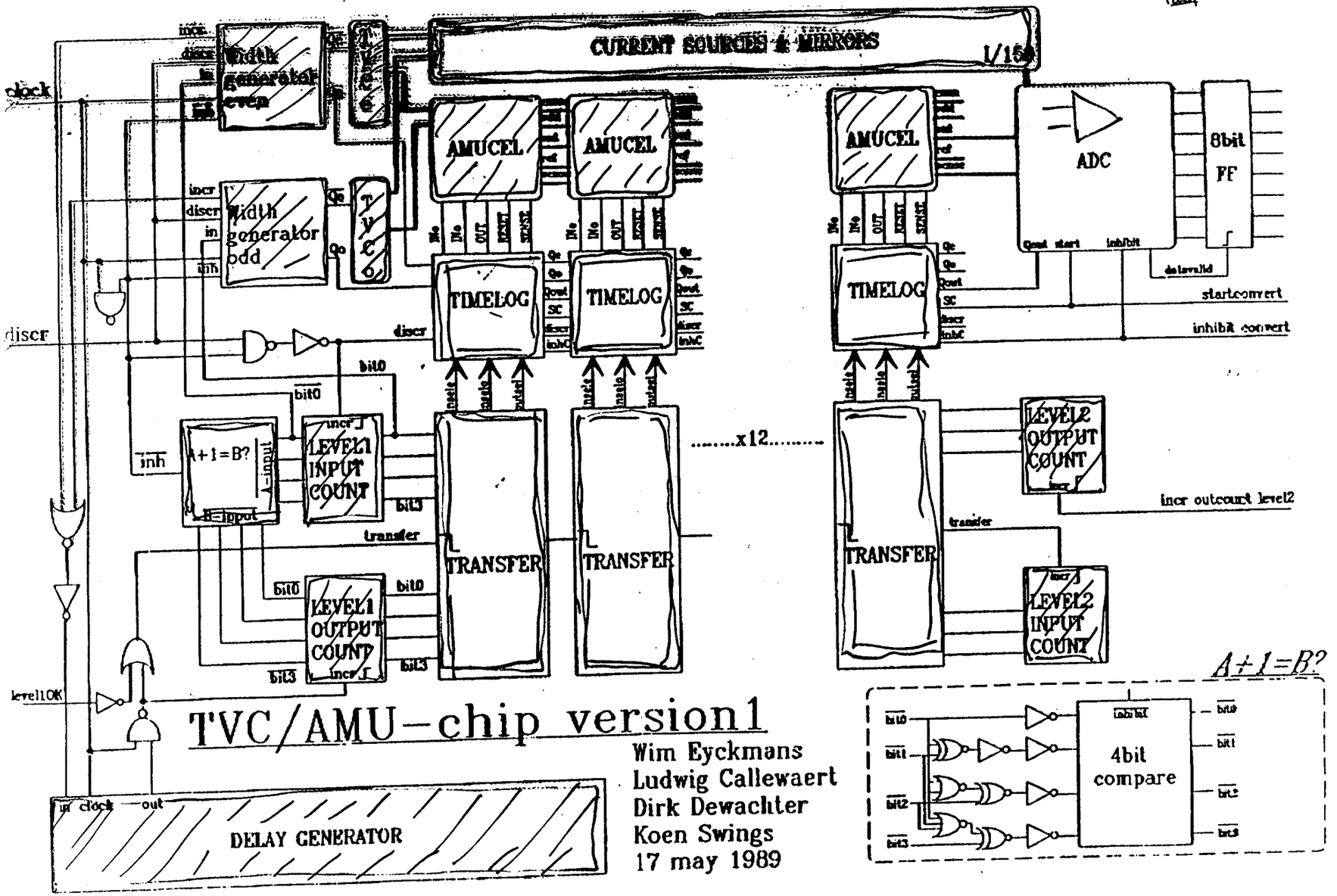
Integral: 16.583503 mV [a,b] = [1.5e+05 Hz, 9.91e+07 Hz]

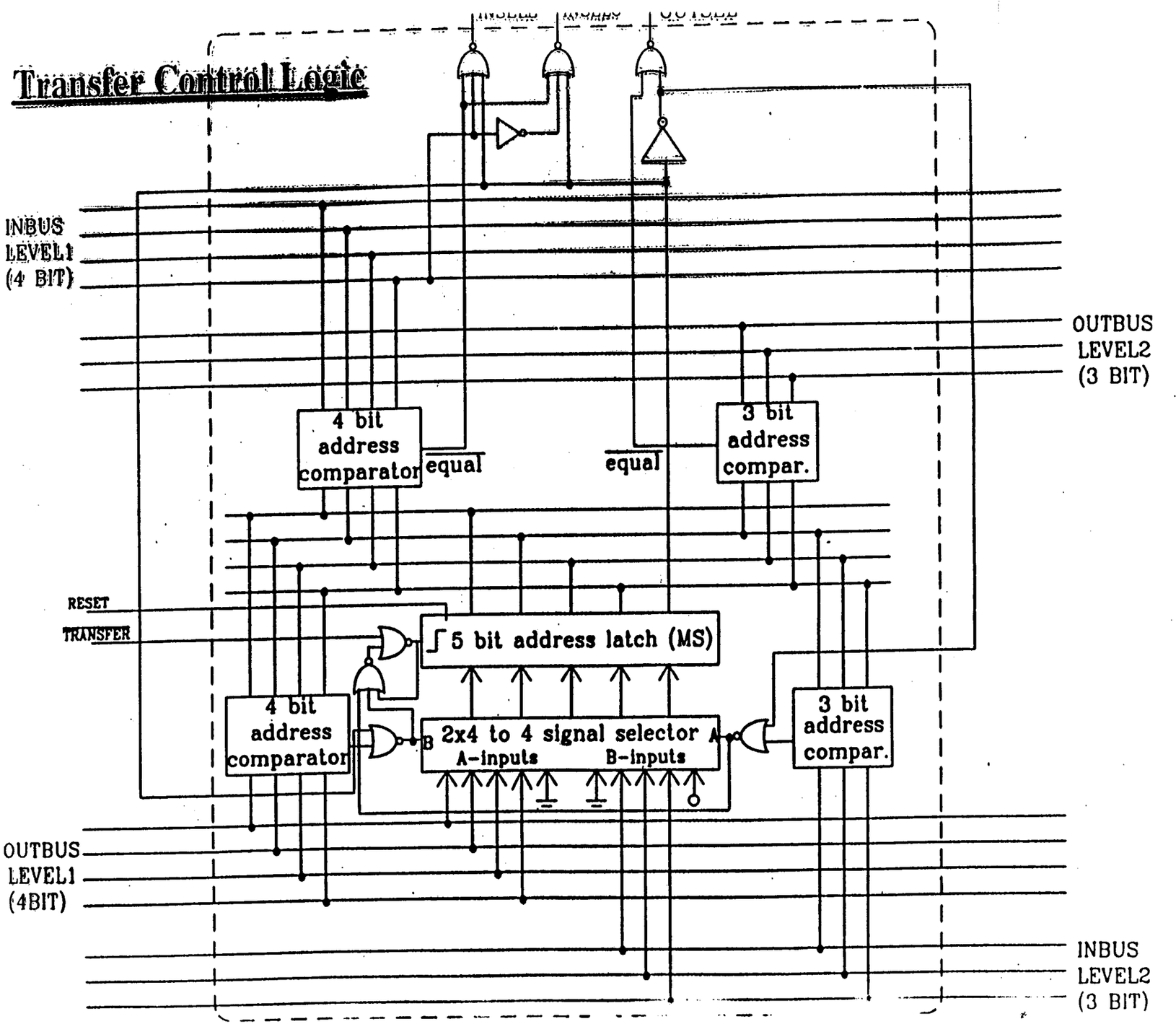


Board Layers

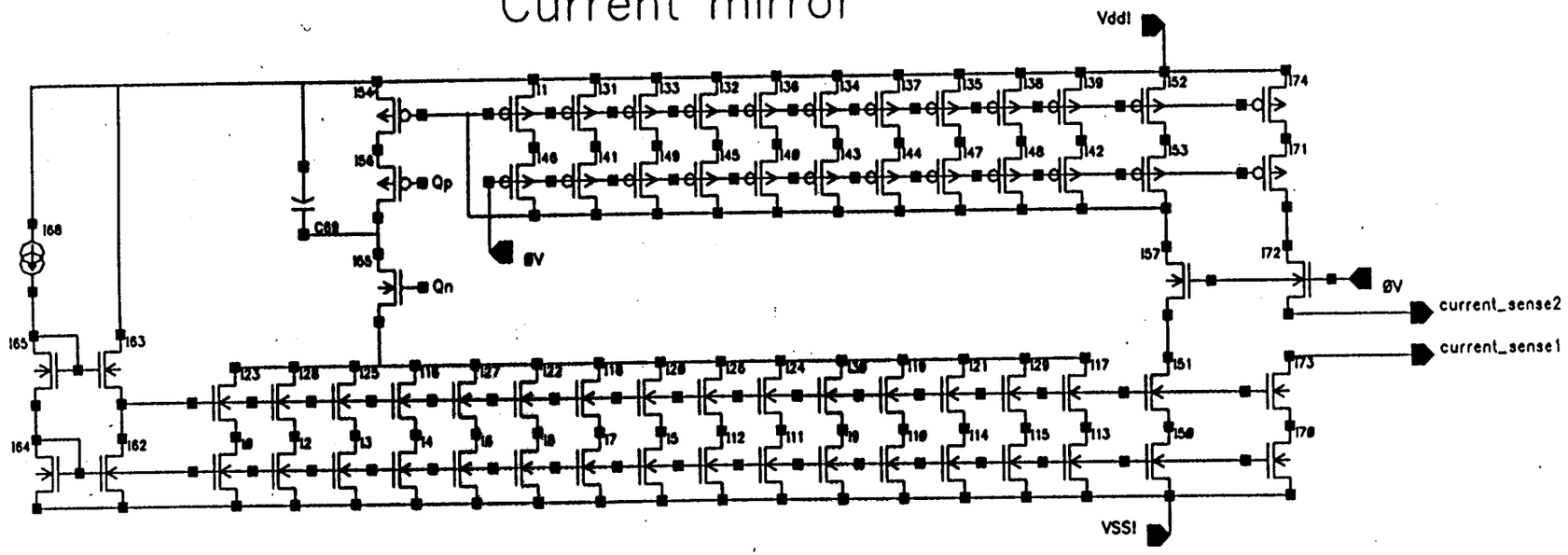
FIGURE 5 Silkscreen and Top Signal Layer -




CURRENT SOURCES & MIRRORS
1/150
clock
discr
inh
Width generator even
Width generator odd
TVC
AMUCEL
TIMELOG
TRANSFER
LEVEL1 INPUT COUNT
LEVEL1 OUTPUT COUNT
A+1=B?
A-input
B-input
bit0
bit3
transfer
.....x12.....
ADC
8bit FF
LEVEL2 OUTPUT COUNT
LEVEL2 INPUT COUNT
startconvert
inhibit convert
incr outcount level2
level1OK
DELAY GENERATOR
in clock out
TVC/AMU-chip version1
Wim Eyckmans
Ludwig Callewaert
Dirk Dewachter
Koen Swings
17 may 1989
A+1=B?
4bit compare

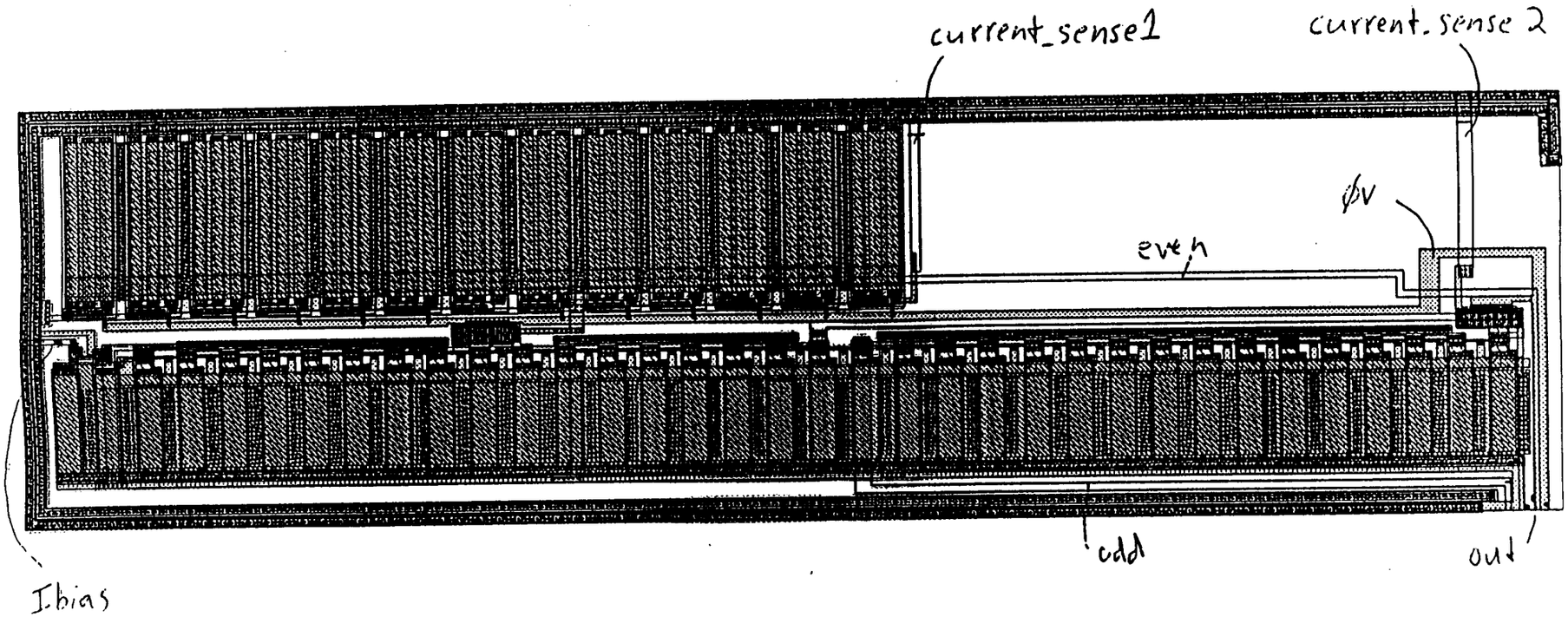

Transfer Control Logic
INBUS
LEVEL1
(4 BIT)
OUTBUS
LEVEL2
(3 BIT)
4 bit
address
comparator
equal
equal
3 bit
address
compar.
RESET
TRANSFER
5 bit address latch (MS)
4 bit
address
comparator
2x4 to 4 signal selector
A-inputs
B-inputs
3 bit
address
compar.
OUTBUS
LEVEL1
(4BIT)
INBUS
LEVEL2
(3 BIT)

Current mirror

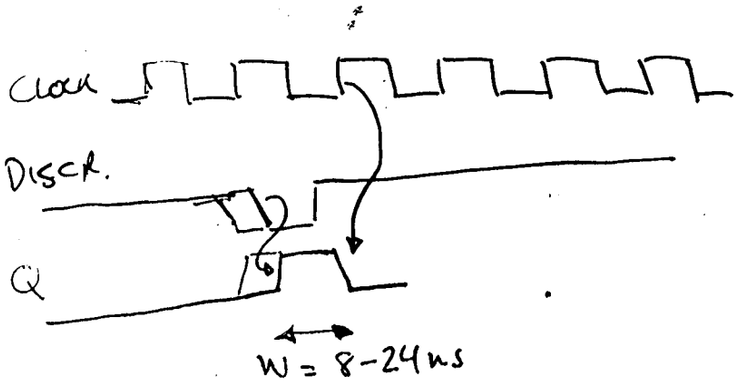


	V_{DD}	V_{SS}	I/I
NOM	3.0	-3.0	149.9876
	±0.1	±0.1	149.98 33 - 87 -
Run 31			150.0036
Run 35	±0.1	±0.1	149.9056

current.2
1640λ × 431λ
λ = 0.8um

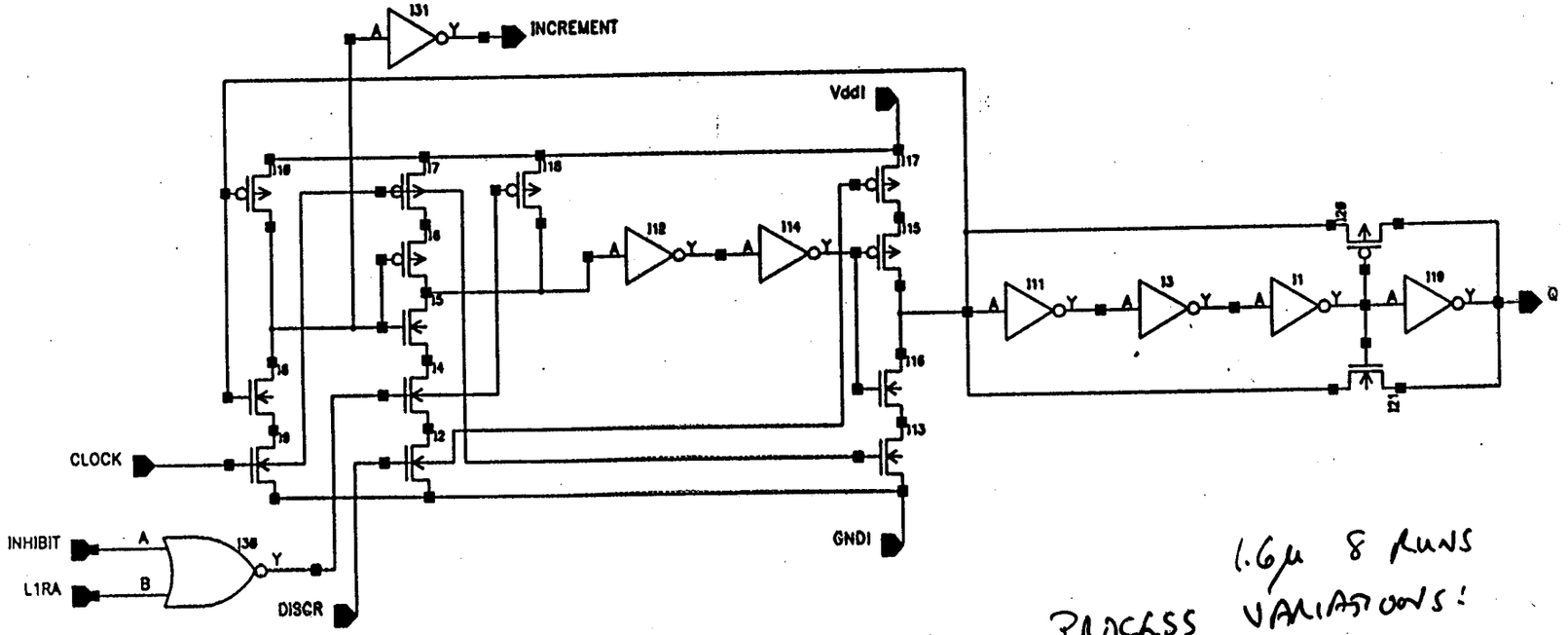


390



$\delta W \begin{matrix} +20 \\ -11 \end{matrix}$ ps over range

Width generator



1.6μ 8 runs

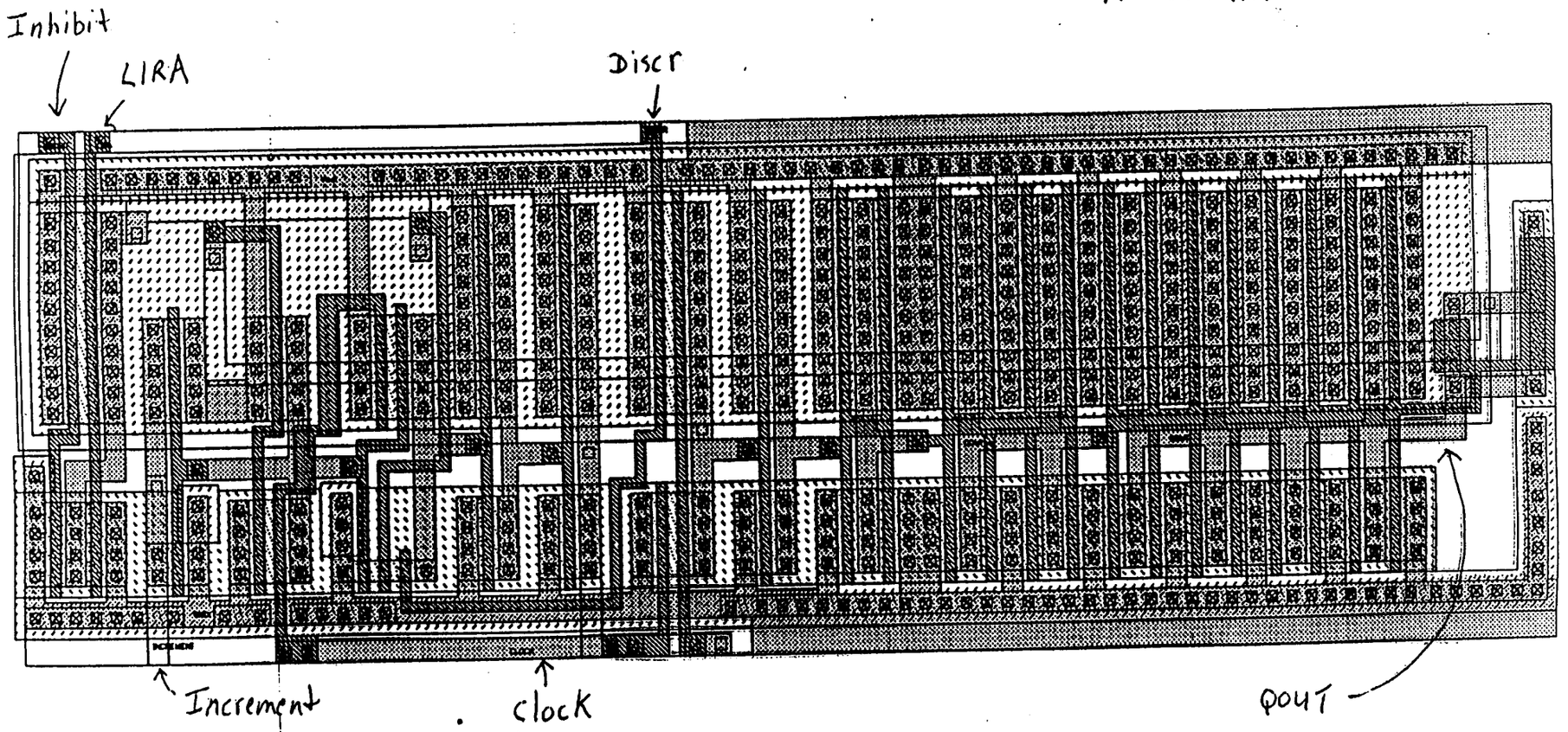
Process variations:

ΔL_N	.35 ± .07
ΔL_P	.12 ± .09
ΔW_N	.25 ± .13
ΔW_P	.63 ± .10
$KP_{N/...}$	2.5 ± .28

Cell wigen.3

300λ × 101λ

λ = 0.8μm



Readout of Shower Max Detectors

D. Hubbard

PRESHOWER SHOWERMAX

FRONT ENDS

Northeastern
Rockefeller
Saclay
SSC
UCLA
Yale

Optical readouts: Responsability of US groups

1) APD.
2) MCPMT.
3) SIT Pixel Tubes.
4) VLPCS.
5) Compact PMT

Front End Readout Architecture

RWR 6-4-91

Roger Rusack

(presented by Dick Hubbard)

CURRENT WORK 1991

We are testing different readout options in our forthcoming test beam run at Fermilab this summer. In that test beam we will test APD's and MCPMT's. These will be compared against a known image-intensifier CCD system which will be used as a reference.

APD's Avalanche Photo-Diodes

The APD's are conventional 500 μ devices from EG&G. We will have 96 which will be used to readout both the preshower and the shower maximum detctor.

1) Ball lens to match the light collection to the APD.
2) Temperature stabilised.
3) Gain order 100.
4) Quantum efficiency about 60%, better in the green than in the blue.

Work being done by SSC lab and Northeastern. and Saclay

MCPMT'S Multi-Channel Photo-Multiplier Tubes

Phillips 64 channel photomultiplier tubes will be tested for both the Preshower and the shower maximum. Conventional photocathode, fiber optic window and maximum gain is 10^6.

Yale - Preshower.
Saclay - Shower Maximum.

PIXEL TUBES: Silicon Intensified Target Tubes

This will not be in preshower/shower maximum test.
Purchasing from Hughes Aircraft bump bonded pixel arrays devices to test inside an image tube. Expect first results from these tests November.

Rockefeller, Yale and South Carolina.

Photon Detectors for Shower-Max

Cost requirement

120 K channels before descope

Current price $40/channel
Goal $20 photo-det + $20 electronics

Dynamic range

12 bit range
8 bit resolution

10 GeV to 400 GeV	×40
Fluctuations	×10
Centroide	×10
Dynamic range	4000

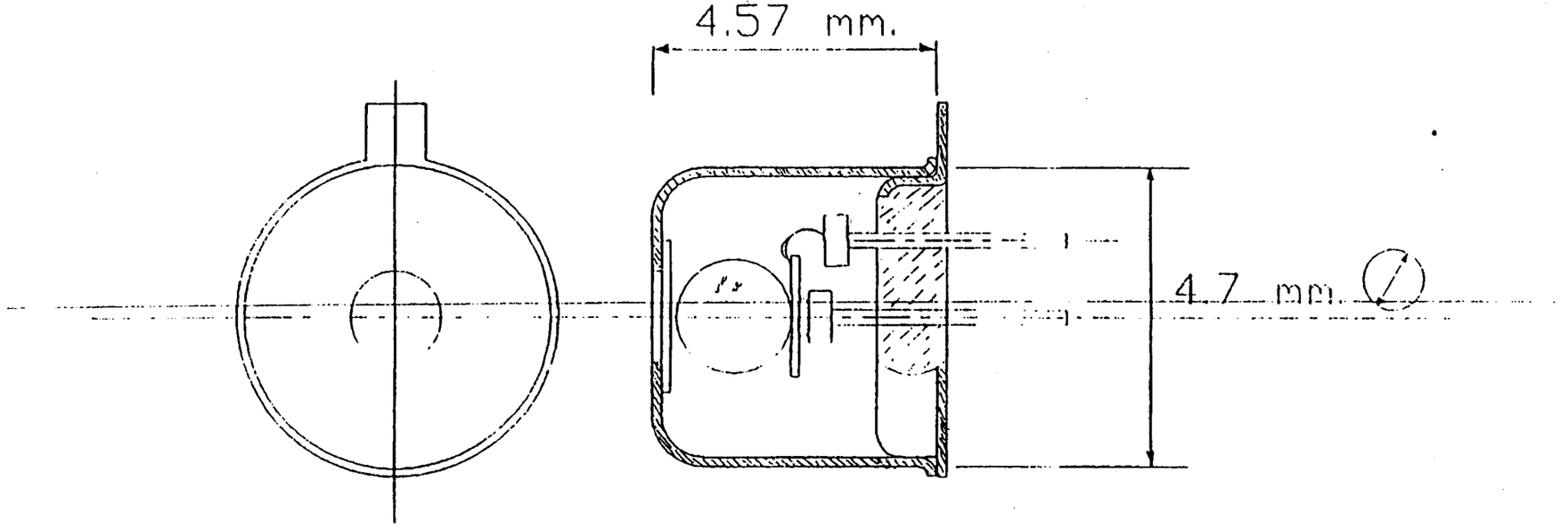
Minimum signal

3 photo-electrons / min-ionizing particle
×100 MIP @ 10 GeV at shower-max
× $\frac{1}{3}$ fluctuations
× $\frac{1}{10}$ centroide

---

10 photo-electrons (100 photons)

EG&G 'Avalanche Photo 'Diode with Ball Lens



Proposed assembly to focus output of 1mm. diam. scintillating fiber on an avalanche photo diode (C30902 OR C30817)

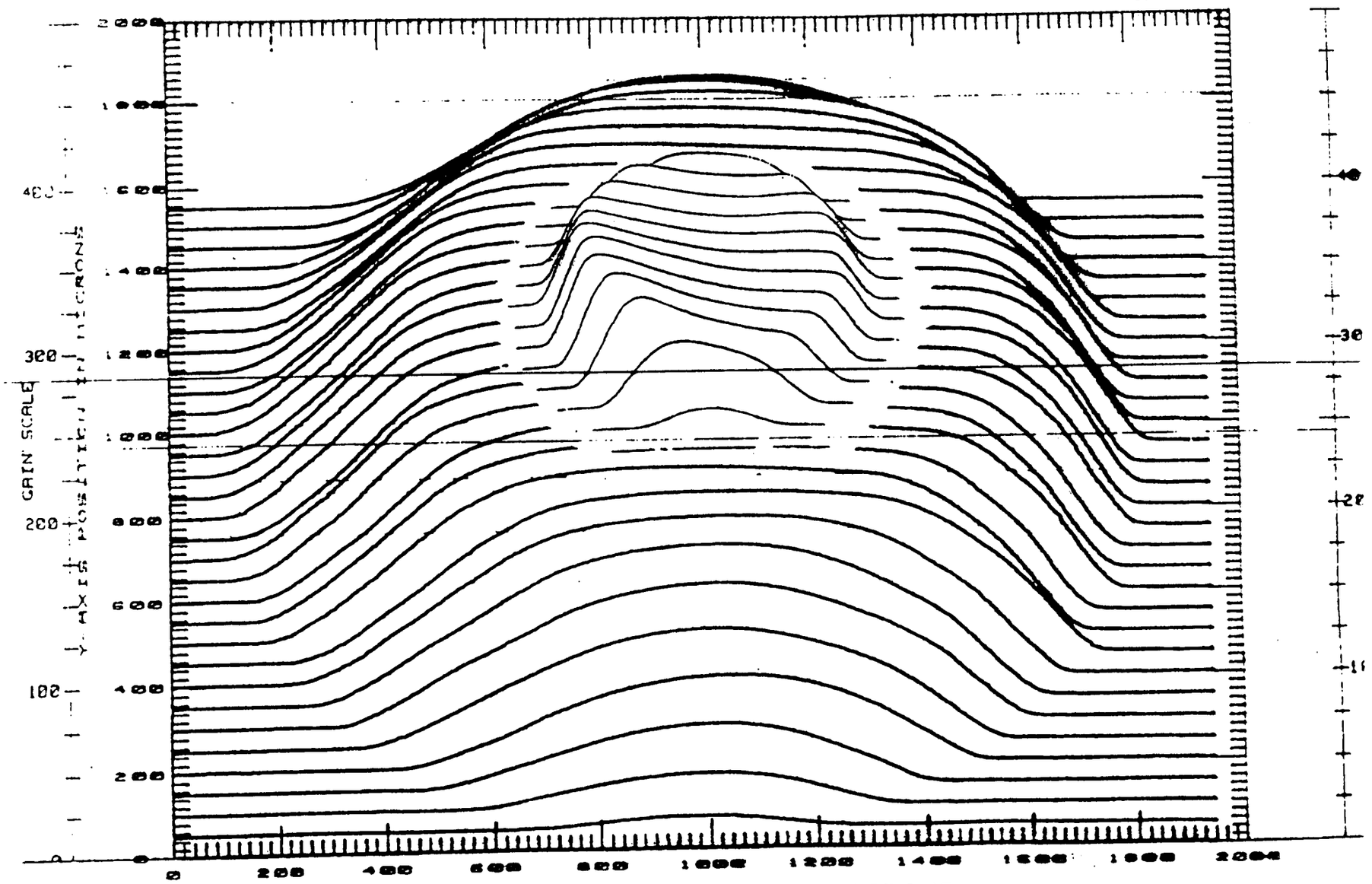
EG&G Bob McIntyre → Henri Dautet

Ball lens

#1-2
V-268-2V

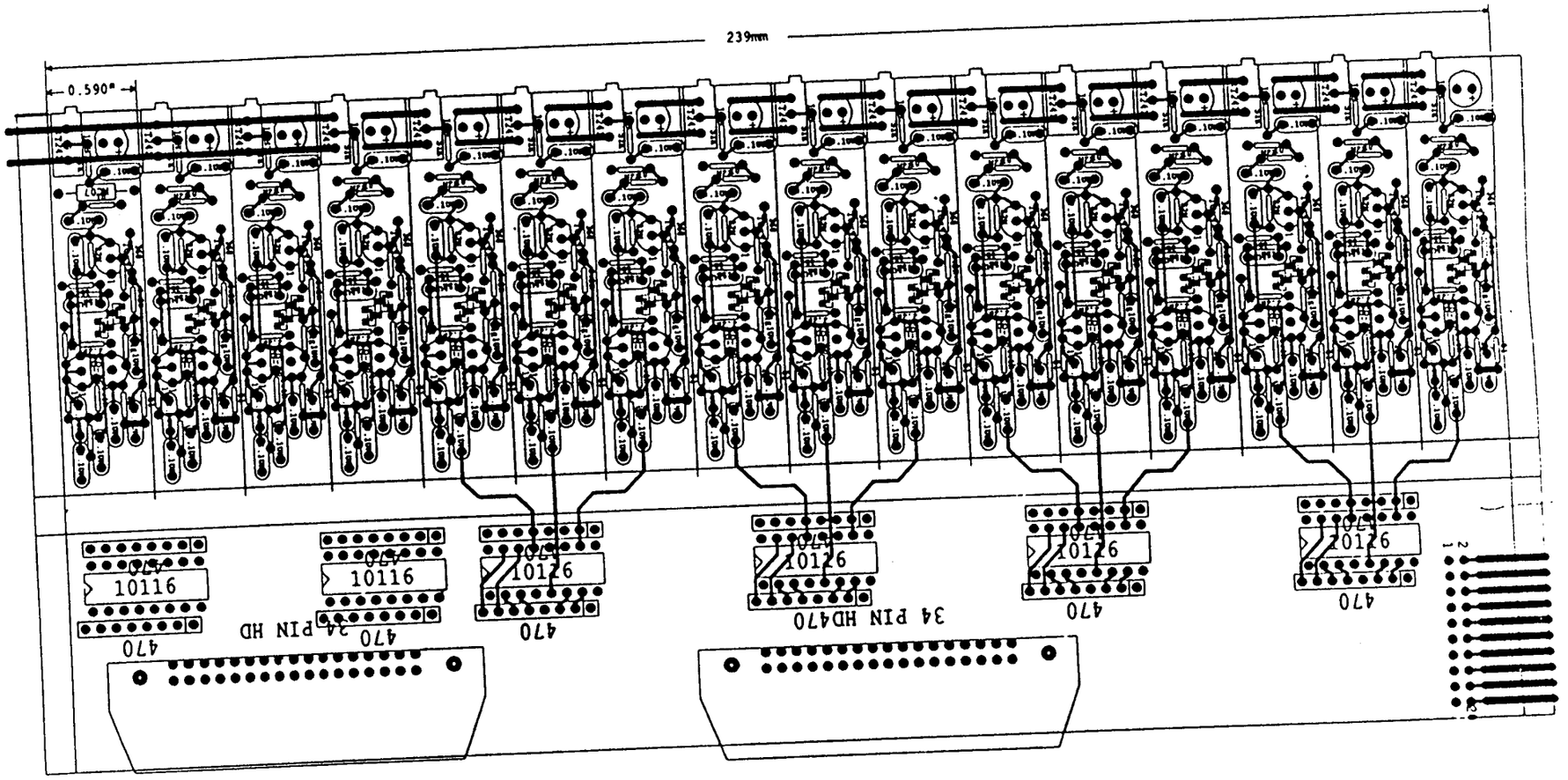
GAIN SCAN OF A SLIK W/LENS

TEST SLAVE: HeNe
WAVELENGTH: 632nm
17/04/91



7

APD Preamp from TSCL

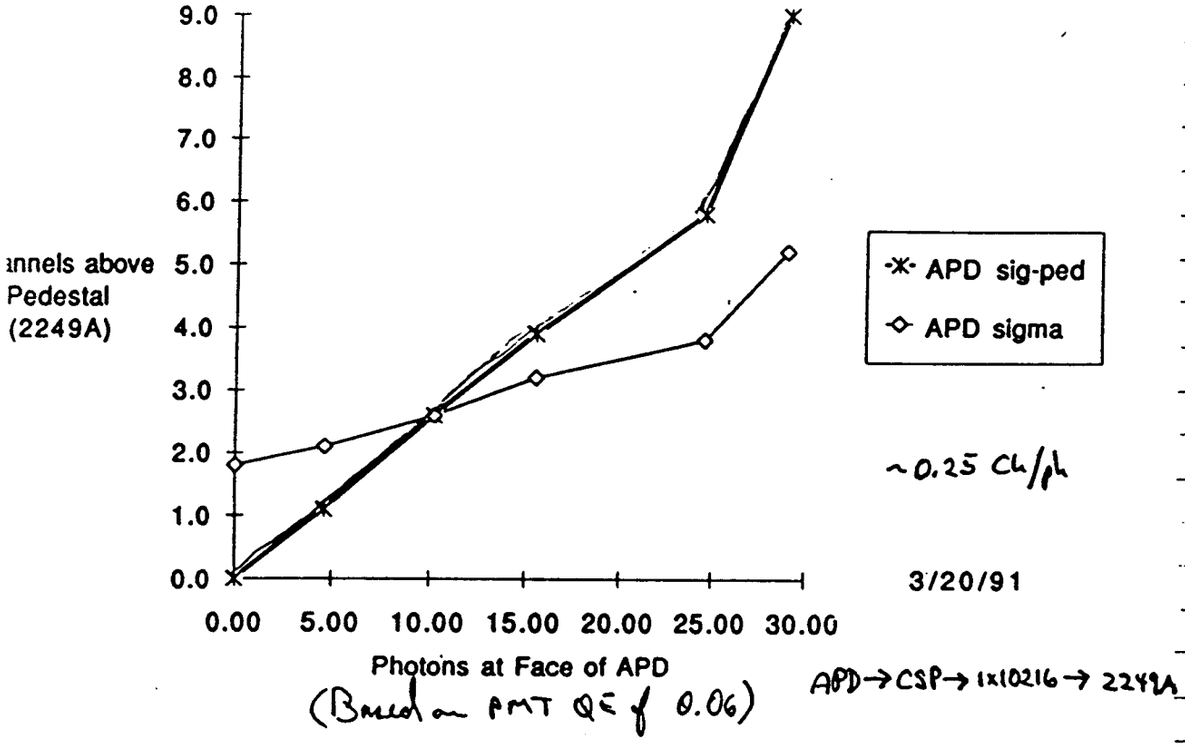


APD temperature control ±0.1 °C

FERMER
SSC LAB

Low Light Levels

500 µm APD Response to 550nm light from 500 µm Fiber



~0.25 ch/ph

3/20/91

(Based on PMT QE of 0.06)

APD → CSP → 1x10216 → 2249A

	# events	Vled	raction ped	<#pe>	<#photons>	APD signal	APD sig-pec	APD sigma
)0	1000	300	1.00	0.00	0.00	52.3	0.0	1.8
50	1004	350	0.76	0.28	4.64	53.4	1.1	2.1
73	1983	400	0.54	0.61	10.24	54.9	2.6	2.6
19	1062	450	0.39	0.93	15.50	56.2	3.9	3.2
)2	1322	500	0.23	1.48	24.61	58.1	5.8	3.8
39	13373	550	0.17	1.74	29.06	61.3	9.0	5.2

FUTURE R&D WORK

APD'S:

Overlapping interest with the tracking group, but tracker is a digital device and operates in Geiger mode, while we need a linear device.

R&D issues.

1) Gain is around 100. There is the expectation that stable gain around 200 or more can be achieved in linear mode with SLIK (super low k) devices.

2) Need to design package with an APD array and fast low-noise preamplifier on the same chip or hybrid.. Expect 16 - 24 APD's per package.

3) Temperature Stability.

Avantek

PIXEL TUBES:

Some times known as 'Hybrid' tubes or Silicon Intensified Target (SIT) tubes. This is a version of a multi-anode PM tube where the anode of the tube is a silicon target. Amplification is provided by stopping the accelerated photo-electron in the silicon, expect gains of order 2000. This type of device offers the possibilty of low-cost, high-channel 'SMART' phototubes.

R&D issues:

1) Cost estimate of volume production.
2) Design or find a diode array optimized for SDC.
3) Make prototype device.

MAPMT

Commercial devices exist from several companies. Need to investigate ways of reducing the cost per channel of these devices. Contacts with two vendors Phillips and Hamamatsu.

VLPC'S

Visible light photon counters. Operate at 6.6 K. They are a manufactured by Rockwell. Trackers say that they will cost about $20 per channel with a digital readout. We will investigate these devices for our choice of readout.

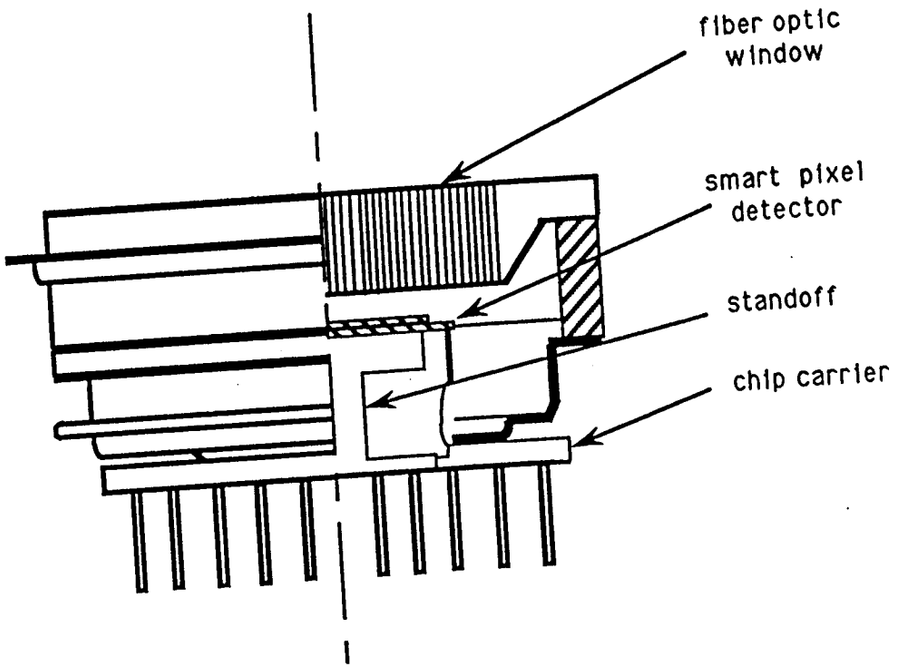
R&D issues:

1) Low temperature operation of a fast preamplifier, difficult enough in digital mode, more so in analog mode.

2) Dynamic range.

3) Cost per channel.

Silicon Intensified Target Tube



SIT tube
PIXEL tube

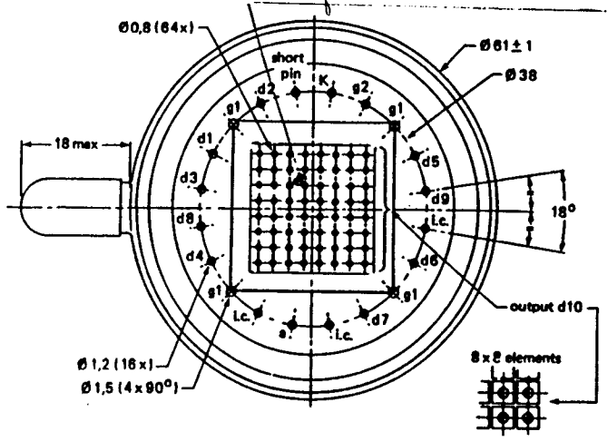
Pixel Tube Schematic.

MCPMT Philips XP 47/02 22

MECHANICAL DATA

Dimensions in mm

Surface sensible ~ 400 mm²



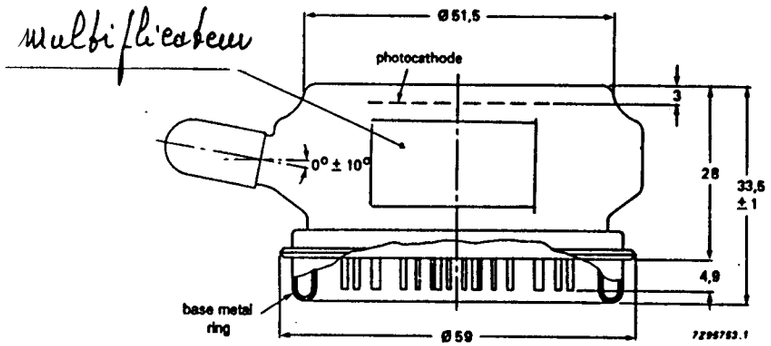


Fig.4 Mechanical outline.

encombrement

~ 3500 mm²

$R_g = \frac{ss}{\text{encombrement}}$ ~ 10 %

Que veut-on ?

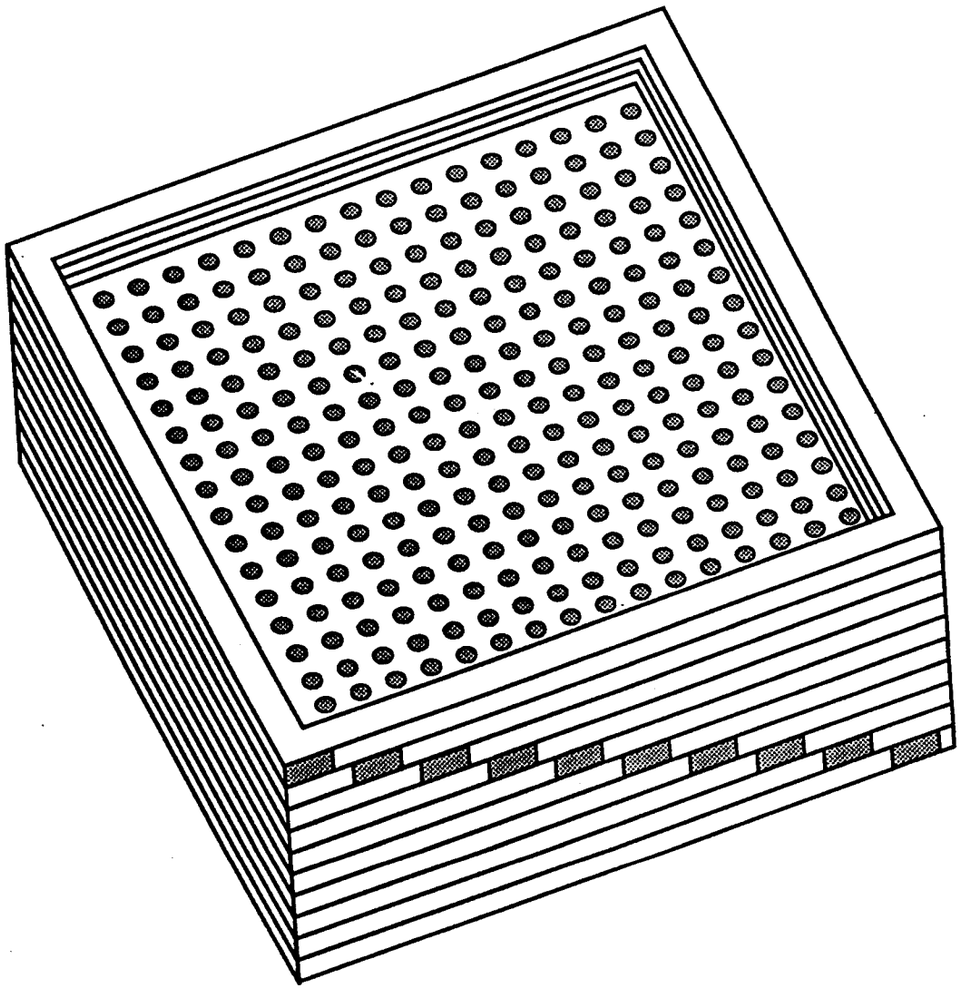
1. augmenter R_g → 80 / 90 %
2. supprimer le queusot
3. obtenir tube mosaïcable
4. simplifier connectique (HT, filaires)
5. Conserver cloisonnement multiplicateur
6. Obtenir tubes 256 voire 1024 voies
7. un prix modéré de la voie.

tout en conservant les performances robustesse

404

Compact PMT

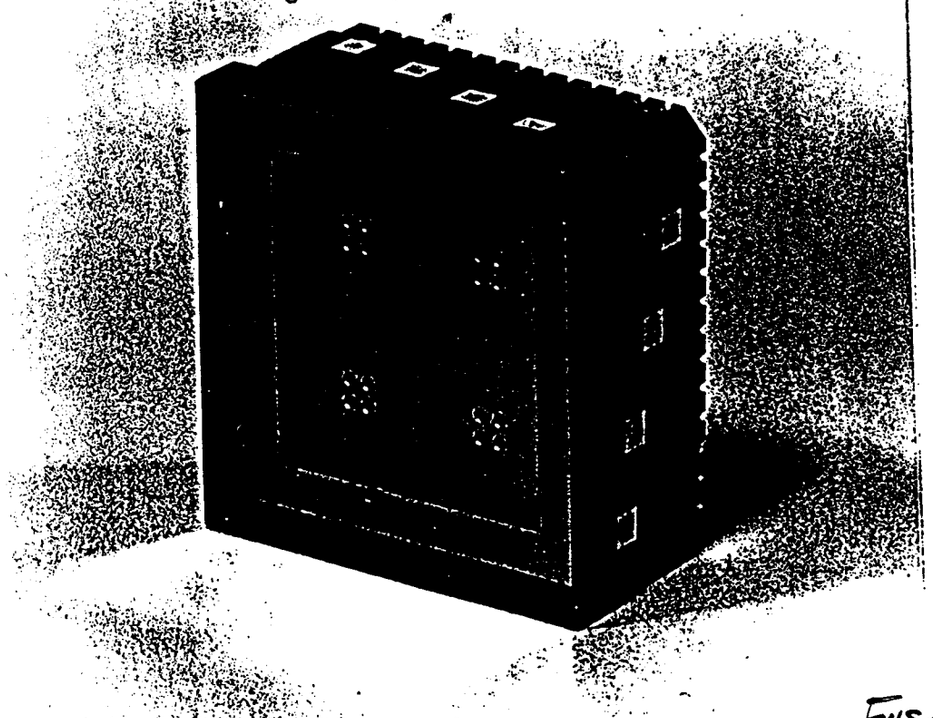
Georges Comby (Saclay)



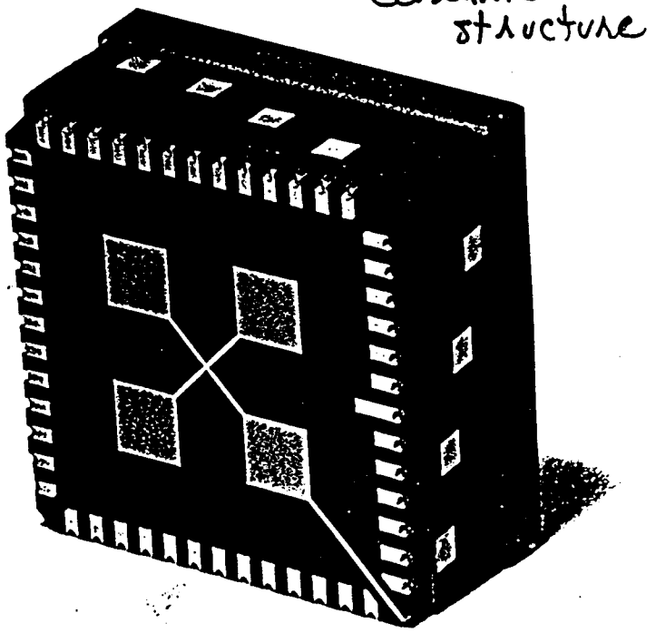
Compact PMT Electrical Contact

Georges Comby (Saclay)

Channels activated with Ag / MgO ?



Ceramic structure



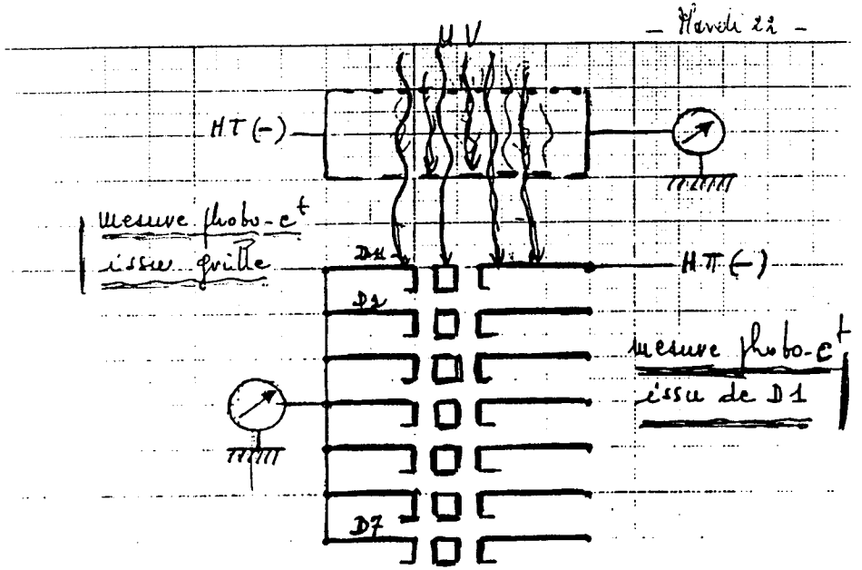
Cheap ?

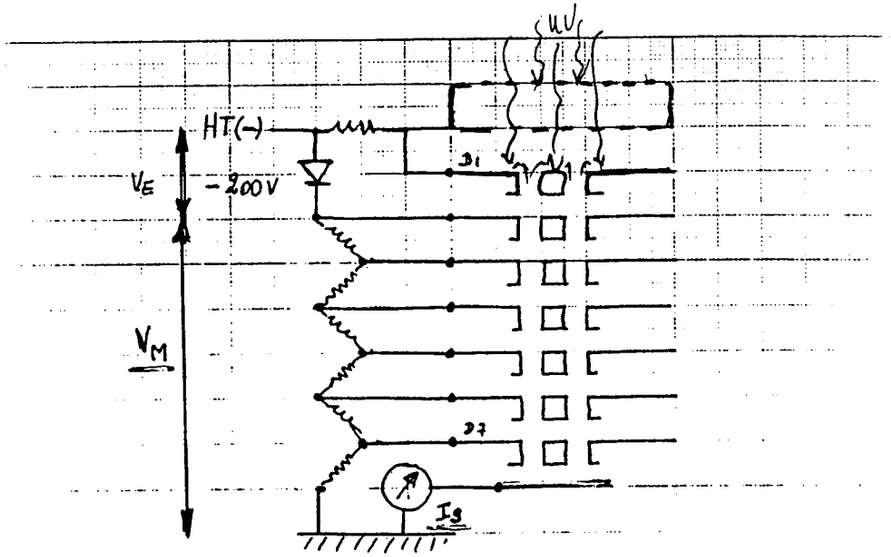
Fused optic fiber window ϕ 55 μm

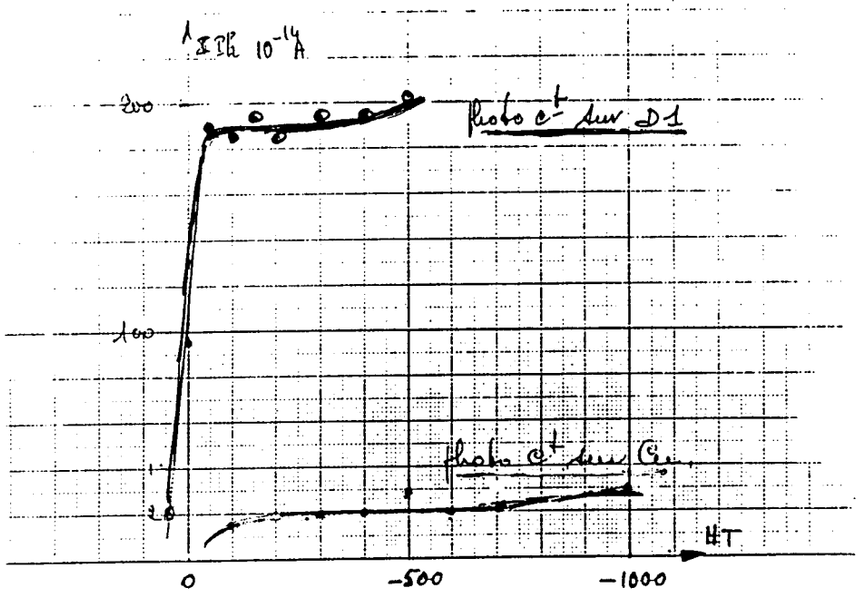
Ga / In solder

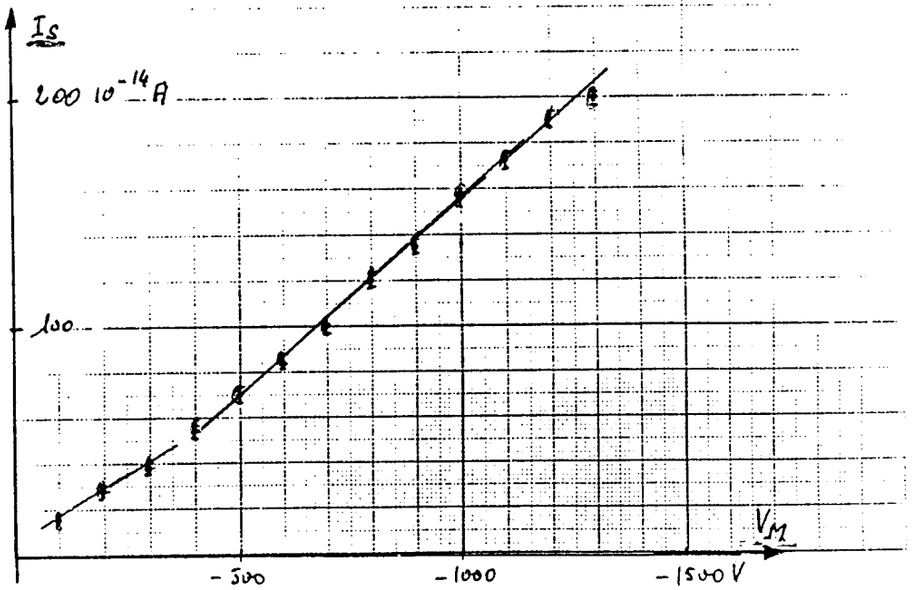
Compact [illegible]

– Mardi 22 –









TMC

H. Williams

TMC and Data Acquisition/Packaging

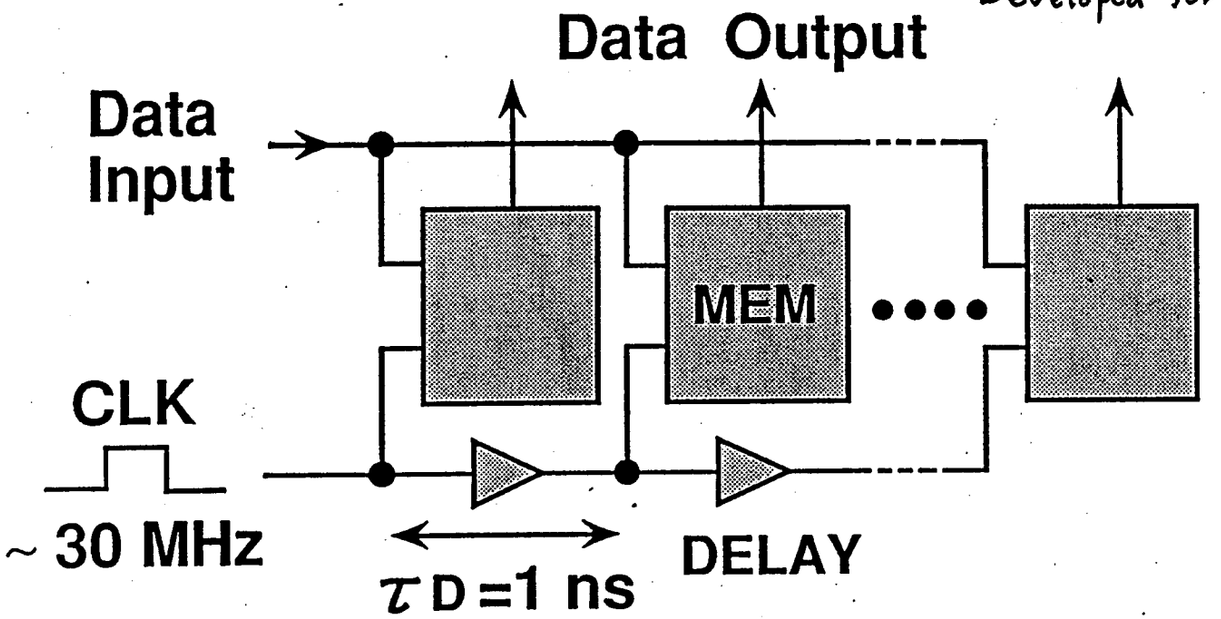
1991.5.14 Yasuo Arai (KEK)

1. Status of TMC chip Development
2. Straw Tube Measurement with TMC
3. Short/Long Range Plan
4. DA Scheme and Packaging

[Advertisement]

What is a Time Memory Cell (TMC) ?

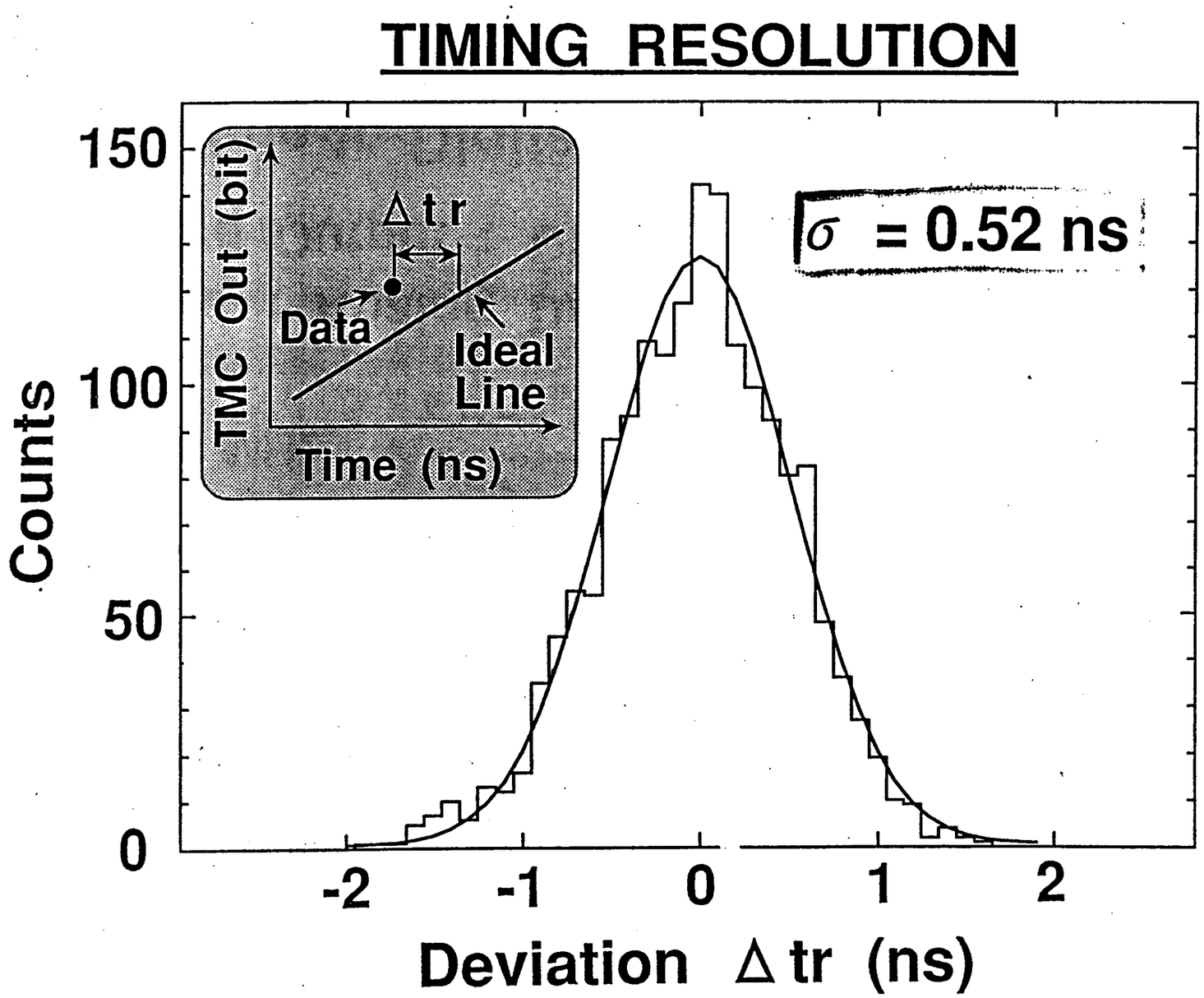
Developed for Straw Chamber

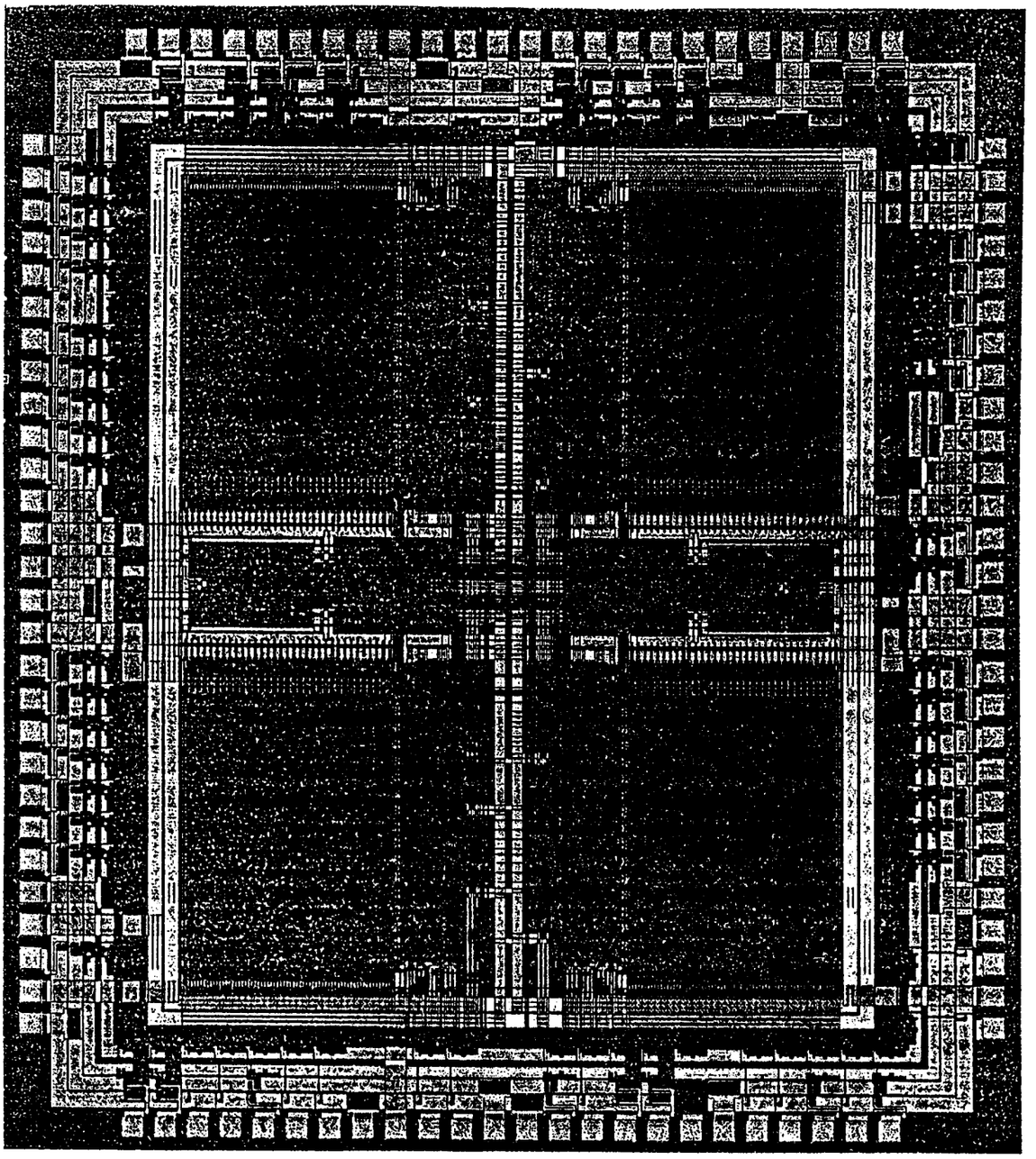


- ○ Input : Analog Data of Timing Information
- ○ Store /Output : Digital Data as Bit Position

⇨ **Time-to-Digital Converter**

Multi Hit


TIMING RESOLUTION
150
100
50
0
Counts
TMC Out (bit)
Δtr
Data
Ideal
Line
Time (ns)
σ = 0.52 ns
-2
-1
0
1
2
Deviation Δtr (ns)

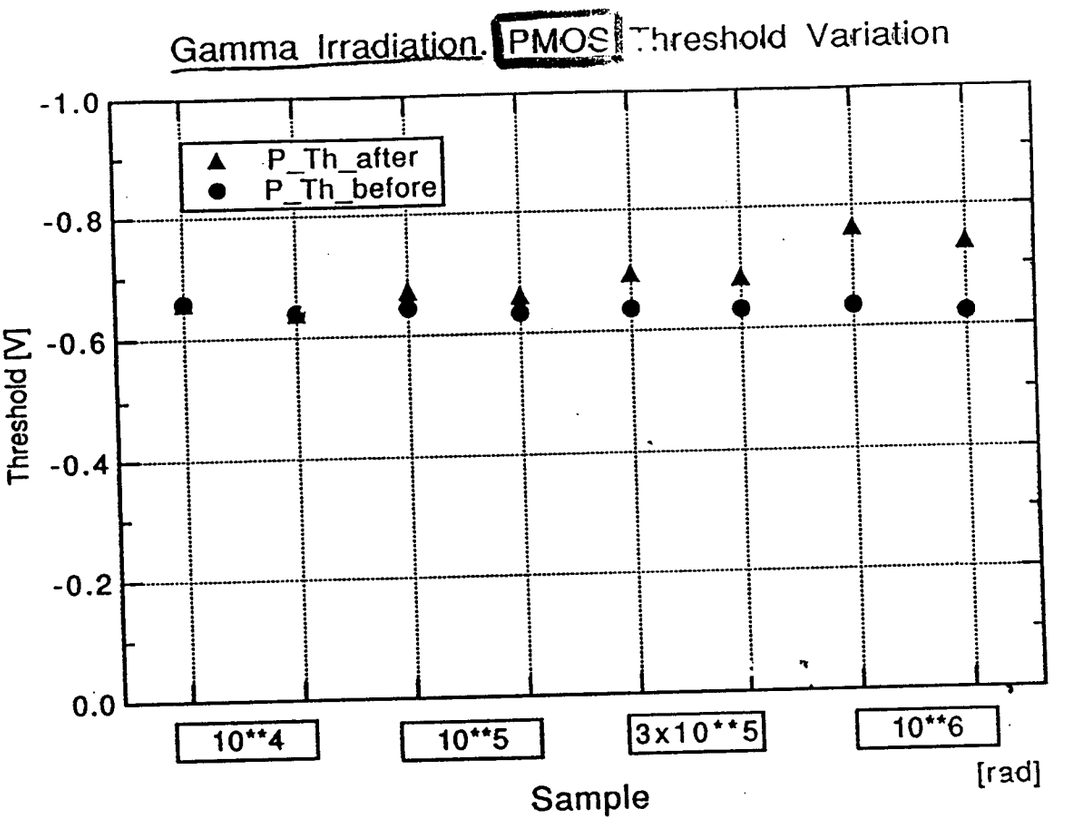


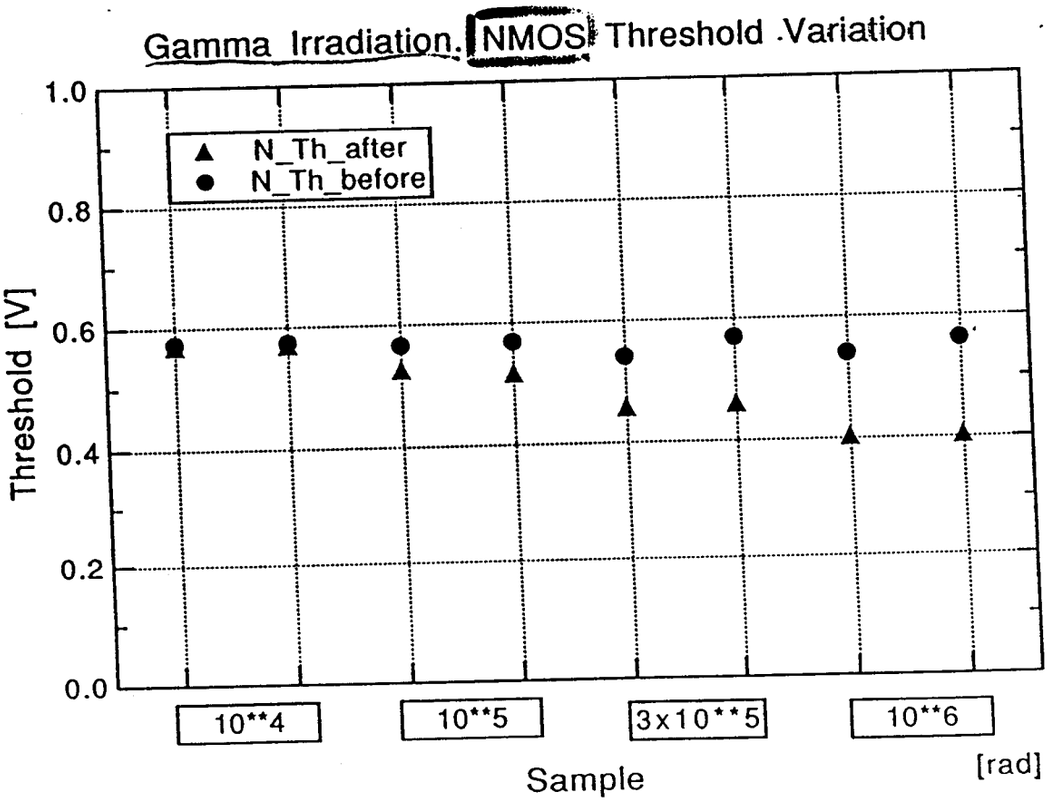
TMC1164

MAIN FEATURES

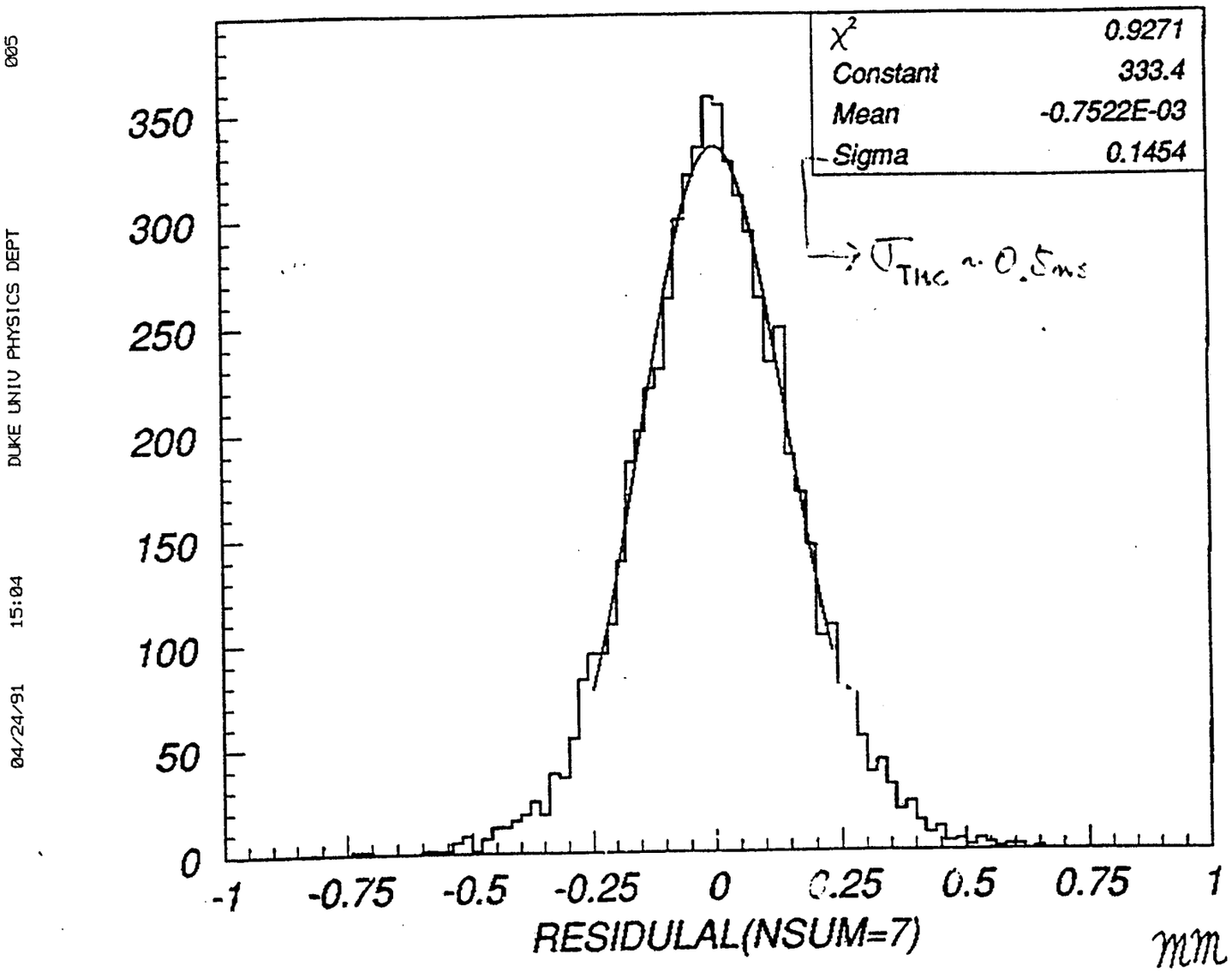
Organization	4 ch $\times$ 1 Kb
Process	0.8 μm N-well CMOS
Least Time Count	1 ns / bit
Timing Resolution	σ = 0.52 ns
Supply Voltage	3 V
Active Power	7 mW / ch (@ 1 % readout duty)
Data Output	32 ns cycle, 2 stage pipeline
Chip Size	5 $\times$ 5.6 mm^2

Threshold Variation (No Power)





TMC


χ² 0.9271
Constant 333.4
Mean -0.7522E-03
Sigma 0.1454
σ_TMC ~ 0.5mm
350
300
250
200
150
100
50
0
-1
-0.75
-0.5
-0.25
0
0.25
0.5
0.75
1
RESIDULAL(NSUM=7)
mm
005
DUKE UNIV PHYSICS DEPT
04/24/91
15:04

Short/Long range Schedule of TMC

FY91 Radiation Damage Test
Start Final Version Design

FY92 Layout Design

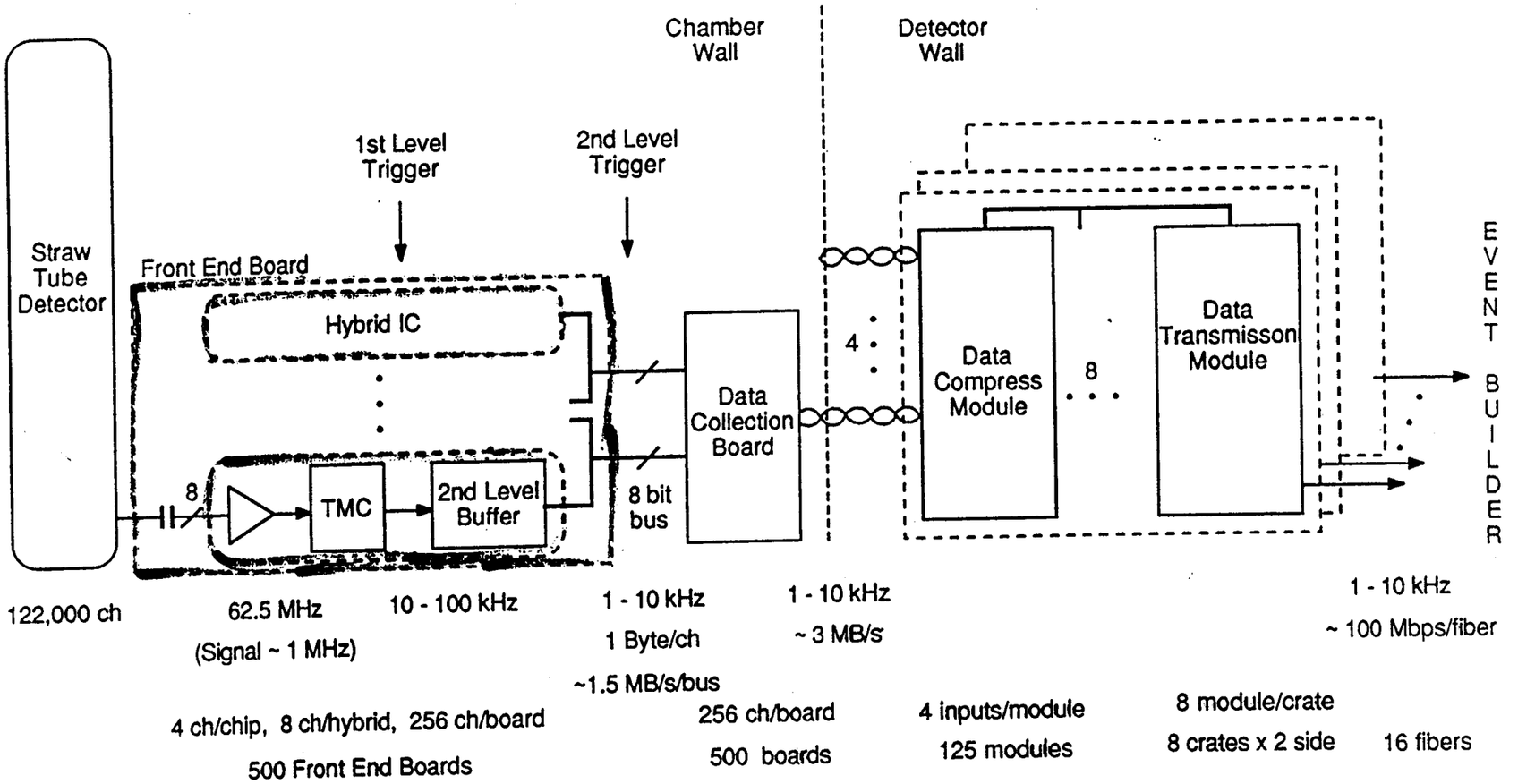
FY93 Chip Test, Modification

FY94 Design of Mass-Production Chip

FY95-96 Mass Production

[Meeting with NEL]

- No problem for 200k channel production at NEL.
- We can use 0.5 μm CMOS process at mass production time if it is cost effective.
- They can provide ~~(Gate Array)~~/Standard Cell which use same process as the TMC (same radiation-hardness). This can be used for Second-level Buffer, DCC etc.
- They can also make hi-density hybrid chips. There are many packaging technology, but hi-density packaging is expensive.



Data Flow Diagram of the Straw Tube Readout

91.5.12 Y.Arai

Summary

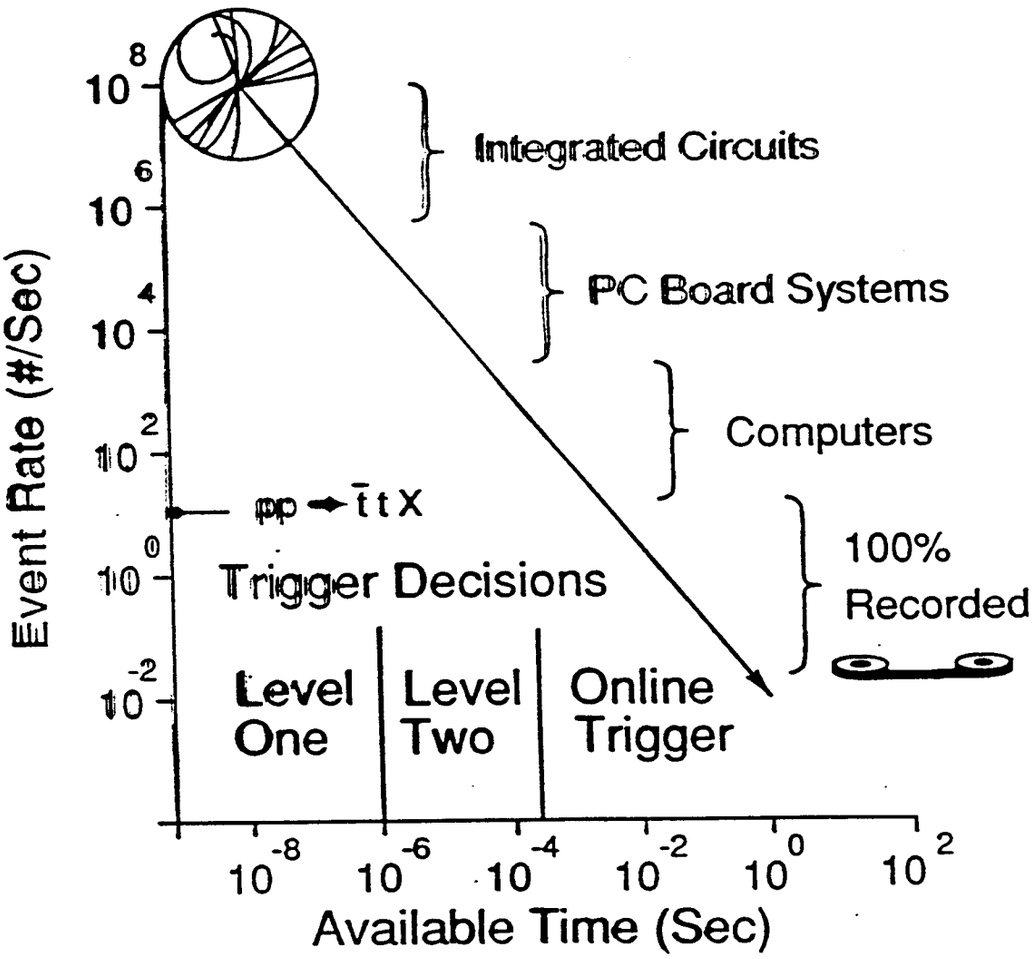
- TMC has worked with 4mm Straw Tube at Duke Univ.
- We would like to start final design of TMC. We need to fix the length of first level buffer.
- We also start to research packaging issue.

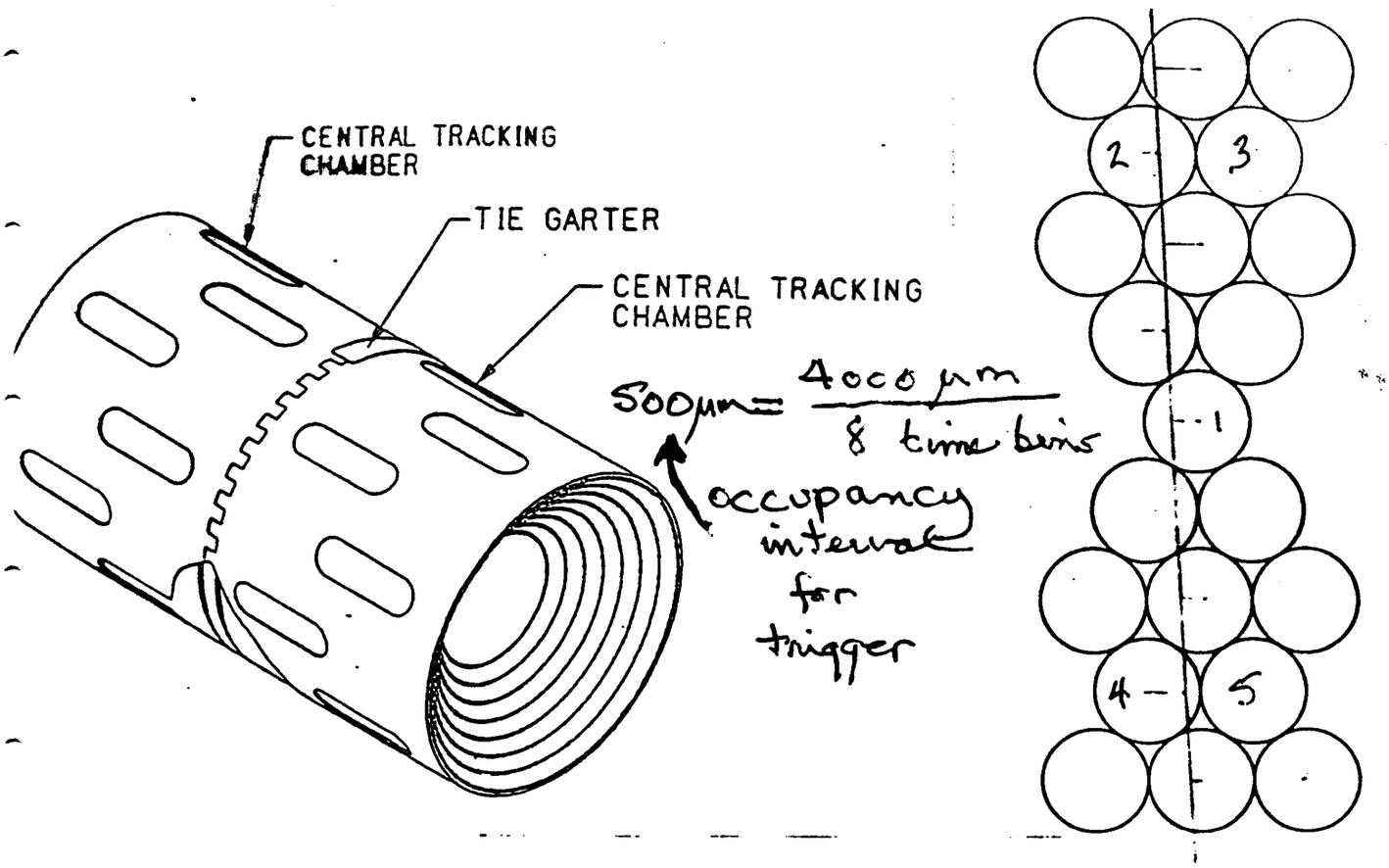
Muon Chamber Readout & Triggering

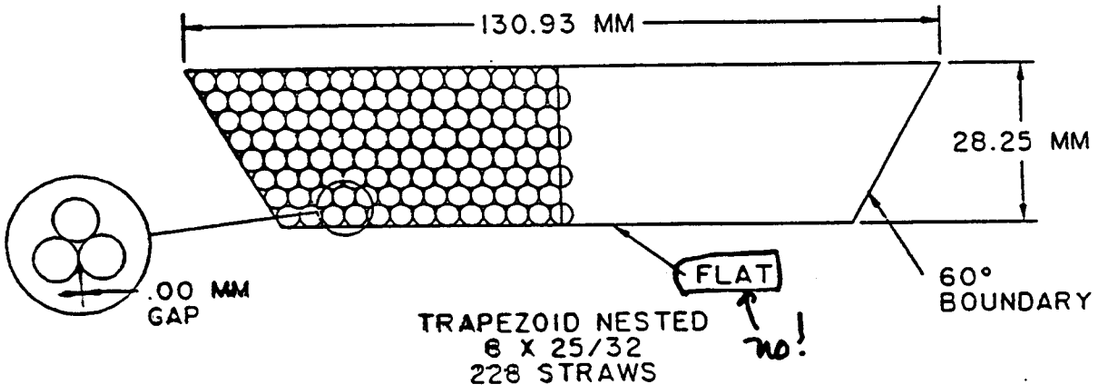
J. Chapman

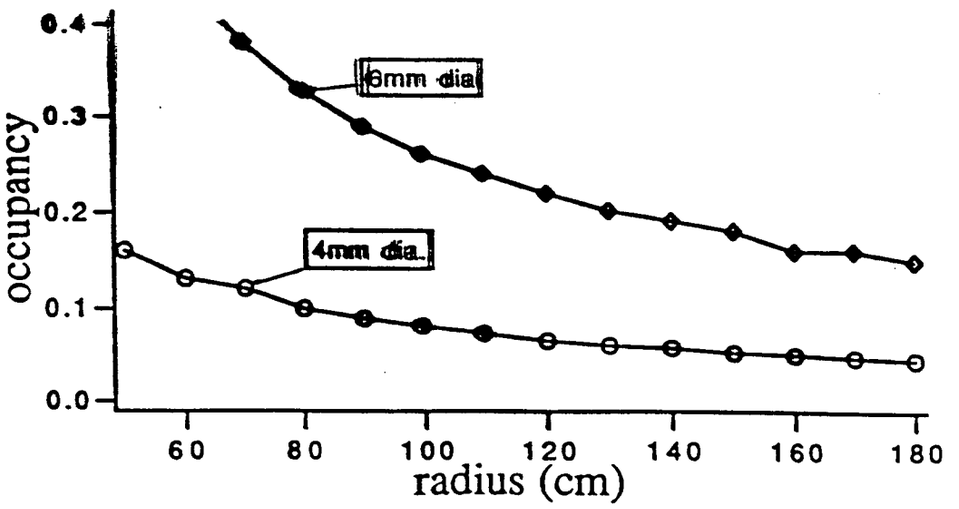
Central Tracking Triggers

J. Chapman

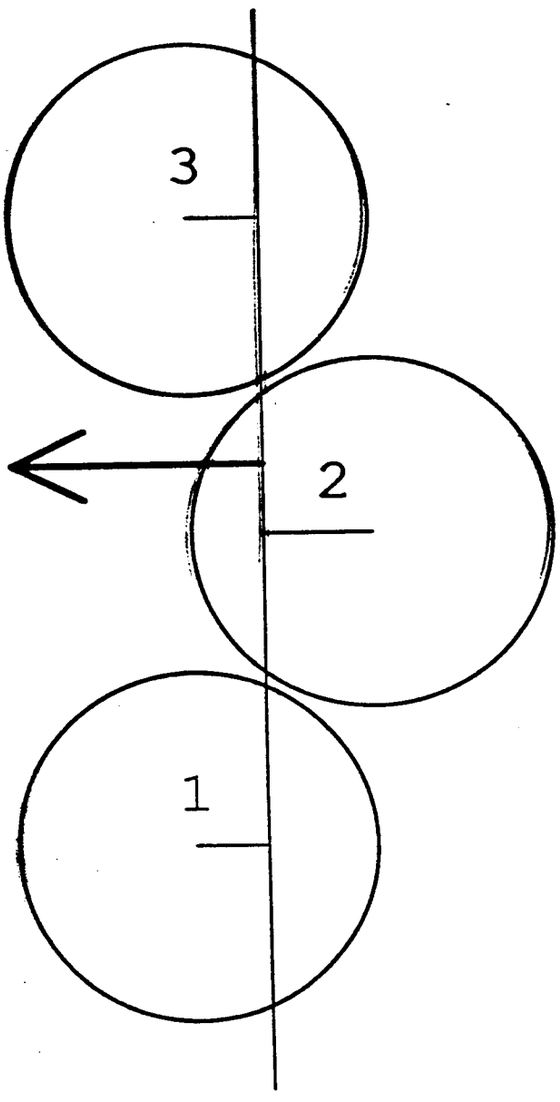



CENTRAL TRACKING CHAMBER
TIE GARTER
CENTRAL TRACKING CHAMBER
500μm = 4000 μm / 8 time bins
occupancy interval for trigger
2
3
1
4
5

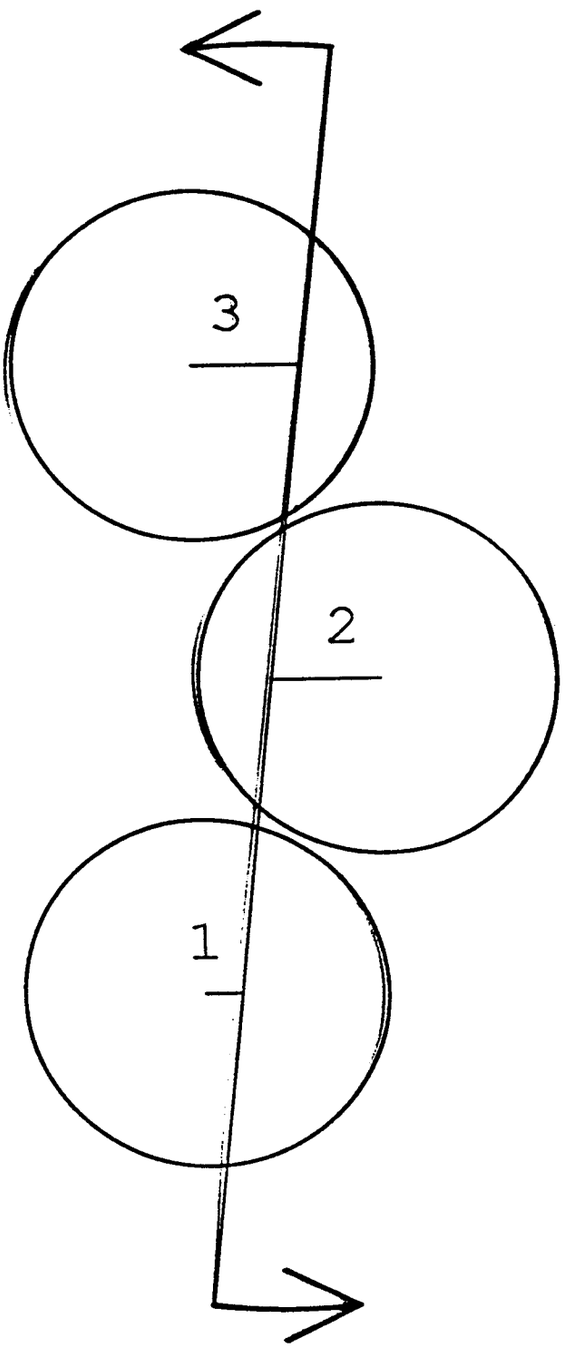

130.93 MM
28.25 MM
.00 MM GAP
FLAT
60° BOUNDARY
TRAPEZOID NESTED
6 X 25/32
228 STRAWS
no!


0.4
0.3
0.2
0.1
0.0
occupancy
6mm dia
4mm dia
60
80
100
120
140
160
180
radius (cm)

Test 1

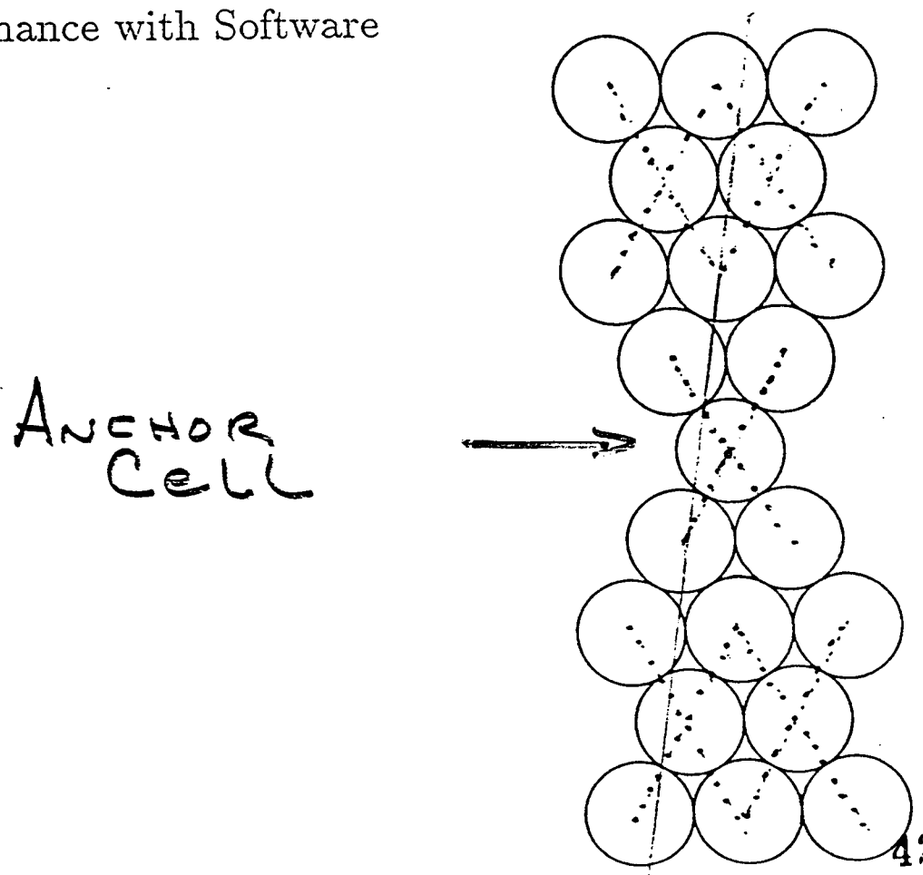


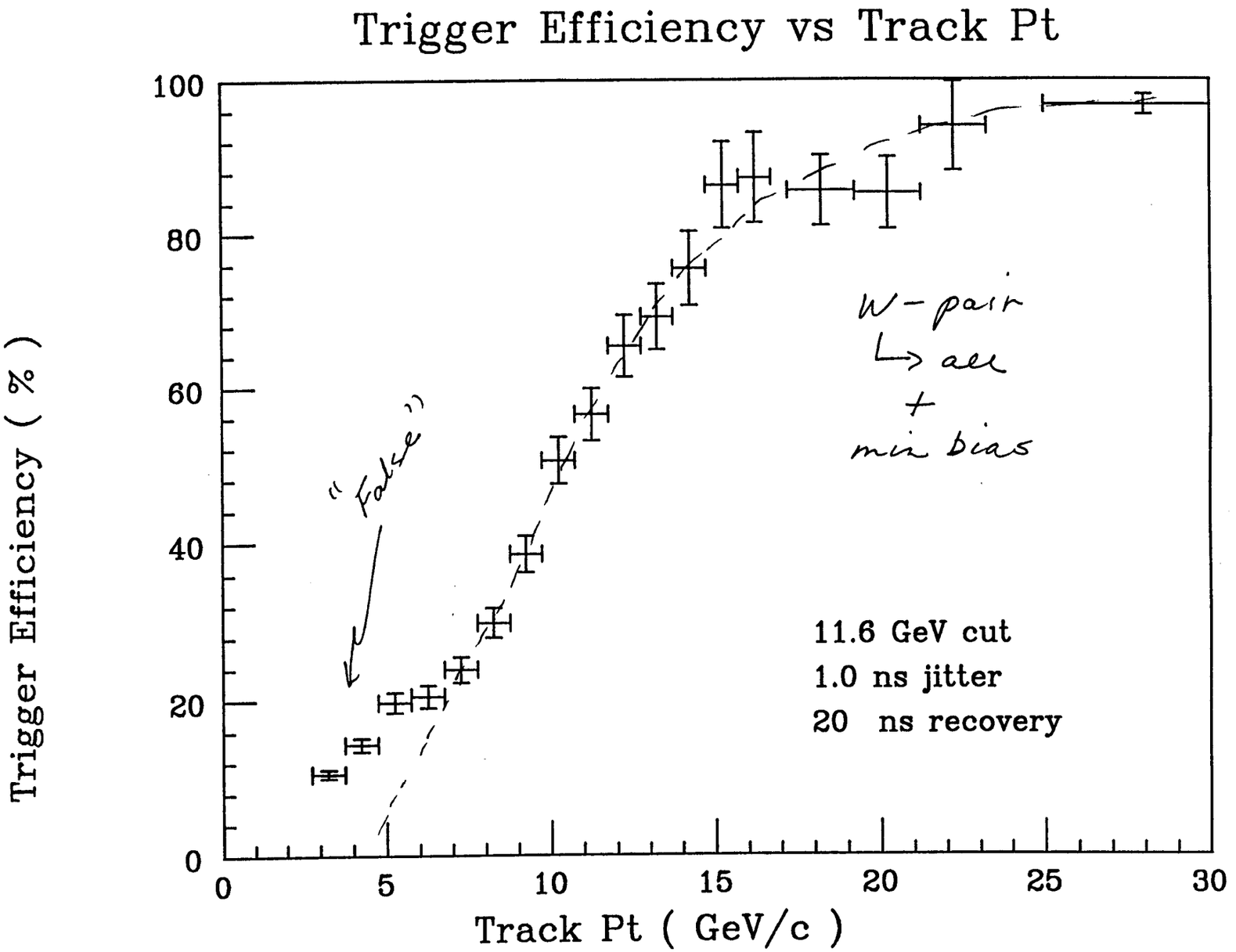
Test 2

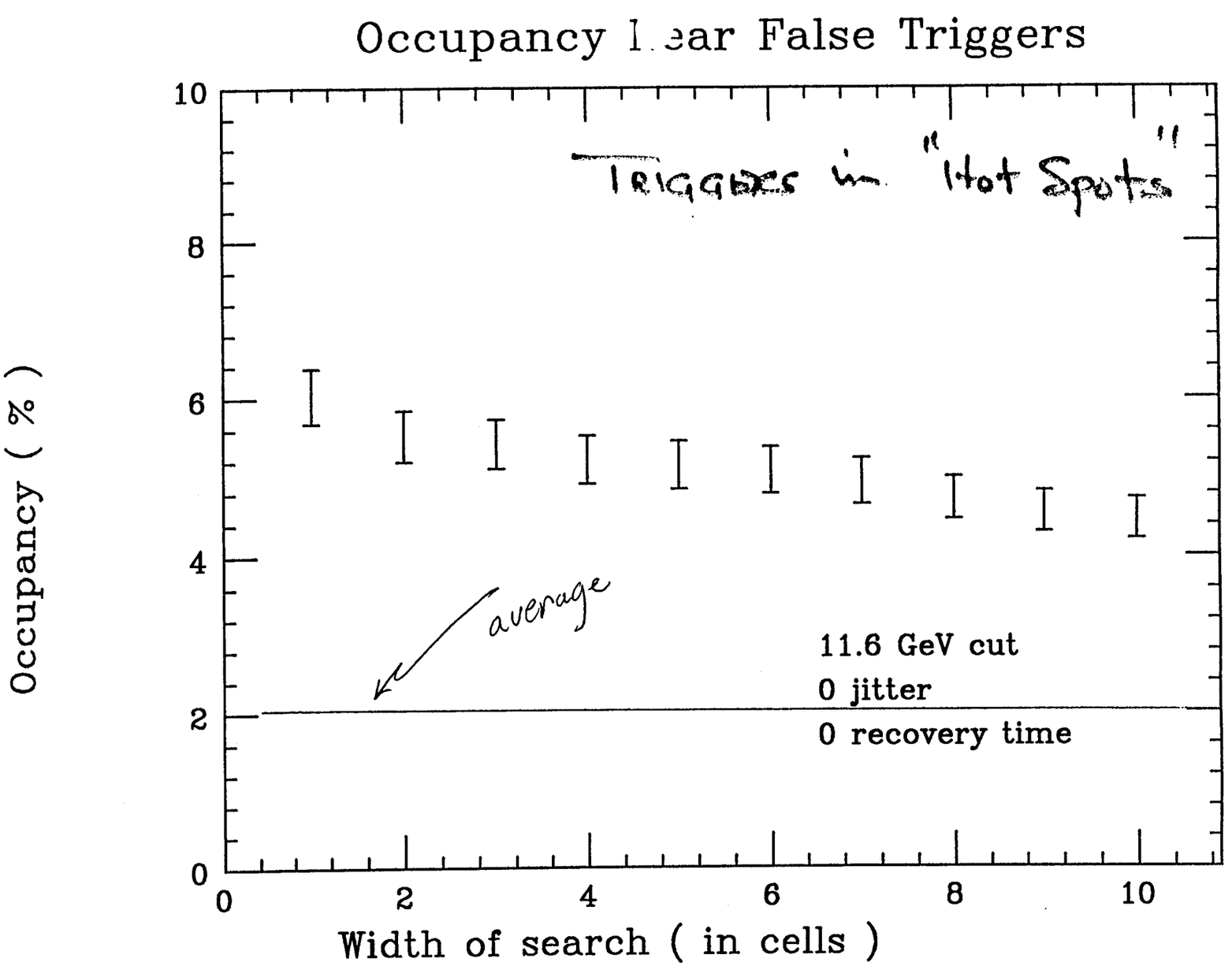


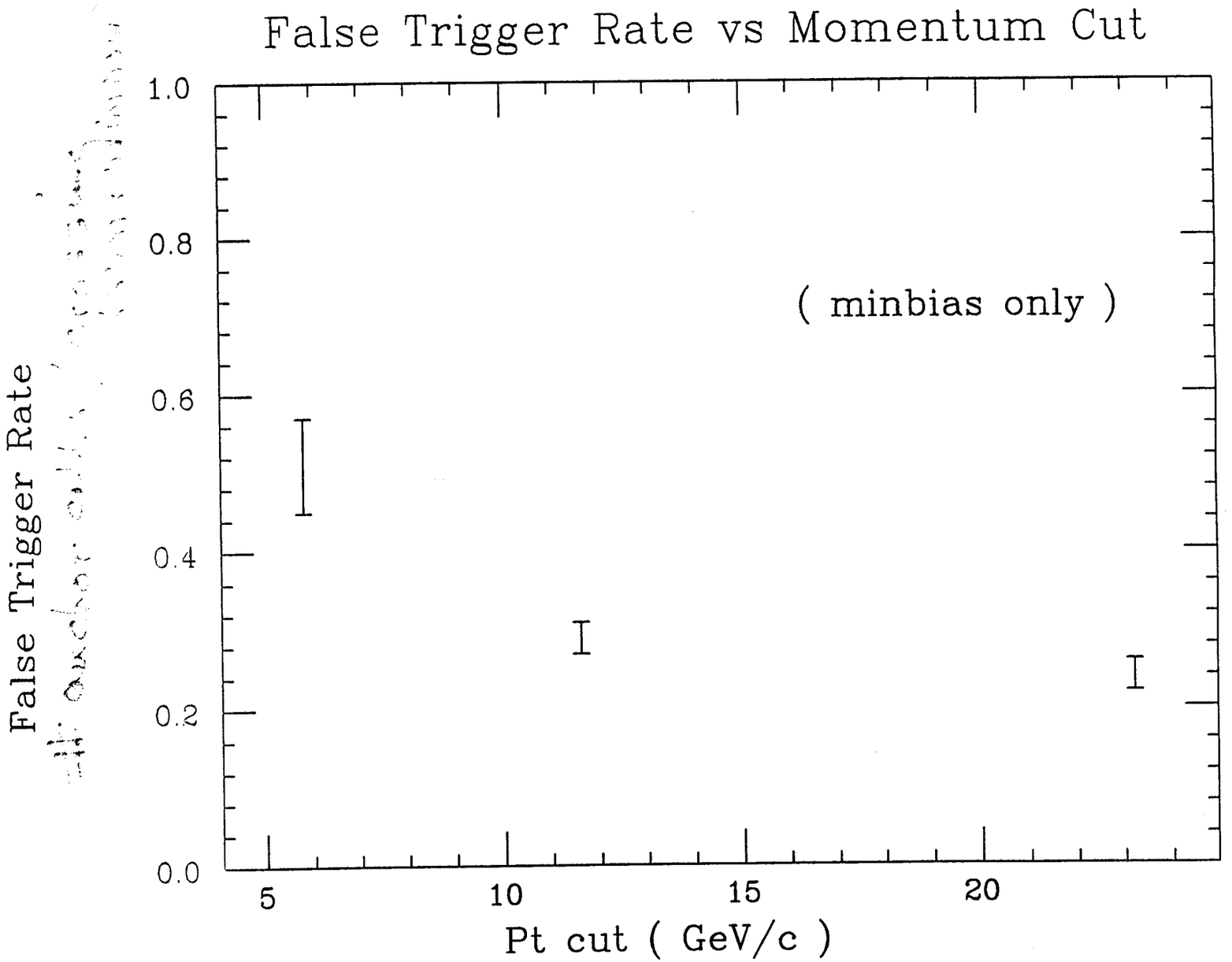
Proposed SDC Tracking Trigger Pattern

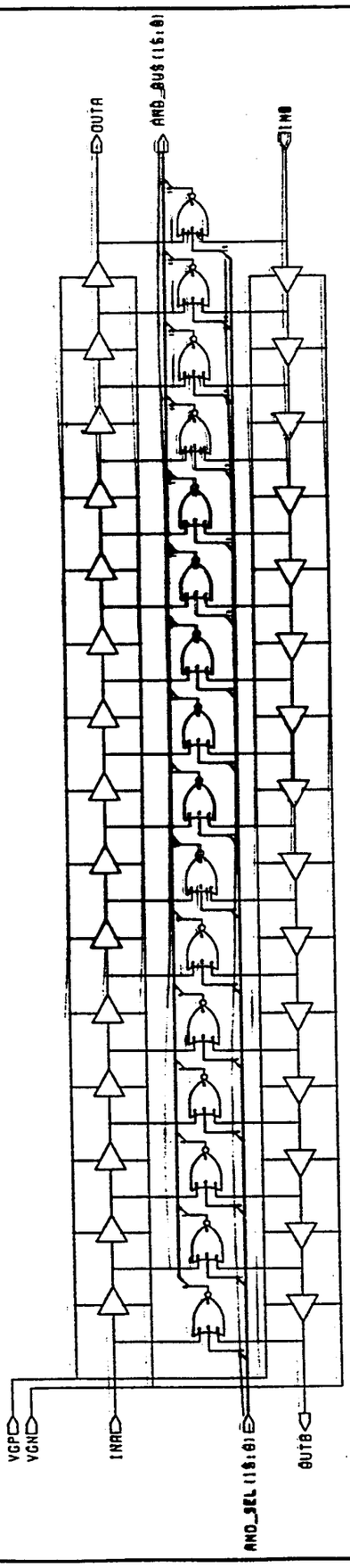
- Based on a 21 Tube Pattern
- Anchored on the Center Cell
- Composed of 10 Synchronizers
- Require a Minimum Track Momentum (Angle)
- Logic:
  - AND all "Good" Patterns of 2 Synchronizers
  - OR of all "Good" Pattern ANDs
- Extract Signal for Each Anchor Cell
- Combine with Calorimeter and Muon Trigger
- Simulate Performance with Software

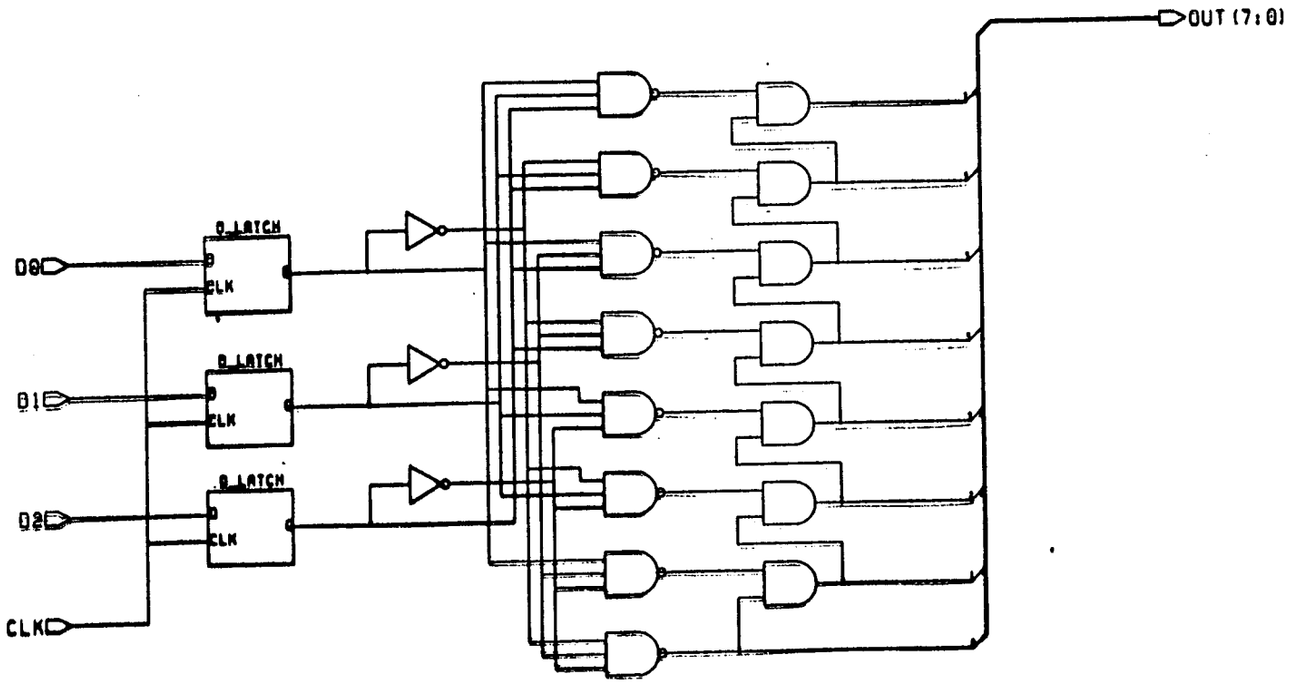


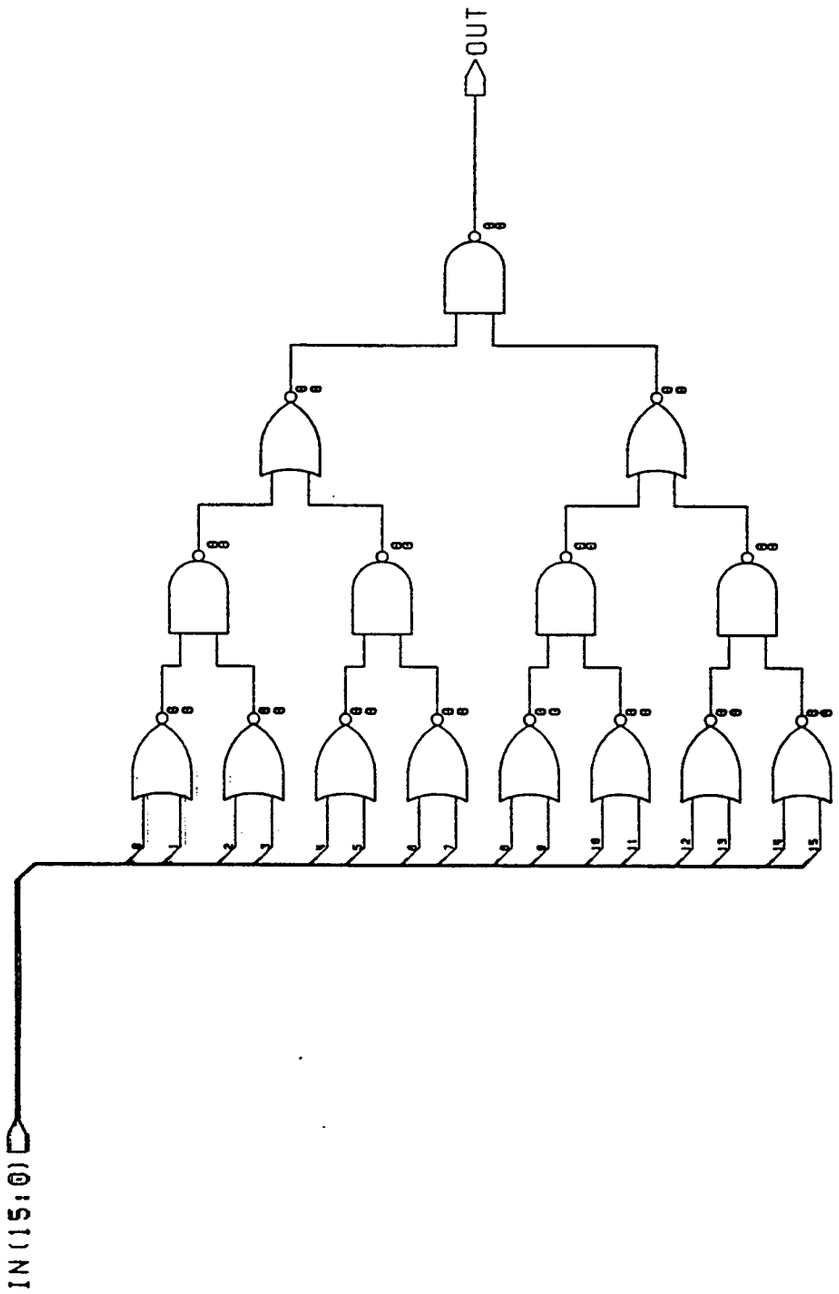

Trigger Efficiency vs Track Pt
Trigger Efficiency (%)
Track Pt (GeV/c)
0
20
40
60
80
100
0
5
10
15
20
25
30
"Fake"
W-pair
↳ all
+
min bias
11.6 GeV cut
1.0 ns jitter
20 ns recovery

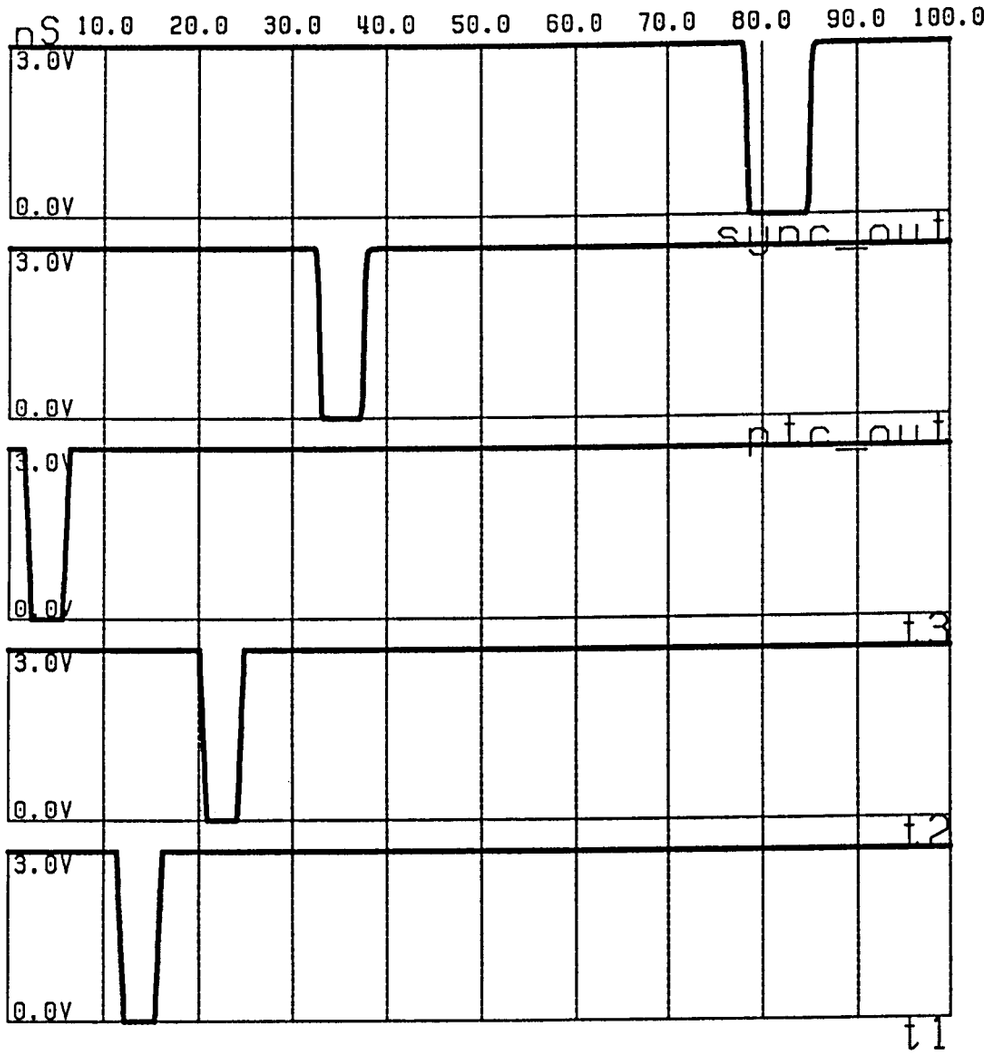

Occupancy Near False Triggers
Triggers in "Hot Spots"
Occupancy (%)
Width of search (in cells)
average
11.6 GeV cut
0 jitter
0 recovery time
0
2
4
6
8
10


False Trigger Rate vs Momentum Cut
False Trigger Rate
1.0
0.8
0.6
0.4
0.2
0.0
5
10
15
20
Pt cut (GeV/c)
(minbias only)


OUTA
AND_BUS[15:0]
INB
VGP
VGN
INA
AND_SEL[15:0]
OUTB


OUT (7:0)
D0
D1
D2
CLK
D_LATCH
D
CLK
D_LATCH
D
CLK
D_LATCH
D
CLK


OUT
IN(15:0)

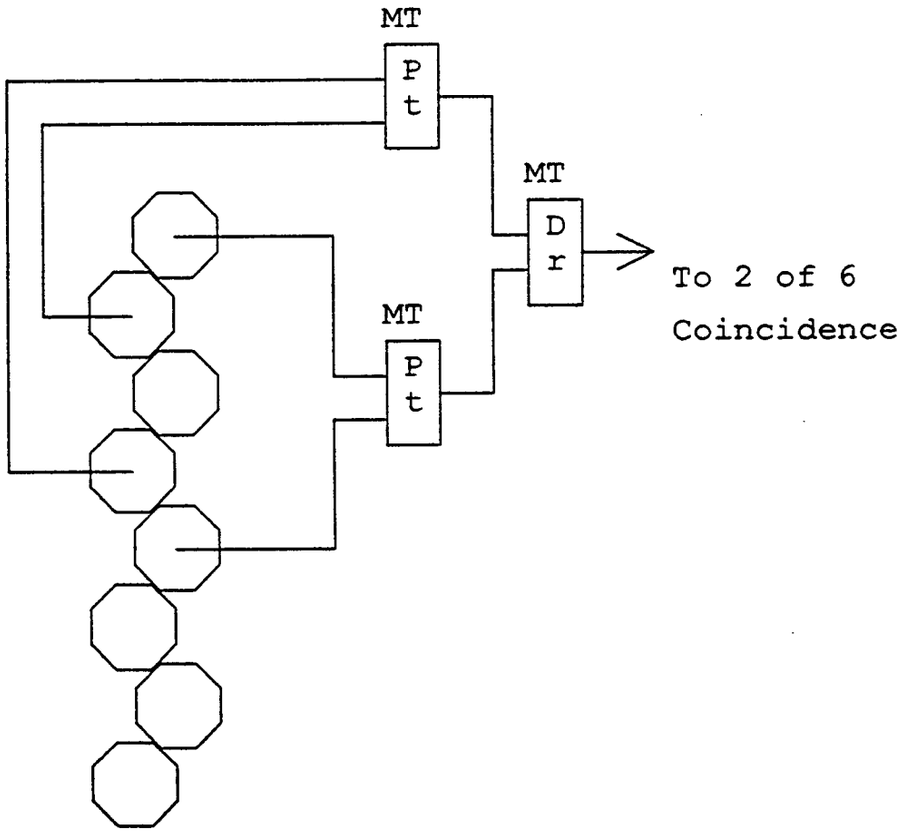


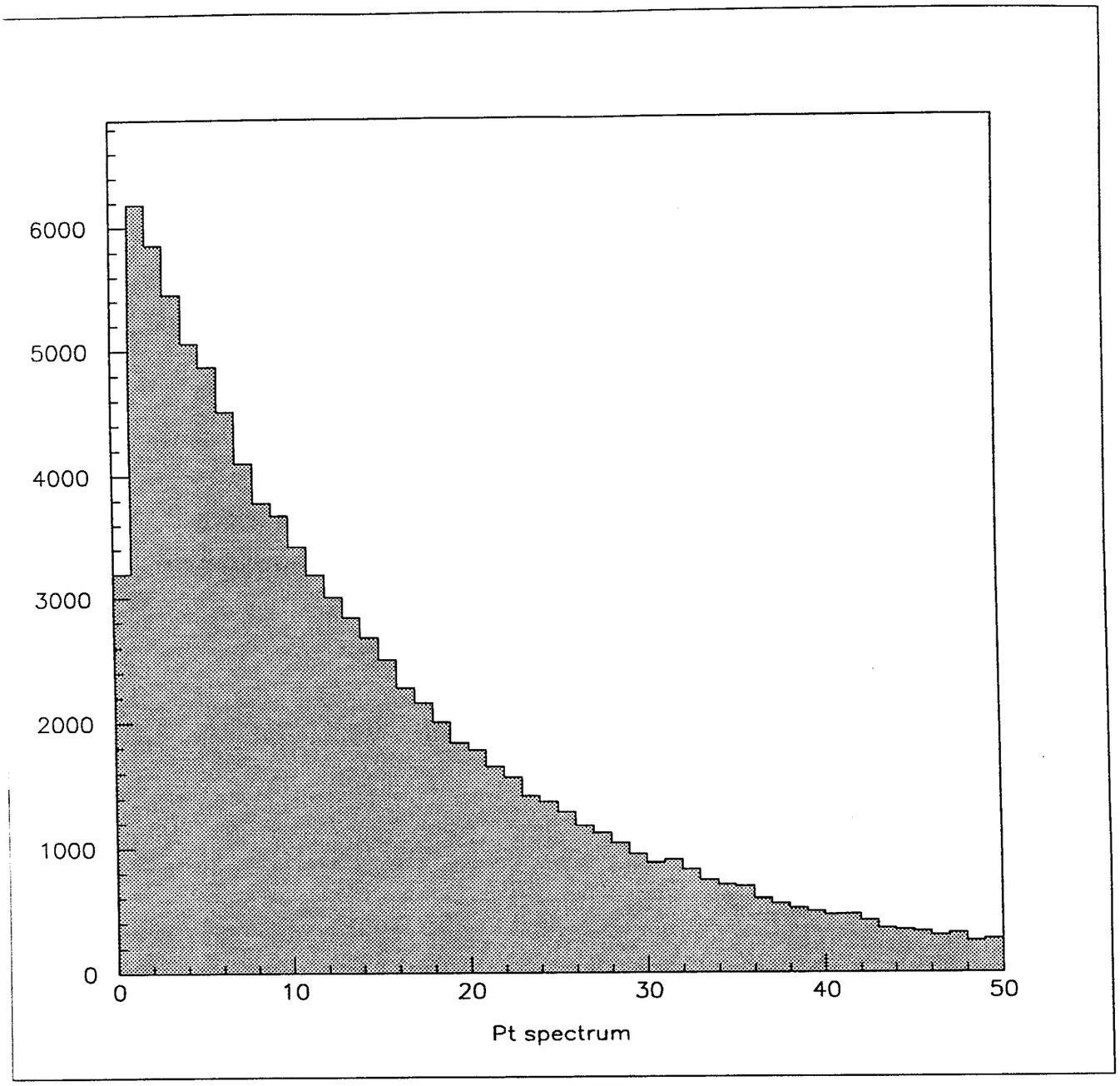
$\Delta t = 98$ nSEC.

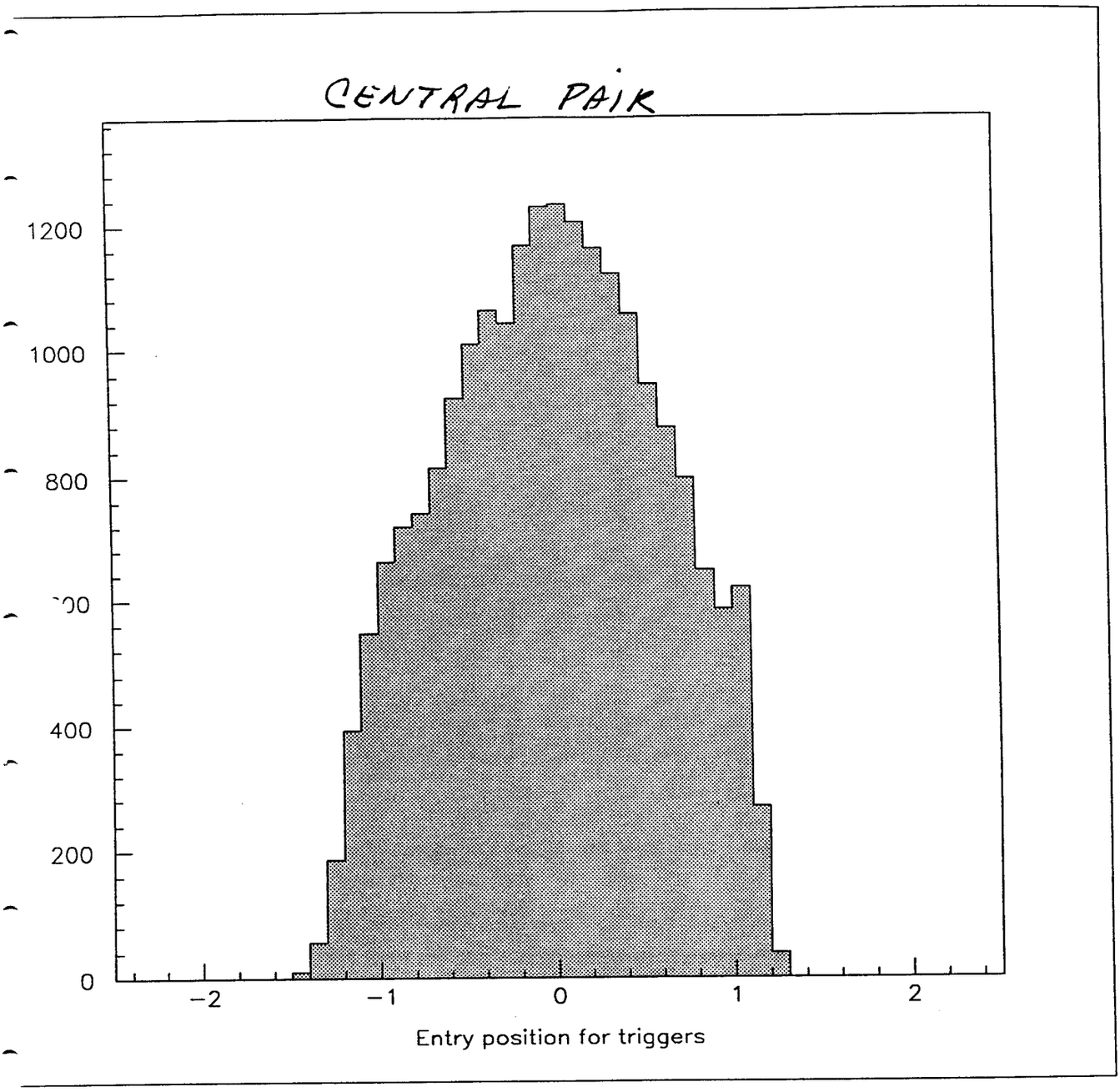
RUN #6 ⇒ PASSES

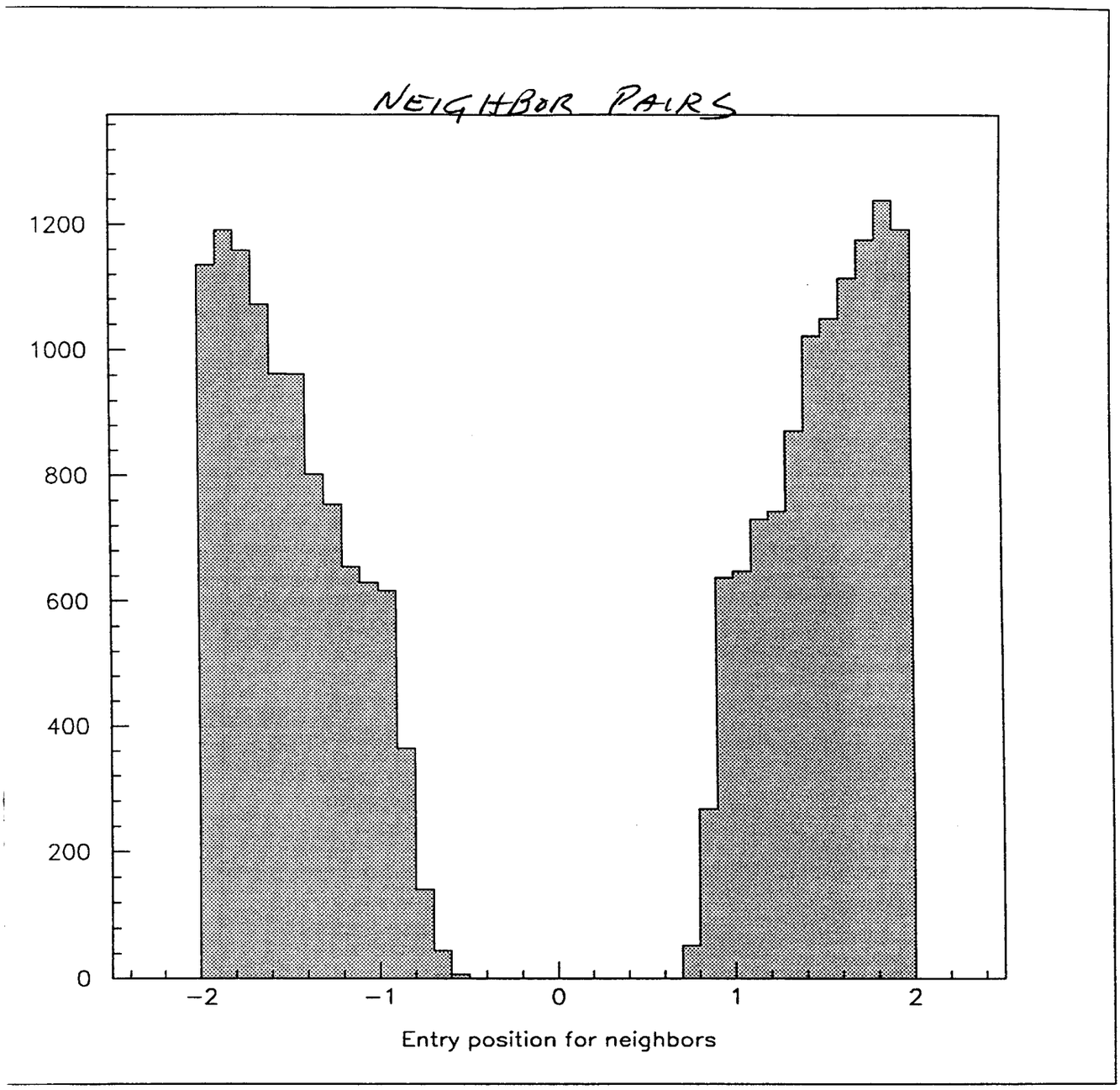
"NEW"

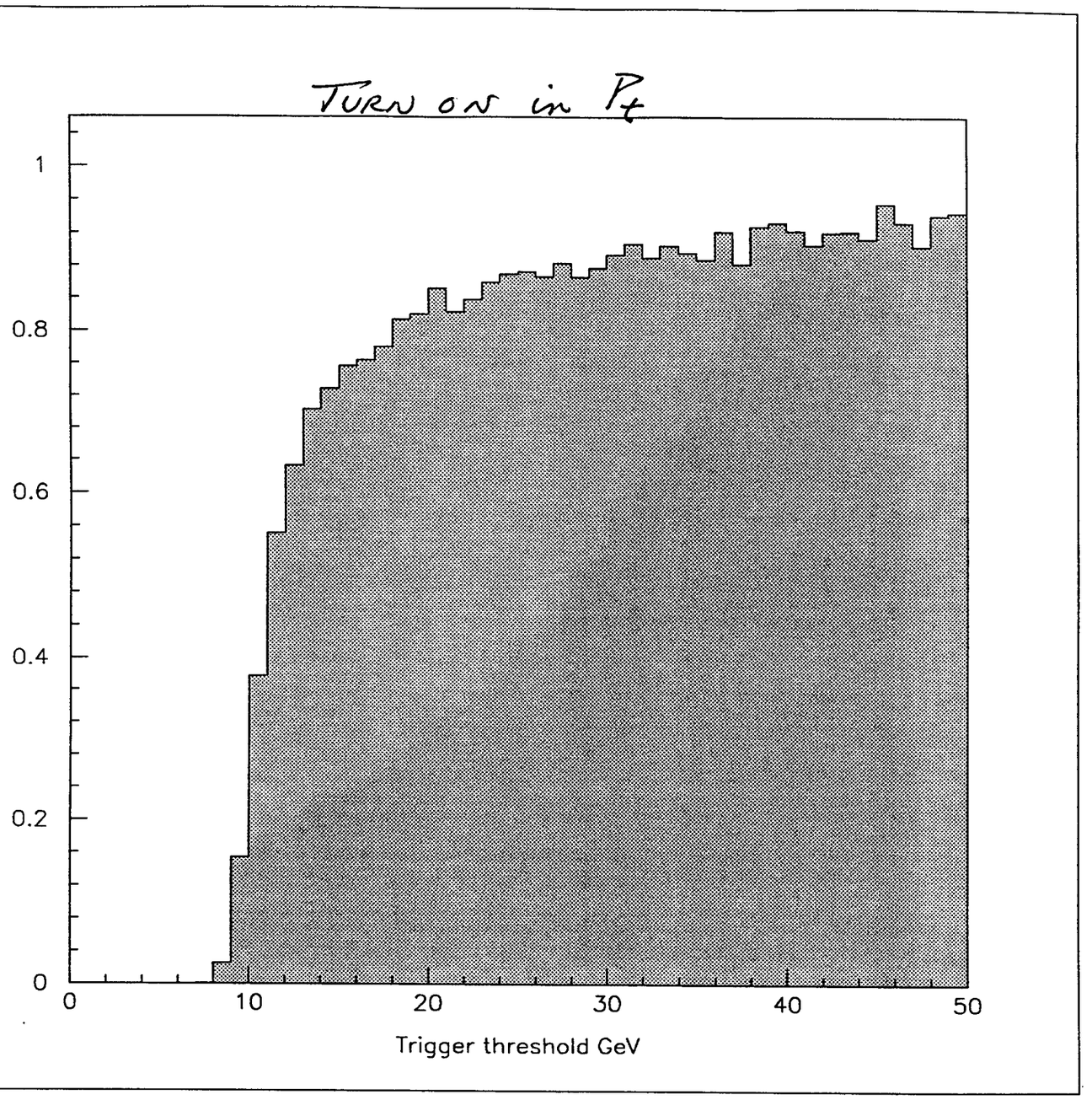
One of Six Patterns

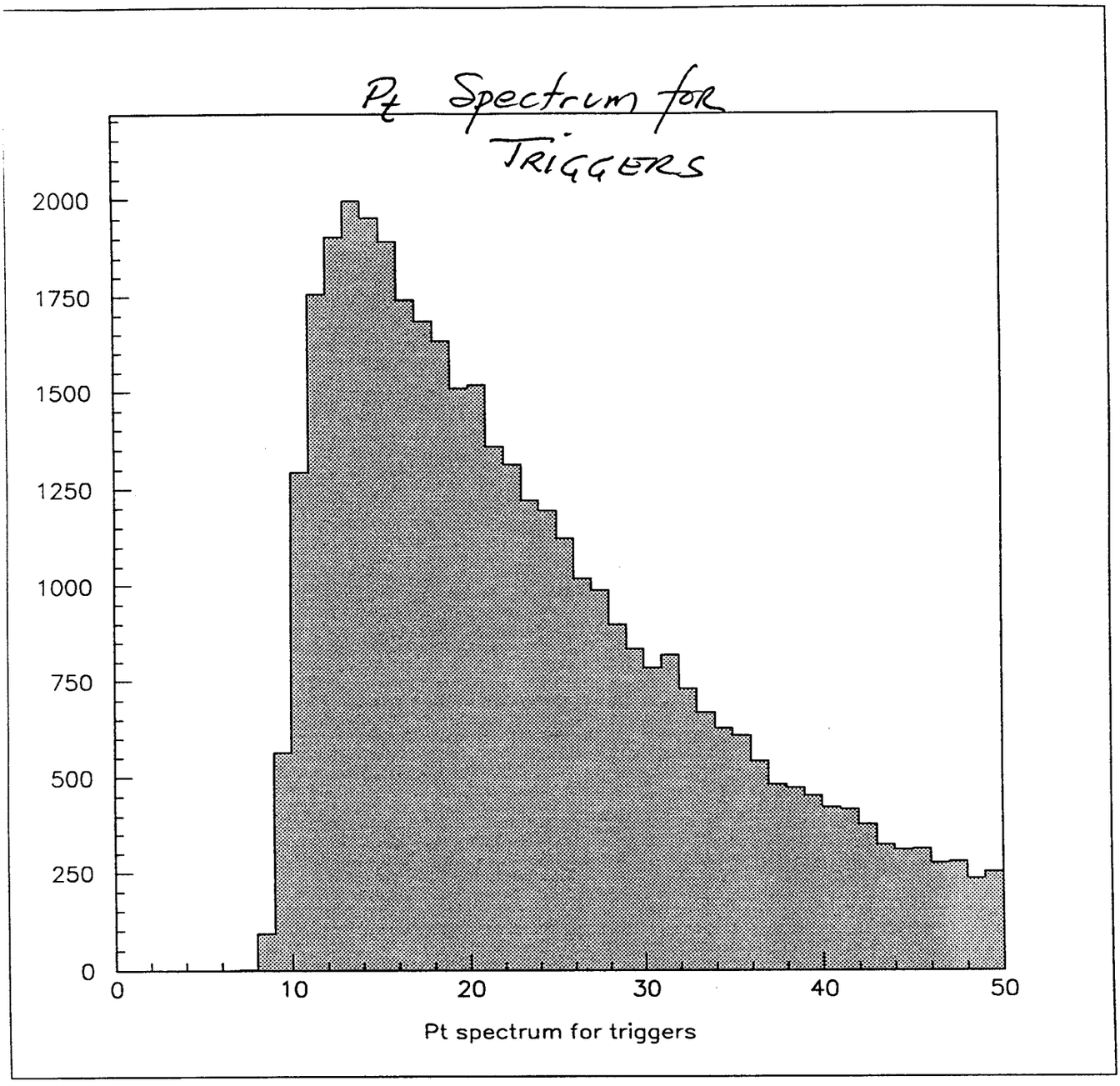


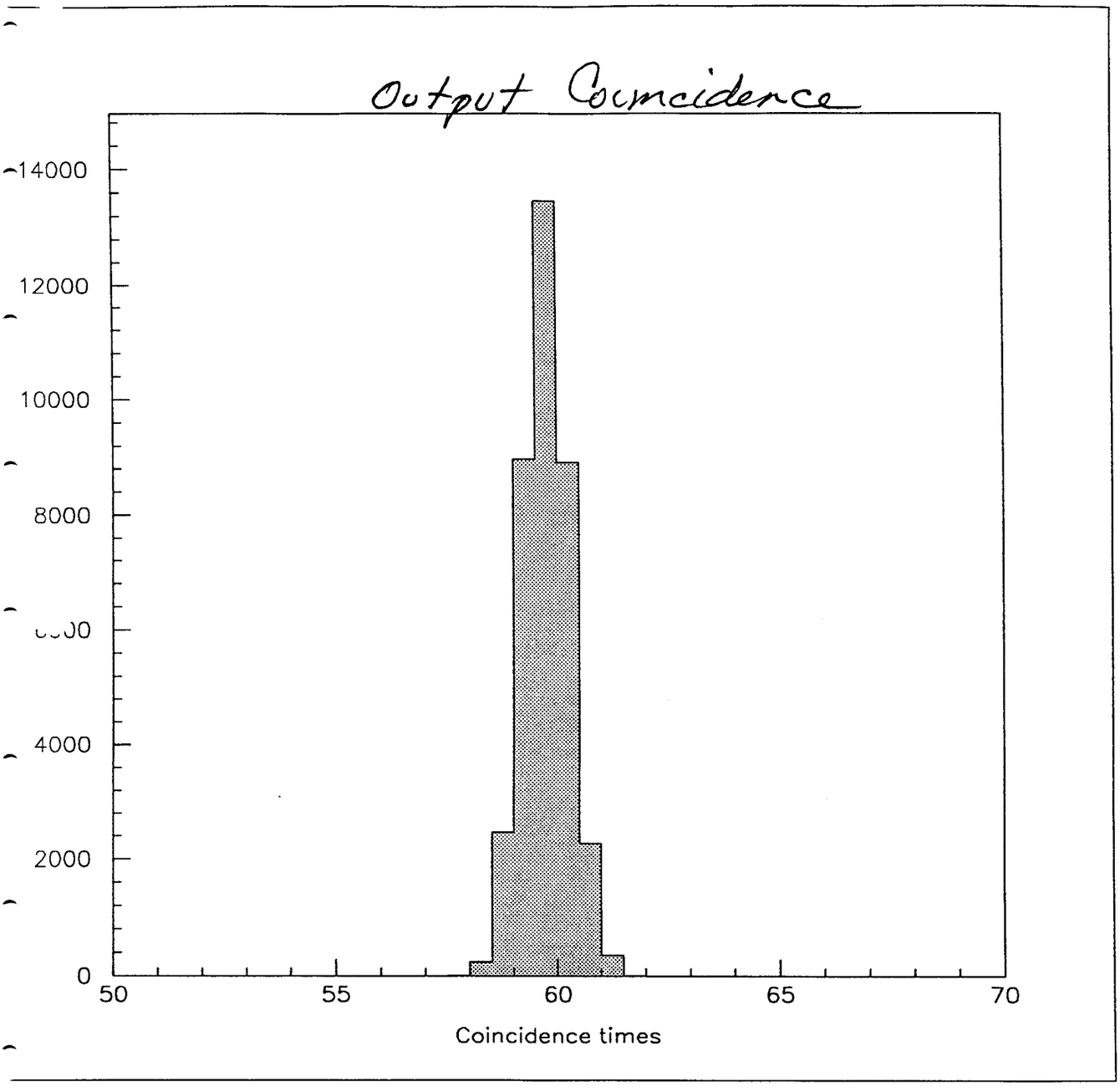

6000
5000
4000
3000
2000
1000
0
0
10
20
30
40
50
Pt spectrum


CENTRAL PAIR
1200
1000
800
400
200
0
−2
−1
0
1
2
Entry position for triggers


NEIGHBOR PAIRS
1200
1000
800
600
400
200
0
−2
−1
0
1
2
Entry position for neighbors

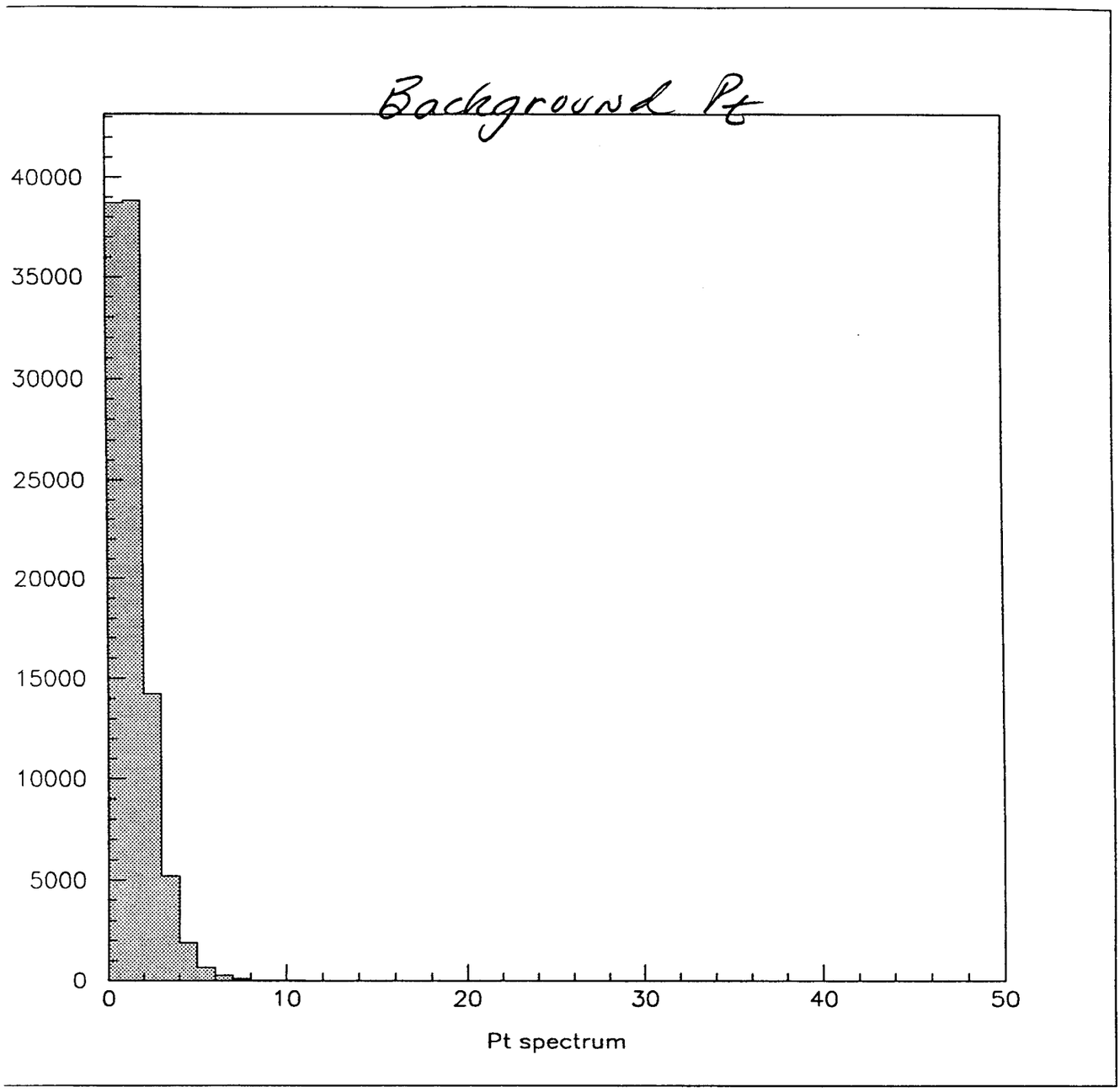

TURN ON in P_t
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
Trigger threshold GeV

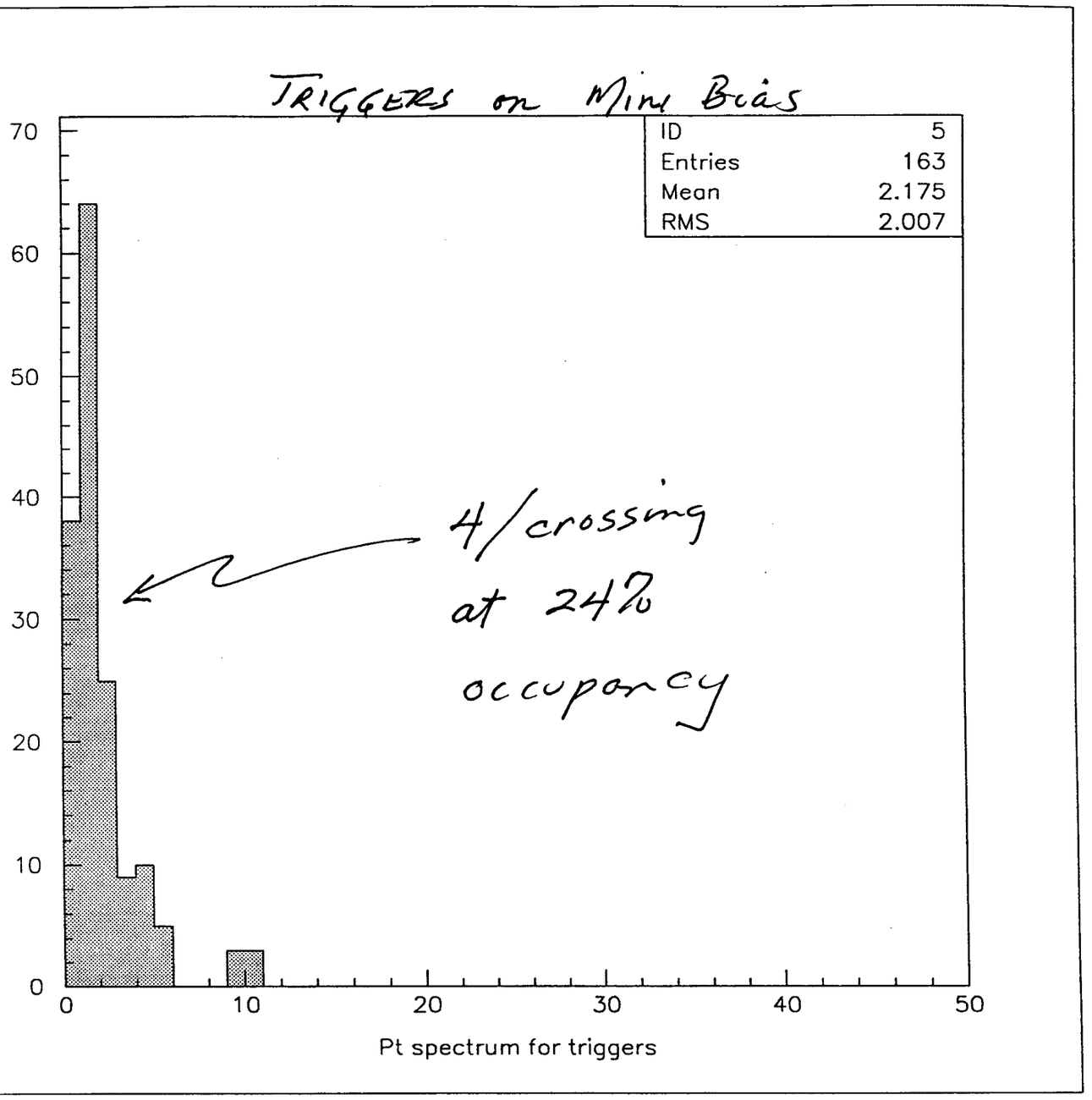

P_t Spectrum for TRIGGERS
2000
1750
1500
1250
1000
750
500
250
0
0
10
20
30
40
50
Pt spectrum for triggers


Output Coincidence
14000
12000
10000
8000
4000
2000
0
50
55
60
65
70
Coincidence times

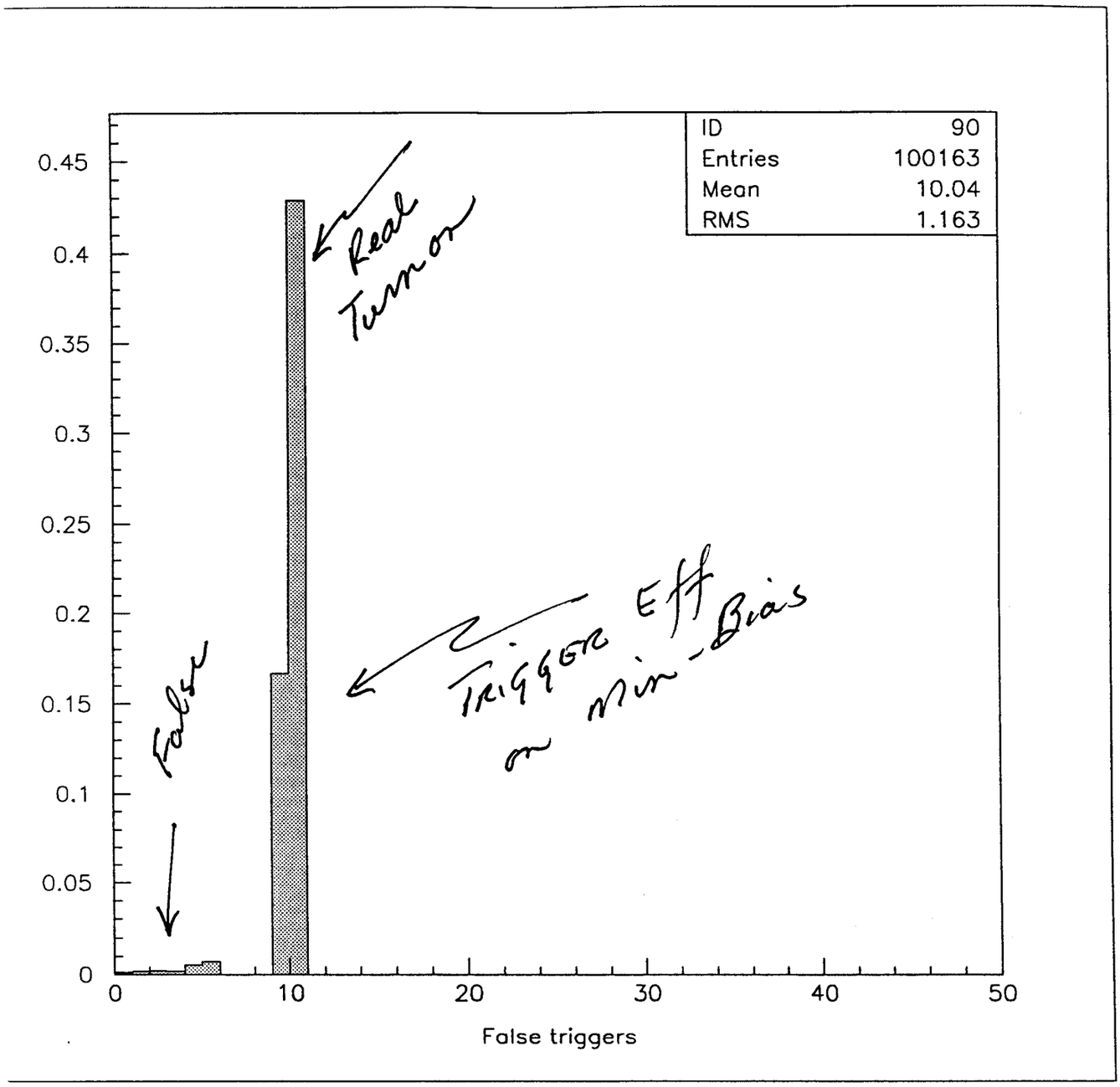
437

4.0 ns

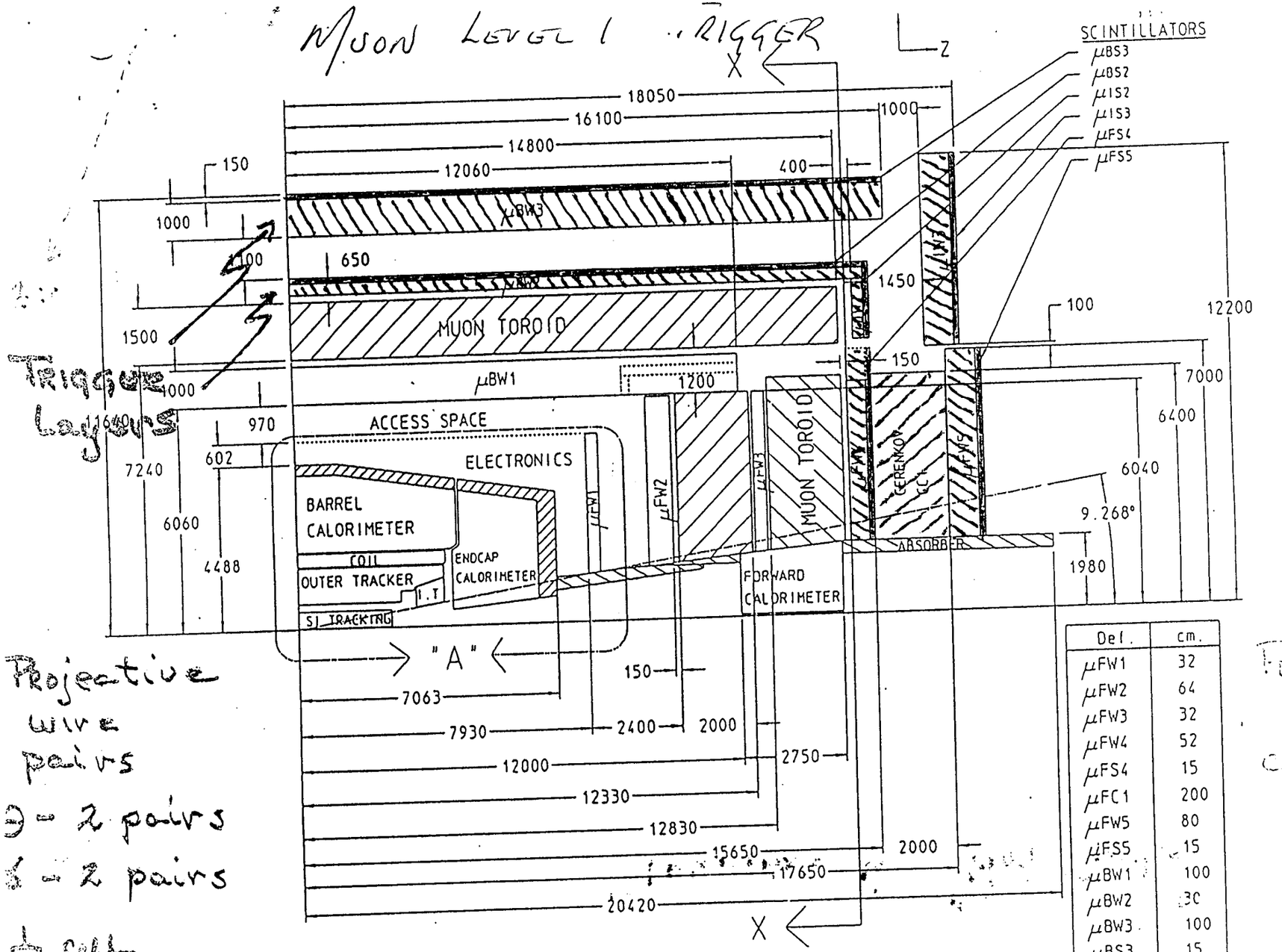

Background Pt
40000
35000
30000
25000
20000
15000
10000
5000
0
0
10
20
30
40
50
Pt spectrum


TRIGGERS on Min Bias
ID 5
Entries 163
Mean 2.175
RMS 2.007
4/crossing
at 24%
occupancy
70
60
50
40
30
20
10
0
0
10
20
30
40
50
Pt spectrum for triggers

24%


ID 90
Entries 100163
Mean 10.04
RMS 1.163
Real Tumor
TRIGGER Eff on Min-Bias
False
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
10
20
30
40
50
False triggers

MUON LEVEL 1 TRIGGER



Det.	cm.
μFW1	32
μFW2	64
μFW3	32
μFW4	52
μFS4	15
μFC1	200
μFW5	80
μFS5	15
μBW1	100
μBW2	30
μBW3	100
μBS3	15
μIW2	30
μIS2	15
μIW3	80
μIS3	15

Trigger Layers

Projective wire pairs

9 - 2 pairs

6 - 2 pairs

1/2 cell staggered

NOTE. ALL DIMENSIONS ARE IN MILLIMETERS

0 1 2 3 4 5 M

TOROID. NO MOVE DESIGN

APRIL 23. 1991

441

US Trigger Work Options

1. Scintillator - projective wires - mean timers
   (a) Layer pairs × 2 - scintillator timing
      (i) Rectangular stacks/cell width vrs radius
      (ii) Rotating/overlapping edges
   (b) Layer triads × 2 - coincidence timing
   (c) Layer pairs × 3 - differential pair timing

2. Call for:
   (a) Description of missing activities
   (b) Interested persons
3. Assemble e-mail list of μ electronics/trigger persons
4. Pull together effort $\rightarrow$ design decisions
5. Form ties with trigger subgroup

- Coordinators meeting after KEK

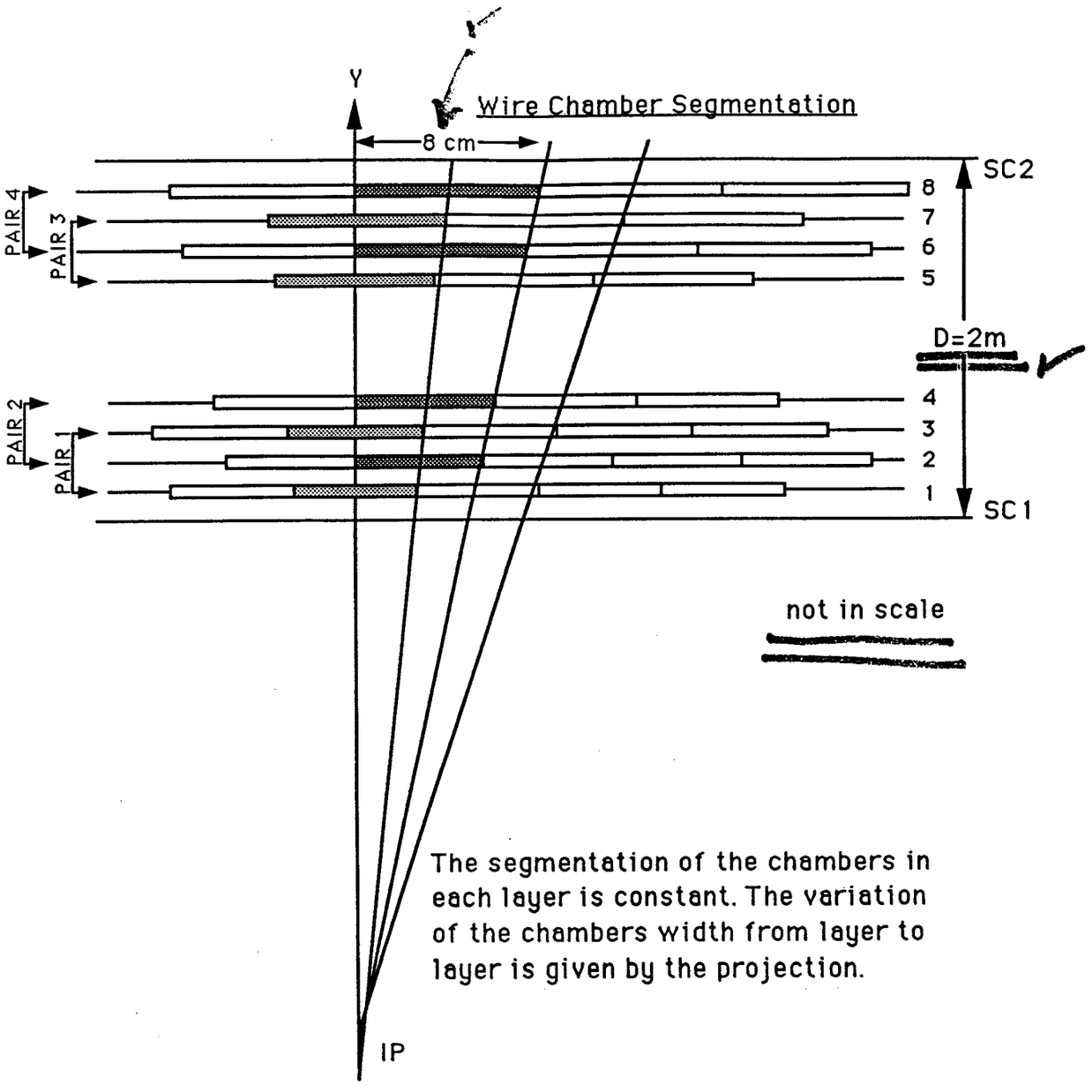
Muon Trigger Work in Japan

H. Sakamoto

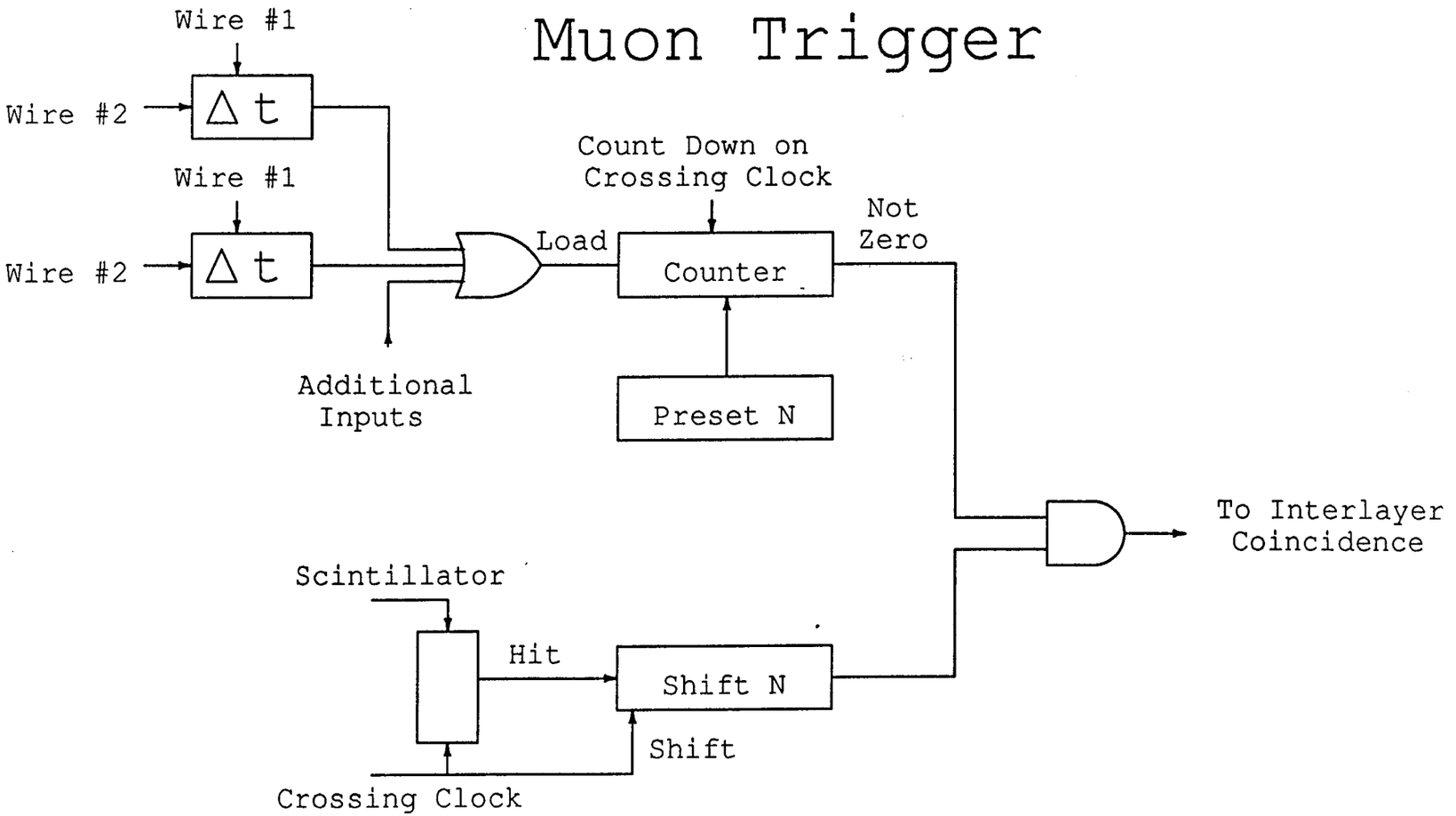
1. Scintillator - projective wires - mean timers
   (a) Layer pairs × 2 - scintillator timing
   (b) Layer triads × 2 - wire and scintillator timing
2. Scintillator - non-projective wires
   (a) Memory lookup
   (b) Pipelined processing

Sakai/Arai

1. Jet Chamber - 4 trigger approaches
   (a) Options:
      (i) Scintillator only (same $\frac{1}{Sin^2(\Theta)}$)
      (ii) Scintillator - 3/4 coincidence in jet cell
      (iii) Scintillator - mean timers on 1/2 staggered wire jet cell
      (iv) Scintillator - wire hits in outer two superlayers
      (v) Scintillator - wire hits in all three superlayers
   (b) Features of options
      (i) P_t cut at ≈10GeV (fixed)
      (ii) P_t cut to 40GeV, timing from scintillator
      (iii) P_t cut to 80GeV, coincidence timing
      (iv) P_t cut ≈40GeV, broad coincidence
      (v) Same P_t cut, better rejection

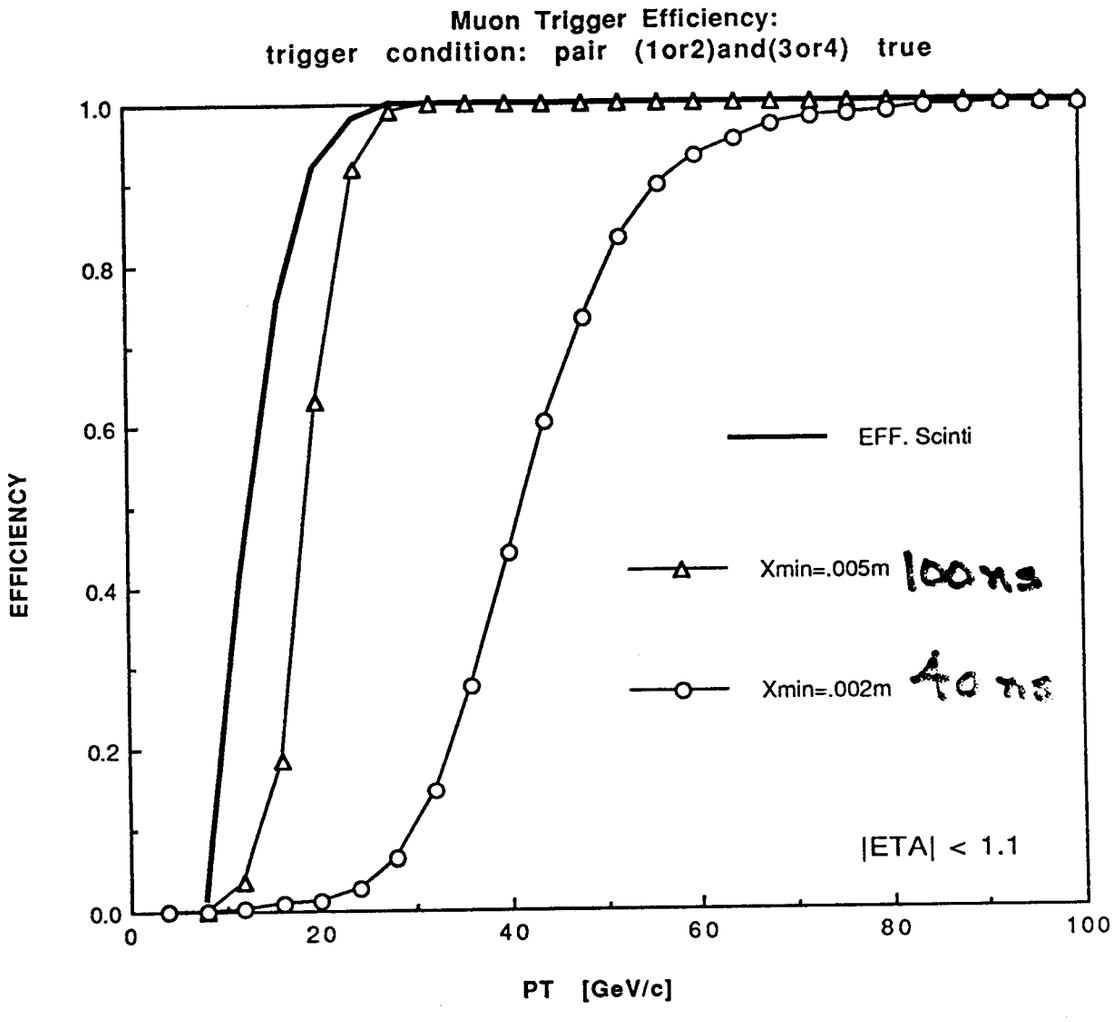

Wire Chamber Segmentation
Y
8 cm
SC2
8
7
6
5
D=2m
4
3
2
1
SC1
PAIR 4
PAIR 3
PAIR 2
PAIR 1
not in scale
The segmentation of the chambers in each layer is constant. The variation of the chambers width from layer to layer is given by the projection.
IP

Muon Trigger



SDC Muon Trigger Simulation

Data from "M3all.dat"



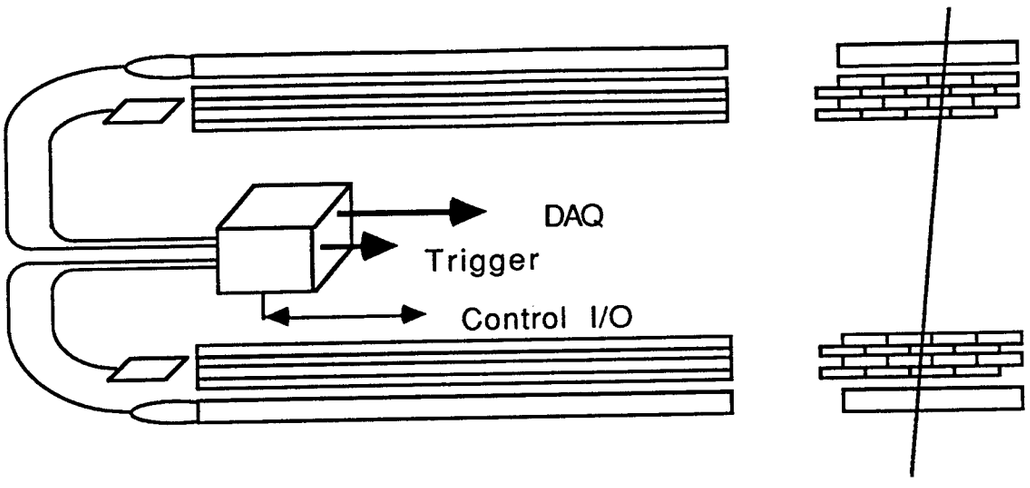
Electronics Tasks - Natural Divisions

1. Tasks/Features/Questions
   (a) On/near chamber amplifier/discriminators
   (b) On/near phototube amplifier/discriminators
   (c) Cabling (digital) to regional trigger crates
   (d) Synchronous 16ns binning of phototube signals
   (e) Mean timers for projective wires
   (f) Synchronous operation with crossing clock
   (g) Tagging (coincidence) of scintillator by Δt pairs
   (h) Do 6 layers offer enough to justify costs?
      (i) Triad pairs $\rightarrow$ narrow timing window
      (ii) 1/3 staggered $\rightarrow$ no dead spots

2. Natural Divisions (Coordinators)
   (a) Scintillators, amplifiers, and discriminators (Thun/?)
   (b) Wires, amplifiers, test pulses, and discriminators (Oliver)
   (c) Čerenkov amplifiers, testing, and discriminators (Nauenberg)
   (d) Storage, L1 trigger, and multiplexing (Chapman)
   (e) L2 trigger and tracking match (Campbell/?)
   (f) Simulations (Errede)
      (i) Physics and geometry (GEANT or quick)
      (ii) Verilog and electronic

μ Trigger Units						
Region	η_{low}	η_{high}	Option	# units	$\Delta\eta_{low}$	$\Delta\eta_{high}$
Barrel	0.0	1.0	15cm	3024		
	0.0	1.0	20cm	2304		
Forward	1.0	2.5	8cm	1824		
	1.0	2.5	10cm	1440		

Muon Level 1 Trigger and Storage



2400 Channels/octant with 4 boxes/octant -> 600 tubes/box

600 tubes/box with 64 channels/tube -> 10 cards/box

10 cards/box with 6 auxillary cards -> 16 slots/box

Assumes 4 Wire layers and one scintillator layer/superlayer

Rough cost estimate is $8M between front-end -> DAQ

Front-end storage and trigger chips
Clock, multiplexing, and fast control
Test pulse distribution
Fiber data drivers
VME slow control i/o

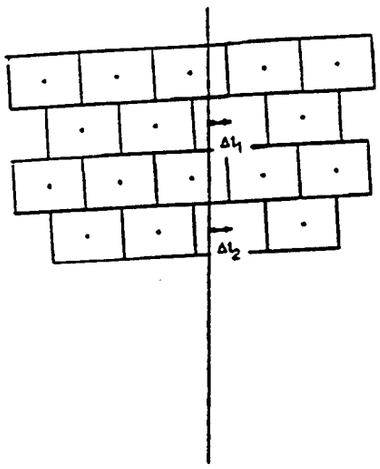


FIG. 10. Arrangement of projective wires for a first-level trigger. An infinite-momentum track will have $\Delta t_1 = \Delta t_2$. Differences in the time signals will be inversely proportional to the transverse momentum. "muonfirst"

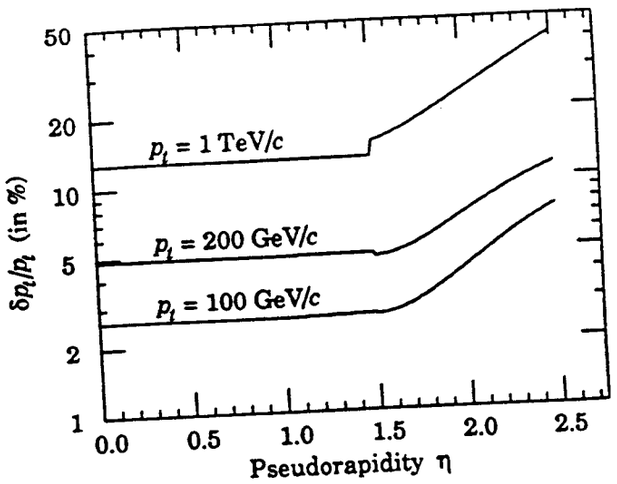


FIG. 12. Muon momentum resolution as a function of rapidity for various values of transverse momentum. The conservative resolution figure quoted in Table ... is used to characterize the central tracking performance. "muonthird"

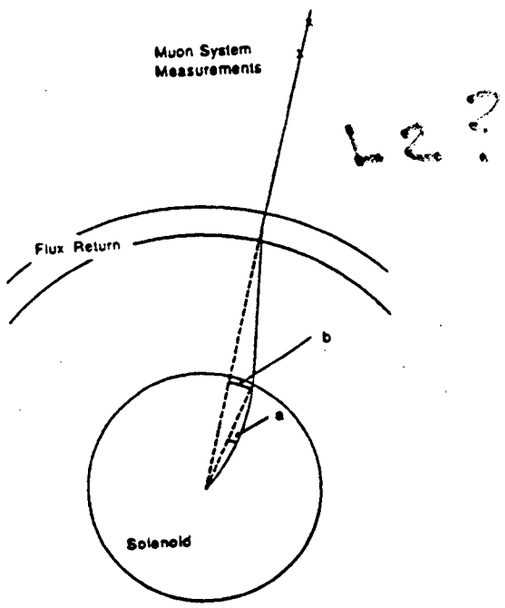


FIG. 11. Illustration of the reason for the improvement of momentum resolution coming from azimuthal measurements in the muon system. Without the muon system measurements, the sagitta is shown by a, whereas with the muon system measurements, the effective sagitta is shown by b. The curvature of a very low momentum track has been used for the purpose of illustration. "muonsecond"

Level 2 Trigger Sagitta Errors			
P_{cut}	10	20	50
Multiple Scattering	18mm	9mm	3.6mm
μ halfcell	2.9mm	2.9mm	2.9mm
Straw cell	1.2mm	1.2mm	1.2mm
Sagitta	100mm	50mm	20mm
% Error	18	18	24

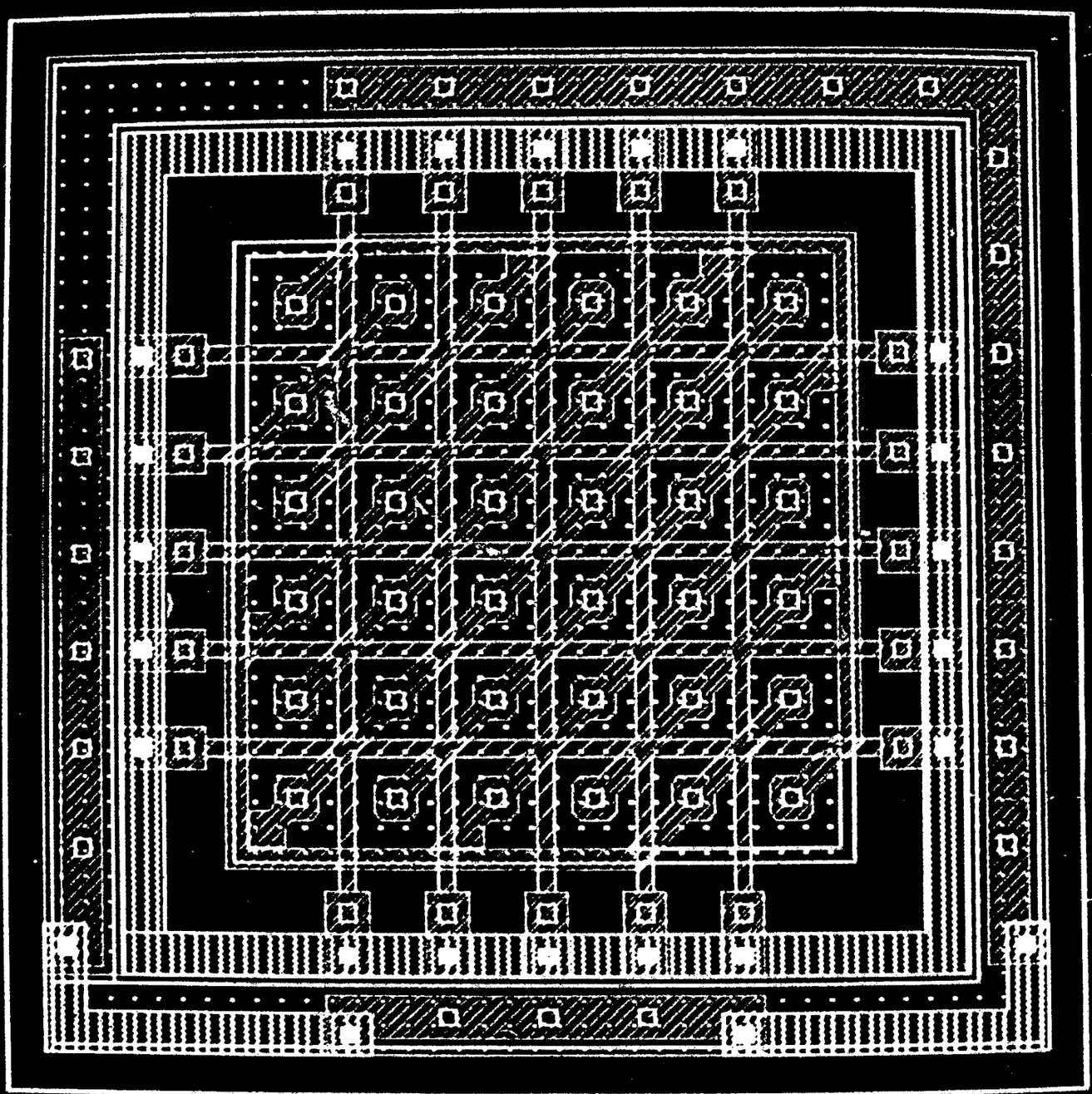
Radiation Hard CMOS & Bipolar

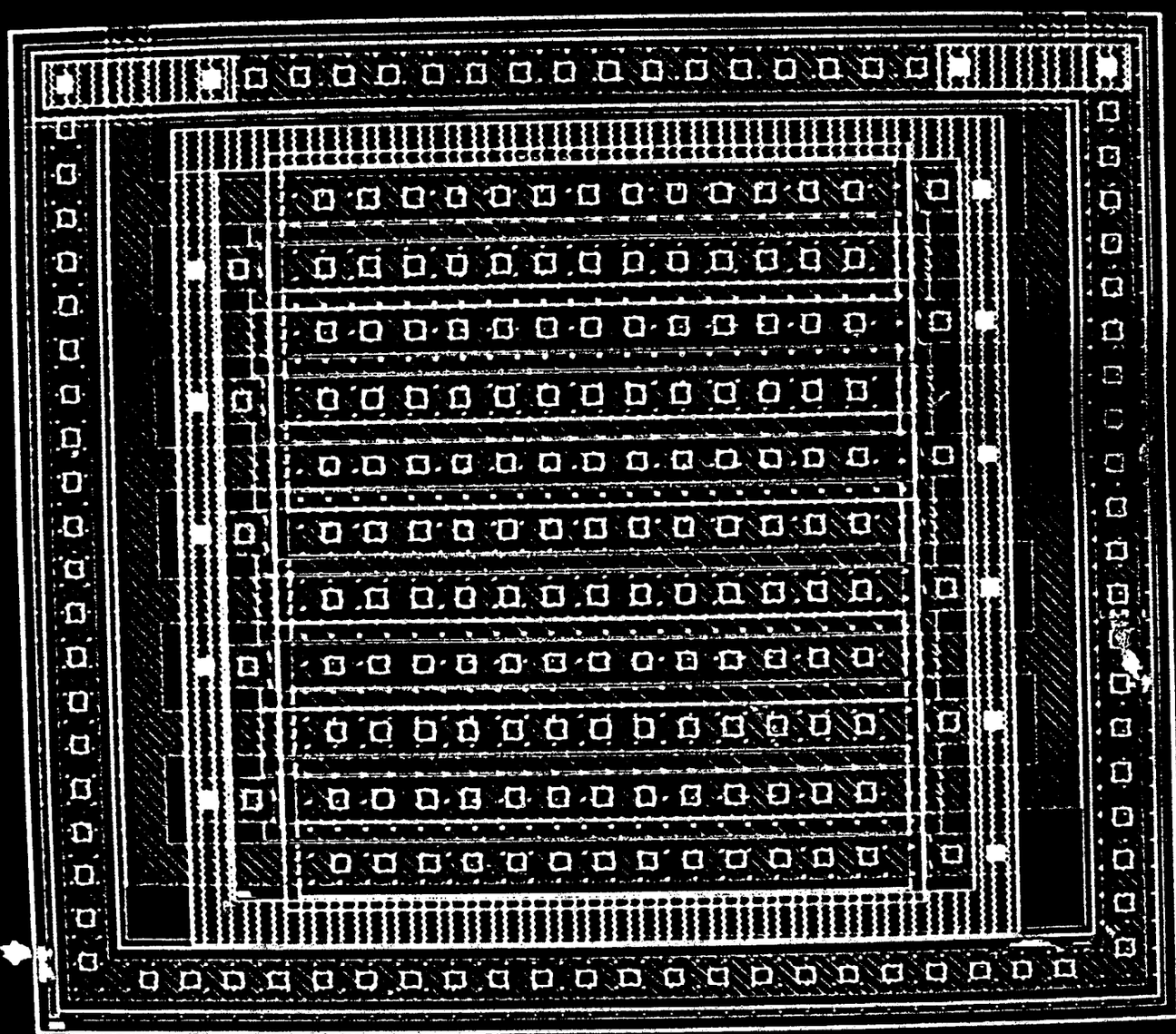
H. Williams

Noise in Rad-Hard CMOS Transistors

study 1/f & thermal noise of large "low noise" transistors

* waffle & interdigitated
* vary w/l



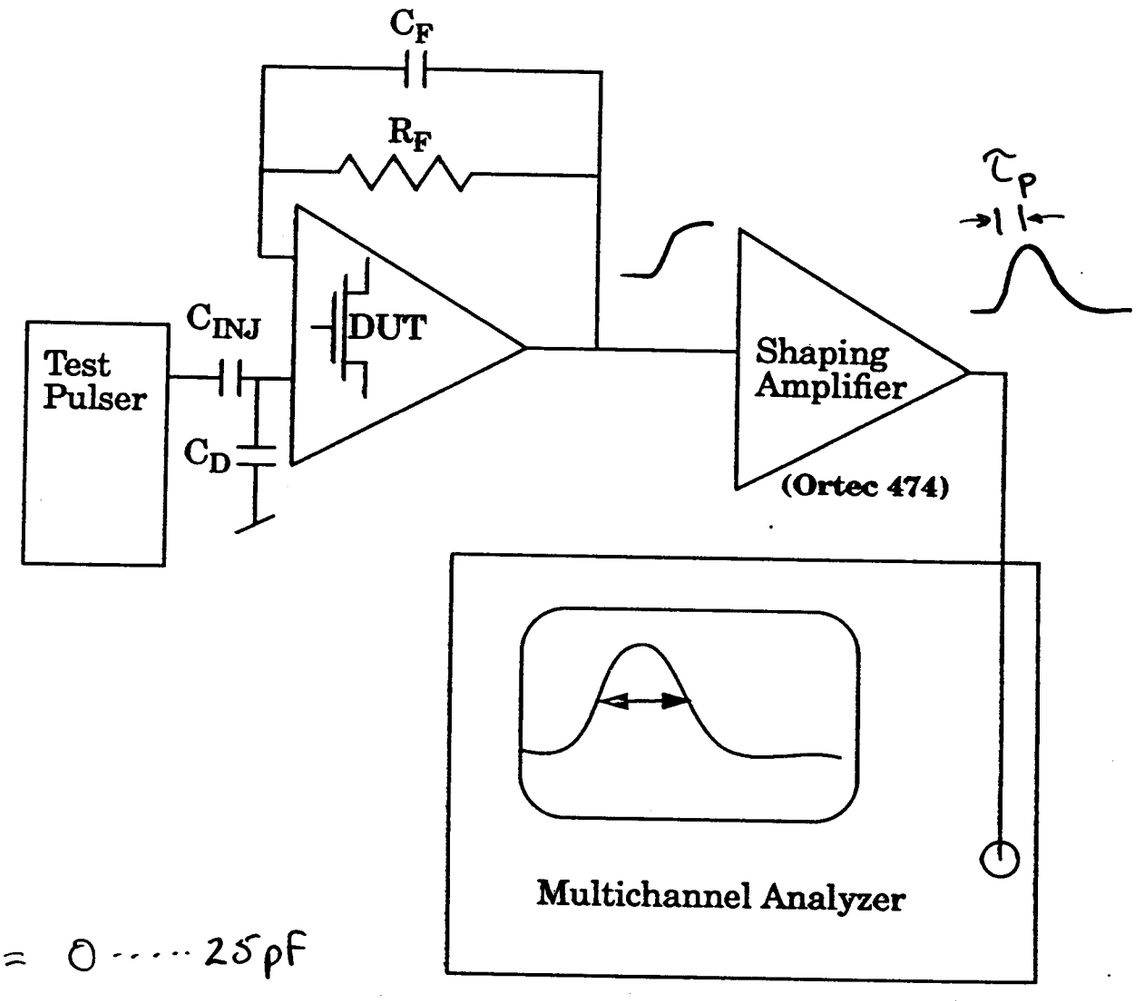


Interdigitated Transistor Capacitances

	$C_{gs} + C_{gd}$ (pF)		C_{Total} (pF)	
Device W/L	NMOS	PMOS	NMOS	PMOS
3996/3.2	13.0	14.3	23.0	25.0
2664/2.2	6.2	6.8	17.0	19.9
1332/1.2	1.8	2.0	14,0	16.3
1332/3.2	4.3	4.8	16.0	17.8
888/2.2	2.1	2.3	13.8	14.9
666/1.7	1.2	1.3	14.0	14.7
444/1.2	0.6	0.7	13.0	13.8
532.8/3.2	1.7	1.9	13.8	15.7
355.2/2.2	0.8	0.9	12.4	14.2
177.6/1.2	0.25	0.3	12.4	13.4

- Note that C_{gs} and C_{gd} are calculated using $C_{ox} = \frac{1.4fF}{\mu m^2}$ for NMOS and $C_{ox} = \frac{1.4fF}{\mu m^2}$ for PMOS. C_{Total} values are measured with $C_D = 0$. C_{Total} includes the pin to GND pin parasitic capacitance of the 181 pin package - approximately 10 pF.

Noise Measurement
UTMC 1.2 μm CMOS

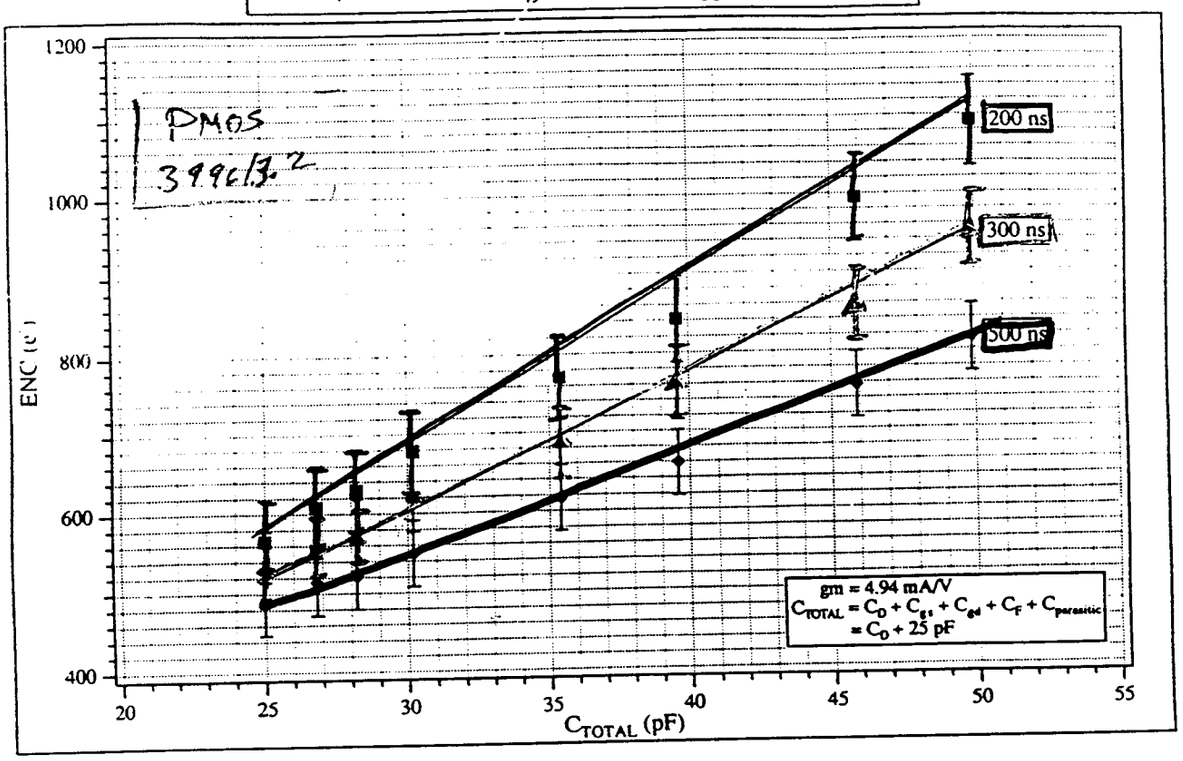


$C_D = 0 \cdots\cdots 25\,pF$

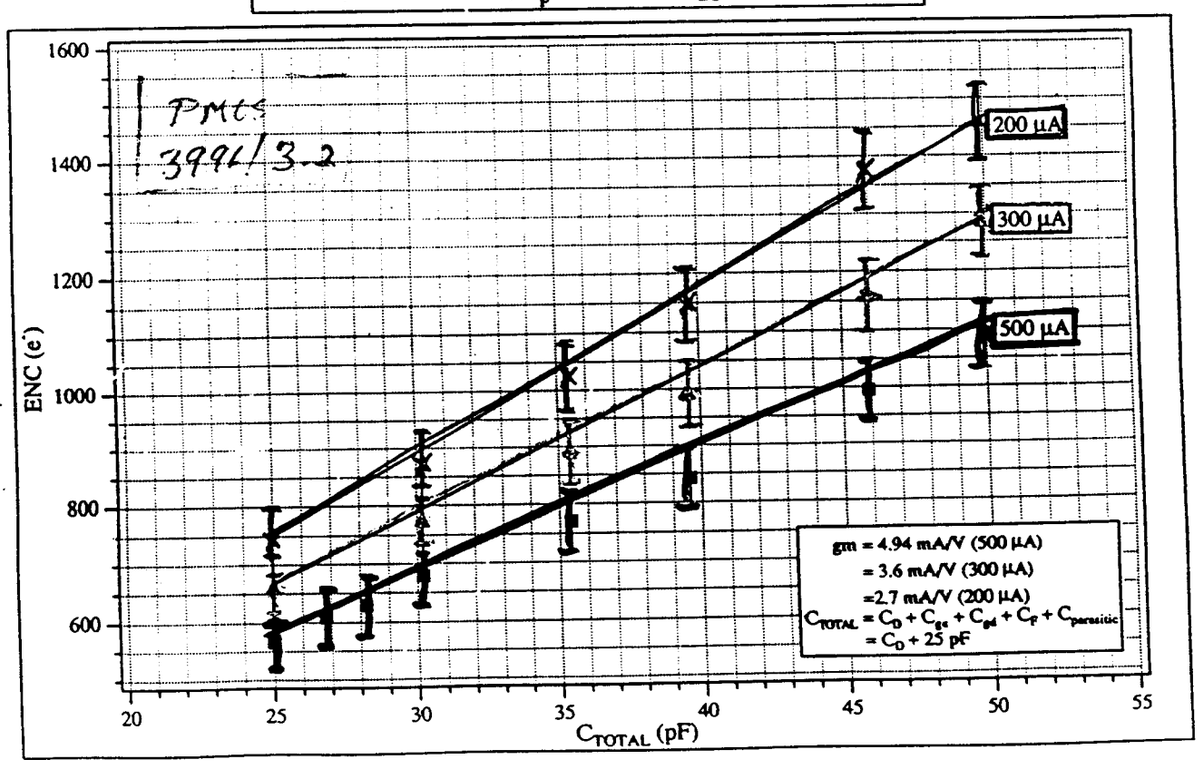
$\tau_p \approx 200 \cdots\cdots 500\,ns$

$I_D \approx 100 \cdots\cdots 500\,\mu A$

Noise Performance of UTMC PMOS devices
ENC vs. Total Capacitance for different peaking time T_p
W/L = 3996/3.2, I_D = 500 µA, V_{DS} = - 2.0 V

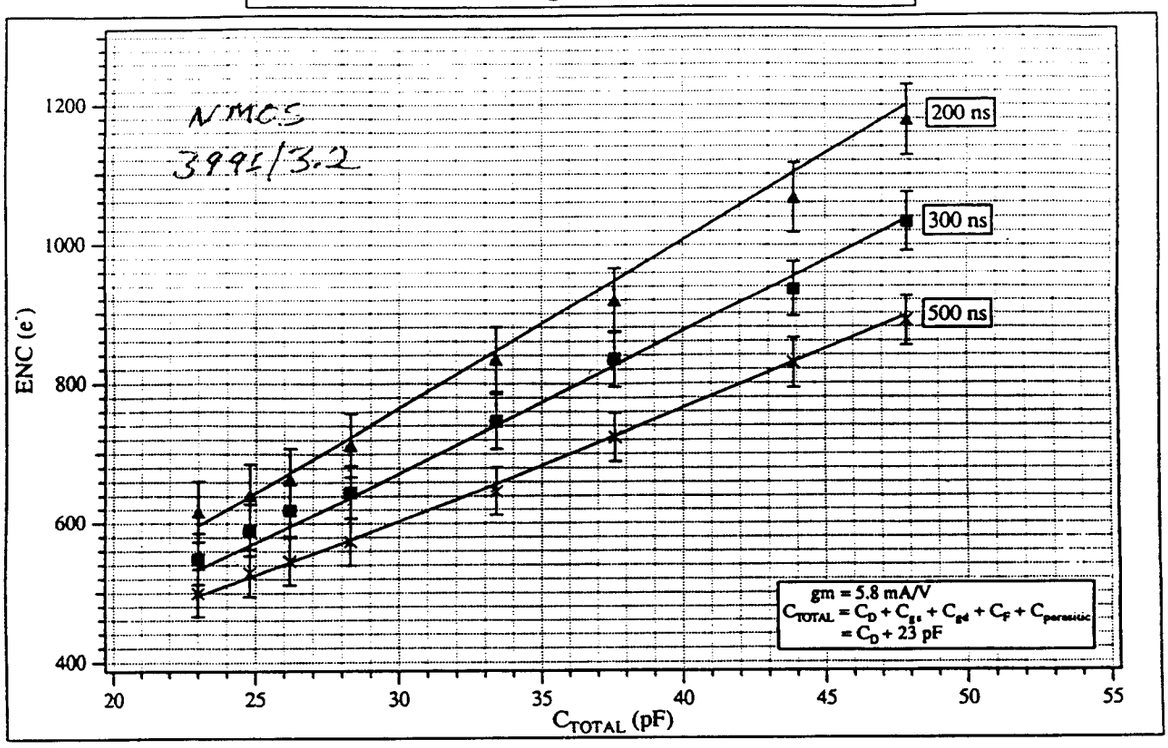


Noise Performance of UTMC PMOS devices
ENC vs. Total Capacitance for different drain current I_D
W/L = 3996/3.2, T_p = 200 ns, V_{DS} = - 2.0 V



ENC vs. Total Capacitance for different peaking time T_p

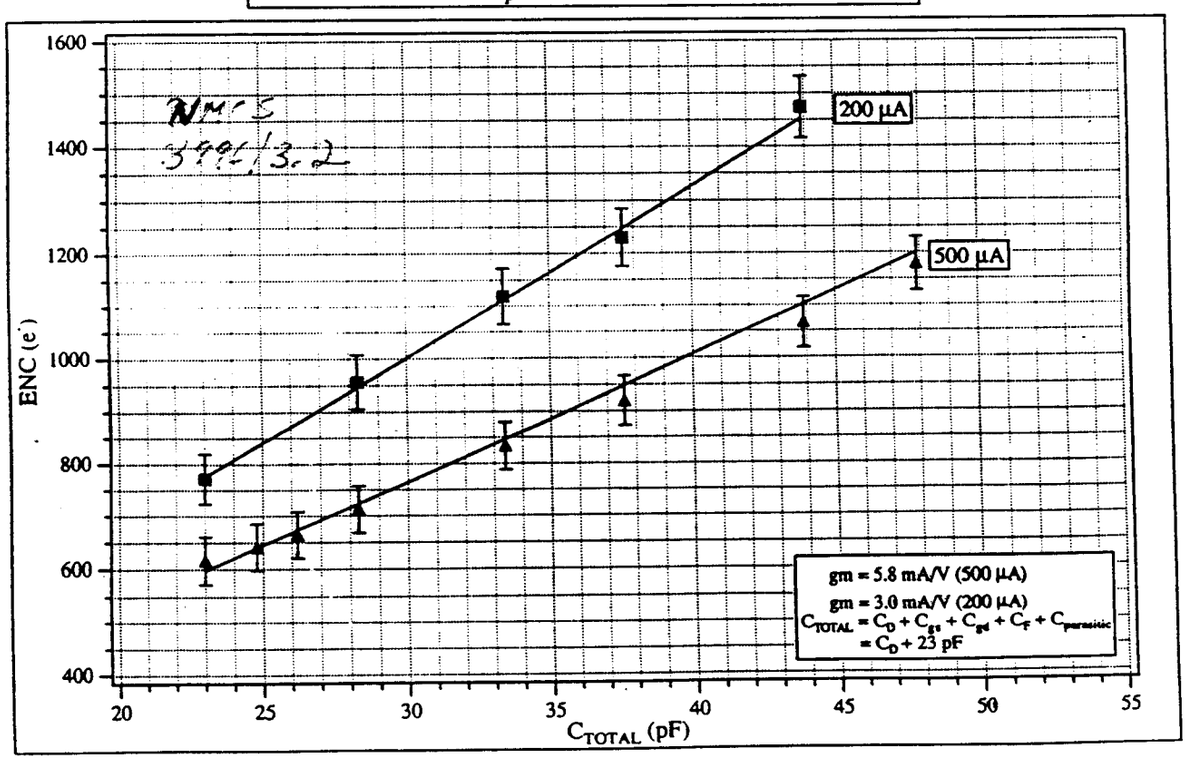
W/L = 3996/3.2, I_D = 500 µA, V_{DS} = 1.9 V



Noise Performance of UTMC NMOS devices

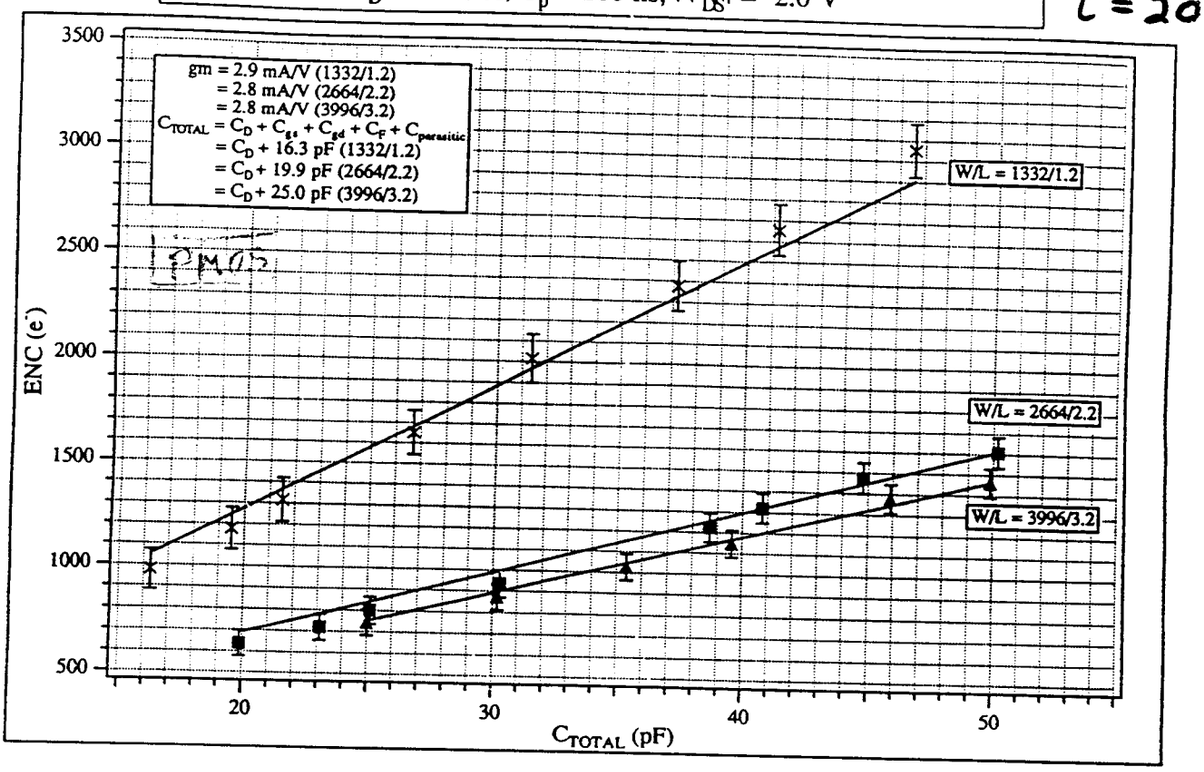
ENC vs. Total Capacitance for different drain current I_D

W/L = 3996/3.2, T_p = 200 ns, V_{DS} = 1.9 - 1.95 V

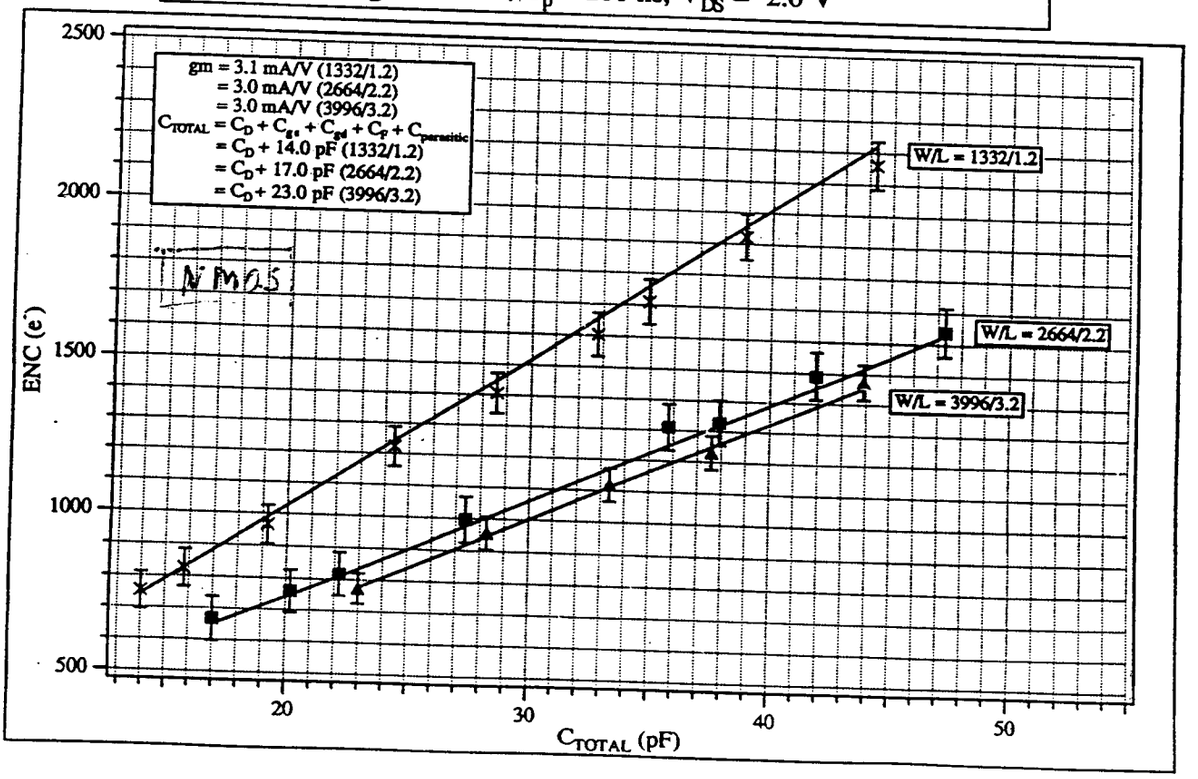


Noise Performance of UTMC PMOS devices
ENC vs. Total Capacitance for different channel lengths (W/L = 1200 : 1)
I_D = 200 µA, T_p = 200 ns, $|V_{DS}|$ = 2.0 V

$I_D = 20$
$\tau = 200$



Noise Performance of UTMC NMOS devices
ENC vs. Total Capacitance for different channel lengths (W/L = 1200 : 1)
I_D = 200 µA, T_p = 200 ns, V_{DS} = 2.0 V



Extraction of Noise Coefficients

- Multiparameter Fit -

  $C_{Total} = C_D + C_{gs} + C_F + C_{inj} + C_{parasitic}$
  g_m
  τ_P
  Area = WL
  $R_F = 111M\Omega$

- Devices of equal L fit simultaneously

Thermal Parallel

$$ENC^2 = \frac{1}{2} \cdot kTe^2 C_{Total}^2 \left[\varepsilon \cdot \frac{1}{g_m \cdot \tau_p} + K_f \cdot \frac{1}{C_{ox}} \cdot \frac{1}{W \cdot L} \cdot \frac{1}{kT} \right] + \frac{1}{2} \cdot kTe^2 \frac{\tau_P}{R_F} + Floor$$

1/f Floor

Ekenberg,
Argonne Nat'l
Lab

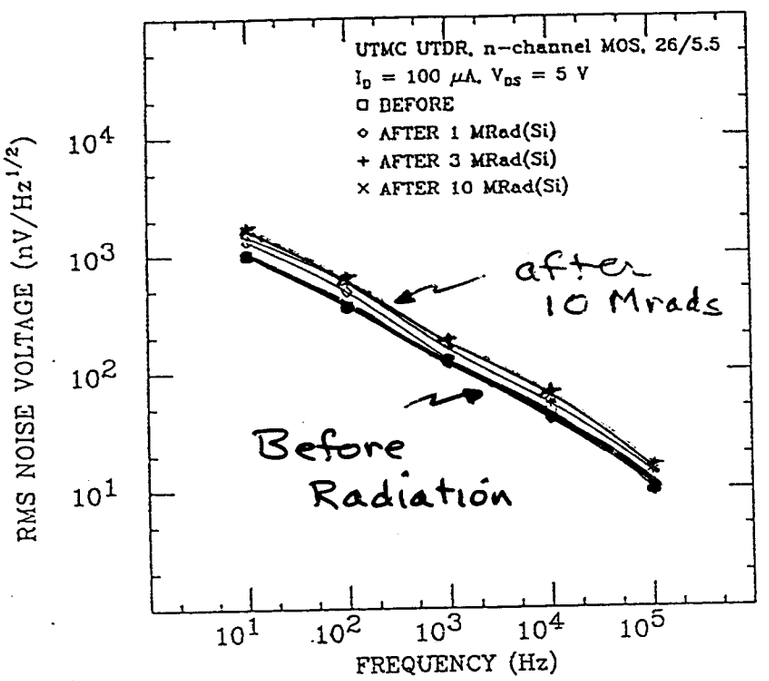
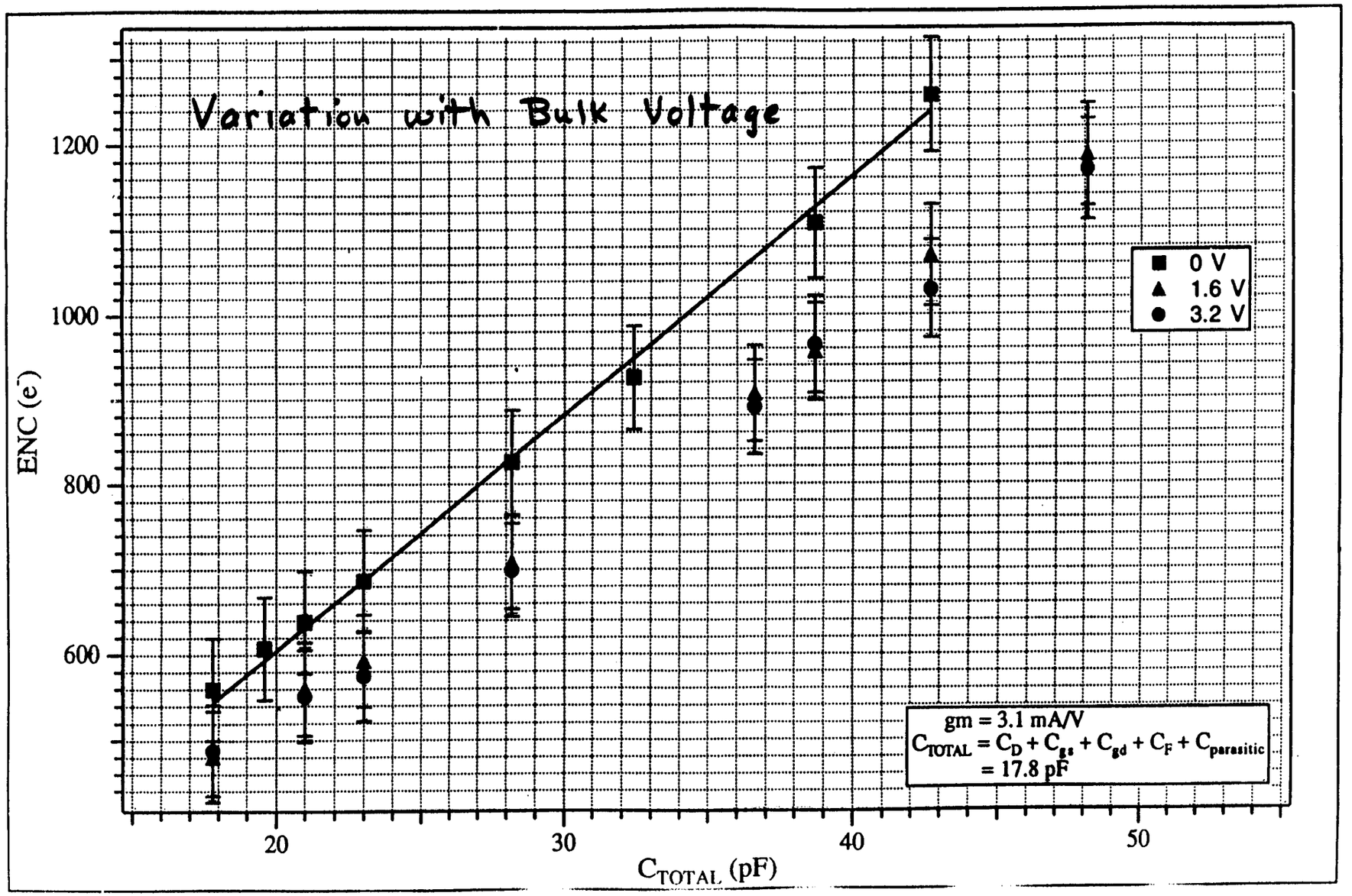
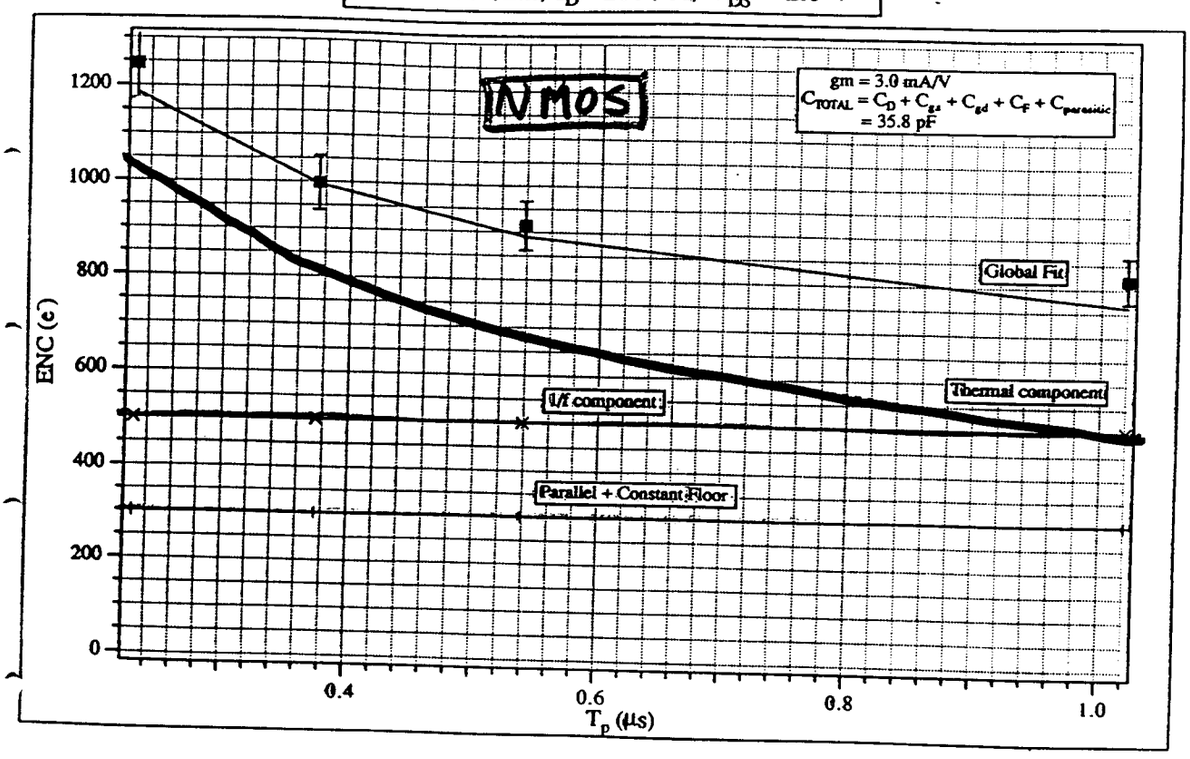


Figure 6: Series noise in UTMC 1.5 μm rad-hard UTDR process in 26/5.5 $(\mu m)^2$ n-channel device pre-rad and after 1 Mrad(Si), 3 MRad(Si), and 10 MRad(Si).

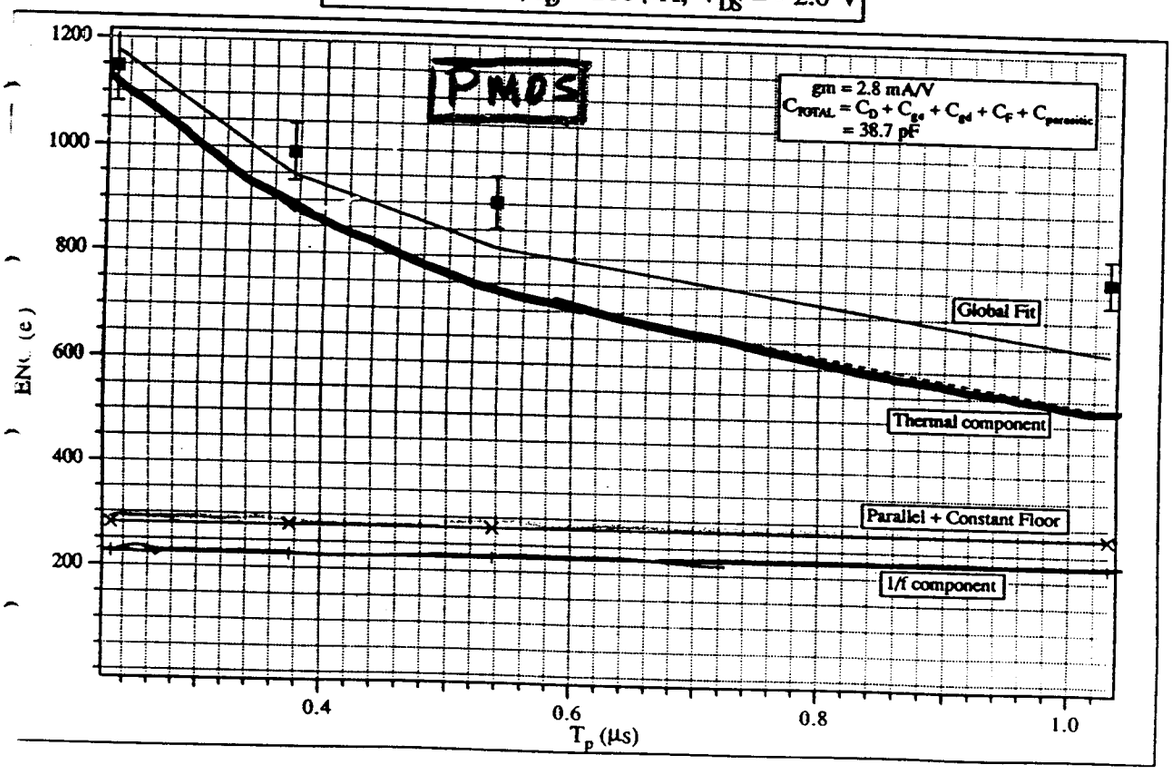
Noise Performance of UTMC PMOS devices
ENC vs.Total Capacitance for different bulk voltages
W/L = 1332/3.2, I_D = 500 μA, T_p = 200 ns, V_{DS} = - 2.0 V



Noise Performance of UTMC NMOS devices
ENC vs.Peaking Time T_p
W/L = 2664/2.2, I_D =200 µA, V_{DS} = 2.0 V



Noise Performance of UTMC PMOS devices
ENC vs.Peaking Time T_p
W/L = 2664/2.2, I_D = 200 µA, V_{DS} = - 2.0 V



Noise Coefficients

$$ENC^2 = \underbrace{\frac{1}{2} \cdot kTe^2 C_{Total}^2 \left[\varepsilon \cdot \frac{1}{g_m \cdot \tau_P} + K_f \cdot \frac{1}{C_{ox}} \cdot \frac{1}{W \cdot L} \cdot \frac{1}{kT} \right]}_{1/f} + \underbrace{\frac{1}{2} \cdot kTe^2 \frac{\tau_P}{R_F}}_{\text{Parallel}} + \underbrace{Floor}_{\text{Floor}}$$

Thermal

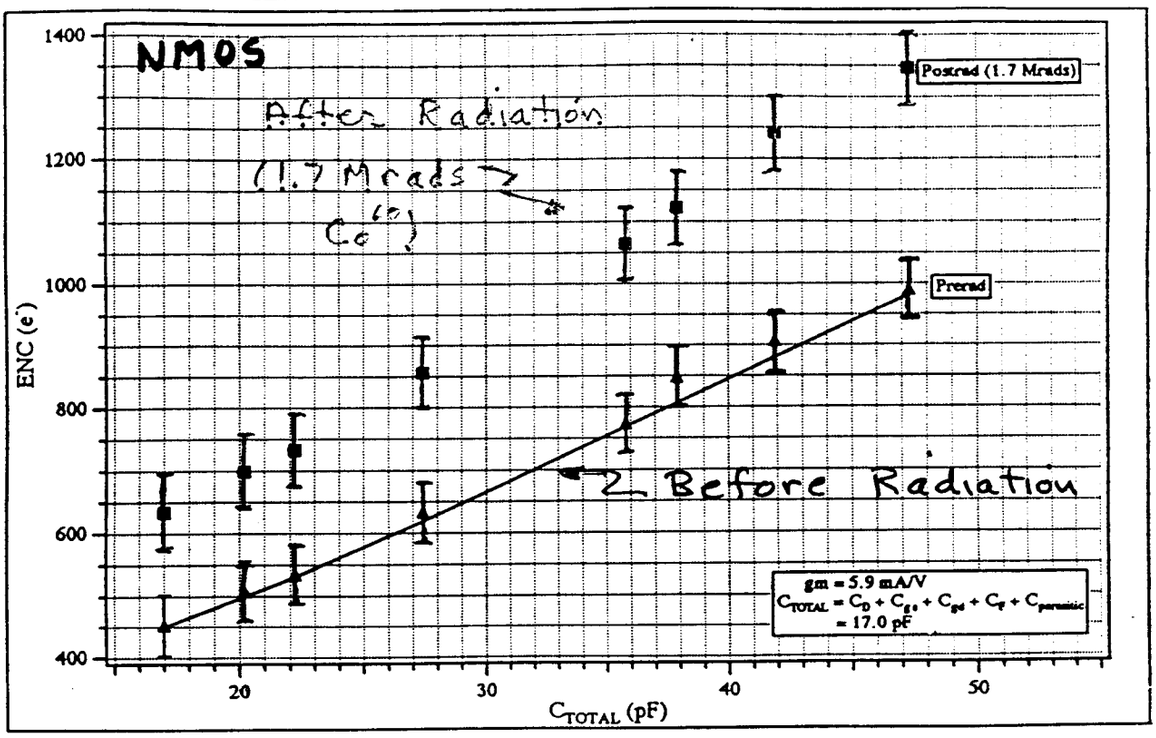
L(μm)	ε "γ"		K_f (x 10^{-12} V^2pF)		Floor (x 10^{-3} fC^2)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
3.2	0.9 ± 0.1	0.75 ± 0.1	13.0 ± 2	3.0 ± 1.5	2.0 ± 0.2	2.0 ± 0.3
2.2	1.0 ± 0.1	0.9 ± 0.1	8.0 ± 1.4	1.5 ± 0.5	2.3 ± 0.3	2.5 ± 0.4
1.7	0.85 ± 0.2	1.0 ± 0.2	6.7 ± 2	1.5 ± 0.5	1.4 ± 0.3	2.2 ± 0.3
1.2	1.5 ± 0.2	2.6 ± 0.3	9.1 ± 1	1.5 ± 0.5	3.5 ± 1	3.5 ± 1

- TYPICAL *MOSIS* K_f:

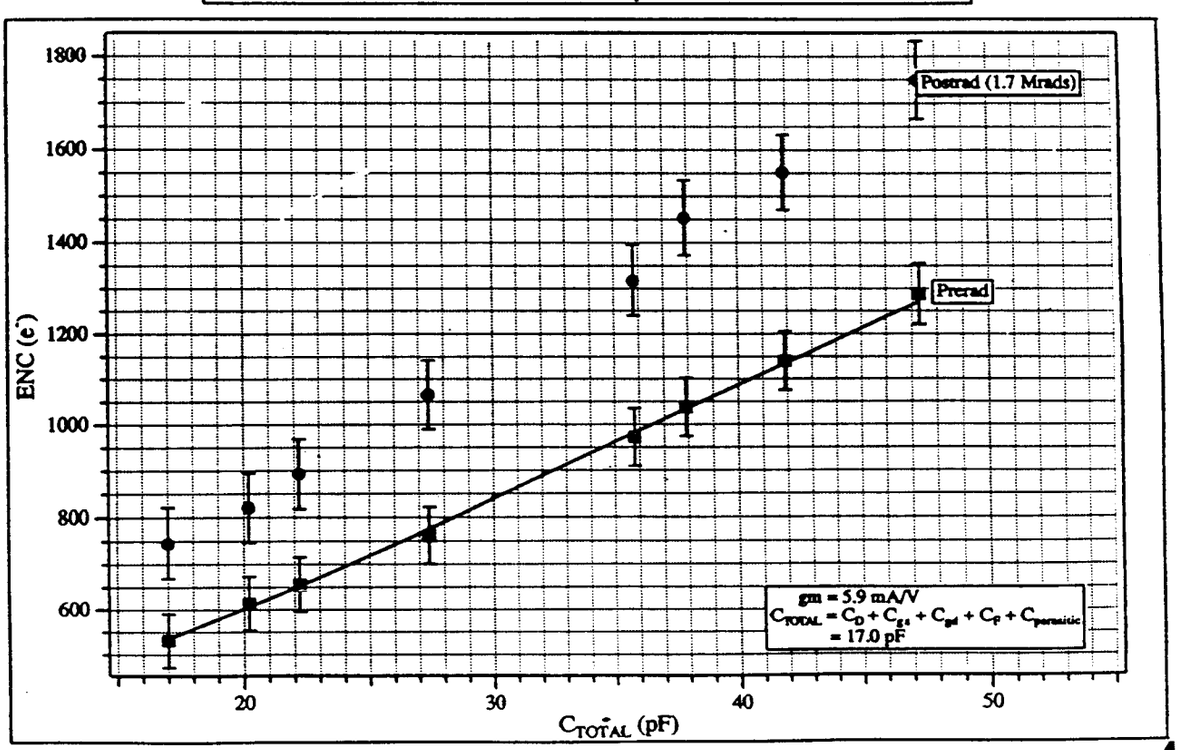
  PMOS: $K_f = 0.5 \times 10^{-12} \cdot V^2 pF$

  NMOS: $K_f = 2.5 \times 10^{-12} \cdot V^2 pF$

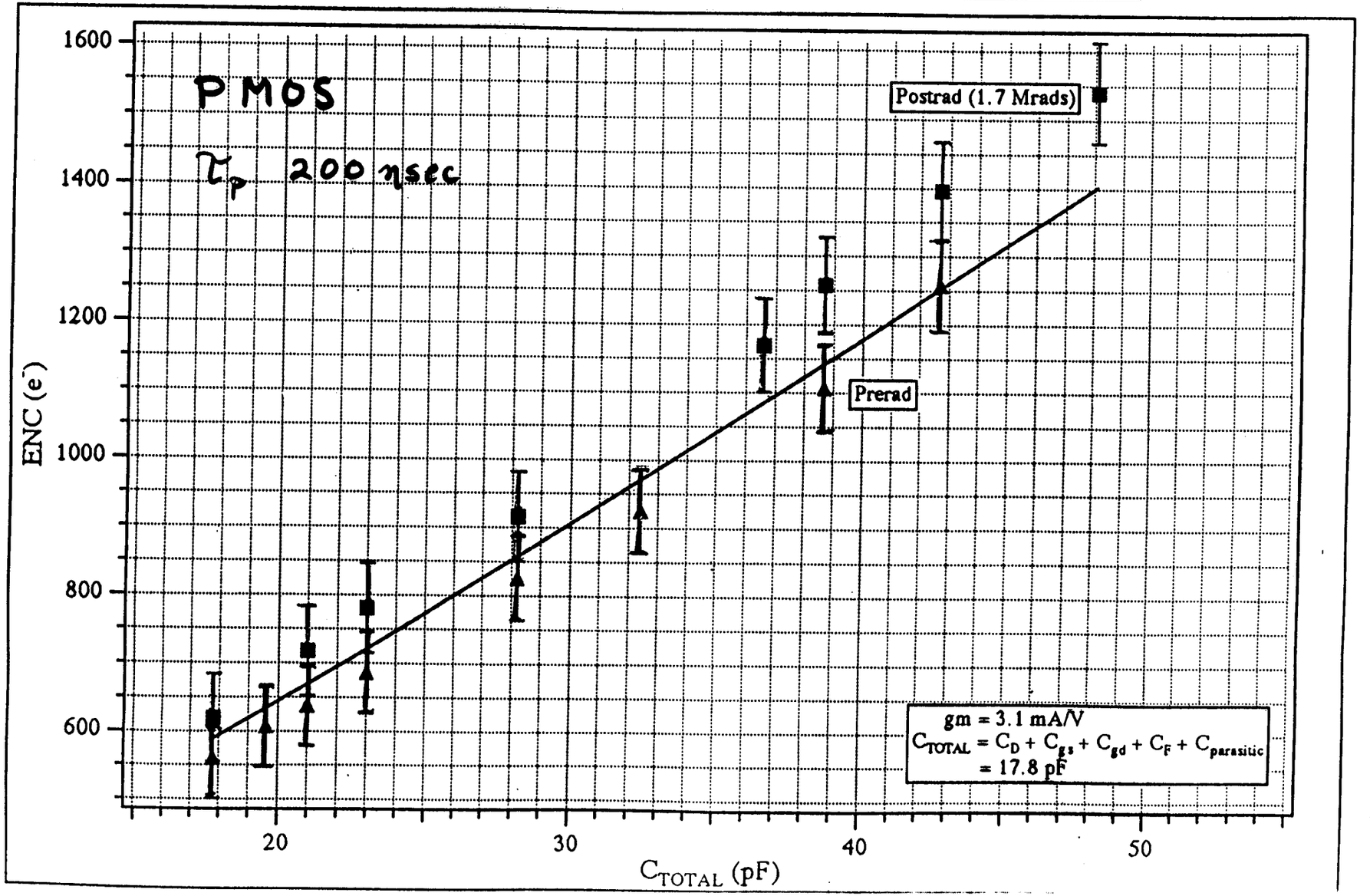
Noise Performance of UTMC NMOS devices
ENC vs. Total Capacitance before and after 1.7 Mrads. radiation
W/L = 2664/2.2, I_D = 500 µA, T_p = 500 ns, V_{DS} = 2.0 V



Noise Performance of UTMC NMOS devices
ENC vs. Total Capacitance before and after 1.7 Mrads. radiation
W/L = 2664/2.2, I_D = 500 µA, T_p = 200 ns, V_{DS} = 2.0 V



Noise Performance of UTMC PMOS devices
ENC vs. Total Capacitance before and after 1.7 Mrads. radiation
W/L = 1332/3.2, I_D = 500 µA, T_p = 200 ns, V_{DS} = - 2.0 V



Extraction of Noise Coefficients

- Multiparameter Fit -

  $C_{Total} = C_D + C_{gs} + C_F + C_{inj} + C_{parasitic}$
  g_m
  τ_P
  Area = WL
  $R_F = 111M\Omega$

- Devices of equal L fit simultaneously

Thermal Parallel

$$ENC^2 = \frac{1}{2} \cdot kTe^2 C_{Total}^2 \left[\varepsilon \cdot \frac{1}{g_m \cdot \tau_p} + K_f \cdot \frac{1}{C_{ox}} \cdot \frac{1}{W \cdot L} \cdot \frac{1}{kT} \right] + \frac{1}{2} \cdot kTe^2 \frac{\tau_P}{R_F} + Floor$$

1/f Floor

Digital Readout of Silicon Strips

K. Shankar

Charge Readout of Silicon Strips

1. Preamp/Shaper/Comparator with adequate noise feasible @ **< 1mW**
   $C_D < 8$–10 pF with CMOS
   < 15 pF with Bipolar

2. Rutherford Lab (Paul Seller, Peter Murray ...) have developed logic for level 1, level 2 virtual storage which is:
   reasonably compact
   runs at 60 MHz

3. Appears possible to have 3 μsec storage in 2 mm length, ≈ 6 μm pitch.

4. Jarron et al, with current amp have obtained: large dynamic range ≈ 12 bits
   8 nsec peaking
   (however more power, noise than we want

5. Not much attention has yet been given to readout; but no obvious problem.
   ADC / channel may even be feasible
   e.g. 100 μ × 200 μ, 40 μW for comparator.

Potential problem: lack of double poly in radiation hard process.

Charge Readout of Silicon Strips

N. Spencer

—— PRELIMINARY RESULTS ——

NOISE IN CMOS TRANSISTORS

- Ned Spencer

UCSC

W. Dabrowski
M. Turala
M. Kajatanowicz
P. Tanenbaum
M. Wilder
W. Rowe
E. Spencer
H. Sadrozinski

SSC SILICON TRACKER FRONT END
MOSFET VOLTAGE NOISE ESTIMATES

SPENCER NOISE 1

TEST STRUCTURE DEVELOPED AT U. PENN OF WIDE CMOS TRANSISTORS, IN UTMC 1.2 μm ℒ

8 STRUCTURES CHOSEN: 4 NMOS 4 PMOS

W/L (μm)	
1332 / 3.2	INTERDIGITATED
888 / 2.4	" "
1332 / 1.2	" "
1138 / 1.2	WAFFLE

I WILL CONCENTRATE ON THE 4 STRUCTURES OF 1332/3.2 (W/L) AND 1332/1.2 (W/L) IN THIS DISCUSSION

$V_{DS} = 1.2$ VOLTS

TO MEASURE NOISE WE USE AN HP 4195 SPECTRUM/NETWORK ANALYZER

75/1.2 μm STRUCTURE BY LBL WAS ALSO TESTED BECAUSE WE HAD EXPERIENCE WITH THIS STRUCTURE IN AN EARLIER RUN.

CMOS OF SAME GEOMETRY BUT DIFFERENT WIDTH SCALE IF CURRENT DENSITY IS THE SAME. CURRENT DENSITY $\triangleq \frac{I_D}{W}$

WE CHOSE 3 I_D/W RATIOS OF

0.03	40 μA	@ W = 1332 μm
0.1	133 μA	"
0.3	400 μA	"

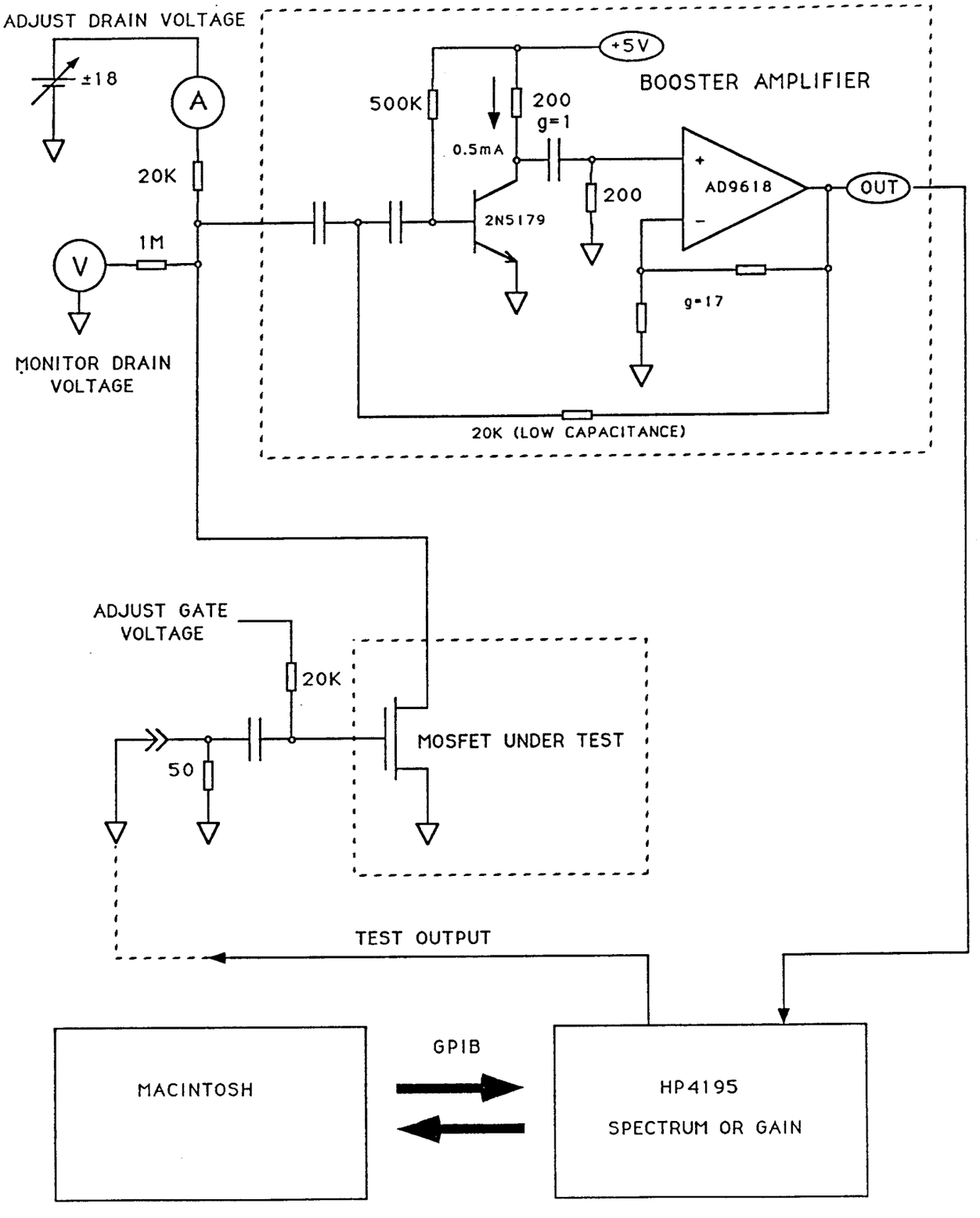
THESE VALUES ARE USEFUL FOR ESTIMATING FRONT END TRANSISTOR NOISE AT LIKELY BIAS LEVELS.

WE HAVE SIX DATA POINTS TAKEN USING Co-60 GAMMA SOURCE AT UCSC

0
250 KRAD
500 KRAD
1 MRAD
2 MRAD
5 MRAD

SPENCER NOISE 3

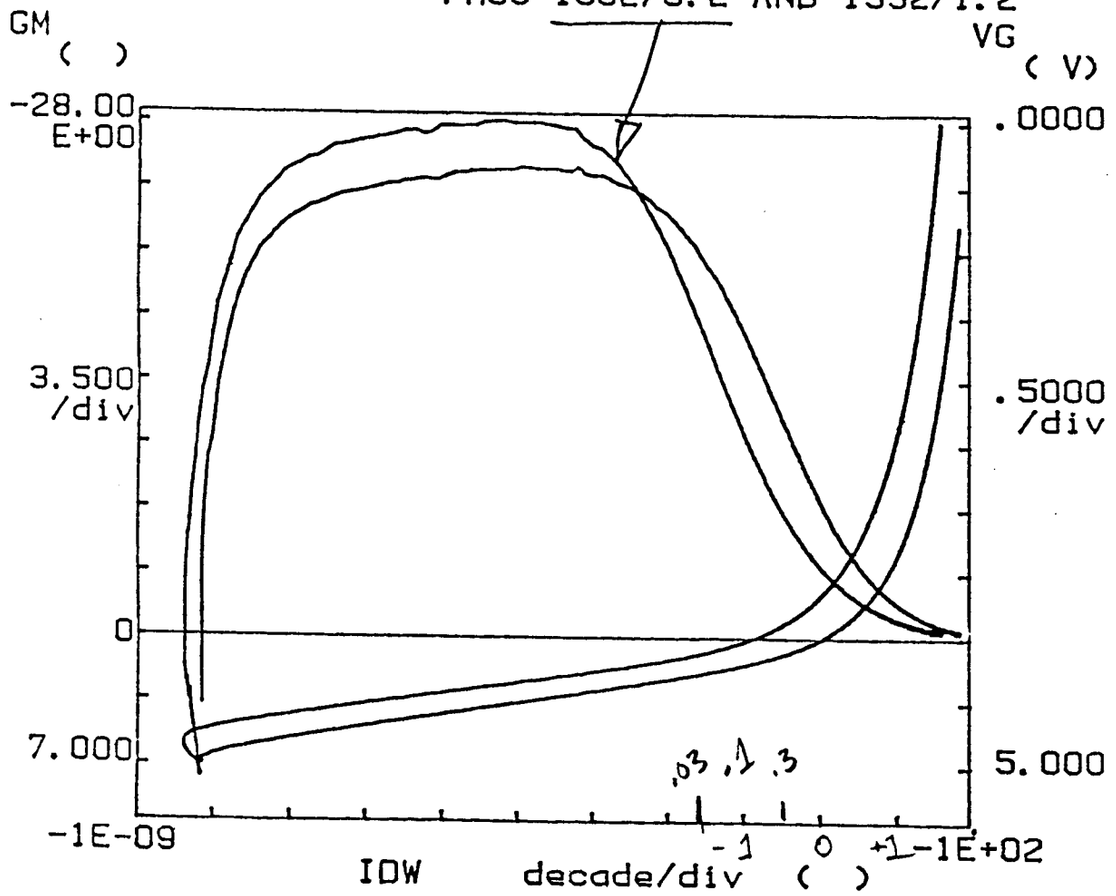
NOISE TEST CONFIGURATION



zero Rad

****** GRAPHICS PLOT ******

PMOS 1332/3.2 AND 1332/1.2

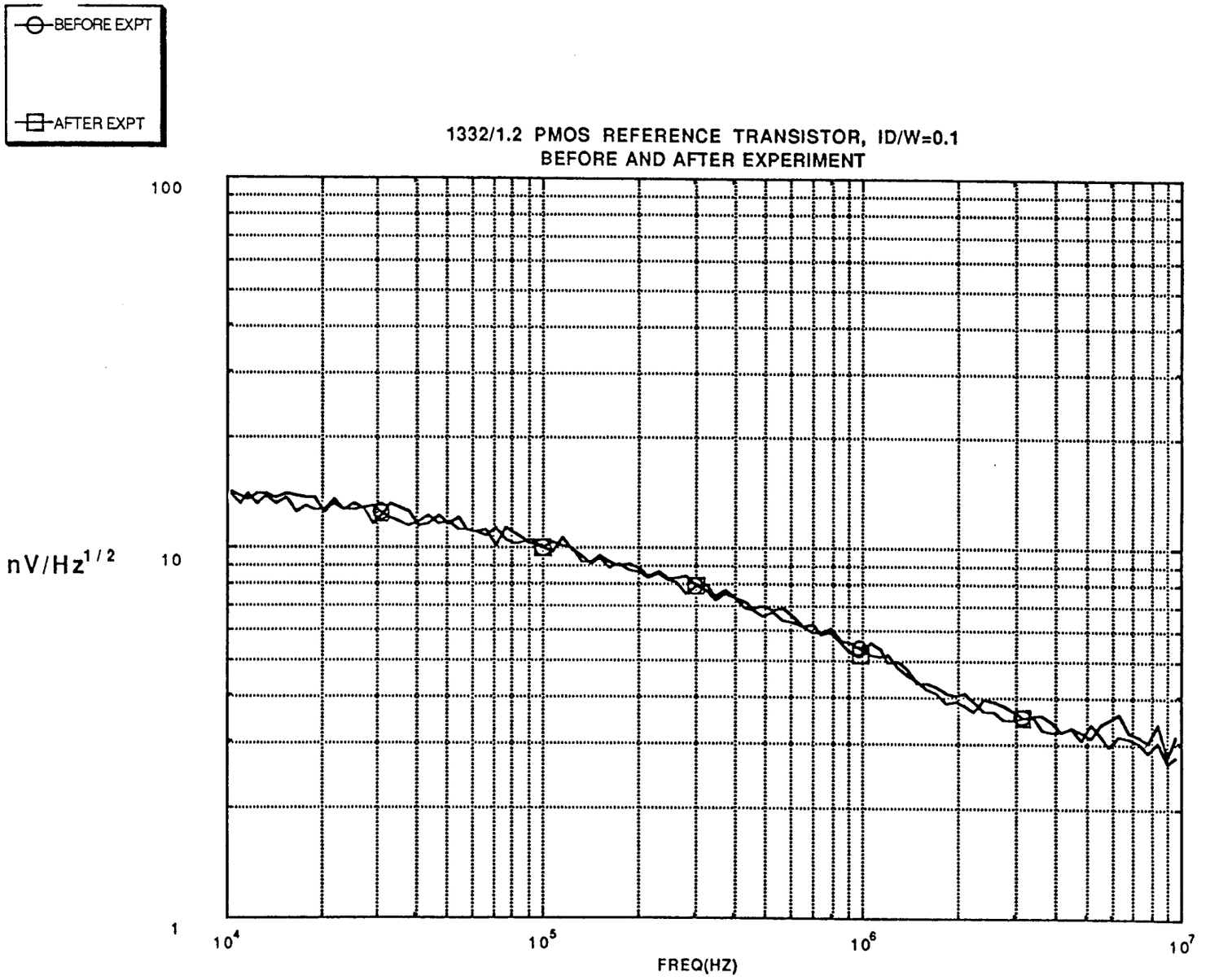


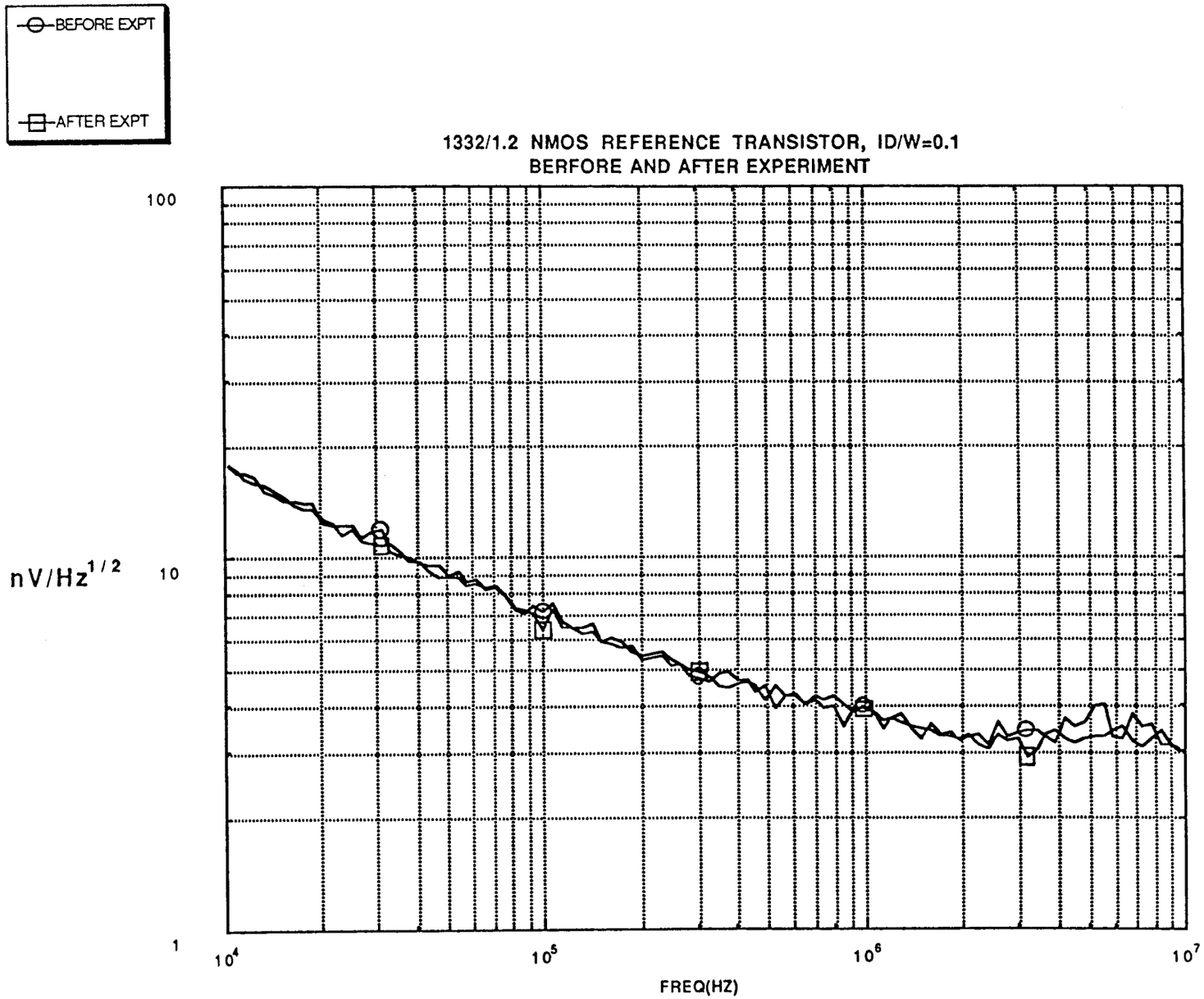
Variable1:
VG -Ch3
Linear sweep
Start 5.0000V
Stop .8000V
Step -.0100V

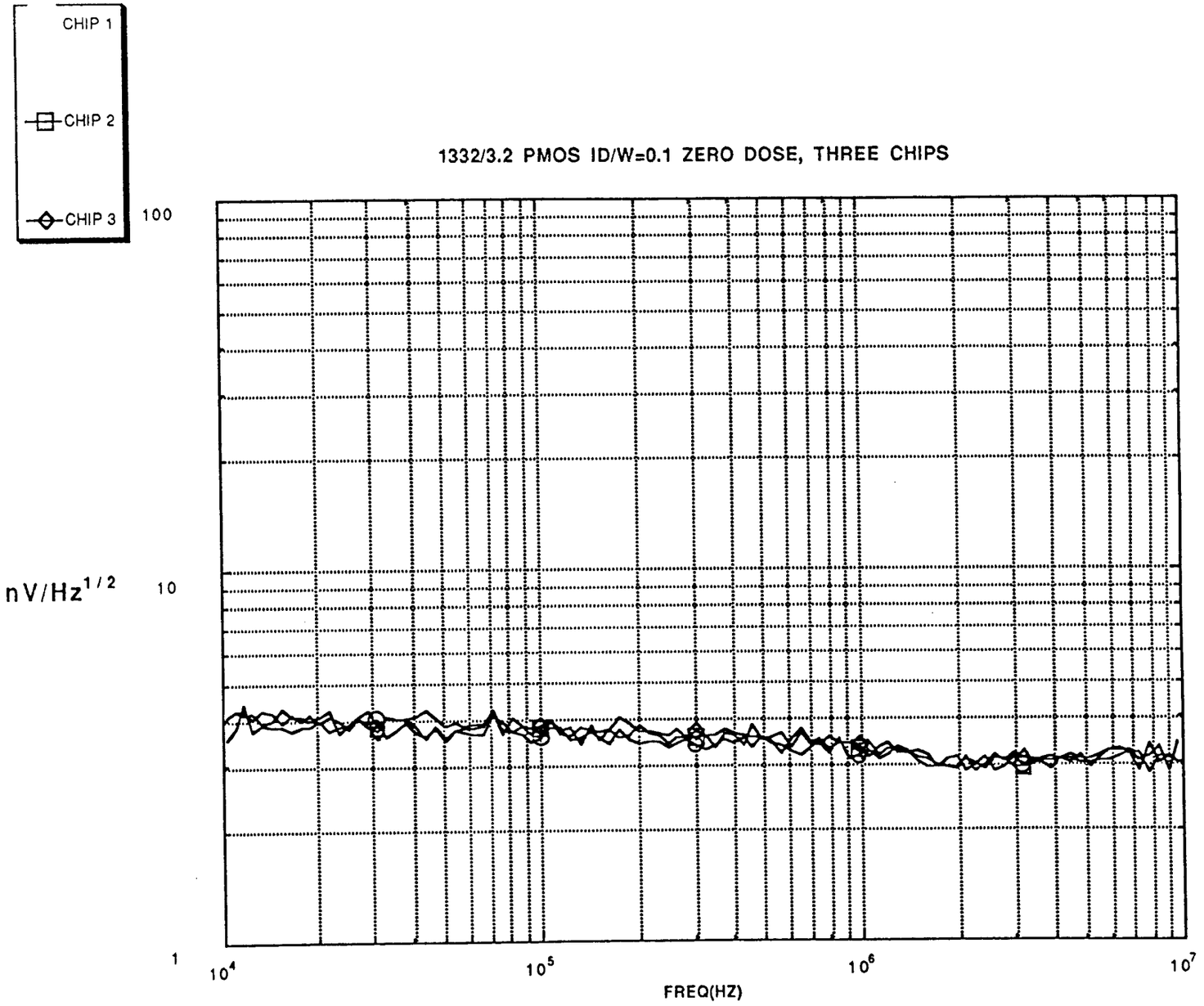
Constants:
VDS -Ch1 .0000V
VSO -Ch2 5.0000V
VSU -Ch4 5.0000V

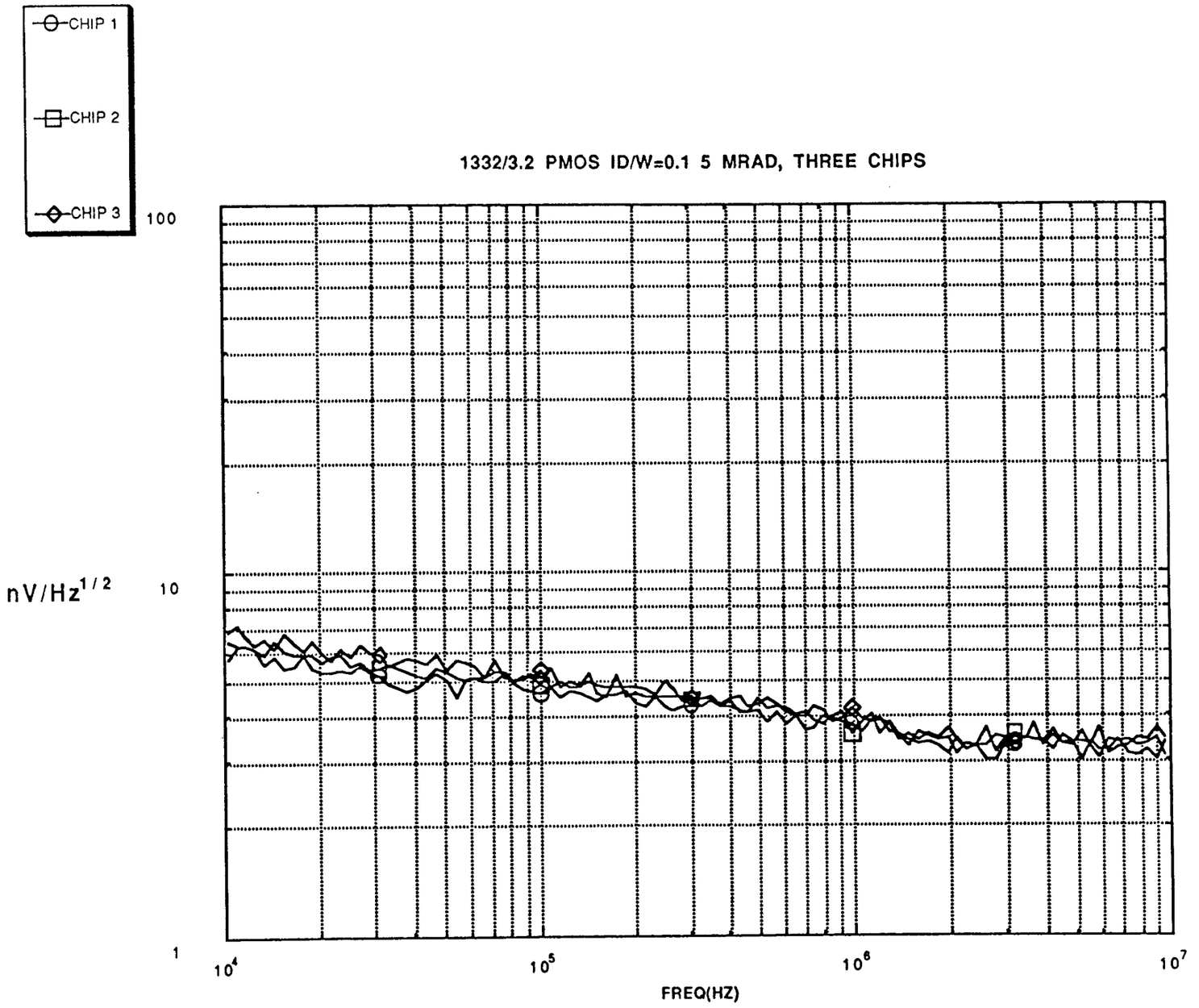
IDW ( ) = IDS/.001332
GM ( ) = (ΔIDS/ΔVG)/IDS

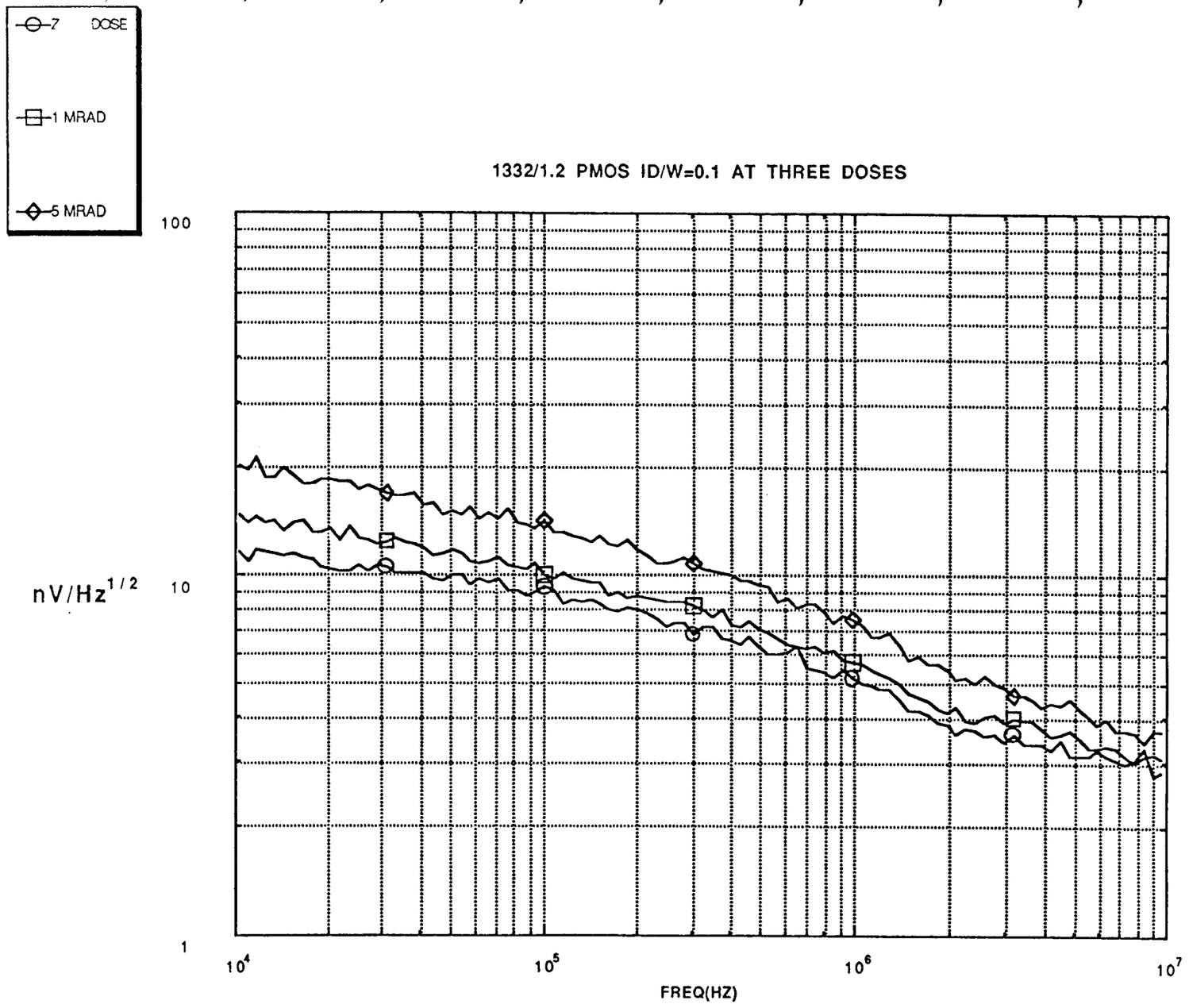
SPENCER NOISE 5

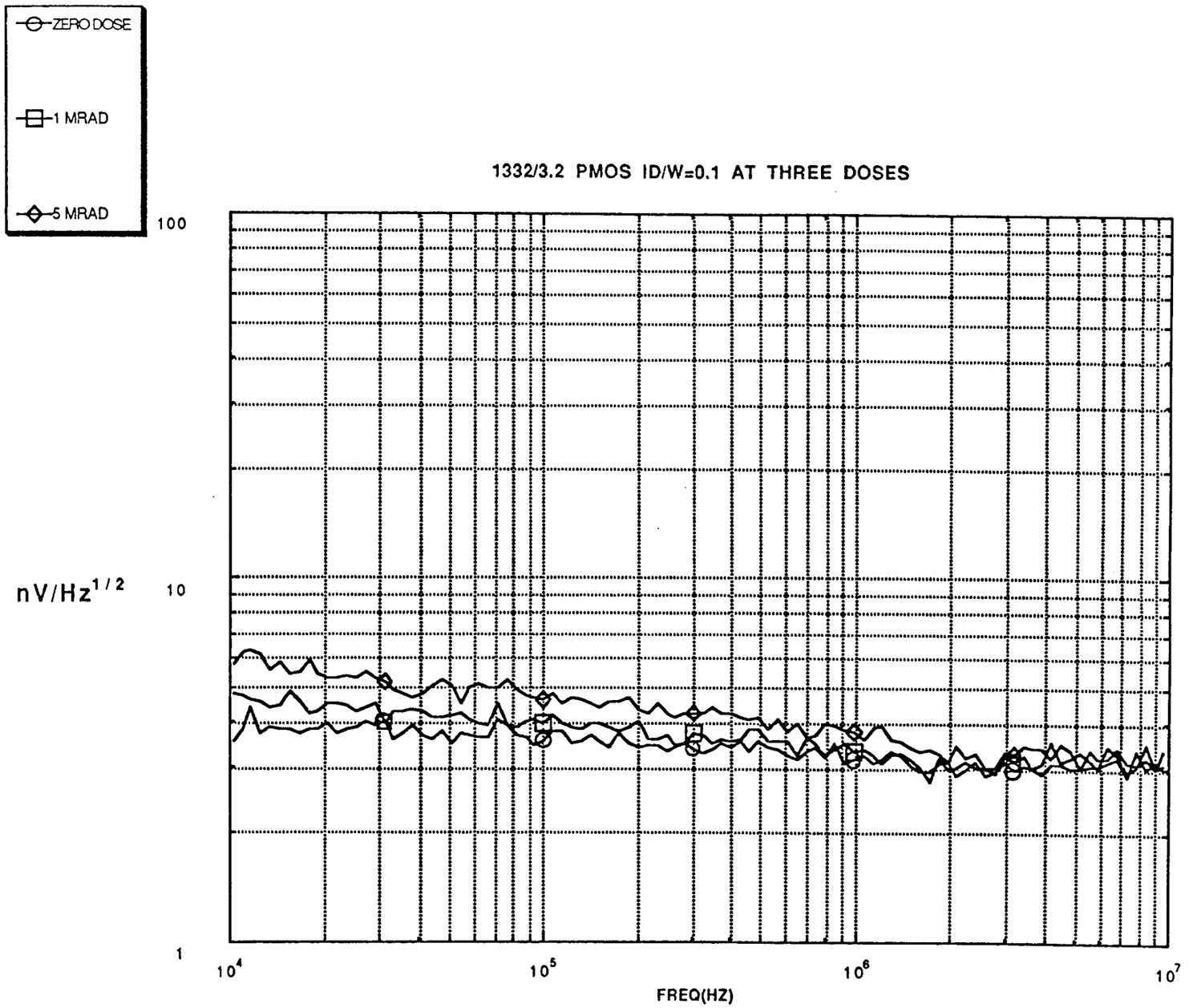

BEFORE EXPT
AFTER EXPT
1332/1.2 PMOS REFERENCE TRANSISTOR, ID/W=0.1
BEFORE AND AFTER EXPERIMENT
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

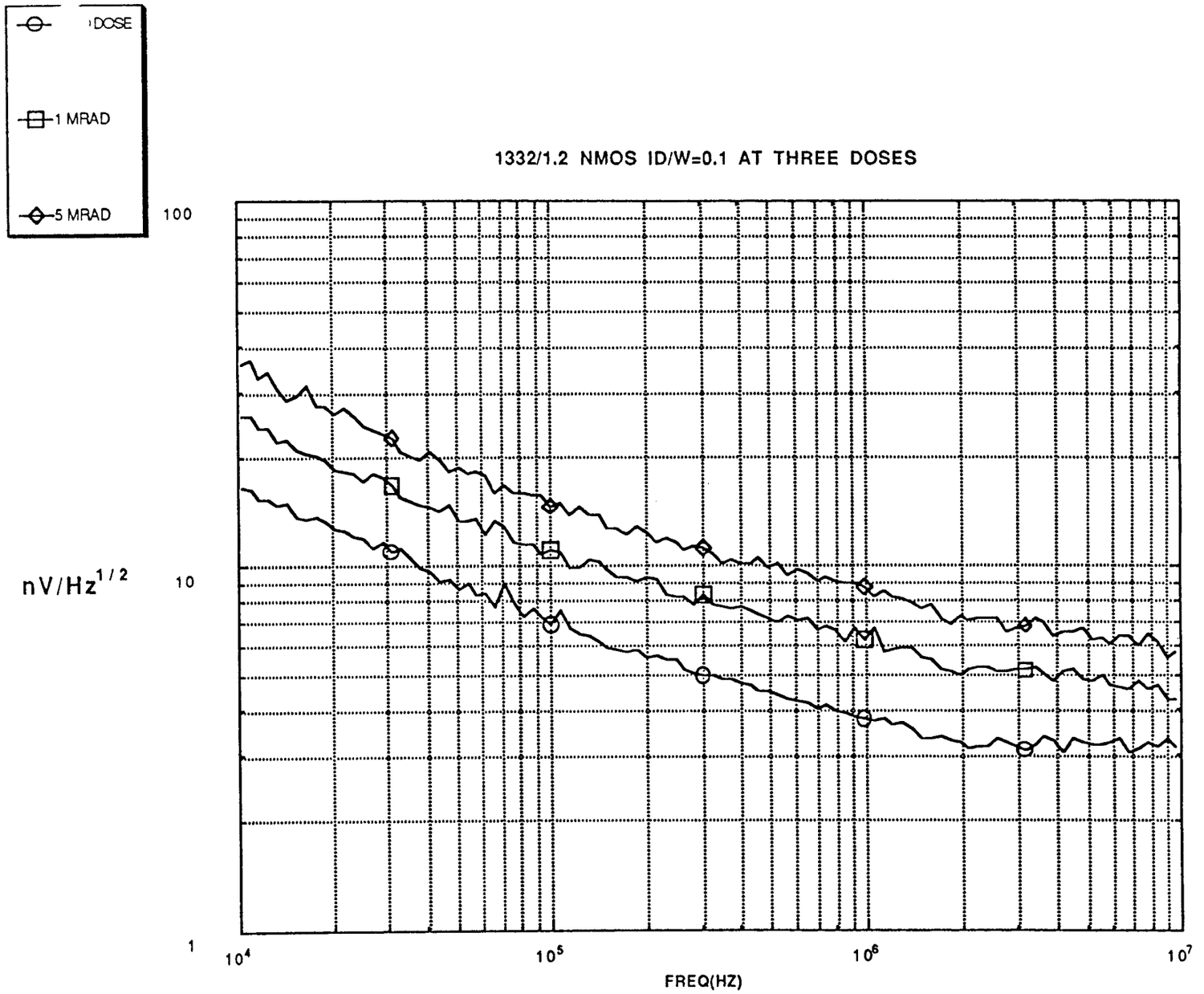

BEFORE EXPT
AFTER EXPT
1332/1.2 NMOS REFERENCE TRANSISTOR, ID/W=0.1
BERFORE AND AFTER EXPERIMENT
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

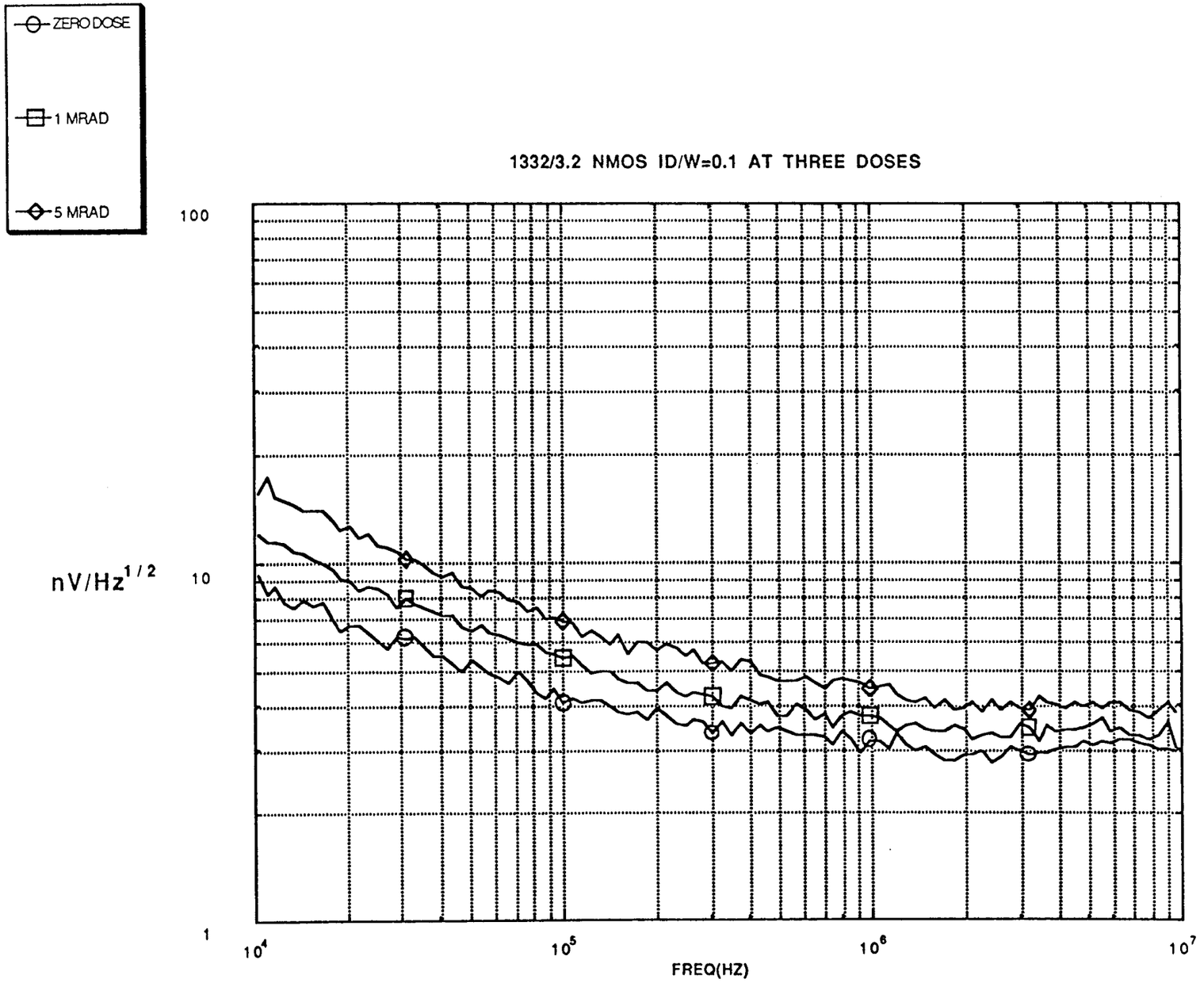

CHIP 1
CHIP 2
CHIP 3
1332/3.2 PMOS ID/W=0.1 ZERO DOSE, THREE CHIPS
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

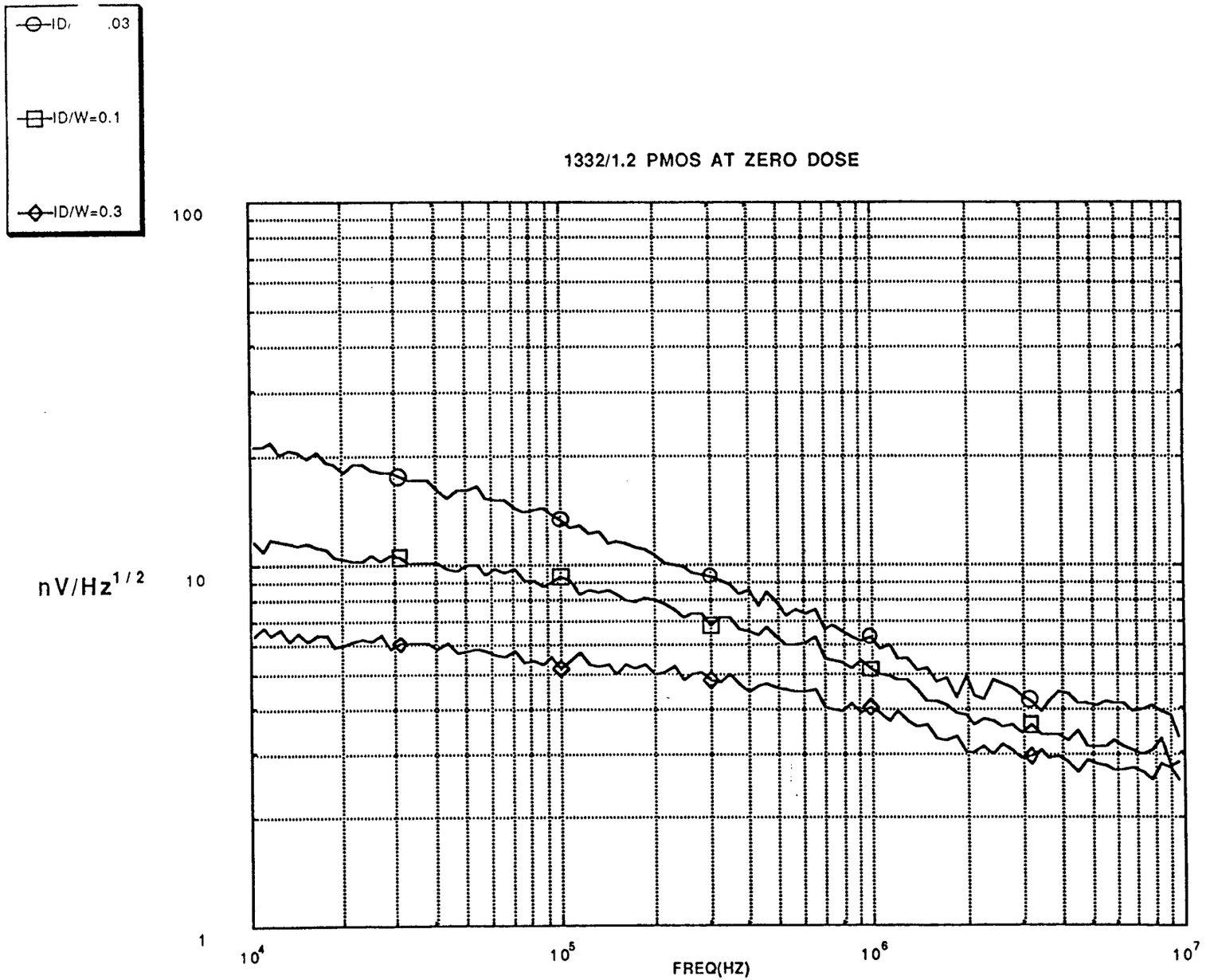

CHIP 1
CHIP 2
CHIP 3
1332/3.2 PMOS ID/W=0.1 5 MRAD, THREE CHIPS
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

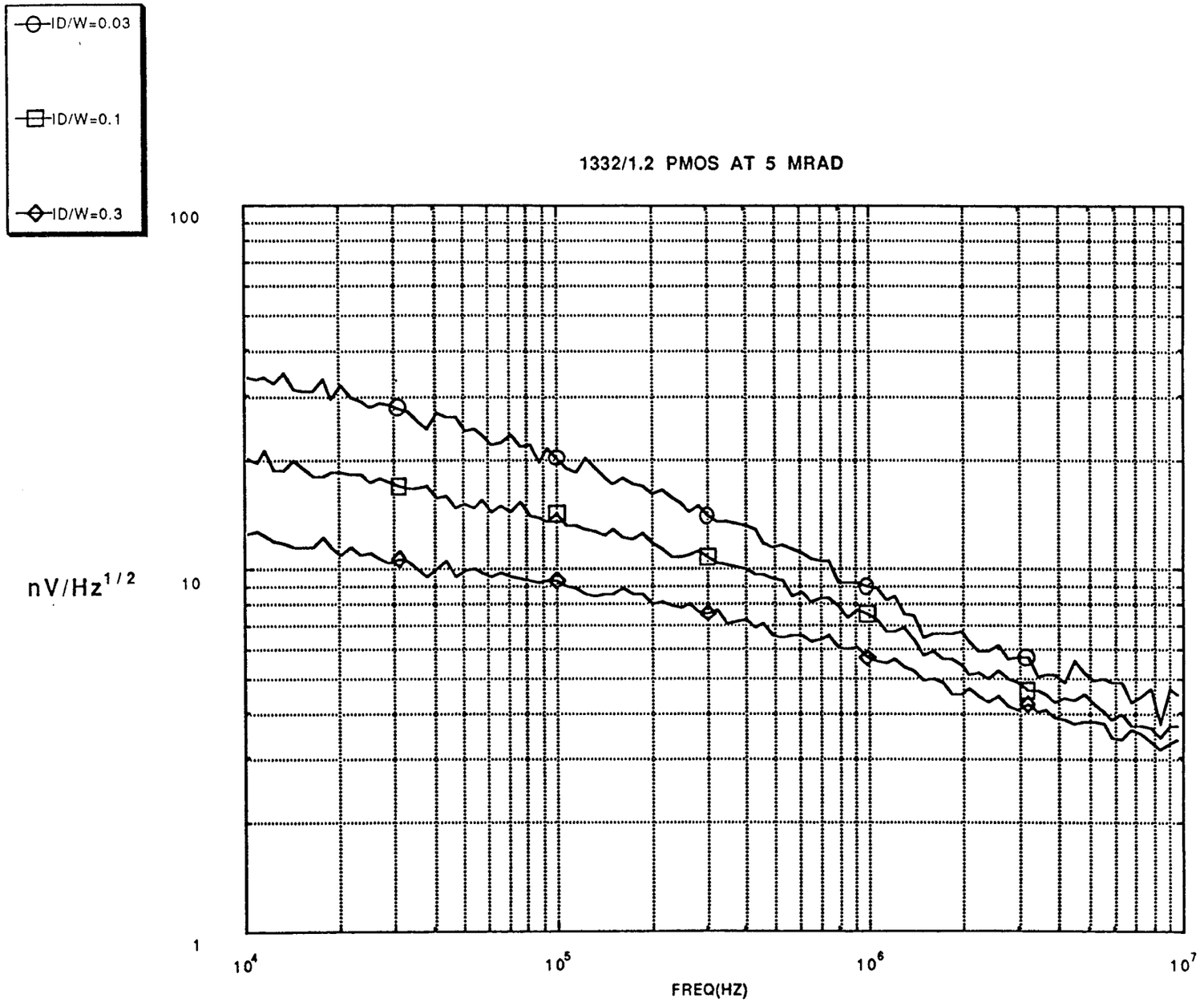

7 DOSE
1 MRAD
5 MRAD
1332/1.2 PMOS ID/W=0.1 AT THREE DOSES
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

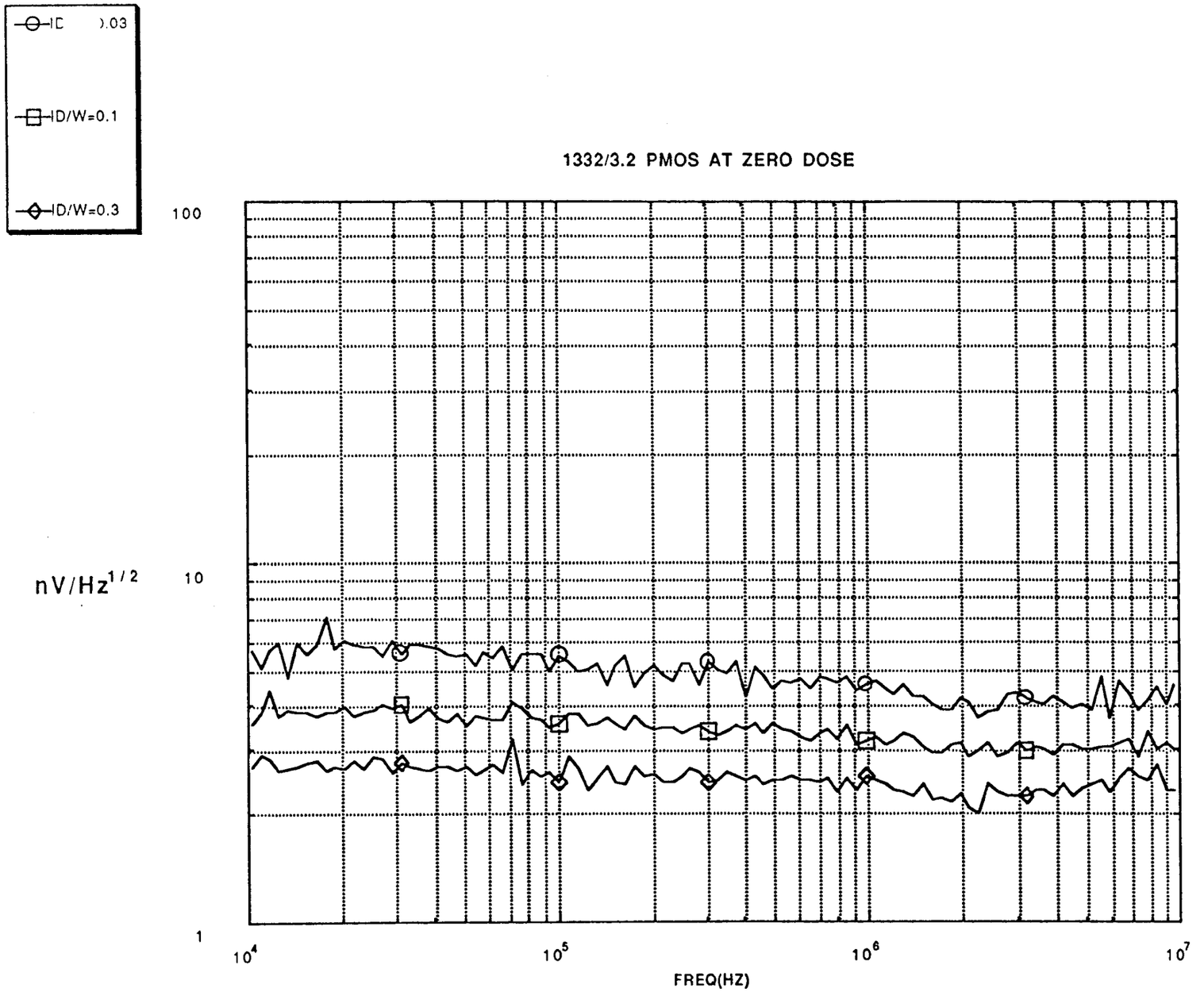

ZERO DOSE
1 MRAD
5 MRAD
1332/3.2 PMOS ID/W=0.1 AT THREE DOSES
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

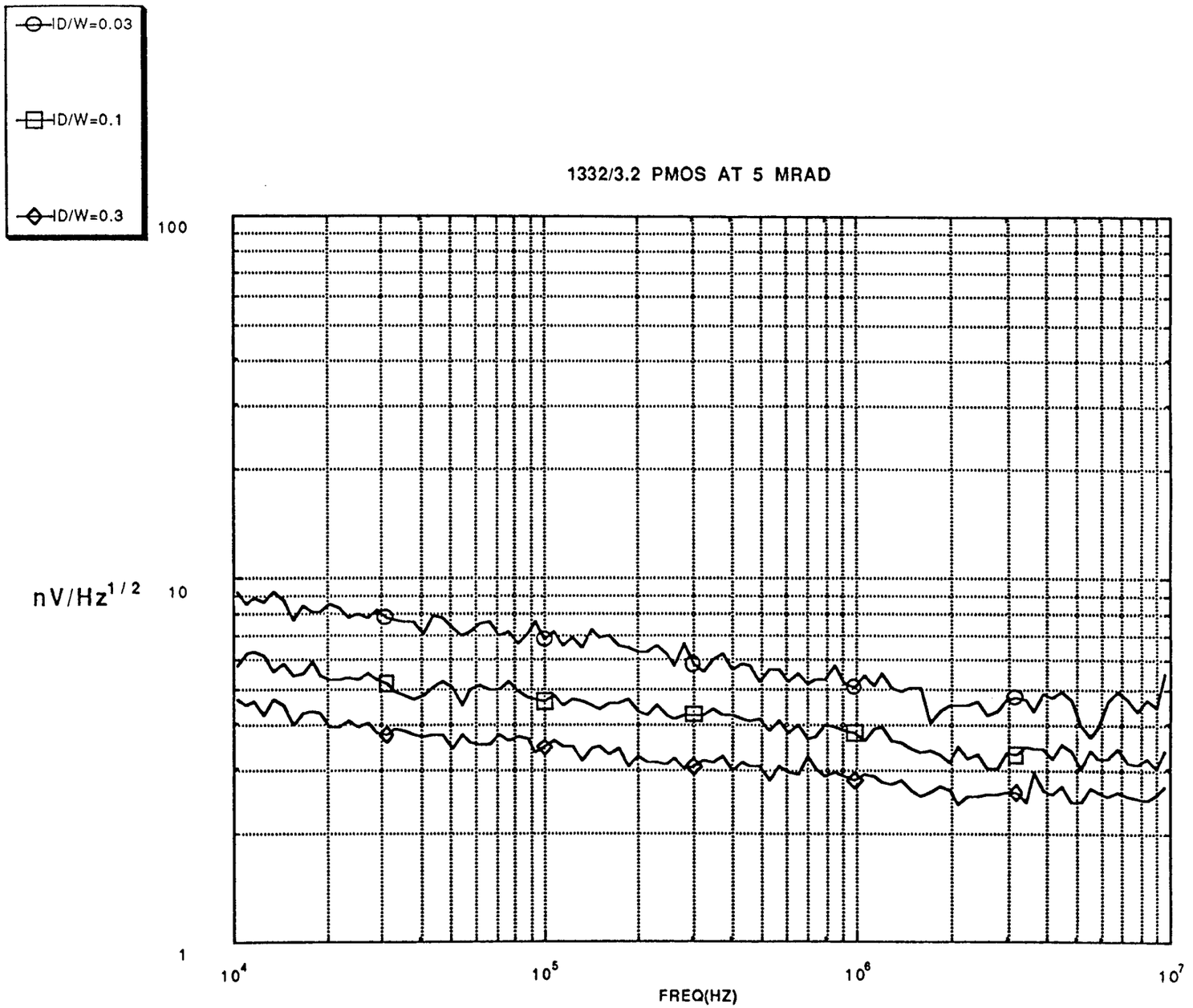

DOSE
1 MRAD
5 MRAD
1332/1.2 NMOS ID/W=0.1 AT THREE DOSES
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

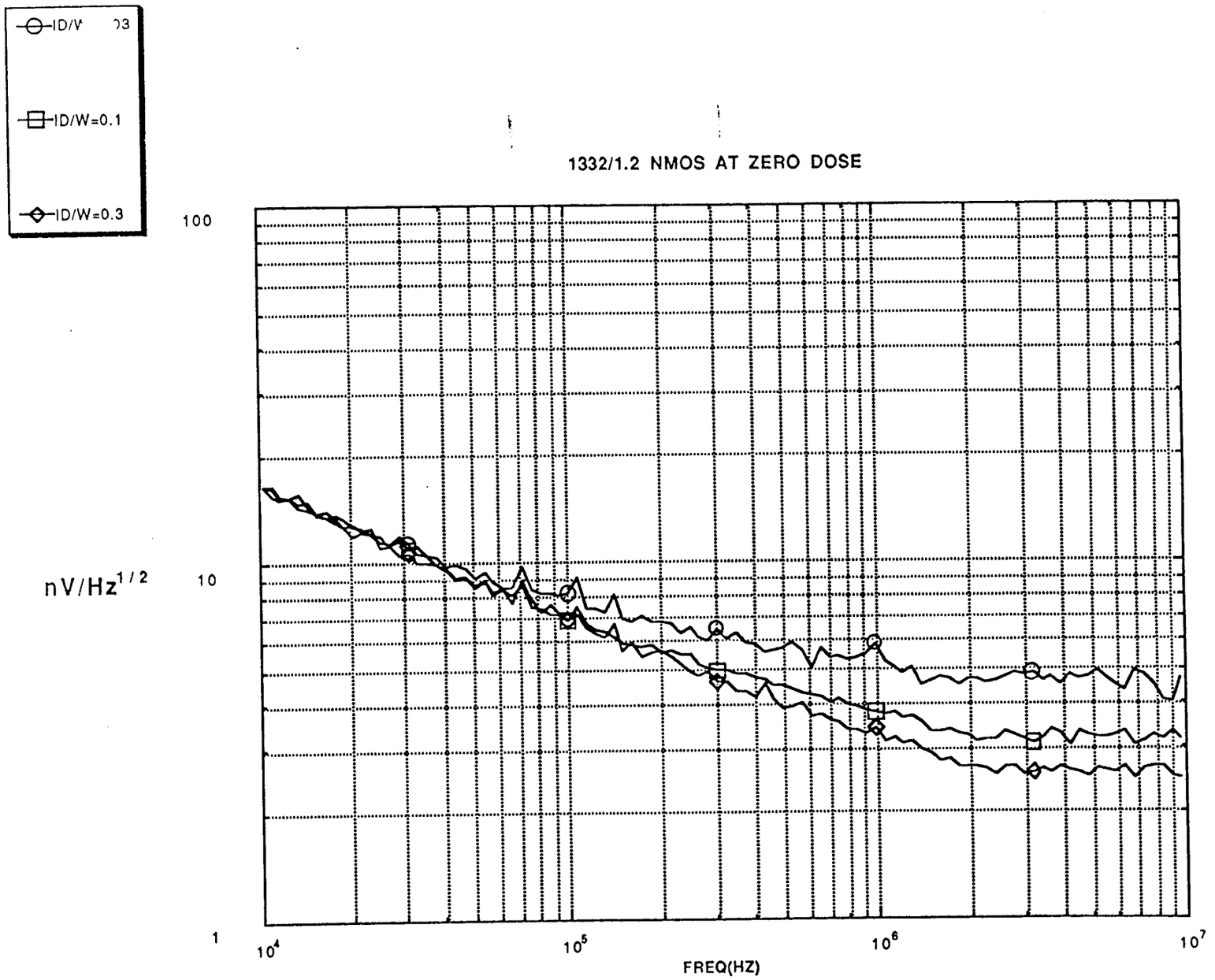

ZERO DOSE
1 MRAD
5 MRAD
1332/3.2 NMOS ID/W=0.1 AT THREE DOSES
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

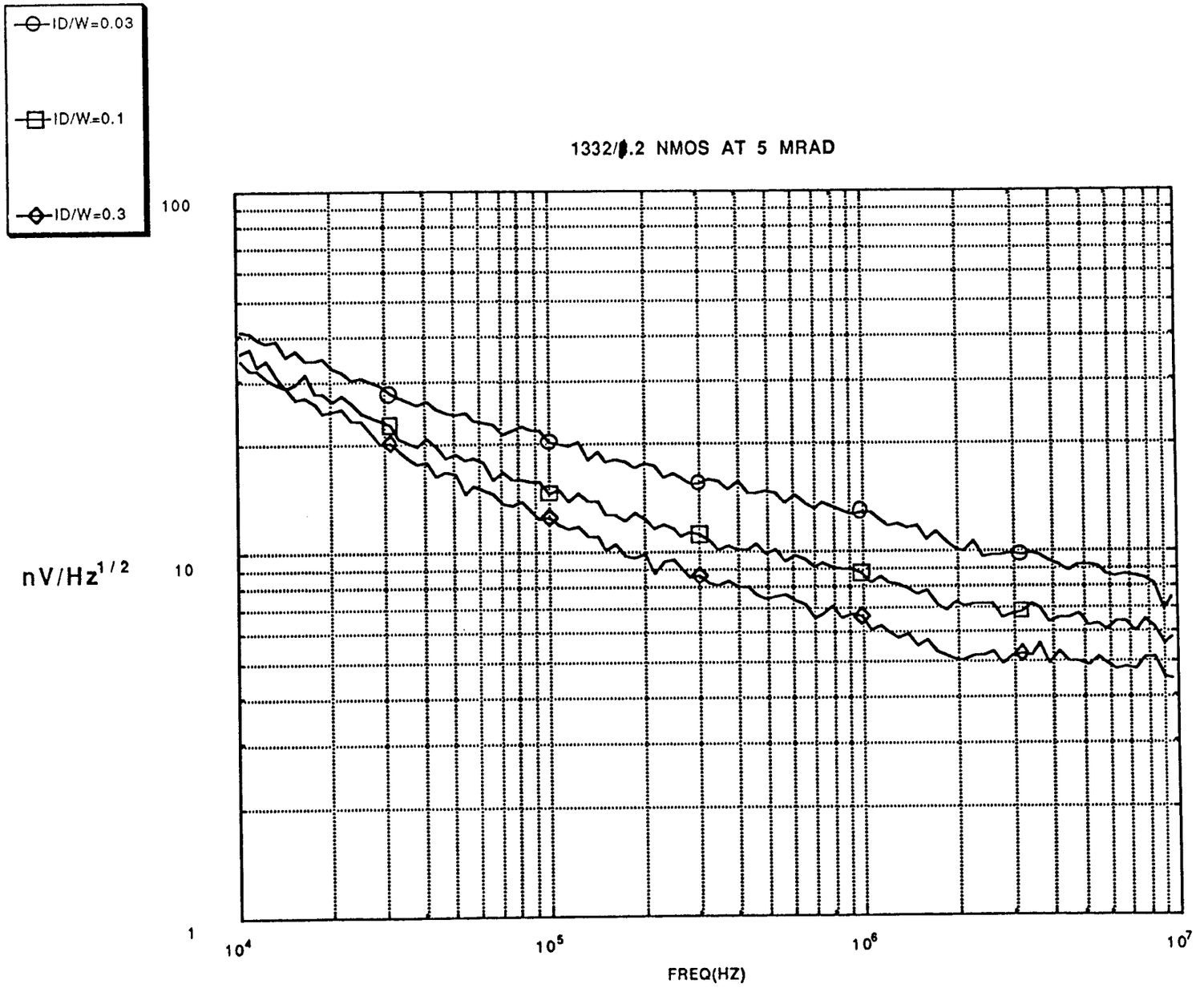

ID/ .03
ID/W=0.1
ID/W=0.3
1332/1.2 PMOS AT ZERO DOSE
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

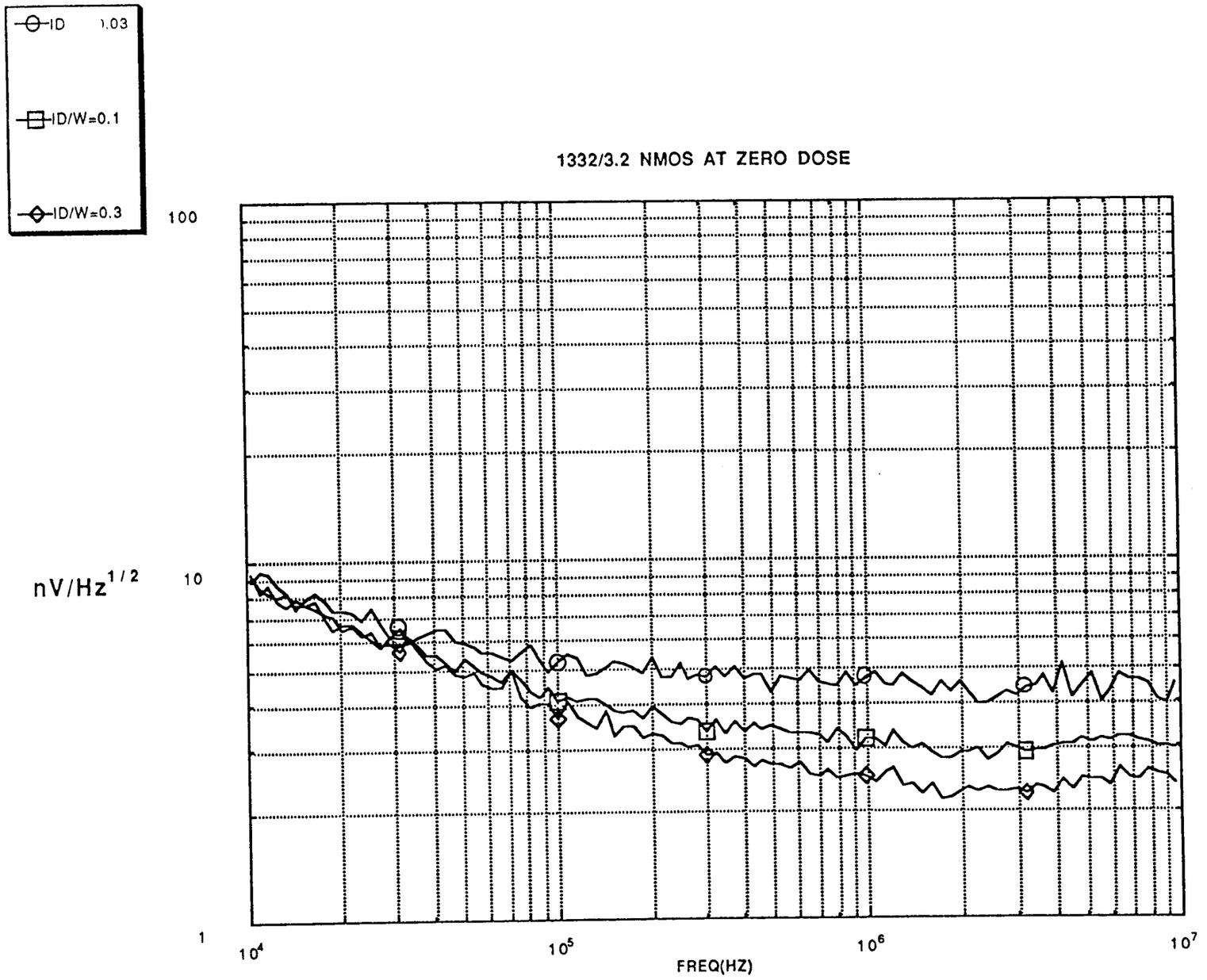

ID/W=0.03
ID/W=0.1
ID/W=0.3
1332/1.2 PMOS AT 5 MRAD
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

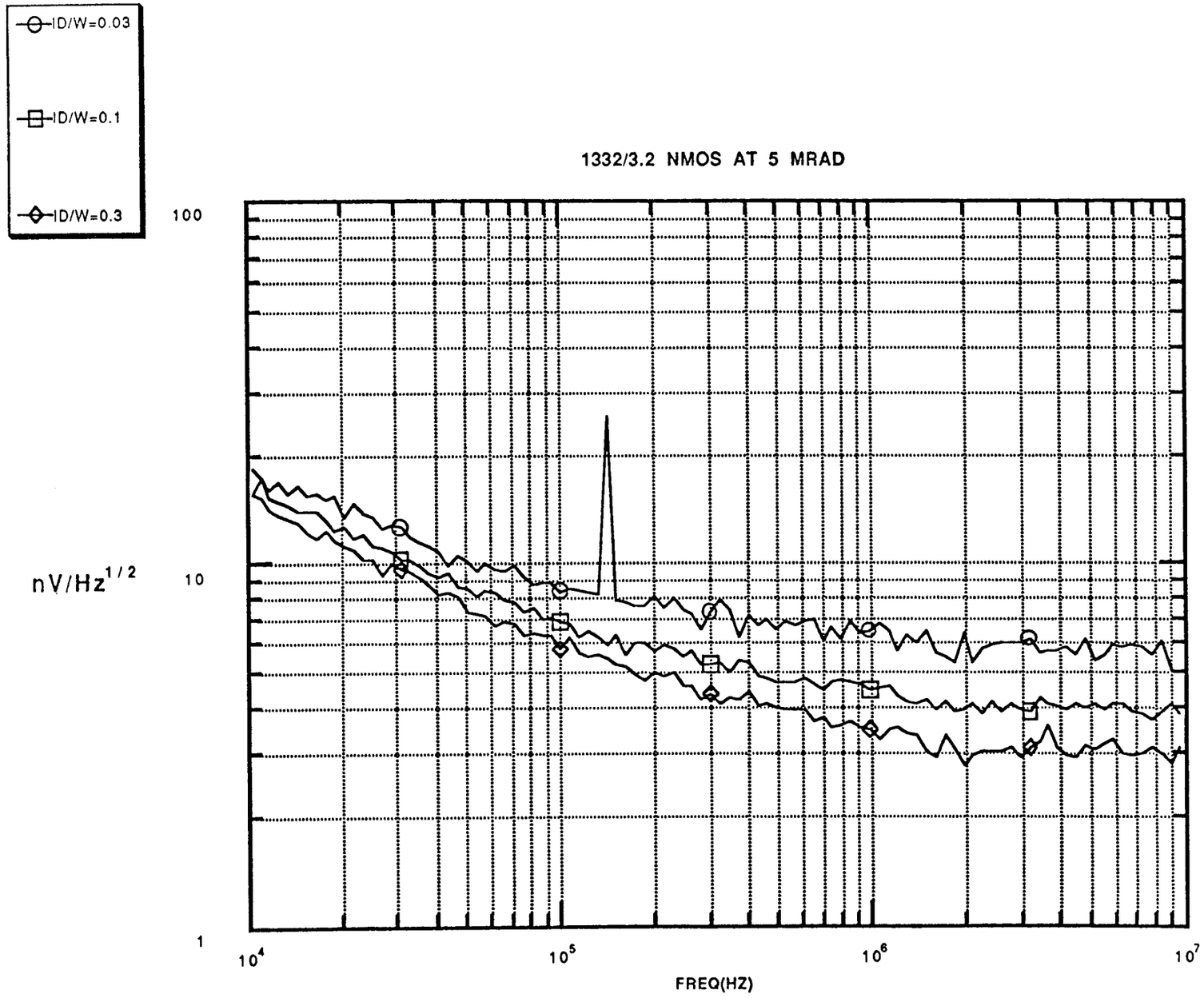

ID/W=0.03
ID/W=0.1
ID/W=0.3
1332/3.2 PMOS AT ZERO DOSE
nV/Hz^1/2
100
10
1
10^4
10^5
10^6
10^7
FREQ(HZ)

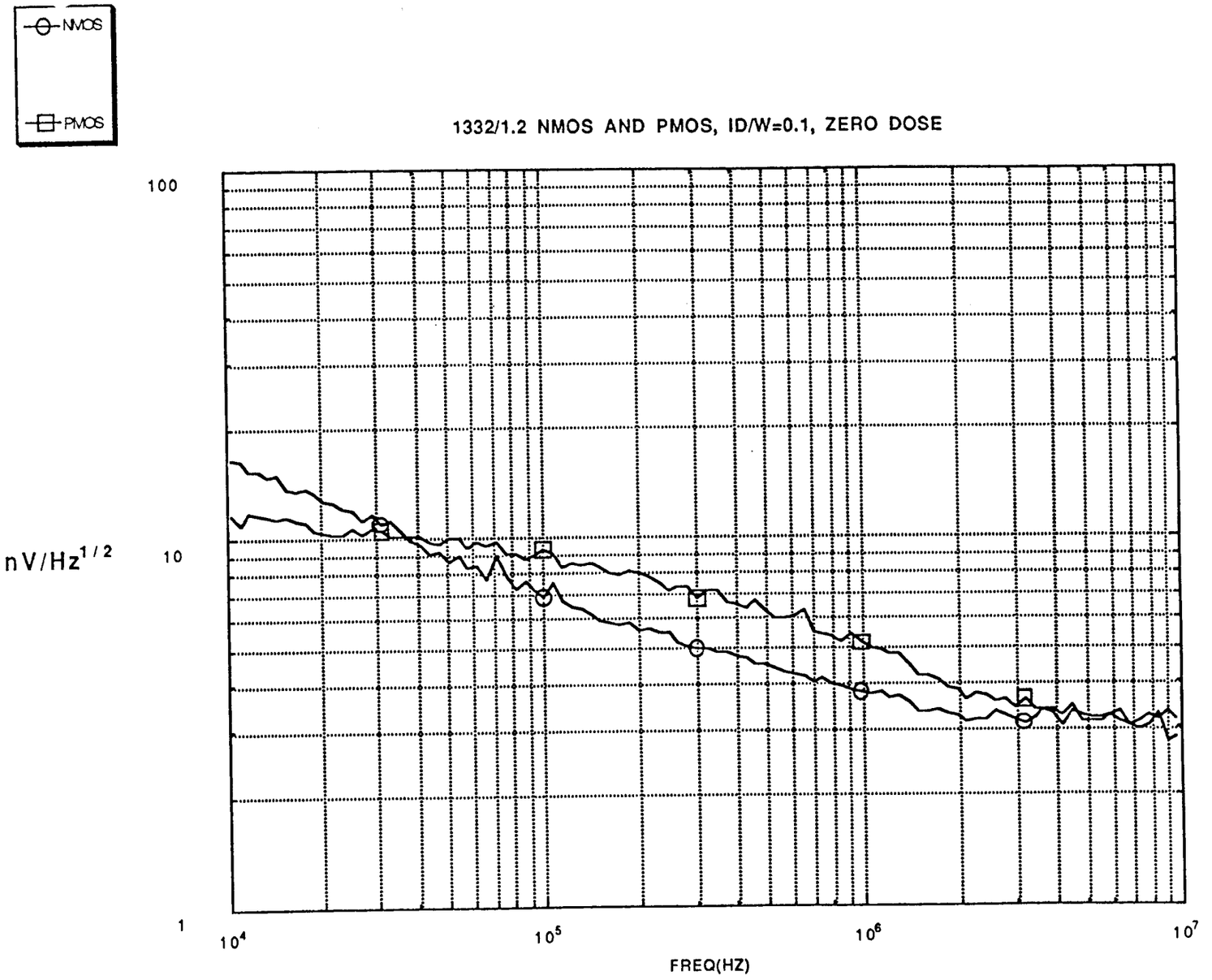

1332/3.2 PMOS AT 5 MRAD
ID/W=0.03
ID/W=0.1
ID/W=0.3
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

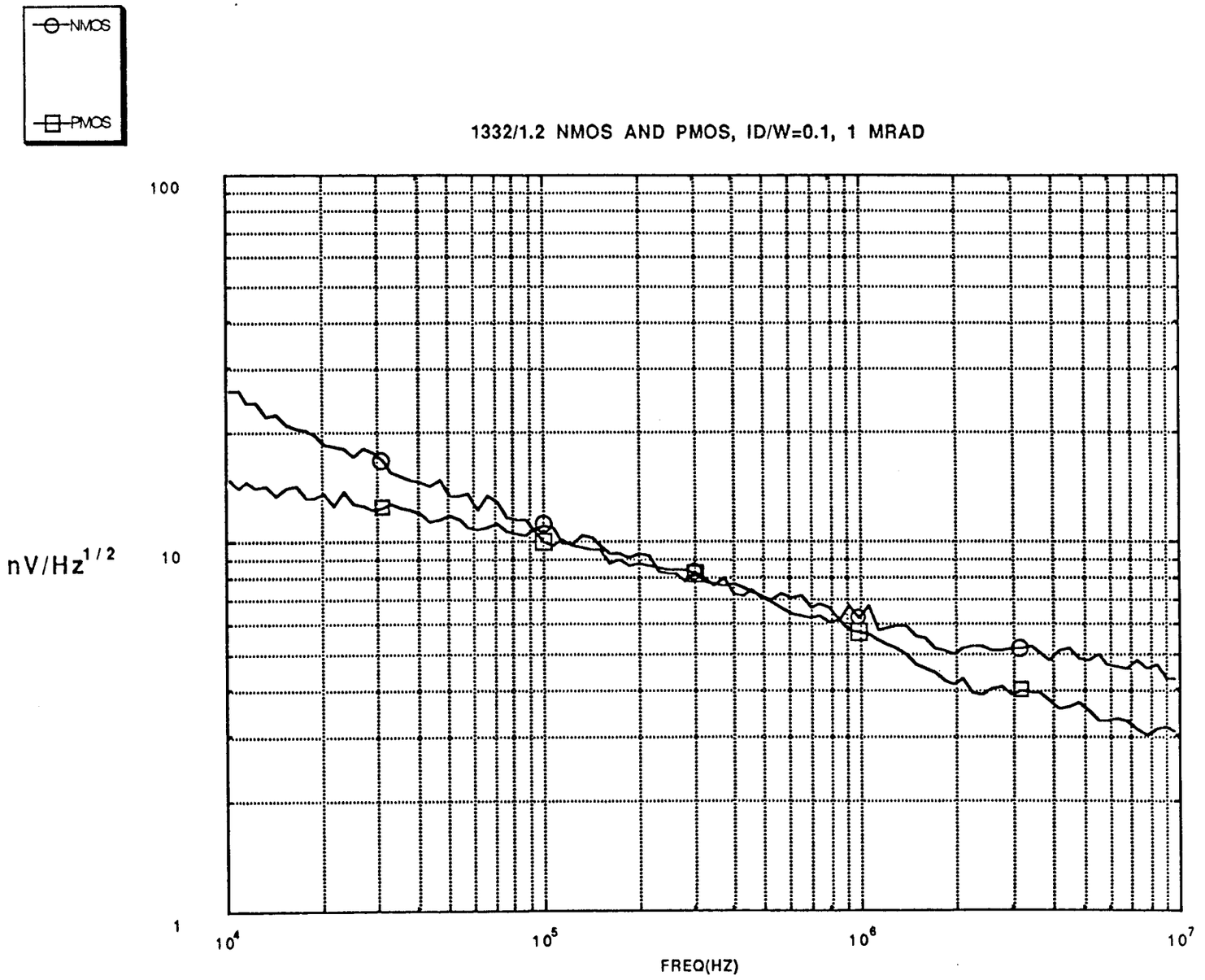

ID/W 03
ID/W=0.1
ID/W=0.3
1332/1.2 NMOS AT ZERO DOSE
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

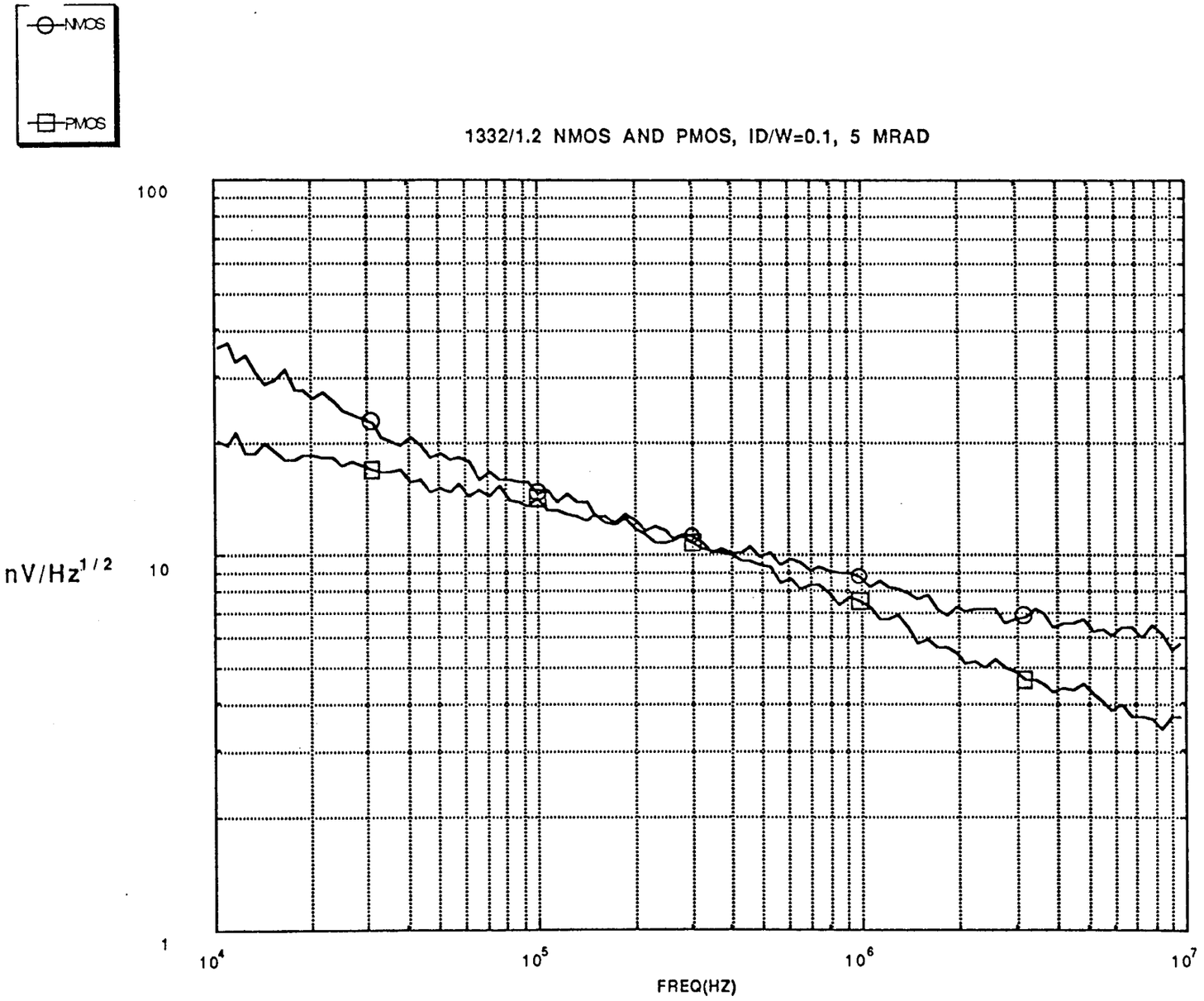

ID/W=0.03
ID/W=0.1
ID/W=0.3
1332/0.2 NMOS AT 5 MRAD
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)


ID 1.03
ID/W=0.1
ID/W=0.3
1332/3.2 NMOS AT ZERO DOSE
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)


ID/W=0.03
ID/W=0.1
ID/W=0.3
1332/3.2 NMOS AT 5 MRAD
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)


NMOS
PMOS
1332/1.2 NMOS AND PMOS, ID/W=0.1, ZERO DOSE
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)


NMOS
PMOS
1332/1.2 NMOS AND PMOS, ID/W=0.1, 1 MRAD
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)


NMOS
PMOS
1332/1.2 NMOS AND PMOS, ID/W=0.1, 5 MRAD
100
10
1
nV/Hz^1/2
10^4
10^5
10^6
10^7
FREQ(HZ)

Protocols/Requirements for DAQ

E. Barsotti

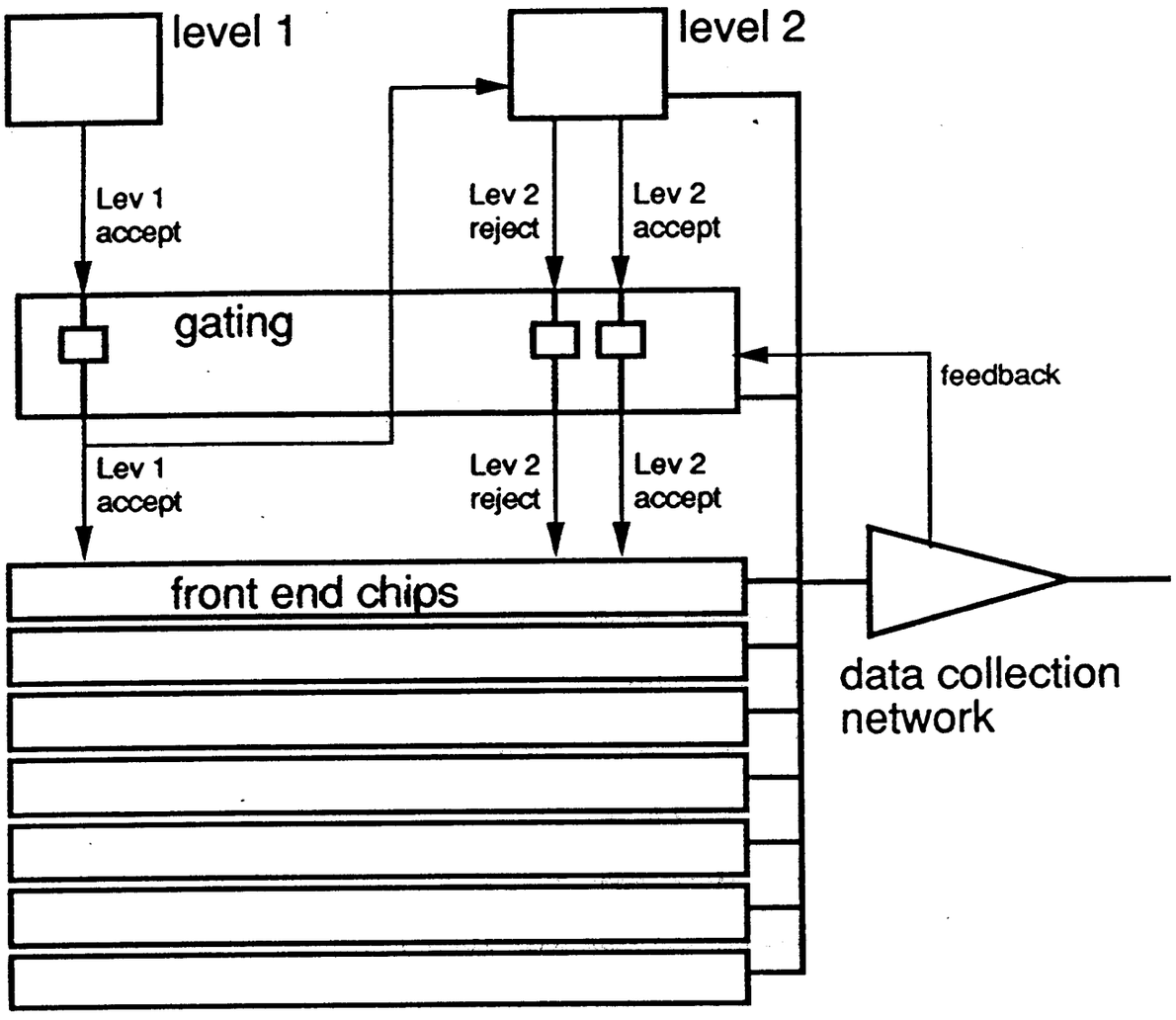
A "Baseline" DAQ System

E. Barsotti

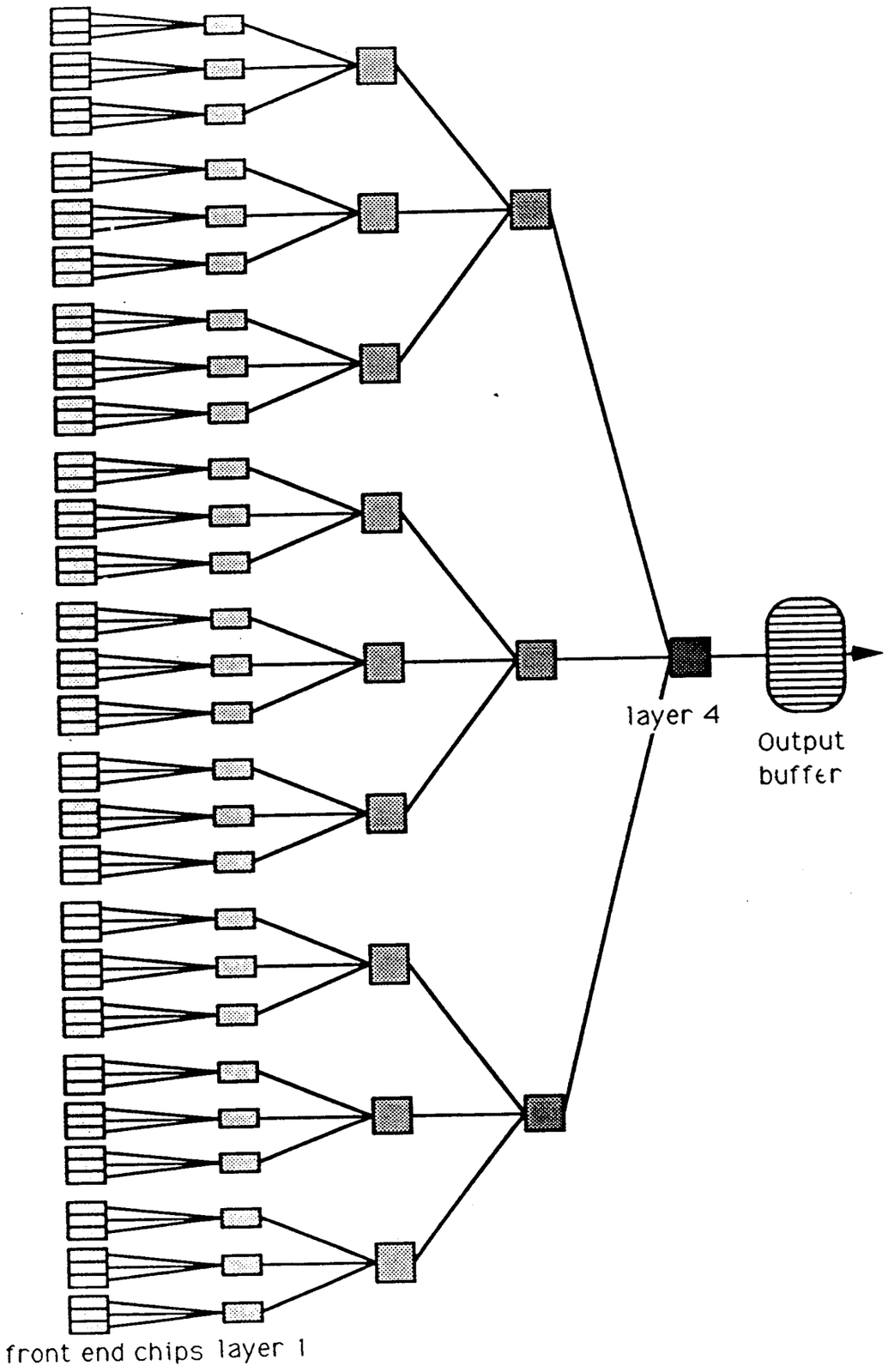
Status of DAQ Simulations

J. Dorenbosch

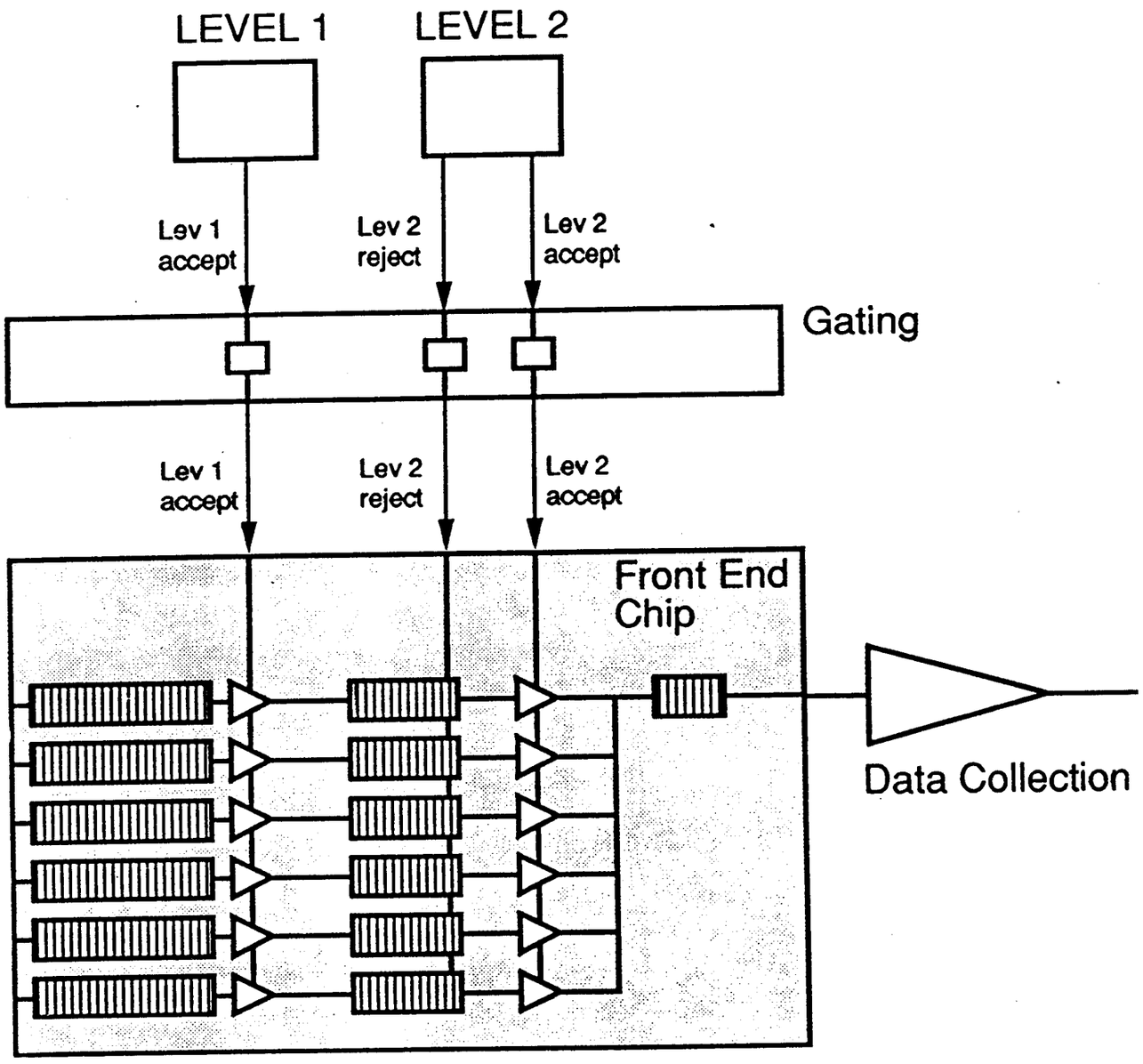
MODSIM data acquisition simulations



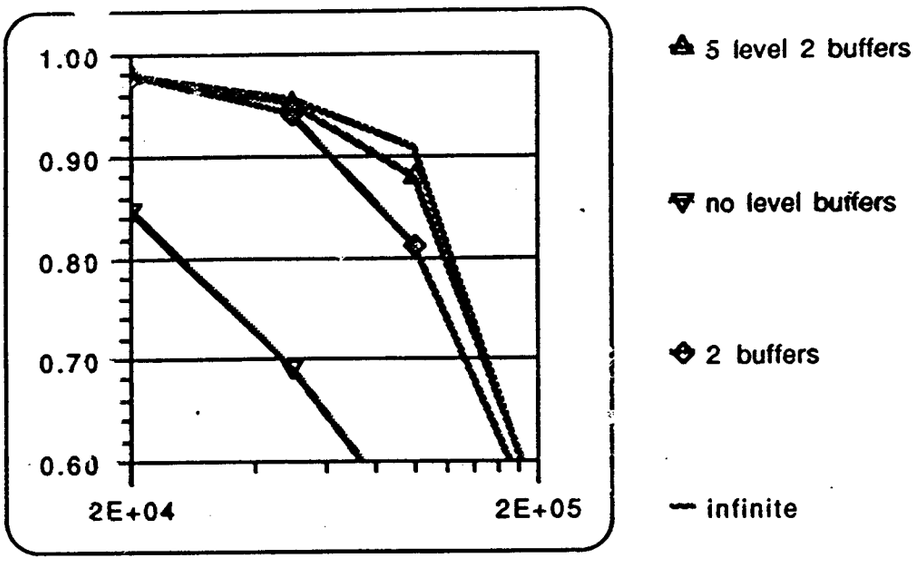
Data Collection Network



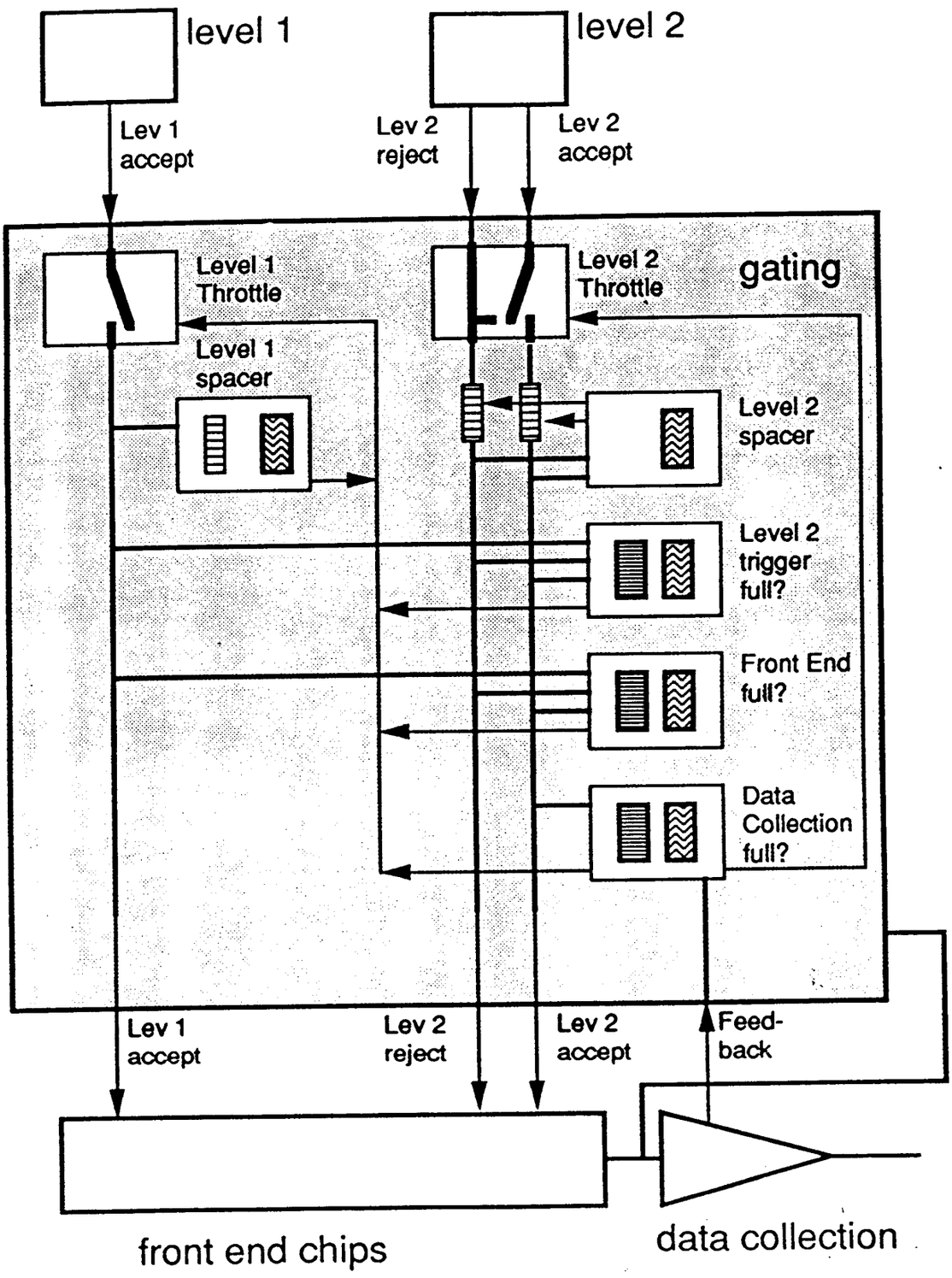
Front end simulation



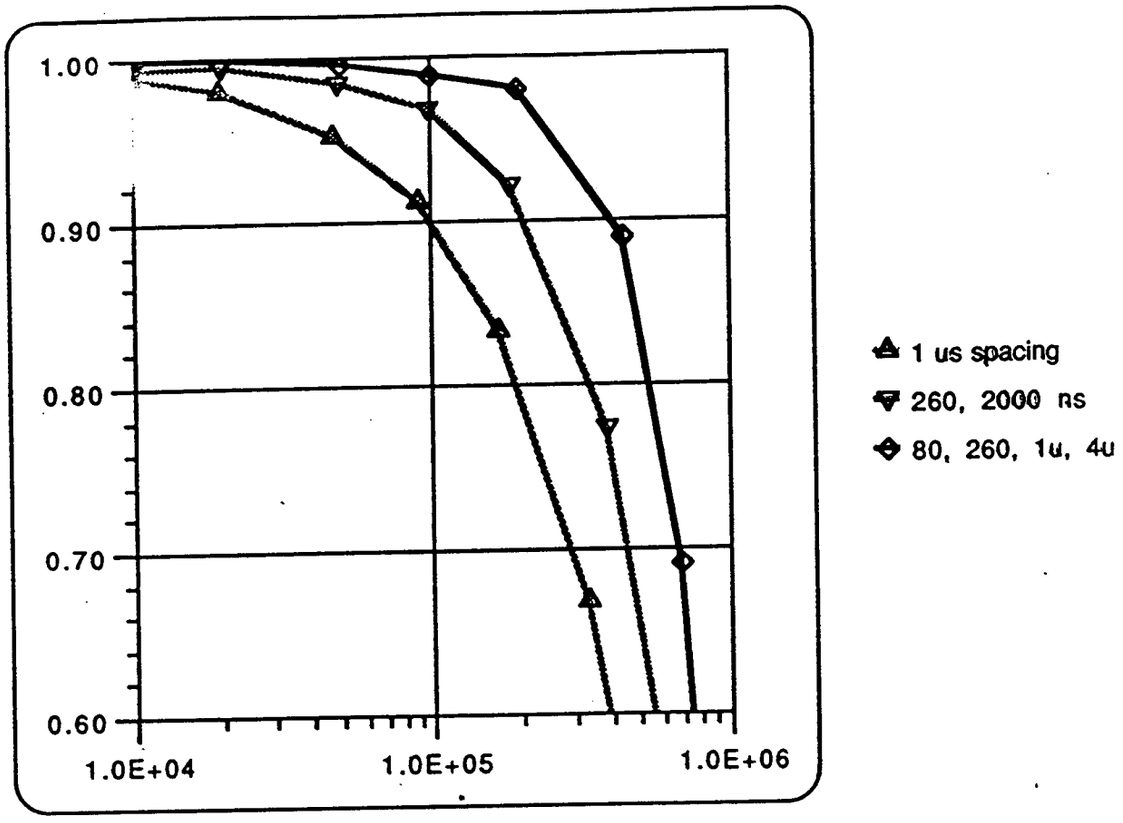
Level 2 needs buffers



Gating logic simulation



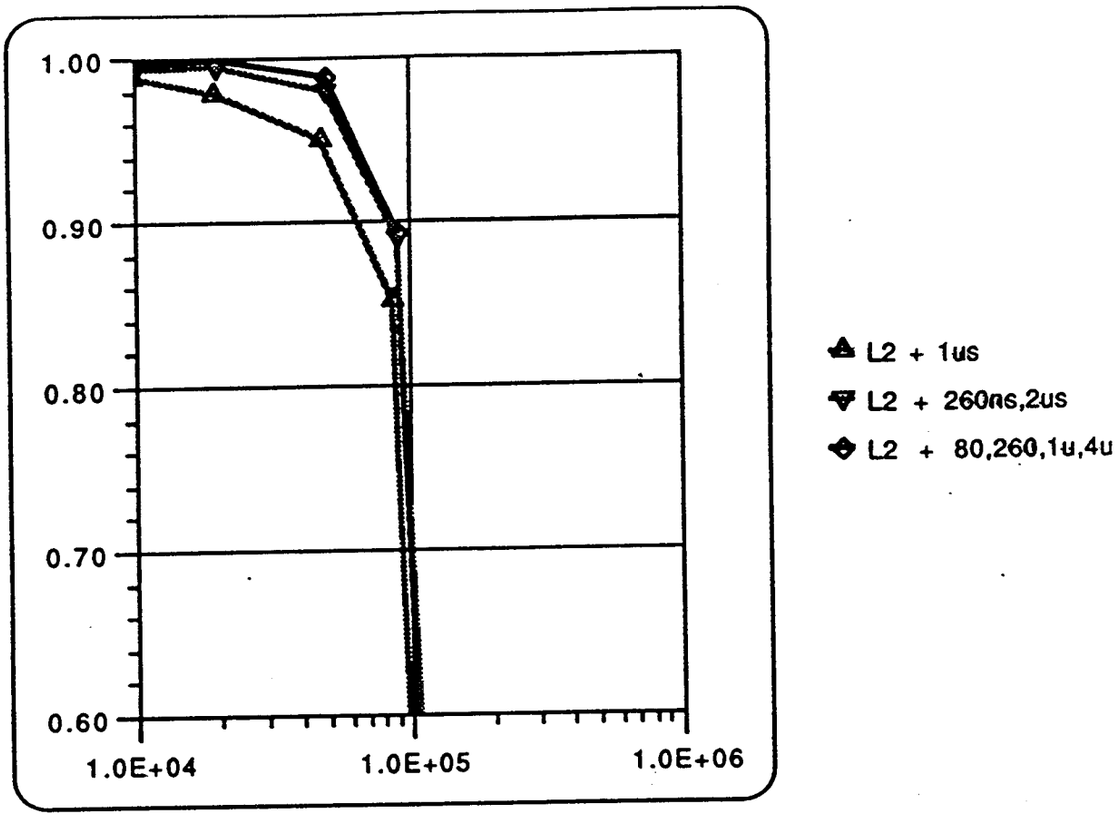
More complicated designs give better readout efficiencies



Efficiency curves for three sets of level 1 spacing rules[1]

[1] Efficiencies have been calculated using MODSIM, a discrete event simulation package.

However, careful design of the complete readout system is needed.



Efficiency curves for three sets of level 1 spacing rules combined with the same, not so efficient, level two trigger.

What can we learn from simulation?

- how to control data flow through system
- how to prevent buffer overflows
- how to throttle level 1 and level 2 rates
- what information is needed for throttle, how does it get there?
- buffer sizes
- throughput requirements
- influence of embedded processing on throughput
- error detection, error diagnostics, error handling

What do we not learn?

Need extensive physics and detector simulations

For all detector subsystems:

- Average data voluem for events accepted by level 1 (2).
- Fluctuations in total event size.
- More important: fluctuations between channels and correlations (dominates buffer size requirements deeper into the data collection network)
- Trigger strategies:
- What physics do we need to trigger on
- What rate with what threshold for which inputs
- What and how much input data is needed at which level.
- Develop complete trigger strategy

Pixel Readout

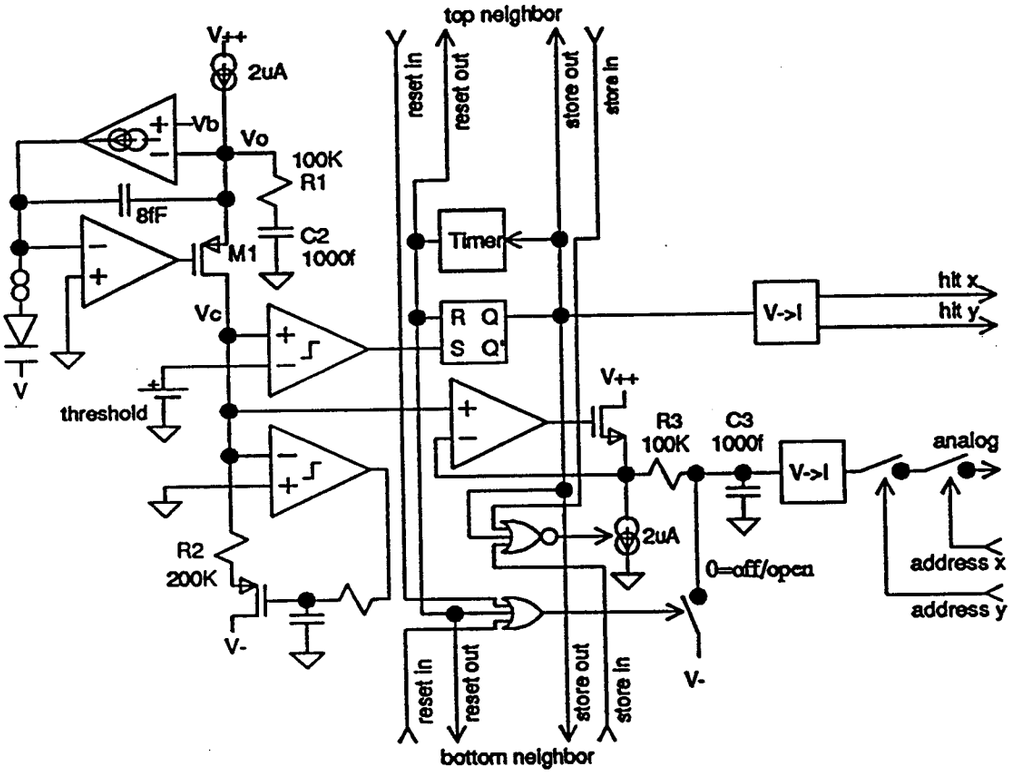
D. Nygren

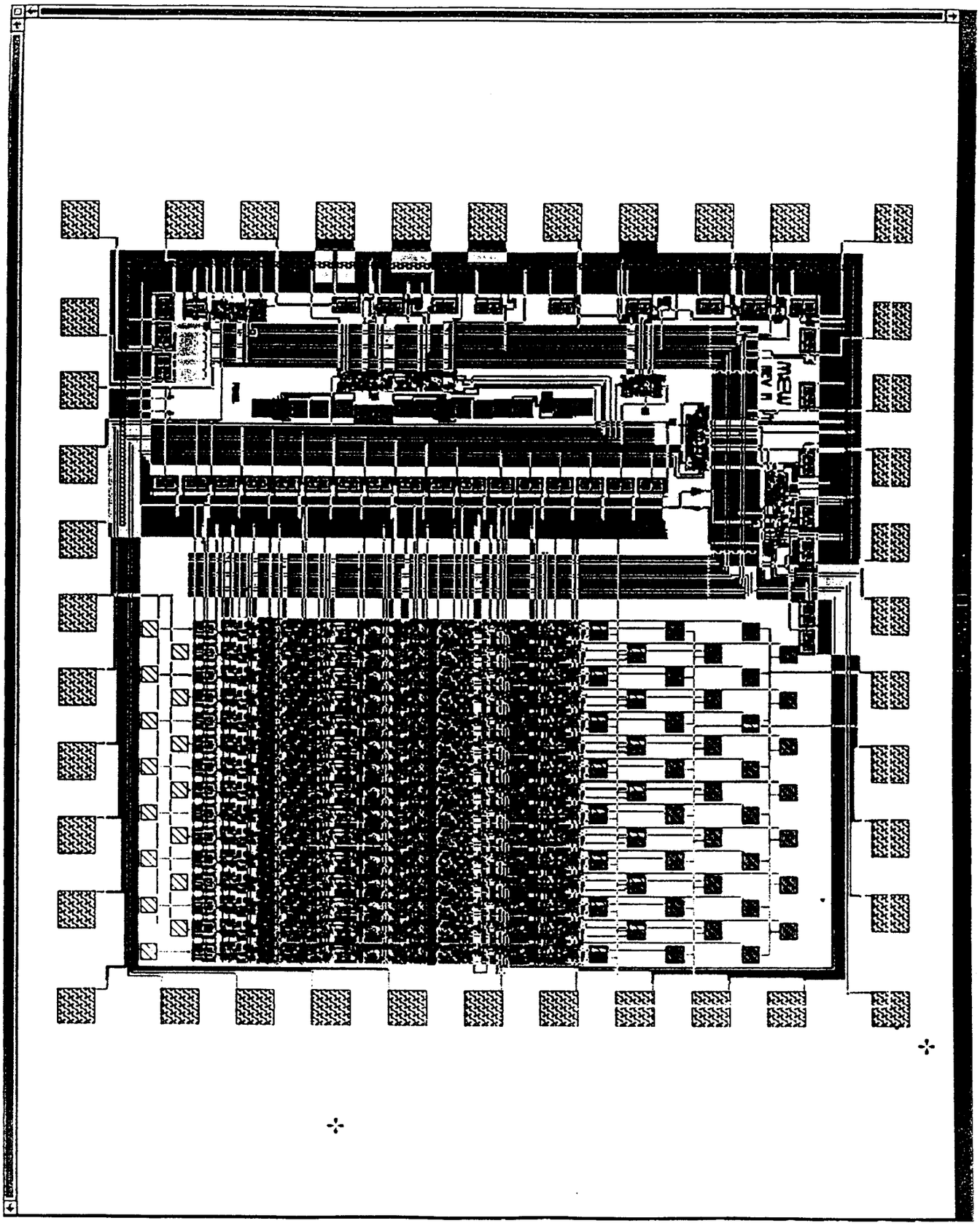
L.B.L. Pixel Prototype

Preliminary Results

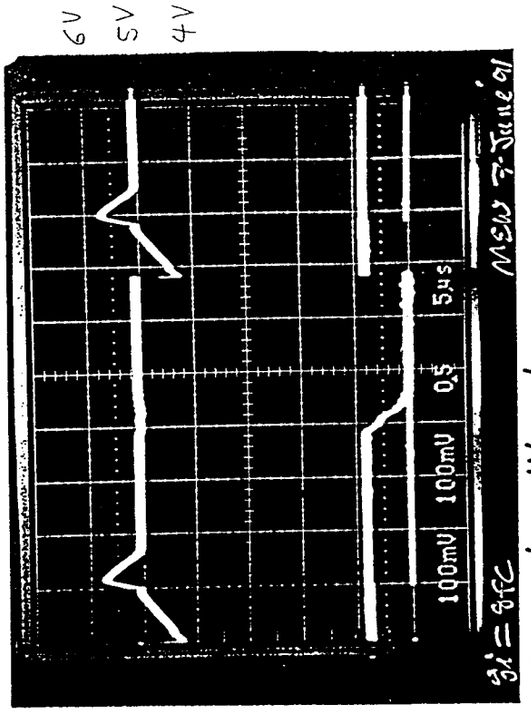
Michael Wright
415-486-4401
mew@analog.lbl.gov

Sat. 8 June '91

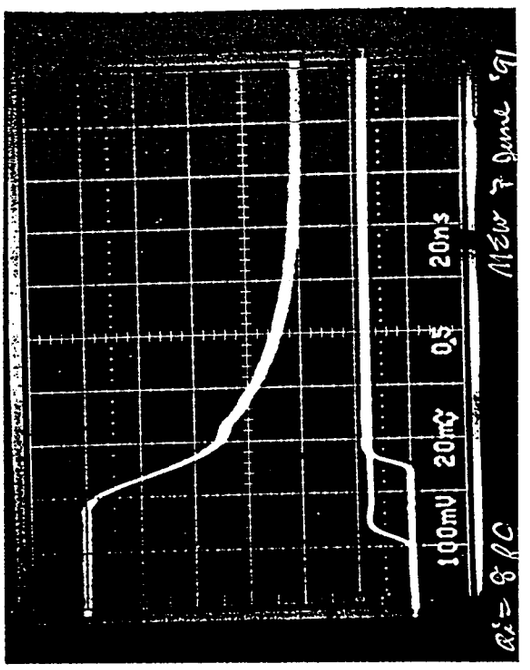

top neighbor
V++
2uA
Vb
Vo
100K
R1
8fF
C2
1000f
M1
Vc
V
threshold
reset in
reset out
store out
store in
Timer
R Q
S Q'
V->I
hit x
hit y
R3
100K
C3
1000f
analog
address x
address y
R2
200K
V-
0=off/open
bottom neighbor

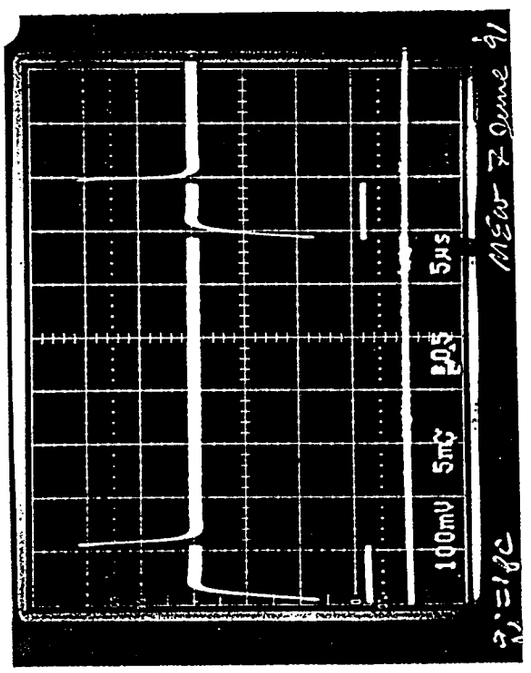


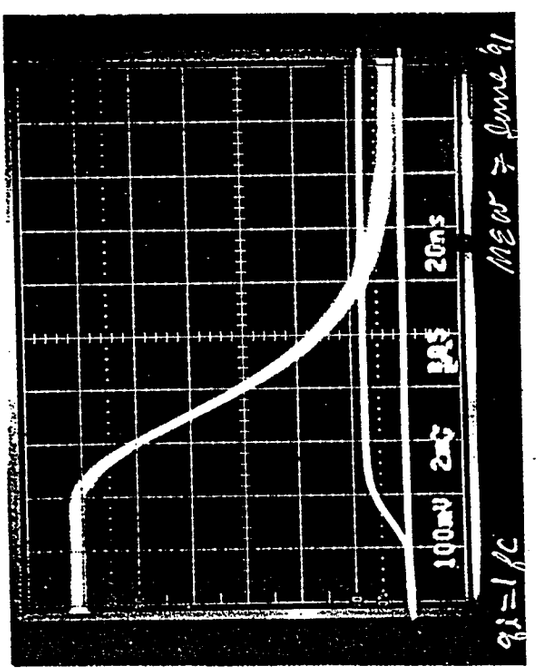
Probed Integrator Response



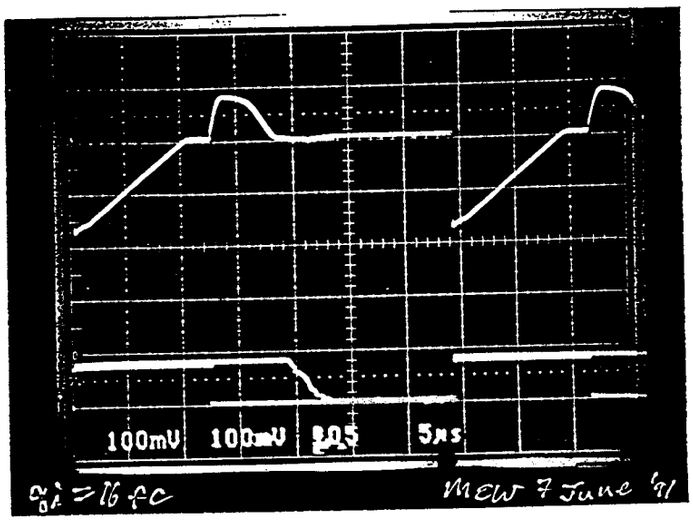
8fC gives 1V step

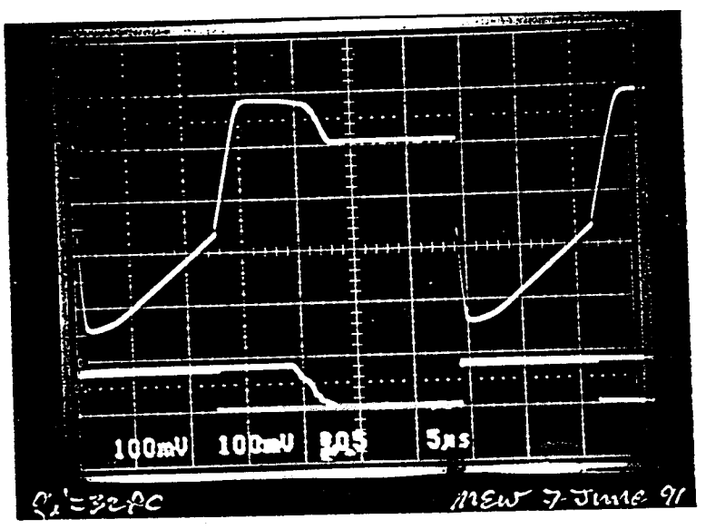






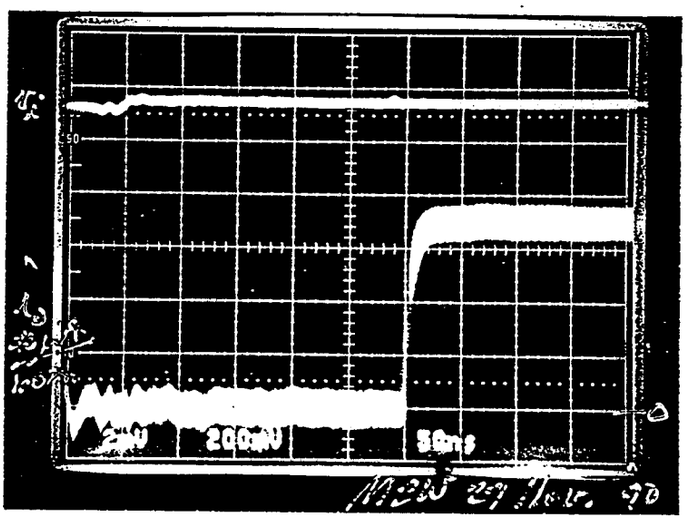
Integrator Saturation
(>16 fC)





Comparator Block

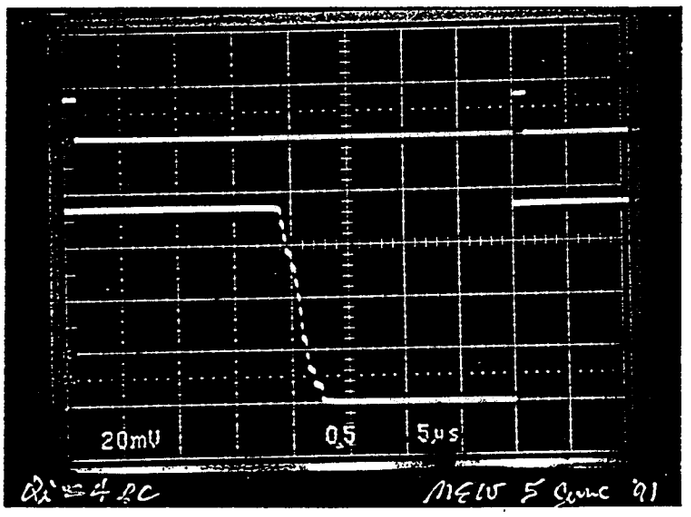
Speed

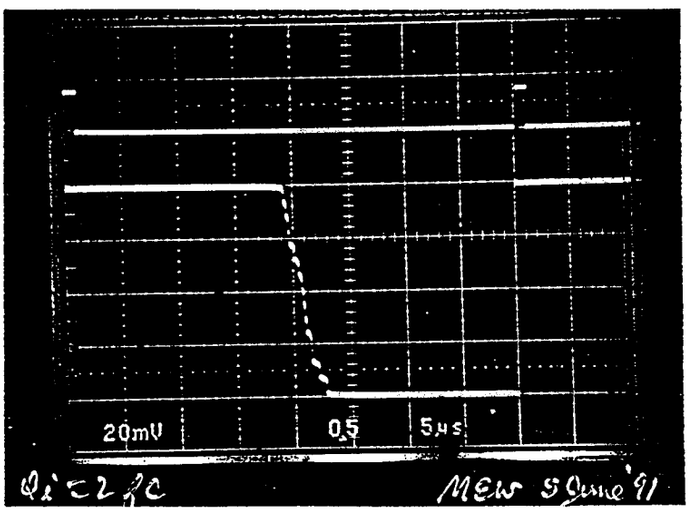


SSC Pixel prototype Comparator time delay, M Wright, 3 Dec. '90.
Δdelay for 1~8 fC input range (ns):
Id = 11 μA: 22 ns
Id = 22 μA: 19 ns
Id = 44 μA: 14 ns
Threshold level, overdrive=0, delay = ∞.
Time Delay to Discriminator Hit (ns)
100
10
Equivalent Input Charge Step (fC)
10
1
0.1

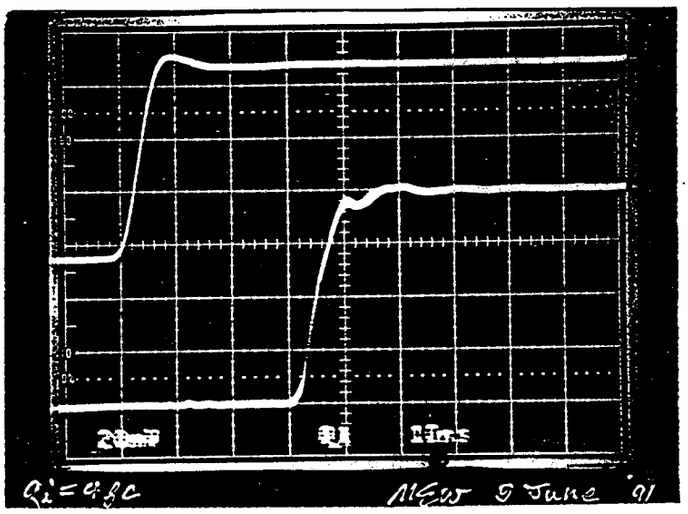
1-D Array Calibrate In, Hit Out

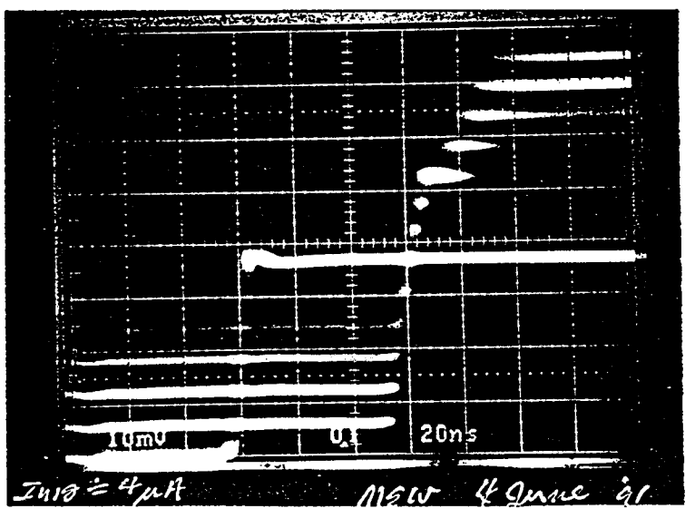
I_{Hit} Wire OR'd

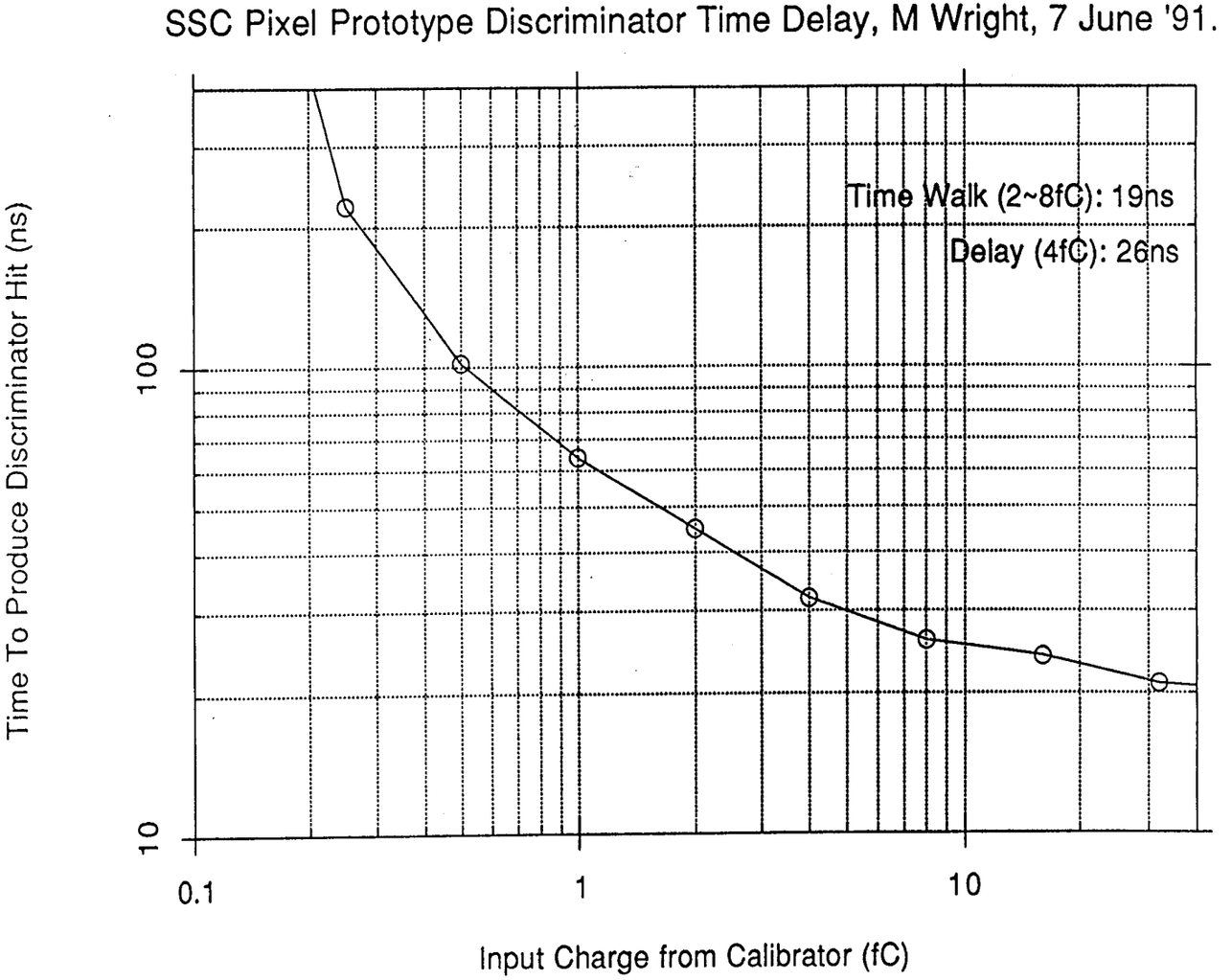




Discriminator Path Speed

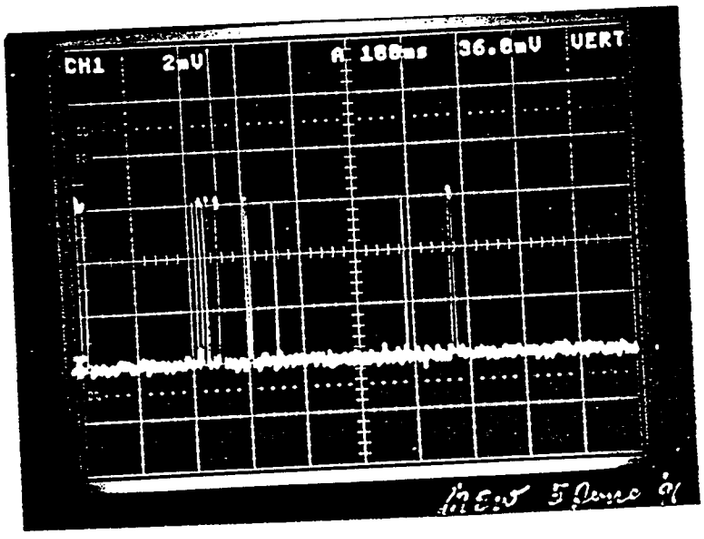





SSC Pixel Prototype Discriminator Time Delay, M Wright, 7 June '91.
Time Walk (2~8fC): 19ns
Delay (4fC): 26ns
Time To Produce Discriminator Hit (ns)
100
10
0.1
1
10
Input Charge from Calibrator (fC)

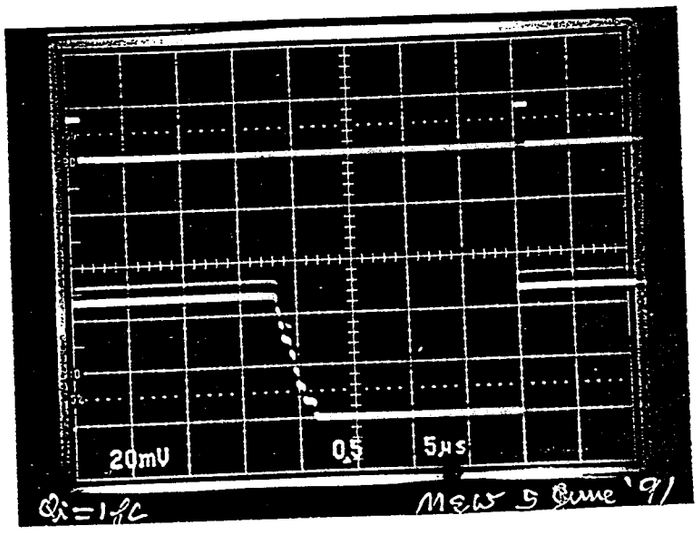
Discriminator Path Noise

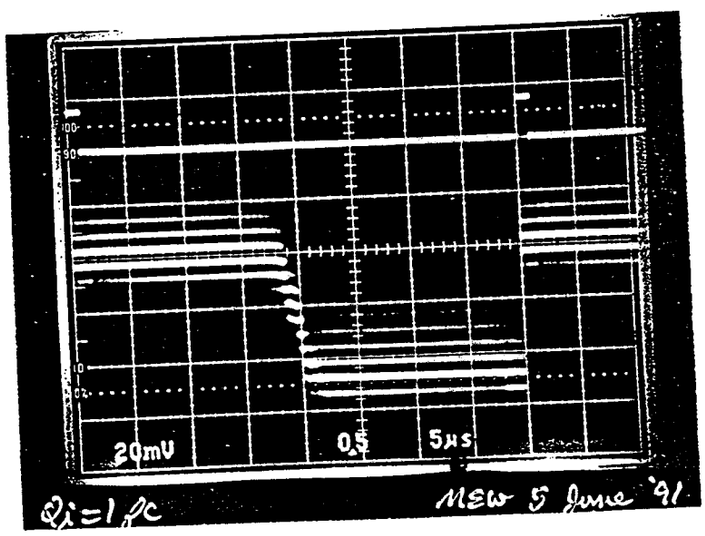
Want to measure false hits/s at nominal threshold.



Channel-Channel Threshold Match

(Example, not proof, of FET matching problems)





MZW 7 June 91

Prototype Specifications

Spec	Goal	Result
pixel area (2μ CMOS) scale to 1.2μ CMOS	50x? μm	50x1000μ 30x? μm
target process, radiation hardenned (all capacitors IGFET gate, 1 term to Vdd) (I did not use Orbits 2nd poly!)	UTMC 1.2μ p well 1 poly, 2 metal	Orbit 2μ p well 1 poly, 2 m
power density power at 50x1000μm	<1 KW/m² 50μW	3.3 KW/m² 55μW int. 60μW disc. 50μW analog
delay from input to discriminator hit (final version speed depends on (slow) detector charge collection)	16 ns	26 ns
time walk, 2~8fC	16 ns	19 ns
feedback capacitor	8fF	9.2±10% fF
threshold uniformity, discriminator	400e ~~40aC~~	10000e ~~1.5fC!~~
input referred charge noise	200 e RMS	215 e RMS
cross-talk * preliminary, 1-D array, highly dependant on bump-bonding of detector	Must not trigger adjacent channel upon 8fC hit! 8fC/1/8fC = 1/64	1/24 *

Pixel/Preamp/Disc

M. Wright

Smart Pixel Motivations

- Pixels provide **three-dimensional spatial data** of superior quality. The N^2 ambiguities characteristic of wire and strip detectors are absent. Track-pair resolutions are on the order of 200 μm.
- **Jets** can be reconstructed and **secondary vertices** resolved with high efficiency, even at SSC, RHIC,.....
- The **smart pixel** concept was developed at LBL in 1985 to meet the challenges of the SSC : **very complex events in a high background environment.**
- A **smart pixel must generate prompt signals** indicating the detection of a charged particle trajectory through the pixel sensitive volume.
- Each smart pixel has a **preamplifier, a shaping element, discriminator, analog storage, and various hit/ interrogation/reset functions.** In a 1.2 micron process, this requires an area of 50 x 150μm^2.
- **On-chip pattern registers** with fast time resolution record x-y position and correlated time information; analog information remains on pixel until read.
- The smart pixel array is **"quiet"**. Architecture is data-driven, without high frequency scanning to search for struck pixels. Power dissipation and noise generation are minimized. No resemblance to CCD's.

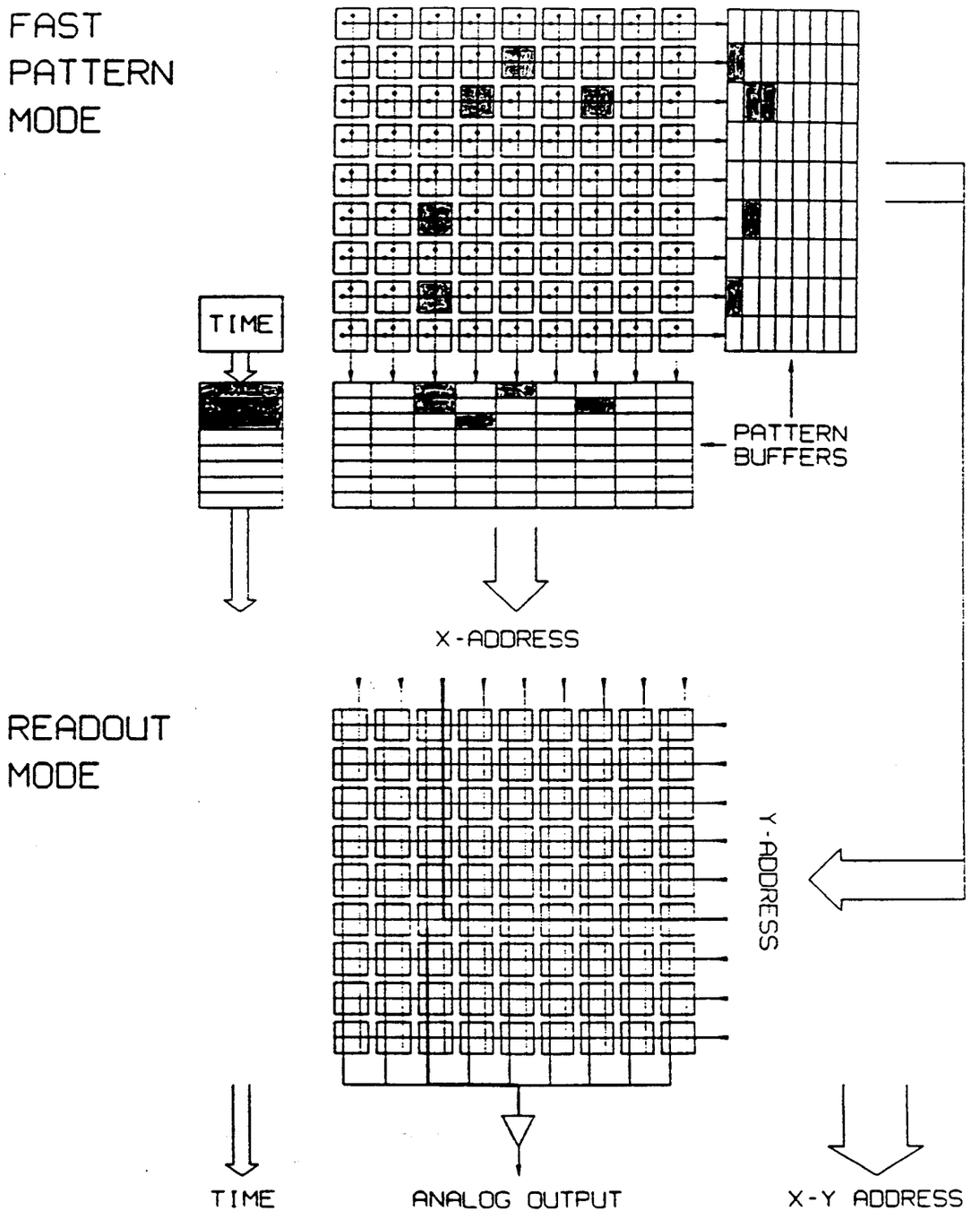


Fig. 3 Readout modes of "smart" pixel device

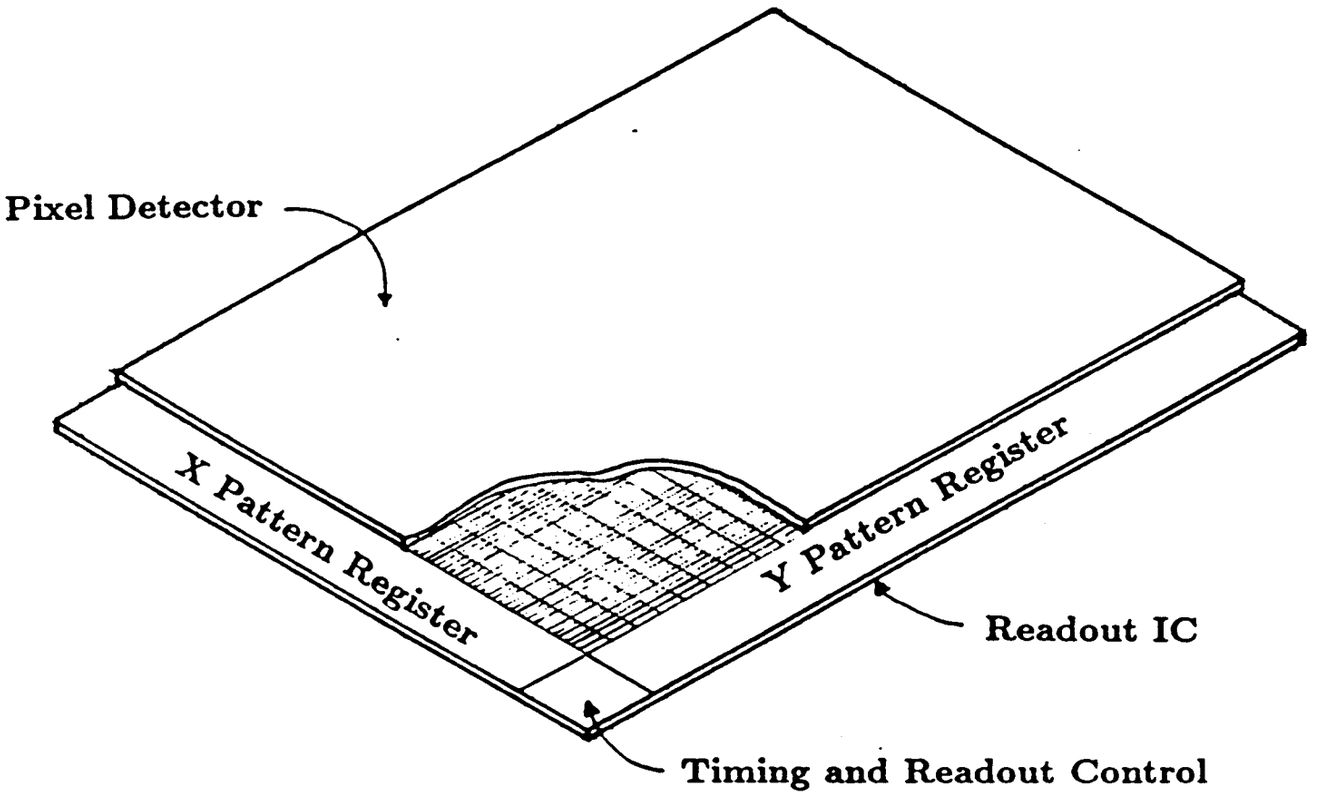
Engineering Advantages:

- **Small capacitance** ($\simeq$ 100 fF) allows amplifier noise to be minimized, leading to S/N ratios of $\geq$ 100.
- Small pixel detector volume provides **inherent radiation hardness.** Shot noise from detector dark current is small, even after a decade at SSC.
- Accuracy of spatial grid determined by **lithography** - $\simeq 0.2\mu m$. No calibration ever necessary within address field of chip.

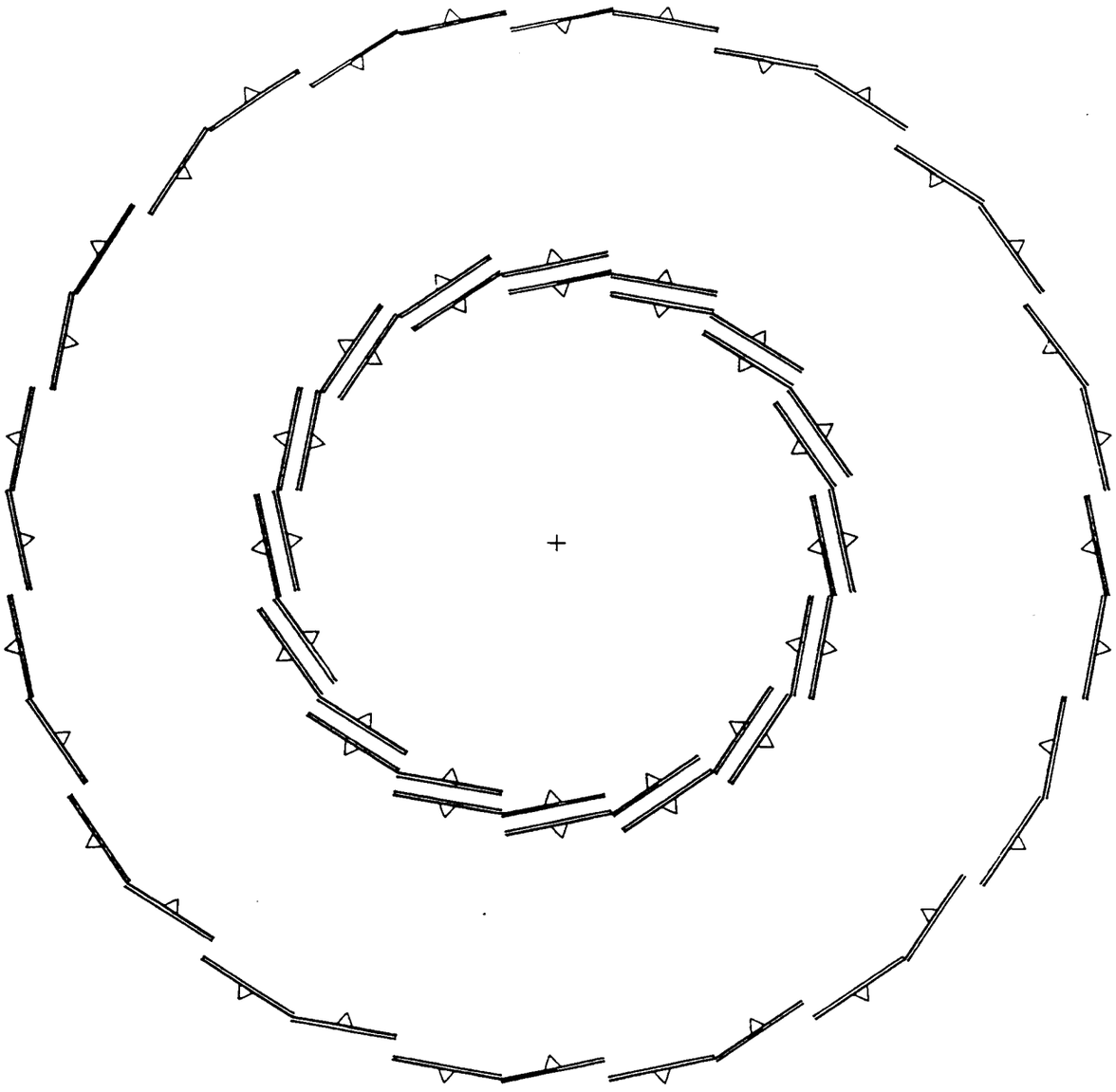
Issues:

- **Digital or Analog?**
  - Analog information offers opportunity for interpolation, yielding better spatial resolution, but makes pixels bigger and system design harder.
  - Digital system makes system easier to design and pixels smaller, but with perhaps worse spatial resolution and system diagnostics.
- **Hybrid or Monolithic Technology?**
  - Hybrid technology is mature and allows separate optimization of detector and readout IC, but adds mass and complexity.
  - Monolithic technology is at a promising, but very early stage. Schedule uncertainties may be large.

Smart Pixel Array Hybrid Technology



- Readout IC and Detector are joined by a matrix of **indium bumps.**
- Array size is $\simeq 1cm^2$.
- Information is stored on-chip for level I trigger only.



Pixel Detector Strategies

1. Choose hybrid technology:
   - Bump-bond technology is mature and available;
   - Allows some circuitry to be built into detector;
   - Allows utilization of available radiation-hard IC technology;
   - Fastest perceived path to achieve SSC performance.
2. Choose analog information output:
   - Need analog information for interpolation;
   - Need analog information for diagnostics;
   - Not enough experience to justify digital only.
3. Choose rectangular pixels:
   - 50 x ? μm, allowing high resolution in r-ϕ plane;
   - Long pixels in z are a good match to wide range of track angles in r-z plane, for SSC applications. (Short pixels in z will not collect much ionization.)

Pixel Vertex Detector
Technical Progress

- Architecture has been established although new ideas are still emerging, *e.g.*, can time-walk measurements replace analog sample-and-hold + ADC?
- Silicon test devices have been designed, fabricated and tested at both Hughes and LBL.
- Hughes:
  - "Foresight 4", a 32 x 64 array of smart pixels plus simple control registers has been designed, fabricated, and tested. Chip is functional but displayed problems due to layout error coupling digital noise to substrate of analog section. Basic analog noise appears small. Many lessons learned have been incorporated into next version ("Foresight 5"), to be fabricated next month, and to serve for proof-of-principle.
  - "Foresight 1", a single pixel cell, identical to circuitry above, has been fabricated in a radiation hard Hughes SOS process. Awaiting test....
  - A complete architecture has been designed for a true prototype, but not yet laid out. We need to simplify this general architecture further.
  - A design study for a complete mechanical engineering concept using air-cooling and silicon carbide foam has been done.

Figure 6.5 Pixel Detector SSC Prototype Architecture.

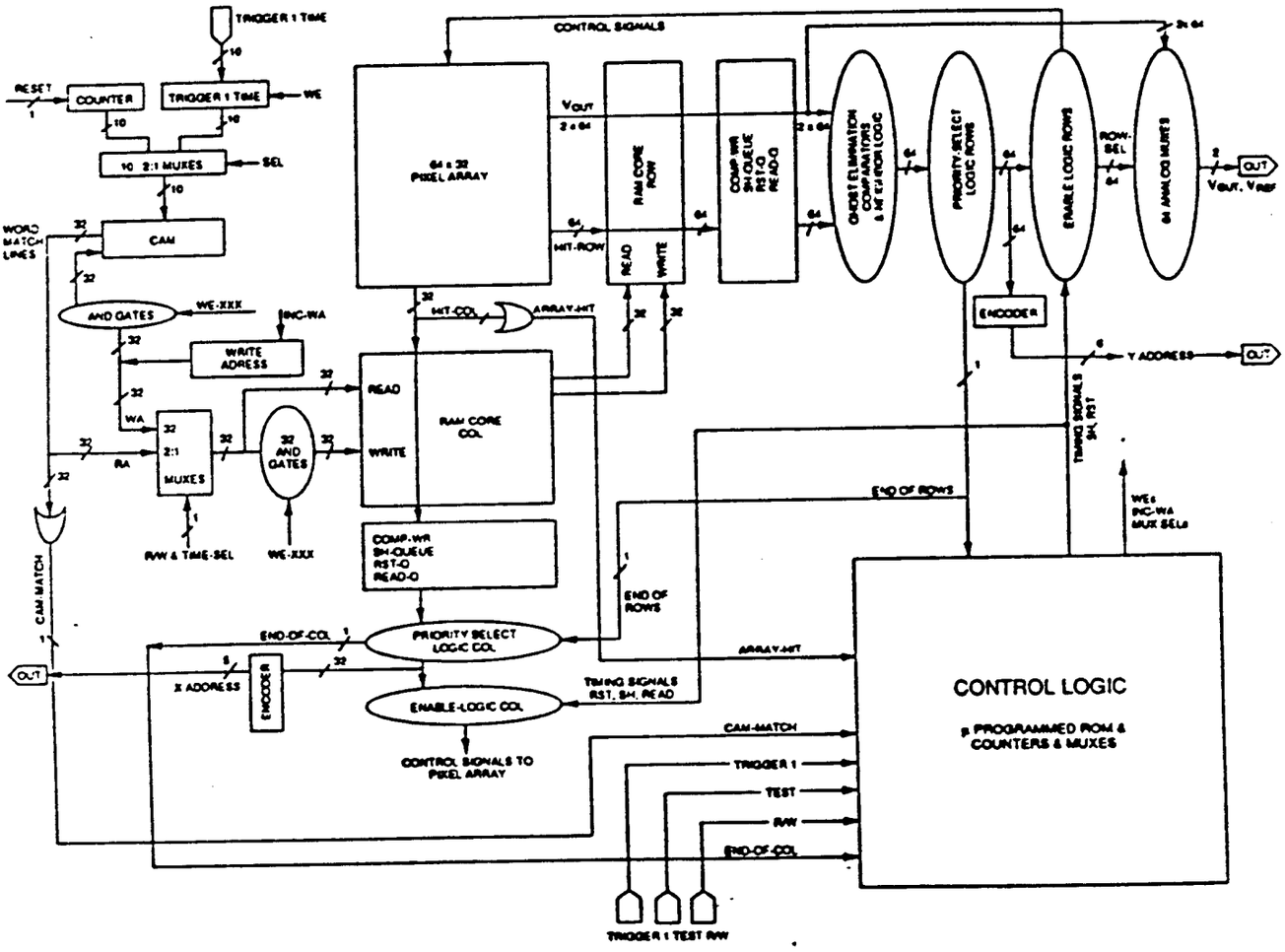
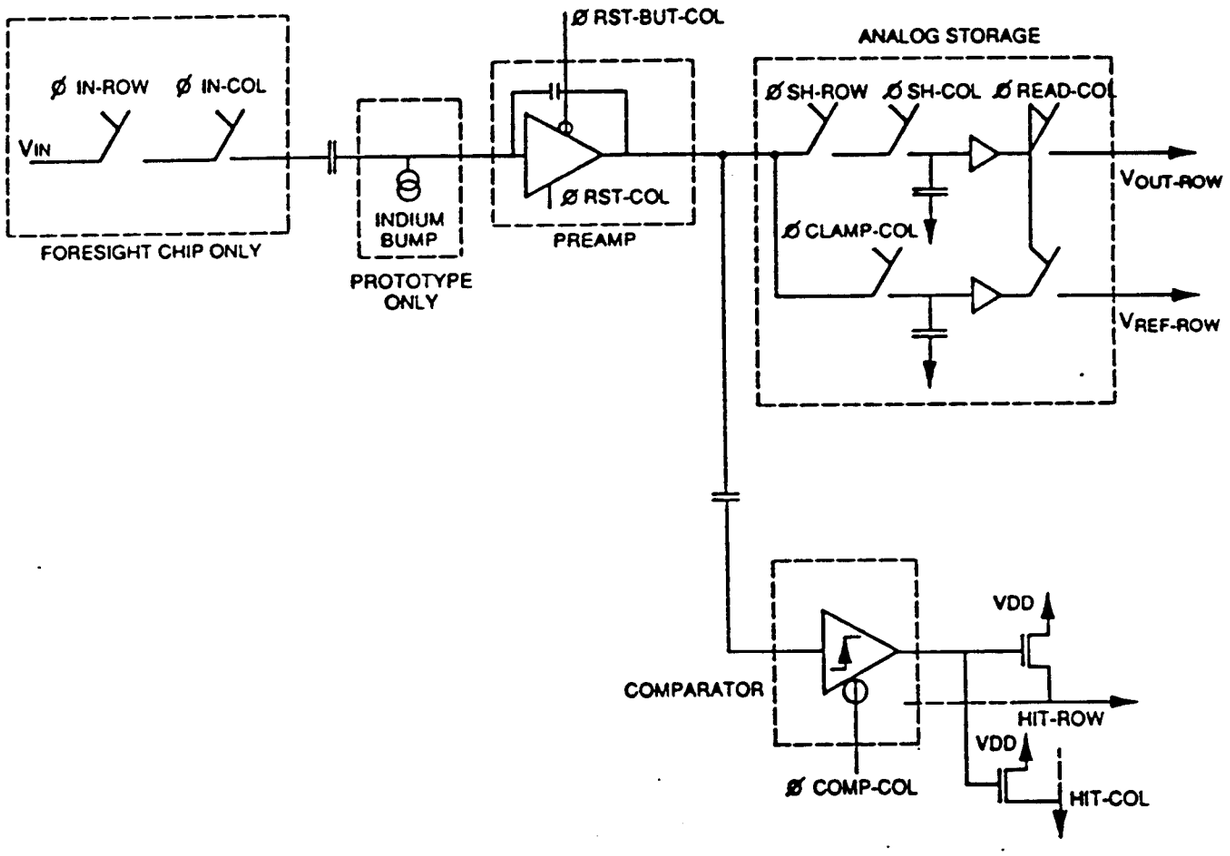


Figure 6.4 Simplified Unit Cell (Pixel) Architecture.



CHP 1 & CHP 4 - LESSONS LEARNED

HUGHES

1) VAST DIFFERENCE BETWEEN 1 PIXEL AND WHOLE ARRAY OPERATION
2) CAN'T HAVE TOO MUCH ISOLATION OF POWER RAILS (DIGITAL COUPLING)
   NEED SEPARATE RAILS FOR OUTPUT BUFFERS AND DRIVERS (VSS SPIKES)
3) VSS IN UNIT CELL WAS A KILLER (NOISE, S/H OPERATION, Zt LOW, INPUT SELECTION)
4) 5V UC DIGITAL OUTPUTS NOT A GOOD IDEA (CROSSTALK TO WHOLE COLUMN)
5) INCOMPLETE VERIFICATION FILES - SHORTED OUTPUT BUFFERS (Zt, "OFFSET OF ONE", Vt MATCHING)
6) CAPACITIVE STRAYS AND FRINGING FIELDS CAN ACCOUNT FOR 50% OF C (LOW Zt, CROSSTALK, TRANSIENT RESPONSE)
7) ANALOG BUFFERS NEED TO BE P-CH FOR GREATER DYNAMIC RANGE (D.R. LIMIT TO .5V)
8) MODEL DOES NOT PREDICT WELL TIGHT LAYOUT UC RESPONSE, ONLY TRENDS (TIME WALK, DELAY)
9) SUBSTRATE CONNECTIONS ARE CRITICAL FOR P&N DEVICES ON BOTH ANALOG AND DIGITAL CIRCUITS

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UC (PIXEL) CHANGES

HUGHES

1) INDIUM BUMPS ADDED, CAN ACCOMMODATE BOTH 50 X 150 & 25 X 300 DETECTOR CONFIGURATIONS

   RETAINED ELECTRICAL INPUT CAPABILITY FOR TESTING

2) DIGITAL OUTPUTS VOLTAGE SWING REDUCED FROM 5V TO 100-300 mV

3) FEEDBACK CAPACITOR AREA REDUCED TO ACCOUNT FOR STRAYS AND FRINGING FIELDS

4) VSS REPLACED BY V_{pw} -PIXEL, A DEDICATED ANALOG BIAS

5) ANALOG SOURCE FOLLOWERS ENLARGED FOR GREATER DRIVE

6) VARIOUS METAL AND POLY LINES REARRANGED AND ENLARGED FOR GREATER COUPLING SHIELDING

7) POSITIVE FEEDBACK CAPACITOR (PFC) ADDED TO PIXEL COMPARATOR TO REDUCE TIME WALK (~2.5 fF)

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SPECIFICATIONS FOR CHIP5

HUGHES

SPECIFICATION	VALUE
PIXEL DIMENSION	50μm x 150μm
ARRAY SIZE	64 x 32
CHIP RESET	YES (1 CLOCK)
PERCENT DEAD PIXELS	TBD
ELIMINATE GHOSTS	YES (PERIPHERY COMPARATORS)
ISOLATED SUPPLIES	YES (28 SEPARATE BIAS & SUPPLY PADS)
MAXIMUM SIGNAL	50 Ke^-
MINIMUM SIGNAL TRIGGER	3 Ke^-
NOISE	300 e^-
ANALOG ACCURACY	4 BIT
TIME-WALK	<50ns FOR VIN >2 x MIN SIGNAL
RADIATION HARD	NO
FILL-FACTOR	DON'T CARE (STANDARD CELLS)
YIELD	TBD
TESTABILITY	YES (PIXELS HAVE ELECTRICAL INPUTS)
PACKAGE	68 PIN LEADLESS

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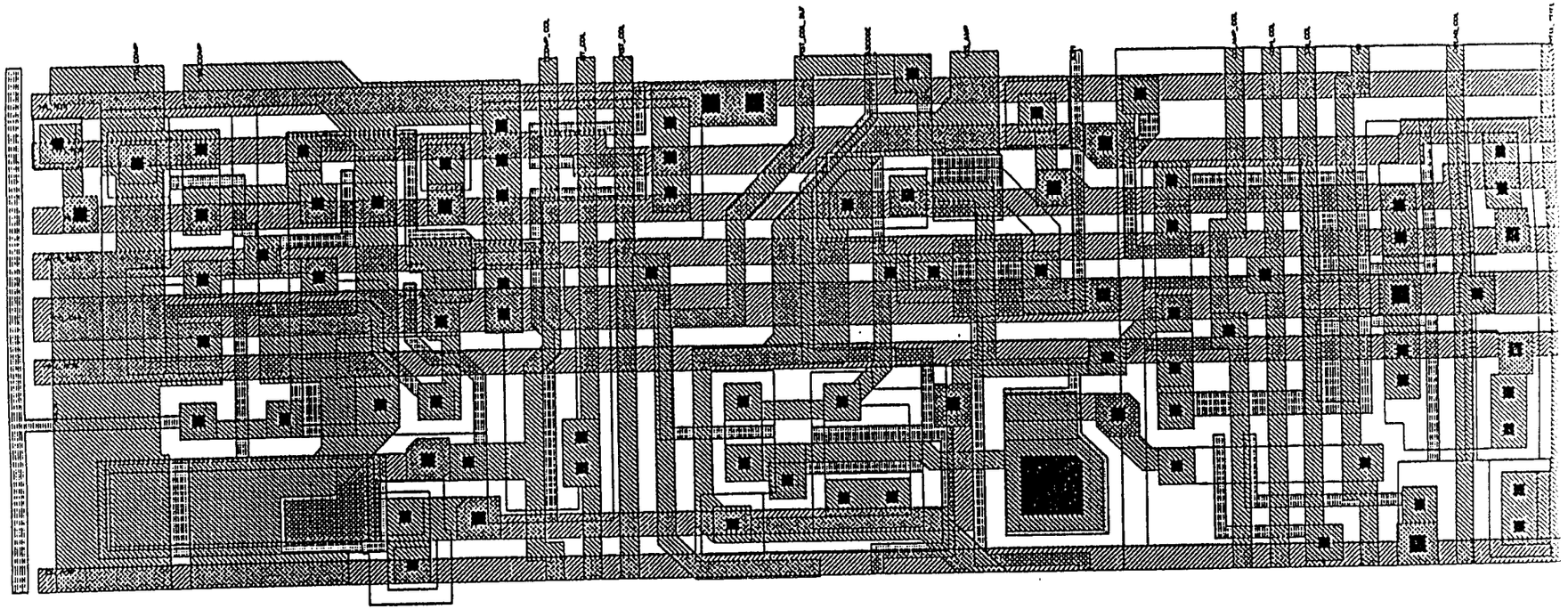
MT91100.BARKAN.3

SSCUC LAYOUT

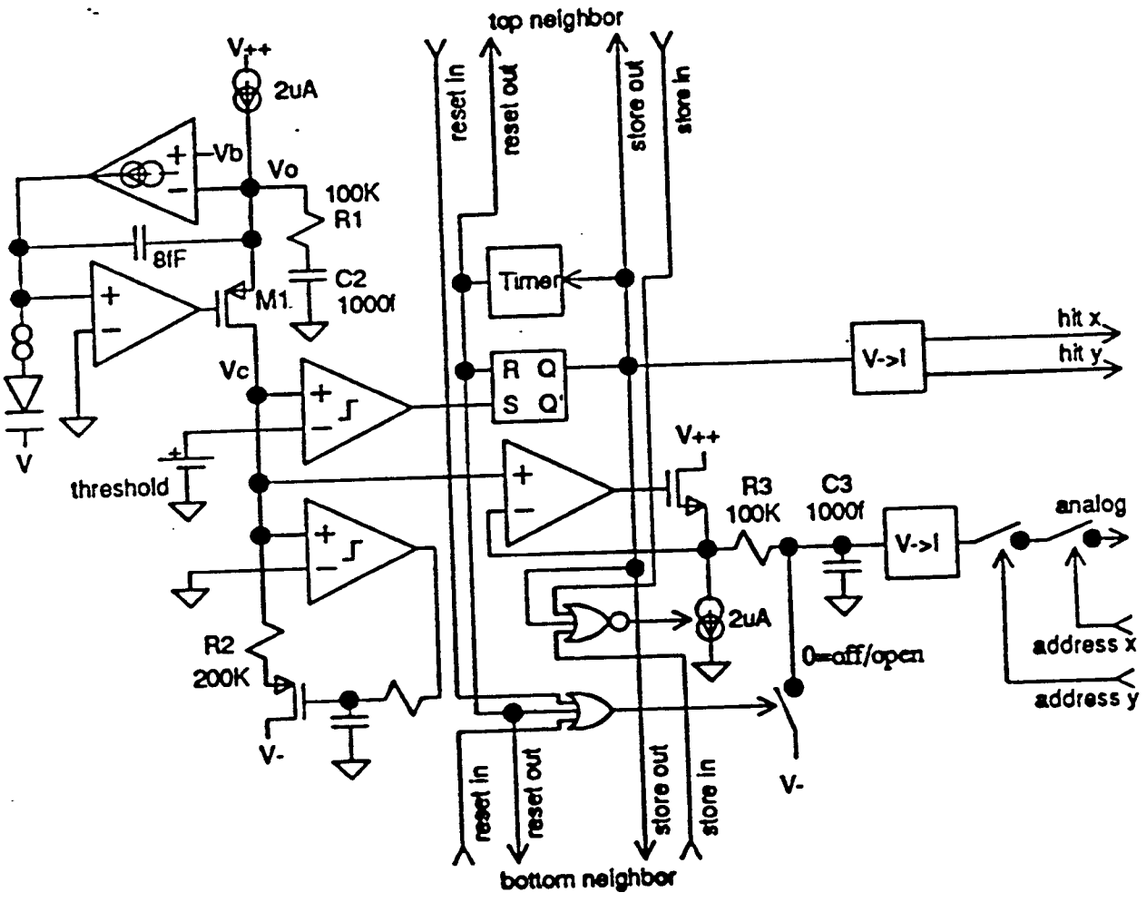
SSCUC LAYOUT



535

- LBL:
  - An advanced smart pixel cell has been designed, fabricated, and partially tested.
  - Advanced circuit design features include:
    * DC servos for stabilization against manufacturing variations and radiation damage;
    * CR-RC filtering for superior rejection of detector shot noise;
    * Autoreset functions for the preamplifier and comparator for completely autonomous operation.
  - The final design will need to incorporate many of these advanced features for robust operation and to withstand radiation damage. This additional complexity increases the pixel cell size considerably, an undesirable consequence.
  - A new concept using time-walk measurements as an indirect measure of charge sharing in neighboring pixels is being evaluated. If successful, this would substantially reduce pixel cell size by eliminating all pixel analog storage and processing circuitry, as well as neighbor logic.
  - Each functional block has been tested and found to be working, but layout error prevented complete operation of entire cell. New chip with fix is now available, awaiting test.
  - Pixel detectors for Hughes Foresight 5 are now being fabricated.

Figure 6.8 Block Diagram of the Advanced Pixel Cell Design Developed at LBL.



Comparator Speed Versus Input Amplitude, MEW, 19 Oct '90

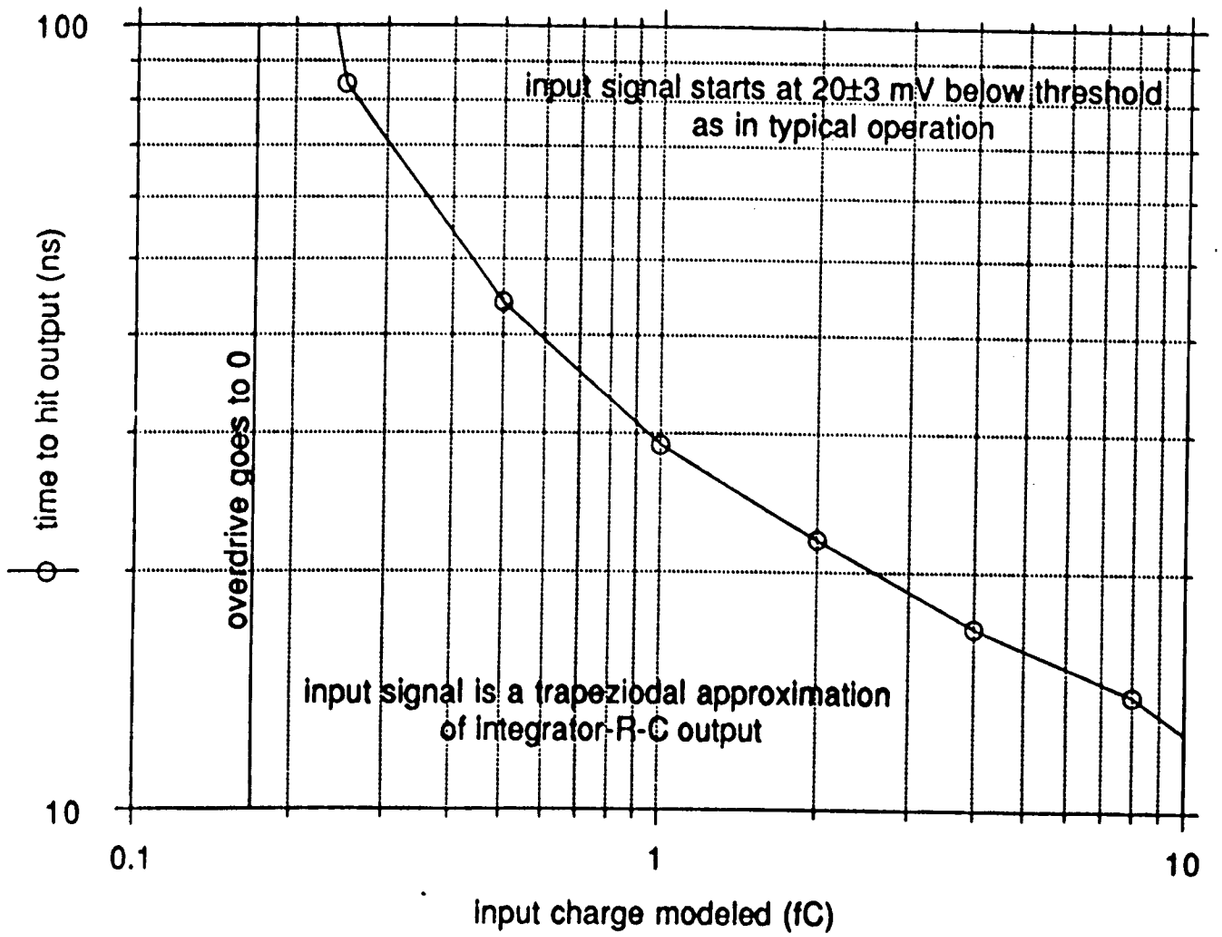


Fig. 1

Potential Advantages of Time-walk ADC:

1. Substantial circuit simplification. The pixel cell circuit area is $\simeq 30\%$ smaller, improving the pixel spatial resolution directly. No sample-and-hold, mux,...
2. Analog to digital conversion is nearly instantaneous.
3. The "dynamic range" of the time-walk ADC is very large, with resolution decreasing for larger signals and limited by noise filtering.
4. The processing of events and pixel interrogation become purely digital.
5. System design would also be substantially simplified, and the readout cycle should be considerably faster.
6. The time measurements provide a natural monitor of system performance.
7. Front-end power dissipation may be minimized.

Let

$$x = m \cdot w + \frac{d(q_n - q_m)}{2(q_n + q_m)} \tag{1}$$

The error δx due to errors δq_i in the charges q_i is

$$\delta x^2 = \frac{d^2}{4}\left(\frac{q_m^2 \delta q_n^2}{Q^4} + \frac{q_n^2 \delta q_m^2}{Q^4}\right) \tag{2}$$

where $Q = q_m + q_n$. Consider the case in which $q_m \simeq q_n$.

$$\delta x^2 = \frac{d^2}{4} \cdot \frac{\delta q_m^2 + \delta q_n^2}{4Q^2} \tag{3}$$

yielding for the symmetric case:

$$\delta x^2 = \frac{d^2}{8} \cdot \frac{\delta q^2}{Q^2} \tag{4}$$

For an effective resolution of 3 bits and d = 20 μm,

$$\delta x = 0.88 \mu m \tag{5}$$

The relationship of time and charge for this data is an approximate inverse square root dependence:

$$t_i = \frac{C_1}{\sqrt{q_i - q_t}} \tag{6}$$

where q_t = comparator threshold charge; equivalently

$$q_i = C_1^2/t_i^2 + q_t \tag{7}$$

$$x = m \cdot w + \frac{d(t_m^2 - t_n^2)}{2(t_m^2 + t_n^2 + C_2 t_m^2 t_n^2)} \tag{8}$$

where $C_2 = 2q_t/C_1^2$. By differentiating equation 7:

$$\frac{\delta q}{q} = -2\frac{\delta t}{t} \tag{9}$$

if δt is 2 nsec, $\delta x \simeq 1 \mu m$ for one fC; For 2 fC, $\delta x \simeq 1.3 \mu m$.

$$\delta t \simeq \frac{t_p}{S/N} \tag{10}$$

where t_p is the peaking time. Then for a 1 fC signal and t_p = 50 nsec, δt = 2.0 nsec.

Summary: Time-walk may offer a means to have a "purely" digital system with nearly "analog" performance.