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SDC
SOLENOIDAL DETECTOR NOTES

DEVELOPMENT OF AC COUPLED SEMICONDUCTOR DETECTORS FOR HIGH LUMINOSITY OPERATIONS: STRATEGY AND DESCRIPTION

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Development of AC coupled semiconductor detectors for high luminosity operations. Strategy and description.

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Introduction.

In the CDF Upgrade Document (CDF/Doc/Public/1172), we have described the need to replace our SVX basic detectors (crystals) with other detectors of different type in the near future. Similar requirements apply to the detectors for the SDC silicon tracker. In the following we will describe the details of a set of prototype detectors, which are presently being designed, after a brief review of the motivations which drive these requirements.

The first generation of silicon detectors, used in the CDF - SVX, are DC coupled to their front end electronics. This mode of operation is certainly not adequate to the experimental environment typical of high luminosity colliders: in particular at CDF, after the Tevatron upgrade, and, even worse, at SDC. In both cases the level of radiation from primary proton - antiproton interactions will rapidly increase the leakage current of each individual strip up to levels which will totally saturate the front end amplifiers. For instance, the leakage currents are expected to grow from 1 to a 450 nA/strip on the first layer of the CDF vertex detector after 200 pb^{-1} of delivered luminosity. Rescaling this value to the SDC situation after one year of running, with the assumption of 10 cm long strips at 10 cm from the beamline, we obtain a current of 720 nA/strip.

One way out to be considered is the use of AC - coupled detectors.

In the present CDF design the decoupling capacitor should be >100 pF, being the strip (source) capacitance ~ 30 pF.

The choice of AC coupled detectors is not without alternatives:

1) One could try to push the technology in order to produce an external array of capacitors with the right pitch and large enough values for the capacitance. It is not proven that this can be done and is not clear how much this chip will be damaged by radiation.
2) Change the design of the preamplifier in order to increase by a sizeable amount the the dynamic range.
3) Change the design of the detector in order to reduce the source capacitance.

Since these solutions would imply big changes in the mechanics, tooling and fabrication procedure of the present SVX detectors, and thus large costs and efforts, it is rather being attempted to modify the detector coupling scheme. This would only add a 20% to the fabrication cost of the crystals.

On the basis of these arguments it was decided within CDF-SVX to proceed with a prototypization of layer # 1 and # 2 in a way which will be suitable for a radiation level two order of magnitude higher than the expected figure for the next run.

The limitation will be the shot noise: at the level of 1 μAmps of leakage current, with the present integration time, shot noise is going to be the main component of the electronic noise. The high luminosity environment, however, forces the development of faster front end electronics, and this, in turn, will reduce this contribution.

Collaborative work has started with Micron Semiconductor, with the goal of producing some AC coupled detector prototypes as of summer 1991. The scheme of these new detectors is outlined below.

Guidelines for the design.

We started from the experience of several groups which obtained satisfactory results by applying different techniques to bias the implant.

i) Punchthrough bias. It makes use of thermoionic injection of holes between two close p-type regions The bias is provided by a line close enough to each strip, kept at a voltage slightly higher than the operation voltage. It is used in the Aleph detectors.
ii) Foxfet regulation. An additional metal line on top of the oxide acts as a gate and allows to change the resistance. It is foreseen for the Opal detector.
iii) Polysilicon resistors. In this scheme resistors made of polysilicon are overlaid to bias the implants. It is used in the Delphi detectors.

There are no comparative measurements in the literature which would enable us to make a rational choice among these different bias techniques, in particular if we focus ourselves on the stability of the system in high radiation conditions. We planned our mask set such that will be possible to have a direct comparison of all these schemes.

In order to minimize the effort of rebuilding the detector we changed as little as possible all geometrical dimensions, pad lay-out etc.

We expect (but it has to be experimentally verified) that the detector will work as a DC detector in case of need, e.g. for comparison with the old series. In other words each electrode's implant will be accessible through suitable pads which will not be used in normal conditions.

Process sequence and electrical specifications.

The process will be similar to the one Micron developed and uses for the fabrication of the Opal detectors with the addition of optional polysilicon deposit in special series.

The mask set will consist of five masks:

a) Openings in the thick oxide which corresponds to the pattern of the implant.
b) Openings in the thin oxide in the spots where the metal should be in touch with the implant.
c) Metal deposition mask. This will produce the outer plate of the strip capacitors, reduce the impedance of the bias electrodes, provide the gate and produce all the pads for bonding and testing.
d) Polysilicon mask. This will produce the network of resistors between the implant and the bias line. This mask may be used or not.
e) Xylon openings. Allows the access to the pads after the final coating. This mask may be used or not.

Fig. 2a-e give details of these masks.

The steps of the process are basically:

1) Standard preparation of the crystal.
2) Growth of a uniform thick oxide layer (typically 1 μm).
3) Polysilicon deposit. Optional. Poly etch with mask d.
4) Oxide etch in the regions to be implanted (mask a).
5) Deposit of a thin oxide layer (typically .2 μm).
6) Boron implant. Ions have an energy such that they will only go through the thin oxide.
7) Etching in the region of the contacts to the implant and polysilicon (mask b).
8) Metal deposition and etch with mask c.
9) Xylon deposit. Optional dielectric surface protection.
10) If the deposit of Xilon is present (step 9)) one opens windows with mask e.

The source capacitance is expected to be the same as in the present CDF detector (~1. pF/cm).

The decoupling capacitance is expected to be at least 10 times bigger.

The interstrip resistance will be the same as in the present CDF detector (10^7~$10^8\Omega$).

The overvoltage to be provided in punchthrough operation ~ 15 V.

Gate characteristic and voltage, same as in Opal design.

Polysilicon resistors ~ few $10^6\ \Omega$.

Geometry.

The perimetral dimensions and thickness of the detector will be identical to the current CDF DC coupled design (see Fig. 3). The pitch is kept at 60 μm.

With respect to the cut line the layout of the electrode pads at the bottom end is almost identical to the current DC design (a change of 50~100 μm may be needed to provide room for the polysilicon resistors). There are more pads on the guard ring and a line to bias the polysilicon resistors.

Two special lines (one each side) are been introduced to access electrodes like the drain and the gate which are located on the other end and to daisy chain the detectors.

At the other end (top end) the bonding pads are moved inward by ~250 μm to leave room for the extra pads conctacting the implant. We do not believe this change will make bonding more difficult; in a sense it should become easier since the fan-out angle is reduced. At this same end the drain and the gate are located, with pads at their ends. In Fig 2 a cross section of this area is shown. One can see how the various electrodes overlap.

The markers at the center of the detector are kept identical to the ones of the current DC design.

The labels of the strip numbers (metal only) are moved inward, within the sensitive area such that they can be read even after bonding.

Operation schemes.

To operate the detector DC (present CDF) one has to connect the electronics to the first two rows of pads at the top.

To operate the detector in punchthrough mode (Aleph scheme) one has to leave the gate floating, ground the drain, rise the voltage of the back by 10 ~ 20 V above depletion. The polysilicon bias line will have to be left floating. The guard ring is grounded in the usual way.

To operate the Foxfet (Opal scheme) the gate should be connected to a suitable voltage. The guard ring should be grounded.

To bias the detector through the polysilicon (Delphi scheme) one has to ground the guard ring and leave floating both the drain and the gate.

A number of variations and combinations may be exercised.

We hope that this extreme flexibility will allow us to make eventually the best choice for a solid and reliable design.

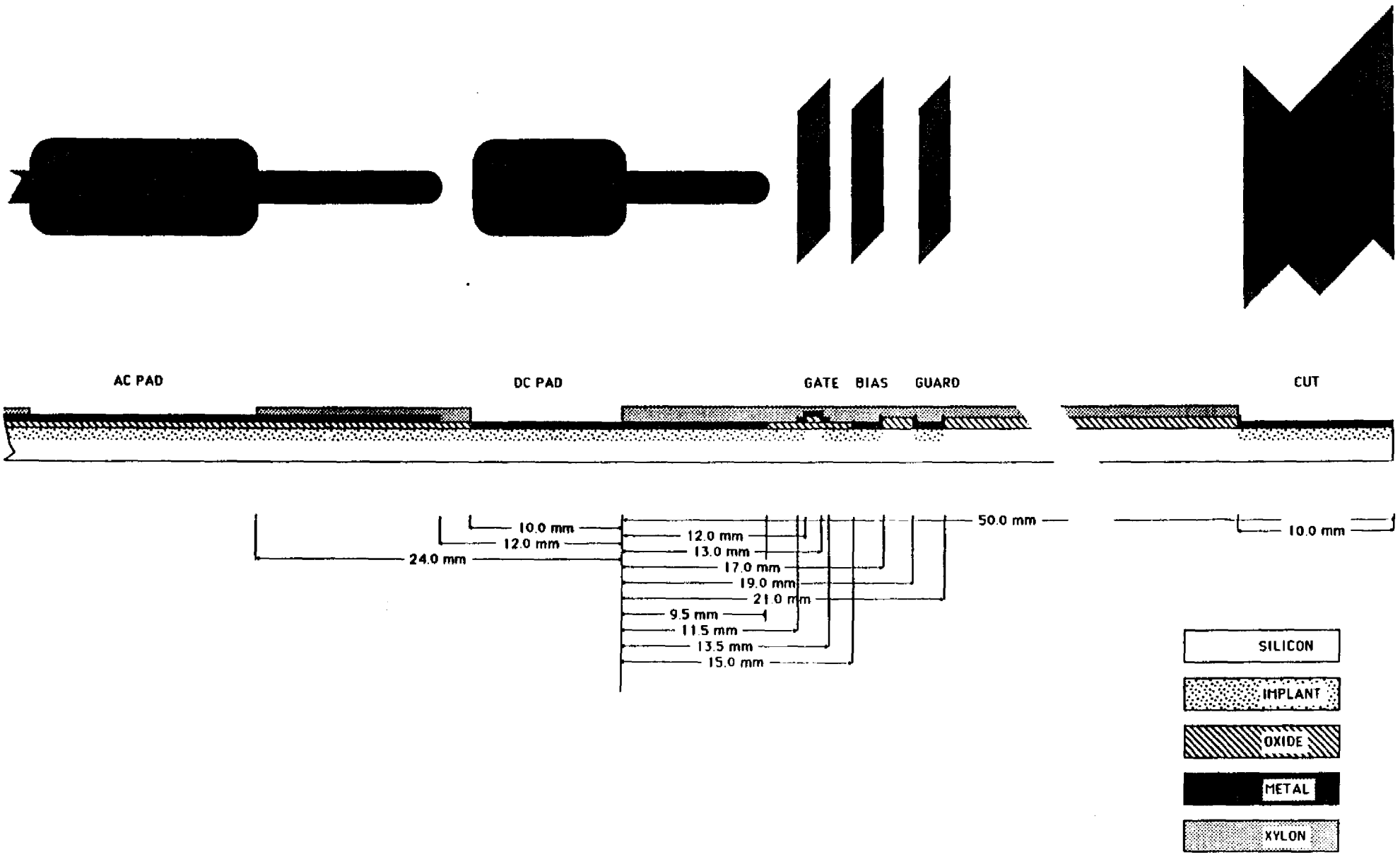
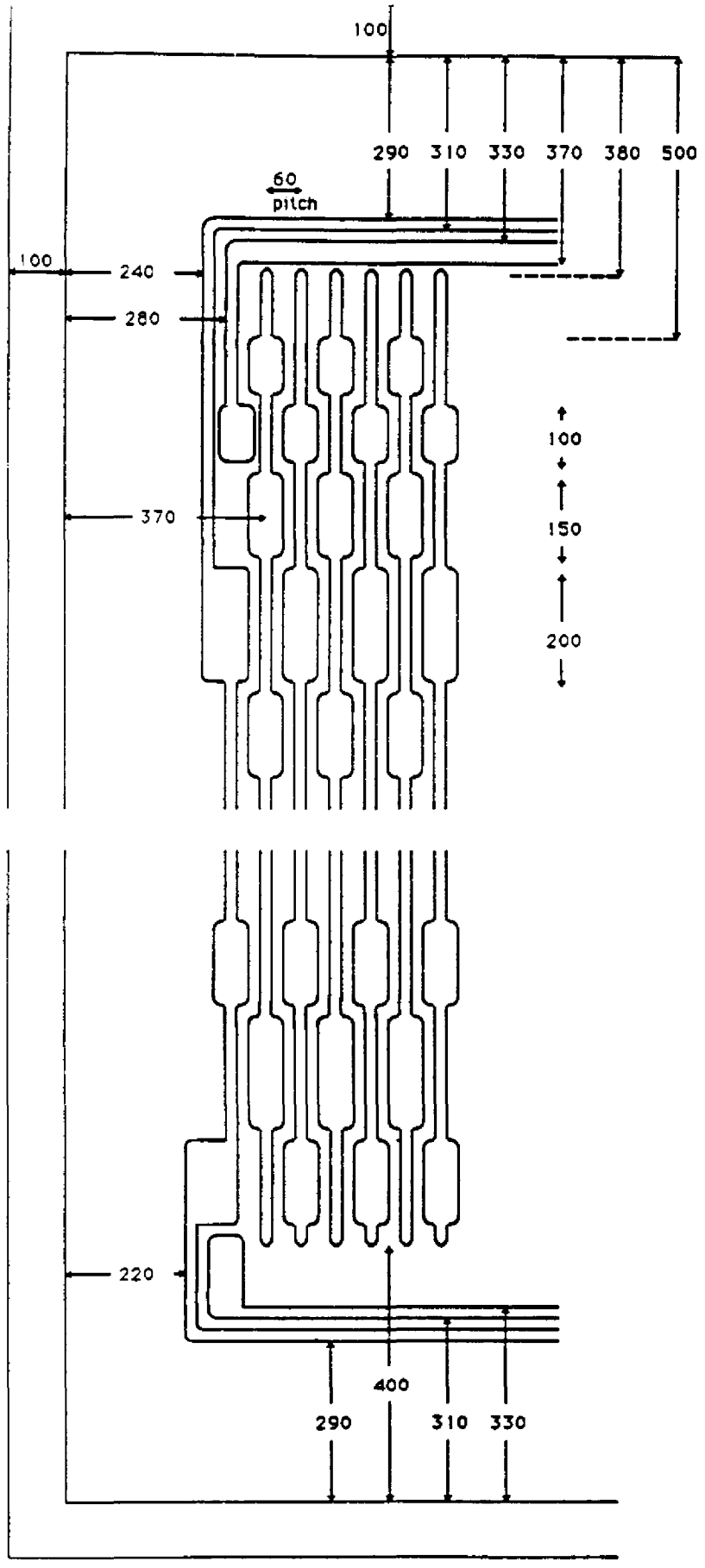


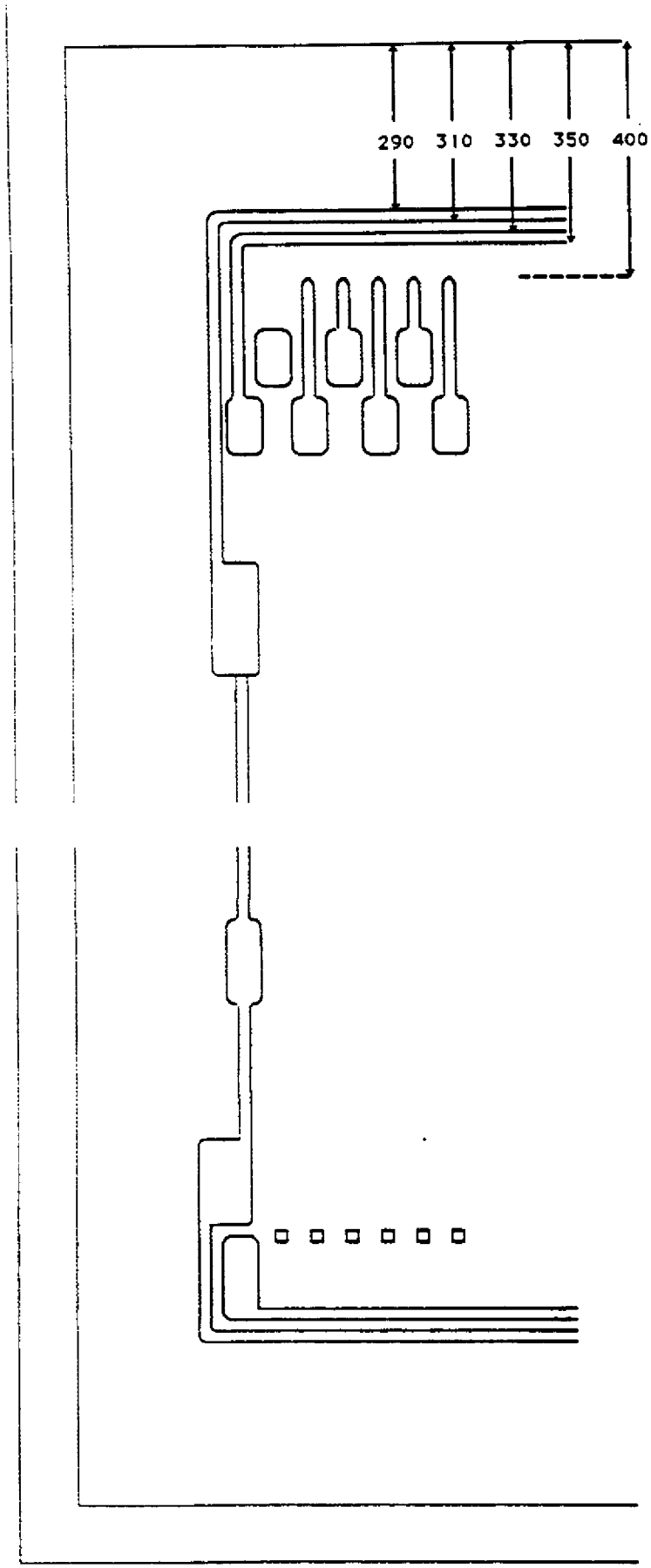
Fig. 1

Note: 1. mm indication corresponds to 100 µm real



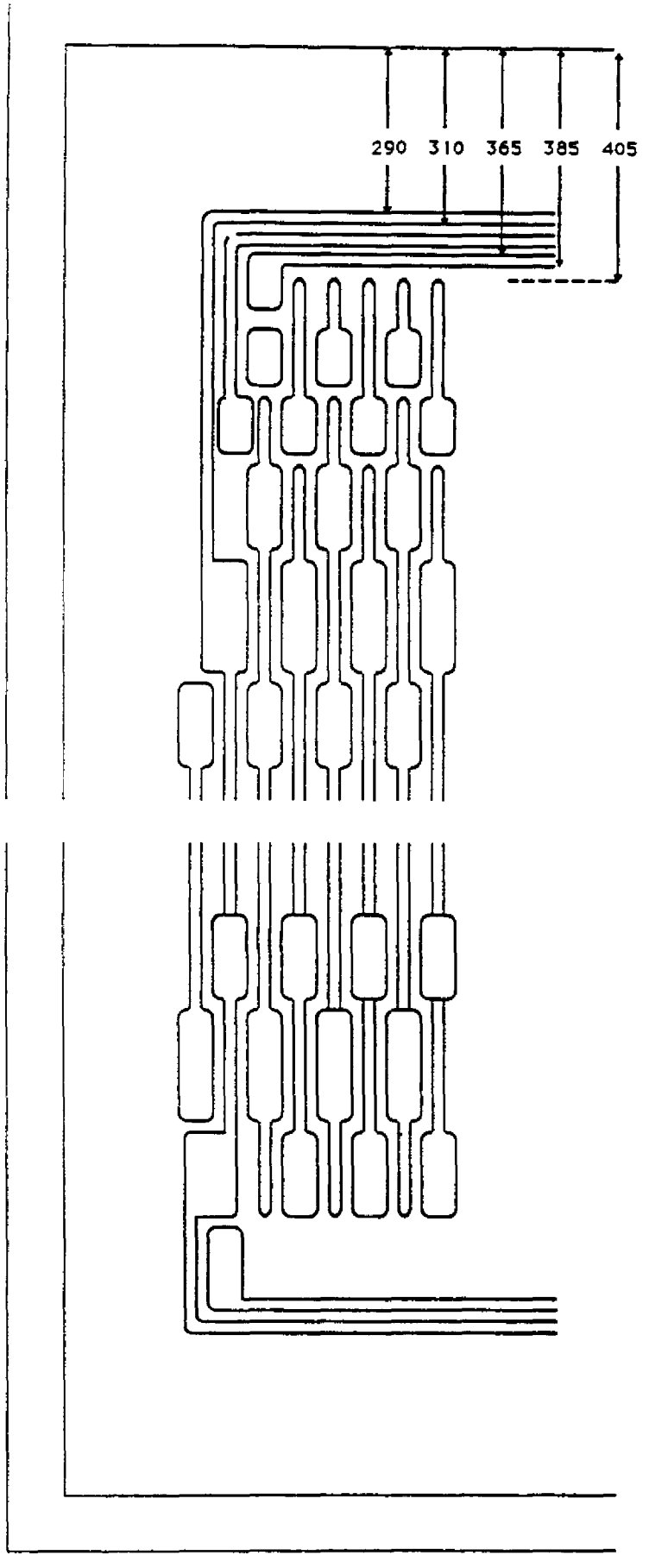
Openings in the thick oxide (implant)

Fig. 2 a



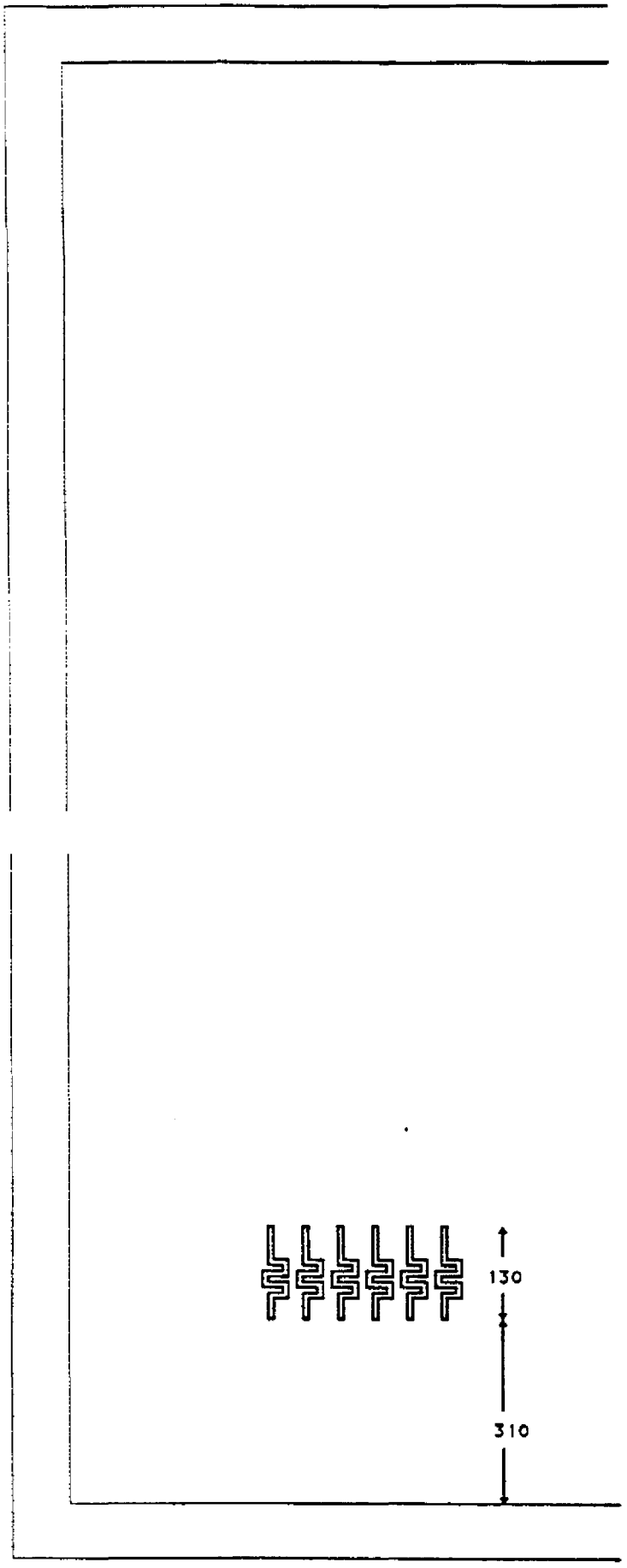
Openings in the thin oxide

Fig. 2 b



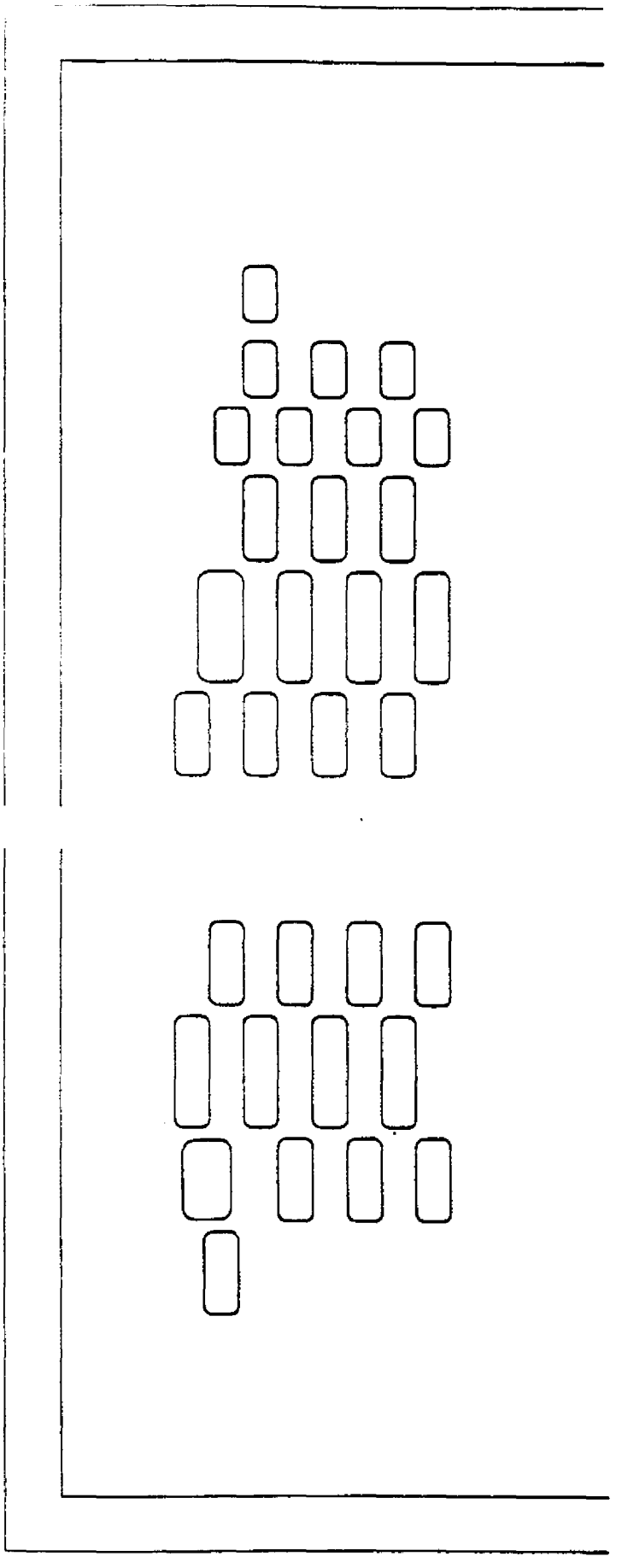
Metal

Fig. 2 c



Polysilicon

Fig. 2 d



Openings in the Xylon coating

Fig. 2 e

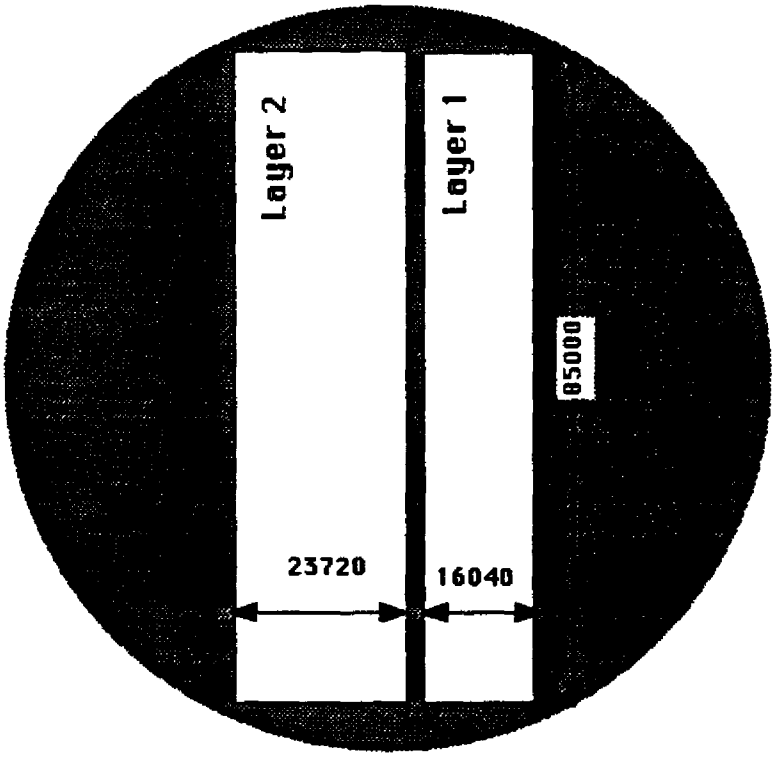


Fig. 3