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AN APPROACH OF TRIGGERING USING DRIFT CHAMBERS

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An Approach of Triggering Using Drift Chambers

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Abstract

This note describes an approach utilizing potentials of high precision drift chambers to make fast trigger decisions. Triggers with programmable thresholds can be generated well within $1\mu s$ after wire signals are collected. This is achieved by moving operations which tranditionally can only be done at higher trigger levels or off line with microprocessors or computers to the first trigger level. New generations of gate arrays, the key components of this design, make constructing such trigger system possible. I will use the SDC muon system as a model to demonstrate basic principles.

1 Introduction

The muon level-1 trigger will likely to be one of the limiting factors for the total length of millions of pipelines in SSC detector readout systems. The minimum amount of time required to generate a trigger using drift chambers is determined by the total drift time. For example, the drift time of CDF and D0 muon chambers is on the order of $\sim 1\mu s$. The delay for trigger decisions due to the long drift time of muon chambers is unavoidable. The question here is how fast we can generate a good trigger after signals are collected by signal wires.

Level-1 trigger circuits for large drift chamber systems are normally based on RAM type of look up tables and associated control logic circuits. An example of such trigger system is the ZEUS central tracking level-1 trigger processor.[1] The segmentation of trigger towers cannot be made very fine due to the capability of the technology. As a results, the quality of the triggers will be poor if such method is used for SDC muon trigger. This will become clear from the following discussion.

Trigger processors in high energy physics are conventionally constructed from MSI ECL or TTL 74xxx IC's and, in some cases, PLAs. Tracking trigger processors alone in a large scale experiment use tens of thousands of such IC's and hundreds of large size printed circuit boards. Such a system uses a lot of power and space. The reliability low. A SSC experiment will be an order of magnitude bigger in terms of channel co and the event rate is at least two order of magnitude higher than today's state of art detectors. The conventional approach are simply impractical.

Making trigger decision based on digitized drift time is time consuming. The TDC conversion time is normally quite long. The logic circuits required to manipulating the measured drift time, which might be 6-10 bit numbers, can be very complicated and slow, especially when the left-right ambiguities of drift chamber measurements are considered. It looks that as if trying to use the precision drift time information at the first level trigger is hopeless.

2 Programmable Cell Array by Xilinx[1]

CMOS Field Programmable Cell Arrays (FPCA) are rapidly replacing TTL, PLD (PAL) and EPLD devices in a variety of applications since their introduction in 1985 by Xilinx. The new sub-micron technologies allows FPCAs to be made bigger, faster and

cheaper. Examples of applications of FPCAs include: fast disk controller, multi-format VCR, high speed satellite earth station, programmable bet-slip reader and in flight reprogrammable missile target finding systems, etc. Comparing to PALs and EPALs, FPCAs are much bigger, more versatile and field programmable, i.e., the configuration of I/O ports, internal logic and routing are controlled by on board static memory cells or directly by workstations and can be configured and re-configured within 100 ms at any time.

The Xilins, started from the 2000 family in 1985, released 3000 family in 1987 which uses 1.2μ technology (Seiko). The new 4000 family scheduled for release starting later this year uses *AT&T* 0.9μ technology which will boost the speed by 30-40%. Now, the 5000 family is on the drawing board.

Architecture and Size

Currently, FPCAs are available in densities ranging from about 1,000 to 9,000 equivalent 2-input gates; larger devices, with up to 20,000 (more powerful) gates will be available next year.

The basic logic elements of FPCAs are Configurable Logic Blocks (gates and flip-flops). A simplest two bit adder can be built from 2 CLB's for the 3000 family and 1 CLB's for the 4000 family. The perimeter of CLB's provide a programmable interface between the internal login arrays and the outside world. There are 320 CLB's in addition of 144 I/O's on the currently available device. Unlike PAL's with basically a matrix of gates, these blocks (cells) are basic units which perform logic functions. There are crystal oscillators on chip. Complicated circuits can be made by programming the interconnecting network.

Xilinx, the most advanced FPCA producer, calls its products Field Programmable Gate Arrays (FPGA). I will use the name FPGA throughout this note.

Speed

FPGA performance is often measured in terms of the toggle rate of an internal flip-flop; devices with up to 100MHz toggle rate are available now. 130MHz devices (4000 family) will be available starting later this year. The performance (speed and size) of these devices tends to double every two to three years.

The actual clock speed that specific logic circuits, shift registers, counters and adders, etc., can operate is ranging from 20MHz to 70MHz depending upon the complexity and

design using 100MHz FPGAs. The normal system clock speed is expected to be raised to 50MHz for the 4000 diveces, which also feature on chip RAM with 5ns access time.

Design Tools

Xilinx sells software tools which can run on IBM PC or other more powerful workstations, such as Sun, Apollo and DEC stations. Programming FPGAs is in principle quick and easy.

Cost

The 1991 projected high volume cost for a 100MHz, 4,000 gate device is $15 (0.37c per gate!). Prices tend to decline as much as 30% a year. We will, however, likely use bigger and faster chips which I would estimate will cost $50-$200 per chip (depending upon the sizes of the FPGAs we use) by the time we are ready to purchase them in large quantities.

In the trigger circuit design described below, one or two trigger towers occupy a FPGA chip. Depending upon the choice of the system design, the total number of FPGA chips (likely to be 4006 or 4008) in the system can be as high as 10,000.

Summary

Xilinx FPGAs are extremely powerful devices which are ideal for very fast and complicated trigger processors required in high energy physics experiments.

3 Principle of the Muon Trigger Design

The scheme outlined below is only intended to demonstrate basic principles. Only single hit drift chambers are considered initially. Multihit trigger logic, although much more complicated, can be considered based on the single hit trigger logic.

The Minimum System

A minimum trigger system consists only one muon drift chamber station behind the toroid which has three wire planes with some kind wire offset. I will assume that the cell offset to be 3/8 of the full cell width. A minimum trigger tower consists five cells shown in fig. 1. Cells in the middle layer are assigned as 'key' cells in trigger towers. Two cells in other layers are associated with a key cell forming a basic trigger tower. Slopes of muon

tracks are measured by these towers.

Programmable trigger thresholds are assigned to each trigger tower. These thresholds are directly related to the track bending angle relative to the line joining the sense wire in the key cell and the beam center. This line is marked as a C-line in fig. 1. Suppose a muon is produced in an event. When it reaches the muon trigger chamber, four factors can make it deviates from the C-line: the finite beam bunch length, the finite key cell width, multiple scattering and the magnetic bending.

In the following discussion, the word resolution is not always used in its conventional meaning, i.e., the standard deviation of a Guassian error distribution of measurements. For example, I say an 8 cm wide drift cell located 8m away from the beam center has a angular resolution of $\pm 5\ mr$.

The bending power of the 1.5m iron toroid is given by

$$\theta = 800\ mr/P_t.$$

It is obvious that low P_t trigger thresholds (10-20 GeV/C) are rather easy to achieve.

The angular spread $\sigma\theta$ due to the multiple scattering, depending on the choice of calorimeter material, is about 1/3 of the bending. (We certainly favor iron calorimeter from this respect.) At 9 meters, the contribution from the finite beam length, which is $\sigma = 5cm$, is not very significant. Here, I will use a 4σ beam bunch length of 20cm ($\pm 10cm$) to represent the beam length. The contribution of the finite bunch length is given by

$$\delta\theta = \pm 10cm/900cm = \pm 11\ mr.$$

The contribution from the 4cm cell half width is much less than this and can be reduce even further by choosing smaller cell width of the key cells (more trigger towers). The relative contributions to the track angular spread from all four sources are illustrated in fig. 2.

Assuming hits can be measured to 1 mm at this level, the angular resolution of a trigger tower is 10 mr if wire planes are separated by 10cm. (This is much wider than that we proposed.) Obviously, this is not the dominate factor affecting the trigger sharpness in this trigger scheme at low P_t. The dominate factor is the multiple scattering. More precise slope measurements, however, are possible by extending the spacing between the two wire planes and by improving the single wire measurement precision.

Trigger thresholds are given as angles relative to the C-line. For example, 20GeV trigger threshold corresponds to $\Delta\theta = 40mr$. It is obvious that there is no problme, in principle, to make extremely sharp triggers up to $\sim 40GeV/c$ using this approach. Trigger efficiency will start dropping above this level.

Just for comparison, the trigger tower angular resolution of trigger counters with overlapping 5cm wide scintillator strips separated by 1.5m is $\sim 100\ mr(\pm 50mr)$.

How Are Triggers Made?

The most difficult task is resolving left-right ambiguities. Although smarter solutions for this difficult problem might be found, I only use more or less straightforward schemes in the discussion.

In order to calculate the slope of a track segment, the drift time has to be converted into coordinates in a local coordinate system for a trigger tower. A hit (drift time T) corresponds to two possible coordinates X and X' as indicated in fig. 1. We, therefore have to deal with three groups of numbers, $(X_1, X_1'), (X_2, X_2')$ and (X_3, X_3').

Slopes can be calculated for possible track segments, including ghosts. They are $(X_2 - X_1, X_2' - X_1 \cdots)$ and $(X_3 - X_2, X_3' - X_2 \cdots)$.

The next step involves matching numbers in the two groups. If two numbers are found to be equal, they belong to a true track and can then be joined together. The slope of a muon track after the toroid bending as well as the precise location of the track inside the trigger tower are then known. The left-right ambiguities, of course, are now resolved.

Finally, if the angle between the measured track slope and the C-line of that trigger tower is less than one of the given thresholds, a single muon trigger is generated.

TDC Start/Stop Time

The start time for the trigger logic is crucial in this trigger design. There are several ways to start/stop TDCs.

We can imaging that we generate trigger in the following way:

- A wire hit received by any of the five wires in a tower starts the clock for all other four TDCs.

- Wire signals received by these TDCs stop the clock counting.
- If no signals arrive within certain amount of time, every thing is reset.

Only time differences between the later arrival signals and the first arrival signal are measured which are not sufficient for reconstructing tracks always correctly. A track can be reconstucted only if it is always on the same side (left or right) of wires based on time differences measured this way. We have to know also the time difference between the event time and the first arriving wire signal.

The correct event time can be measured by the fast scintilator trigger circuits, the so called level-0 trigger. However, if we have to wait after this signal is received before starting the level-1 trigger processor, the time required to produce a level-0 trigger has to be added to the time required to produce a level-1 trigger by muon drift chambers. This could be a 200ns-500ns additional delay depending on where the level-0 and level-1 triggers are located. In addition, the wire signals have to be delayed accordingly in order to avoid loosing early arrival wire signals. From this point of view, starting the TDCs by the level-0 trigger is not a good idea.

Actually, the level-1 and level-0 trigger can proceed in paralell. In this case, the level-1 trigger logic is started by either a fixed rate clock or by the earlest arrival wire signal. Since the conversion time has to be as long as 800ns, there is plenty time for level-0 to make a decision. TDCs are now operated in a common stop mode. The level-0 trigger stops the counter counting. The time jitter of this stop signal will affect the timing precision.

Another factor affecting the timing resolution is the wire signal time jittering. The propogration speed of signals on sense wires is about 4ns/m. There is a $\pm 16ns$ time jitter for 8m long wire. Such time jitter has to be corrected in order to optimize the trigger tower anguler resolution. The lelve-0 outputs have to be able to tell the level-1 processor the rough location of the muon track along the wire, so that the level-1 processors can make corrections. Such a correction is simply a offset of the measured time.

Benifits of Redundant Measurements

Better triggers can be made with a four layer chamber module. The trigger tower will have to include 7-8 cells for a 4 layer system as indicated in fig. 3. There will be three groups of 4 possible track segments in a trigger tower. In spite of these complications, the track slope can now be measured more precisely and less mistakes will result since we

have much more ability to resolving the left-right ambiguities.

Moreover, the damage caused by wrong measurements due to soft electrons in some of the cells can be minimized since we now have redundancy. This is important for improving the trigger efficiency because we do expect that soft electron showers accompanying muons are big problems. This factor alone is enough to justify the need for four plane modules.

Triggers With Two Chamber Stations

Cosmic ray triggers which will likely dominate rate for the trigger system discussed in the previous section. The cosmic ray muon trigger can be suppressed by including in the trigger two muon chamber stations, one in front of and one behind the toroid. The system is shown in . 4. Correct track segments found in each station following procedures described in the above sections, are compared and the bending angle is measured to an accuracy of about 10 mr as mentioned above.

The inaccuracy caused by the finite beam bunch length and cell size can be avoid with triggers made with two muon stations. The smearing of muon track angles due to the large multiple scattering and interaction in the calorimeter is completely avoided. P_t trigger thresholds up to 50 GeV/c are possible using this method.

Only two muon chamber stations are involved in this scheme. Comparing to the trig schemes which require all four muon drift chamber stations, we can benefit in two ways:

- The cable interconnections and the resulting time delays are reduced.
- The muon chamber station right after the return york can be eliminated because its only function is for triggering muons.

Although the angular smearing effect of the 5 cm beam size is now removed, the angular resolution of each trigger towers are not enough to allow us to have sharp high P_t (100 GeV/c) threshold triggers.

A 100 GeV/c muon has a bending angle only 8 mr. The trigger tower angular resolution has to be better than this.

Triggers With All Four Supermodules

If track locations are measured to 3 mm by a muon station, the angular resolution of a track is 4 mr assuming two muon stations are separated by 1.5m. The combined error

for two measurements, one before the toroid and one after the toroid, is about 6 mr. So, 3 mm ($\sigma = 1\ mm$) position resolution for each muon station is what we need in order to generate good triggers with up to 100 GeV/c threshold.

This looks very easy to achieve. However, the hard job is to resolve the left-right ambiguities which involve track segment matching. The approach discussed above can then be used for this purpose. In addition, each trigger processor (a FPGA chip) can give an output indicating expected locations of tracks in other stations.

4 How to Realize These Ideas?

Difficulties

The position measuring precision of drift chambers has never been fully utilized in the past at the first trigger level. Here, I define the level-1 trigger as a trigger within a few μs or less. Normally, big drift chamber cells, 1cm to about 10 centimeters in size, are used as basic trigger units forming trigger towers in some of the experiments. Large drift cells may be devided into smaller regions. Trigger processors are normally constructed from look up tables which store the allowed hit patterns. Only very crude track direction information can be obtained at the first trigger level.

If we want to achieve high precision position measurements at the first trigger level, two very difficult obstacles have to be overcome:

- The conversion time of conventional TDCs, such as LeCroy 2229s and 1879s are very long. LeCroy is developing zero conversion time TDCs. However, in order to truly solve this problem, the data transfer speed from TDCs to trigger processors has to be extremely fast too.
- The trigger logic required are too complicated.

  As discussed in previous sections, resolving the left-right ambiguities and calculating track slopes require very complicated processors and thousands of such processors are needed in a large scale experiment.

Drift Time Measurements With FPGAs

The of FPGAs can be conured as multichannel pipeline TDCs with zero conversion time. Those low time resolution TDCs are basically fast binary counters. The time reso-

lution of such TDCs, though low, is sufficient for the triggering purpose.

The actually wire hits, the discriminated signal from a wire amplifier card are connected to FPGA inputs. Counters wihch measure the drift time by simply counting the clocks, are started by wire signals. A level-0 trigger stops the counting and also provide the track location information along wiers to the trigger processor for necessary timing corrections.

Fast counters, 8 bit in length for example, count the clock cycles and record the drift time of each wire. The recorded drift time is immediately available for further manipulation by the logic circuits on the same chip after the clock is disabled by a wire signal eliminating the need for data transfer through cables and controllers.

Counters conured in 100MHz FPGAs using the carry look-ahead technique can run as fast as 40MHz resulting a time resolution of 25ns ($\sim 8ns$ rms) corresponding to a position resolution 1.2 mm ($400\mu m$ rms). The carry propagation is always the speed limiting factor in counter design. 60MHz counting rate, synchronized with the SSC clock, is possible with devices Xilinx is about to release. The rms resolution of these TDC's can be reduced to $250\mu m$.

After a signal from a wire is received, the FPGA will search for hits from other wi in a trigger tower. If no hits are found within the full drift time (800ns for a 4cm half width cell), this signal will be reset. Track slope calculation begins if all three hits are found.

Time to Coordinate Conversion

Parallel binary adders and subtractors, which are needed for doing the required calculations, can be conured easily in FPGAs. Each 8 bit adder or subtractor requires 8 CLB's in Xilinx 3000 family. The speed of the adder/subtractor is about 40ns per operation for the simplest desgin. Again, the 4000 seriel Xilinx FPGA will allow us to run simple adders/subtractors at 50MHz speed and a 8 bit adder only require 4 CLB's. Faster operation is possible also by using fancier design which require more CLB's.

Wire locations, including the alignment data, are stored in the chip. The measured drift time cab be converted into coordinates in the local coordinate system easily by adders/subtractors, associated control logic and memories in parallel for each wire.

Such conversion can also be done at the end of the slope determination because only a overal offset is involved.

Track Slope Determination

The hit coordinates from two wires in two layers of chambers are fed into subtractors for slope determination by calculating the differences between the coordinators pairs, X2-X1, X2-X1', $\cdots$ Results are 4 numbers representing slopes of a correct track segment and three ghosts. We have two such processors in our minimum trigger system with three layers of drift chambers. This operation requires four clock cycles. Four parallel subtractors can do the job four times faster than a single subtractor.

The next step is linking the track segments by comparing the numbers in two groups. There are 16 possible combinations. This can be done using four comparators within four clock cycles or one comaprator in 16 clock cycles.

Slopes of matched two track segments are then added together and sent to the last stage for the finaltrigger determination.

Final Trigger Decision

The last step is to compare the measured track slope with predetermined trigger thresholds. Comparators, one for each threshold, can be used. A trigger bit for each thresholds can be flagged for output if the track slope is found to be within the limits of a P_t threshold.

The trigger processor flow diagram is given in . 5 and . 6.

Triggering With Two Muon Stations

The track slopes measured by two muon chamber stations, one before and one after the toroid, can be compared using another stage of logic. The bending angle of a muon track by the toroid is then directly measured. The required number of trigger processors, of course, is doubled.

5 Last CTC Stub and Φ Trigger

Φ triggers based on the central solenoid bending independent of the Θ triggers based on the toroid may be very useful to reduce the single muon trigger rate. Simple Φ triggers

can be made by measuring the slopes of track segments in the last stub of the central tracking chamber (CTC) where the ocupancy is relatively low using the same method described above.

We measure the angle $\beta/2$ (. 7) which is given by:

$$\beta/2 = 0.3BD/2 = 0.3 \times 2.0 \times 1.8 \times /2 = 540\ mr/P_t.$$

If slopes of track segments can be measured to a precision of about 10 mr, P_t threshold can be set as high as 50 GeV/c. 1 mm signle wire resolution achievable with the FPGAs should be sufficient here. Combining this information with tracks found in outside muon Φ chambers, a muon Φ trigger can be formed.

6 Final Remarks

The trigger method outline above utilize the great power and versatility of the FPGA logic devices. Advantages of this type of trigger circuits are clear. Although only muon trigger application is discussed in this note. FPGAs can, in fact, be used making trigger processors for all kinds of tracking devices.

The final muon trigger processor design will be based on the Xilinx 4000 family wh' will be available in 1991. We have, however, started a program in Seattle intended demonstrate the feasibility of this method using the Xilinx 3060 or 3090 chips and plan to upgrade to 4000 serial whenever it becomes available.

7 Acknoledgement

I would like to thank R. Davisson and W. Dougherty for introducing the FPGA devices to me and W. Dougherty for some stimulating discussions at Snowmass.

References

[1] R. Halsall et al., The ZEUS Central Tracking Detector First Level Trigger Processor, IEEE Trans. NS-37, 1203 (1990)

[2] Xilinx Programmable Gate Array Date Book, 1989

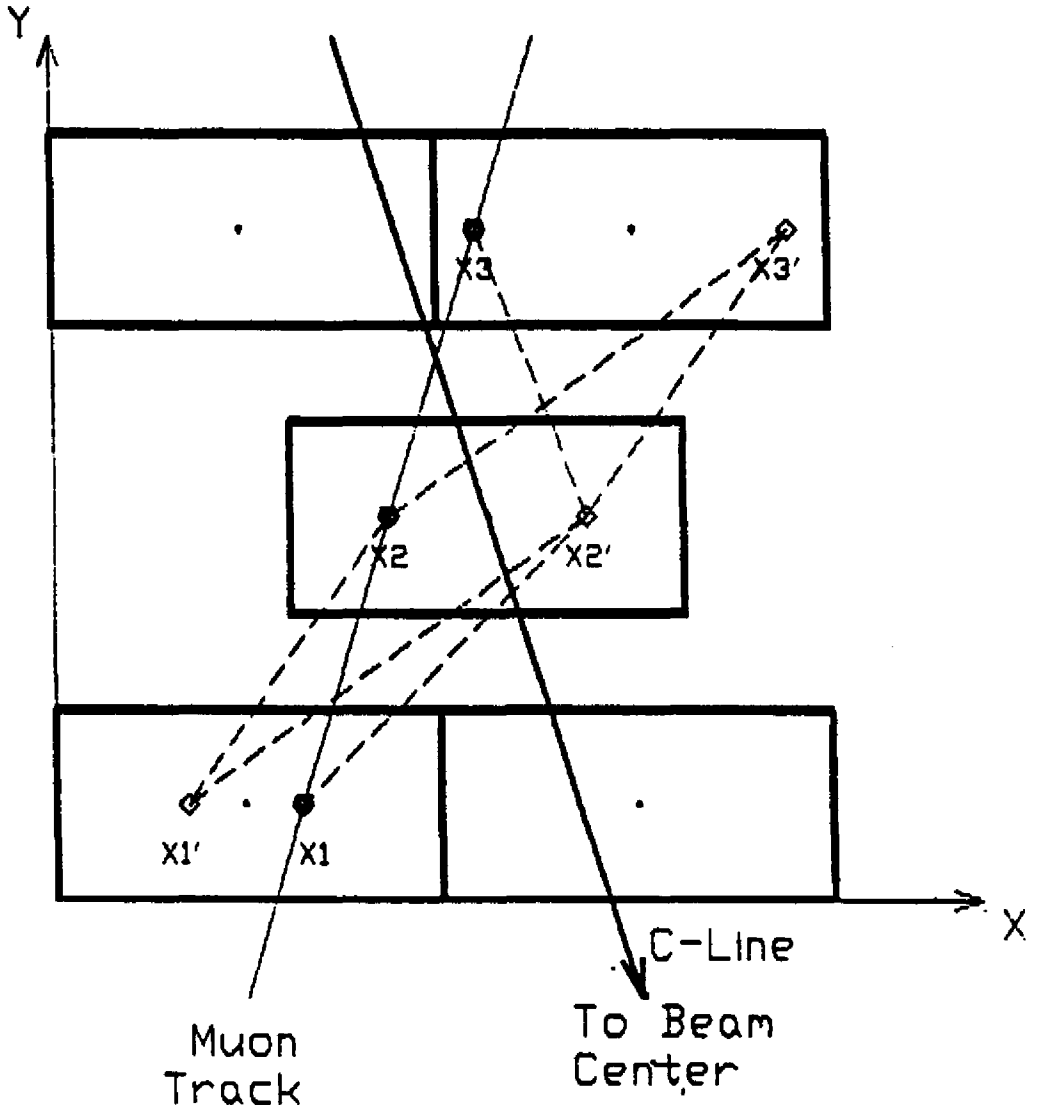


Fig. 1. A five cell trigger tower. The C-line from the wire in key cell to beam center is shown. A muon track generates 3 hits and 6 possible coordinates. 8 possible track segments, including 6 ghosts are shown.

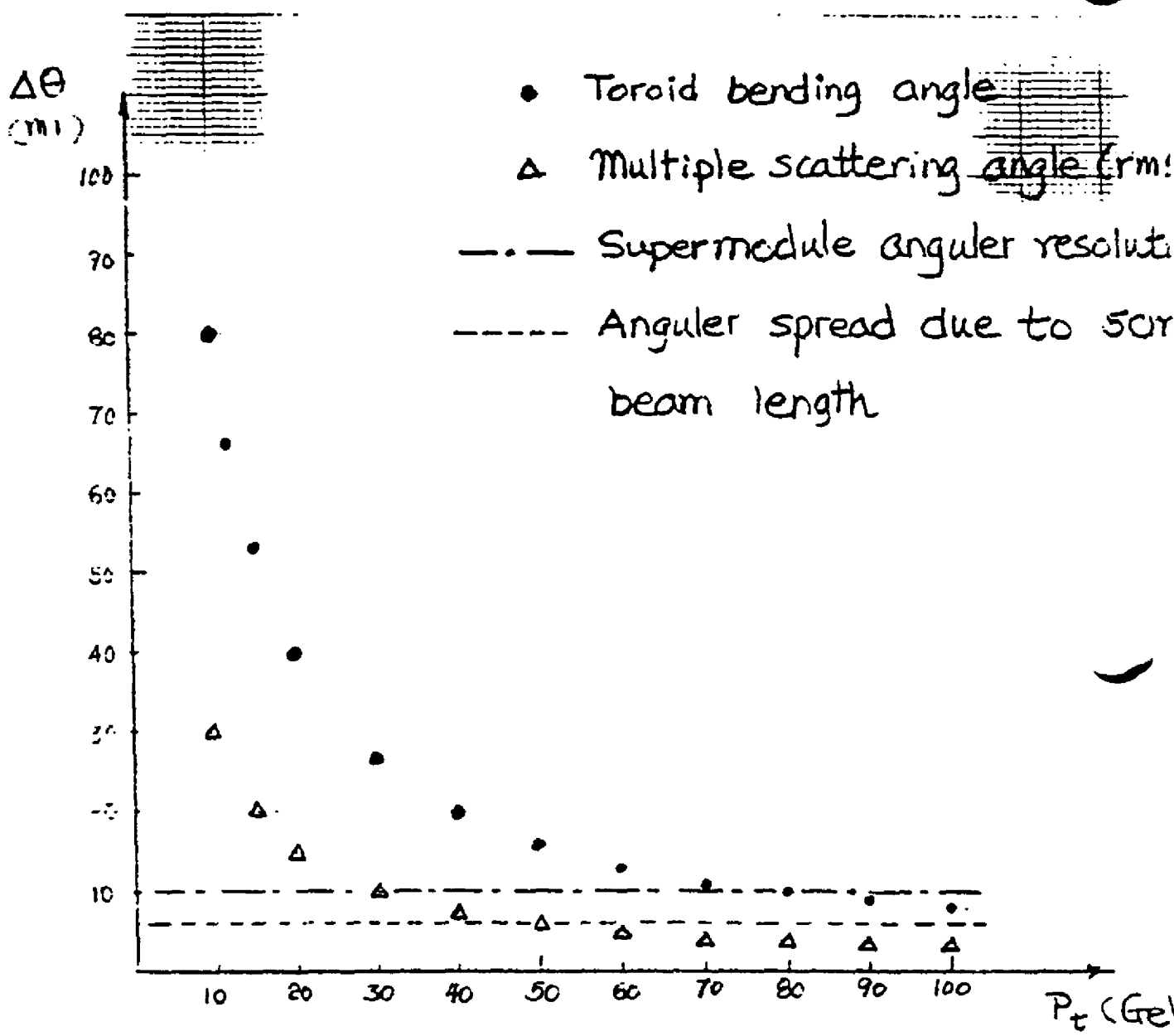


Fig. 2. The toroid bending power and errors of muon track slope measurements.

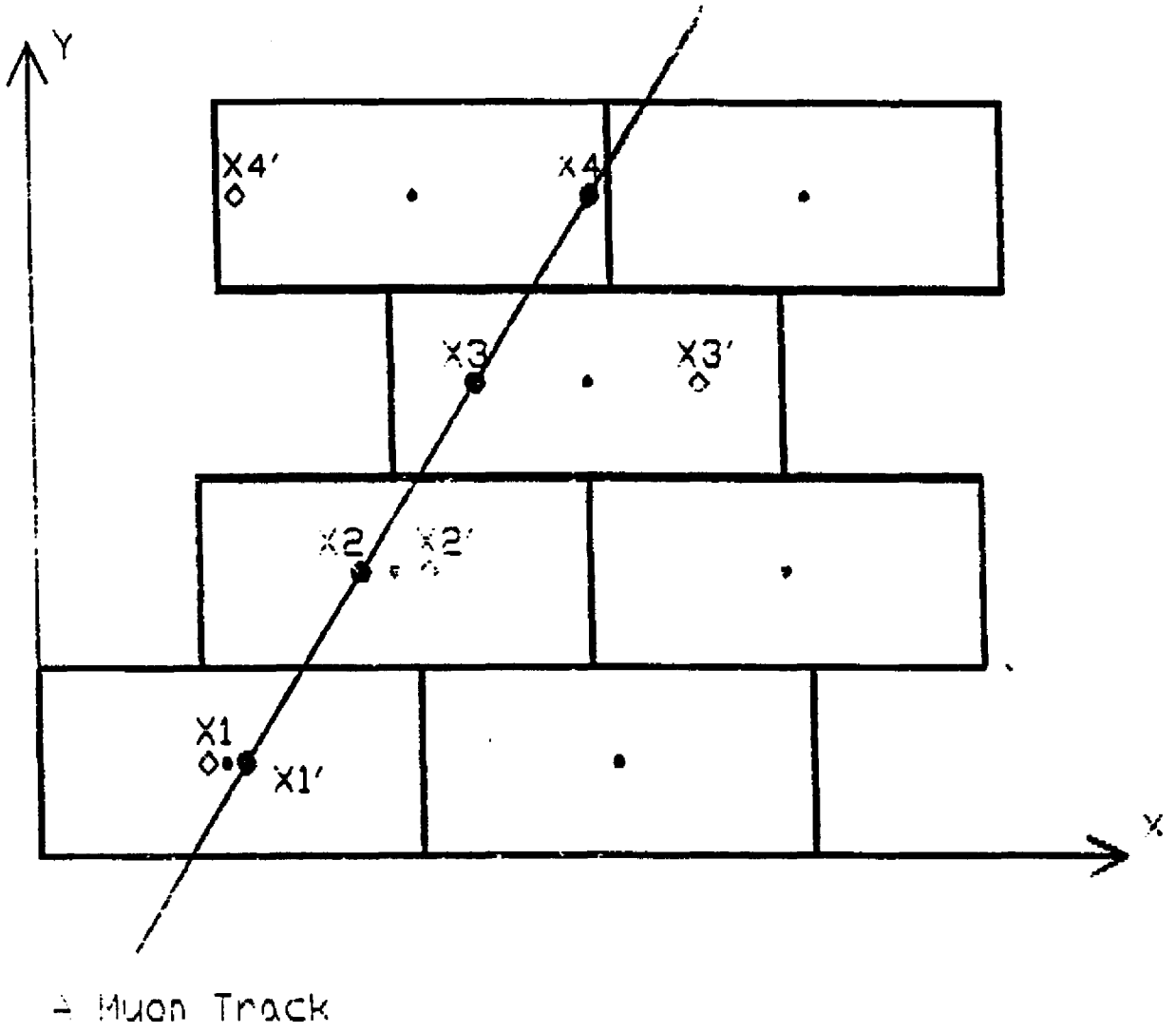
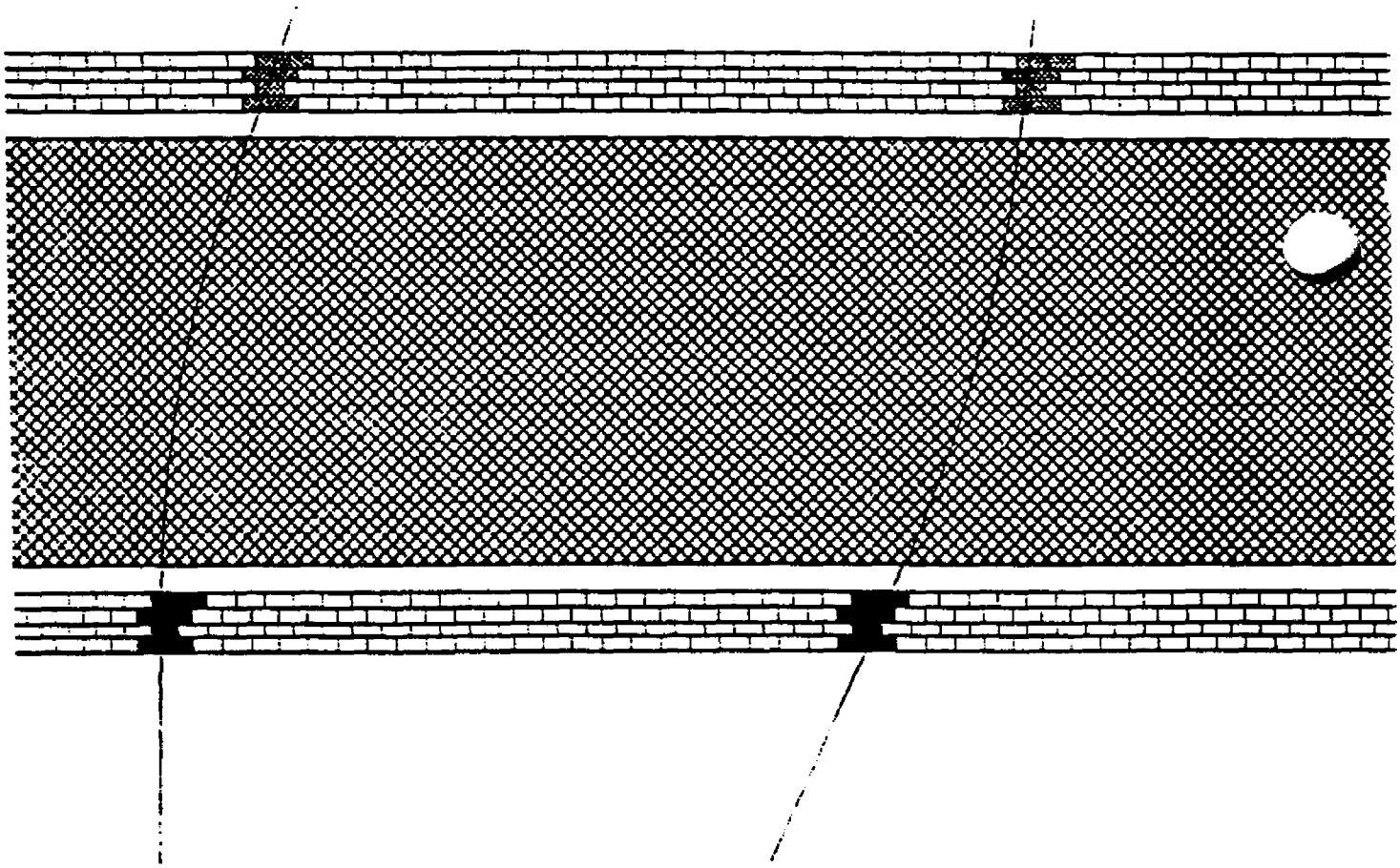


Fig. 3. A seven cell trigger tower with wire offset. X1 to X4 are true hit coordinates X1' to X4' are ghosts.

Fig. 4. Triggers with two supermodules of muon chambers.



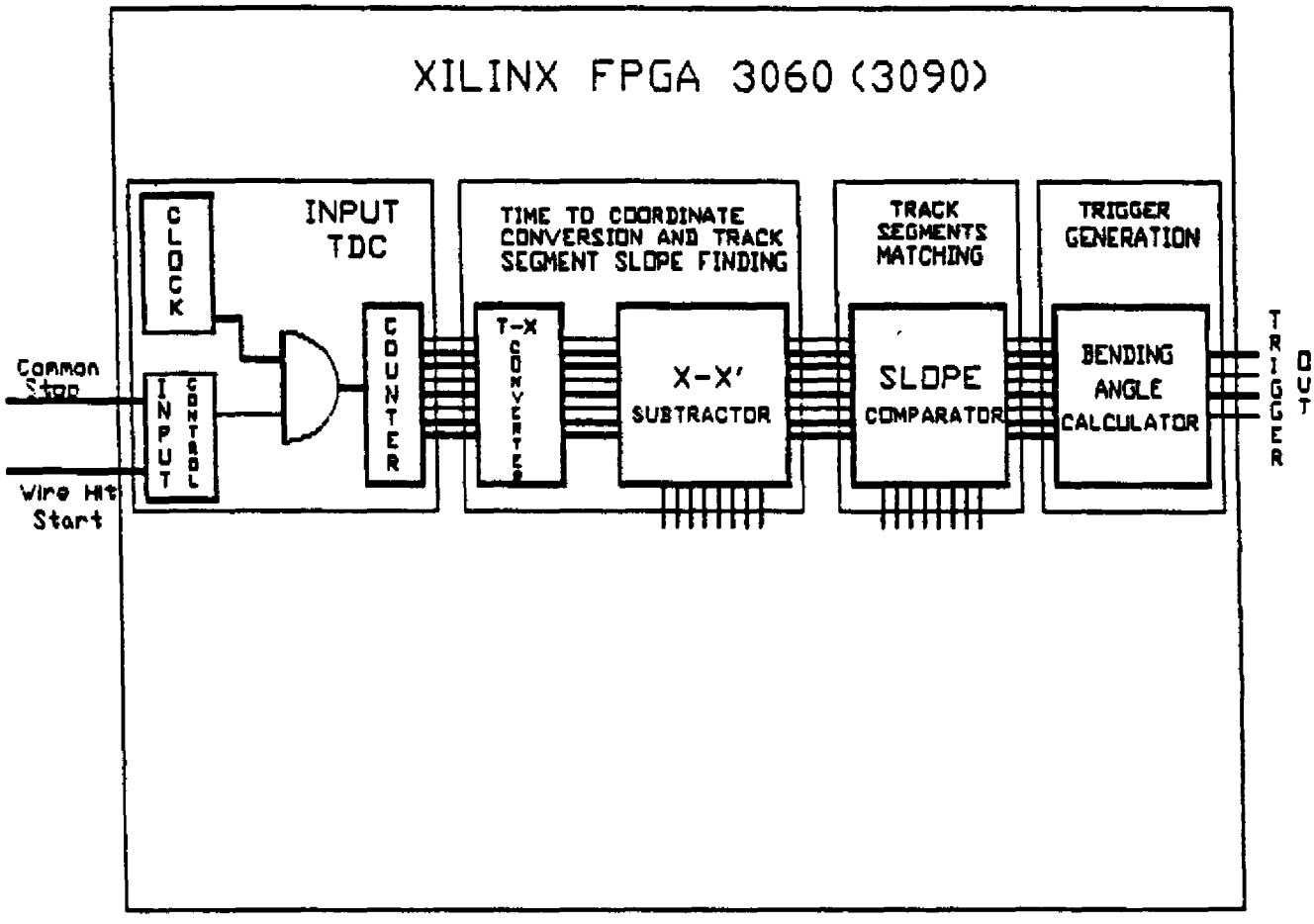


Fig. 5. A simplified trigger diagram

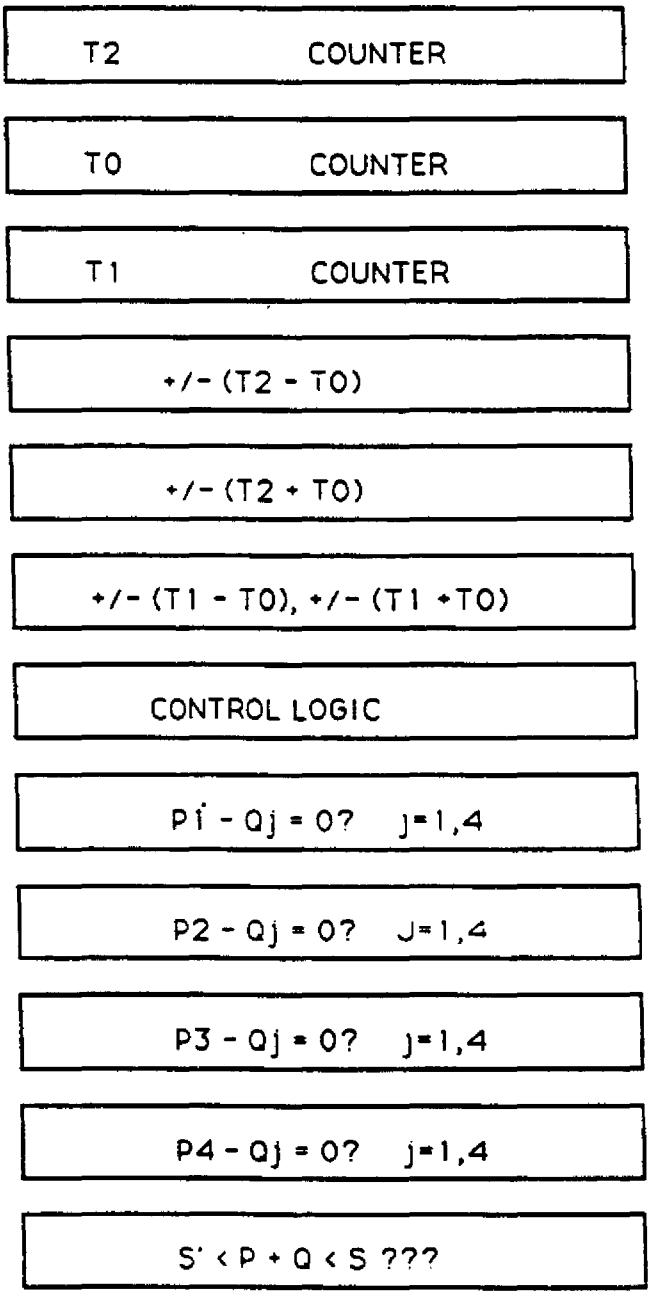


Fig. 6. The simplified flow diagram of a trigger processor. A trigger can be generated in 10 to 20 clock cycles.

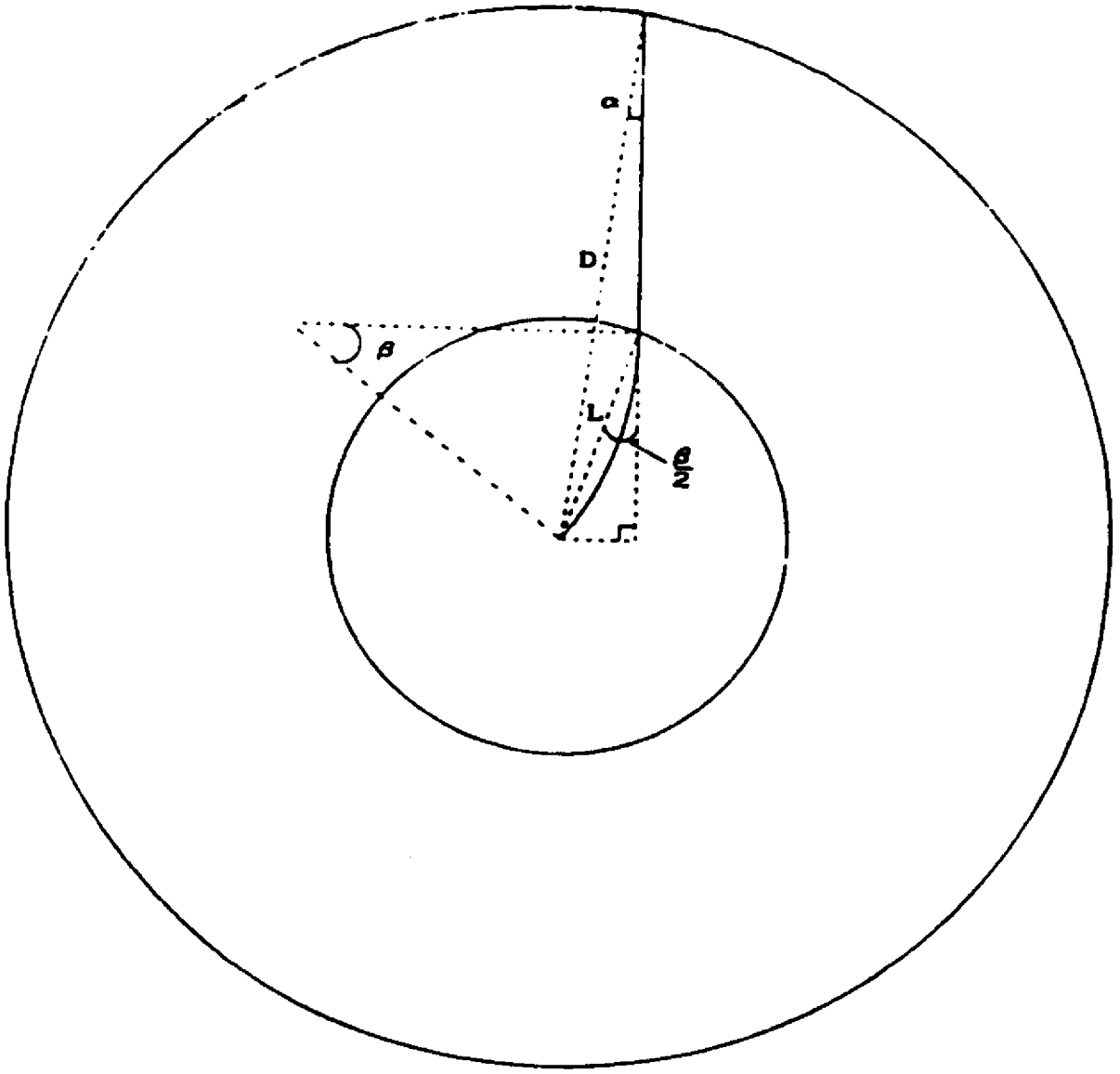


Fig. 7. The solenoid bending. An independent phi trigger can be made by measureing the track angle in the last stub of CTC.