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SOLENOIDAL DETECTOR NOTES

DEVELOPMENT OF AN INTEGRATED PIXEL DETECTOR

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We are developing a pixel detector in which the electronics is integrated directly on the silicon of the detecting diode, as described in the original SSC generic R&D proposal [1]. Our collaboration is a continuation of the development effort that produced the Microplex chip, now in use in the Mark II detector-the first integrated circuit to provide direct 1:1 scale readout of a silicon strip detector [2], [3]. Keeping the signal charge on a small structure on the same wafer, helps to keep the capacity low and the signal to noise ratio high. The integrated structure also keeps the detector thin and the pixel size small. The detector is free from ambiguity even in dense jets, and should significantly improve both pattern recognition and vertexing capability.

1. Design

The basic idea of the detector, described in more detail in reference [4], is summarized here, and sketched in Figure 1.

(a) Ionization charges, generated in the depleted intrinsic region of the diode are guided to small, low-capacity collection electrodes which are connected, through the channels of transistors that can provide isolation for the charge during readout, to the gate of a nearby signal transistor.

(b) These transistors and other on-pixel electronics are contained in an implanted well in the substrate, rather than directly in the high-resistivity intrinsic silicon. The well, which provides an optimum doping level for the operation of the transistors, acts as a Faraday cage-like shield to prevent transistor switching transients from altering the collection field. Most importantly, the well is a charged structure which guides all of the ionization charge from the bulk to the collection electrode, preventing it from drifting to the bottom of the readout electronics, where it would be lost for readout.

(c) Thus, the entire central, detecting region is sensitive, including the area under the pixel electronics. The charge can be reset rapidly and simultaneously on all pixels, or can be allowed to bleed off slowly with a time longer than the trigger delay time but short compared to the time between hits in the same pixel. This "continuous reset" preserves hits that may later form part of a triggered event while preventing cluttering of the pixels with old hits. The bleed rate can be adjusted with a control pulse.

(d) During readout, the charge on the signal gate controls a current that flows from a nearby column conductor to an adjacent row conductor, and then out to the readout, rather than letting the ionization charge itself spread out on a high capacity output electrode.

(e) Sparse field readout techniques which provide hit-pixel data with no x-y ambiguities will be used. In the simplest scheme, one column at a time is activated, and all row currents are detected simultaneously. If no hit is found, the next column is activated; if one or more hits are found, they are read out in sequence using a priority encoder, with no significant time spent on the intervening rows. The hits will

correspond unambiguously to the pixels at the intersection of the activated column and read out rows. A following version will place low noise amplifiers on each pixel, discriminators on the column outputs, and detect struck columns with another priority encoder.

(f) This architecture will be compatible with the suggestion of David Nygren and Helmuth Spieler [5], for adding a time tag to each hit, something that will be necessary for pixel devices used at the SSC.

(g) A similar architecture could also be used to read out the short silicon strips proposed by Alan Litke and Helmuth Spieler [6].

(h) One important addition to this scheme was made by Walter Snoeys, the Stanford Electrical Engineering graduate student who is working on this project for his Ph.D. thesis. The original design placed the diode at the collection electrode, on the side (the "front" side) with the readout electronics. This is similar to the arrangement normally used with strip detectors, which have the diode immediately under the collection strips. The electric field is strongest at the diode junction, where opposite signs of uncovered charge meet, and is further intensified as the lines of force converge from both the back side and from the well. Thus, placing the junction there limits the permissible size of wells that hold the electronics. Detailed modeling shows that high junction fields, in addition to making breakdown more likely, makes full depletion of the silicon under the wells more difficult.

Placing the diode on the back eliminates all these problems, and allows the use of large wells that can contain the sophisticated electronics needed for a complex SSC readout. Figure 2 shows this general scheme. Figure 3a shows the current flowlines for a properly

biased well; all end on the collection electrode even though it occupies only 4% of the pitch width. Figure 3b shows most lines under inadequate bias ending on the well; the magnitude of current flow is about 300 times greater in this case.

This scheme does add two problems. (1) The device can now operate only if it is fully depleted. The side away from the junction is the last to deplete. With junction on the backside, all the pickup electrodes on the front side are shorted together until full depletion is reached. (2) The need to end the diode before the (conducting) chip edges, requires back side lithography in combination with high resolution front side lithography, technology new for Stanford's CIS. Overall, we expect that the great advantages of the new structure will more than compensate for these disadvantages.

The overall project involves three separate tasks: (a) designing a new fabrication technology, (b) providing a readout capable of meeting SSC needs, and (c) making the detector radiation hard. The first requires a technology which must concern itself with the fields throughout the volume of the wafer, rather than just near the surface, and for a wafer made of a type of silicon (float zone, high resistivity) that is not normally used in the industry. The second task is similar to the development of the Microplex chip, but is more difficult. That project took two years. Other readout chips, finished later, have taken three in five years. To date we have concentrated on the first two tasks.

The results thus far — described below — are that standard CMOS steps plus three additional ones, all now developed, will do the job.

2. Progress

Eleven major steps were listed in the University of Hawaii FY 1988 renewal proposal, before the start of this project in the summer of 1988:

1. Select a fabrication technology.
2. Design test structures, test procedures, and a complete device.
3. Complete detailed field calculations.
4. Acquire information on detector fabrication.
5. Acquire information on transistor fabrication.
6. Continue radiation hardness studies.
7. Select a fabrication facility.
8. Investigate possible collaborations with other HEP groups on the either pixel development or radiation hardness investigations.
9. Fabricate devices.
10. Test devices for radiation hardness.
11. Run beam tests.

ITEMS 1, the first two parts of 2, and ITEMS 3, 4, and 7 were completed by August 1989. The work involved in the third part of 2, designing a complete pixel detector, is comparable to that in the design of the Microplex chip, except that that was done with an already developed technology.

Layouts for the first two types of pixel devices planned were started in January 1990 and now have been completed. They have a simple readout with x and y shift registers, and will require all pixels to be read out. In addition, a third, also completed, does not have individual pixel readouts, but has discriminators on the column outputs to test our ability to measure the time of a hit somewhere in that column. This will be needed for SSC running where hits must be time-tagged, so that a triggering event can be

picked out of the hundred or so following ones that come in before the trigger time.

The first type with a 5 by 14 array of 30 x 83 micron pixels, has the simple one-stage amplifier described in [4]. The second type, with 5 x 14 and 10 x 30 arrays of 34 x 125 micron pixels, has two multi-stage, double correlated sample-and-hold, low noise amplifiers which will permit the detection of smaller signals. This amplifier was designed by G. Rosseel, a recent Stanford Electrical Engineering Ph.D. experienced in analog design. The layout program, MAGIC, provides a facility for the automatic derivation, from the layout, of the parameters necessary to run SPICE, a circuit simulation program. Simulations were carried out for all designs. Two-micron poly and three-micron single-level metal were used. It is expected that finer lines and double-level metal could be used in the future, but it is also likely one will want to add more electronics within each pixel, with the present sizes remaining typical of what will be available.

ITEM 5, Transistor Fabrication Steps: The detailed steps needed for transistor fabrication, had been planned to follow the steps in the existing CMOS/BiCMOS run sheets, as far as practicable. (BiCMOS, a recent development in fabrication technology, combines bipolar, NMOS, and PMOS transistors on the same substrate, permitting simultaneous use of high impedance, low power circuits and powerful, high current drive transistors.) However, some significant changes were necessary to accommodate a diode that spans the wafer thickness, and to allow for backside lithography, neither of which are found on standard MOS circuits. The three major additions were (a) an extra well, making the process somewhat similar to the twin tub CMOS process, so no transistors are directly in high purity silicon; (b) an

effective getter for impurities, to preserve the high purity during high temperature steps; and (c) double sided lithography.

The getter will be phosphorus in polysilicon, as described by Steve Holland [7], and will form the backside of the diode. The bulk, then, will be of P type (100) silicon, which has the added advantage of hardness with respect to radiation induced doping changes. For now, we will not use bipolar transistors. Although they would be nice for driving any long output analog lines, bipolar transistors are not needed now and would only add mask steps and complications.

In addition to the remaining 13 masks for the front, an additional 3 will be needed on the back, because the diode junction, which is inside the surface at the back side, must be terminated well away from the wafer edge and from interchip saw edges, all of which will be conducting.

Prior to completing the detailed calculations for the modified process steps, it was decided to do an initial fabrication run to produce the diode test structures. This was to let us study any possible problems in producing deeply depleted diodes on high purity silicon at CIS, to measure the diode leakage currents, and to identify their sources. The test structures were on the front side. The diode, on the entire back of the wafer, was kept from the edges with crude lithography. The run was started in September 1989, and ended in December. The diodes had too much leakage; defects were too numerous to permit wafer-scale diodes. In addition, a number of wafers were lost from several problems during the fabrication, including the October 17 earthquake, leaving an inadequate number at the end.

In part this was due to our starting a limited number of wafers, as the cost from Topsil, one of the two European suppliers, had gradually climbed from $36 to $283 per wafer. (There are currently no U.S. suppliers. The U.S. sales

offices of the other European company, Wacker, and the two Japanese companies did not seem interested in giving quotes or accepting orders.) It was clear we needed better backside lithography to permit us to go immediately to individual chip-sized diodes and a supply of less expensive silicon so we could start more wafers on the primary run and have a backup run following along as well.

The silicon problem was unexpectedly solved at the September 1989 Barcelona instrumentation conference. Dr. Peter Dreier of Wacker gave a talk on silicon manufacturing in which he mentioned that high resistivity P type (the kind we needed) was "easy" to make. With a direct contact inside Wacker, we were able to purchase an 8.2 kg, 10 cm diameter ingot. This will give us a supply of several hundred wafers at a raw material cost of $11 per wafer. Sawing, grinding, edge rounding, and double sided polishing by a local company brought the cost, for a small first order, to $87 per wafer.

Two major problems were expected to dominate double sided lithography: (a) each side had to be protected from even minute scratches when it was facing down during lithographic steps on the other side and (b) the pattern on the back had to be properly aligned with the one on the front. In principle this can be done using an infrared aligner, since when the photon energy is below the bandgap, silicon becomes almost transparent. However, the one infrared aligner at CIS did not have adequate resolution for the 2 micron electronics we plan to use, and the high resolution Ultratech aligner was not designed to use infrared.

A run, using standard, low resistivity wafers, was started to test solutions to these problems. Since it was not practical to modify every machine to be used at CIS to prevent backside scratches, a special one micron thick coat of photoresist was spun, using a plastic holder, on the side that was to face

down, prior to the start of each operation. The wafers were then hard baked at 150° C for 40 minutes. Alignment was attempted by dead reckoning in from the edge along the major flat. It turned out that the major part of the alignment error was systematic, and could be corrected with a fixed offset. The remainder, about 50 microns, was sufficiently small with respect to the wafer thickness (300 microns), to allow satisfactory back to front alignment of large diodes (several square mm) on the back, by providing some safety margin in the layout. (CIS is now improving the resolution of its infrared aligner, so direct front to back alignment should be possible in future.) Another task, also completed, was learning how to protect the bottom side of the wafer from splash back during the spinning of photoresist on the top side.

The results of the run showed about 35 of the 40 diodes on typical wafers working satisfactorily, with breakdown voltages between 50 and 100 volts, and typical leakage currents before breakdown of a few nanoamps. Figure 4 shows an I (back) vs. V plot for a typical diode. Since the diodes were made of low resistivity silicon, we did not deplete through to the other side of the wafer. The yield was adequate, but also consistent with our negative results with the earlier wafer-sized diodes. Some scratching was still noticed, even with the one micron resist, so we are using a thicker layer on the next run.

ITEM 6, Radiation Hardness: Hardness studies are not a high priority until devices have been fabricated. Lalita Manchanda of Bell Labs, the inventor of a bulk CMOS process using self-aligned field shields [8], visited us in April. Her process, which should be compatible with ours, produces circuits that work in the GHz frequency range after radiation doses in excess of 50 megarads. She has offered to help us use it if we wish. A license would presumably be needed, so we may end up using the Sandia process, which should also be available. The growth of noise with radiation has not yet been

measured for these processes. However, the signal on the small-capacity pixel electrodes is relatively large, and so should be less sensitive to noise than signals on strip detectors. Measurements will also need to be made of radiation induced doping changes and of charge trapping in the depleted substrate of the detector volume.

ITEM 7, Fabrication Facility: Device fabrication will be at the Center for Integrated Systems at Stanford University.

ITEM 8, Collaboration with other Groups: This is not yet firmly settled. We are on the Silicon Tracking and Pixel subsystems proposals for the SSC, but have been excluded from their funding requests. We are also a member of the SDC collaboration. Members of a number of other collaborations have expressed interest in this pixel technology. Should it be successful, it would be relatively easy to modify the design for use in other detectors, and then, using the same run steps, to fabricate additional chips. The major work, which would have to be done by the other groups, of the actual construction, could provide valuable experience for the preparation of the SSC detector.

We are in frequent contact with the LBL members of the SSC pixel detector subsystem group. They currently use fabrication facilities on the Berkeley campus. Our ideas on design and fabrication are reasonably compatible and complement each others in some cases. However, it is best to continue to use both Berkeley and the Stanford fabrication facilities, and not put all our "eggs in the same basket" (or on the same earthquake fault). We have known of semiconductor labs that have been shut down for many months by accidents, by failure of a single key piece of equipment, or even by such simple things as contamination in a high purity water system. In addition, having access to two labs, both staffed with experienced engineers in a field in which much

practical knowledge has not yet made it into textbooks, provides a better opportunity of finding useful ideas and solutions to unexpected problems.

ITEM 9, Device Fabrication: Fabrication was started last year for diodes and diode test structures. Starting on the more complex pixel fabrication task, it seemed best to progress in several overlapping steps. For additional safety, each wafer is planned to include simple devices, more complex ones, and test structures to monitor each major element in the circuit.

The first run, now complete, has all elements except the deep depletion diodes, which are replaced with test inputs. It is part of a regular, shared-wafer, CIS BiCMOS run on normal, low resistivity silicon. In addition to the 5 by 14 pixel arrays with and without low noise amplifiers, it has separate amplifiers, separate shift register readout control, standard test structures, and a special test structure designed to predict the yield for large circuits. Figure 5 shows a photomicrograph of one of the simple 5 by 14 arrays. Testing of these devices has just started. Figure 6 shows a pulse from the shift register.

The next run, now between the 12th and 13th mask step, uses high resistivity silicon. These wafers will have the arrays and test structures of BiCMOS pixel arrays, but now with diodes, a larger (10 by 30) version of the pixel detector with amplifiers, and a 3 by 20 array without shift register readout, but with discriminators to tag the time a column was hit. Calculations using the process simulation program, SUPREM, which had earlier been used to verify the practicability of the fabrication, were extended and specialized for the planned structures. Run sheets, detailing the steps, take 79 pages. We expect this run will be completed by fall. While some wafers are being held back at certain critical steps, as insurance against a need to start the process over in case of problems, we also plan to have a follow up run, staffed mainly by technicians, coming along behind this one.

ITEMS 10 and 11, Testing: While fabrication is underway, an infrared test setup is being prepared. Synthetic tracks of ionization will be made using the red/infrared light source that was used to test the 18,000 channels of silicon strip detectors for the Mark II vertex detector. A light emitting diode, placed just above the eyepiece of a microscope, produces a demagnified image only microns across, at the silicon substrate. The near infrared penetrates many tens of microns to make the track. To adapt the Mark II IR source for two-dimensional motion we must add a second stepper motor and drive/control circuit. X-ray sources will also be useful in these initial tests. Once we start making larger arrays, quite a bit can be done with a Sr-90 "beam" similar to that used to test the first silicon strip detector with Microplex readout (see G. Anzivino et al, [3]). Radiation hardness and high energy beam tests must await the completion of chip fabrication.

3. Additional Design Work

Additional design work and calculations have been done or are underway. Using a modification of the field calculation program described in [4], we are calculating the expected time structure of the pulses for tracks with various impact points and inclinations, and with Landau fluctuations.

A modified device that can measure light photons in the presence of high energy ionizing particles has been designed. It has p+ and n+ collection electrodes on the front side. Visible photons, which are absorbed in the first few microns, send their electrons and holes only to those front side electrodes. Ionizing particles, penetrating the entire detector, send a few electrons to the front n+ electrode (and all their holes to the p+ electrode) but send most electrons to the back side diode. To make a useful subtraction of this backside signal for photon isolation, rather than just vetoing the event,

the capacity of the backside would generally need to be reduced by subdividing it.

Future Plans: While the current fabrication run is being completed, we will be designing, laying out, and using SPICE to simulate the sparse field readout for devices on the next fabrication run. The first one will provide a parallel readout of all rows, with a priority encoder that allows only rows with struck pixels to be read out. The priority encoder and other control electronics will be in N and P wells along the border. A chip with hit discriminators on columns reading into a column priority encoder would follow, and then one that includes the time-tagging scheme suggested by D. Nygren and H. Spieler [5].

Modification of the process steps to produce radiation hard devices could start almost immediately, and should start as soon as successful devices have been fabricated. Our pace is now largely limited by the availability of personnel.

Beam tests should be run once tested devices become available.

5. Scheduling Considerations

The natural schedule for an inner pixel detector differs from that of the large detector components, which will require a number of years to fabricate. All of the detectors needed would occupy the area of about 75 wafers — 3 batches for the low volume lab equipment at CIS. Hand assembly, which was painfully slow for the Mark II vertex detector, should be replaced by automatic assembly using standard industry equipment. For example, a chip can be selected, placed to better than 25 micron accuracy, and bonded to its support in less than 15 seconds. Modern automatic wire bonding machines with pattern recognition make from 1 to 10 bonds per second. None of over 20,000 wire

bonds in the Mark II detector has failed. (But one of the relatively small number of traces in a handmade cable attachment did fail, disabling one of the 36 modules.) Designing for manufacturability will be an important part of the effort. If this mechanical engineering progresses in parallel with final chip design, then fabrication, test, and assembly should take less than two years.

The first modules with chips, cooling, voltage supply, and fiber optic links should be made as rapidly as possible. However, if the final design is not frozen at this time, and fabrication is started, allowing for contingencies, at an optimum time, significantly improved electronics will result.

For the last 20 years, the minimum integrated circuit feature size has been cut in half every 5 years; maximum chip area has doubled every 6. The maximum number of transistors per chip has doubled every 2 years and energy dissipated per logic operation has been halved every 1.25 years [9]. No letup is expected in these trends for most of the 90's [10]. Such an optimum start will also permit additional development and more thorough testing, resulting in a far better vertex detector that should still be ready at turn-on.

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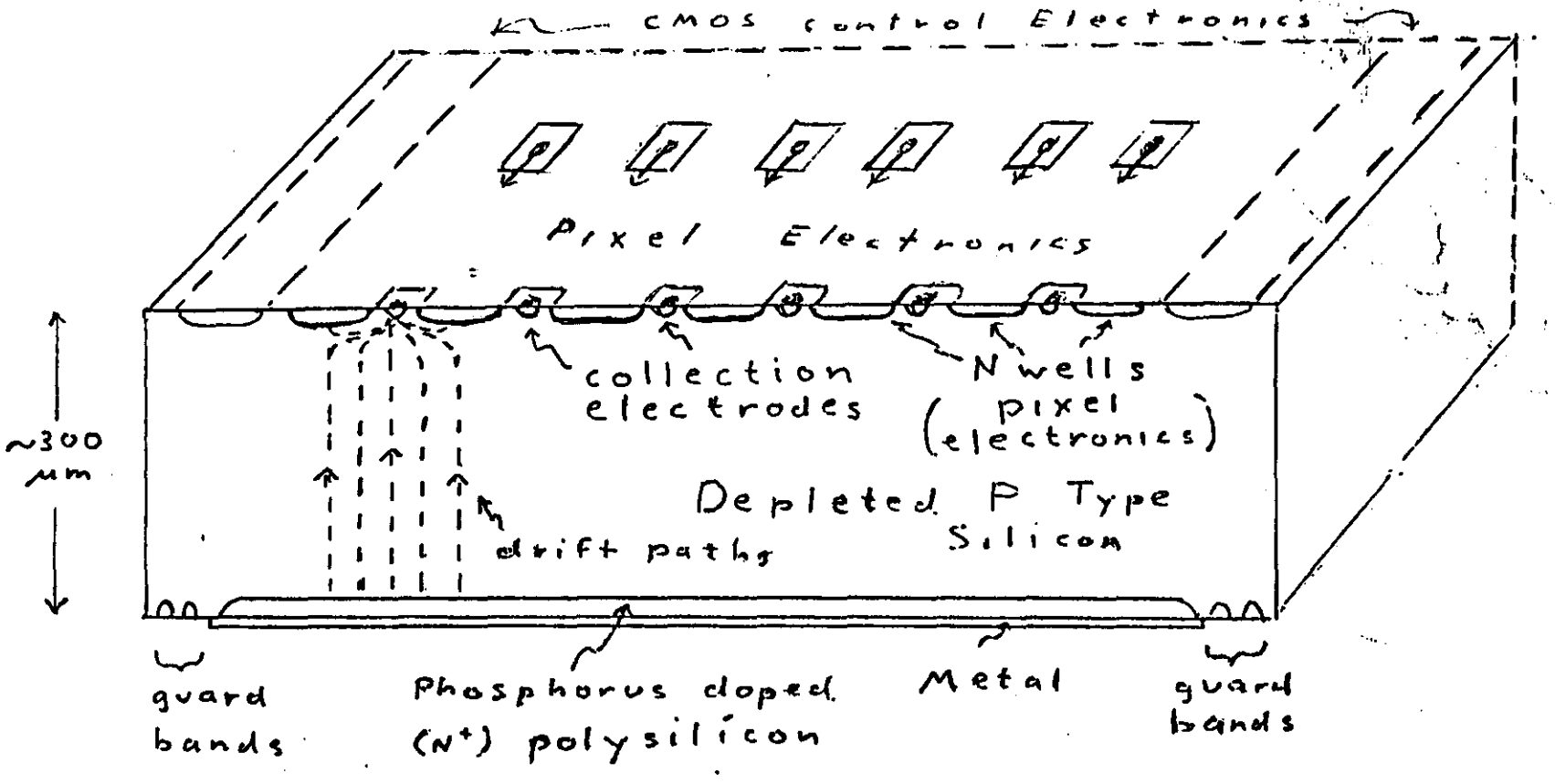

(Not to scale)

Figure 1

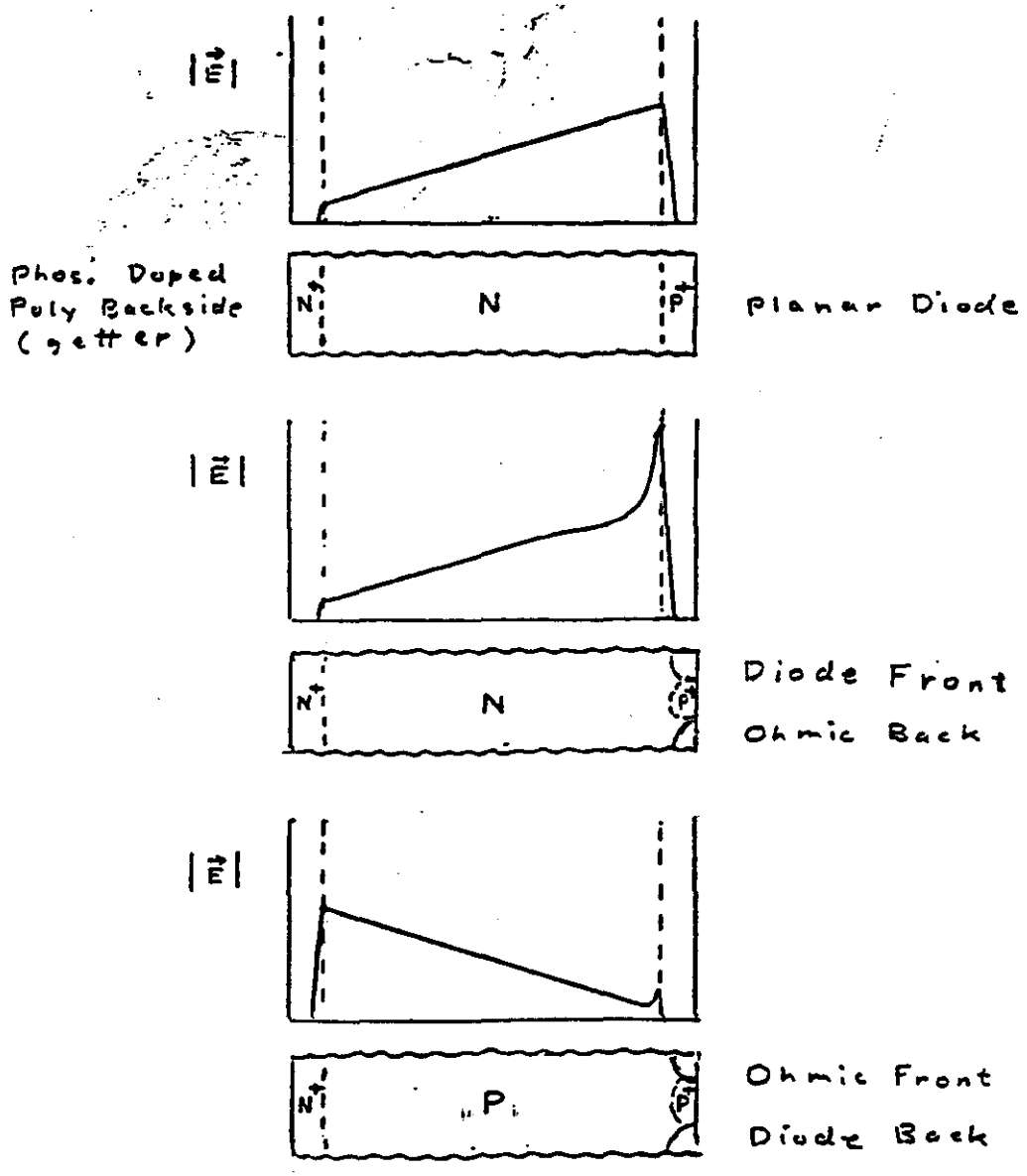

Fig. 2. Reducing peak fields with a back side diode. Typical fields are shown as function of depth, over the corresponding cross-sections, for (top) a planar diode, (middle) a pixel with an ohmic back and front diode collection electrode, and (bottom) a pixel with a diode back and a front ohmic collection electrode. For detectors with collection of electrodes that are only a few percent of the pitch, the near electrode fields are an order of magnitude larger than shown.

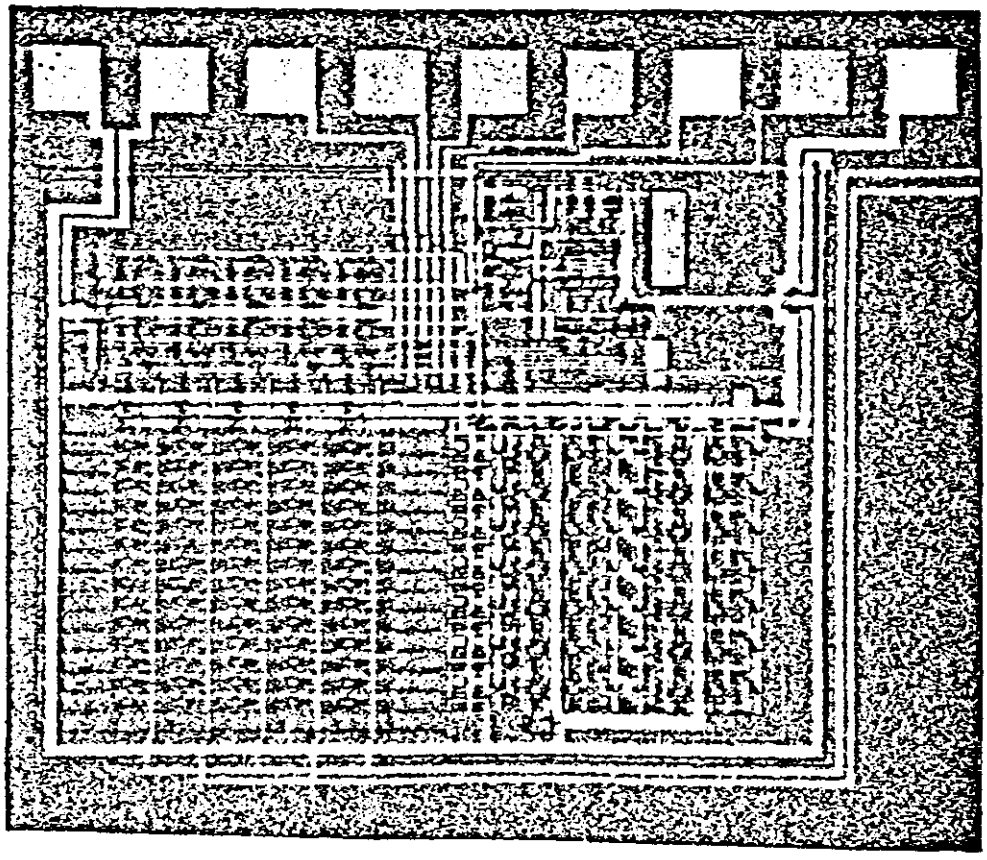

Fig. 5. Photomicrograph of a 5 by 14 pixel test chip.

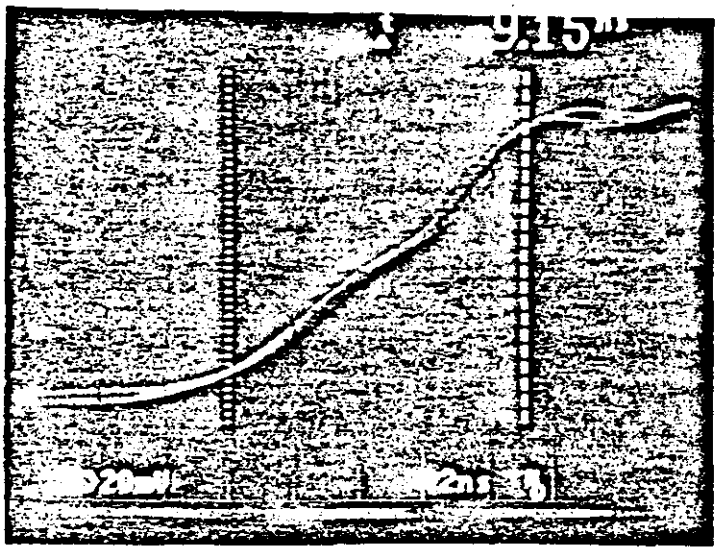

Fig. 6. Fourth stage output from x shift register.