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DESIGN OF ELECTRONIC READOUT BOARD FOR STRAW TUBE ARRAYS

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ABSTRACT

The electronics readout board for straw tube arrays is in the early design stage. At this time the emphasis is on developing techniques to produce a high density electronics board with reliable circuit connections. The choices of materials, techniques, and technologies are discussed.

Introduction

Wire drift arrays are suitable tracking detectors for SSC provided the drift distances and times are made small enough. The resulting large channel count puts a premium on the use of extensive on-board signal processing. The close packing of cells implies high densities of chips on the readout assemblies. We consider a model layout and techniques for its implementation.

The circuit designs have been described elsewhere[1]. Each drift wire is capacitively coupled to a preamp/-shaper/discriminator, whose differential output drives a time-to-voltage converter (TVC). Data collection chips (DCC) handle the digital data flow from some number of TVC's to the higher-level data stream. Information for triggering the experiment must flow both to and from the on-board circuits, which also have to supply high voltage to the wires.

A straw tube array such as that described by the Solenoidal Detector Collaboration[2] (SDC) comprises superlayers of 6-10 close-packed straw layers conforming to cylindrical surfaces, perhaps assembled from modules of a few cm width. For the present study we assume modules of trapezoidal cross section containing 228 straws, each 4 mm in diameter, in eight layers. Removable readout boards are placed perpendicular to the straw ends, respecting the 10-15 cm radial spacing between superlayers. In this paper we present the choices available to produce a board with such high density electronics.

Model Board Design

The model layout we have developed is shown in Fig. 1. The amplifiers, shapers, and discriminators for four wires are packaged into a single chip of dimensions 2 mm × 3 mm. Connections to each chip include four each of single-end wire input and differential pair output, one signal ground, and 2-3 DC voltage supply levels. The TVC is a single four channel chip 8 mm × 8 mm which has a pair of differential inputs per channel. Forty parallel buss lines handle data addressing and control, as well as power and ground. These connections terminate at the DCC which communicates between higher level DCC's.

Design Considerations

The main problem is making reliable connections from the IC die to the PC board and having enough room left over for test points and via connections to other layers. The technology available for making high density connections is not completely reliable. The physical properties of bonds are not easy to determine by visual inspection. Each board may have up to 5000 connections.

There are four different technologies that could be used:

- tape automated bonding (TAB)
- chip on board wire bonding (COB)
- flip chip
- thick film hybrid

FR4 Multilayer Circuit Board

A FR4 PC board is widely used, and it is fairly easy to find vendors capable of producing multilayers with traces of 4mil × 4mil. With multilayer boards vias are used to connect layers. There are three types of vias; conventional, blind and buried as illustrated in Fig. 2. To insure vias make connections to the other layers, pads have a relatively large size of .025", to provide for error in registration. Blind and buried vias can reduce the space taken up by the pads and allow more room for traces. However, these vias can trap contaminants thus affecting reliability. The cost of multilayer boards increases significantly with the more layers there are and the number of buried

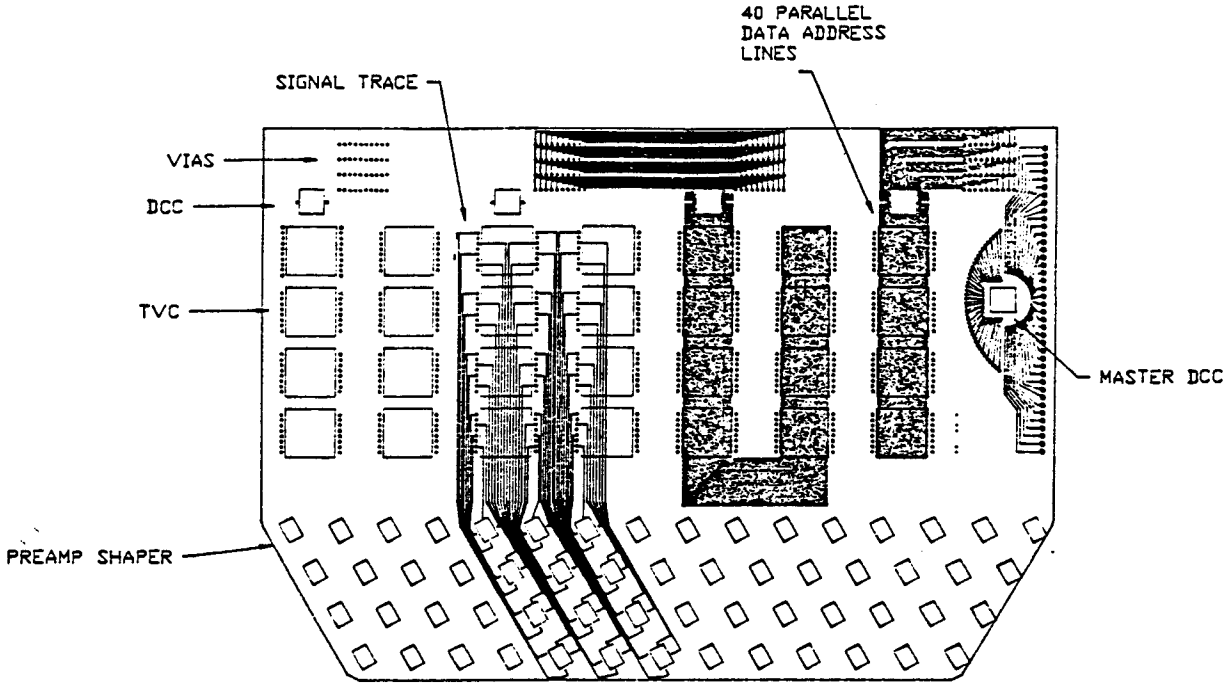

Fig. 1

and blind vias. Trace thickness also increases price when reducing trace and space sizes, due to lower yields.

A vacuum process is used to laminate the layers together. The board for this design will probably be about .062" thick. Fig 1 shows a layout suitable for this technique.

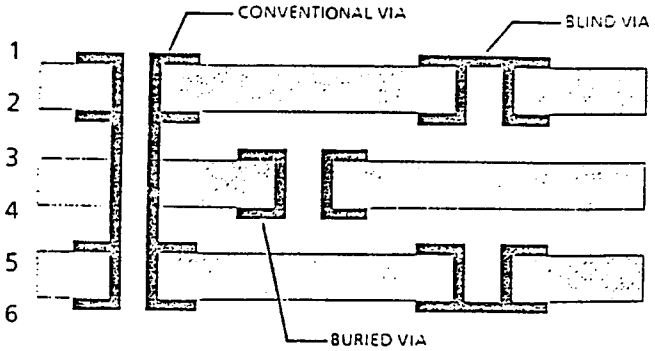

Fig. 2

FR4 Substrate TAB

Tape automated bonding uses an etched metal frame with inner leads that match the pattern of the die and outer leads that match the trace pattern and spacing on the PC board. The inner leads can be reliably connected in a variety of ways. The outer leads can be reflow soldered similarly to surface mount techniques. Problems arise with solder bridges between closely spaced traces. A solder mask cannot be used because of the closely spaced traces. However with a metal etched stencil, solder paste can be accurately printed through to the trace. Then the TAB is placed on the board and held in place by the tackiness of the solder paste. When all components are in place, the board can be heated to make the solder connection. If the solder paste is strictly controlled during application through the stencil, solder bridges can be kept to a minimum.

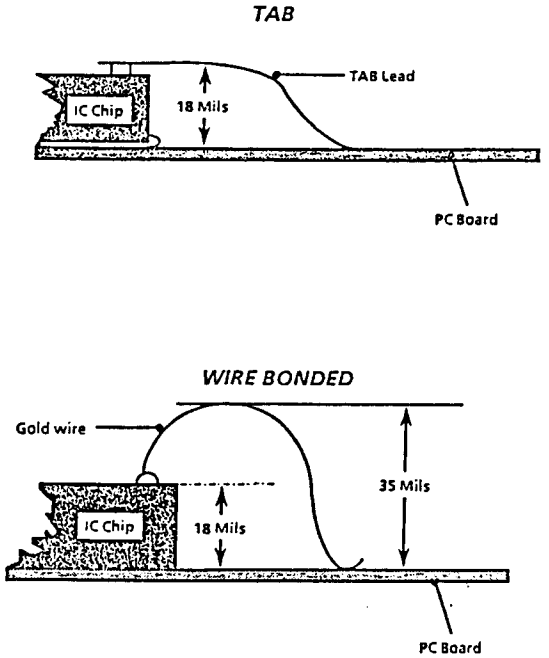

Fig. 3

Comparison of the COB and tape automated bonding (TAB) technologies

FR4 Chip on Board

With COB technology, the tab is done away with and the chip is mounted on the substrate. 25 micron gold wire is used to make the connections from the die to the trace, as illustrated in Fig. 3.

With FR4, heat is a problem. The stress generated by the differences of coefficent of thermal expansion (CTE) could cause the die to come off. Also, the temperature applied to the FR4 during bonding could cause it to melt, producing an unreliable connection. In order to bond to the trace, soft gold must be plated on the trace where bonds will be made. The purer the gold the lower the temperature of the bonding tool.

Flip Chip

Flip chip process eliminates the need for bond wires or tab mounting. The chip is turned over and mounted directly on the substrate. Solder on the die pads and substrate make the connections using surface mount soldering techniques. CTE is very important. To prevent solder joint cracking a substrate should have similar CTE to the die.

If a die is going to be used in a flip chip process, it needs to have solder bumps deposited on the pads. This is done in a vacuum deposition process while it is still in wafer form. The PC board also needs solder bumps. The solder bump size and diameter need to be tightly controlled. Before the chips are placed on the board a rosin flux is applied to the substrate to provide tackiness and to prevent chip movement until reflow soldering is done.

Ceramic Substrate Thick Film Hybrids

With polymer thick film technology it is possible to lay down layers of conductive traces, using screen printing techniques. Multilayers are easily formed by printing alternate layers of conductor and insulator. After each layer is screened, it is fired to cure the polymer. A board can have up to 20 layers per side. Interconnections between layers are made by printing through windows in the insulator layer. Printing line widths of 5mil with 5mil spaces are possible, however registration accuracy becomes a problem with smaller trace spacing. Any trace that might need to be soldered to can be screened with a solderable ink. Traces that need to be bonded to can be gold plated by using a platable ink base.

A ceramic substrate is the best choice for reliable wire bonding since the substrate is very stiff and can be heated. Thicknesses of ceramic are available as thin as .005", although the repeated firings of the polymer ink system tend to make ceramic brittle. A .025" thickness is commonly used.

High Voltage Input Board

Surface mount chip resistors could be used for current limiting, reducing board size. If a thick film process is used, the current limiting resistors would be screen printed on, further reducing the board mass.

The decoupling capacitors could stand on end (see Fig. 4) and be sandwiched between the HV input board and the readout board. Conductive epoxy could make the connection.

One possible way to make connections to the sense wire would be a conductive rubber tube from the HV board to the wire feedthrough.

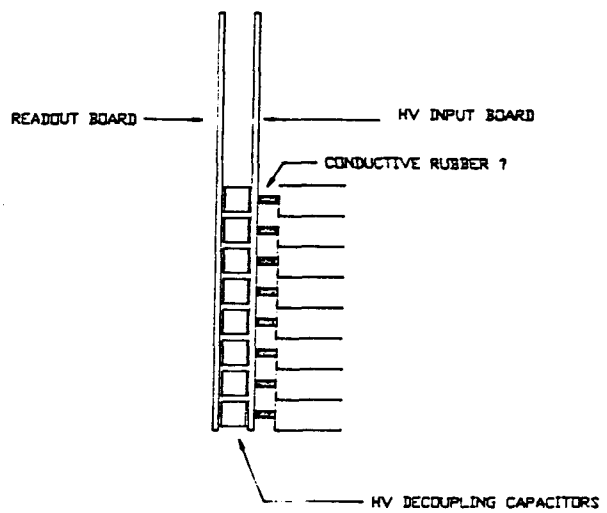

Fig. 4

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[1] M. Newcomer, paper at this conference.

[2] Solenoidal Detector Collaboration, Expression of Interest (1990).