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SDC
SOLENOIDAL DETECTOR NOTES

A CALCULATION OF THE TRIGGER PIPELINE LENGTH*

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This is an attempt to itemize the number of clock cycles required for a digitally pipelined 1st-level trigger for the SDC. It comes out to about 110.

ASSUMPTIONS

- The trigger accept bit comes back as a synchronous logic level which is valid a fixed number of crossings following the crossing which produced the trigger.

- The calorimeter trigger is segmented into:
  - 128 Phi slices (electrically)
  - 32 Phi slices (mechanically)
    (i.e. each "wedge" contains 4 phi-slices)
  - 128 Eta slices (electrically)
  - 4 Eta slices (mechanically)
    (i.e. two barrel sections and two plug sections each containing 32 towers in Eta.)

- The signals are digitized on the PMT base. Digital trigger sums, etc. are formed by a single crate of trigger/DAQ electronics per wedge. Each wedge produces a pipelined output (~100 bits) which is cabled to a central trigger location located outside the muon steel. Global trigger sums are produced there, and a final trigger decision bit is pipelined back to each front-end channel.

- Trigger Sums are calculated:
  - using digitized information from exactly one crossing
  - in a straight fall-through digital pipeline
  - using pipelined floating-point adders with 2-cycle latency

- The tracking information is available
  - in the lowest-level pipeline
  - in the vicinity of the tracking readout crack
  - less than ~40 clock cycles after the crossing
  - as Pt threshold bits in each of the 128 phi-slices
  - separately for each end of the tracking system

  (Whether or not the tracking information gets used in the 1st level trigger or not is not a big factor in the pipeline length).

- Global energy sums (Et, Missing Et) are performed in a pipelined binary tree.

- The accounting below is for a very complete electron trigger, which is likely to be the critical path. It performs:
  - 2x2 overlapping sums for EM signal region
  - a cut on the ratio of Hadron:EM energy in the signal region
  - an optional "isolation" cut on the ratio of EM energy to the energy in a 4x4 "guard ring" around the signal region.
  - a pipelined track match with a granularity of a single tower (3 degrees in Phi).
  - the Et's of both the 1st & 2nd largest electrons in the detector are preserved in the pipeline.

CALCULATION OF THE PIPELINE LENGTH

PHYSICS PROPAGATION DELAYS/PRE-SAMPLES

(These are "off budget" for calculating the pipeline length, but may be relevant for synchronization between systems. They are included in this accounting to allow for up to 6 "Pre-Samples" to study pile-up, etc.)

#clocks	Pipeline function	Comments
1	Time-of-Flight to EM calorimeter	Depends on Eta
1	Fiber Propagation Delay	cancels hadron time-of-flight
4	PMT propagation delay	depends on # stages in PMT, HV

6 Total 6 cumulative

PHOTOTUBE DIGITIZATION

#clocks	Pipeline function	Comments
1	Signal Integration Time on ASIC	Assume FNAL digitizer
1	Range encoding, drive signal off-chip	ditto
2	FADC	some FADCs are only 1 clock

4 Total 10 cumulative

LOCAL TRIGGER SUMS & ELECTRON/PHOTON ID

#clocks	Pipeline function	Comments
2	Worst-case cable delay to logic box	For signals which cross mechanical boundaries & require fanout.
2	Input synchronization	Elastic store or equivalent to compensate for cable delays, etc. Gets all pipelines operating on same clock phase.
1	Calibration/Et weighting	Single-cycle RAM lookup.
1	Drive off-chip to 2x2 summing logic	PC trace delay.
4	Floating point adds for 2x2 sums	Overlapping EM & Had sums for local electron signature.
2	Floating point add for (EM+HAD)	Total energy sum for Sum_Et and electron isolation.
1	Drive 2x2 sums off-chip to neighbors	Can cross wedge boundaries.
4	Floating point adds of 2x2 sums to produce 4x4 sums	Calculate 4x4 sums for electron isolation region. EM/had cut takes place in parallel with 4x4 sums.
4	Floating point compare of 2x2 EM sum with 4x4 total energy sum	Determine if local electron isolation criteria is satisfied.

21 Total 31 cumulative

ON-WEDGE SUMMATION OVER ETA, CALCULATION OF BIGGEST ELECTRON IN WEDGE, ETC.

#clocks	Pipeline function	Comments
2	Signal delay to wedge summation logic	Centrally located on wedge.
10	5-stage Binary tree to find largest and 2nd largest electron candidate in the phi-slice (32 towers in Eta).	May be only 5 clock cycles if we can do each stage in 1 cycle. The floating-point adder for Sum_Et will also take 10 cycles.

12 Total 43 cumulative

PHI-COINCIDENCE WITH TRACKING TO FORM "TRACKED" ELECTRON CANDIDATES

(performed locally near the readout crack for the tracking)

#clocks	Pipeline function	Comments
1	Data transmission to track-coincidence logic	
1	Phi-coincidence with tracking to form tracked electron candidates.	Combined Pt, Et threshold
4	Two-stage Binary tree to determine biggest, 2nd biggest electron in wedge.	

6 Total 49 cumulative

TRANSMISSION OF WEDGE DATA TO TRIGGER LOCATION

(At this point the wedge data consists of ~100 bits [4 "Ansley cables"] for each wedge. Total cables = (4 Ansleys/wedge) * (32 wedges) * (4 bays) = 512 "Ansley cables").

#clocks	Pipeline function	Comments
12	Cable delay from farthest wedge to trigger logic (~120', ~200 ns)	Ansley cables are OK for fast timing at lengths up to 300 ns.

****** NOTE: some devices (e.g. forward calorimetry) may have longer cable
****** runs. They will however have fewer elements to sum and probably simpler
****** trigger logic, hence a smaller total pipeline delay.

2	Input synchronization	Elastic store or equivalent to equalize delays and to catch the pulses which are "hung up" in the data transmission cables.

14 Total 63 cumulative

GLOBAL TRIGGER SUMMATIONS

#clocks	Pipeline function	Comments
4	2-stage Binary tree to calculate biggest, 2nd biggest electron in an entire phi-slice.	Inputs are from 4 "wedges" in Eta.
10	5-stage Binary tree to calculate biggest, 2nd biggest electron in entire detector.	Inputs are from 32 "wedges" in Phi. Similar calculations are taking place in parallel for Sum_Et, missing Et, etc...
1	Transmission to Trigger Decision Logic	
15 Total	78 cumulative	

FINAL TRIGGER DECISION LOGIC

(At this point all information from the crossing has been distilled to a single very wide binary word which contains Sum Et, Missing Et, biggest, 2nd biggest electron, muon, etc. This word is examined in parallel by a number of circuits to determine if the crossing satisfies a given trigger, e.g. "1 electron above 10 Gev and one muon above 15 Gev and Sum_Et above 100 gev").

#clocks	Pipeline function	Comments
1	Fanout to trigger decision modules	crate backplane
3	Internal calculations of trigger trigger decision modules	could be faster
1	Rate-limiting & prescaling of individual triggers	maybe in parallel
1	Collection of "or" of all "accepts"	crate backplane?
10	WESLEY SMITH FACTOR	Wesley assures us that he will use up these clock cycles in some way that he doesn't know about yet.
16 Total	94 cumulative	

FANOUT OF "TRIGGER ACCEPT" BIT BACK TO FRONT END IC's

#clocks	Pipeline function	Comments
12	Cable delay from trigger logic to farthest wedge (~120', ~200 ns)	Decent cables are OK for fast timing at lengths up to 300 ns.
2	Input synchronization	Elastic store or equivalent to equalize delays and to catch the pulses which are "hung up" in the data transmission cables.
4	"Trigger Accept" fanout within each wedge	Two-stage synchronous fanout with last stage servicing ~1m**2 of calorimetry surface.
18 Total	112 cumulative	

CONCLUSIONS

This is comfortably below 128 but not temptingly close to 64. There is a lot of fat. For example the 2-stage floating-point adder which is possible in 2u CMOS may be possible in a single pipeline stage in submicron, and this would save a bunch of cycles. There are also things that I have forgotten or ignored. For example, it is unclear whether the fixup necessary to prevent the same electron from being found multiple times in multiple overlapping sums will cost extra clock cycles or not.

If the longer pipelines makes the muon systems significantly cheaper, we should do it.

Answers to Andy's Questions:

At FNAL we have been designing for a 128-cycle pipeline. For the calorimetry, the cost of a single pipeline stage is a 12-bit digital RAM cell for each of ~20k PM tubes, or about 250k bits of RAM for the entire calorimeter. The incremental total cost for an additional microsecond of storage (64 stages; 16Mbits) is << $50k. Similarly, the power dissipation of adding additional pipeline stages is negligible since they are non-clocked static CMOS RAM cells.

For the fiber tracking/trigger, only a single digital bit is stored per channel per pipeline stage. I think that the fiber tracking has now been weaseled down to 250k-500k channels. The cost of extending the pipeline is then ~500k RAM cells per clock cycle, or again <$50k per microsecond of storage. Again, very little additional power is consumed.