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A Sixty four channel Low Power Bipolar Amplifier-Comparator for use with Silicon Strip Detectors in high Radiation Environments

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ABSTRACT

A bipolar integrated circuit containing 64 amplifier-comparators has been fabricated for use with the Zeus silicon strip detector system. The individual circuits' performance matches the simulations very closely. No unexpected system problems have surfaced and the yield has exceeded expectations for such a large bipolar chip.

Introduction

Silicon detectors and the associated electronics used at hadron colliders have to survive large radiation doses. The radiation damage to the detectors themselves results in large (~microamps) leakage currents. In order to counter the shot noise from these large leakage currents, a short shaping time is favored, although another scheme has been proposed which uses a longer shaping time and recovers the time information using a digital filtering process [1]. For the large capacitance and the predicted leakage currents from the long detector strips which we use, it can be shown that bipolar amplifiers are inherently quieter than their CMOS counterparts for fixed power comsumption. In addition fast bipolar circuitry is invariably radiation hard, whereas CMOS needs special processing to survive the anticipated radiation doses. This radiation hard CMOS is comparable in cost and availability to custom bipolar.

We embarked on a program aimed at producing low power bipolar amplifier-comparators for use with long strip silicon detectors in high radiation areas. We chose to use a digital system. For a given beam crossing we detect a one or zero from the comparators. This information is stored in a second IC which buffers the data in two levels appropriate for use with an hierarchical trigger system. The second IC is a radiation hardened CMOS chip which is described elsewhere [2].

The circuit described here is the first of a series which will go down in power and shorten the shaping time We aim to reduce the power to less than 1 mw and lower the shaping time to 20ns to handle the shorter time between bunches envisaged at future hadron colliders [3]. One factor which made the design of this first IC somewhat more complex was the fact that DC coupled detectors are being used. Given the large anticipated leakage currents steps had to be taken to ensure that the amplifier remains correctly biased.

Design Considerations

The circuit was designed to have a 30 nsec shaping time, give a signal to noise of at least 20/1 with an 11 pf input capacitance and a real signal. The last consideration does not translate into an ENC of 25000/20 because with this shaping time we can only collect about 85% of the charge resulting from the passage of a charged particle through the detector. The most difficult design goal was to get acceptable matching of the gains and thresholds without trimming each channel. Obviously we could not afford to have a separate threshold adjustment for each channel. We aimed to get matching of 2.5% so as to ensure that all the channels fired with essentially the same charge on a strip. This requirement was further complicated for the Zeus Detectors as they vary in length and, consequently input capacitance. We could have achieved excellent matching had we chosen to use laser trimming of the die. We rejected this option because this would not be feasible for the version we were planning to use on the SDC detector on account of the large number of channels which this system was planning to utilize. The amplifiers were also designed to withstand 10 megarads of radiation from protons.

We chose to use Tektronix SHIP as this has very small geometry features which make it feasible to lay out amplifiers on a pitch suitable for use with microstrip detectors of 50 micron pitch. The Tektronix process also has very high ft npn transistors, 9Ghz, which function adequately when run at the reduced currents we use. Typically the peak ft is attained with a 1ma current on the smallest geometry npns, but we often run these transistors with tens of microamps bias currents, which degrades the ft substantially. With

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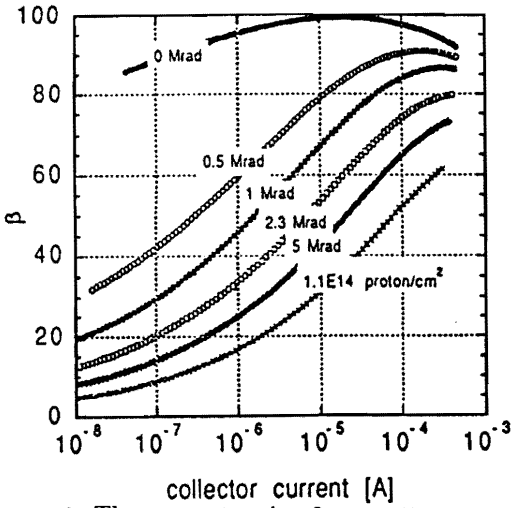

Figure 1. The current gain β vs. the collector current for the N2 npn transistor for different total ^{60}Co doses and a proton fluence of $1.1*10^{14}$ p cm^{-2}.

the exception of the lateral pnp transistors, the components available for use with this process are all adequately radiation resistant. At the time this circuit was designed we had not tested the radiation resistance of the JFETs and so we were left without a device suitable for making active loads as the pnp's were unusable as mentioned above. Typically the npn's betas were degraded by about a factor of 3 after irradiation at the current densities used (fig. 1). The problem was worst for the input transistor as a fairly large transistor was used there. Designing a circuit which was insensitive to these changes in beta proved relatively straightforward.

Circuit Description

The amplifier is shown in fig. 2. In order to meet the threshold matching requirement it was necessary to use 3 gain stages. After the AC coupling capacitor, C3, it was only possible to use a gain of 10 before the comparator or the mismatch resulting from the slight differences in Vbe for Q15 and Q16 would cause unacceptable threshold variations. The input section, Q1-Q8 has two stages under the feedback. This was necessary because it was not possible to get sufficient gain without an active load in a single stage. The feed- back impedance is essentially 200K in parallel with 150ff. It is shown as two parallel pairs of 100K and 100ff but when strays are taken into account it functions like a 200K in parallel with 150ff. The use of the large 200K resistor kept the current noise down. We could not tolerate a larger value because of potential bias problems which would result with high leakage currents and base currents which are expected after irradiation. The second amplifier consisting of Q200-Q202 gives a gain of 3 in the frequency range of interest while stripping away the DC shift which results from high leakage currents across the feedback resistor. It used less space on the die to do it this way rather than using an additional standard AC coupling.

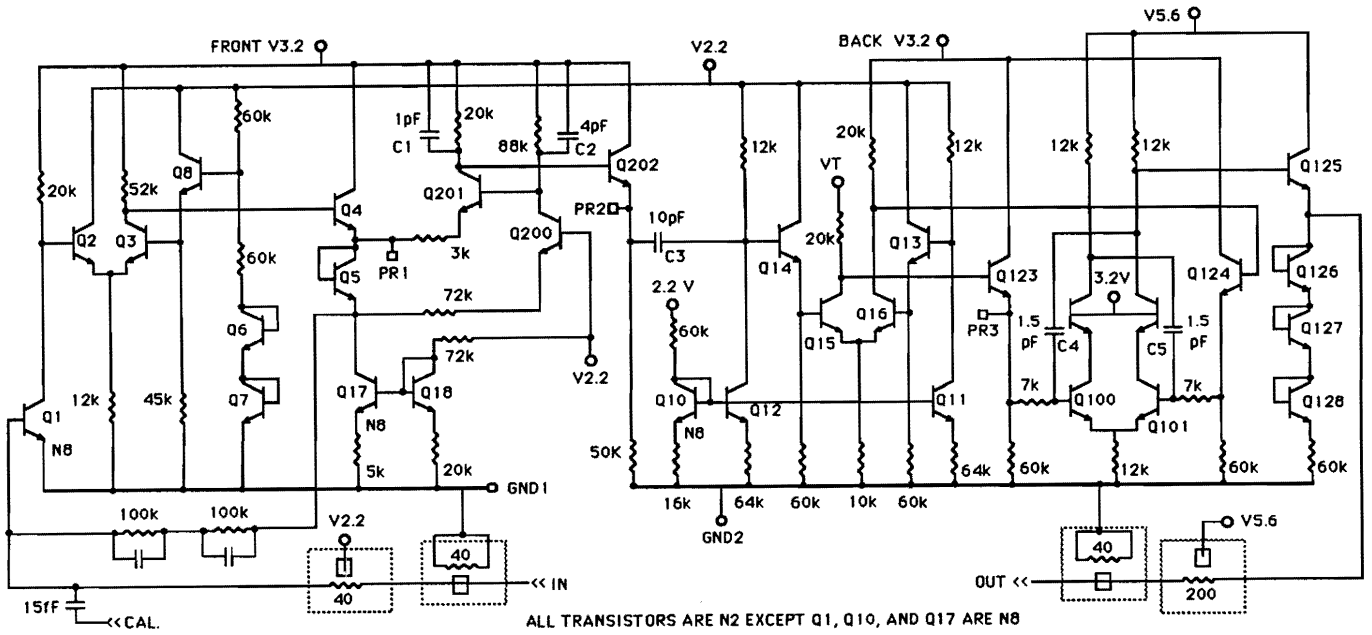

Figure 2 Single channel schematic of amplifier-comparator

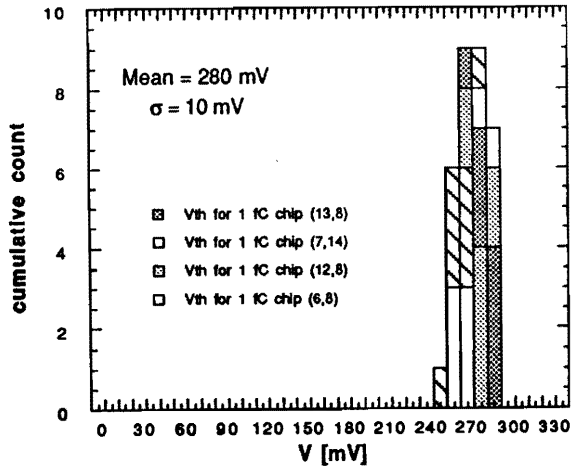

Figure 3. δV_t for 1 fC.

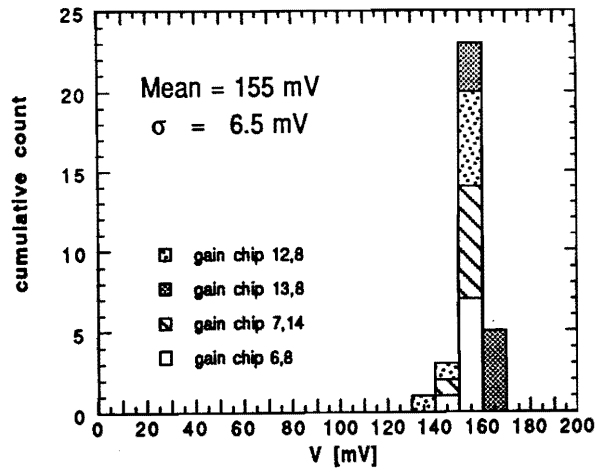

Figure 4 Gain for 1.

The comparator is a straightforward monostable which produces a 30nsec wide pulse. It utilizes a cascode to minimize walk in the circuit.

Input and output protection are provided in an unusual, but effective manner. The diode junctions formed between the p+ resistors and the epi tubs are used as the protection diodes. This gives diodes which have a substantial area with low capacitance. As described below this affords excellent protection.

Each channel was 72 micron wide. Channels are separated by a grounded line to prevent cross talk. Each channel has a test input, with channels grouped in 4 sets of 16 for calibration tests. The power and ground lines are very wide covering the entire chip to help isolate the amplifiers from pickup and to provide low enough ohmic drops across a die to permit the power to several die to be connected in series.

Results

The chip is easy to use, displaying no tendency to oscillate. AC and DC testing can be done with a wafer probe. Test points are available to view the pulses after each stage of amplification and these pulses were compared to those predicted by the simulations. There is a slight loss of gain which is not fully understood and the shaping time is slightly longer than we predicted. Time walk is due entirely to the rise time of the amplifiers. With a threshold setting corresponding to 25% of a minimum ionizing pulse, the comparator has less than a nsec of walk for a range of pulse heights from 2% of a minimum ionizing pulse above the threshold up to pulses of 400% of minimum ionizing.

The ENC was carefully measured as a function of input capacitance, C, and was found to be (580 + 38*C)electrons, where C is the value of the input capacitance in pf. The simulations predicted 600 + 40*C so the agreement is excellent.

The input protection was found to work extremely well. The amplifiers suffer no damage when a 10 nf capacitor is charged to 160 volts and then shorted while connected to the input. With 13pf of capacitance discharged from 160V the input traces are vaporized but the protection diodes are still functional. The rugged nature of these chips probably makes them suitable for use with gas microstrip detectors.

Crosstalk between channels has been measured to be less than 2% by bonding the chip to a detector and illuminating the detector with a sharply collimated laser source. Moving the source across the strip adjacent to the one under observation enable us to set limit of the cross talk. The cross talk observed could all be attributed to capacitive coupling between the detector strips and a limit of 2% was set for cross talk on the die.

Matching of the channels and gains on a single chip met our goals and plots for the variations for different chips from the same wafer are shown in figs. 3 and 4. These match well enough so that the same threshold can be used for chips from the same wafer. This is helpful since several chips are typically mounted on a single hybrid assembly which can have a single threshold.

The yields have been excellent and over 60% of the die are perfect. This is based on the observation of 11 wafers from two separate production runs.

Chips were subjected to a 5megarad radiation dose

from 600Mev to 800Mev protons and no degradation in their performance was observed.

Conclusions

The amplifier comparator made for use in high radiation environments met all its performance goals and is currently in use in the Zeus Silicon Detector. Yields are excellent and more aggressive designs using less than 1mw per channel suitable for use with 50 micron pitch detectors are currently being integrated.

Acknowledgements

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References

[1] J. deWitt, *Nucl. Instrum. & Methods* **A288**, 209 (1990).

[2] S. Gadomski *et al.*, CERN-PPE/92-24 (1991).

[3] A newer version using $\sim 800\mu w$ with a 20ns shaping time is currently being integrated.

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