Development of high speed low noise transimpedance preamplifier in bipolar technology for silicon photodetectors of the CMS electromagnetic calorimeter.

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ABSTRACT

A front-end transimpedance preamplifier is studied to be matched with photodetector in the CMS electromagnetic calorimeter. A fast low noise preamplifier has been designed with bipolar transistor devices for detector capacitances in the range of 10 to 100pF. A noise lower than 2500 e- rms has been achieved in beam tests with PIN photodiodes of 1cm² area and 50pF capacitance. Performances and results will be presented.

Chips have been made using rad-hard capability Harris Semiconductor UHF complementary bipolar process. Preliminary results of some prototypes will be given. These results may contribute to prove the feasibility of front-end electronics in bipolar transistor technology.
INTRODUCTION

The photosensors which are studying for the CMS-ECAL are silicon solid state devices: PIN photodiodes and more recently APD's which will probably used. From 1 or 10 nA in initial conditions, the silicon detector leakage current increases up to 10 μA or more due to radiation effect. The characteristics of associated front-end must not change with the variation of this parameter. The working conditions for processing time range typically from 10 to 30 ns. A fast shaping is the best solution to solve these problems and the bipolar junction transistor is a good technology for short shaping time and relatively large photodetector capacitances. Several publications proposed to use bipolar transistors in broadband and low noise preamplifiers [1-6]. Now, the design of a front-end with a good performance is easier by the use of high quality UHF devices. A transimpedance preamplifier configuration is proposed. Experimental results, transient response and noise have been measured. Some results obtained in tests beam are given for APD's associated to PbWO4 crystals.

NOISE EVALUATION

The equivalent noise charge has been calculated for the current sensitive configuration shown in figure 1.

\[ \text{ENC}_{\text{p}} = k \cdot (2kT \cdot (R_{bb'} + R_s + \frac{1}{2} \cdot \text{gm}) + \frac{q \cdot (l_f + l_{inv})}{R_{bb'}}) \times \tau \]
\[ \text{ENC}_{\text{f}} = 2k \cdot \frac{\Delta f}{(C_{in} + C_d)^2} \]
with: leakage current \( l_f = 50 \text{pA} \), transconductance \( \text{gm} = 20 \text{mA/V} \), input capacitance \( C_{in} = C_{gs} + C_{gd} = 20 \text{pF} \),
1/f noise: \( \Delta f = 10^{-14} \),
in the case of BJT.

\[ \text{ENC}_{\text{p}} = k \cdot (2kT \cdot R_T + \frac{q \cdot (I_{inv} + I_c)}{B}) \times \tau \]
\[ \text{ENC}_{\text{f}} = 2k \cdot \frac{\Delta f}{(C_{in} + C_d)^2} \]
with: collector current \( I_c = 0.4 \text{mA} \), base spreading resistance \( R_{bb'} = 10 \Omega \),
and with the following parameters values:
- Detector: capacitance \( C_d = 50 \text{pF} \), \( I_{inv} = 10 \text{mA} \) and \( 10 \mu A \),
- serial resistance \( R_s = 5 \Omega \).
- Input parallel resistance \( R_T = 33 \text{KΩ} \).
- \( k \) = shaping factor, \( \tau = RC \).

For a 20 ns RC-CR shaping time the noise charge is practically equivalent for bipolar and the field-effect transistor as we can see in figure 2.

![figure 2](image-url)

PREAMPLIFIER DESIGN

A preamplifier simplified schematic is shown in figure 3. The circuit is composed of:
- front-end with RF (gain) and CF (phase control),
- integration cell = 5 ns,
- buffer to drive 50 Ω line.

The test capacitance is integrated on the circuit.

![figure 3](image-url)
First this design has been evaluated in SMD (surface mounting devices) technology and then its implementation in specific integrated circuit is carried out using Harris Semiconductor UHF complementary bipolar process with transition frequency ($f_T$) values of 8GHz(npn) and 4GHz(pnp). This dielectrically isolated (10V) technology reduces the radiation effect on devices. The simulation has been done with Harris FASTRACK software, a complete ASIC development system. Its analysis capability allows the designer to predict the performance of circuit.

Figure 5a shows an example of simulated transient response (20ns/div) in comparison with a typical measured response (12.5ns/div), figure 5b. As we can see, experimental results and calculation agree very well.

Two complementary ASIC's have been processed. For the first test, the dies are mounted in dual in line package. It is very easy to use but the wire bonding length introduces a parasitic serial inductance. In these conditions, only the circuit with npn at the input is stable at nominal collector current.

In order to limit these parasitic serial inductance a direct die testing must be used.

The chip layout is shown in figure 6. Its area is equal to $1.3 \times 1.9\, \text{mm}^2$.

### NOISE PERFORMANCE

For noise measurements and calibration a classical analysis chain using gamma from a $\text{Cs}^{57}$ source is used (figure 7). The method employed consists in the measurement of the r.m.s. noise charge by integrating the signal noise in a fixed time gate. After front-end and post-amplifier (20db gain), the analog signal is split into two parts: one going to a constant fraction discriminator to generate the gate signal, the other one going to the integrator after suitable delay.

Another method to measure the r.m.s. noise voltage is to use a digitizing oscilloscope and a r.m.s. voltmeter. In peaking mode, the total noise depends on the shaping time. An additional integration of 100ns is used to determine, with a better precision, the base spreading resistance $R_{bb'}$.

### SMD prototype

A discrete semiconductor version has been tested. Two integrations are used to match the detector signal processing time: 5ns in the front-end and 10ns at the post-amplifier input.

The noise measurement in gated integrator mode is made for different gate values. The results are shown in figure 8 as a function of input capacitance.

\begin{align*}
\text{gate} = 250\, \text{ns: } (\text{ENC})^2 &= (16.0 \, \text{Cin})^2 + (2477)^2 \\
\text{gate} = 160\, \text{ns: } (\text{ENC})^2 &= (17.1 \, \text{Cin})^2 + (1922)^2 
\end{align*}

When the integration time increases, the curve shifts but the slope is constant. With a short gate (160ns) and an input capacitance above 50pF, the slope increases because the total charge is not completely integrated inside the gate (eq.2).
An external feedback capacitance $C_{fe}$ (0.47pF) is added in parallel to internal $C_{fi}$ feedback capacitance (0.2pF) figure 11. This additional integration, which stays below the realistic limits of the processing time for detector signal, allows a larger dynamic range.

The figure 9 presents the experimental results in peaking amplitude mode.

Measured transient pulse responses on 50Ω are shown in figure 12 (25ns/div) for three input capacitance values and with a total feedback capacitance $C_F = C_{fi} + C_{fe} = 0.67pF$.

Experimental noise measurements of the ASIC have been made with the same previous method. A fast shaping amplifier with 100ns integration constant is used after post-amplifier. Figure 13 presents the results in gated integration mode.
noise measurement (gated integrator)

\[ \text{ENC} = \sqrt{\text{ENC}^2_{\text{imp}} + \text{ENC}^2_{\text{noise}}} \]

- gate = 250ns: \( \text{ENC} = (31.1 \ C_{\text{in}})^2 + (3100)^2 \)
- gate = 150ns: \( \text{ENC} = (31.6 \ C_{\text{in}})^2 + (2108)^2 \)

For peaking detector mode results are plotted in figure 14.

noise measurement (peaking detector)

\[ \text{ENC} = \sqrt{\text{ENC}^2_{\text{imp}} + \text{ENC}^2_{\text{noise}}} \]

- \( \text{RC} = 20\text{ns}: \text{ENC} = (36.9 \ C_{\text{in}})^2 + (1409)^2 \)
- \( \text{RC} = 100\text{ns}: \text{ENC} = (29.4 \ C_{\text{in}})^2 + (1825)^2 \)

The value of \( R_{bb} \) obtained by these measurements is 90Ω for pnp UHFP3 transistor, \( we = 50\mu \text{m} \). To achieve the best noise performance, several bipolar transistors can be paralleled, keeping the total current constant[9].

**DYNAMIC RANGE**

The dynamic range is the ratio of the largest permissible signal output to the smallest detectable signal. For example, with a 2volts maximum signal on 50Ω and 200ns integration time, the total charge is \( 25.10^6\text{e}^- \). With three sigma equal to 5000e- and gain = 500, the dynamic range is 80db.

Figure 15 shows the output signals of the Harris DIL14 module for 4 charge injection values corresponding each to a 20db step attenuation.

**CERN BEAM TESTS**

The measurements of the electronic noise due to the use of APD's, Hamamatsu and EG&G, associated to our SMD and Harris ASIC prototypes have been done[10]. Figure 16(b) presents the typical response registered with an hexagonal PbWO4 crystal of 23.52cm length coupled to EG&G avalanche photodiode C30719E and excited by 4GeV electrons. A long tail is observed for this crystal, figure 16b, compared with a pulser response (figure 16a).
The electronic noise in MeV has been measured as a function of gain, respectively for two type of APD's at 27°C. 
- type 1: EG&G, C30719E, 25mm², Cd=35pF.
- type 2: Hamamatsu, S5345 (low C), 20mm², Cd=90pF.

Figure 17 shows the noise measurements for EG&G-APD connected to SMD and Harris ASIC prototypes.

**CONCLUSION**

The noise parameters of several transimpedance prototypes are measured.

For a 50pF input capacitance:
- noise = 2100e- rms, gate=160ns, SMD prototype,
- noise = 2500e- rms, gate=120ns, Harris ASIC prototype,
- peaking time = 15ns,
- low consumption = 15mW, (+10V) for the front-end,
- large dynamic range (2V output on 50Ω).

These measurements show the feasibility of front-end electronics in bipolar transistor technology. Encouraging results on the noise performance of the first run Harris monolithic preamplifier have been obtained. 1995 CMS ECAL electronic noise milestones requirements have been reached with APD's photoreadout (EG&G and Hamamatsu) and a typical PbWO₄ crystal.

The future improvements are:
- use a smaller package (chip carrier) or chip on board (COB) technology to limit the connections length.
- reduce the input transistor base spreading resistance down to values below 50Ω.
- integrate two channels (two gains) on single chip to match the ECAL dynamic range.

**ACKNOWLEDGEMENTS**

I would like to thank J.C. Legrand of CERN for the opportunity to be involved with RD32 and T. Melebeck, C. Poncelet, SdM (Belgium), for prototype assistance, CAD support and integrated circuit layout. I would like also to thank B. Ille (IPNLyon) and Y. Moussienko (I.N.R.,Moscow, Russia) for many profitable discussions and comments.

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