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DESIGN AND TESTING OF A DIGITAL REGULATOR FOR FERMILAB MAGNET POWER SYSTEMS

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To my grandfather Giovanni.

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Abstract

In this thesis, the design of a digitally controlled DC power system for testing conventional and superconducting magnets is proposed. The designed PID controller performances have been tested by the 30kA test stand for superconducting magnets, Vertical Magnet Test Facility (VMTF), which is hosted at the Fermilab Magnet Test Facility (MTF). The system is implemented on a National Instruments CompactRIO and both real-time and FPGA targets are programmed. A full 24-bit PID algorithm is coded and successfully tested by a manual tuning approach. An automated tuning algorithm is then introduced. As it will be shown by simulation and experimental results, the proposed system meets all design specifications. The current loop stability is up to 14 times better than the existing regulator and a control accuracy less than 4 ppm is achieved. Shorted-bus tests of the PID regulator have been successfully performed on the VMTF power system. In order to test the generalization capability of the designed system towards different types of magnets, the system has been easily adapted to and tested on the 10kA conventional magnet test stand (Stand C at Fermilab). As shown by experimental results, the designed PID controller features really high performances in terms of steady-state accuracy and effectiveness of the tuning algorithm.

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Introduction

Fermi National Accelerator Laboratory (Fermilab) in Batavia, Illinois USA, is an US Department of Energy (DOE) national laboratory. The Fermilab research activity is mainly focused on high-energy particle physics, pursuing the mission of a better comprehension of ultimate components of matter and the nature of the forces that rule in this domain. Within laboratories, high-energy beams of elementary particles are produced by particle accelerators and their associated detection equipment. Until 2011, Fermilab hosted the world's second largest particle accelerator – the Tevatron. The Tevatron was a synchrotron that for 30 years has accelerated protons and antiprotons in a 6.28 km (3.90 mi) ring to energies of up to 1 TeV, hence its name.

In a linear accelerator, such as the Tevatron, the LHC at CERN in Geneva, Switzerland, or the future International Linear Collider, the "heart" of experimentation is made up of superconducting magnets. A series of such magnets composes the main ring of the accelerator and focuses the beams. Hence the relationship between the magnetic field and the magnetic current should be accurately characterized and modeled. Before these superconducting magnets operate in the main beam line, it is necessary to test them for their usefulness. Power testing is usually performed. This method tests the maximum allowable current through the magnet, and the quality of its magnetic field. This test ensures optimum quality of all operating beam-line magnets. The Fermilab Magnet Test Facility (MTF) resides inside the Industrial Building 1 (IB1). Several high current and low current power systems are involved in the power testing of both superconducting and conventional magnets.

During my stay at Fermilab as "Guest Engineer", a digital PID regulator was designed. The implemented digital regulator was designed mainly for the CPS3 power system, which drives the Vertical Magnet Test Facility (VMTF). If compared with the existing analog regulator, the designed controller improves system performances in terms of rise-time, overshoot, stability and precision. The regulator was also tested on the "Stand C", that is a $10\,kA$ power system used to test conventional magnets, and on a KEPCO Bipolar Operational Power Supply/Amplifier (BOP) power supply, widely used at Fermilab for low-power and high slew-rate current tests.

The R&D for this digital regulator aims for accommodating the future International Linear Collider (ILC) magnet tests. The implemented digital regulator is also suitable for several power supplies for conventional and superconducting magnets tests, within

and beyond Fermilab. Some sister laboratories, such as DESY, are actually working on similar R&D projects for digital regulation of accelerator power supplies. So far no successful completion has been announced for similar projects all over the world.

Chapter 1 describes equipment and targets for magnet testing. The power systems architecture is introduced. Project assignments are listed and discussed.

Chapter 2 describes the design and development tools which has been used for the PID design and test. The architecture of the National Instruments CompactRIO is described, as well as the DAQs.

Chapter 3 describes in detail the proposed digital regulator. The manual tuning procedure is fully analyzed and the auto-tuning algorithm is described.

Chapter 4 shows and discusses the results of tests performed on the power systems using the implemented digital regulator. Hints for future developments are provided.

Appendix A reports some of the schematics of the VMTF power system.

Chapter 1

Magnets test: targets and equipment

1.1 Magnets

Within laboratories, high-energy particle beams, elementary particles or different types of nuclei, are produced by particle accelerators and their associated detection equipment. These beams can be focused on the centre of a detector, providing physicists with intense and controlled collisions for matter science research. A particle accelerator raises the particles energy, simultaneously steering them towards the right direction. These jobs are performed by different devices: RF cavities use electric fields to accelerate particles, while magnets use magnetic fields to steer particles [1].

Protons travel through a pipe which resides between the poles of accelerator magnets. In a dipole, magnetic lines of force emerge from the North pole and re-enter the magnet at the South pole. The field is nearly uniform where the protons travel. Magnet manufacturers arrange these dipoles around a circle, having all their fields pointing straight up. This enables a beam of protons to circulate around in a clockwise direction. Antiprotons, having negative charges, would circulate counterclockwise.

To keep protons in line on the plane of the accelerator ring, another type of magnet called quadrupole is used. A quadrupole is a four-pole magnet, two North and two South poles. The magnetic field in this type of magnet is zero at the dead center, but grows linearly as you move further away from the center. Consequently a proton moving along the center will be left alone by the quadrupole, while a proton wandering off the beam axis will be moved back towards the center. This results in focusing the beam of protons, just like a glass lens does with a light beam. For instance, to hold the particles on track the Tevatron uses 774 niobium-titanium superconducting dipole magnets cooled in liquid helium producing 4.2 Tesla. Another 240 NbTi quadrupole magnets are used to focus the beam.

1.1.1 Conventional magnets

An electric current through a winding generates a magnetic field, whose intensity raises with the number of windings. Surrounding the wire coils with a ferromagnetic material, such as soft iron, strengthens the magnetic field. When placed in a magnetic field, the iron atoms aligns themselves with the magnetic field lines, strengthening the field. The ferromagnetic core increases the magnetic field to thousands of times the strength of the field of the coil alone, due to the high magnetic permeability μ of the ferromagnetic material [2].

Magnet builders can control such a magnet by changing the amount of windings current: higher currents result in stronger fields. Since in accelerators strong fields are required, large currents are used (i.e. nearly 10,000 A for the dipoles). To carry away the heat generated by this current, water is forced to circulate inside the magnet. A dipole magnet is shown in Fig 1.1.

Figure 1.1: CDC103 conventional dipole magnet.

1.1.2 Superconducting magnets

When a magnetic field higher than the ferromagnetic limit of 1.6 T is needed, superconducting electromagnets can be used. Fermilab's Tevatron was the first synchrotron to use this type of magnet. Instead of using ferromagnetic materials, these magnets use superconducting windings cooled with liquid helium, which conduct current without electrical resistance. These allow huge currents to flow, which generate intense magnetic fields. Superconducting magnets are limited by the field strength at which the winding material ceases to be superconducting. Most superconducting magnets coils are made of niobium-titanium (NbTi) alloy embedded in a copper matrix.

Superconducting magnets can handle very high current densities featuring a negligible resistance value. Another feature of superconducting magnets is the stability of the magnetic field in the persistent mode of operation, where no energy is lost as heat in windings. In fact, after the superconducting magnet has been energized, it can be operated in the persistent mode by short circuiting the magnet with a superconductor. This is accomplished by connecting a section of superconducting wire included in the persistent switch across the terminals of the magnet. This section of superconductor can be heated to drive it into the resistive state so a voltage can be established across the terminals and the magnet can be charged or discharged. After reaching the desired field, the heater is turned off and the magnet is shorted by the switch [3]. Therefore, in the persistent mode of operation, the L/R time constant is extremely long and the magnet can be operated for days or even months at a nearly constant field, a feature of great significance where signal averaging must be performed over an extended period of time.

In superconducting magnets a destructive phenomenon, which is called quench, can occur. In a quench a small part of the superconducting material enters into the normal state. A quench typically occurs at the location of the highest field in the magnet. Resistance is restored to that location of superconductor and heating occurs in the magnet. This heat spreads to adjacent areas and drives more of the material to its normal state. The normal state zone continues to spread until the magnet is completely discharged. Any superconducting magnet can be quenched by increasing the current and field indiscriminately, or if the rate of change of the field is too high [4].

Unlike the few volts used in charging the magnet, the voltages generated during a quench discharge can be as high as kilovolts. Initially, the resistive voltage is restricted to the layers of windings near the point where the quench initiated. Internal arcing between layers could occur if sufficient insulation is not provided. During a quench a magnet can be damaged by high voltage, high temperature, and high forces. Heaters are typically installed on the magnets to heat them up in the event of a quench. Heating the whole magnet coil avoids the problem of too much current dissipating in a small part of the magnet coil, resulting in a much reduced temperature overall.

Before conventional and superconducting magnets operate in the main beam line of an accelerator, it is necessary to test them for their usefulness. Power testing is usually performed. This method tests the maximum allowable current through the magnet before quenching, and the quality of its magnetic field. This test ensures optimum quality of all operating beam-line magnets. The Fermilab Magnet Test Facility (MTF) resides inside the Industrial Building 1 (IB1). Several high current and low current power systems are involved in the power testing of both superconducting and conventional magnets.

1.2 Multipulse converters

Some of the high-current power supplies used at the Magnet Test Facility, such as the many Power Energy Industries supplies of the VMTF and the Stand C, rely on multipulse SCR converters. The SCR is a thyristor-based device with three terminals: anode (A), cathode (K) and gate (G) as shown in Fig 1.2.

When the device is reverse biassed (V_{AK} negative) it behaves like a diode and blocks current until enough voltage is applied to cause avalanche breakdown (and consequently device destruction) [6, 7]. When the device is forward biassed (V_{AK} positive) two states are possible:

1. Forward blocking: a switch in the OPEN position, where the device supports a large applied voltage with negligible current flow;
2. Forward on-state: a switch in the CLOSED position, where the device conducts forward current with little forward voltage drop.

The SCR can be turned on by applying a pulse of positive gate current with a short duration provided that it is forward-biased. Once the SCR is turned on, it is latched on. The device can be turned off by applying a negative anode current produced by its power circuit.

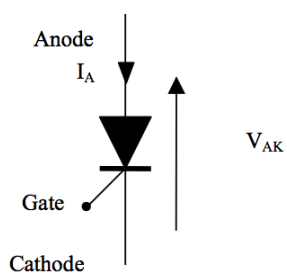


Figure 1.2: SCR schematic symbol.

Multipulse thyristor converters are being employed in industrial applications to control output current/voltage through adjustment of the thyristors' triggering angle. The main advantage of the multipulse rectifier lies in its ability to reduce the line current harmonic distortion. This is achieved by the phase shifting transformer, through which some of the low-order harmonic currents generated by the six-pulse rectifiers are canceled. In general, the higher the number of rectifier pulses, the lower the line current distortion is [8]. Rectifiers with more than 30 pulses are seldom used in practice mainly due to increased transformer costs and limited performance improvements. Each thyristor has a gate firing circuit associated with it which provides gate current when required to do so to fire the device. A control circuit, synchronized to the supply voltages, controls

the firing of the thyristors via the gate firing circuits. The multipulse diode rectifiers can be classified into two types:

- Series-type multipulse rectifiers, where all the six-pulse rectifiers are connected in series on their dc side.
- Separate-type multipulse rectifiers, where each of the six-pulse rectifiers feeds a separate dc load.

Fig 1.3 shows the typical configuration of a 12-pulse series-type diode rectifier. There are two identical six-pulse diode rectifiers powered by a phase-shifting transformer with two secondary windings. The dc outputs of the six-pulse rectifiers are connected in series.

A detailed description of multipulse converters is reported in [8].

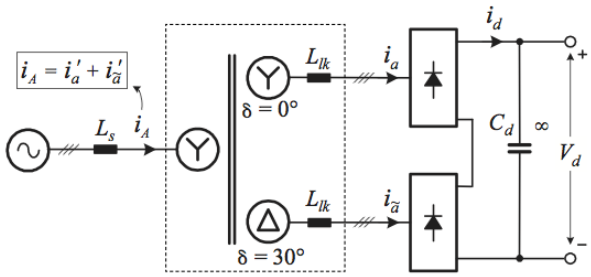


Figure 1.3: Simplified diagram of a series-type 12-pulse series-type diode rectifier.

1.3 Zero-flux current transformers

A current feedback signal is required by the designed digital PID controller and the existing analog regulator as well. Introducing a resistor is the simplest way to generate a current proportional signal. The sensed current flows through a shunt resistor. The voltage is measured across the known resistance and the current value is obtained. However, this approach is not always suitable for high-currents, which are required by accelerator magnets. If a wide range of currents is considered, the shunt resistor characteristics will change with current and temperature. In this section the "zero flux" approach is described. The HITEC TOPACC current transformer, used in both VMTF and Stand C, relies on this principle.

As shown in Fig 1.4, the sensed primary current (I_p) is balanced by a compensating current (I_s) in order to achieve a zero-flux in the ferromagnetic toroid [5]. The zero-flux condition is determined using an AC excitation current (I_e) which drives the ferromagnetic material out of its linear region. The the magnetic susceptibility μ drops causing a change in $\frac{dV}{dt}$ versus I_e. A larger distortion for the polarity is achieved when

I_e adds to the magnetic flux from $I_s + I_p$, a smaller distortion when I_e partly cancels the flux from $I_s + I_p$, and symmetric distortion if I_s perfectly cancels I_p. A feedback loop automatically adjusts I_s to achieve the zero-flux condition.

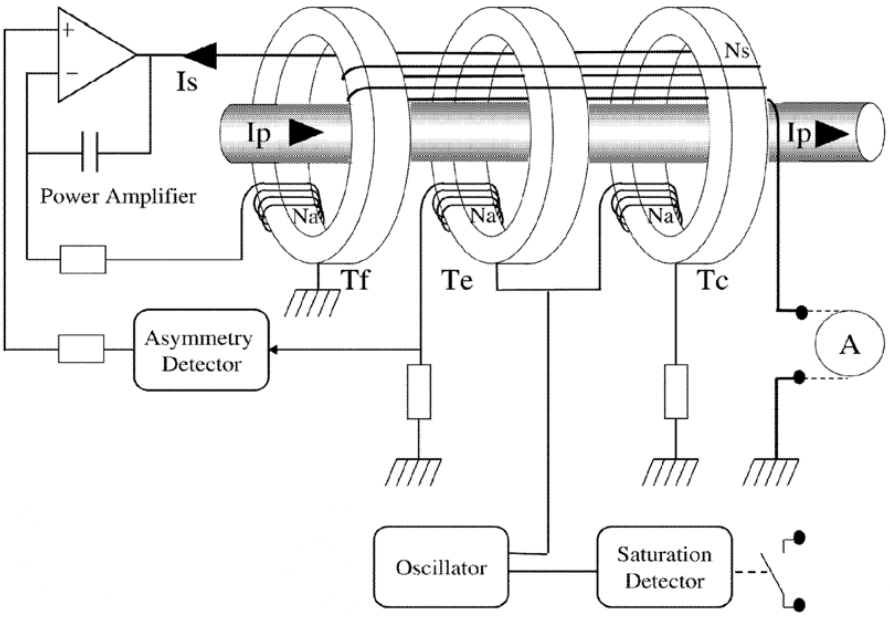


Figure 1.4: Zero-flux transducer.

In its simplest form, if the condition $I_s = I_p$ is verified, the current I_s should be measured. Really, the I_p current could be balanced by the means of several turns. The balancing current I_s is therefore much smaller than I_p and it could be measured by a resistive sensing. The oscillating I_e will induce current in the primary electrode, i.e. causing fluctuations in I_p. To avoid this, a pair of toroids are used. I_e is forced in opposite directions through the two toroids so it causes no net induced current. The response time of such a system is limited by the frequency of the excitation, which in turn is limited by the properties of the ferromagnetic material.

1.4 Power systems for magnets testing

The Testing and Instrumentation (T&I) Magnet Test Facility is supported by several high current and low current power systems used for power testing of both superconducting and conventional magnets.

The superconducting (cryogenic) test stands include the vertical magnet test facility (VMTF), the Tevatron Test Stands 2, and 6, and Test Stand 4, which was designed for testing LHC magnets. Meanwhile, VMTF and test Stand 3, 4 can be powered by the 30 kA cryogenic power system (CPS3), and test Stand 2, 6 can be powered by the 10 kA

cryogenic power system (CPS1). Cryogenic test Stands 3 and 6 are also being used to test High Intensity Neutrino Source (HINS) solenoid magnets and high temperature superconductors (HTS) leads. These tests are supported by low current (330 A) power supplies.

The conventional test stands include test Stand A, B, and C. Stands A is powered by a 150 kW PEI power supplies, Stand B is powered by a 240 kW PEI power supply and test Stand C is powered by two 150 kW PEI power supply in master-slave mode for up to 10 kA total. Stand A doubles as the Booster Corrector Magnet Test Stand and uses six dedicated low current power supplies. Test Stand C is also used to test pulsed magnets and is supported by a dedicated 750 V pulsed power system.

Figure 1.5: The Testing and Instrumentation (T&I) Magnet Test Facility.

Stand C and CPS3 are the power systems on which the proposed digital regulator was tested. Since the Stand C architecture is barely different from the CPS3 one, the former consisting in a subset of the latter, only the more complex system is described.

The CPS3 system supports the High Field Magnet (HFM) testing program at the Vertical Magnet Test Facility (VMTF) stand. Fig 1.6 shows a block diagram of the

30 kA Power System. The 30 kA bus is shown by solid lines, and electrical signals are shown by dashed lines. Another more detailed block diagram is shown in Appendix A.

The VMTF is the only test facility of its kind at Fermilab, with test temperatures reaching down to 1.8 K. However the importance of the VMTF is not limited to Fermilab: this test facility is of great importance on a worldwide scale. In fact some of VMTF's high resolution, precision power tested magnets are used in the historic worldwide collaboration experiment, the Large Hadron Collider Experiment (LHC) at CERN. The CPS3 commits a highly regulated, low-noise and highly reliable test facility for these magnets. The inductances of these magnets range from 30 µH to 90 mH. The different characteristics of magnet tests, such as large range of inductance and fast ramp rates, require high performances for current regulation.

CPS3 consists of six 30 V/5 kA Power Energy Industries (PEI) power supply modules, bussed in parallel to create a 30 kA current capacity, and the following modules built at Fermilab: six 720 Hz filters, two 15 kA/1kV dc solid-state dump switch and a 3 MJ/30 kA/1 kV dc dump resistor. Additional electronic components have been designed and built to provide precise current regulation and distribution of current (I) and current rate of change (I_{dot}). An industrial-type Programmable Logic Controller (PLC) system provides equipment interlocks and monitoring.

The HITEC zero-flux current transformer electronics, the summing amplifier module, the current regulator module, the fast trip module and the VME current transmitter module are located in a temperature-controlled rack in order to meet the strict current regulation and stability requirements. The rack is shown in Fig 1.7.

Figure 1.7: The temperature-controlled rack.

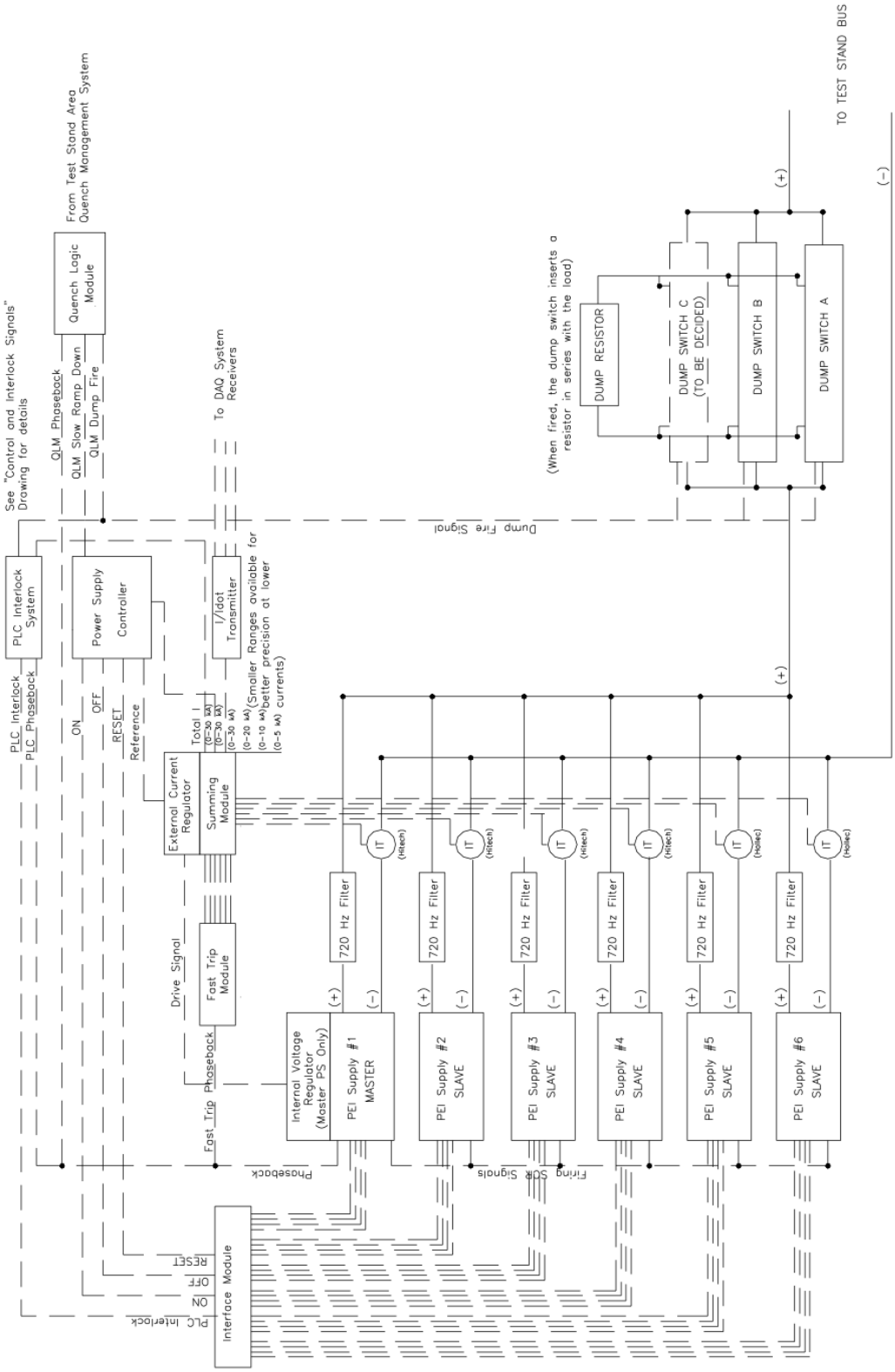


Figure 1.6: Power supply interface block diagram.

1.4.1 Power Supplies

The power supplies consist in six 150 kW Power Energy Industries (PEI) bussed in parallel. Each PEI supply has four firing modules with three Silicon Controlled Rectifiers (SCR) each, one per phase, for a total of 12 SCR's that are combined through inter-phase transformers, and delivers up to 5,000 A dc at 30 Volts. Optionally each supply can be tapped at higher voltages and corresponding lower maximum current (i.e. 5,000 A DC @ 30 V, 2,500 A DC @ 60 V, 1,250 A DC @ 120 V). Some of the schematics of the PEI power supply are reported in Appendix A. One of this six power supplies is the Master Power Supply (MPS) and provides the SCR firing signals for all modules. The MPS voltage regulator is cascaded to an external analog proportional-integral (PI) current regulator. Voltage regulators for the other 5 slave PEIs are removed or disabled. This power system can run with just the MPS and up to all six power supplies.

The power supply outputs float with respect to ground and are grounded through a symmetric grounding scheme. The bus of all power systems within the Magnet Test Facility is grounded in order to provide equipment and personnel safety. The grounding scheme is sensitive to any asymmetric (fault not at the center of the coil) ground fault. The purpose of a ground fault detection circuit is to detect ground current associated with an electrical fault of a magnet coil to ground and initiate a slow ramp down to minimize the inductive voltage across the coil and therefore minimize fault current.

The filtered outputs of the supplies are connected to a spine of 2" × 4" bus work that runs between them and carries the total current through a 30kA dump switch and then to the magnet load. The power supply filters have $2\mu F$ capacitors from each output terminal to ground to reduce the common-mode bouncing of the rectifier supplies. A common-mode capacitor filter was also installed at the load side to further reduce noises. The most frequently observed low frequency noises are 60 Hz, 120 Hz and 180 Hz sub-harmonics, besides the 720 Hz ripple inherited in SCR firing.

A Praeg-style filter [11] is added to each power supply to reduce the 720 Hz ripple. This ripple is caused by the twelve-pulse converters that means its frequency is $12 \times 60\,Hz = 720\,Hz$. Each filter includes: a serial $250\,\mu H$ choke cooled by Low Conductivity Water (LCW), two parallel capacitor banks (a 5.5 mF bank and a 27 mF) in series with a $200\,\Omega$ resistor.

1.4.2 Dump Switch and Resistor

Sometimes is necessary to dump the energy stored inside the magnet. This is accomplished by quickly switching, using two 15,000 A 1000 V dc solid state dump switches [12], a load resistor in series with the bus. These six SCR's, mounted in water-cooled heat-sinks, are connected in parallel with the dump resistor. This means that usually the current flows through the SCR's and, once these are switched off, the current will flow trough the dump resistor. The switches are commutated off from stored energy in approximately $25\,\mu s$ after detection of a fault or a trip command.

The dump switch works in combination with the dump resistor which dissipates the stored energy from the magnet after a quench or trip. The dump resistor was built from air-cooled stainless steel elements. The adjustable taps are 0, 15, 30, 60, 90 and 120 $m\Omega$. It is rated for a maximum current of 30,000 A, a maximum energy dump of 3 MJ, and a maximum voltage across the resistor of 1000 V dc.

1.4.3 Current transformers and Summing Amplifier

Six bipolar zero-flux current transformers measures the current flowing in the bus. A HITEC system TOPACC type 60-8 bipolar, rated for a current of 6,000 A is used for each PEI module. The HITEC provides a DC accuracy error less than 30 ppm, with a temperature coefficient less than 1.5 ppm/K and drift less than 10 ppm/year. The datasheet is reported in [14].

A summing amplifier sums the output of the six zero-flux current transformers. This summed signal is sent to the current regulator and to a VME current transmitter module for distribution and monitoring purposes. The precision resistors used to build the summing amplifier have an absolute tolerance of ±0.001%, and an absolute temperature coefficient of ±0.8 ppm/Deg C. Stability tests made on this unit showed less than 2.7 ppm drift in 90 hours.

1.4.4 VME Current Transmitter/Receiver Modules

The current (I) and current rate of change (I_{dot}) is distributed via fiber optic cable (maximum length 250 m) toward up to 8 different locations inside the Fermilab Magnet Test Facility. This is achieved by a current transmitter and receiver module, based on the VME bus. The measured accuracy of the current readout is ±10 ppm (integrated over one Power Line Cycle) and the resolution is ±2 ppm. The current receiver module accepts the fiber optic signal from the transmitter module and provides six buffered analog I outputs and three analog I_{dot} outputs. The measured analog current value accuracy is ±25 ppm, with a resolution of ±2 ppm.

1.4.5 Current Regulator

The summing amplifier output signal controls the current with a feedback loop. The analog current sense signal is subtracted from a current reference signal and the error is amplified in a load compensation circuit with adjustments for the load inductance and resistance. The setpoint for this external current regulator is provided by a Power Supply Controller. The current regulator is illustrated in Fig 1.8.

The load compensation circuit is implemented by an analog PI controller, conveniently referred to as current regulator. The MPS voltage regulator is fed by the output of the

current regulator. Since the 30 kA Power System aims to drive a wide range of load inductance and resistance values, the current regulator includes independent settings of load resistance and inductance for tuning the control loop to each particular load. Stability measurements performed at 10 kA show less than 3.5 ppm drift of the current receiver output over a period of 2 hours (a typical magnetic measurement duration). Its AC and DC gain can be adjusted for load inductance and resistance.

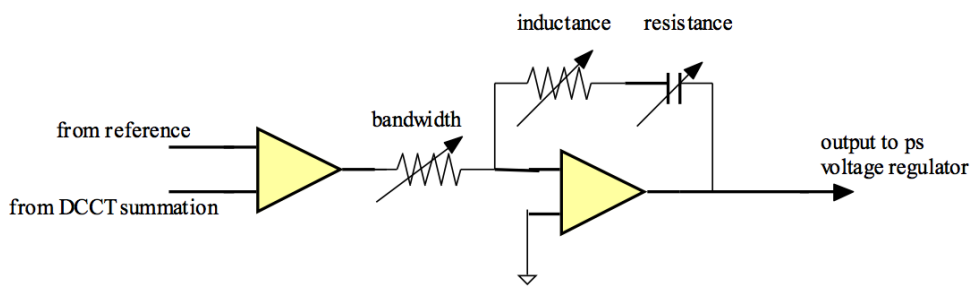


Figure 1.8: Illustration for Analog Current Regulator.

The existing discrete settings for "inductance" are: $0.05\,mH$, $0.5\,mH$, $2\,mH$, $4\,mH$, $10\,mH$, $25\,mH$, $50\,mH$ and $100\,mH$. The existing discrete settings for "resistance" are: $100\,\mu\Omega$, $500\,\mu\Omega$, $1\,\mu\Omega$, and $2\,\mu\Omega$. Normally, for all super-conducting magnet tests it is set at $500\,\mu\Omega$ to compensate the bus resistance, while for short bus test it is set at $100\,\mu\Omega$ to achieve better regulation. If it's set at $100\,\mu\Omega$, the variable capacitor will be adjusted to zero.

The existing discrete settings for "bandwidth" are 1 Hz, 2 Hz, 5 Hz, 10 Hz and 20 Hz. Larger bandwidth corresponds to larger resistor value in Fig 1.8. As suggested by the designer of the regulator, the bandwidth must be set at 20 Hz under "normal" condition.

The overall control schematic is shown in Fig. 1.9.

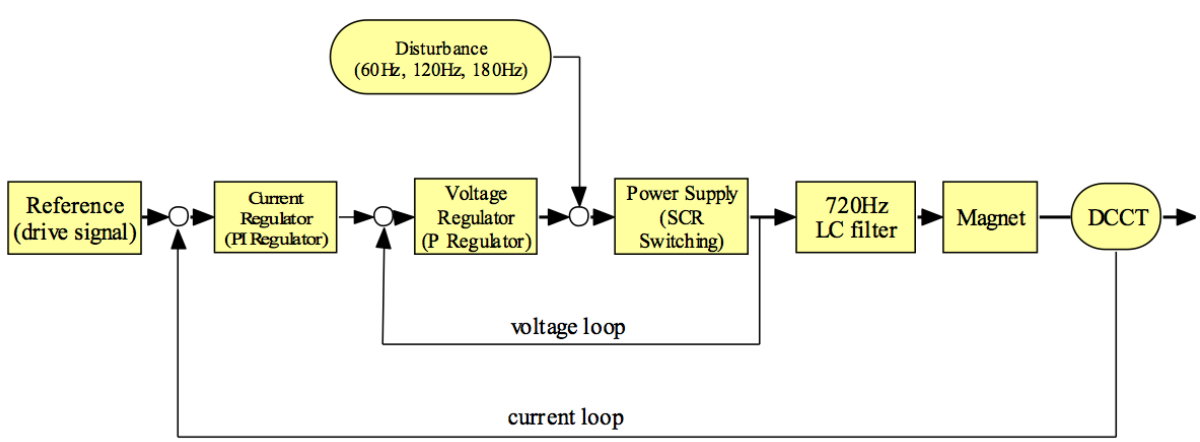


Figure 1.9: Current and Voltage Regulation Loops.

Tab 1.1 lists the name of some magnets that were tested, along with the optimal control settings of resistance, inductance, and bandwidth for the existing current regulator.

Magnet Name	Magnet Inductance	Date Tested	R-Setting	L-Setting	Bandwidth	Voltage Regulator ID	Peak-to-Peak Ripple	Notes
SR04	35μH	Sept. 06	500μΩ	0.05mH	10Hz	3	70A	
MQXB20	16mH	Oct. 06	500μΩ	10mH	20Hz	4	5A	
SQ02c	2mH	Oct. 06	500μΩ	2mH	20Hz	4	8-10A	
HFDM06	200μH	Nov. 06	500μΩ	0.5mH	20Hz	4	8-10A	
TQC01b	5mH	Jan. 07	500μΩ	4mH	10Hz	4		500A/s required
TM01	1.1mH	May 07	500μΩ	0.5mH	20Hz	4		
TQS01a	5mH	June 07	500μΩ	4mH	20Hz	4		
TQC02e	5mH	Oct. 07	500μΩ	4mH	20Hz	4		
LM02	2.2mH	Dec. 07	500μΩ	2mH	5Hz	1 then 4		
TQC02a	5mH	Jan 08	500μΩ	4mH	10Hz	4		
SR06	22μH	Mar. 08	500μΩ	0.05mH	5Hz	4		
SR07	22 μH	July 08	500μΩ	0.05mH	5Hz	4		
TQC02b	5mH	Aug. 08	500μΩ	4mH	10Hz	4		
HSM01	322 μH	Nov. 08	500μΩ	0.5mH	20Hz	4		
TQM01	0.4-2mH	Jan. 09	500μΩ	2mH	20Hz	4		
TQM02	0.4-2mH	Mar. 09	500μΩ	2mH	20Hz	4		
TQM03	0.4-2mH	Mar. 09	500μΩ	0.5mH	20Hz	4		
LQS01	12mH	Oct. 09	500μΩ	10mH	20Hz	4		
TQM03C	0.4-2mH	Feb. 10	500μΩ	0.5mH	20Hz	4		
APUL	50μH	Mar. 10	500μΩ	0.05mH	10Hz, 5Hz	4		
TQC02eb	5mH	Mar. 10	500μΩ	4mH	10Hz	4		
TQM04	0.4-2mH	May 10	500μΩ	2mH	20Hz	4		
LQS01b	12mH	June 10	500μΩ	10mH	20Hz	4		
Mu2e	~14mH	Sep. 10	500μΩ	10mH	10Hz	4		
HSM02	322 μH	Nov. 10	500μΩ	0.5mH	20Hz	4		

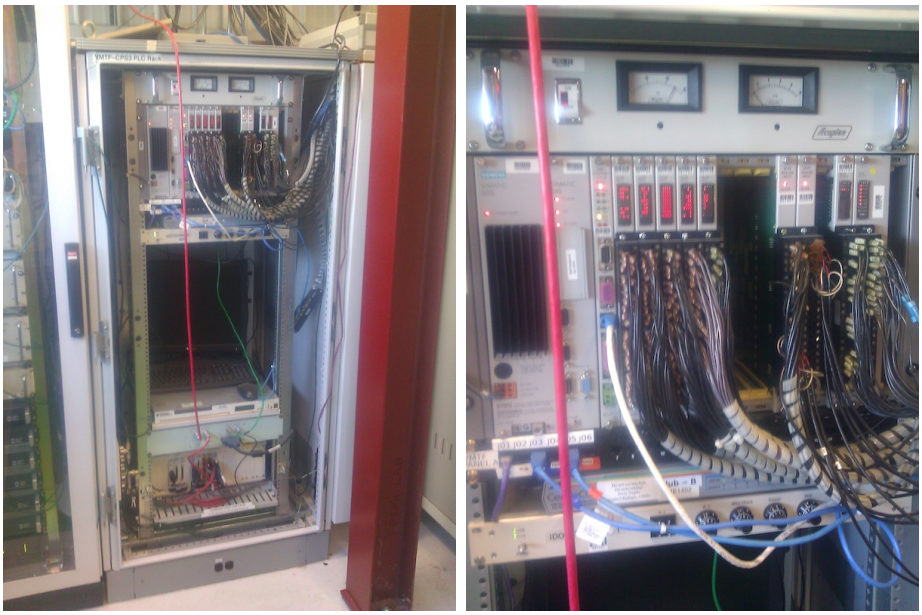
Table 1.1: Optimal control settings of resistance, inductance, and bandwidth for some magnets using the analog current regulator.

1.4.6 Personnel and Equipment Safety

Opening cabinet doors and covers while the system is powered represents a personnel hazard and mechanical switches are provided to detect these situations. In adherence to Fermilab's safety regulations, personnel safety is provided by a hardwired interlock chain. This system is called the "Electrical Trip System" (ETS). In the event that any cabinet door or any cover is opened while the system is powered, the ETS system will take three simultaneous actions to protect personnel from electrical hazards:

1. immediately initiate a power system phaseback;
2. fire the dump to quickly extract stored energy;
3. remove the external interlock permissive to each PEI supply.

The status of door switches is also monitored by the PLC system, so the operator will be able to tell what was the cause of the system trip, and to initiate a phaseback and fire the dump as backup of the ETS system.



(a) (b)

Figure 1.10: (a) The PLC rack of the VMTF; (b) The PLC modules.

A Programmable Logic Controller (PLC) provides most of the equipment safety interlocks and system status monitoring. This system is based on the 1500 W Helium Refrigerator Control System [15], and includes the series 505 Siemens module for PLC and Input/Output modules, Ethernet communication to the control room, and GE/FANUC FIX32 Human Machine Interface. The PLC monitors the status of various temperature, flow, and other switches and devices. There are 135 physical Input/Output points in this system. In addition to the PLC system, a module called the "Fast Trip Module" is used.

The Fast Trip Module monitors the DCCT signal from each PEI to detect a positive or negative current imbalance: the module will quickly initiate a phaseback (without firing the dump) to avoid further equipment damage. Current imbalance can be caused, for instance, by a shorted SCR. Because the response time required for this type of condition is very short ($<$ 16 ms to avoid further damages of the SCRs), the PLC is not suitable to provide this fast interlock and a separate module performs this function.

In addition to the phaseback signal, the Fast Trip Module intercepts the Drive Signal going the Master PEI "External Reference" input. If the Fast Trip Module trips, the Drive Signal is driven to a negative value. Otherwise, it is not affected. The purpose of this action is to provide a backup to the phaseback signal.

Once tripped, the Fast Trip Module requires a manual reset because this fault condition is serious and must be investigated by a power knowledgeable person.

1.5 Project assignments

The existing CPS3 system meets the following requirements:

- Repeatability: $<$ 20 ppm of reading (e.g., 0.6 A for a 30 kA measurement);
- Accuracy: $<$ 300 ppm of reading (e.g., 9 A for a 30 kA measurement);
- Resolution: $<$ 1 ppm of reading (e.g., 0.03 A for a 30 kA measurement).

However, as it will be further discussed, improvements have been required.

Assuming well-known magnet characteristics, the analog current regulator enables a proper selection of the inductance, resistance and bandwidth for the specific magnet under test. Sometimes, for example, the L value of a magnet falls between two discrete settings. If magnet characteristics are barely known or even optimal settings do not give expected results, several combinations of all parameters should be tried.

The test setup is often slowed down by the tuning procedure, since, in case of barely known or unknown magnet characteristics, several test are required to fix the optimal regulator gain. The implemented digital regulator aims at providing an automatic tuning procedure to save human efforts during the setup procedure. No matter what magnet characteristics are, all parameters will be automatically tuned. The smart controller will detect the system step response, recording overshoot and settling time, thus adjusting the PID parameters accordingly. The settings found, both manually or by the algorithm, are saved to be recalled in further tests.

As shown by former test, the existing system response gets worse if magnets with edge characteristics are selected. For example, testing magnets with a $35\mu H$ inductance results in a 180 Hz resonance with the LC filter components. As a consequence, the current ripple reaches dangerous levels, as high as 70 A.

On the contrary, if high inductance values are selected, for example 30 mH, conventional setting leads to glitches in the current ramping and trips the quench detection system. The situation is even worse when trying ramping up and down the current at a faster rate such as 500 A/s.

A compactRIO-based digital controller has been developed to improve performances and reliability, achieving low-complexity of the overall system. The block diagram is shown in Fig 1.11. The analog PI current regulator is replaced by the compactRIO-based real-time PID regulator. As it will be shown by simulation and experimental results, overshoot are heavily reduced and a faster settle time is achieved by the proposed solution.

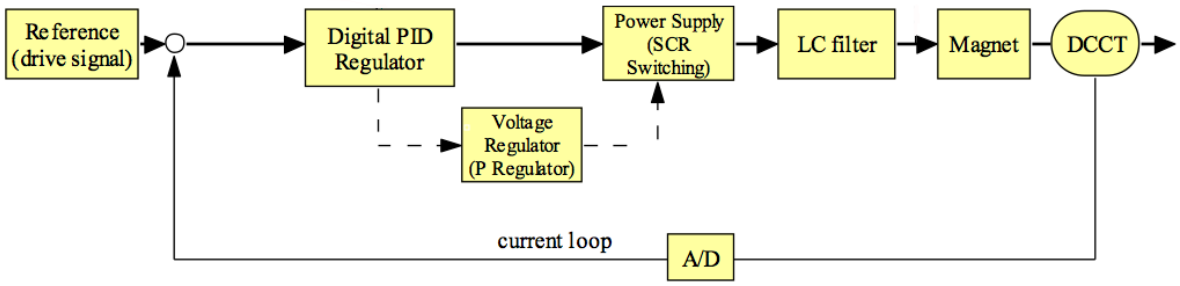


Figure 1.11: The proposed regulation system

The description and requirements as provided by the Technical Division of Fermilab for the present project are here reported.

Design a digital regulator and current readout distribution system for DC power systems. The digital regulator will be used to test conventional and superconducting accelerator magnets. The power supply current ranges are from 1 A to 30kA. This system should include digital PID regulation with automatic tuning for a broad range of inductive loads. This project will require LabVIEW programming for FPGA and Realtime and will be based on National Instruments CompactRIO. Furthermore the digital regulator will have digital and analog I/O interface to the power systems.

Following are listed the desired requirements of the digital regulator:

- Provide Stability of Current Regulation $<$ 10ppm of Full Range for typical $\pm$10% AC Input Voltage change, load change, and temperature change;
- Provide ripple suppression at least 10 times compared to present CPS3 ripple level;
- Provide manual settings of optimal PID parameters for full range of loads (magnets) with low granularity;
- Provide Current Profile function;
- Develop an auto-tuning algorithm for PID parameters;
- Provide Slow Ramp Down function;
- Provide Phaseback function;
- Provide Current Limit and Ramp Rate Limit protection.

The tasks to be performed are:

- Develop the general software and hardware architecture based on requirement specifications;
- Develop PID control and tuning algorithms using LabVIEW software for Realtime and FPGA and characterize using low current power supplies;
- The design solutions should improve current ripple noise and overshoot and eliminate oscillations over a broad range of inductive loads;
- Fully test and characterize the final product using different loads and power supplies;
- Prepare software and hardware documentation.

Chapter 2

Design and development tools

2.1 Introduction

In this chapter, the architecture of the Digital Regulator is described. Basically the proposed PID Digital Regulator is implemented on a CompactRIO (cRIO) made by National Instruments (NI). This small sized, rugged system for industrial control systems allowed to build and test this custom embedded system in a short time frame. cRIO is programmed in National Instruments LabVIEW, that is the industrial Standard graphical programming environment characterized by high code reuse, good documentation and easy debugging capability.

2.2 National Instruments CompactRIO

The heart of the Digital Regulator runs on a National Instruments hardware chassis (see Fig 2.2a) based upon NI's Compact RIO (Reconfigurable I/O) architecture. The National Instruments CompactRIO platform is an advanced embedded control and data acquisition system designed for high-performances, high-reliability applications.

The implementation on an internal FPGA, which allows several processes to be simultaneously run, is a key advantage brought by this configuration. This is a true parallel process environment at a minimum of 40 MHz. Further, all subsystems are programmed by LabVIEW. In fact three pieces of software must be written, for the FPGA, the Real-Time target and the Host PC, but they all share the common graphical programming paradigm of Labview, the virtual instrument (VI).

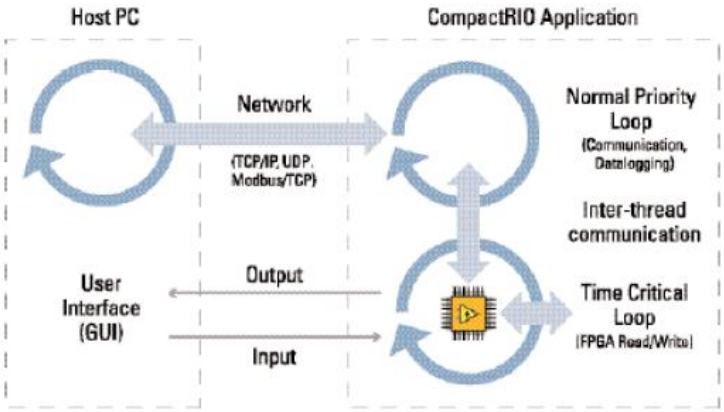


Figure 2.1: CompactRIO Software Architecture.

CompactRIO includes an embedded processor with a real-time operative system, a high-performance FPGA and hot-swappable I/O modules to form a complete control system. Each module is directly connected to the FPGA and the FPGA is connected to the real-time processor via a high-speed PCI bus. The National Instruments CompactRIO device used for the Digital Regulator is composed by the NI cRIO 9118 (see Fig 2.2a), the cRIO-9024 (see Fig 2.2b) and further modules further listed in this chapter.

(a) (b)

Figure 2.2: (a) NI cRIO-9118 chassis; (b) NI cRIO-9024 controller.

2.2.1 Chassis: cRIO-9118

The cRIO-9118 is an 8-slot chassis with a Virtex-5 LX110 Field Programmable Gate Array (FPGA). Main features are listed in Tab 2.1.

FPGA type	Virtex-5 LX110
Number of flip-flops	69,120
Number of 6-input LUTs	69,120
Number of DSP48 slices (25 × 18 multipliers)	64
Embedded block RAM	4,608 kbits

Table 2.1: Main features of the FPGA on the cRIO-9118 chassis.

The chassis is the heart of the CompactRIO system because it includes the reconfigurable I/O core. The RIO field-programmable gate array core features an individual connection to each I/O module, accessible by LabVIEW with elementary I/O functions to read or write signal information from each module. Since no shared communication bus between the RIO FPGA core and the I/O modules is provided, I/O operation in each module could be synchronized with a 25 ns resolution. The RIO core can perform local integer-based or fixed-point signal processing, decision making and direct interface between modules.

The FPGA is connected to the real-time processor inside the controller via a local high-speed PCI bus interface. The real-time controller can retrieve data from any control or indicator on the RIO FPGA application front panel through Scan Interface or simple FPGA Read/Write function. The RIO FPGA can also generate interrupt requests (IRQs) to synchronize the real-time software execution with the RIO FPGA.

2.2.2 Real-Time Controller: cRIO-9024

The real-time controller includes a processor that reliably and deterministically executes LabVIEW Real-Time applications and offers multirate control, execution tracing, onboard data logging, and communication with peripherals. Typically, the real-time controller is used to convert the integer-based I/O data to scaled floating-point numbers. In addition, it performs single-point control, waveform analysis, data logging, and Ethernet/serial communication.

The embedded processor in the cRIO-9024 is a 800 MHz PowerPC Freescale MPC8377 that runs the WindRiver VxWorks real-time operating system. The cRIO-9024 also features 512 MB DRAM and 4 GB nonvolatile memory. A resume of the features of this device are listed in Tab 2.2.

Processor Core Type	PowerPC Freescale MPC8377
CPU Clock Frequency	800 MHz
System Memory	512 MB
Ethernet (# of ports)	2
Ethernet Port Type	100BaseTX , 1000BaseT , 10BaseT
Serial Ports (RS232)	1
USB Ports	Yes
Number of Slots	0
Input Voltage Range	9 V - 35 V
Recommended Power Supply:	24V
Power Consumption	35W
Operating temperature range	–20 to 55 °C

Table 2.2: Characteristics of the controller cRIO-9024.

2.2.3 DAQs

Following are described all the C series modules used in the CompactRIO to implement the PID Digital Regulator.

The NI 9222 is a high-speed, simultaneous C Series module for use in CompactRIO chassis. Four 16-bit analog-to-digital converters (ADCs) for simultaneous sampling at up to 500 MkS/s per channel are implemented.

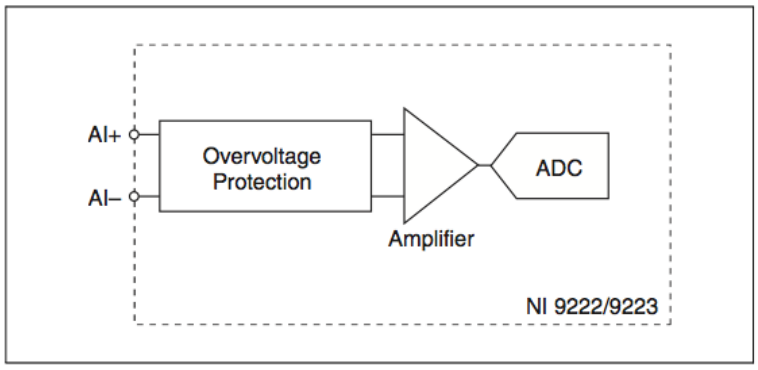


Figure 2.3: Input Circuitry for One Channel of the NI 9222.

The NI 9222 analog input channels are floating with respect to earth ground and each to other. The incoming analog signal on each channel is buffered, conditioned, and then sampled by a 16-bit successive approximation register (SAR) ADC. Each channel provides an independent signal path and ADC, enabling the simultaneous sampling of all four channels. Refer to Fig 2.3 for an illustration of the circuitry for one channel. It should be noted that the NI 9222 does not offer any anti-aliasing filter stage at the

input and this has to be provided. Stability parameters of the NI 9222 are listed in Tab 2.3.

Stability Gain drift	6 ppm/°C
Offset drift	29 µV/°C

Table 2.3: Stability of the NI 9222.

The NI 9239 is a 4-channel, 24-bit C Series analog input module for use in a CompactRIO chassis (or on a NI CompactDAQ as well). Detailed specifications for the NI 9239 are provided in [22].

In this module a channel-to-channel isolation that provides protection from harmful voltage spikes up and also eliminates measurement errors caused by ground loops. The NI 9229/9239 analog input channels are floating with respect to earth ground and each to other. The incoming analog signal on each channel is conditioned, buffered, and then sampled by a 24-bit Delta-Sigma ADC. This board provides four channels simultaneous sampling, so that each channel provides an independent signal path and ADC. Refer to Fig 2.4 for an illustration of the circuitry for one channel.

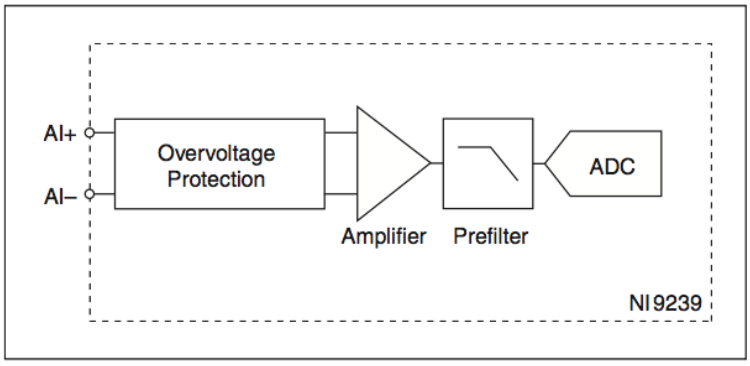


Figure 2.4: Input Circuitry for One Channel of the NI 9239.

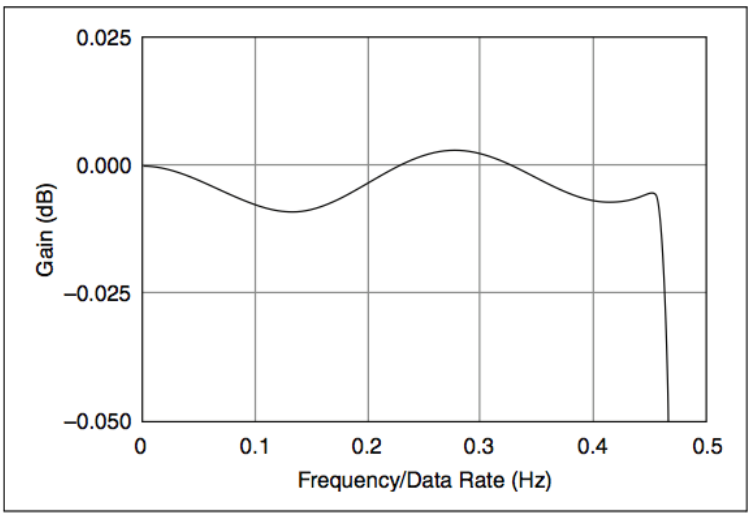


Figure 2.5: Typical Passband Response of the NI 9239.

The NI 9239 features analog pre-filtering and digital filtering for out-of-band signal rejecting. The signals within the passband have frequency-dependent gain or attenuation. The small amount of variation in gain with respect to frequency is called the passband flatness. The digital filters of the NI 9239 adjust the frequency range of the passband to match the chosen data rate. Therefore, the amount of gain or attenuation at a given frequency depends on the data rate. Fig 2.5 shows typical passband flatness for the NI 9239. Also stability parameters of the NI 9239 are reported in Tab 2.4.

Stability Gain drift	±5 ppm/°C
Offset drift	±26 µV/°C

Table 2.4: Stabilty of the NI 9239.

The NI 9269 is a four-channel, 100 kS/s per channel Analog Output module for the C Series chassis for NI CompactRIO (and NI CompactDAQ). This module provides channel-to-channel isolation and the ability to stack channels to output up to 40 V.

The analog output channels are floating with respect to earth ground and each to other. A digital-to-analog converter (DAC) is included in each channel. Each channel provides an independent signal path, enabling the simultaneous update of all four channels. The DAC is implemented by a 16-bit R-2R network. Further, each channel provides overvoltage and short-circuit protection. Refer to Fig 2.6 for an illustration of the output circuitry for one channel of the NI 9269. Refer to the Specifications section in [23] for more informations.

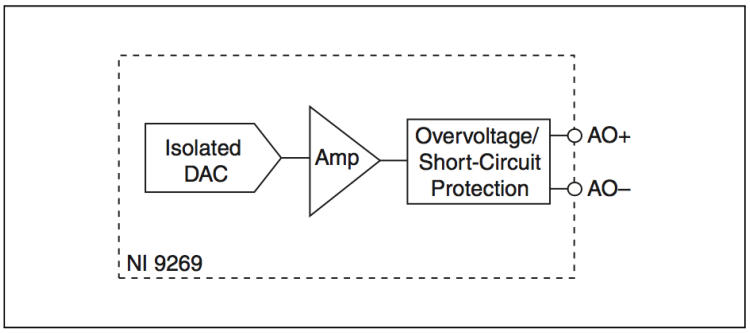


Figure 2.6: Output Circuitry for One Channel of the NI 9269.

The NI 9401 is an eight-channel, 100 ns bidirectional digital input C Series module for CompactRIO chassis. It is possible to configure the direction of the digital lines on the NI 9401 for input or output by nibble. Each channel is compatible with 5 V/TTL signals and features 1,000 Vrms transient isolation between the I/O channels and the backplane.

The NI 9401 has a 25-pin DSUB connector that provides connections for eight digital input/output channels. The pin-out of the DSUB connector is shown in Fig 2.7.

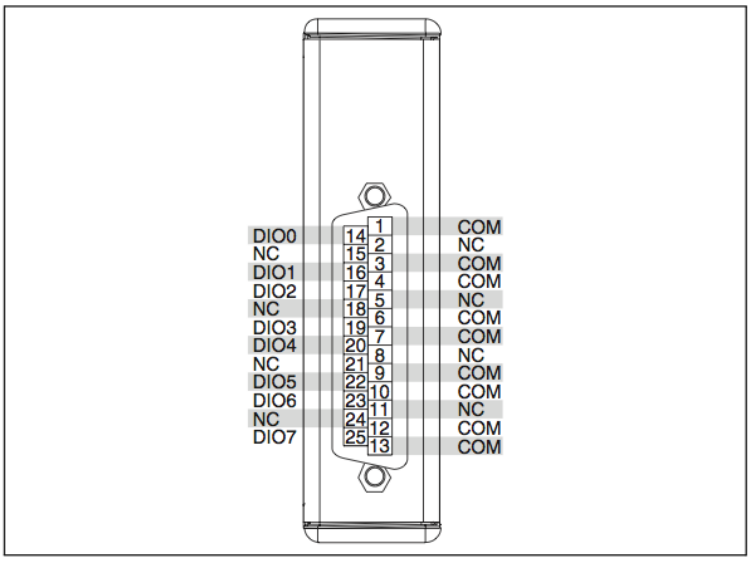


Figure 2.7: NI 9401 Pin Assignments.

Each channel has a *DIO* pin to which you can connect a digital input or output device. The eight DIO channels are internally referenced to COM, so it is possible to use any of the nine COM lines as a reference for the external signal. The DIO channels are grouped in two ports, one containing channels 0, 1, 2, and 3, and one containing channels 4, 5, 6, and 7. Each digital port is independently configurable in software for input or

output (all four channels in the port must share the same line direction). Each channel also has a pull-down resistor and includes over-voltage, over-current, and short-circuit protection.

Since this module is used not only for slow-changing signals (e.g. Ramping_Down request) but also to transmit the value of current and its derivative for remote monitoring, it is useful to report the characteristics listed in Tab 2.5a and Tab 2.5b.

8 input channels	9 MHz
4 input channels	16 MHz
2 input channels	30 MHz

(a)

8 input channels	5 MHz
4 input channels	10 MHz
2 input channels	20 MHz

(b)

Table 2.5: (a) Maximum input signal switching frequency by number of input channels, per channel; (b) Maximum output signal switching frequency by number of output channels with an output load of 1 mA, 50 pF, per channel.

2.3 National Instruments LabView

LabVIEW is a graphical programming environment used by millions of engineers and scientists to develop sophisticated control systems using graphical icons and wires that resemble a flowchart. It offers integration with thousands of hardware devices and provides hundreds of built-in libraries for advanced control, analysis, and data visualization. The LabVIEW platform is scalable across multiple targets and operative systems and, in the case of CompactRIO, LabVIEW can be used to access and integrate all of the components of the reconfigurable I/O (RIO) architecture.

The National Instruments CompactRIO platform requires two different LabVIEW software modules, one for the Real-Time processor and one for the FPGA. These modules contain custom functions specific to the Real-Time processor or the FPGA in addition to all the functionalities of the Standard LabVIEW module. The code for both the Real-Time processor and the FPGA is developed on a host computer. The program for the FPGA is developed by using a standard LabVIEW software module called "LabVIEW FPGA Module". The LabVIEW FPGA code is then translated to VHDL code and compiled using the Xilinx tool chain. The program for the Real-Time processor is also developed by using a standard LabVIEW software module, the "LabVIEW Real-time Module". When ready, the code for the Real-Time processor and the FPGA is downloaded to the CompactRIO device via Ethernet. Once the code is downloaded, the CompactRIO can run in a stand-alone mode or communicate directly with a host over a standard Ethernet connection.

The LabVIEW programming environment provides a graphical High-Level Synthesis Design Tools (HLS) for FPGA programming. Since parallelism and data flow are clearly

represented, Labview is well-suited for FPGA programming [25]. Specific features are provided to test the effective behavior of the FPGA logic.

LabVIEW FPGA compilation tools automate the compilation process, so it's possible to start the process with a click and receive reports and errors, if any, as compilation stages are completed. If timing errors do occur because of the code design, LabVIEW highlights critical paths graphically to expedite the debugging process.

The PID and Fuzzy Logic Toolkit is provided by National Instruments to speed-up the design process of complex control systems, such as a PID regulator. This toolkit provides many blocks to easily implement PID algorithms and auto-tuning techniques. Some of these algorithms put the basis for the here discussed PID Digital Regulator.

Chapter 3

Architecture of the Digital Regulator

3.1 PID regulator

The PID controller, which consists of proportional, integral and derivative elements, is widely used in feedback control of industrial processes. The transfer function of the PID controller is the following:

$$H(s) = K_p + \frac{K_i}{s} + K_d s = \frac{K_d s^2 + K_p s + K_i}{s}$$

where $\mathrm{K_p}$ is the proportional gain, $\mathrm{K_i}$ the integral gain and $\mathrm{K_d}$ the derivative gain [26].

Proportional control, also known as ratio control, is a control action correcting the deviation from the set level back toward the setpoint. The correction is proportional to the amount of error. Higher K_p leads to better speed of response and smaller steady-state error. Yet proportional control does not usually work effectively by itself, requiring an integral action to remove the steady-state error. [27]

To drive the output of the system to the chosen setpoint, integral control, also known as reset control, is added. The integral action integrates the error from the starting time to the current time and supplies control effort to drive steady state error to zero. An integral control signal can be used in conjunction with the proportional corrective signal. In the controller, the added integral signal reduces the error signal that caused the output deviation from the setpoint. Therefore, over a period of time, the process deviation from the setpoint is reduced to minimum. However, this correction takes a relatively long period of time.

To speed up this correction, derivative control is added to the proportional-integral system. Derivative control, also known as rate control, produces a corrective signal based on the rate of change of the signal. The faster the change from the setpoint, the larger the corrective signal. This provides faster action than the proportional-integral system signal alone.

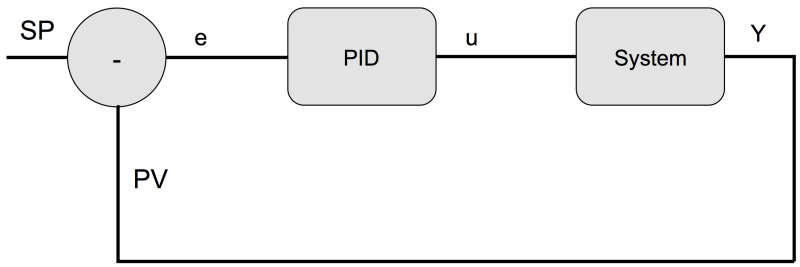


Figure 3.1: Unity Feedback System.

In the schematic shown in Fig 3.1, the variable (e) represents the tracking error, the difference between the desired input value (SP) and the actual output (Y). This error signal (e) will be sent to the PID controller, and the controller computes the proportional, the integral and the derivative part of this error signal. The signal (u) just past the controller is now equal to [28]:

$$u = K_p e + K_i \int e dt + K_d \frac{de}{dt}$$

A proportional controller (K_p) will have the effect of reducing the rise time and will reduce but never eliminate the steady-state error. An integral control (K_i) will have the effect of eliminating the steady-state error, but it may make the transient response worse. A derivative control (K_d) will have the effect of increasing the stability of the system, reducing the overshoot, and improving the transient response [29, 30]. Effects of each of controllers K_p, K_d, and K_i on a closed-loop system are summarized in the Tab 3.1 [31].

These correlations may not be exactly accurate, because K_p, K_d, and K_i are dependent on each other. For this reason, Tab 3.1 should only be used as a reference when determining the values for K_p, K_d, and K_i [32].

CL RESPONSE	RISE TIME	OVERSHOOT	SETTLING TIME	S-S ERROR
Kp	Decrease	Increase	Small Change	Decrease
Ki	Decrease	Increase	Increase	Eliminate
Kd	Small Change	Decrease	Decrease	Small Change

Table 3.1: Effect of each term of PID Controllers on closed-loop system.

3.2 Digital Regulator Architecture

As described in Chapter 2, the Digital Regulator is implemented on a National Instruments Compact RIO. The architecture of the implemented digital regulator consists of three parts:

1. FPGA VI running on the Virtex-5 target.
2. Real-Time VI hosted by the operating system on the Freescale MPC377.
3. PC Host application executed by a remote computer.

3.3 FPGA target

The most important part of the implemented regulator is the PID algorithm itself. A considerable amount of time was demanded to the comparison of all the available PID algorithms, in order to choose the best solution for controlling the process variable to the desired current. In particular National Instruments provides two PID VIs, one of these featuring auto-tuning capabilities. These VIs have been shown reasonable performances in line with the existing analog regulator.

Good results on rising-time values have been achieved using PID VI block provided by "NI LabVIEW PID and Fuzzy Logic Toolkit", while better performances in regulation stability have been achieved with the "Control Loop (Fixed Point PID)" provided by NI SoftMotion Module for LabVIEW 8.6.

The first algorithm is a 16-bit PID and, since the sigma-delta analog input is a 24-bit DAQ, the use of this VI block resulted in unsatisfactory stability in shorted-bus test, but still in line with the performances of the existing analog regulator.

The second algorithm is a 32-bit PID algorithm mainly thought for motion control applications. The main advantage of this algorithm resides on the possibility to make the most of the 24-bit analog input. In fact, the stability in the steady-state current regulation in shorted-bus tests overcame the existing regulator one. On the contrary, the main disadvantage of this VI consists in the intrinsic high gain of the control algorithm. In fact, parameters higher than $K_p = 1$, $K_i = 1$, $K_d = 0$ resulted in undesired current oscillations and overshoots during the transients.

Another attempt was to reduce the number of bits of the digitalized process variable, that enabled the tuning of the regulator to values different from $K_p = 1$, $K_i = 1$. The disadvantage of this method consists in a worse current regulation when compared to a full 24-bit approach.

These tests have been shown that none of the available algorithms meets the provided requirements for the regulator, and further proves that a full 24-bit algorithm had to

be developed from scratch in order to provide low granularity PID parameters for full range of magnets.

The implemented VI, shown in Fig 3.2, allows to achieve fine tuning capabilities and best performances. This VI consists in three "frames" shown in Fig 3.3(a), 3.3(b), 3.3(c). The PID time loop is set at $20\mu s$ and it can be easily changed from the real-time VI. The sign of the feedback signal can also be changed. In fact, sometimes cables pinout changes from one test stand to one other and therefore the feedback signal polarity should be changed accordingly.

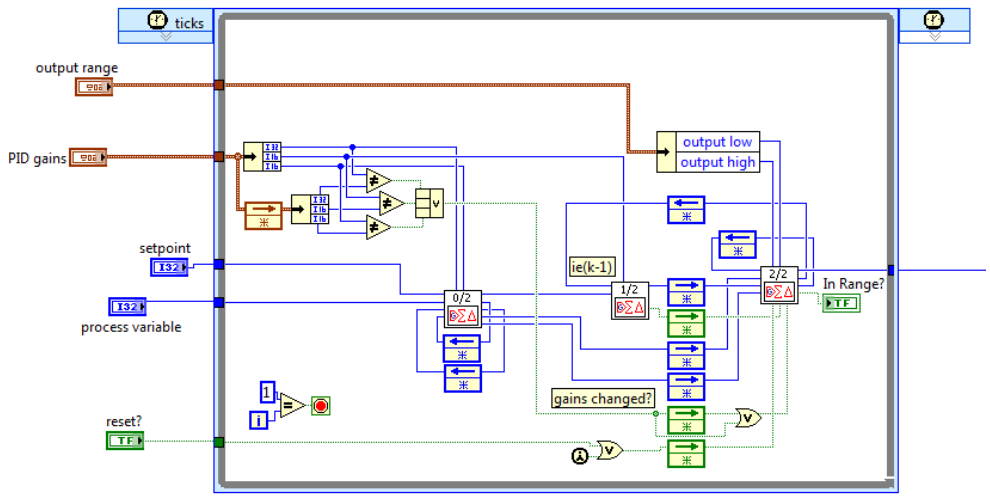


Figure 3.2: 24-bit PID algorithm.

Another important section of the FPGA VI is the communication loop, that allows the communication between the FPGA and the Real-Time target. In fact, since no direct communication between the DAQs and the Real-Time target is provided by the CompactRIO architecture, a specific routine on the FPGA target has to be written. This task is performed by the communication loop where the setpoint value is read from the numeric indicator on the PID loop and stored in a DMA FIFO channel to be read by the real-time VI. The DMA timing loop is set to $2ms$ and it can be easily changed from the real-time VI. The communication loop is shown in Fig 3.4.

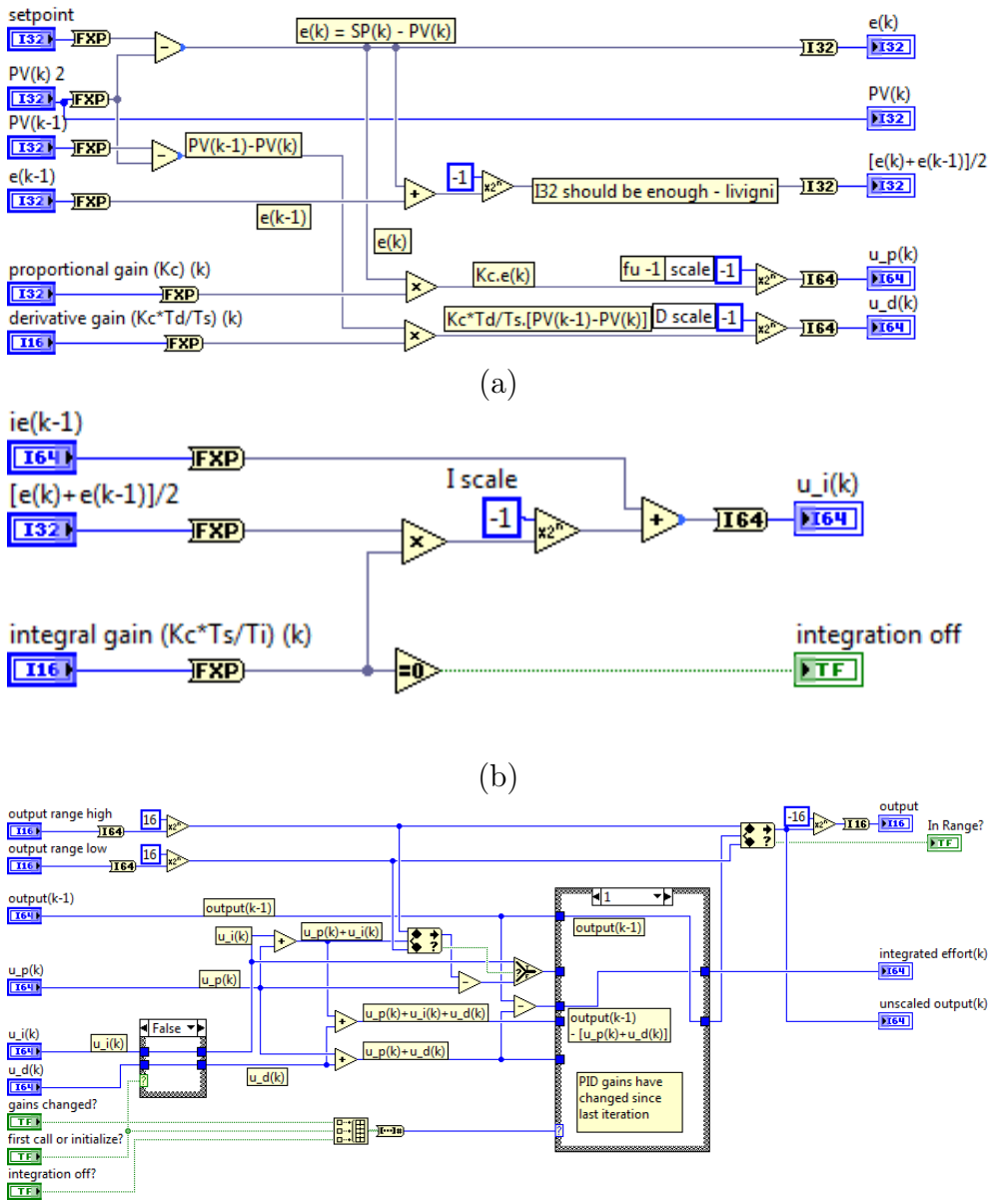


Figure 3.3: Frame 0 (a), Frame 1 (b) and Frame (c) of the 24-bit PID algorithm.

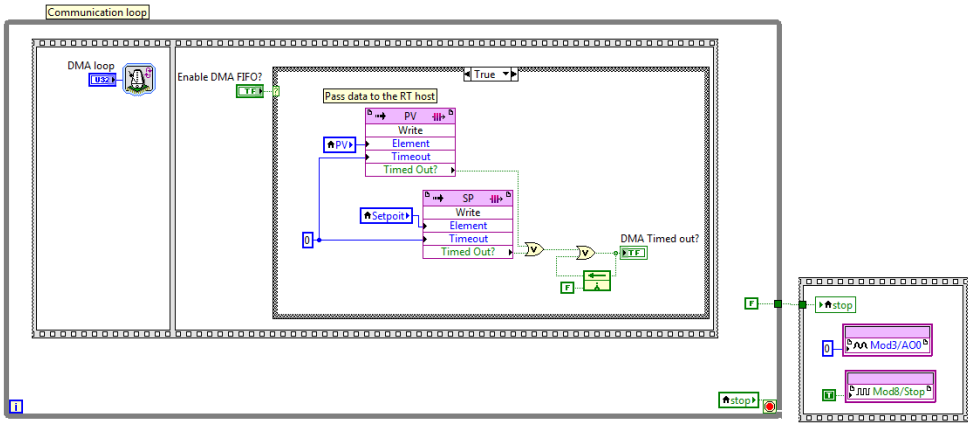


Figure 3.4: Communication loop on the FPGA targer.

The FPGA VI also implements the current limit and slow ramp down function as shown in Fig 3.5. When the current value exceeds the threshold set by the real-time target VI, the slow ramp down function is called. The result is the zero-current setting as setpoint and the slow ramping down of the current at a fixed rate. The rate for the ramping down function can be set by the host VI as well. This function can also be called by an external TTL signal applied to the channel 0 of the NI-9401 Digital Input Output module or using a control on the GUI.

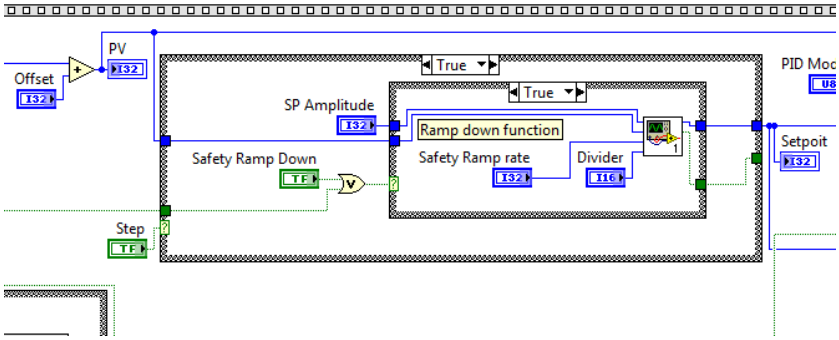


Figure 3.5: Slow Ramp Down function on the FPGA.

The output of the digital regulator can be set to zero by an external Reset/Phaseback signal or as well using a control on the GUI. The behavior of the Reset signal can be changed through the GUI: the PID algorithm can regulate the output to zero-current or the output of the regulator can be set to zero bypassing the PID algorithm. A Reset signal is usually set by the interlock logic of some test stands before power supplies are switched on. If the Reset signal is disabled, the PID regulator starts to regulate to the chosen setpoint. If an error occurs, a Reset/Phaseback signal can be used to set zero-current. A small part of this feature is shown in Fig 3.6.

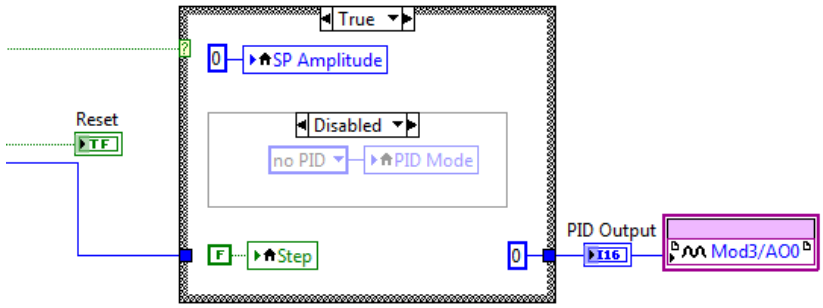


Figure 3.6: Reset/Phaseback function on the FPGA target.

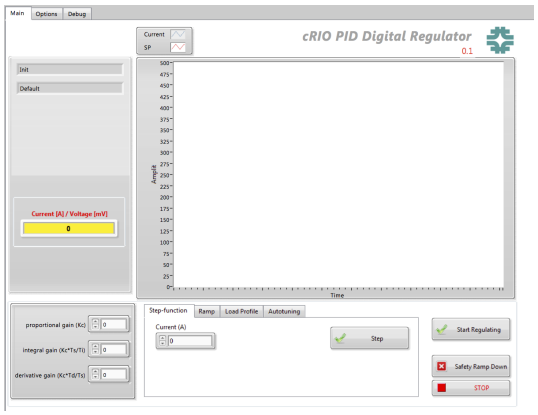
3.4 Real-Time target

The Real-Time (RT) target initializes, executes and controls the FPGA VI. The end-user can interact with the digital regulator by the RT VI front panel. The GUI is shown in Fig 3.7a. The GUI of the Digital Regulator has been designed to look like the one of the existing regulator running on an Unix machine. The current monitor frame, the actual current value, the ramp function frame (see Fig 3.8) look similar to the GUI of the existing regulator.

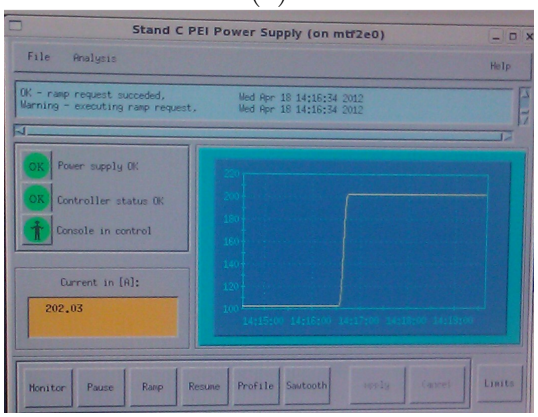
In the bottom left corner in Fig 3.7a the PID controller gain parameters can be set. The *Current [A]/Voltage [mV]* indicator shows the actual value of the current flowing through the bus. On the right, the Amplitude vs. Time chart (*Current Monitor*) of the current is shown. On the bottom center of the window, a frame with four tabs is introduced. Every tab handles a specific function provided by the digital regulator:

1. Step-function: enables the operator to perform a step function of the current. This function is useful when performing manual tuning on conventional magnets or shorted-bus test.

2. Ramp: when selecting with the two slide cursors the amplitude and the rate of the ramp, one click on the "Ramp" button will enable the Ramp function. The current in fact ramps up to the chosen value at the set rate (see Fig 3.8).

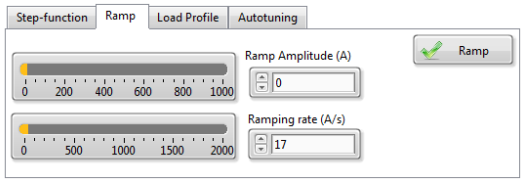


(a)

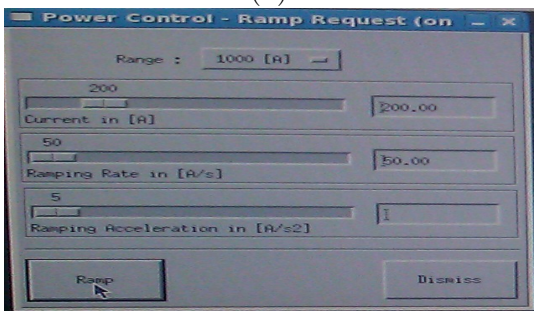


(b)

Figure 3.7: (a) GUI of the Real-time VI; (b) GUI of the existing regulator.



(a)



(b)

Figure 3.8: (a) Ramp tab on the Real-Time Vi; (b) Ramp frame on the existing regulator GUI.

3. Load Profile: a current profile is read from a file, whose path is selected by the control. “Load Profile” will load the current pattern and the power supplies will drive the load accordingly. The smaller chart in this tab shows the whole profile and a cursor follows the evolution of the profile. The main VI implementing the current profile is shown in Fig .

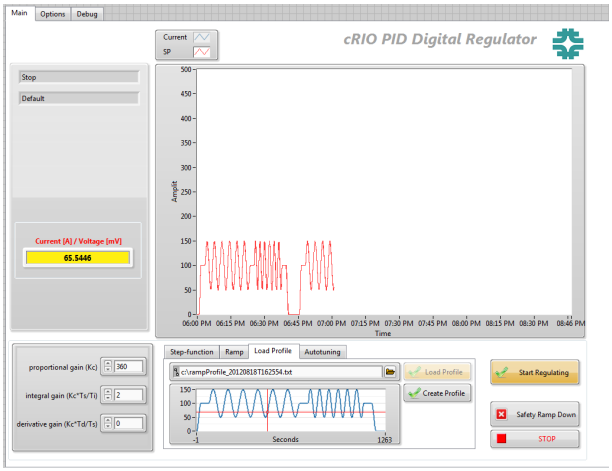


Figure 3.9: The profile loading function on the Real-time GUI.

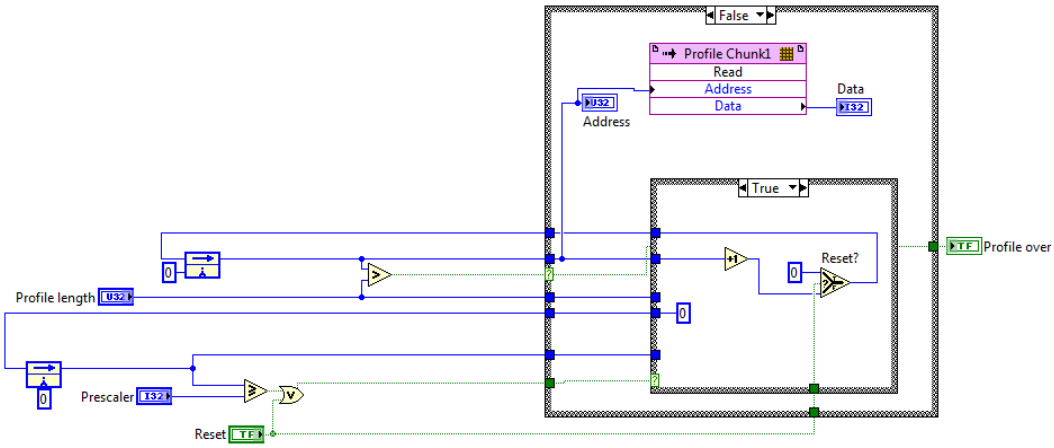


Figure 3.10: The current profile reader VI.

The last tab represents the stub for the auto-tuning algorithm further illustrated in this work.

It should be noted that if a function is selected, for instance the Ramp function, it won’t be possible to activate another function. That means that the operator should wait for the function to complete its job before switching to another function. Describing the case of the Ramp function, when the current reaches the set current it will be again

possible to use another function, such as the Profile Loading. This ensures safety during working procedures. Of course it is always possible to safely ramp down the current pressing the *Safety Ramp Down* button on the GUI.

As planned at the beginning of the present work, the real-time target VI is implemented as a state machine. This improves the reliability of the system and make easier to maintain and further edit the code. The state diagram is shown in Fig 3.11.

The RT main VI implements two parallel loops. The first loop implements the state machine itself, while the second one corresponds to the "Current Monitor and Data Logger" in the state diagram of Fig 3.11.

The State Machine provides 8 different states:

1. *Init*: this is the initial state in which many parameters are set for both the RT and FPGA VIs. The most important parameters and respectively values are shown on Tab 3.2. Many of these parameters can be changed at run-time, such as the *Current Limit Threshold* or the *Safe Ramp Down rate*. Also all the controls and indicators are initialized to the default value. The next state after the initialization is the *Ready* state.

PID loop timing	$20\mu s$
Communication loop	$1ms$
PID Gains	$K_p = 1$, $K_i = 1$, $K_d = 0$
Current Limit Threshold	∞
Integer-to-Ampere conversion factor	0,00125667
Safe Ramp Down rate	$500A/s$

Table 3.2: Initial values for some parameters of the digital regulator.

2. *Ready*: in this state the PID is working and regulating the current to zero. The Step button sets the setpoint to the chosen value and performs a step function moving to the next *Regulating* state. The Ramp button sets the Ramping Up/Down as next state, while the Load Profile button selects the Profile Loading as next state. If an error occurs the future state will be the Error one.

3. *Regulating*: here the regulator is controlling the current to the value set by the Step function or to the final value imposed by the Ramp function. The Ramp button sets the Ramping Up-Down as next state. The Safety Ramp Down button sets the Safety Ramp Down as next state. The Ready state is forced by disabling the Start Regulating button. If an error occurs the next state will be the Error state.

4. *Ramping Up/Down*: the regulator ramps the current incrementing or decrementing the value of the setpoint at the set ramping rate. After the final current is

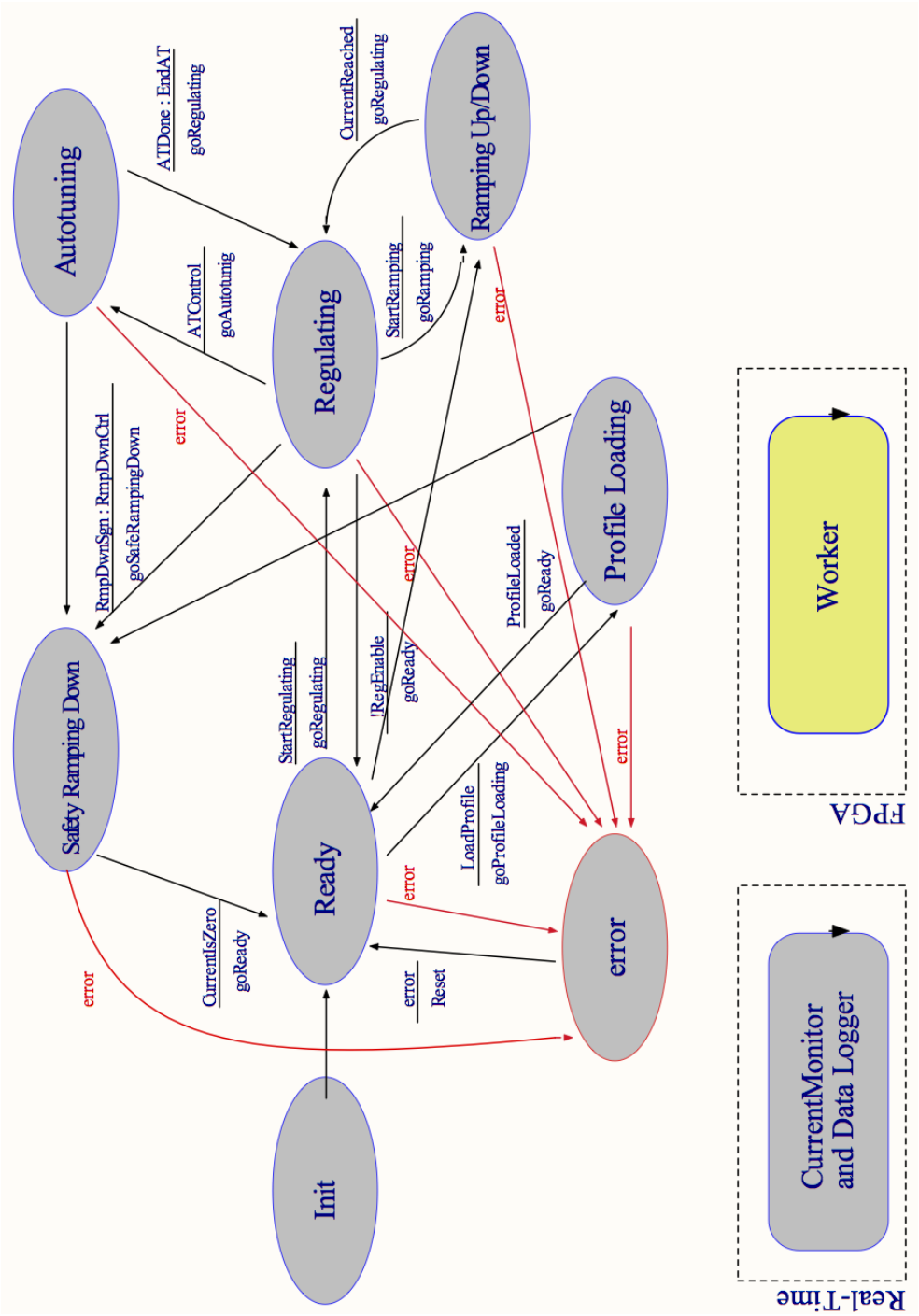


Figure 3.11: State diagram of the state machine on the RT target.

reached, the next state is the Regulating one. The Safety Ramp Down button triggers the transition towards the Safety Ramp Down state. If an error occurs the next state will be the Error state.

5. *Profile Loading*: the provided current profile is performed. Since the current profile must end with a zero value of current, the next state after the profile is fully performed is the Ready state. Also in this state, it is possible to safely ramp down the current moving to the appropriate sate. If an error occurs the next state will be the Error state.

6. *Safety Ramp Down*: the RT VI forces the FPGA VI to safely ramp down the current at the set rate. The final state is the Ready one. If an error occurs the next state will be the Error state.

7. *Error state*: depending on the occurred error the correct action is taken and the next state is the Ready one after the user's acknowledgement.

8. *Autotuning*: this state is a stub for the proposed autotuning algorithm.

It is now analyzed the Current Monitor and Data Logger loop shown in Fig 3.12. This loop handles the drawing of the current evolution and its logging for performances evaluation.

A certain number of points are read from the two DMA FIFO channels, respectively for the Process Variable and for the Setpoint. The timing of this loop is $50ms$ and this is the refresh-rate of the Current Monitor chart as well. Since the FPGA Communication loop puts 1 point for Process Variable and Setpoint into the DMA FIFO channel every $2ms$ (see again Tab 3.2), every $50ms$ the loop on the RT target takes 25 elements from the two DMA FIFO channels. The two "Invoke methods" are used to get the data from the DMA FIFOs. A numeric constant of 50 as *Number of Elements* ($>$ 25 elements) has been set to compensate an accumulation of elements inside of the DMA FIFOs. The *Timeout (ms)* is set to zero so no additional time is required if the exact number of elements are present inside the FIFOs.

Inside this loop a Data Logger is also implemented. Every $30s$ the mean, the minimum and the maximum of the current are calculated and, together with the timestamp, stored inside an array of clusters. This 30s value results from:

$$T_{loop} \cdot PV_Logging_rate = 50ms \cdot 600 = 30s$$

Data is sent on user request to the Host PC application by means of a Shared Variable hosted by the CompactRIO.

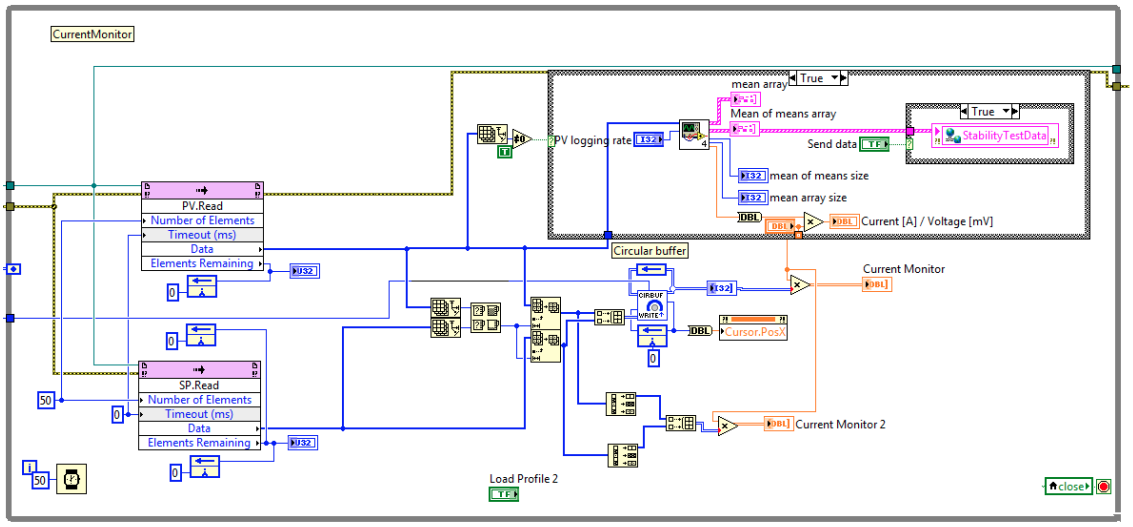


Figure 3.12: Current Monitor and Data Logger loop on the Real-Time target VI.

3.5 PC Host

The PC Host application reads and stores the data read from the Shared Variable on the CompactRIO. As already discussed in the previous section, the Shared Variable holds informations about the maximum, minimum and mean values of the current and these are shown respectively red, green and blu colored on the chart. This application is useful to evaluate the performances in stability regulation of the digital regulator and to compare these to the existing regulator ones. In fact, the difference between the maximum and the minimum value of the current (precision of the regulation) and the trend of the mean current value can be measured from the chart. The sampling time of these maximum, minimum and mean values of the current is equal to $30s$.

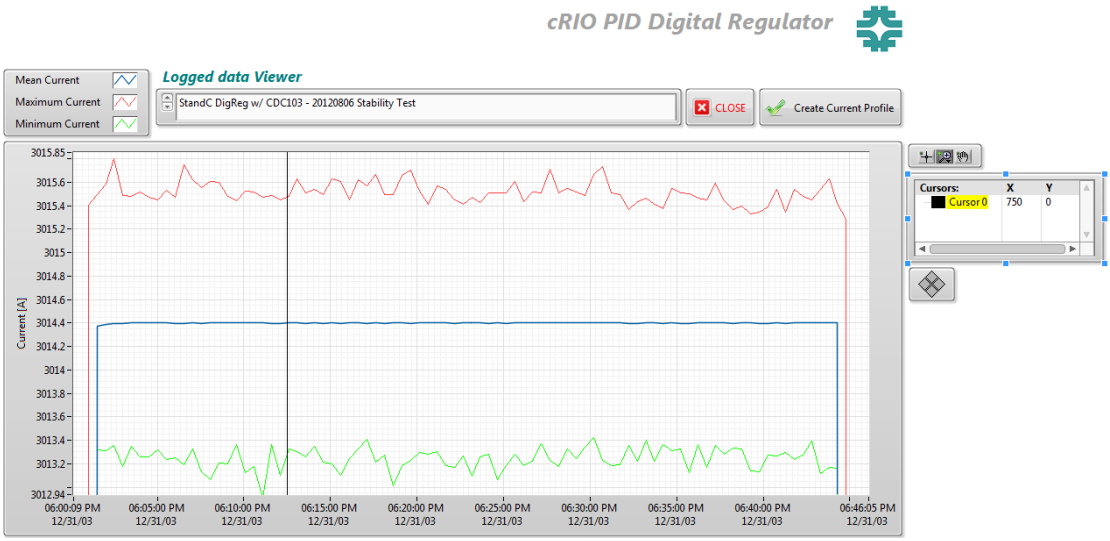
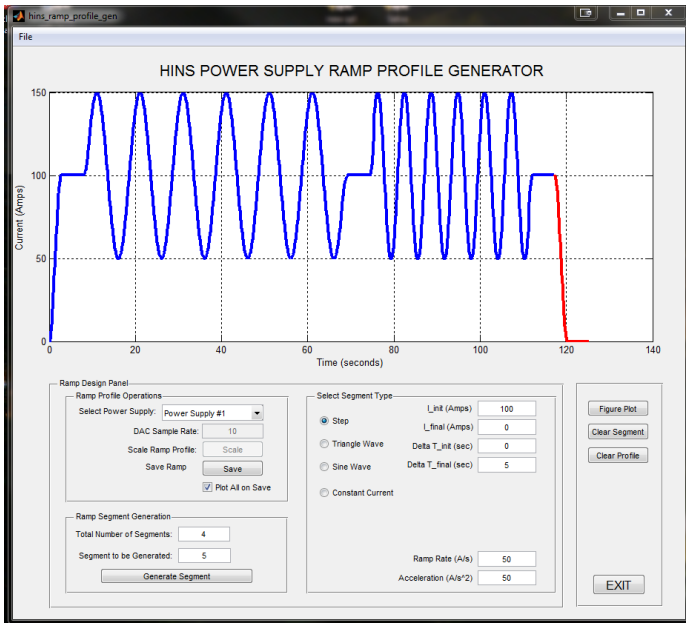


Figure 3.13: Host PC application.

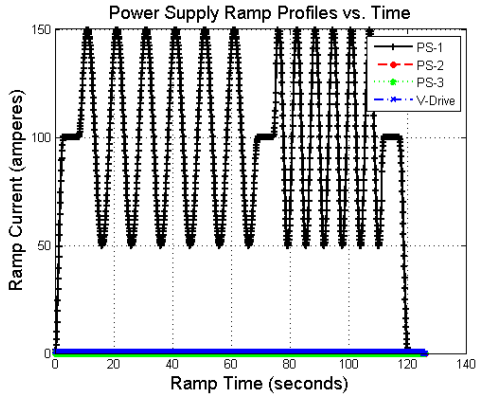
On the GUI of the application a *Create Current Profile* button is introduced, which is able to call an application used at the Magnet Test Facility for creating current profiles. These profiles can be saved and then loaded on the digital regulator. The Section 3.6 explains the current profile creation and loading.

3.6 Current Profile

The designed digital regulator allows the end-user to load a custom current profile. A click on the *Create Current Profile* button of the Host PC application will load the application that is currently used at the Fermilab Technical Division to create custom current profiles for the power supplies. This application is written in Matlab and built as a standalone executable running inside the MATLAB Compiler Runtime (MCR). The Digital regulator correctly implements the standard file format used by this application. The GUI of the utility is shown in Fig 3.14a.



(a)



(b)

Figure 3.14: (a) Ramp profile generator application; (b) The output current profile generated by the application.

The created custom profile can be saved and further loaded on the digital regulator in two different ways. The first way is to load the current profile file by means of the web application built-in on the CompactRIO. In fact it is possible to interact with the CompactRIO just writing its IP address on a standard web browser. Therefore, the IP address of the CompactRIO must be accessible by the Host PC, so both have to share the same network. Further, the Microsoft Silverlight web browser plug-in should be installed on the Host PC. A screenshot of the web application is shown in Fig 3.15.

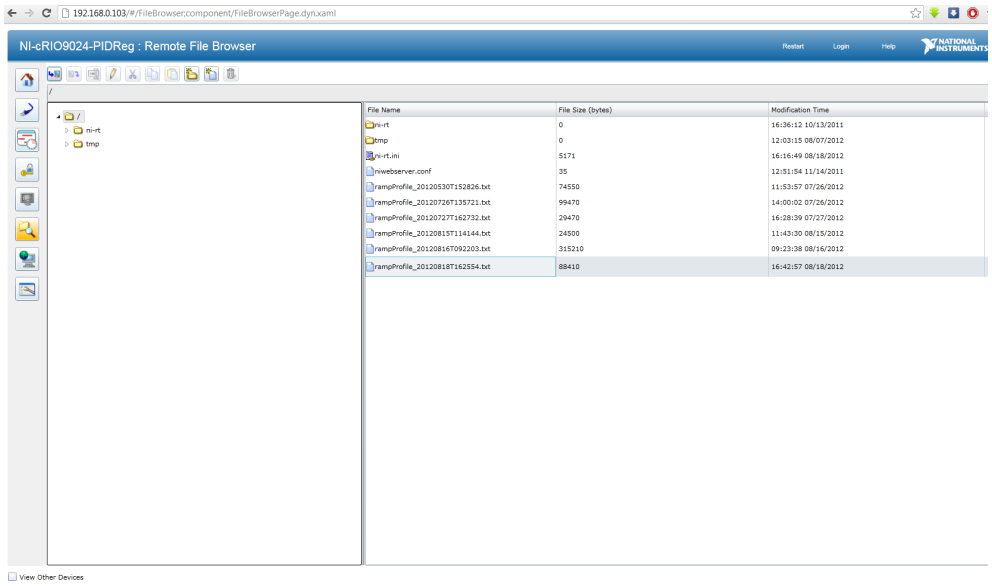
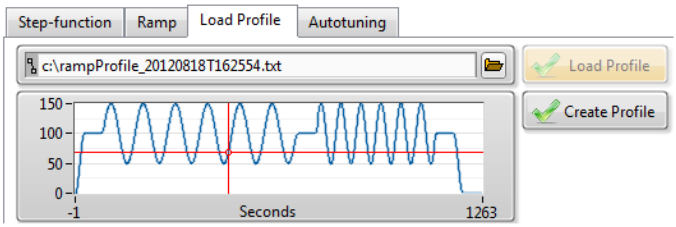


Figure 3.15: Web application of the CompactRIO running on the Host PC browser.

Uploading a file on the CompactRIO using the web interface is a straightforward operation. By setting the file local path on the Real-Time VI GUI, the application is enabled to read the current profile (see Fig 3.16).



(a)

(b)

Figure 3.16: (a) Loading a Current Profile; (b) A common USB flash drive.

The second way in order to load a current profile is even more straightforward. The cRIO-9024 Real-Time controller is featured by a host USB connector where a common USB flash drive (see Fig 3.16b) can be plugged in. Any file stored inside the USB

flash drive can be read by the RT target VI writing the filename of the current profile appended to the string "U:\" (any USB storage device attached to the CompactRIO is mapped to the U: letter).

3.7 Manual tuning procedure

Modeling the power systems architecture is quite complex. An efficient model is obtained by a system identification approach. This can be achieved combining data acquisition tools with system identification algorithms. In other words it could be possible to stimulate and acquire data from the system under test and then automatically identify a dynamic system model. In this way it could be straightforward to off-line predict the gains of the PID. Instead, an online tuning method for the PID controller has been developed in order to speed up the identification procedure. The identification procedure has been repeated for several load types, that is for several possible resistance-inductance arrangement. Load parameters (resistance and inductance value) and the corresponding PID gain values have been stored. The dependance of PID controller parameters on the load parameters has been fully characterized.

It is now described how the tuning of the PID algorithm was achieved. Referring to the flow chart shown in Fig 3.17, we start selecting the minimum values for the proportional and integral gains, $K_p = 1$ and $K_i = 1$. The next step is to catch the response of the system to a known function. If a conventional magnet is connected to the power supply, the most suitable function is the step function (usually 100A). The system response is stored and analyzed in order to evaluate the PID performances in terms of steady-state error, rise-time, overshoot, settling-time, oscillations. At first, since the gain is still low neither overshoots nor oscillations are expected, while the rise-time and the steady-state error are expected to be too high. To reduce the steady-state error and the rise-time as well, the proportional gain has to be increased. This procedure is repeated until the steady-state error is as low as possible. Then the rise-time has to be minimized. To decrease the rise-time, the integral gain K_i should be increased until good performances are achieved without overshoots, oscillations or huge settling-time. In case overshoots or oscillations are found, K_i should be reduced. If some overshoot is still present, K_d should be used to reduce it. The contribute of K_d helped to reduce overshoots and oscillations when performing initial tests on the KEPCO Bipolar Operational Power Supply/Amplifier (BOP), but so far haven't been necessary on CPS3 and Stand C with the tested type of loads. The effects of each term of PID controllers on closed-loop system have been previously summarized in Tab 3.1.

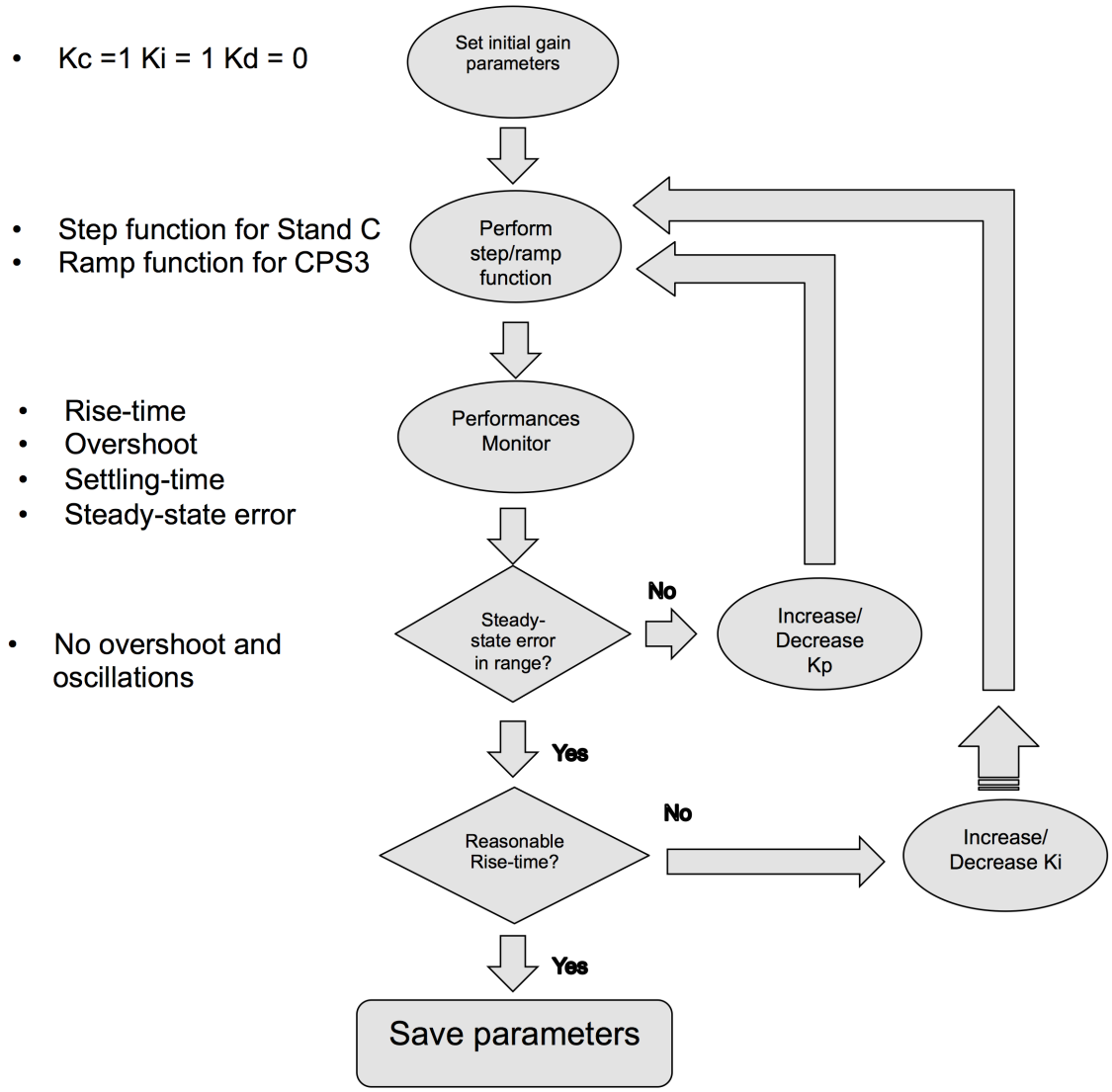


Figure 3.17: Flow chart of the manual tuning approach.

3.8 Auto-tuning

An automatic tuning procedure of the PID parameters aims at saving human efforts during the setup procedure. No matter what magnet characteristics are, all parameters will be automatically tuned. LabVIEW itself provides some VIs that should be able to automatically find good parameters for the regulator. Unfortunately many tests showed that these algorithms are not suitable for the proposed application. In fact the parameters found by the autotuning VIs are always very far from the one found by manual tuning and of course not appropriate to regulate the system. In this section

an auto-tuning algorithm which is suitable for magnet tests with high-current power supplies is proposed. The flow chart is shown in Fig 3.19. It should be immediately noticed that is quite similar to the one proposed for the manual tuning approach (see Fig 3.17) for the manual tuning approach. In fact, the manual tuning algorithm proved to be quite reliable and easy to set up. That's why this algorithm has been chosen to further implement the auto-tuning capability of the digital regulator.

Unlike in the manual tuning approach, the PID gains corresponding to a previously tested magnet could be set as a starting point for a new identification procedure. If the inductance and resistance of the magnet are known, it could be possible to calculate the ideal settings for the PID and set these values as a starting point for a new auto-tuning procedure.

At the end of the algorithm, when gains are found, the algorithm will ask the operator to accept or discard the parameters and, in the second case, it will switch to manual tuning. The parameters that has been found will be saved to be later reviewed or recalled. In Fig 3.18 is shown the front panel of the VI which analyzes the response of the system in order to evaluate the PID performances in terms of steady-state error, rise-time, overshoot, settling-time, oscillations. This VI will be used to implement the proposed auto-tuning algorithm.

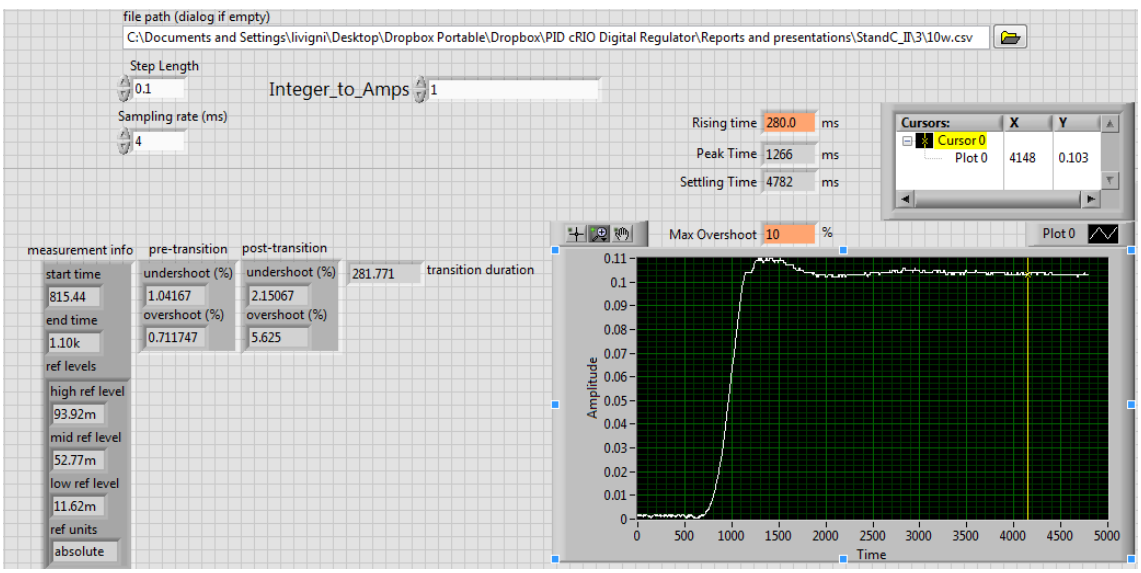


Figure 3.18: The VI which analyzes the system response to a step function.

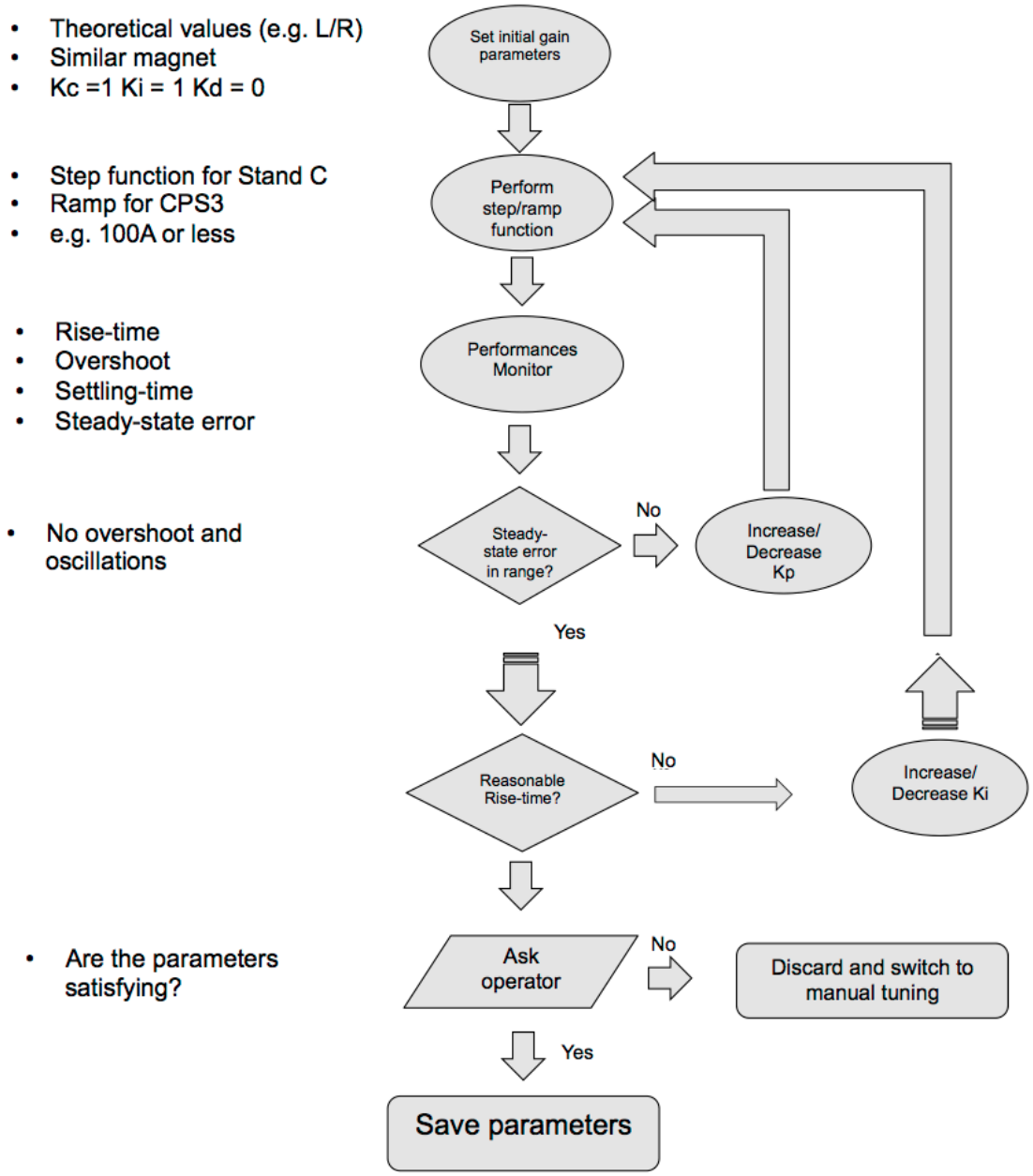


Figure 3.19: Flow chart of the auto-tuning approach.

Chapter 4

Evaluating system performances

Introduction

In this chapter some of the tests performed on Stand C and CPS3 will be discussed. Usually the tests have been run using first the existing regulator and then with the digital regulator. Whenever possible, the tests with both regulators have been consecutively performed in order to have similar environmental conditions and consistent results. Performances are evaluated taking in account rise-time, overshoot, stability in current regulation, settling-time. Usually overshoots are not acceptable when testing magnets. For instance, when performing tests on a superconducting magnet, an overshoot could induce a quench on the magnet. For this reason, overshoots may be avoided. During the manual tuning procedures, PID gains that provided good stability in regulation over other gains with better rise-time have been chosen.

After the manual tuning procedure, the current have been kept at the same value for a fixed time. Usually this time interval has been equal to 30 minutes, where every point for the maximum, minimum and current values are sampled every 30 seconds. This data is stored by the real-time target VI on the shared variable hosted by the CompactRIO and it is possible to monitor this data directly from the Host PC application.

The comparison of the performances for the current loop stability have been performed by calculating the difference between the maximum and the minimum current values (precision of the regulation) and doing the same for the maximum and the minimum current mean value (stability of current regulation). The same test has been performed with both the digital regulator and the existing analog one. The current setpoint during these tests depends on the available power supplies and the load. In case of the Stand C with the shorted-bus the current can be 1kA, while with magnets the value does depend on the magnet rated current. In case of the CPS3 with the shorted-bus the current is set to 3kA. The results are discussed in the following sections.

4.1 Stand C

The results of two tests performed on the Stand C are here reported. The former is a shorted-bus test, the latter uses the dipole CDC103.

4.1.1 Measurements and experimental setup

A schematic block diagram of the experimental setup is shown in Fig 4.1. One channel of the analog input module NI-9239, that is attached to the CompactRIO, is connected to the output of the HITEC DC Current Transformer (DCCT), which provides a voltage signal proportional to the current flowing through the bus. This feedback signal for the regulator is the process variable (PV). An ad-hoc adapter was realized to connect the DCCT to the DAQ.

The calculated output of the PID algorithm is driven out by the first channel of the analog output module NI-9269 and connected to the input of the voltage regulator of the master PEI power supply. This connection is shown in Fig 4.2b. When the existing regulator is used, the master voltage regulator is connected to the Power Supply Controller module and the bottom green coax cable unplugged. The analog current PI regulator module is bypassed, being set in voltage mode moving the switch shown in Fig 4.2a. The master voltage regulator drives both master and slave PEI power supplies.

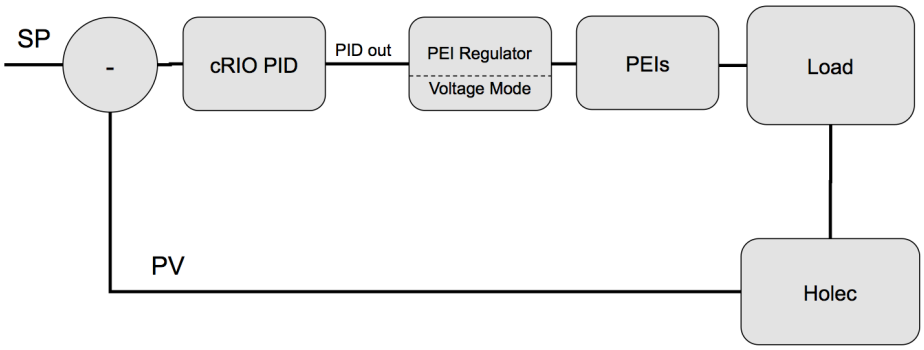
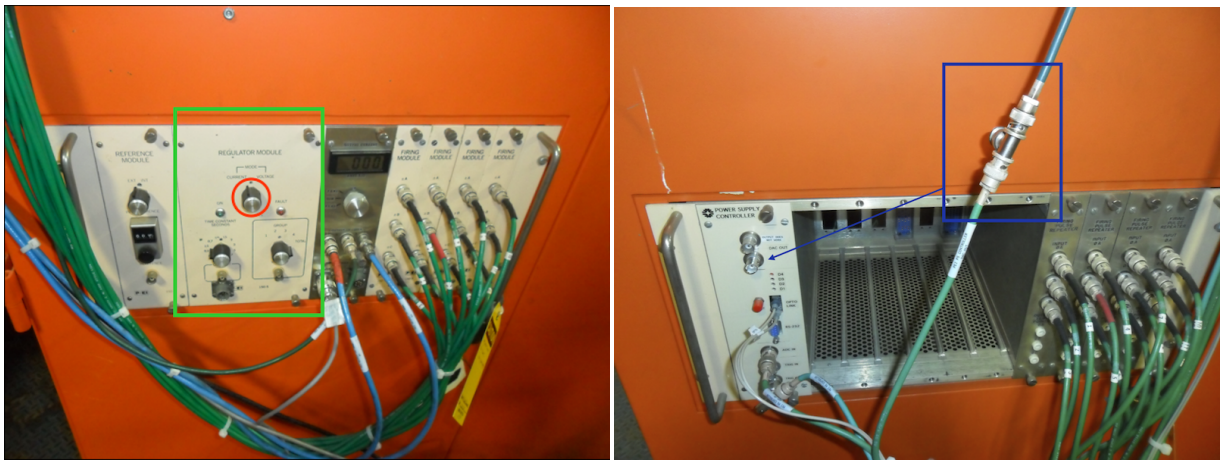


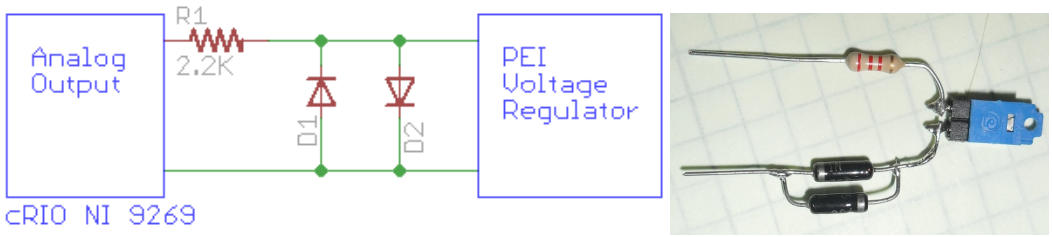
Figure 4.1: Block diagram of the testing setup on Stand C.



(a) (b)

Figure 4.2: (a) Current Regulator Module on the master power supply of the Stand C; (b) PID output coax cable connected to the input of the master voltage regulator.

In parallel with the analog output a simple circuit with a resistor and two diodes in antiparallel configuration is placed as shown in Fig 4.3a and 4.3b. A jumper will disable this passive network. When the jumper is shorted the diodes limit the output of the PID to the value 0.6 V that means a current of approximately 600 A. In fact, usually this current limitation has been enabled mainly during the very first tests with the digital regulator, in order to avoid to overcome the maximum current for the magnet under test (usually 700-1100A). The jumper is then opened after checking that the regulator is working as expected.



(a) (b)

Figure 4.3: (a) Schematic of the current limit circuit; (b) the circuit itself.

Before starting a test is necessary to remove the locks from the switches (as show in Fig 4.4a and 4.4b), as provided for in the Fermilab Lockout/Tagout Program (LOTO), and then power on first the master PEI and then the slave. The light indicator automatically switches on. Another indicator is present near the magnet for the safety of the operator.

(a) (b)

Figure 4.4: (a) Locked and unlocked (b) PEI power supply of the Stand C.

Just before starting the test, the interlock module should be reset and the operator should check wether or not any LED indicators are off. The interlock module is shown on the right in Fig 4.5. After that, it is possible to press the Reset button on the *Dual Power Supply Controller* (on the left in Fig 4.5) and finally the D.C. ON button. The red D.C. OFF button switches off the power supplies.

Figure 4.5: Dual Power Supply Controller and Interlock module of the Stand C.

4.1.2 Shorted-bus test

In this test the current flows on the shorted-bus. The shorted-bus test represents the worst-case since an extremely low inductance and resistance values are accounted for.

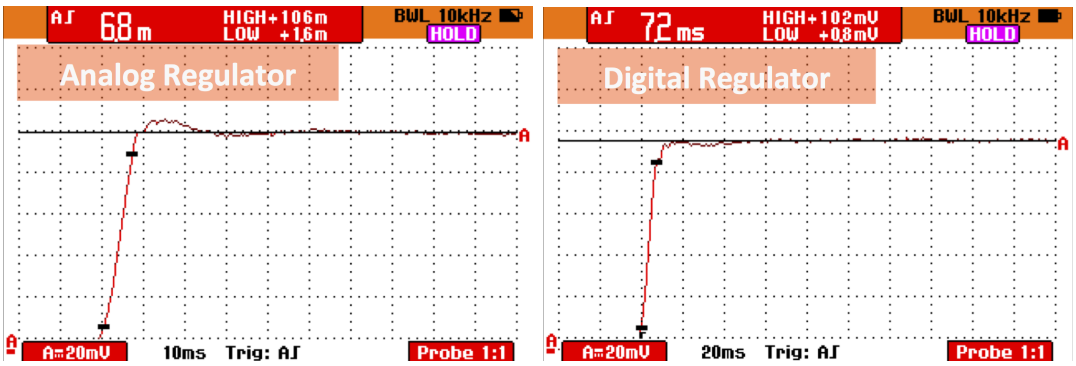
Here the results achieved by using the existing analog regulator and the proposed digital regulator are compared and discussed.

The first part of the test has been performed with the existing regulator. The switch on the current regulator module is set in *Current Mode* and the time-constant selector is set to its lowest value of 0.1s. The DAC of the Power Supply Controller module drives the master voltage regulator. Here we interact with the power supplies by using the Power Supply GUI running on the Unix machine. A current of 1kA has been selected and kept constant for 30 minutes.

In the second part of the test, the digital regulator has been used. The manual tuning of the PID resulted in the parameters: $K_p = 9000$, $K_i = 1$, $K_d = 0$. Again, a current of 1kA has been chosen and kept for 30 minutes.

For both regulators, the response to a 100A step function has been analyzed by using a portable scope, as shown in Fig 4.6a and 4.6b. The rise-time is quite the same for both regulators. Yet, the analog regulator response exhibits a significant overshoot. The settling-time is 20ms less using the digital regulator.

Looking at the maximum, minimum and mean current trends in Fig 4.7a it should be noted that the precision in regulation is comparable (below 2 A), while the stability is far different. As show in Fig 4.7b, the mean value of the current for the analog regulator falls within the range 997.922 ÷ 997.978A that means an excursion of $56mA$ and 56ppm. On the contrary, for the digital regulator the mean value of the current is 1004.796 ÷ 1004.800 that is $4\,mA$ and so $4\,ppm$. The proposed digital regulator is 14 times better when regulating the current compared to the analog regulator. The results are summarized in Tab 4.1.



(a) (b)

Figure 4.6: Response at a 100A step function for the (a) analog and (b) digital regulator for the shorted-bus test on the Stand C.

Figure 4.7: (a) Maximum, minimum and mean value of the current on a shorted-bus test using analog and digital regulator on Stand C; (b) Zoom on the mean value of the current.

	Analog ($T_c = 0.1s$)	Digital ($K_p = 9000$, $K_i = 1$, $K_d = 0$)
rise-time	6.8ms	7.2ms
settling-time	80ms	60ms
overshoot	6%	-
stability (at 1kA)	56ppm	4ppm

Table 4.1: Performances comparison of the two regulators on a shorted-bus test with the Stand C.

4.1.3 Magnet CDC103

For this test the magnet CDC103 shown in Fig 4.8a is used as load. The CDC is a series of dipole magnets realized by Fermilab. Their characteristics are reported in Tab 4.2. In particular the CDC103 features an inductance of 18.192 mH at 100 Hz and a resistance of 47.17 $m\Omega$ as shown in Fig 4.8b.

(a) (b)

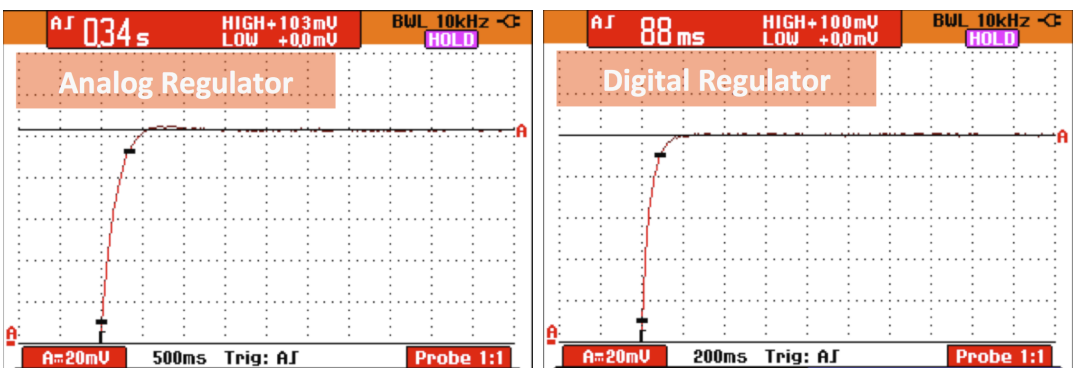
Figure 4.8: (a) CDC103 dipole magnet and (b) its characteristics.

Magnet Builder	Fermilab
Magnet Weight	6100 lbs (2767 Kg)
Magnet Length	59.937 in (1,52 m)
Magnet Type (# of poles)	Dipole (2)
Magnet Inductance @ 1kHz)	20.00 to 24.44 mH
Q @ 1kHz	3.8 to 4.6
Magnet Inductance @ 100Hz	27.74 to 33.9 mH
Q @ 100Hz	6.9 to 8.5
Magnet Resistance	44.08 to 53.58 $m\Omega$
Maximum Voltage (Hipot to core)	1500 V
Maximum Hi pot Leakage Current	5 μA
Maximum current	1230 A
Waveform Description (DC, bi-polar, or pulse@frequency)	DC

Table 4.2: Characteristics of the CDC magnet series.

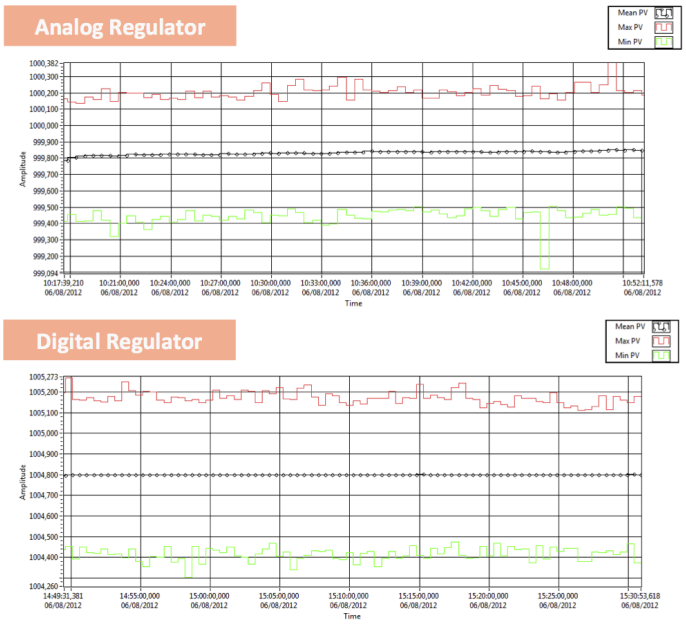
The following PID gains are obtained by the manual tuning algorithm: $K_p = 58000$, $K_i = 4$, $K_d = 0$. The response to a 100A step-function is shown in Fig 4.9a and 4.9b for both the analog and the digital regulator. The rise-time of 88ms achieved by the digital regulator outperforms the one of the analog regulator. It should be also noticed the presence of an overshoot on the response of the analog regulator. The settling-time of 300ms achieved by the digital regulator is 5 times better than the one achieved by the analog regulator.

The precision in regulation for both regulators is also in this case comparable (below 1.6A). Control accuracy is far better with the digital regulator: $999.815 \div 999.855$ that means $40mA$ and so 40ppm. Comparing this result to the case of the digital regulator - $1004.797 \div 1004.801 = 4mA$ that means 4ppm - the performances of the proposed regulator are 10 times better. The results are summarized in Tab 4.3.

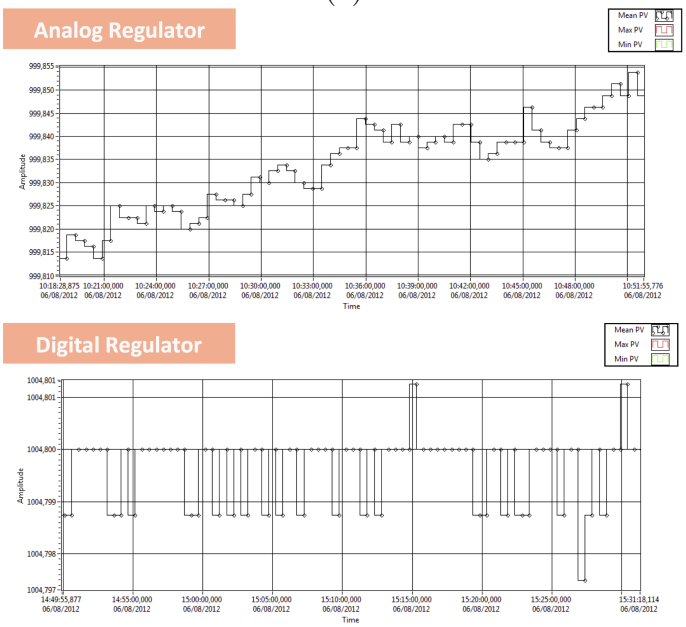


(a) (b)

Figure 4.9: Response at a 100A step function for the (a) analog and (b) digital regulator with CDC103 on Stand C.



(a)



(b)

Figure 4.10: (a) Maximum, minimum and mean value of the current during the test with the CDC magnet, using the analog and digital regulator on Stand C; (b) Zoom on the mean value of the current.

	Analog ($T_c = 0.1s$)	Digital ($K_p = 58000$, $K_i = 4$, $K_d = 0$)
rise-time	340ms	88ms
settling-time	1.5s	300ms
overshoot	3%	-
stability (at 1kA)	40ppm	4ppm

Table 4.3: Performances comparison of the two regulators on a shorted-bus test with the Stand C.

4.2 Vertical Magnet Test Facility

The results of the shorted-bus test performed on the VMTF are here reported. So far the tight schedule on this Stand didn't allow to test the digital regulator on a superconductive magnet. In fact here superconductive magnets come only for a short time interval to be tested. Most of the time is needed to cool down the magnet and, after the test is performed, warm it up. Some tests with a superconductive will performed in the near future.

4.2.1 Measurements and experimental setup

A schematic block diagram of the experimental setup is shown in Fig 4.1. As discussed before, the VMTF uses 6 HITEC current transformers and these signals are summed by the Summation unit in order to have a unique 0-10V feedback signal for the regulator. The output of the Summation unit module is connected to the first channel of the analog input module NI-9239 on the CompactRIO.

The calculated output of the PID algorithm is driven out by the first channel of the analog output module NI-9269 and connected to the input of the Fast Trip Box and from here to the master voltage regulator. The Fault-ground Detection Module (FDM) can set the *Ramp down* and trip the current to zero using the built-in safe ramp down feature of the digital regulator. The external slow ramp down module is used when the existing regulator is selected, while with the digital regulator the module has been bypassed.

An adapter had to be realized in order to connect the NI-9401 Digital I/O module to the fault-ground detection module. In this way if a fault-ground or a quench (if a superconducting magnet is being tested) is detected, the external logic will call the safe ramp down function provided by the digital regulator. Another adapter was realized to connect the output of the summing unit to the analog input of the CompactRIO.

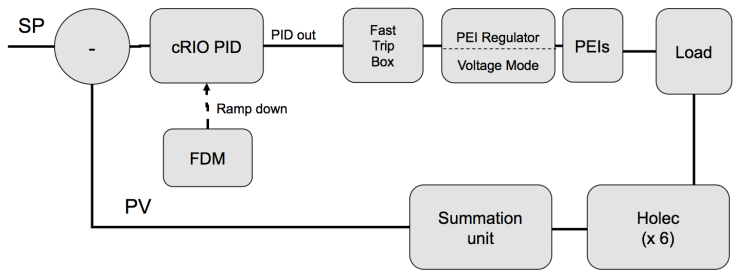


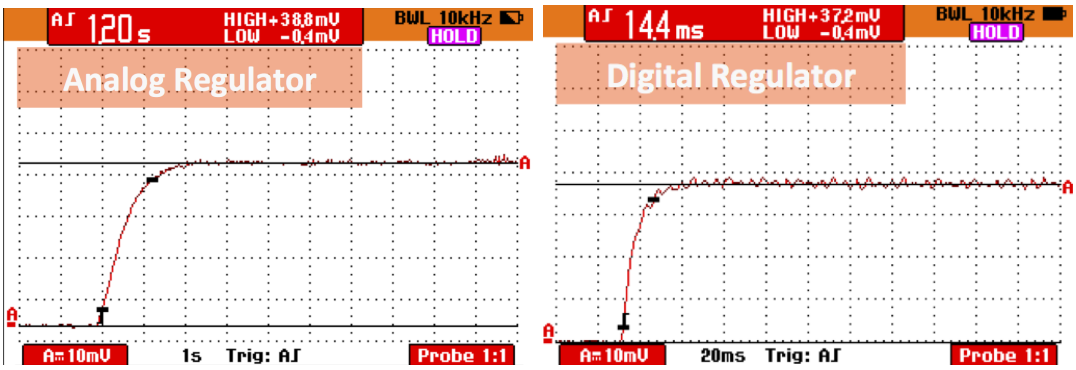
Figure 4.11: Block diagram of the testing setup on VMTF.

4.2.2 Shorted-bus test

In this test the current flows on the shorted-bus, so no load is connected. This results in a stress test for the regulator, since it has to regulate the current in the worst condition that is a load featured by negligible inductance and very low resistance.

The time-constant selector of the existing regulator was set to 0.1s and a 30 minutes test was performed with a current of 3000A. The same was performed with the digital regulator using the parameters $K_p = 30000$, $K_i = 16$, $K_d = 0$ which resulted by the manual tuning process.

For both regulators, the response to a 100A step function has been analyzed by using a portable scope, as shown in Fig 4.12a and 4.12b. With the existing regulator rise-time is 1.20s and settling-time is 3s. On the contrary, with the digital regulator rise-time and settling-time are smaller, 14.4ms and 60ms respectively.



(a) (b)

Figure 4.12: Response at a 100A step function for the (a) analog and (b) digital regulator on VMTF.

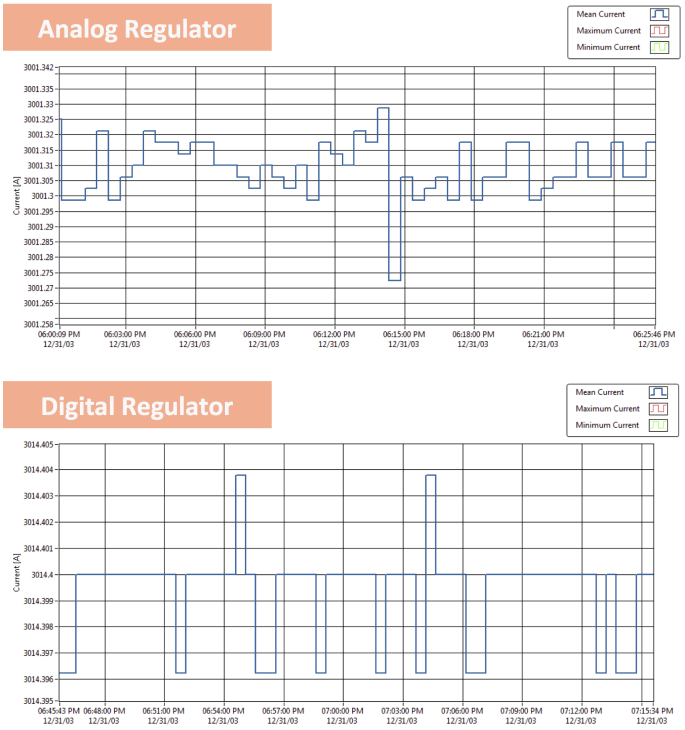
The stability tests performed on VMTF are shown in Fig 4.13a and 4.13b. Here the existing regulator achieved a precision in regulation (difference between the maximum

and minimum value of the current) equal to 22 A, while it's better, being equal to 13 A, with the proposed digital regulator. Control accuracy is $3001.272 \div 3001.332 = 60mA$ that means 20ppm, while with the digital regulator is $3014.396 \div 3014.404 = 8mA$ that means less than 3ppm. The results are summarized in Tab 4.4.

	Analog ($T_c = 0.1s$)	Digital ($K_p = 30000$, $K_i = 16$, $K_d = 0$)
rise-time	1.20s	14.4ms
settling-time	3s	60ms
overshoot	-	-
stability (at 1kA)	20ppm	3ppm

Table 4.4: Performances comparison of the two regulators on a shorted-bus test with the Stand C.

(a)



(b)

Figure 4.13: (a) Maximum, minimum and mean value of the current on a shorted-bus test using analog and digital regulator on CPS3; (b) Zoom on the mean value of the current.

4.3 Conclusions and future developments

The design of a digital PID regulator for DC power systems used to test conventional and superconducting magnets has been described. The performances of the designed digital regulator meet all assigned requirements, as shown by the tests performed on the VMTF as well as on the Stand C. This result has been achieved by implementing a full 24-bit PID algorithm running on the FPGA target of the CompactRIO. In particular a control accuracy less than 4 ppm and a current loop stability up to 14 times better than the existing regulator is obtained. While a manual tuning approach was successfully used during all the tests, a promising automated tuning algorithm was also proposed and will be tested in the near future.

This project has room for improvements and the "digital approach" enables significant further developments. For instance, it can be possible to implement the voltage regulator on the FPGA as well, avoiding the one hosted by the master PEI power supply of both VMTF and Stand C. In this way a more effective control on the suppression of the ripple of the current can be achieved as well as noise rejection.

It could also be implemented on the FPGA a method to provide protection for not even current sharing and for negative current for each of the bussed power supplies. Using further analog input modules, the summation unit on the VMTF could be also replaced, performing the current summation on the CompactRIO itself.

Furthermore, a fiber optic current distribution system can be easily implemented on the same hardware, replacing the existing VME modules described in Section 1.4.4. The fiber optic current transmitter will be hosted by the proposed digital regulator device, while fiber optic current receivers will be implemented by other CompactRIOs. If no other tasks should be performed by these devices, entry-level CompactRIO hardware to implement every receiver can be used to save costs. The transmitter and the receiver cRIO will be featured by two front-end, respectively a digital-to-optic front-end and a optic-to-digital one.

Also, the PC Host VI could be extended in order to act as main GUI of the Digital Regulator, instead of using the CompactRIO VI front panel.

Appendix A

Schematics

All the schematics reported in this Appendix are property of Fermilab.

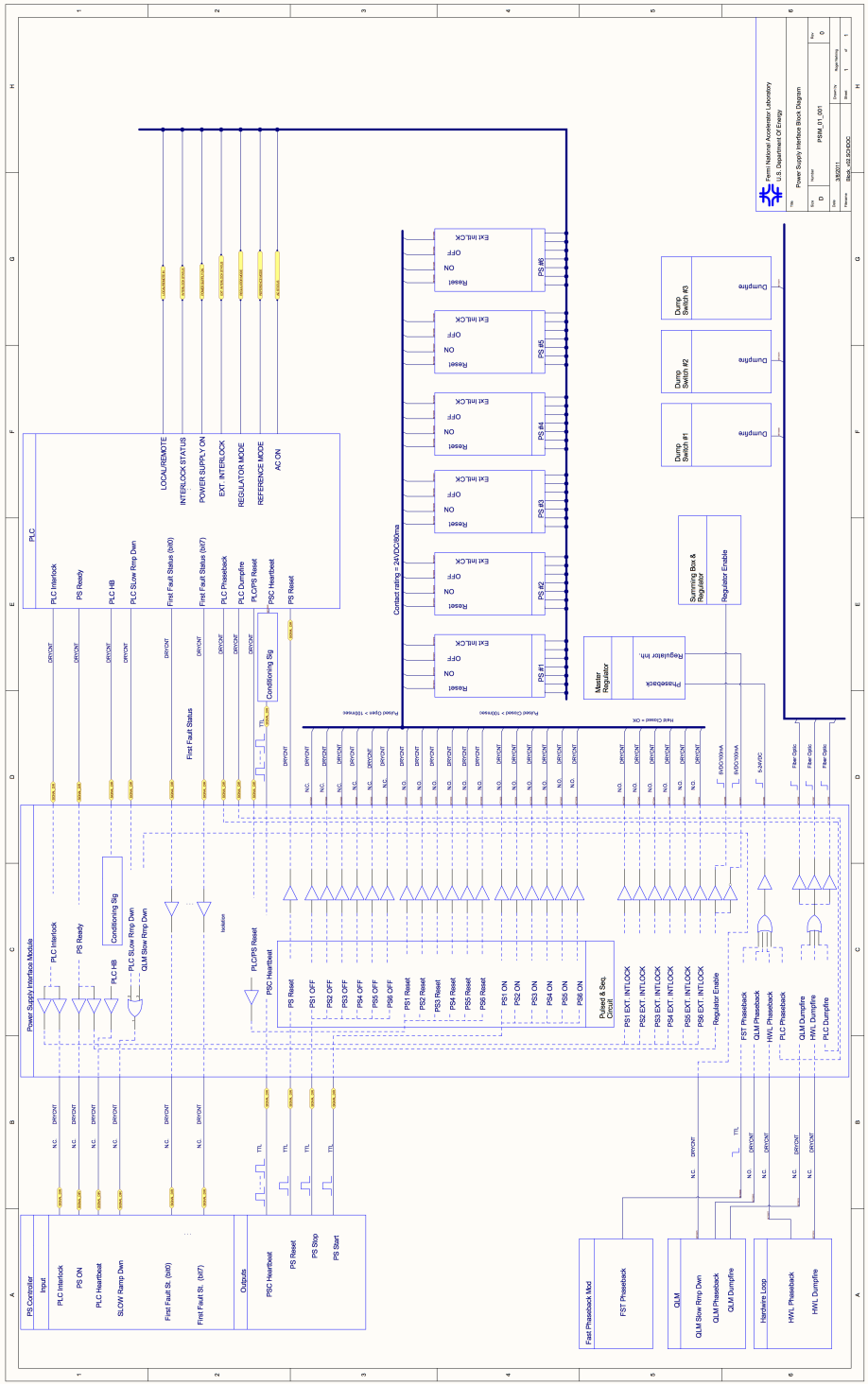


Figure A.1: Power supply interface block diagram.

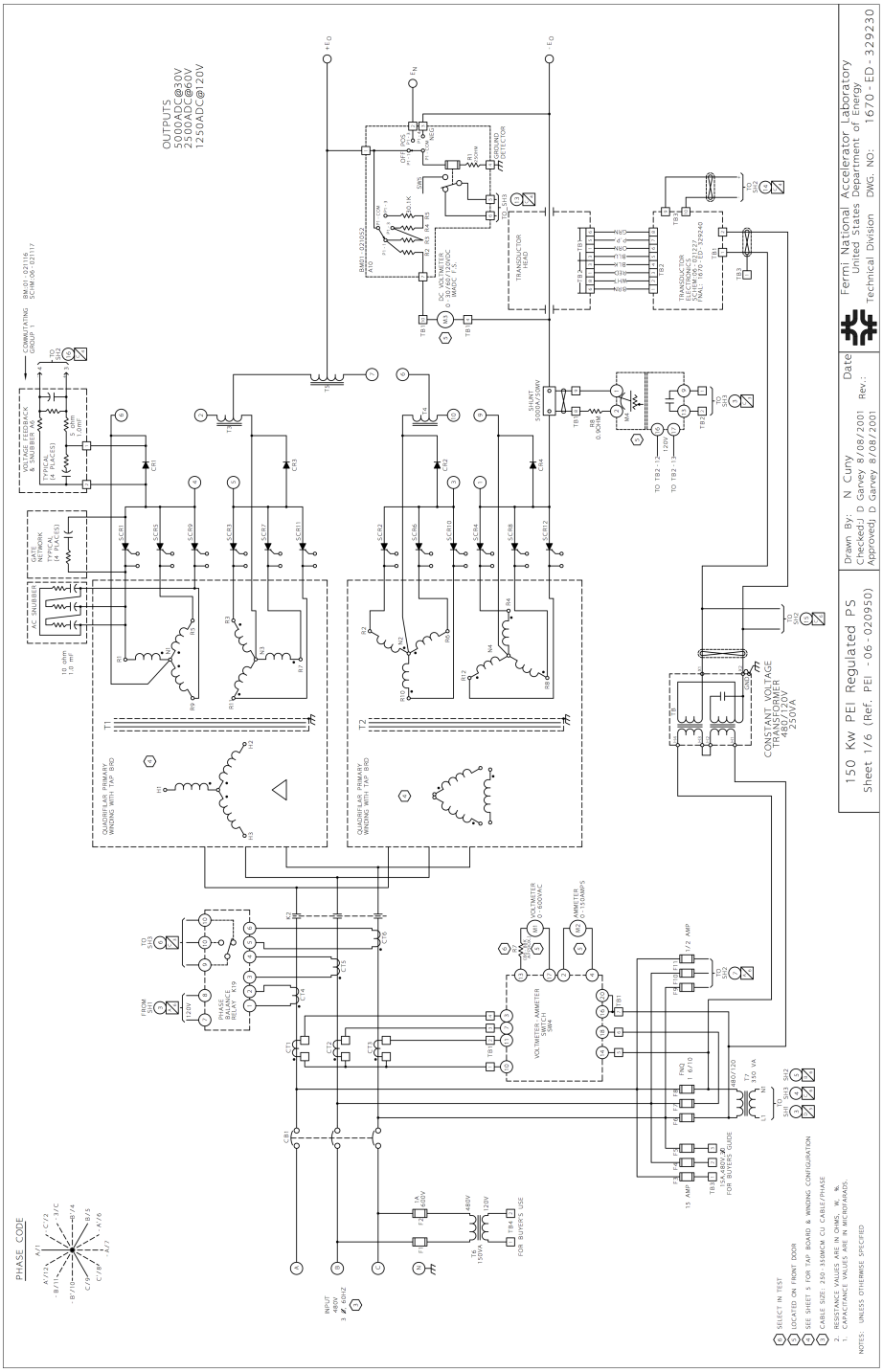


Figure A.2: PEI power supply schematic.

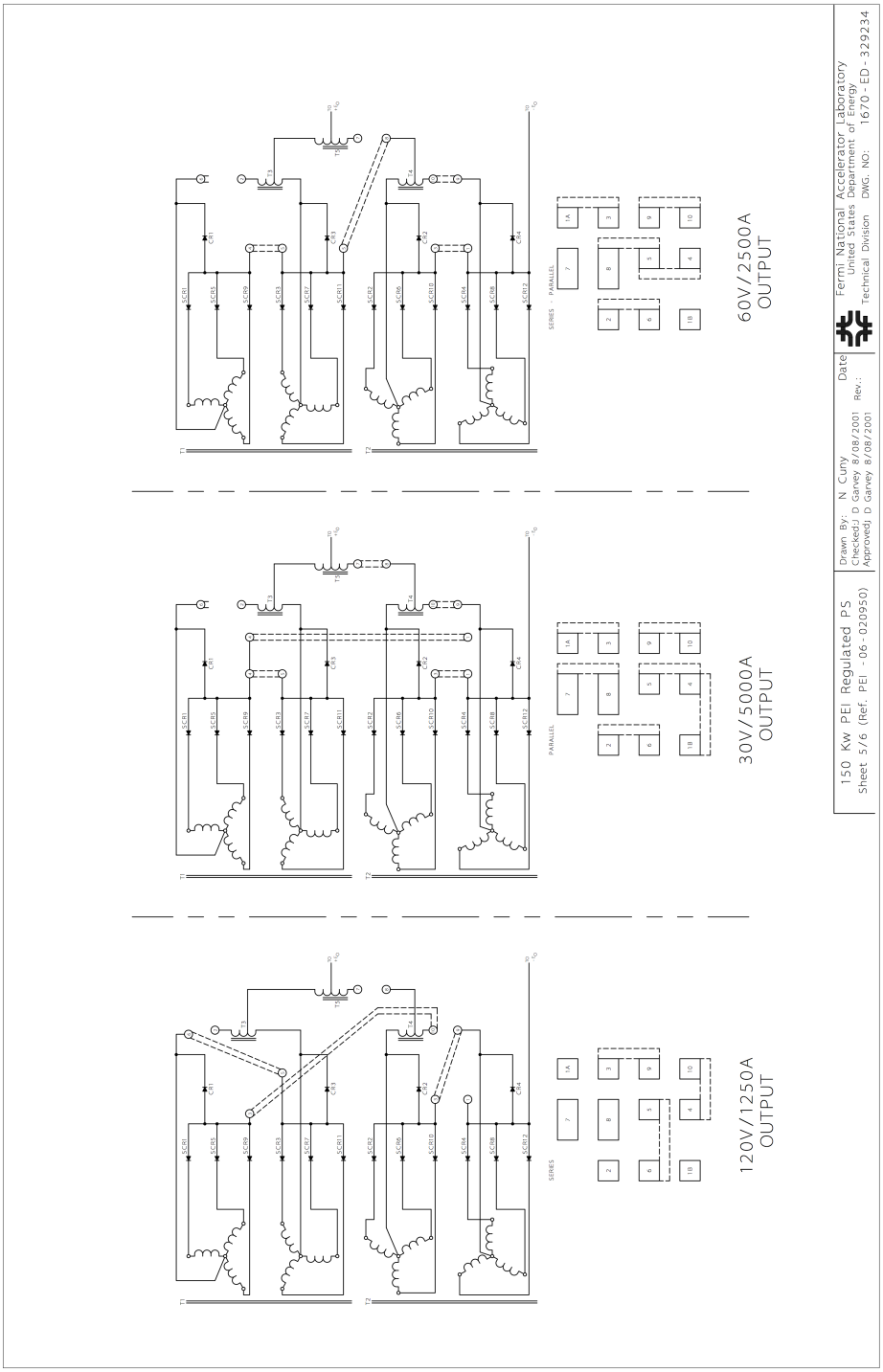


Figure A.3: PEI power supply transformer taps.

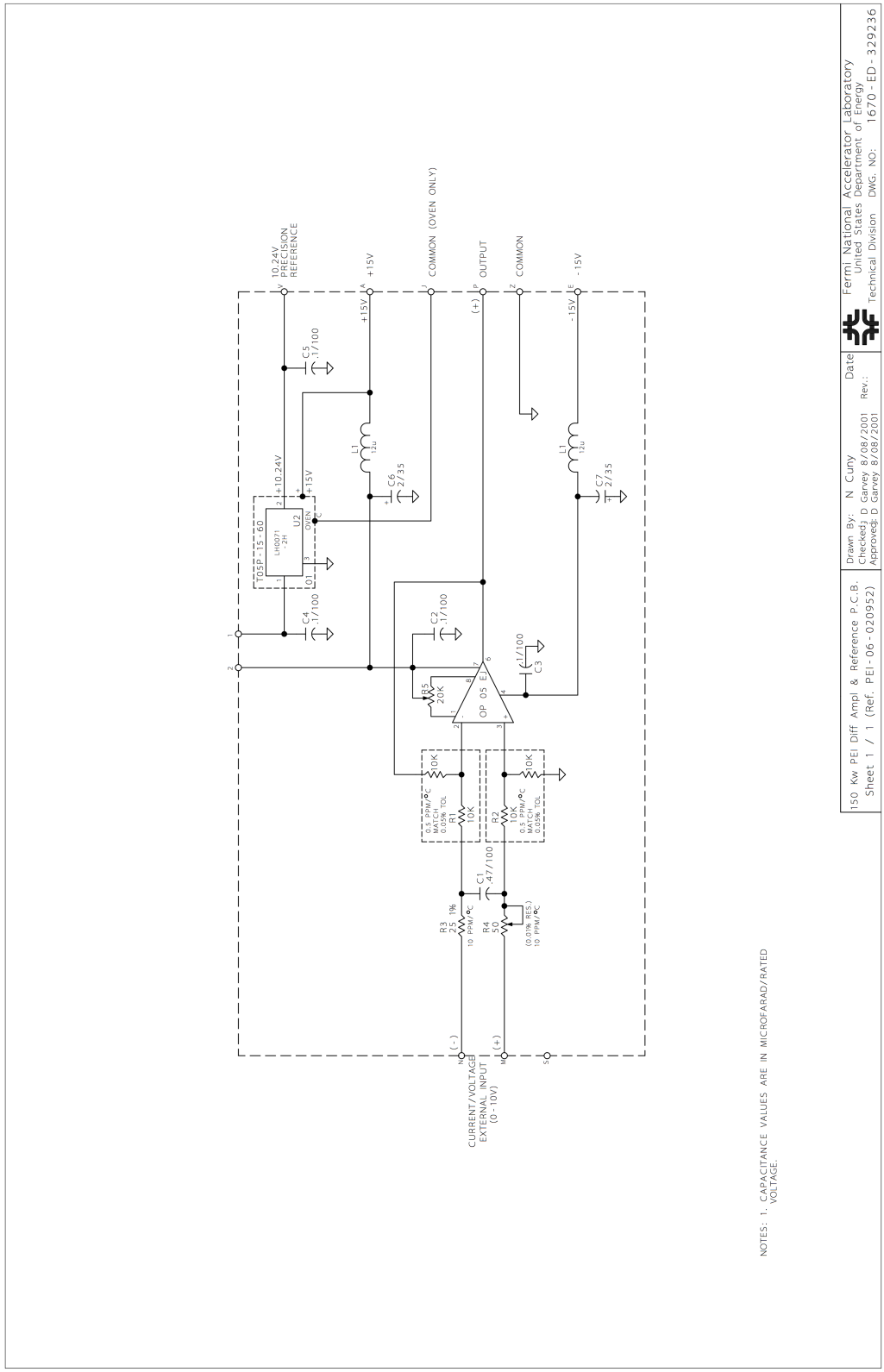


Figure A.4: PEI Difference Amplifier and Reference.

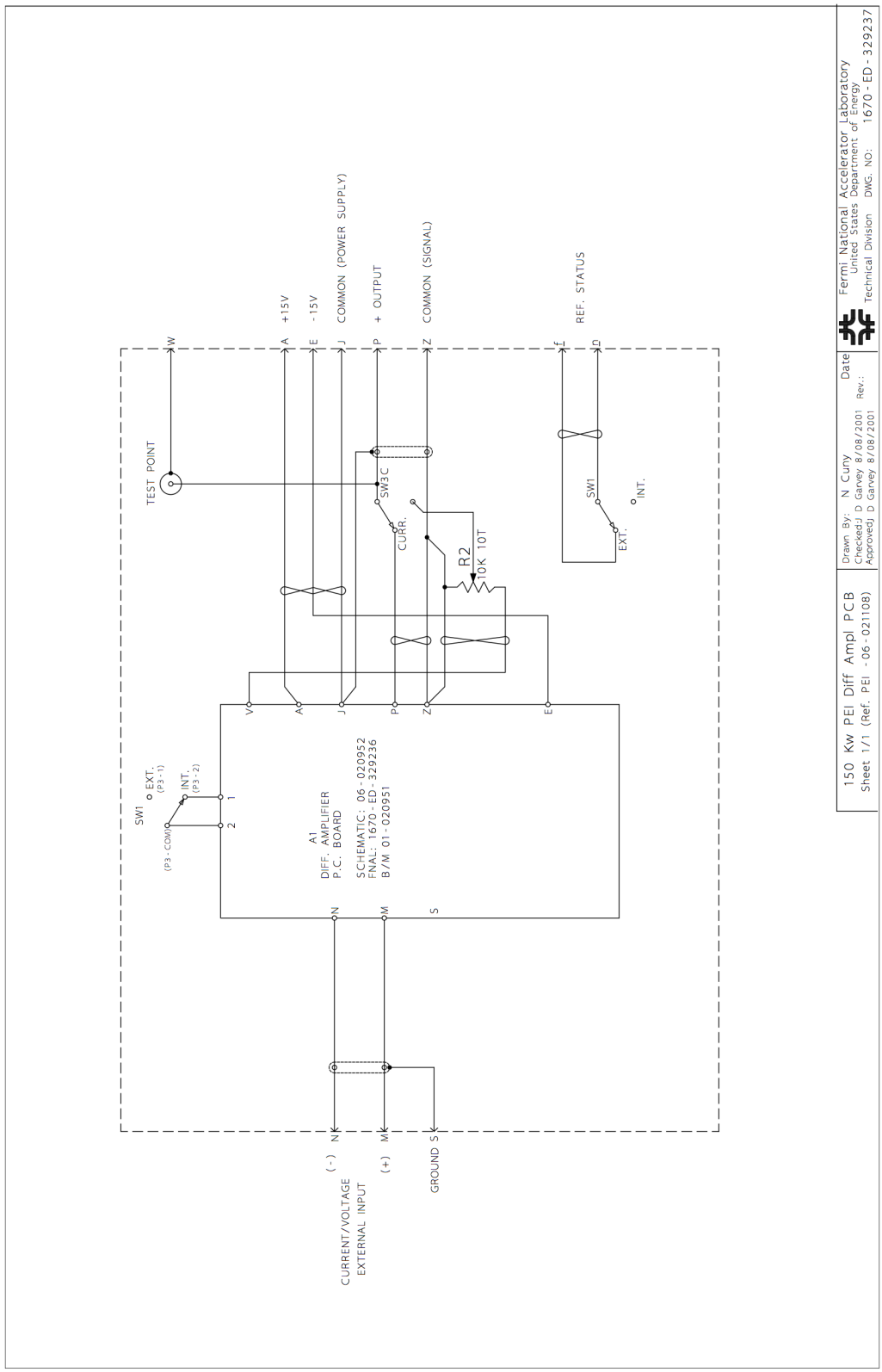


Figure A.5: Difference Amplifier.

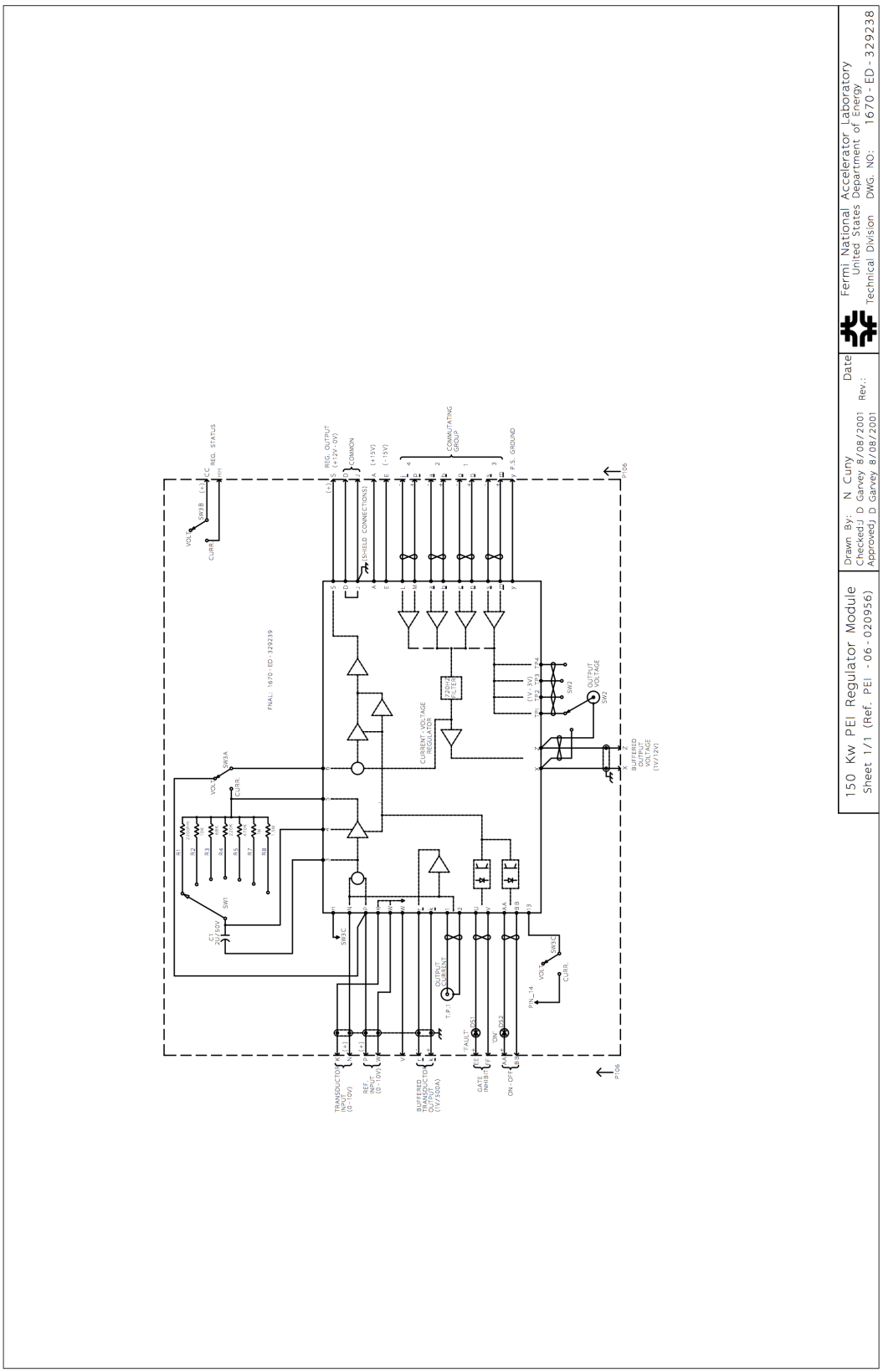


Figure A.6: Power Supply regulator module.

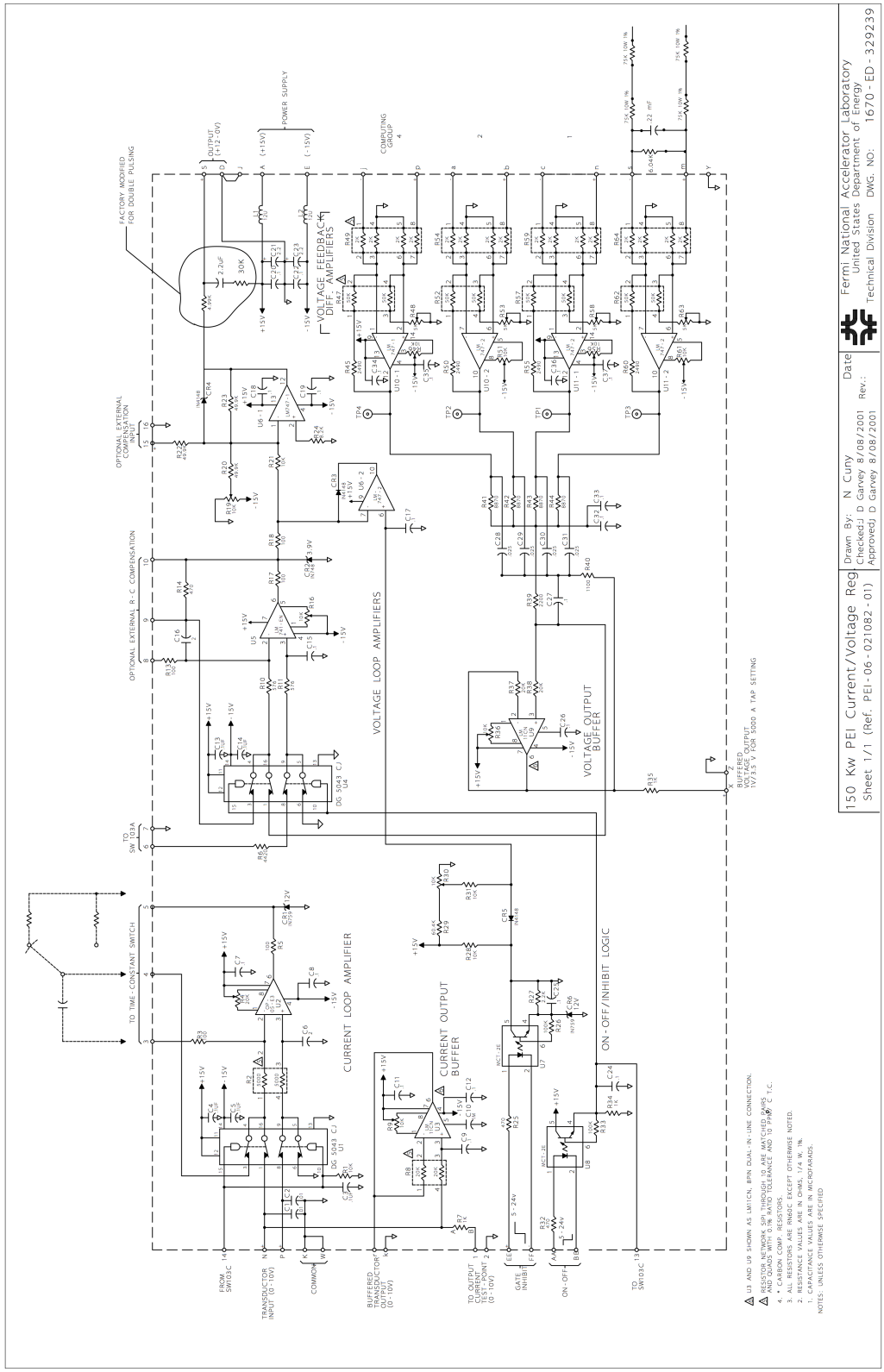


Figure A.7: PS Current/Voltage regulator.

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