A Voltage Monitoring Device

by

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Chairman, Departmental Committee on Theses

Acknowledgement

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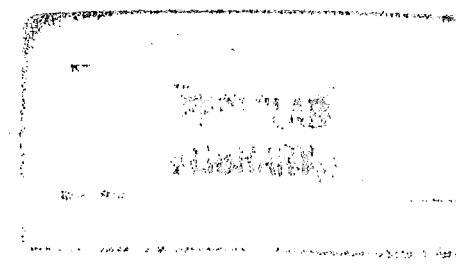


Introduction

This voltage monitoring device was designed and constructed for the APC group for use in a series of experiments to be conducted at the Fermi laboratory. These experiments will utilize a 30" hybrid spectrometer, consisting of a 30" bubble chamber, a system of proportional wire chambers (PWC), a fast particle identifier (CRISIS) and a forward gamma detector (FGD). The set up allows measurement of the incident beam over 300 meters, and measurement of the fast outgoing track to six meters, increasing the accuracy in path measurements.

The construction of the voltage monitor was motivated by the use of the FGD. The FGD consists of a converter, a vertex locator and an absorber. A γ enters the converter, four radiation lengths of Pb glass, and is converted into a shower of e's, $\bar{e}$'s and γ's. The Cerenkov radiation produced by the e's and $\bar{e}$'s is detected by an array of photo multiplier tubes (PM). After the converter shower is near its maximum size it passes through the vertex locator and into the absorber, 24 radiation lengths where it is completely absorbed. There are approximately 250 PM tubes in this system and the desired invariance in the gain of the PM tubes, and hence the desired invariance of the PM tubes' supply voltages resulted in the construction of the voltage monitor. Because of the large number of voltages to monitor, it was not economically feasible to buy a commercial device for this function.

While the device was still in the planning stage, it was decided to expand its capability to 511 channels to accomodate any other voltages that might require monitoring.

The following are the specifications.

Specifications [1]

The system will monitor up to 511 channels with channel zero left unused. Each channel will monitor either polarity. The system will sound an alarm if the voltage monitored changes by more than a specified percentage.

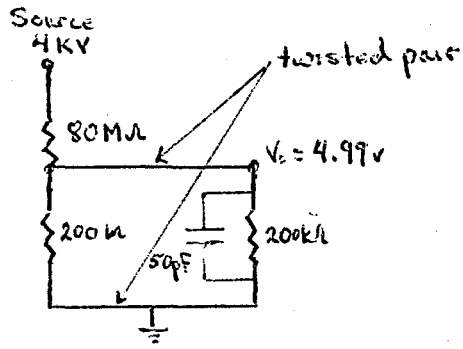
The input impedance of the system is 200 KΩ and the input voltage for all channels is ± 5v. Any users with high voltage sources should step down his or her voltage to this value. (See fig, 1 for recommended circuit.) The users' step down resistor chains should not drift more than 1%. The desired current to the system is approximately 50 μA.

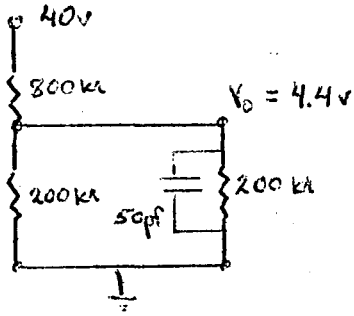
The input impedance to the Analog to Digital Converter is 1 MΩ. This is obtained by a buffer system before the ADC. The output of the ADC is eight bit and 5v. will correspond to 200 binary. A 2% change in a monitored voltage corresponds to a change of four least counts.

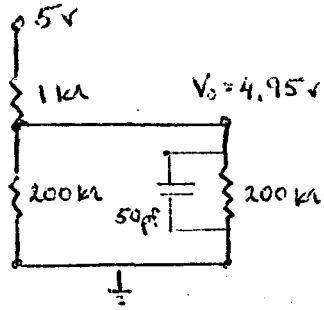
Three modes of operation will be incorporated and consist of:

a. An initialization mode which will run one full cycle (all 511 channels)and read the voltages to be monitored into memory. These voltages are presumed to be correct and will be used for all further comparisons. 8K of random access memory (RAM) is used. This mode is controlled by a guarded switch to prevent later destruction of recorded values.

[1] M. Elahy, D. Lewis & S. Oh, "Specifications of a Voltage Monitoring Device," APC Engineering Note 79-1, (Feb. 28, 1979)


Source
4KV
twisted pair
80MΩ
V_o = 4.99v
200 Ω
200kΩ
50pF


40v
800kΩ
V_o = 4.4v
200kΩ
50pf
200 kΩ


5v
1kΩ
V_o = 4.95v
200kΩ
50pf
200 kΩ

(fig. 1)

b. A run mode, which is continuous full cycle monitoring. This mode is interrupted when a deviation between the monitored and recorded value exceeds four least counts. When this occurs, an audio and a visual alarm are triggered and a display will read out:

   i) sign bit

   ii) scaled recorded voltage

   iii) scaled monitored voltage

   iv) channel number

c. A manual mode that allows single channel monitoring and single channel corrections to recorded values in memory. Corrections to memory must be done in the manual mode so only that channel is changed. There are two channel incrementing switches, one that advances channels at a rate of 20 per second, and one that increments singly. There is also a channel correct switch.

The run mode and initialization mode operate at a minimum of 50 μs per channel, 26 ms minimum full operating cycle. The actual operating rate is 2 ms per channel.

There is a remote display and an alarm in the control room. Adjustments however, can only be made at the main pannel.

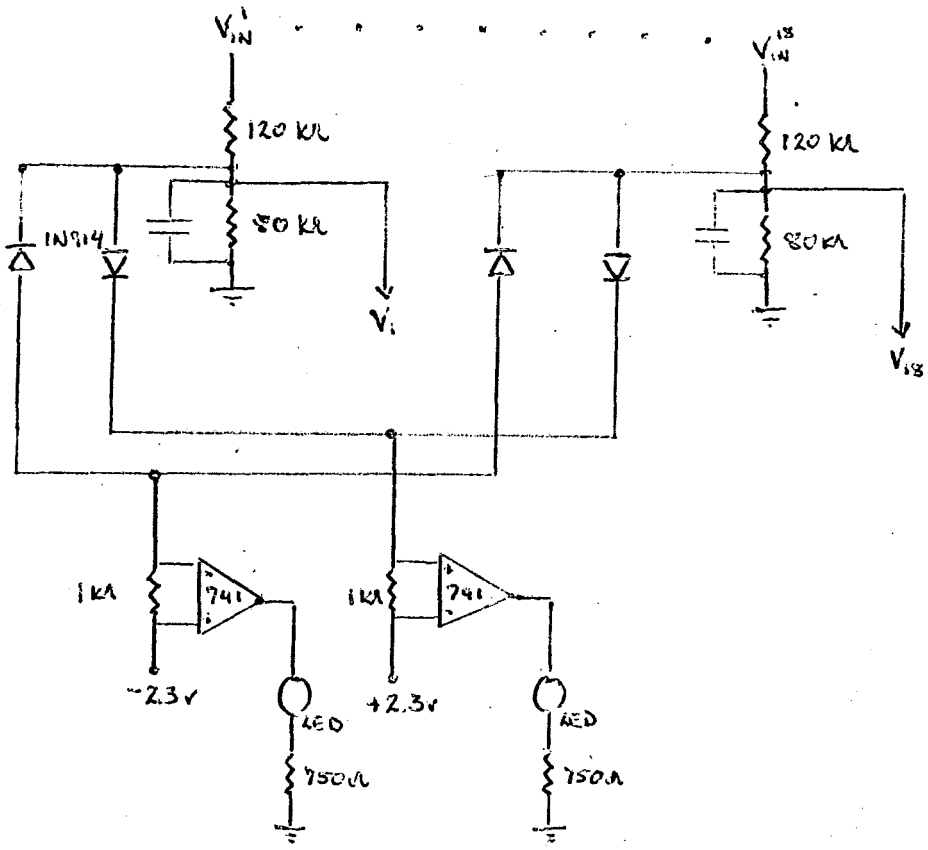
The system requires four operating voltages, +5, -5, +15 and -15 volts. The power dissipation is approximately 500mW.

Each channel is protected by diodes limiting the input voltage to $\pm$ 6 v. Light emitting diodes (LED) indicate improper voltages.

Design

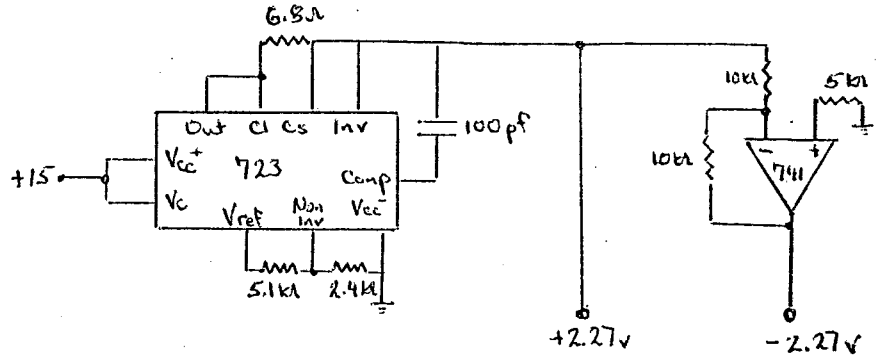
A complete schematic of the system is included as Appendix I. The first component of the design consisted of the multiplexer. CMOS components were used since they allow direct transmission of analog signals, being voltage controlled devices rather than current controlled devices as are TTL components. Since the voltages to be monitored were not determinate, it was decided that the voltage step down to meet internal requirements should be external to the system. Users would then be required to step down their own voltages taking into account the internal impedance and send the system $\pm$ 5 volts as mentioned in the specifications. The user is then responsible for keeping track of his or her own scaling factor. The $\pm$ 5 volt input was then stepped down internally to $\pm$ 2 volts which corresponded to an output from the ADC of 200 binary. 1%, $\frac{1}{4}$ W resistors were used for the internal resistor chains. The internal resistor chains were protected by two diodes pegged to the voltage limits and overloads triggered an LED. Every 18 channels were tied together by the diode protection lines, and these lines went to two Op-amps to ensure sufficient current to render the LED's visible. (See fig. 2 and fig. 3) The Op-amp will saturate at approximately 2mV. The 1 KΩ resistor ensured that the current was sufficient to drop this. The diodes used, IN914's, had a sufficiently rounded firing point to allow this current when they were forward biased in excess of .2 volts.

Setting the limiting voltages at ± 2.3 volts then pegs the internally stepped down voltage to ± 2.5 volts and triggers the LED when the input voltage exceeds 6.5 volts.



(fig. 2)

± 2.3 volt regulator [2]



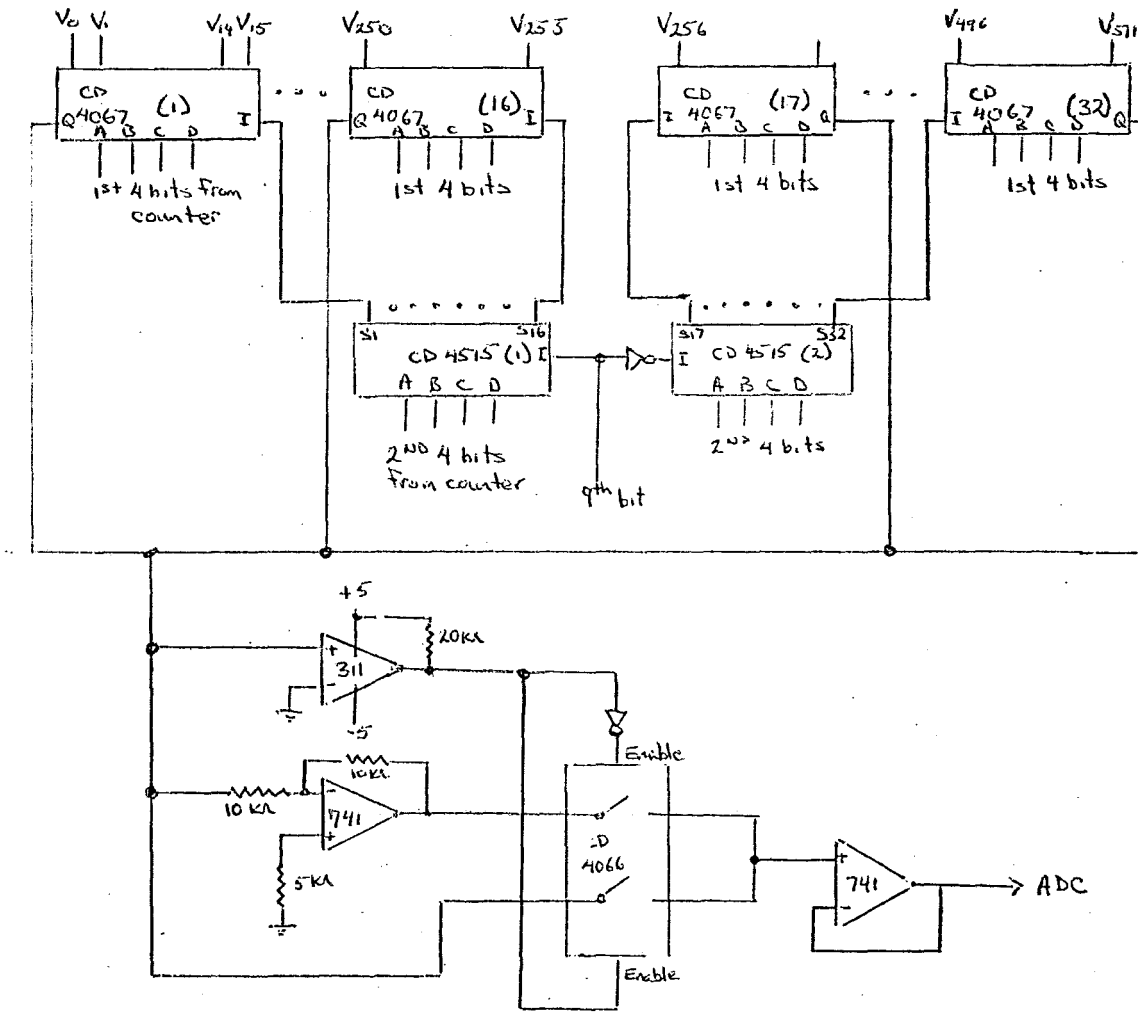
(fig. 3)

The voltages were multiplexed using 32 CD 4067's, CMOS 16 to 1 multiplexers, and two CD 4515's, 4 to 16 line decoders. The fact that both positive and negative voltages were being transmitted required these CMOS components to be operated at +5 volts VDD and -5 volts VSS, to meet the operating requirements VDD $\geq V_i \geq$ VSS and VDD - VSS $\leq$ 15v. Each of the 32 CD 4067's multiplexed 16 channels and was operated by the four lowest bits of the 9 bit address. The two 4515's were operated by the next four bits and each selected one of 16 CD 4067's and enabled it in turn. The 9th bit of the address selected the CD 4515 to enable.

The output of the multiplexers was then sent to a comparator to test whether it was positive or negative. The output of the comparator then selected a path for the multiplexer output to the ADC by means of a CD 4066, Quad Analog Switch, the path for negative signals passing through an inverter. The signal was buffered before reaching the ADC by an op-amp in a unity gain configuration.

[2]The Linear Integrated Circuits Data Book, Texas Instruments 1976, p. 5-15.

The choice of resistors used in the inverter was determined by the frequency requirements for 500 cps. [3]



(fig. 4)

[3] Linear Integrated Circuits Data Book, Fairchild Semiconductor, 1976, p. 12-85 ff.

CD 4515 TRUTH TABLE

Inhibit (I)	A	B	C	D	Selected Output S_i=0, all others=1
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16
1	X	X	X	X	all S_i=1

The CD 4515 has a 4 bit strobed latch input, allowing changes when the strobe input is high. In this system, the strobe is held high.

(fig. 5)

X = Don't Care

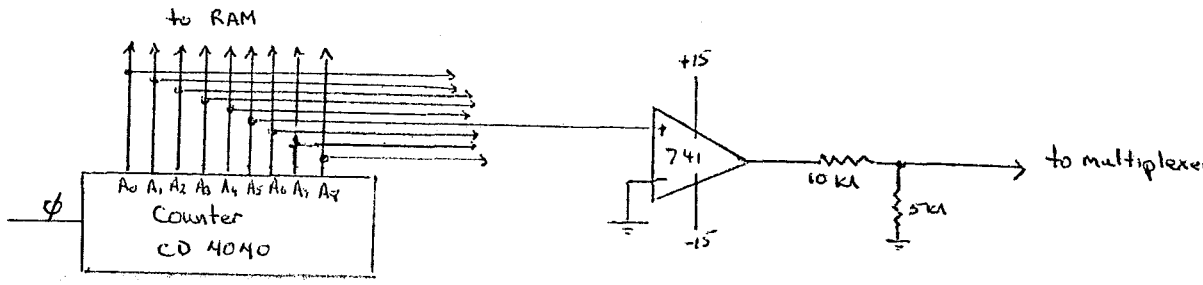
CD 4067 TRUTH TABLE

Inhibit (I)	A	B	C	D	Selected Channel
0	0	0	0	0	1
0	0	0	0	1	2
0	0	0	1	0	3
0	0	0	1	1	4
0	0	1	0	0	5
0	0	1	0	1	6
0	0	1	1	0	7
0	0	1	1	1	8
0	1	0	0	0	9
0	1	0	0	1	10
0	1	0	1	0	11
0	1	0	1	1	12
0	1	1	0	0	13
0	1	1	0	1	14
0	1	1	1	0	15
0	1	1	1	1	16
1	X	X	X	X	None, output is high impedance

(fig. 6)

The output from the ADC was 10 bits full scaled against 10 v. The 2 v. ADC input therefore corresponded to 200 binary, and only the first 8 bits were used from the ADC. The output from the ADC was 5 volts high and 0 volts low. Since it was later necessary to interface this output with TTL components, it was decided to leave the output unchanged and operate the remaining CMOS components at +5 and 0 volts.

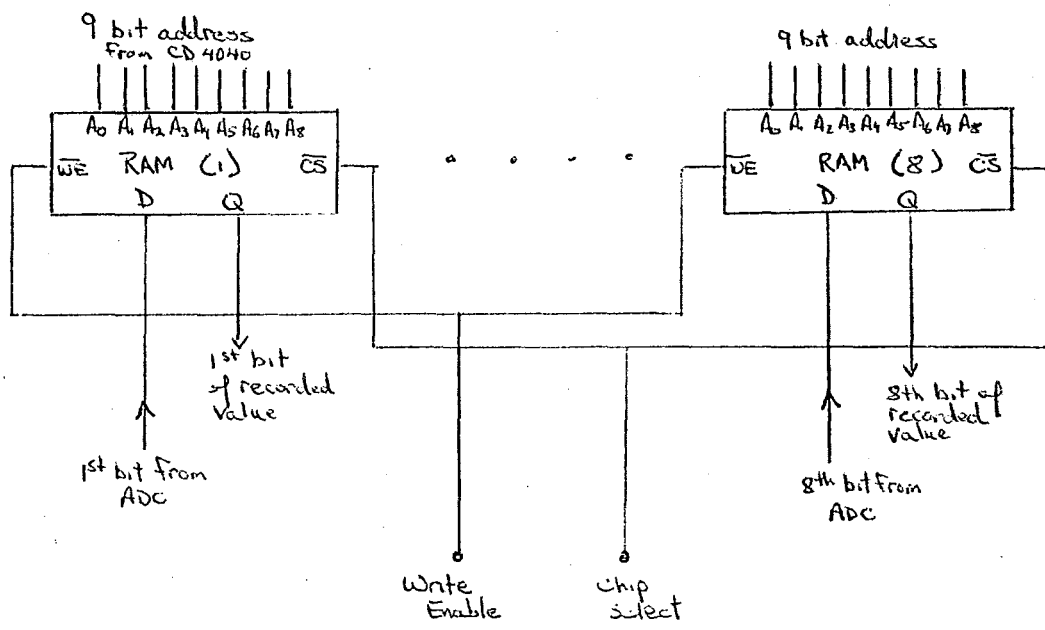
The same counter output that addressed the channel to be converted also addressed eight 1K X 1 bit RAM's. Since the CD 4515's and CD 4067's are operated at ± 5 volts to accomodate both input polarities, it is necessary to convert the +5 volt and 0 volt address before it is sent to the multiplexing components. The address is sent to an array of op-amps acting as comparators against 2.5 volts. The output of the comparators is ± Vsat., ± 15 volts, and this is stepped down by a resistor chain to ± 5 volts. The address lines to the RAM's are tapped off before the conversion.



(fig. 7)

The slew rate of the Op-amps is .7 μs/v.[4] This requires approximately 40 μs set up time for the converted pulse.

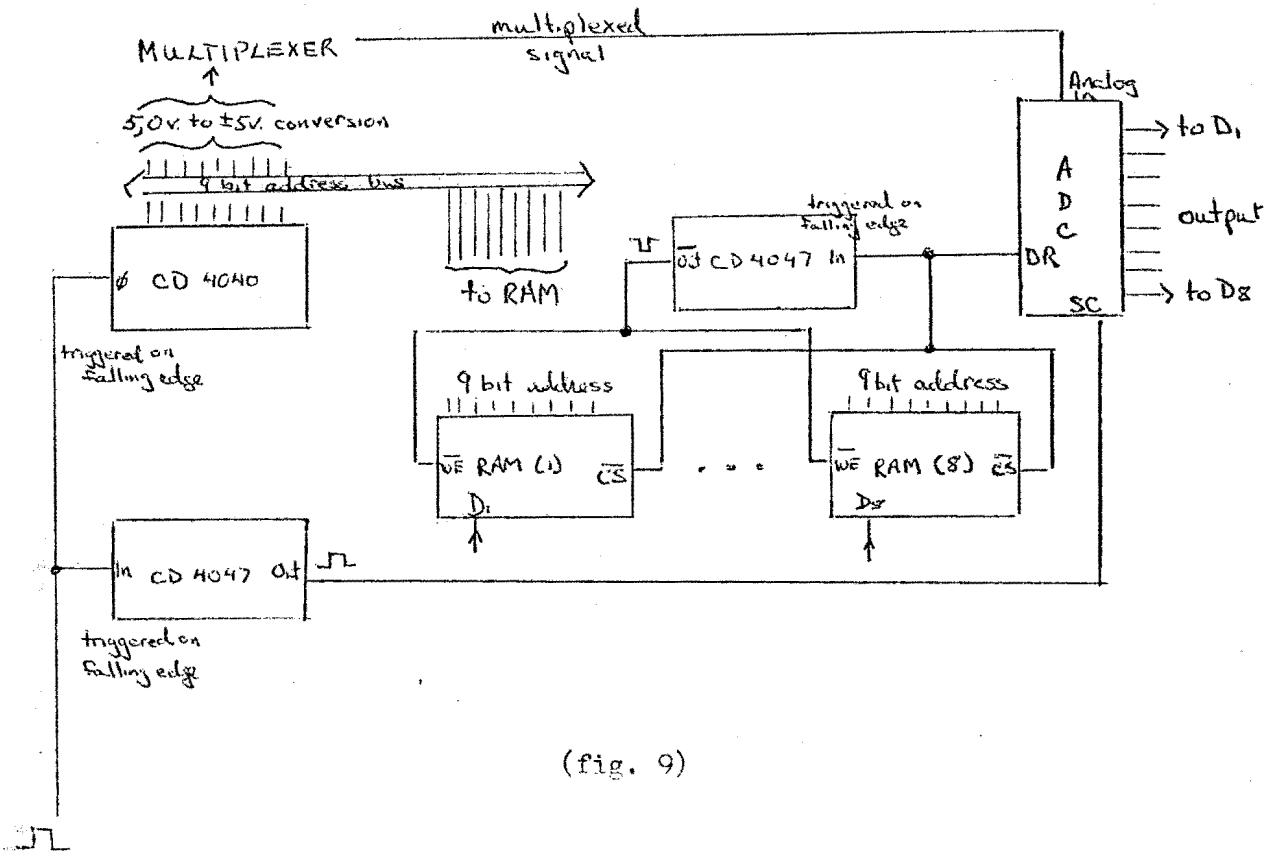
4 Linear Integrated Circuits Data Book, Fairchild Semiconductor, 1976, p. 12-85 ff.



(fig. 8)

Data is written into the RAMs when Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) are low. Data is read out when $\overline{CS}$ is low and $\overline{WE}$ is high. Memory is addressed when $\overline{CS}$ is high, and the output is at a high impedance state during $\overline{CS}$ high. As shown in figure 8 above, each Ram contains one of the eight data bits for each address. The 10th address bit, not shown, is held low. Figure 9 shows the interconnection between the counter, ADC and RAMs in the write mode.

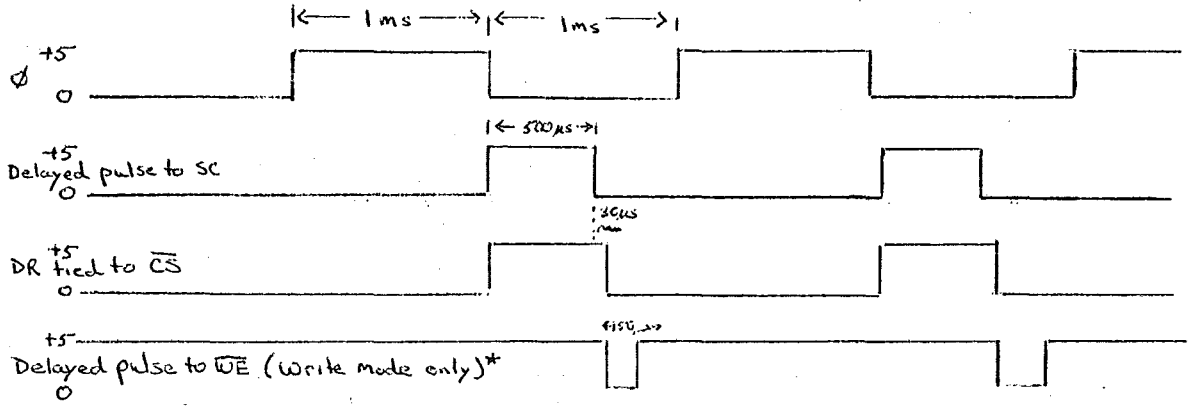
The clock pulse to the counter increments the channel and multiplexes a new voltage to the ADC. The clock pulse also goes to a CD 4047, a Monostable/Astable Multivibrator, used in this instance in the monostable mode to produce a delayed pulse triggered by the falling edge of the clock pulse. This delayed pulse starts the ADC conversion and allows sufficient time for the multiplexed analog signal to stablize. (This takes into account the slew rate of the op-amps.)



(fig. 9)

When the Start Convert (SC) input of the ADC recieves the rising edge of the delayed pulse, the Data Ready output of the ADC goes high. The Data Ready (DR) output is tied to the $\overline{CS}$'s of the RAMs, and its transition to high allows the RAM memory address to change. The ADC starts conversion on the falling edge of the delayed pulse and the conversion takes approximately 30 μs. When the conversion is completed DR returns low. The DR signal also goes to a second monostable, triggered on the falling edge but using $\overline{Q}$ as the output. (⊓⊔) The transition of DR to a low output therefore pulses the $\overline{WE}$ inputs of the RAMs low for a sufficient amount of time to write the ADC output into memory. The system then waits for the next clock pulse.

In the normal operating mode, the second monostable is disconnected and $\overline{WE}$ is held high, keeping the RAM's in a read mode.



(fig. 10)

The pulse widths used are much greater than is necessary. The requirement of one second to check all channels gives 2 ms. per channel. This allows huge margins. Operation on a new channel commences on the falling edge of ϕ. 50 μs for the start convert pulse width would have been sufficient to accomodate the op-amps' slew rate. 500 μs have been allocated. The conversion time is independent of the circuitry. .5 μs would have sufficed for the write pulse. 150 μs have been allocated, and 1300 μs are still left over. The delayed pulse widths from the monostables are determined by an RC time constant where $Tw = 2.48\ RC$. For $Tw = 500\ \mu s$, $R = 100\ k\Omega$ and $C = 2000\ pf$.[5] For

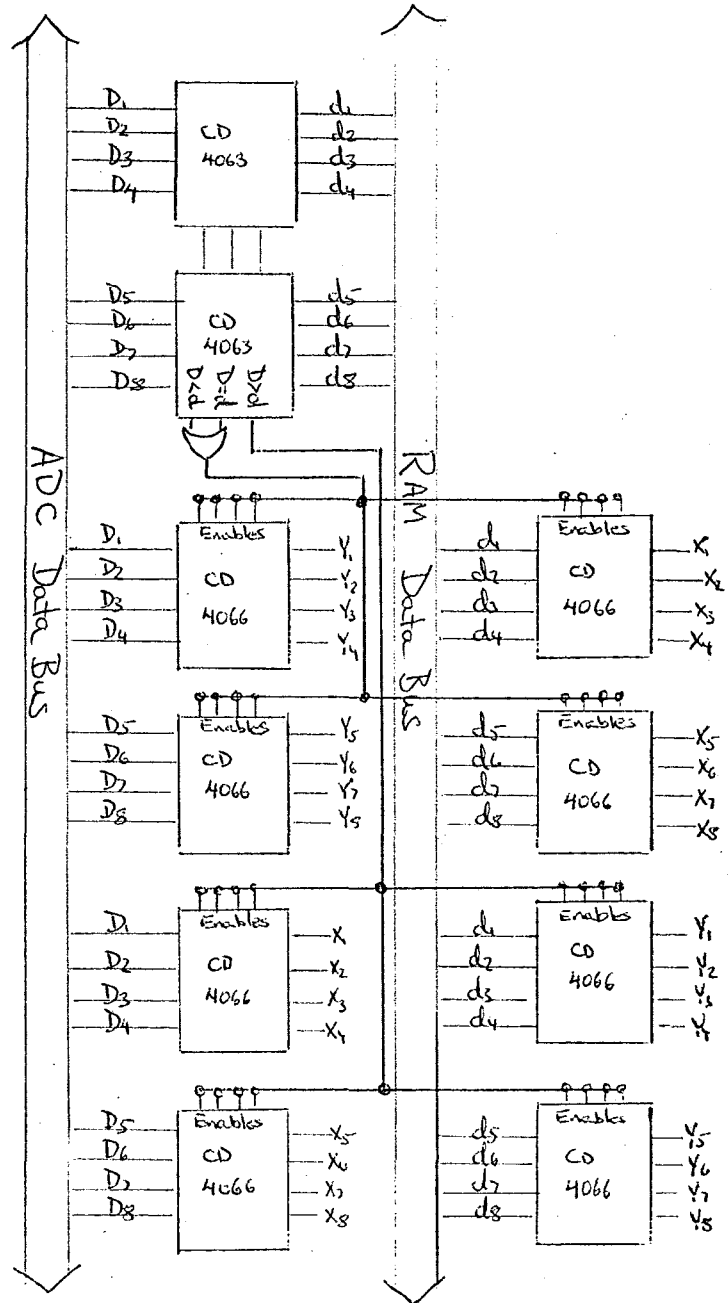
[5] COS/MOS Integrated Circuits, RCA Corp., 1974, p. 235

Tw = 150 μs, R = 30 KΩ and C = 2000 pf.

When the circuit is in the normal operating mode ($\overline{WE}$ held high), the output from the ADC and the output from the RAM is subtracted and compared with binary 3, three least counts. If the remainder is less than or equal to three least counts, the next clock pulse is enabled. If the remainder exceeds three least counts, the following clock pulses are inhibited. The subtraction and comparison involves four CD 4063's (4 bit comparators), two CD 4030's (Quad exclusive or gates), two CD 4008's (4 bit full adders), and eight CD 4066's (Quad switches). Two CD 4063's and the eight CD 4066's are used to determine which of the two 8 bit numbers is larger and load the larger number into the X inputs of the X-Y subtracting circuit to avoid negative values. See figure 11. The Y input, (the smaller number) is then complemented by the exclusive or gates. This complement is then added to the X input with 1 carried in to the lowest bit. The operation is therefore $\overline{Y} + X + 1$ which is equivalent to X - Y if $X > Y$, which we have ensured by the loading scheme. See figures 12 and 13.

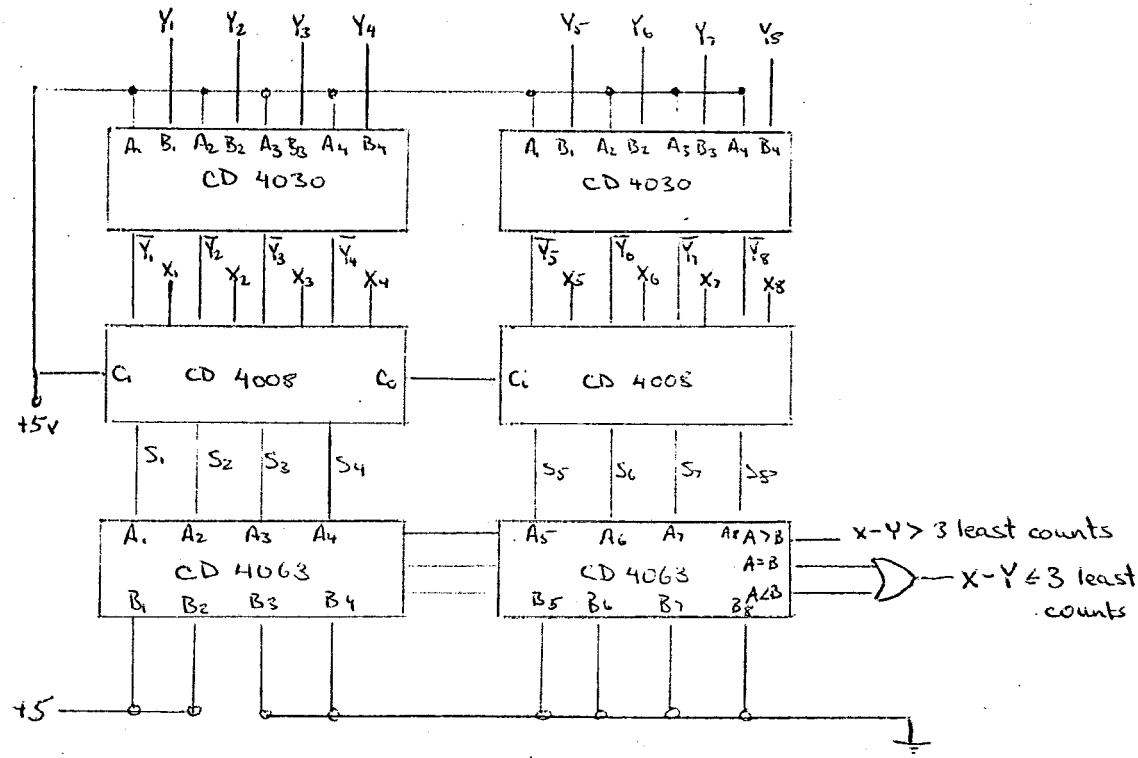
The output of the full adder, X - Y, is then compared to the three least counts by two CD 4063's. The comparator has three outputs, X-Y < three least counts, X - Y = three least counts, and X - Y > three least counts. The first two outputs are run through an OR gate reducing the logical outputs to X - Y $\leq$ three least counts or X - Y > three least counts.

Loading Scheme



(fig. 11)

Subtractor



(fig. 12)

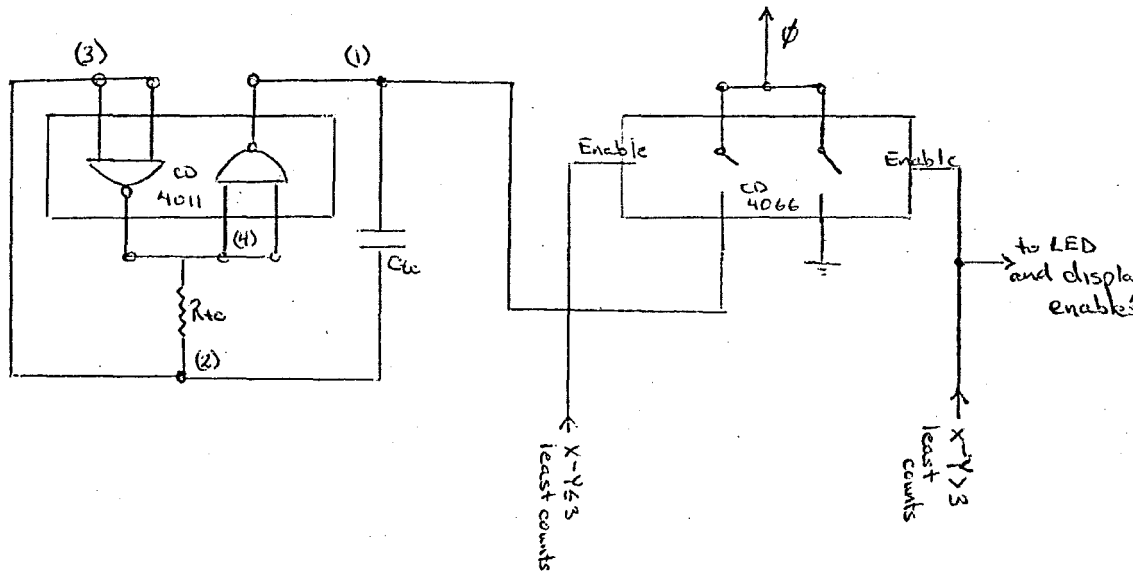
Exclusive Or Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0
1	Y_i	$\overline{Y_i}$

(fig. 13)

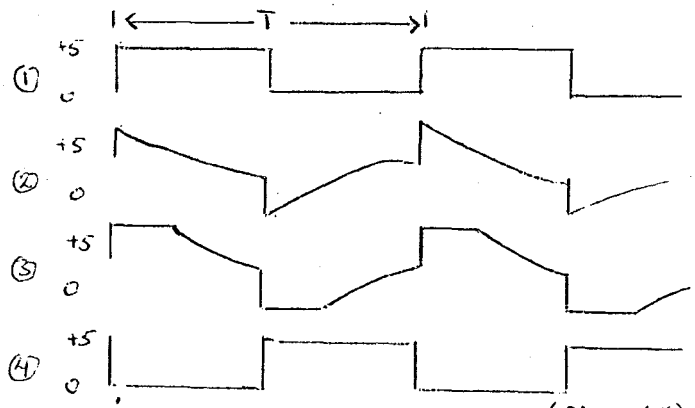
These two outputs are fed to the enable inputs of half of a CD 4066 (Quad switch). The X-Y$\leq$ 3 least counts enables the clock pulse to the counter, while the X-Y> 3 least counts sets the counter's clock pulse input to ground. The X-Y> 3 least counts also triggers an LED and enables the three displays, channel number, ADC output and RAM output.

The clock pulse generator is half of a CD 4011 (Quad NAND gate).



(fig. 14)

The two NAND gates act as a multivibrator. The voltage waveforms at the points numbered in figure 14 are:



(fig. 15)

$$T = -RC\left[\ln \frac{Vtr}{(Vdd + Vtr)} + \ln \frac{(Vdd - Vtr)}{(2Vdd - Vtr)}\right]$$

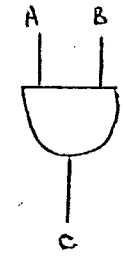
$\simeq 2.2\ RC$ Maximum variations in T are less than 5%.[6]

For 512 channels per second, Rtc = 500 KΩ, and C = 2000pf. For 20 channels per second, Rtc = 250 KΩ and C = .1 μf.

The display components of the system required interfacing with TTL devices. The binary number must be converted to binary coded decimal (BCD), and then to a seven segment output. Binary to BCD converters are not manufactured in CMOS. The nine bit address, eight bit ADC output and eight bit RAM output are run through CD 4050's, hex buffers, to meet the current sourcing requirements for TTL components, and are then enabled by the X-Y > 3 least counts line. The enable function is accomplished by an array of AND gates, SN 7408's. Each gate has one input tied to the X-Y > 3 least counts line. When this is a logical high, the data on the other input is enabled. Otherwise a display output of 0 is observed.

AND Logic Table

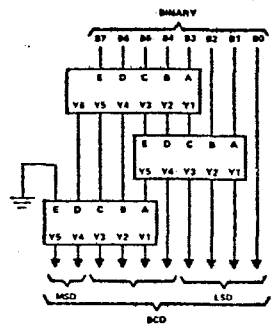
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



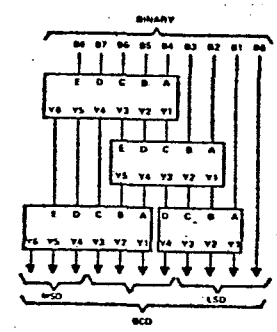
(fig. 16)

6 COS/MOS Integrated Circuits, RCA Corp., 1974, p. 532

The data lines are then run through an array of SN 74185's, binary to BCD converters, in the following configuration. [7]



8 bit Binary to BCD



9 bit Binary to BCD

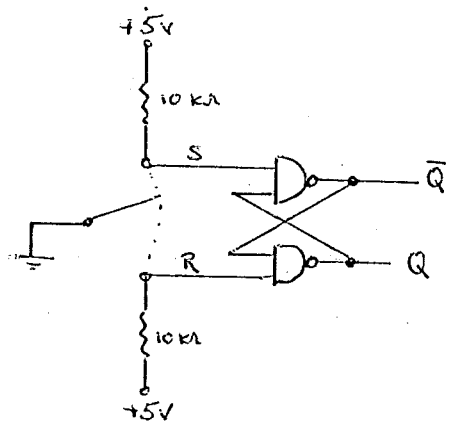
(fig. 17)

The BCD output then goes to SN 7447's, BCD to 7 segment decoder/ drivers, which run the displays.

Reset is accomplished by pulsing the SC input of the ADC after correcting the source voltage. If the recorded value in memory is to be changed, the 500 cps clock pulse is disconnected, the counter is advanced to the channel to be corrected, and the write input is pulsed high. There are two alternative clock pulses , a one shot pulse, and a 20 cps pulse, that are used in the manual mode. The 20 cps pulse uses the same configuration as the 500 cps pulse but with a different RC time constant. The one shot pulse is generated by two NAND gates in an S-R flip flop configuration. This avoids bounce pulses. The 20 cps and one shot clock pulses are independent of the X-Y $\leq$ 3 least counts enable line. The display can be enabled during the manual mode by setting the inputs of the AND gates previously described high.

[7] The TTL Data Book for Design Engineers, Texas Instruments Inc., 1976, p. 7-295

R/S Flip Flop & Truth Table

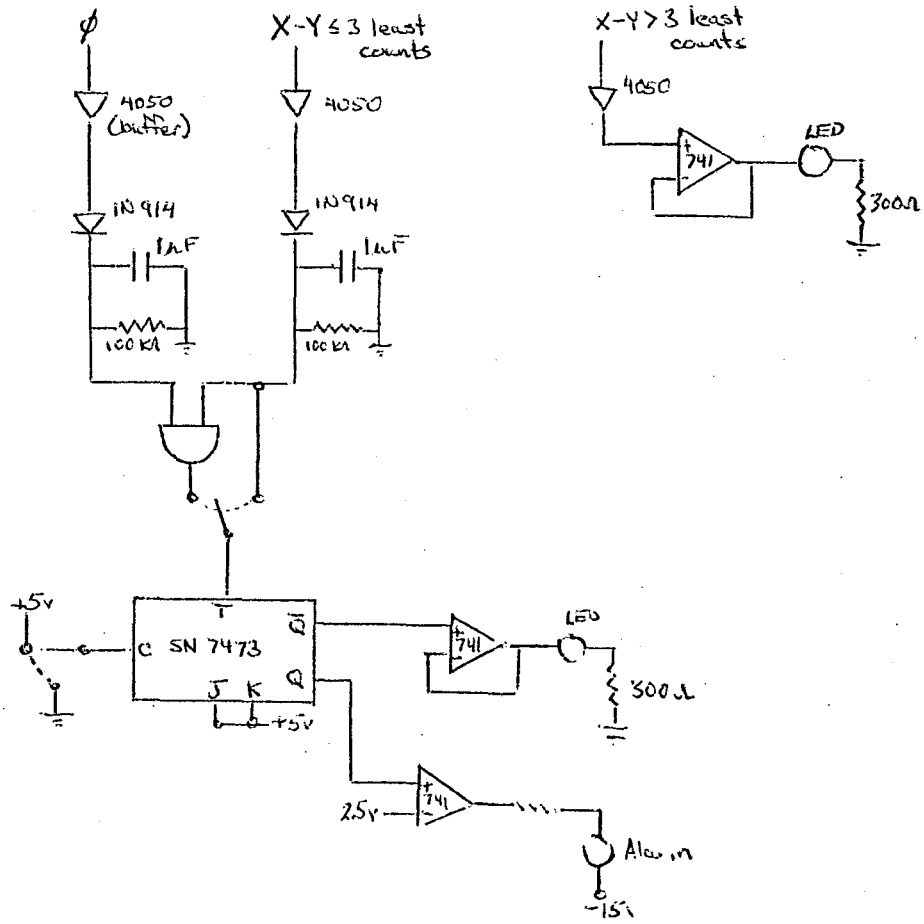


R	S	Q
0	0	Retains last State
0	1	1
1	0	0
1	1	Retains last state if previous SR state was 01 or 10

(fig. 18)

The alarm will trigger if either the voltage monitored differs from the recorded value by more than three least counts or if, in the run mode, the clock pulse fails. The clock pulse and the X-Y $\leq$ 3 least counts are run through buffers and then through peak followers. When either of these inputs is high, +5 volts, the output of the peak follower will be 4.4 volts (There is a .6 volt drop across the diode). When either of the inputs drops to ground, the output of the follower will decay exponentialy, $4.4\ e^{-t/RC}$. By choosing RC much larger than the frequency of the clock pulse and the fluctuations in X-Y during the arithmetic operation, the output will only drop to a logical low if either input drops low for a significant time. R was chosen to be 100 KΩ and C to be 1 μf, giving a time constant of .1 second. See figure 19. The output of the two peak followers is run through an AND gate. If either input drops low, the output of the AND gate will drop low, and the falling edge will complement the outputs of a J-K flip flop used in a clocked operation mode. The alarm is fired by

the Q output of the J-K flip flop, while the $\overline{Q}$ output indicates that the system is running normally. The alarm can be silenced by pulsing the clear input of the J-K flip flop low. The X-Y > 3 least counts line will also trigger an LED, indicating a voltage flucuation in the monitored voltage, and will remain on until the voltage is corrected. The and gate connecting the two peak followers is automatically disconnected when the manual mode is used, and the alarm will only trigger if the X-Y $\leq$ 3 least counts drops low.



(fig. 19)

J-K Flip Flop
Truth Table *

Clear	Clock	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Retains last state	
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Complements	

X = Don't Care
H = High level
L = Low level
↓ = Falling edge of clock pulse

* Without Preset input

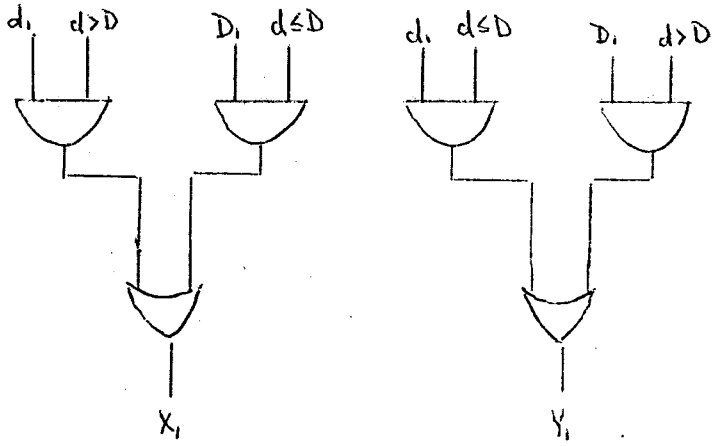
(fig. 20)

Test Results

At the present time, construction of the system is not yet complete due to non-receipt of several components. However, a 64 channel proto-type was constructed and tested. The displays were not included in this proto-type since we were not able to obtain the SN 74185's, binary to BCD converters. The ADC used for the proto-type was also defective, one bit of the output always remaining low and another always remaining high. A new ADC and the SN 74185's are expected to arrive in late July.

A heat test was conducted on the resistor chains and multiplexing components with the monitored voltages varying less than .1%. Since this is one tenth of one least significant bit, it presents no problem. The tests on the conversion components and memory was instrumental in determining the timing scheme. It was originally planned to maintain $\overline{WE}$ low throughout the initialization mode. It was found, however, that the ADC's output would change to a high impedance state approximately 10 ns before the DR output went high. Since the DR output controlled the change in address to memory, the high impedance output from the ADC was the last data written into memory prior to a new address, and this resulted in erroneous data being written into memory. For this reason, a delayed inverted pulse triggered by the fall of DR was used to write data into memory, and the pulse width was limited to ensure that the write operation was completed prior to a new conversion.

It was also originally planned to use CD 4066's, quad analog switches, to enable the display. It was found, however, that these switches are very susceptible to failure resulting from static charges, and their internal protection was insufficient. They were replaced by AND gates. A series of these switches is still used to load the arithmetic components, and this is probably the weakest part of the design. If the system were redesigned, a better scheme would probably be to replace these by a series of AND and OR gates.



(fig. 21)

This would require only four more chips. Replacing all other CMOS components other than the multiplexing components which must remain CMOS, with their TTL equivalent would probably result in a hardier system. The only alternative to the use of a CMOS multiplexer is the use of reed switches controlled by decoder/drivers. This would be expensive and bulky. These changes were not made since during the two months the proto-type was operative and under test, the CMOS components did not fail once installed, and since most components for

the real system had already been obtained.

The only real discrepancy between rated and actual performance was found in the clock pulse generators. The CMOS manual suggested using another resistor between Rtc and the inputs of the first NAND gate (See figure 14). It was found, however, that this resulted in damped oscillation on the rising edge of the clock pulse, oscillations with a width of approximately 100 ns, damped to zero in about 1 μs. This was eliminated by not using the resistor. Since the resistor was suggested only to decrease variations in frequency by one to two percent, there was no problem in eliminating it.

Finally, a low pass filter was added to the visual alarm and display enable lines. This was necessary since during analog to digital conversion, the ADC's output was a high impedance state, and the alarm and enable lines went high during the conversion. With the low pass filter, the visual alarm and display enable lines were only affected by a real discrepency in the monitored voltage.

Summary

The resistor chains were mounted on two input pannels, $10\frac{1}{2}$" x 19" rack pannels. The diode chains and the multiplexing components were mounted on two 12" x 19" fiberglass boards. All other components were mounted on five Vector D. I. P. plugboards (3677's). All CMOS and TTL components were wirewrapped. The plugboards were not used for the multiplexing components due to the large number of inputs. The entire device was rack mounted. The plugboard connectors mounted on the back of the card cage allow access to all signals for diagnostic purposes.

The construction of the voltage monitor does not easily allow further expansion. The counter (CD 4040) is however a 12 bit counter and further channels could be obtained by the addition of CD 4067's (multiplexers) and another CD 4515 (4 to 16 decoder/driver) enabled by the 10th bit of the counter. The enable inputs to the two original CD 4515's would have to be passed through an AND gate with the complement of the 10th bit. The main difficulty would be to expand the address display. This could not be done simply.

The allowed deviation of the monitored voltage can be changed fairly easily by rewiring the comparator (two CD 4063's) that tests X-Y against three least counts. If, however, it was desired to be able to vary the deviation with channel number, a further set of components would have to be added. The easiest way to do this would

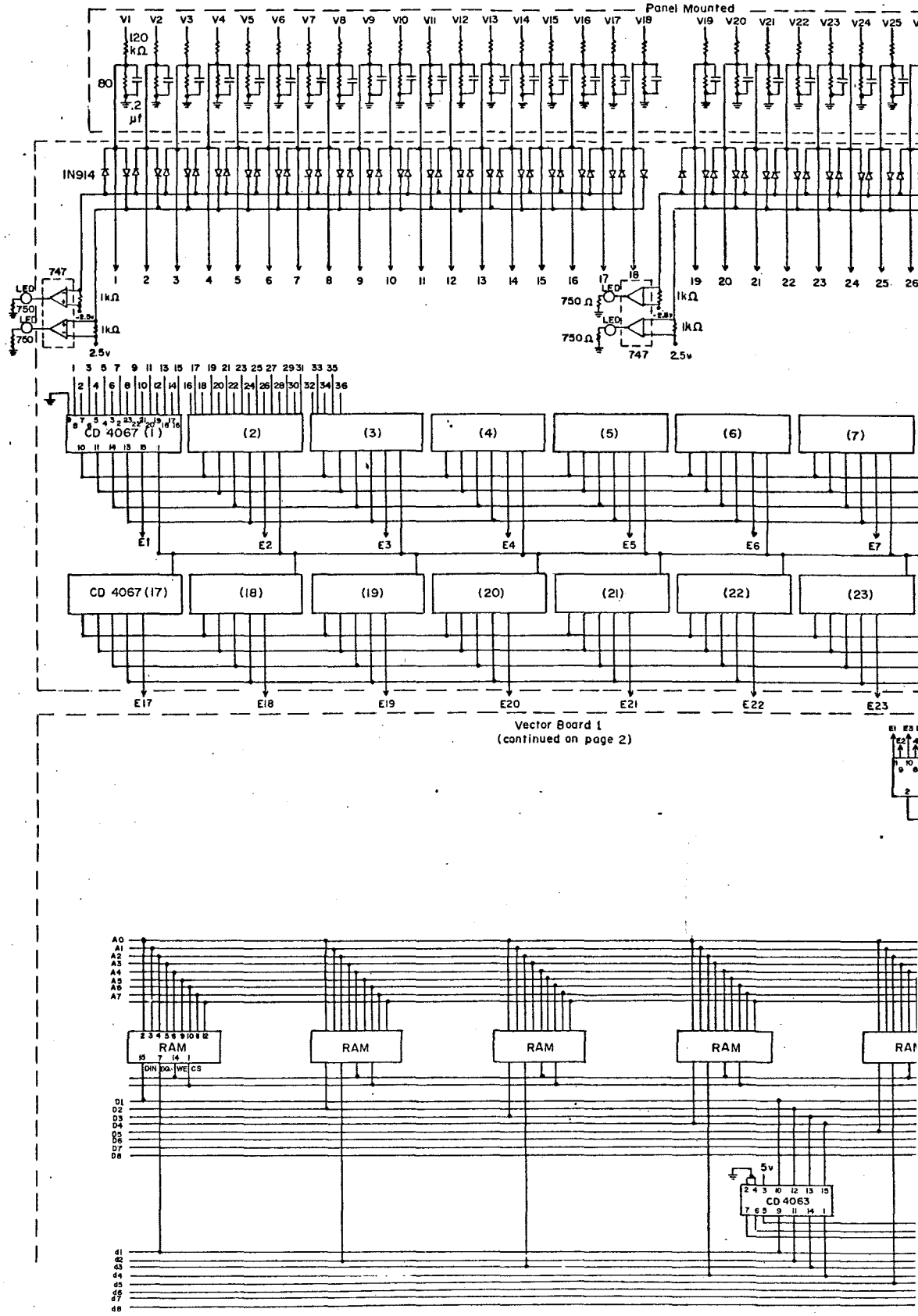
be to locate the special channels at the end of the array, (the last channels), and to compare the address with the channel number of the first special channel. The logical output of the operation would then be used to load the X-Y comparator with the desired number of least counts.

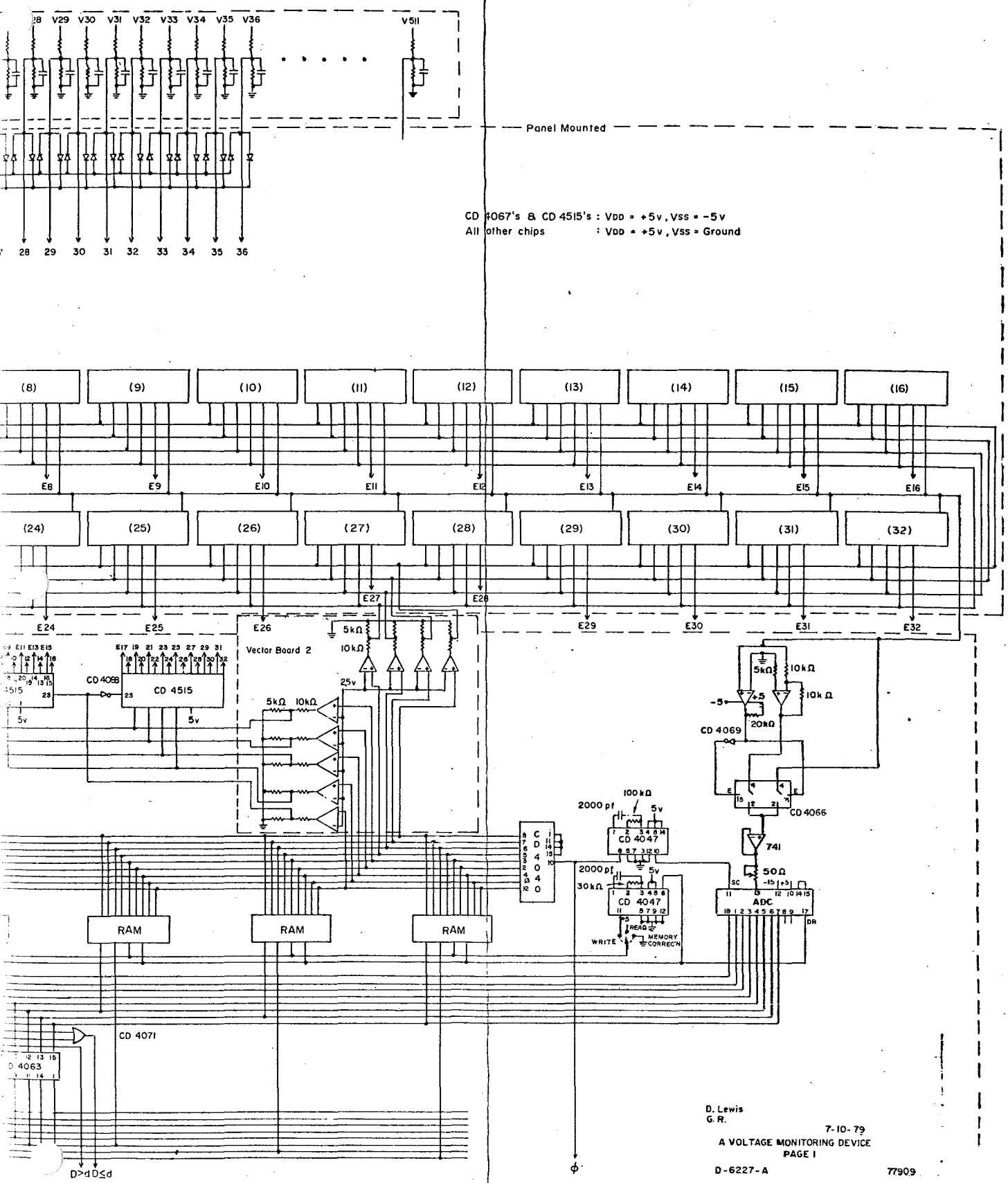
The monitoring rate can be changed by replacing the resistors and capacitors which control the time constant of the clock pulse generator. However, if faster monitoring is desired, the delayed pulses need to be adjusted accordingly.

Individual component specifications can be found in the CMOS and TTL manuals. The pin configurations of the components used have been included as Appendix II to facilitate use of the schematic.

In conclusion, although construction of the device is not complete, tests of the proto-type, individual components and those portions of the actual device presently completed conform to the specifications on page six. The system does monitor 511 voltages of either polarity, sounding an audio and a visual alarm when a monitored voltage deviates from its initial value by four or more least counts. The audio alarm can be silenced at the control pannel. The system does indicate the address of the incorrect voltage, its value, and the initial value, and all channels are monitored in one second. The initialization mode is quick and accurate. The correction to memory mode has been tested and works, and the 20 cps clock and single pulse generator work as designed. The system is temperature and noise immune.

Since the components that have not been tested are peripheral to the device, it can be stated safely that the device will function properly and no problems in the completion of the device are expected.


Panel Mounted
V1 V2 V3 V4 V5 V6 V7 V8 V9 V10 V11 V12 V13 V14 V15 V16 V17 V18
V19 V20 V21 V22 V23 V24 V25
120 kΩ
80
.2 µf
IN914
747
LED
750
1kΩ
2.5v
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
19 20 21 22 23 24 25 26
750Ω
CD 4067 (1)
(2) (3) (4) (5) (6) (7)
E1 E2 E3 E4 E5 E6 E7
CD 4067 (17)
(18) (19) (20) (21) (22) (23)
E17 E18 E19 E20 E21 E22 E23
Vector Board 1
(continued on page 2)
A0 A1 A2 A3 A4 A5 A6 A7
RAM
DIN WE CS
D1 D2 D3 D4 D5 D6 D7 D8
d1 d2 d3 d4 d5 d6 d7 d8
5v
CD 4063



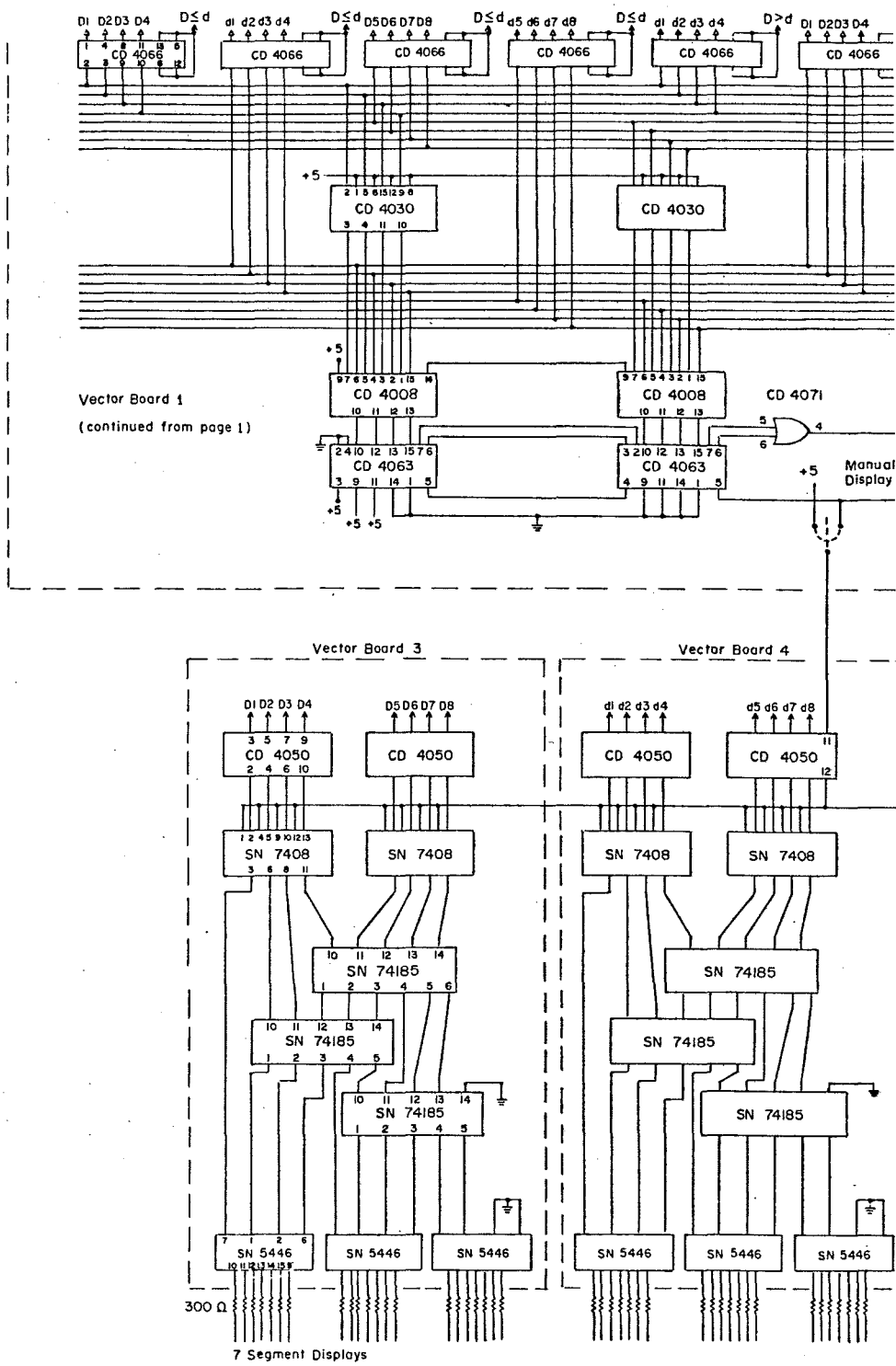
D. Lewis
G. R.

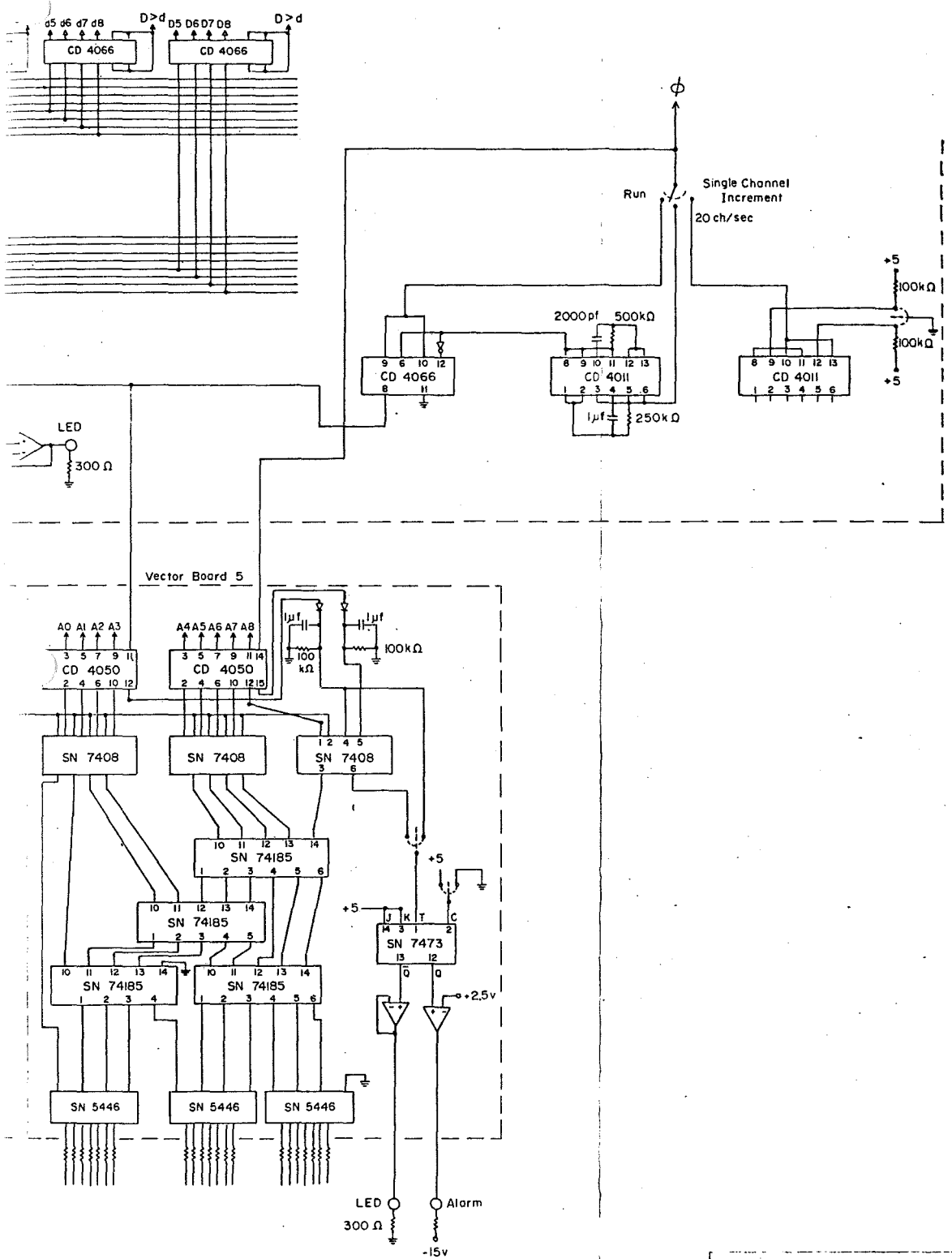
7-10-79

A VOLTAGE MONITORING DEVICE
PAGE 1

D-6227-A

77909


D1 D2 D3 D4 D≤d
CD 4066
d1 d2 d3 d4 D≤d
D5 D6 D7 D8 D≤d
d5 d6 d7 d8 D≤d
d1 d2 d3 d4 D>d
+5
CD 4030
CD 4008
CD 4063
CD 4071
Vector Board 1
(continued from page 1)
Manual Display
Vector Board 3
Vector Board 4
CD 4050
SN 7408
SN 74185
SN 5446
300 Ω
7 Segment Displays



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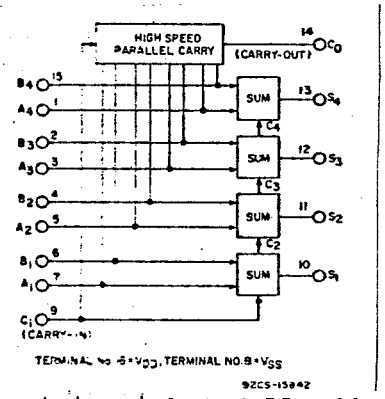
A VOLTAGE MONITORING DEVICE

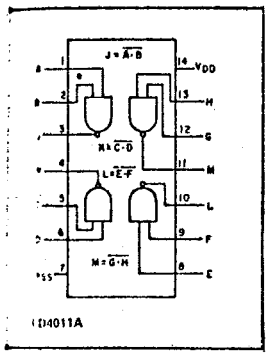
PAGE 2

DWG. D-6227-B | REV. | PROJ. 77909

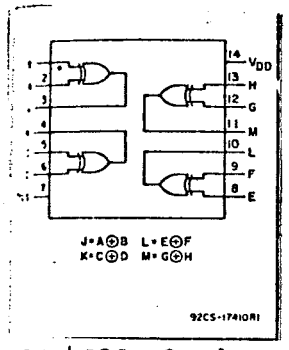
Appendix II



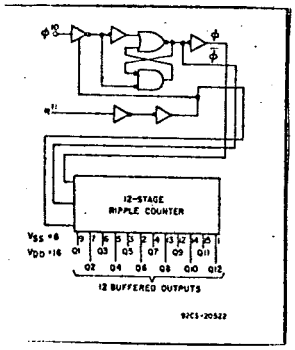
CD 4040, 4 bit full adder



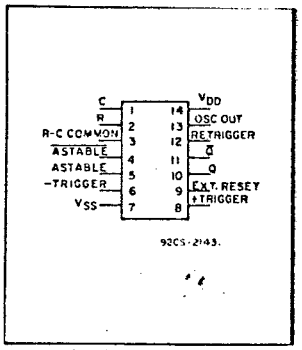
CD 4011, Quad Nand Gate



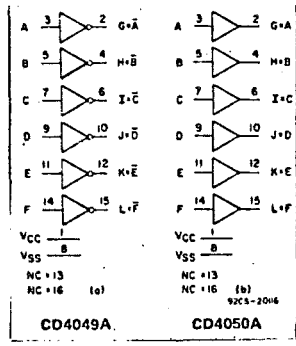
CD 4030, Quad Exclusive Or Gate



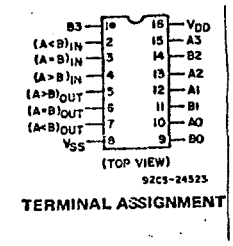
CD 4040, 12 Bit Counter



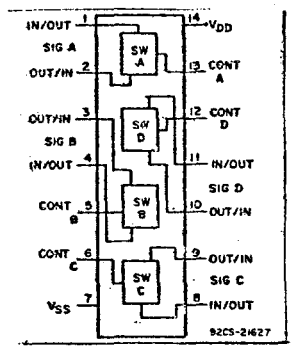
CD 4047, Monostable/ Astable Multivibrator



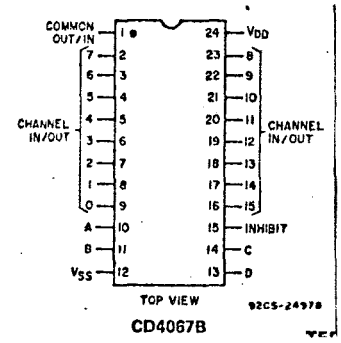
CD 4050, Hex Buffer



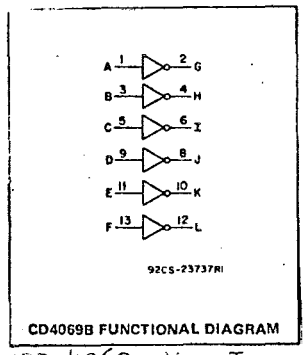
CD 4063, 4 Bit Comparator



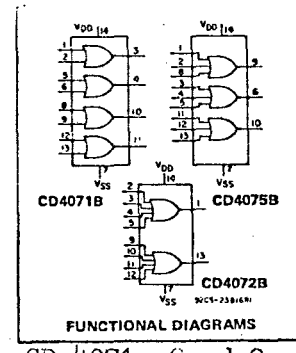
CD 4066, Quad Analog Switch



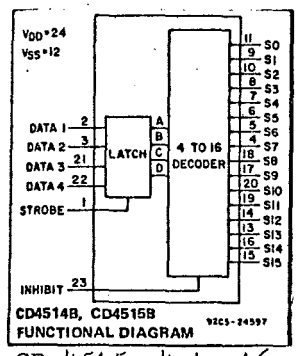
CD 4067, 16 Channel Multiplexer



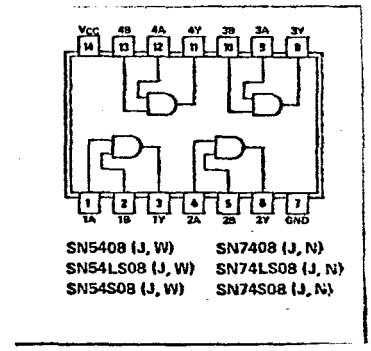
CD 4069, Hex Inverter



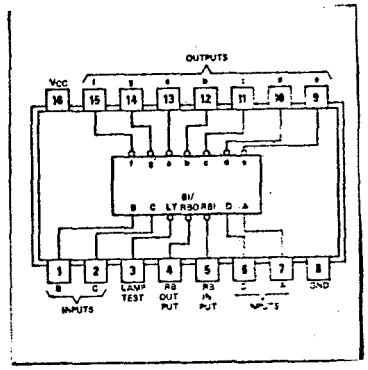
CD 4071, Quad Or Gate



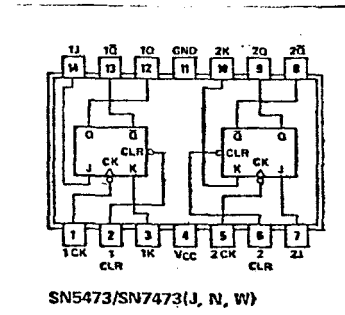
CD 4515, 4 to 16
Line Decoder



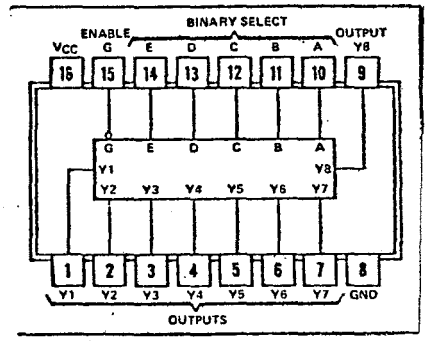
SN 7408, Quad And Gate



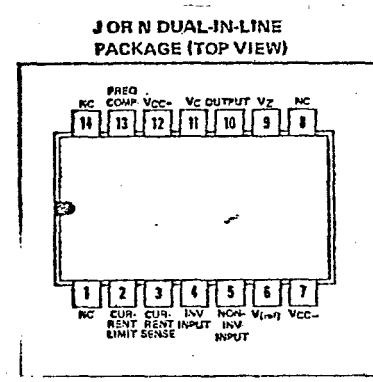
SN 7446, BCD to 7
Segment Decoder/Driver



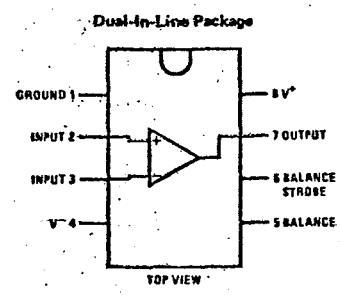
SN 7473, J-K Flip Flop



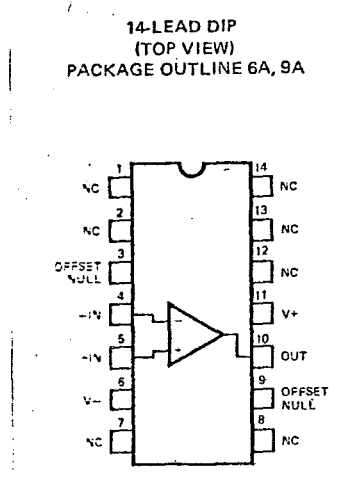
SN 74185, Binary to BCD
Converter



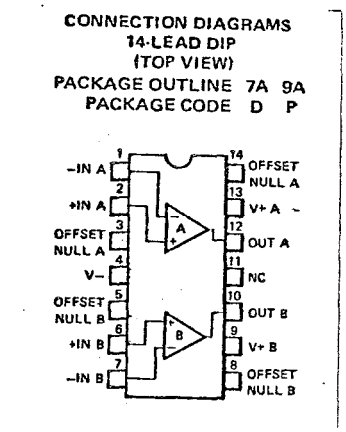
SN 72723, Precision
Voltage Regulator



LM 311, Voltage Comparator



μA 741, Op-Amp



μA 747, Dual Op-Amp