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Vertically Integrated Edgeless Photon Imaging Camera

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Abstract: The Vertically Integrated Photon Imaging Chip - Large, (VIPIC-L), is a large area, small pixel (65µm), 3D integrated, photon counting ASIC with zero-suppressed or full frame dead-time-less data readout. It features data throughput of 14.4 Gbps per chip with a full frame readout speed of 56kframes/s in the imaging mode. VIPIC-L contain 192 x 192 pixel array and the total size of the chip is 1.248cm x 1.248cm with only a 5µm periphery. It contains about 120M transistors. A 1.3M pixel camera module will be developed by arranging a 6 x 6 array of 3D VIPIC-L's bonded to a large area silicon sensor on the analog side and to a readout board on the digital side. The readout board hosts a bank of FPGA's, one per VIPIC-L to allow processing of up to 0.7 Tbps of raw data produced by the camera.

Keywords: Stacked Imagers, low noise analog front-end, camera system.

1. Introduction

A prototype vertically integrated photon imaging readout integrated circuit (VIPIC1) was designed for X-ray Photon Correlation Spectroscopy experiments at synchrotron radiation sources [[i]]. This pixel detector utilized 3D stacking technology with both the Cu-Cu thermo-compression [[ii]] and the Cu DBI [[iii]] bonding which yielded operational devices. The ROICs with a pixel pitch of 80 µm were bonded to silicon pixelated sensors with the measured noise corresponding to 39 e- and 70 e-, respectively for the readout channels that were not connected and connected to the sensor diodes. The conversion gain varied from 43 to 52 µV/e- as a function of the bias current in the front-end block. Essentially all the pixels on a small prototype were operational [[iv]]. The next step in this development process aims at creating a large camera module as shown in Figure 1, with an array of large area (> 1cm^2), small pixel (65µm) 3D bonded pixelated ROICs connected to a large area pixelated sensor on one end and a readout board on the other end. The aim of the development is to create a large area, gapless camera module.

The Vertically Integrated Photon Imaging Chip- Large (VIPIC-L) is a large area, edgeless, vertically integrated analog and a digital 3D stacked ROIC.

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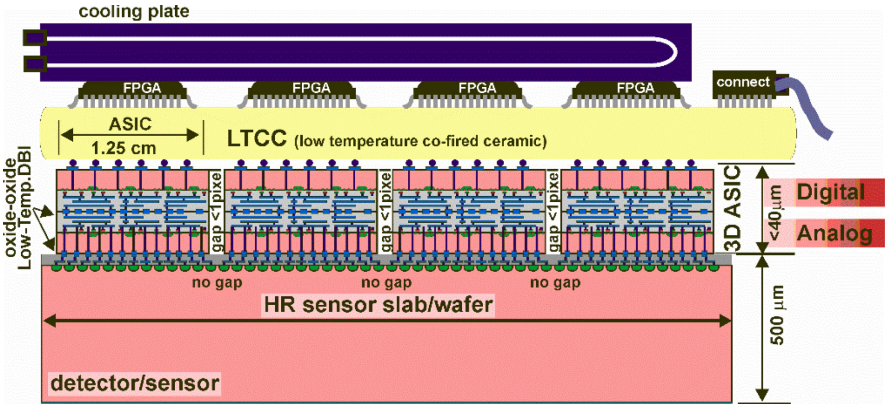

Figure 1. Single module of 3D integrated edgeless camera

2. VIPIC Analog Tier

A full custom analog pixel is connected to a sensor pixel of the same size on one side, and on the other side it has approximately 40 connections to the digital pixel. Each pixel in the analog tier contains a signal processing chain which includes a charge sensitive amplifier with sensor leakage current compensation, followed by a two stage shaping filter and a window discriminator. Additionally, two 7-bit trimming Digital to Analog Converters (DAC) are used to remove systematic offsets in the comparators in every pixel as shown in Figure 2. The VIPIC-L has no peripheral functional blocks, and hence the active area extends to the edge of the detector.

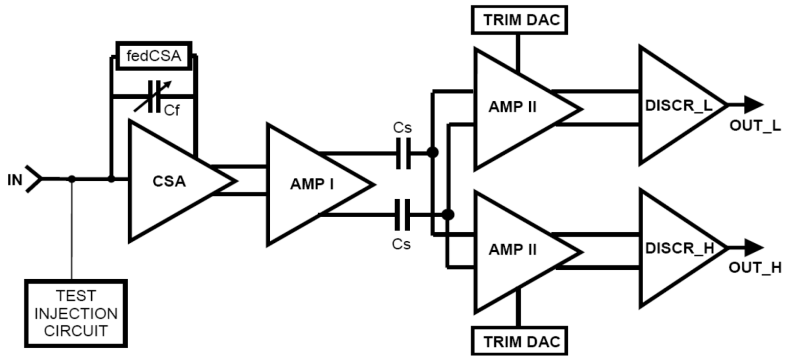

Figure 2 Analog Pixel Block diagram

3. VIPIC Digital Tier

The Digital ASIC consists of approximately 100 million transistors and 1.5 million inter-tier connections to the Analog ASIC. The ASIC is subdivided into a 6 x 6 array of an indivisible functional unit (sub-chip) [Y]. A sub-chip is a grouping of 1024 pixels, which allows for adequate area to contain the hit processing logic of all the pixels along with a priority encoder, an output serializer, LVDS drivers and receivers, as well as a 21,510-bit serial configuration register for trimming and setup of the analog pixels as shown in Figure 3.

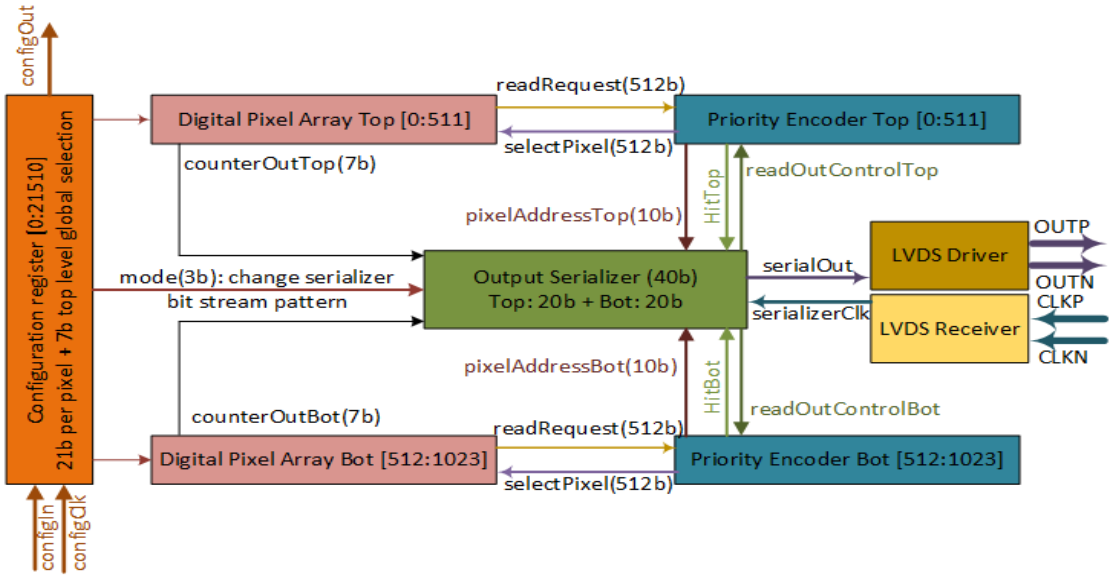

Figure 3. Digital sub-chip functionality

4. VIPIC Readout Board

Each ASIC has 720 bump-bond I/O connections, on the back of the digital tier to the ceramic PCB. All the analog tier power and biasing is conveyed through the digital tier from the PCB. The detector module is a composite of three rafts, each raft containing a 2 x 6 array of VIPIC-L chips bonded to a monolithic p-in-n diode pixel array as shown in Figure 4. Each VIPIC chip has 36 LVDS readout ports. Routing 36 x 12 such signals off the raft is not practical hence each VIPIC chip has a small FPGA to serve as a data concentrator, reducing the wiring to 12 high-speed serial links. Since significant power dissipation is anticipated, a water-cooled copper block is added which is thermally connected to the FPGA packages.

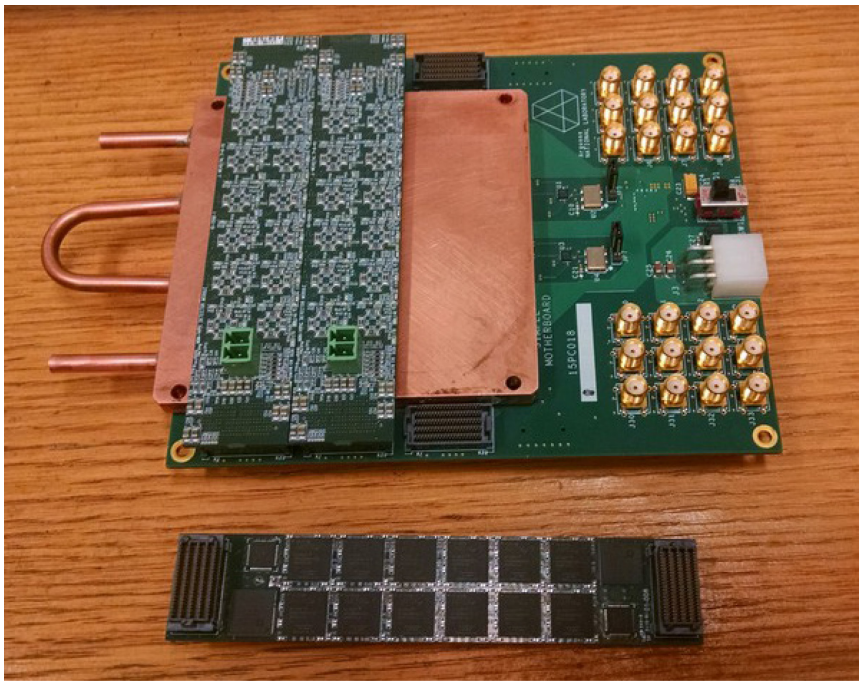

Figure 4. Module test board with 3 rafts each containing 2 x 6 array of VIPIC-L

5. Conclusions

The ROICs have been manufactured in GF130nm process and the 3D stacking process is currently underway.

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