

# Cryogenic Lifetime Studies of 130 nm and 65 nm CMOS Technologies for High-Energy Physics Experiments

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**Abstract**— The Long Baseline Neutrino Facility intends to use unprecedented volumes of liquid argon to fill a time projection chamber in an underground facility. Research is under way to place the electronics inside the cryostat. For reasons of efficiency and economics, the lifetimes of these circuits must be well in excess of 20 years. The principle mechanism for lifetime degradation of MOSFET devices and circuits operating at cryogenic temperatures is hot carrier degradation. Choosing a process technology that is, as much as possible, immune to such degradation and developing design techniques to avoid exposure to such damage are the goals. This requires careful investigation and a basic understanding of the mechanisms that underlie hot carrier degradation and the secondary effects they cause in circuits. In this work, commercially available 130 nm and 65 nm nMOS transistors operating at cryogenic temperatures are investigated. The results show that both technologies achieve the lifetimes required by the experiment. Minimal design changes are necessary in the case of the 130 nm process and no changes whatsoever are necessary for the 65 nm process.

**Index Terms**—Cryogenic electronics, degradation, hot-carrier degradation, MOSFET

## I. INTRODUCTION

The Long Baseline Neutrino Facility (LBNF) [1] will use a large, multi-kiloton volume of liquid argon to detect interactions from the world's highest-intensity neutrino beam after it has passed through 800 miles of the Earth's mantle. To increase the performance of readout electronics, investigations have been launched into the placement of those electronics inside the cryostat. Due to the scale and cost associated with evacuating and filling the cryostat, any electronics inside the cryostat must be deemed unserviceable for the duration of the experiment. Therefore, the lifetimes of these circuits must be in excess of 20 years.

The obvious advantage to placing the readout electronics inside the cryostat is to minimize the input capacitance of any

front-end amplifiers and thereby minimize noise [2]. Beyond that, there are considerable advantages to cryogenic operation because it is well known that low temperatures improve all aspects of device performance such as speed, noise, and current drive [3]-[5]. Unfortunately, early research declared that cryogenic operation may dramatically reduce device and circuit lifetimes [6], [7]. More recent studies, however, suggest that the evolution of CMOS technology and, in particular, the continued reduction in operating voltage is minimizing the significance of operating temperature on device lifetimes [8]-[10]. This paper is a continuation of that research in a CMOS 130 nm technology. More importantly, since the stated intention of the High Energy Physics VLSI community is to work in 65 nm in the foreseeable future [11]-[13], lifetime studies are extended to this technology as well.

It is commonly known that most failure mechanisms in transistors (electromigration, stress migration, time-dependent dielectric breakdown, and thermal cycling) are highly temperature dependent and become negligible at cryogenic temperatures [14]. The exception is hot carrier degradation. Hot carriers are energetic electrons and holes with higher effective temperatures than the carriers in the surrounding lattice [14]-[17]. Their higher energy is generated in and by the electric field *near the drain* assisted by Electron-Electron Scattering in modern field-effect transistors (FET) [10]. Hot carriers arise at all temperatures whenever electric fields accelerate electrons or holes to sufficient kinetic energies to approach or overcome potential barriers at the Si/SiO<sub>2</sub> interface, resulting in trapped charges or broken bonds and interface states. The increase in charge at both the Si/SiO<sub>2</sub> interface and deeper in the oxide alters the device threshold voltage  $V_{TH}$  causing it to increase after stress. This is generally the case for both nMOS and pMOS transistors, though the physical mechanism causing the increase is different [16], [17]. This paper will deal exclusively with degradation in nMOS transistors because nMOS transistors are considered to be much more susceptible to hot carrier degradation.

The goal of this work is to predict a degree of degradation after 5, 10, or 20 years of operation in a cold environment and to develop guidelines for future cryogenic integrated circuit design. Section II briefly covers the effects of hot carrier degradation as well as the effect of cryogenic temperatures on transistors themselves. Section III details the experimental procedures used in this work. Section IV lists the

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experimental results and makes the lifetime predictions. Finally Section V presents the conclusions.

## II. HOT CARRIERS AND CRYOGENIC EFFECTS

### A. Cryogenic Temperature and Its Effect on nMOS Transistor Performance

With reduction in temperature comes a reduction in lattice vibration and, consequently phonon scattering [14]-[16]. This results in a substantial improvement in carrier mobility and a reduction in thermal noise. The improved mobility results in an increase in current drive capability for a given bias and improved transconductance. Another consequence of reduced temperature is an increase in the subthreshold slope and a reduction in drain-source leakage current when the device is off, resulting in improved switching times and lower power dissipation. Finally, threshold voltage increases, largely due to the temperature dependence of the intrinsic carrier concentration.

Unfortunately, the reduction in lattice vibration also results in a higher carrier mean-free path and, consequently, higher carrier kinetic energies. With higher average kinetic energies comes the higher probability of hot carrier generation and the possibility of increased hot carrier degradation.

### B. Hot Carrier Degradation and Its Effects on nMOS Transistor Performance

Due to the localized generation of hot carriers in high electric fields, the Si/SiO<sub>2</sub> damage is not uniformly distributed across the channel. It is located *near the drain*. Hot electrons with enough energy can damage the Si/SiO<sub>2</sub> interface itself causing interface traps that can exchange charge with the channel [13], [17]. Alternatively, carriers with enough energy to actually overcome the Si/SiO<sub>2</sub> barrier can travel deeper into the oxide causing electron traps that can influence the channel but not necessarily exchange charge with the channel. Finally, energetic carriers can travel through the oxide completely as gate current. Which alternative is followed depends on a number of factors, including the Si/SiO<sub>2</sub> barrier activation energy, oxide thickness and transistor biasing.

The trapped charges increase threshold voltage. The interface traps decrease carrier mobility. Together, the change in threshold voltage and the change in mobility have a measurable effect on channel transconductance and drain current. Eventually, this can lead device or system failure, especially in sensitive analog front ends or time-sensitive digital networks.

## III. EXPERIMENTAL PROCEDURE

Generally speaking, the tests followed the classic format of rigidly timed stress periods alternating with stress-free measurement periods as shown by the flowchart in Fig. 1. Stressing means the exposure of the device to voltages that exceed the ordinary limits of the process. Stressing results in the same type of damage that occurs under ordinary operation, but it occurs much more rapidly. It is assumed in this type of experiment that no quantifiable damage occurs during the stress-free measurement period and that degradation damage accumulates in the device, i.e. the damage does not repair itself. The experiment continues, alternating stress and

measurement periods until the end-of-experiment goal is reached (e.g. stress for a certain time or stress until a certain transconductance degradation is reached, etc.) At each measurement period, the  $I_{DS}$  versus  $V_{GS}$  curve is measured with a fixed  $V_{DS}$ , typically 50 mV, and stored. Final data analysis after the experiment quantizes the degradation as drain current degradation:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{I_{DS}(T) - I_{DS}(max)}{I_{DS}(max)}, \quad (1)$$

peak transconductance degradation:

$$\frac{\Delta g_m}{g_m} = \frac{g_m(T) - g_m(max)}{g_m(max)}, \quad (2)$$

and threshold voltage shift:

$$\Delta V_{TH} = V_{TH}(T) - V_{TH}(max) \quad (3)$$

In all three equations, T represents the aggregate stress time at each measurement step and  $I_{DS}(max)$  and  $g_m(max)$  represent the initial, maximum drain current and peak transconductance, respectively.

The ultimate goal of these experiments is the prediction of lifetime and the establishment of guidelines for circuit designers. Lifetime ( $\tau$ ) is the time required to take a device from a virgin state to one of the defined end-of-life definitions. End-of-life has been arbitrarily defined as either a 10% reduction in transconductance or 10% reduction in drain current or a 50 mV increase of threshold voltage. Lifetime prediction via stress experimentation is accomplished by plotting the log of lifetime versus  $1/V_{DS}(stress)$ , determining the rate-of-change of lifetime with inverse stress voltage and then extrapolating that slope to a lifetime of 20 years. This method is correct as long as the degradation follows a power law and recent work has shown that degradation is always a power law even down to deep submicron processes [26]. The stress voltage that corresponds to a desired lifetime represents an upper limit of possible power supplies for the circuitry. In other words, if the voltage corresponding to a lifetime of 20 years is 1 V, then the maximum positive power supply that can be used in CMOS circuit design is 1 V.

In previous lifetime tests [8][9], a simple liquid nitrogen bath was used to keep the stressed devices at cryogenic temperatures. This technique, while simple and effective, has practical limitations. Most notably, the liquid nitrogen bath evaporates steadily and this limits reproducible tests to approximately 10k seconds. Consequently, stressing at high-voltage (substantially exceeding the nominal power supply limit) was typically necessary to achieve the stress/lifetime goals. Under non-stressed conditions and in modern VLSI processes, the electric fields are insufficient to energize charge carriers to cause hot carrier degradation without the assistance of Electron-Electron Scattering [10]. However, under very high stress, it is possible to impart the 3.7 eV necessary to directly cause interface states with simple electric field acceleration. Such high stresses could adversely affect the

data gathered. Therefore, to increase the possible stress times and decrease the required stress voltages, the tests were performed using a custom-built, vacuum-insulated cryostat with a Cryomech PT60 Single-Stage Pulse Tube Cryocooler. The system is capable of cooling a copper plate on which the device under test was placed to a minimum of 60 K. The system also has a DC heater, which is controlled by a feedback network that reads the cold-plate temperature via a 100  $\Omega$  platinum resistance-temperature detector (RTD) and cycles the heater on and off to achieve and maintain the set-point temperature. Any temperature between 60 K and 300 K can be set. A National Instruments (NI) PXIe-8135 embedded controller with two sets of PXIe-4141 and one set of PXIe-4145 (precision Source Measurement Units (SMUs)) are used to control power supplies and measure the drain, gate, and substrate currents of the devices under test. Each PXIe-4141 and PXIe-4145 has four programmable (SMU), giving a total of 12 SMUs available for testing.

Custom LabView programs control the experiment and record the data. During stress periods the program set gate-source voltages to either the full drain-source voltage ( $V_{DS}$ ) or one half of the drain voltage ( $V_{DS}/2$ ) as required by the particular experiment being performed. All measurements of  $g_m$  were conducted in the linear region with  $V_{DS}=50$  mV or  $V_{DS}=100$  mV. This ensures that charges crossing the channel experience the maximum effect of the damaged region [19]. If higher  $V_{DS}$  voltages were used, the device would move into saturation, current would be injected across the pinched-off region, and carriers would not fully experience the conditions of the damaged region.

The peak value of small-signal transconductance is used as a monitor of hot-carrier degradation in real-time. It is determined by a numerical differentiation of the device's  $I_{DS}$  versus  $V_{GS}$  curve at each  $V_{GS}$ . For speed and simplicity, this differentiation is calculated by a simple numerical procedure during the experiment. Afterwards, to eliminate noise, the transconductance curve is fitted by a 5<sup>th</sup> order polynomial in the vicinity of the coarsely defined peak. This allows calculation of the peak transconductance with the required precision and reproducibility.

Stressing times were varied over the course of each experiment to allow for the possibility of probing quickly developing phenomena early in the experiment, while at the same time minimizing the loop duty cycle over long

TABLE I  
PROGRESSION OF STRESS TIMES OVER THE COURSE OF EACH SINGLE EXPERIMENT

Period Number	Period Duration (s)	Total Time (s)
1-10	1	0-10
11-20	2	10-30
21-30	5	30-180
31-40	10	80-180
41-50	20	180-380
51-60	50	380-880
61-70	100	880-1880
71-80	200	1880-3880
81-90	500	3880-8880
>91	1000	>8880

experiments. The stress periods progressed in a programmed pseudo-logarithmic fashion as shown in Table 1.

An additional modification to the testing procedures in this paper is the rigorous use of 4-point sensing. The integrated circuit test structures were specifically designed to allow sensing of the source and drain voltages in addition to the typical, required source and drain connections. Fig. 2 shows the 4-point connections for a single transistor controlled by three independent SMUs. Each SMU has four connections, H, Hs, L and Ls. H and L are low impedance, high current connections. Hs and Ls are high impedance, low current connections. H and L provide the positive (H) and negative (L) terminals of a voltage source. Hs and Ls are used to sense the voltage values supplied by H and L, respectively, along an independent path and as close as possible to the transistors themselves. The purpose of these sense lines is to read the actual voltage applied at the device under test. It is not uncommon for large devices to flow hundreds of milliamps of current during stressing. A few ohms of parasitic resistance in the traces between the device under test and the SMUs could significantly affect the accuracy of the experiments. The Hs and Ls sense lines in the four point sensing ensure that the requested stress voltages are actually applied at the transistor terminals.

In these transistor experiments, the L connections of all three SMUs are connected together, providing the local ground of the experiment. SMU1 provides the substrate connection. Since little substrate current will flow, sense leads are not necessary here. H and L of SMU2 in Fig. 2 provides the  $V_{DS}$  voltage for the experiment. The Hs and Ls sense lines of SMU2 ensure the accuracy of the high current drain-source voltage. Finally, SMU3 provides  $V_{GS}$ . Again, since little current will flow through the gate, no sense lines are used here either.

#### IV. EXPERIMENTAL RESULTS

The test transistors were fabricated in two technologies: a low-power version of a 1.2 V, 65 nm bulk CMOS process and a 1.5 V, 130 nm bulk CMOS process. The transistor sizes available for experimentation in the 65 nm technology are: widths of 25  $\mu\text{m}$ , 10  $\mu\text{m}$ , 5  $\mu\text{m}$ , 2.5  $\mu\text{m}$ , 1  $\mu\text{m}$ , and 0.5  $\mu\text{m}$  and lengths of 0.06  $\mu\text{m}$ , 0.1  $\mu\text{m}$  and 0.2  $\mu\text{m}$ . The transistor sizes available for experimentation in the 130 nm technology are: widths of 50  $\mu\text{m}$ , 20  $\mu\text{m}$ , 10  $\mu\text{m}$ , 5  $\mu\text{m}$ , 2  $\mu\text{m}$ , and 1  $\mu\text{m}$  and lengths of 0.13  $\mu\text{m}$ , 0.2  $\mu\text{m}$  and 0.4  $\mu\text{m}$ .

##### A. Worst-Case Stress Conditions

Hot-carrier degradation has traditionally been evaluated under  $V_{GS}=V_{DS}/2$  as the worst-case stress condition [8][20][21]. However, dependences of the worst-case stress condition on channel length, drain bias and temperature have been observed [3][22].  $V_{GS}=V_{DS}$  has been declared a worst-case condition for shorter channel length transistors at low temperature [3]. This has been attributed to the dependence of the electron density near the drain on the applied  $V_{GS}$  [10]. In particular, as  $V_{GS}$  increases the peak electron concentration near the drain moves from the bulk Si closer to the Si/SiO<sub>2</sub> interface. The higher concentration of electrons near the drain means that there is an increase in Electron-Electron Scattering

in this region and, since this region is now close to the interface, the distance necessary for a charge carrier to travel without re-scattering is much smaller. So, for short channel devices,  $V_{GS}=V_{DS}$  should display more hot carrier degradation than  $V_{GS}=V_{DS}/2$ .

In this work, the stress conditions of both the  $V_{GS}=V_{DS}$  and  $V_{GS}=V_{DS}/2$  are investigated on different sizes of transistors and in both technologies. Fig. 3 shows the drain current degradation at  $V_{GS}=V_{DS}=2.4$  V and  $V_{GS}=V_{DS}/2=1.2$  V for transistors of  $W/L=2$   $\mu\text{m}/0.13$   $\mu\text{m}$ ,  $W/L=2$   $\mu\text{m}/0.2$   $\mu\text{m}$  and  $W/L=2$   $\mu\text{m}/0.4$   $\mu\text{m}$  in the 130 nm process. At short channel length,  $V_{GS}=V_{DS}$  clearly degrades more rapidly than  $V_{GS}=V_{DS}/2$ . In Fig. 3(a), for the same stress time, the  $V_{GS}=V_{DS}$  curve has a higher value than the  $V_{GS}=V_{DS}/2$  curve. At slightly longer length, i.e. Fig. 3(b),  $V_{GS}=V_{DS}$  and  $V_{GS}=V_{DS}/2$  are not very different. Finally, at the longest length, the  $V_{GS}=V_{DS}/2$  curve is higher than the  $V_{GS}=V_{DS}$  curve indicating that the long channel devices degrade more rapidly under the  $V_{GS}=V_{DS}/2$  condition. The same observations are obtained from transconductance and threshold voltage degradations which, for reasons of brevity, are not presented here. The results of these transconductance and threshold voltage degradation measurements are used for lifetime predictions and are presented hereafter.

Fig. 4 shows the drain current degradation at  $V_{GS}=V_{DS}=1.8$  V and  $V_{GS}=V_{DS}/2=0.9$  V for transistors of  $W/L=10$   $\mu\text{m}/0.06$   $\mu\text{m}$ ,  $W/L=10$   $\mu\text{m}/0.1$   $\mu\text{m}$  and  $W/L=10$   $\mu\text{m}/0.2$   $\mu\text{m}$  in the 65 nm process. The worst-case stress condition remains  $V_{GS}=V_{DS}$  for all three different channel lengths. However, the trend in Fig. 4 is similar to that in Fig. 3. While  $V_{GS}=V_{DS}$  is clearly the worst-case condition, it is less and less dominant as channel length increases. Intuitively, it is expected that  $V_{GS}=V_{DS}/2$  would become the worst-case stress condition in the 65 nm technology if the channel length is permitted to increase beyond 0.2  $\mu\text{m}$ . However, it was not possible to test this speculation because no test transistors were available with channel lengths longer than 0.2  $\mu\text{m}$  in the 65 nm process.

### B. Width Dependence

The hot-carrier degradation dependence on the transistor width was observed in [9] and [23] and this width dependence has been shown to result from non-uniformity of the channel across the channel width. Moreover, hot-carrier degradation dependence on the transistor width has been observed to change with temperature [9]. At cryogenic temperatures, the width dependence was found to be insignificant.

The degradations of transistors with different widths at 77 K are investigated. Fig. 5 (a) and (b) show the drain current degradations measured in the linear region versus stress time for transistors with six different widths at 77 K in the 130 nm and 65 nm technologies, respectively. It can be concluded that the drain current degradations of transistors with different widths are close to each other and width dependence is negligible at 77 K.

### C. Lifetime Predictions

There is no absolute definition of lifetime. No event or phenomenon signals an actual and definitive end of life for a

device. Rather, lifetime and end of life are defined in a manner acceptable to the experimenter. In this work, the drain current, threshold voltage, and transconductance are employed as the monitors of performance and for each monitor a definition of end of life is defined (10% drain current degradation, 10% transconductance degradation, and 50 mV threshold voltage shift). The lifetimes as determined by these different monitors may be different for the same transistor. However, since all of them are caused by the same mechanism the lifetime extrapolation curves have the same slopes [20].

Fig. 6(a) shows the lifetime extrapolation curves for a 2  $\mu\text{m}/0.13$   $\mu\text{m}$  transistor in the 130 nm technology. This transistor was chosen as representative of all the short-channel transistors tested. Fig. 3 demonstrates that lifetime increases with increasing length [8]. Fig. 5 demonstrates that lifetime at cryogenic temperature is unaffected by transistor width. Obviously, the slopes of all the lifetime measurements are virtually identical. The uniformity of slope holds true even for changes in stress condition from  $V_{GS}=V_{DS}$  to  $V_{GS}=V_{DS}/2$ . The uniformity of slope confirms that the degradation mechanism remains the same regardless of stress condition.  $V_{GS}=V_{DS}$  is simply the worst-case condition for the same hot carrier degradation. To meet the 20 year lifetime requirement of the LBNF experiment, drain voltages should be reduced to 1.49 V which is an almost negligible change from the 1.5V nominal voltage recommended for the process.

Fig. 6(b) shows the lifetime extrapolation curves for a 10  $\mu\text{m}/0.06$   $\mu\text{m}$  transistor in the 65 nm technology. In this figure, only the  $V_{GS}=V_{DS}$  curves are shown. To meet the 20 year lifetime requirement of the LBNF experiment, drain voltages should be kept below to 1.3 V but since the 65 nm technology is a 1.2 V process, this represents no restriction at all. Designers may choose to decrease the power supply rails as an additional precaution. However, these experiments indicate that this is not a requirement.

## V. CONCLUSIONS

The results confirm earlier work that states that  $V_{GS}=V_{DS}$  is the worst case stress condition for short channel devices. Moreover, at cryogenic temperatures, width dependence is negligible. The predicted lifetime for 130 nm devices reaches 20 years provided the drain voltages are reduced from the nominal, room temperature value of 1.5 V to a cryogenic temperature value of 1.49 V. As noteworthy as this prediction is, the 65 nm device is even more resistant to cryogenic hot carrier degradation. Its nominal, room temperature voltage of 1.2 V is already lower than the maximum allowable cryogenic temperature voltage of 1.3 V.

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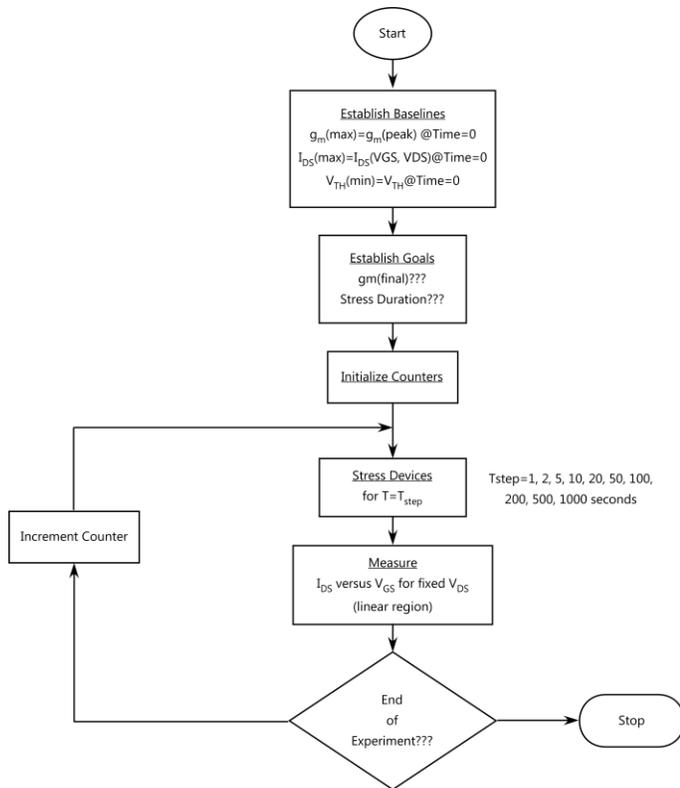


Fig. 1. The flowchart for the experimental procedure. First, baseline drain current, small-signal transconductance peak, and threshold voltage are established. Second, degradation level goals are established. Goals could be to degrade the transconductance peak by a certain percentage or to simply run the experiment for a certain total stress time. Finally, a loop is started in which the device under test is stressed and then measured and tested for end of experiment. Each measurement is stored for later analysis. If the end of experiment has been reached, the experiment is ended. Otherwise, the loop continues.

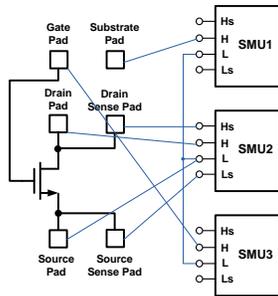


Fig. 2. Schematic of the experimental setup of a transistor and a 4-point sensing structure.

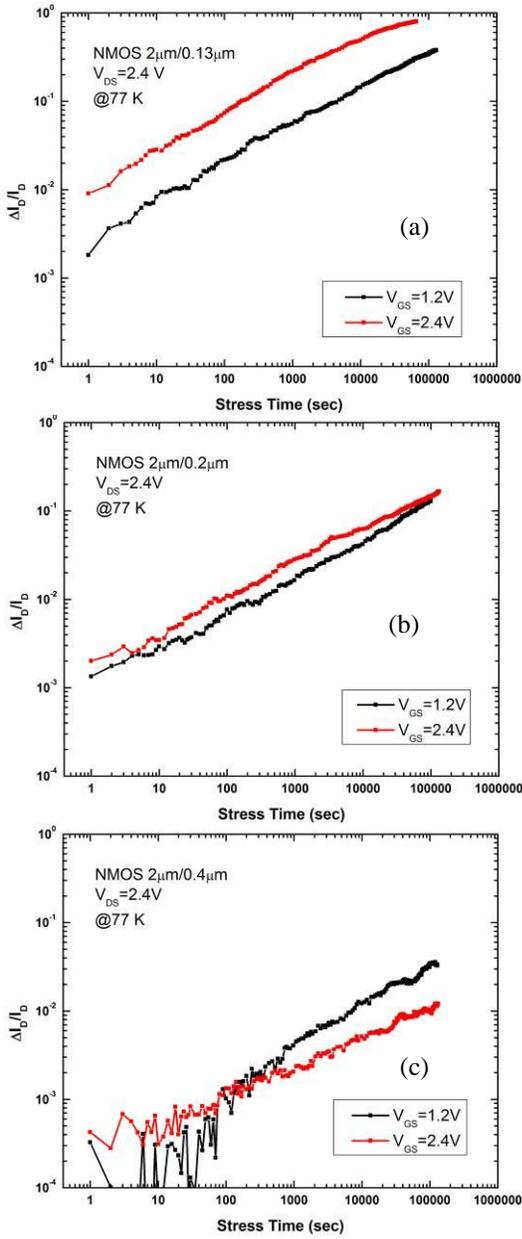


Fig. 3. Normalized change in drain current with stress time at 77 K for transistors with different lengths: (a) 2  $\mu\text{m}/0.13 \mu\text{m}$ , (b) 2  $\mu\text{m}/0.2 \mu\text{m}$ , (c) 2  $\mu\text{m}/0.4 \mu\text{m}$  at stress conditions of  $V_{GS}=V_{DS}=2.4 \text{ V}$  and  $V_{GS}=(1/2)V_{DS}=1.2 \text{ V}$ .

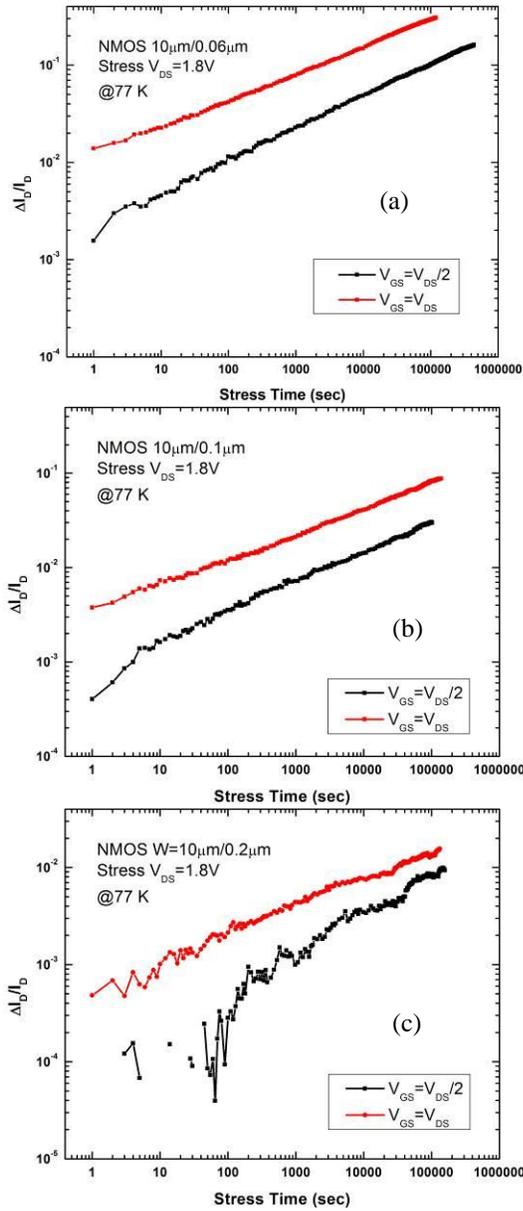


Fig. 4. Normalized change in drain current with stress time at 77 K for transistors with different lengths: (a)  $10\mu\text{m}/0.06\mu\text{m}$ , (b)  $10\mu\text{m}/0.1\mu\text{m}$ , (c)  $10\mu\text{m}/0.2\mu\text{m}$  at stress conditions of  $V_{GS} = V_{DS} = 1.8$  V and  $V_{GS} = (1/2)V_{DS} = 0.9$  V.

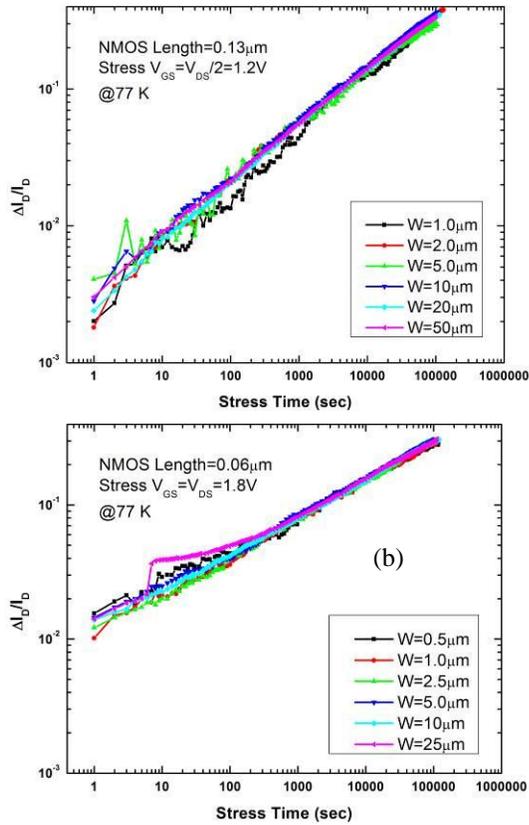


Fig. 5. Normalized change in drain current with stress time at 77 K for transistors with different widths: (a) 130 nm technology, (b) 65 nm technology. The 20  $\mu\text{m}/0.13\mu\text{m}$  and 50  $\mu\text{m}/0.13\mu\text{m}$  transistors in 130 nm technology have 2 and 5 fingers, respectively, The 10  $\mu\text{m}/0.06\mu\text{m}$  and 25  $\mu\text{m}/0.06\mu\text{m}$  transistors in 65 nm technology, likewise, have 2 and 5 fingers, respectively.

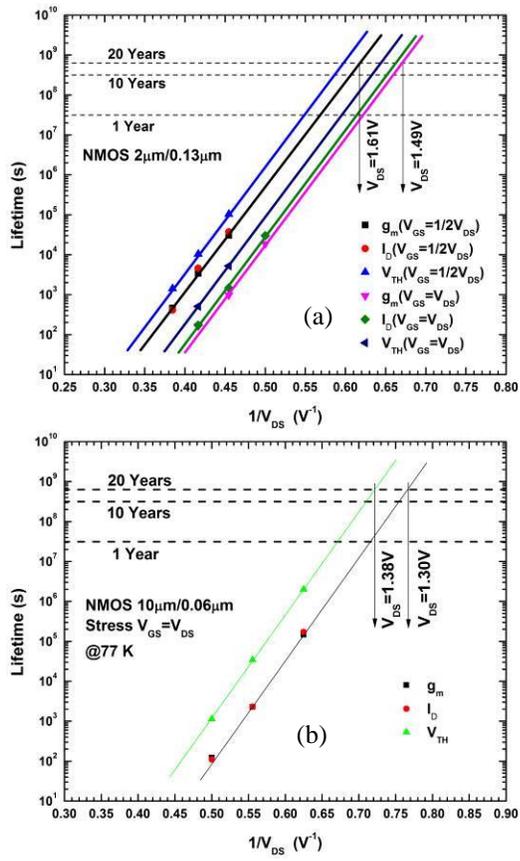


Fig. 6 Preliminary lifetime predictions for the 2 µm/0.13 µm and 10 µm/0.06 µm transistors at 77K by degradation of  $g_m$  and  $I_{DS}$  and by increase of  $V_{TH}$ .