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Fully 3D-Integrated Pixel Detectors for X-Rays

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***Abstract*– The VIPIC1 pixel detector is a stack consisting of a 500 μm thick silicon sensor, a two-tier, 34 μm-thick integrated circuit, and a host printed circuit board. The integrated circuit tiers were bonded using the Cu-DBI® technology and each tier features 1 μm diameter through silicon vias that were used for connections to the sensor on one side, and to the host printed circuit board on the other side. The 80 μm-pixel-pitch sensor was Ni-DBI® bonded to the integrated circuit. The stack was mounted on the board using Sn-Pb balls placed on a 320 μm pitch, yielding an entirely wire-bond-less structure. The analog front-end features a pulse response peaking at below 250 ns and the power consumption per pixel is 25 μW. A successful completion of the 3D integration is reported. Also all pixels in the matrix of 64×64 pixels were responding on well bonded devices. Correct operation of the sparsified readout, allowing single 153 ns bunch timing resolution, was confirmed in the tests on a synchrotron beam of 10 keV X-rays. Equivalent noise charge of 36.2 e^- rms and conversion gain of 69.5 μV/e^- with 2.6 e^- rms and 2.7 μV/e^- rms pixel-to-pixel variations respectively were measured.**

I. Introduction

3D-integration technology is emerging in the industry for the "more than Moore" scale of integration [1]. Whether this can transformationally benefit pixel detectors in High Energy Physics, Photon Science and similar applications has been the subject of much debate [2][3][4]. This paper reports on the use of the ingredients of the 3D-integration technology at various stages to implement a successful detector concept for detection of X-rays. The design presented here has been driven by the specific needs of X-ray Photon Correlation Spectroscopy experiments, which are performed using coherent X-rays at a synchrotron radiation facility [5]. This method allows the study of atomic dynamics at very short time and distance scales through the analysis of the so called "speckle" patterns, resulting from a superposition of many single-particle diffraction patterns, when a coherent beam of X-rays scatters off the atoms, and the atoms are in motion.

Previous attempts to produce 3D stacked, hybrid detectors can be named, e.g. one based on stacking of SOI wafers [6]. However, they in general relied on non-commercial custom processes. The device described here demonstrates the feasibility of the first fully 3D-integrated pixel detector using a commercially available, bulk CMOS process as a cornerstone. The goal for the Vertically Integrated Photon Imaging Chip (VIPIC) detector project is to build a hybrid pixel detector, because this allows an independent optimization of the sensing and readout components, in contrast to monolithic detectors. The device should register incoming photons and provide two-dimensionally resolved position and arrival time information for each photon. The construction details of the fully 3D-integrated detector, based on the first version of the two-tier VIPIC1 chip [7][8], are revealed and the test results obtained are discussed for the first time. The emphasis was, first, on demonstration of a path for building detectors with large-area, maximally free of dead zones, and second, on validation of high integration of functionalities, along with low noise. For both goals it was essential to use a bonding method that yields smallest capacitive load, least cross-talk and having inputs of charge signals and all other connections to the readout integrated circuit (ROIC) on separate sides of the structure.

This paper is organized in 4 sections. The first section is an introduction. A pathway for the fully 3D-integrated VIPIC1 detector is described in the second section. The third section discusses the results of testing. First, the result obtained with a laboratory radioactive ^{55}Fe source are given. Measurements of parameters, like gain and noise of the system are shown and the performances of the devices that were LTD-bonded to sensors are compared with the devices that were solder-bump bonded to sensors. Then, the tests carried out with electrons from a ^{90}Sr laboratory source are presented. Finally, this section addresses dead-time-less detection of mono-energetic X-ray photons and tracking of bunch-to-bunch beam intensity variations at the Argonne National laboratory Advance Photon Source (APS), using the VIPIC1 detector operated with sub-microsecond timing resolution. The last, fourth, section concludes and summarizes the presented material.

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II. Pathway to the Fully 3D-Integrated Detector

The VIPCI1 detector is a stack consisting of a pixelated 500 μm thick silicon sensor, a two-tier ROIC having a total thickness of 34 μm after both side thinning, and a host printed circuit board (PCB). The tiers of the ROIC were bonded together first and the resulting 3D integrated dies were later bonded onto a 80 μm-pixel-pitch sensor using a low temperature direct bonding (LTD-bonding) technology with copper (Cu-DBI®) and nickel (Ni-DBI®), respectively, as metals of the bonding posts [9]. The LTD-bonding technology is based on a complete fusion of the two oxide surfaces with embedded metal connections without external pressure.

Both tiers of the VIPIC1 chip feature small-diameter (1 μm) and short (6 μm) tungsten through silicon vias (TSV) that were embedded after the front-end-of-line steps of the wafer processing and, later, exposed by thinning of the tiers. This translated to connections to the sensor on one side, using the mentioned LTD-bonding, and to the host PCB on the opposite side, using an array of Sn-Pb balls with a 320 μm pitch. Thus, the finished pixel detector was a wire-bond-less structure.

A. Basic Features of the VIPIC1 Chip

The VIPIC1 chip is a small prototype. The size was set by the division of the reticle into 5.5×6.3 mm^2 blocks in the first 3D High Energy Physics Multi-Project-Wafer run [3]. The chip features a matrix of 64×64 pixels, which is divided into 16 groups of 256 pixels, thus each group consists of 4 rows of 64 pixels. The pixel size is 80×80 μm^2 and there are about 280 and 1400 transistors in the analog and digital blocks of a pixel, respectively. The analog front-end circuit features a pulse response peaking at less than 250 ns and analog circuitry power consumption of 25 μW per pixel. A pulse, generated in the front-end circuit due to collection of charge from a photon impact, is fed to a discriminator in every pixel. If the amplitude is higher than a threshold, a flag is set in a pixel and this information is fed to the digital part of the chip. The main feature of the digital part is a sparsification engine that is based on the priority encoder principle. Each group of 256 pixels is served by an independent sparsification circuit, allowing sending off the chip only the binary-coded addresses of pixels that have absorbed photons within each group and the contents of 5-bit long hit counters that record how many times the same pixel was hit successively during an exposure. Implementing photon-by-photon processing makes the VIPIC1 chip a scientific instrument that operates differently from classical imagers [7]. The pixel electronics, feeding the sparsifier, operates as a single stage pipeline. Advancing of the pipeline is synchronous with a clock that defines consecutive time frames (exposures), to which photon arrivals are allocated. There is no readout dead time, i.e. hits in a new time frame are being acquired, while the hits from the previous time frame are being sent off the chip. The expected count readouts should not exceed a few per pixel in typical exposures of up to 10 μs long in the experiments. Thus, the 5-bit length of the counters is largely sufficient. The addresses and the counter contents are passed from the sparsifier to a serializer in each group. The data is output serially through LVDS drivers in parallel from each group.

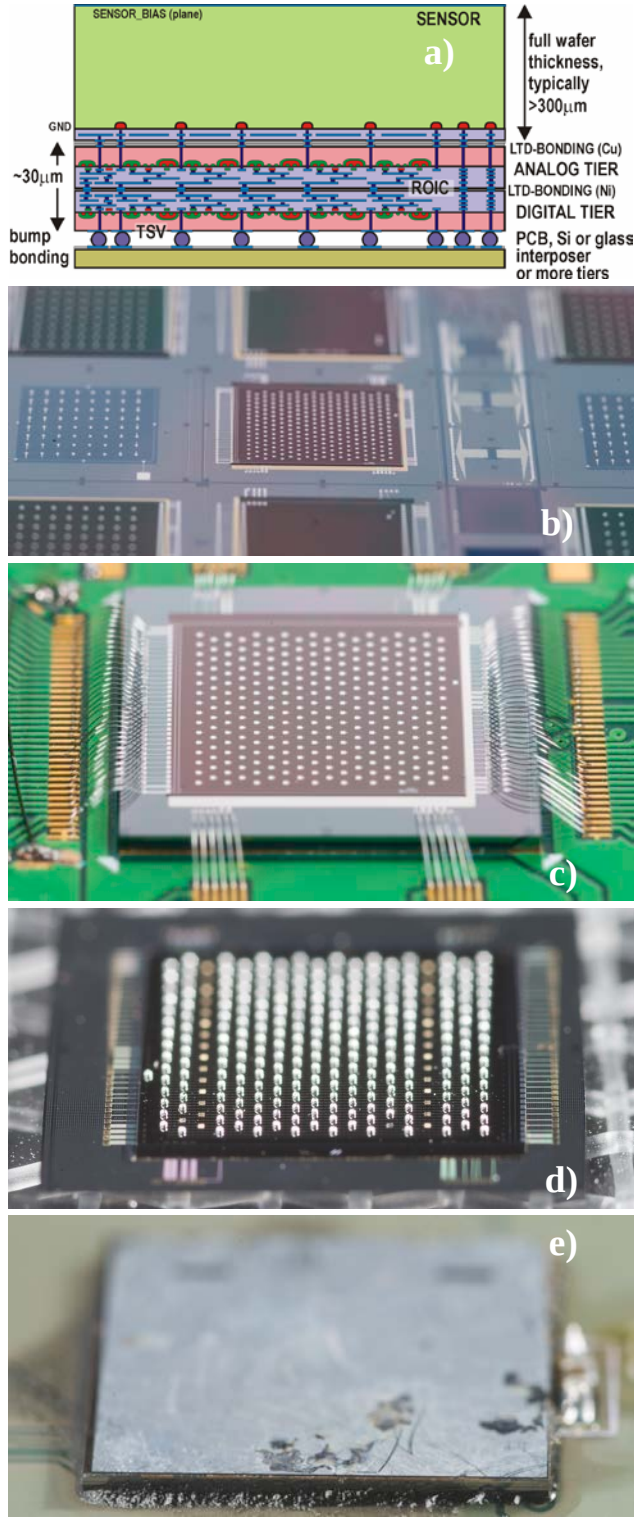

Fig. 1. a) Cartoon of a fully 3D-integrated pixel detector, b) VIPIC1 LTD-bonded on the sensor wafer with back-side bump-bonding pads exposed before wafer dicing, c) VIPIC1 LTD-bonded on the sensor with wire-bonding connections to PCB using traces on the sensor, d) VIPIC1 LTD-bonded to the sensor with bump-bonding Sn-Pb balls deposited on the back, e) VIPIC1 LTD-bonded on the sensor bump-bonded upside down on the precision PCB.

B. The Development Plan and Early Steps

The most complete plan consisted of building a prototype

stacked detector device, whose cartoon form is shown in Fig. 1a. All the work, including the design of the ROIC, carried significant risks because of the pioneering nature of the efforts. Thus, the work was carried out in stages, sometimes requiring developments of new pieces of technology or modifying the existing recipes. Thorough tests were performed at every stage and the results have been previously reported. This included the tests and characterization of the VIPIC1 chip in a configuration without any sensors [7][8][10]. Tests of X-ray detection were performed later on the VIPIC1 chip bump-bonded using solder (Sn-Pb) bumps to small silicon sensors containing arrays of 32×38 pixels [11]. Those tests were possible thanks to the bump-bonding pads that were deposited for VIPIC1 chips on a few 3D-wafer stacks that were pulled out in a processing split. The success of these tests motivated further more complicated steps, leading to the full three-dimensional integration. Also, having the bump-bonded and LTD-bonded versions of the device allowed carrying out direct comparisons of their performances.

C.Fully 3D Stacked Structure and Intermediate Steps

The tiers of the ROIC were bonded using the Cu-DBI® technology, applying the procedure on a wafer-to-wafer basis [12][13]. Eight-inch wafers, manufactured in a 130 nm bulk CMOS process, were bonded together using inter-tier metal posts laid out on a staggered 4 μm, two-dimensional grid. The tight pitch of the inter-tier connections defined stringent requirements on the alignment of bonded wafers that had to be within about 1 μm. This precision had to be maintained across whole wafers; otherwise the devices would not work. It was proven that such an alignment could be achieved and six bonded wafer pairs were successfully produced. Two wafer pairs, each having the bonding pattern suitable for attachment of the small silicon sensors using the bump-bonding technique, were diced immediately for testing. Four remaining wafers were used for building assemblies based on the LTD-bonding to the sensors.

A unique feature of the VIPIC1 chip is the presence of small diameter TSVs in both tiers, as shown in Fig. 1a. Initially, the TSVs were buried when both sides of the bonded pairs of wafers had full thicknesses. Later, thinning exposed the TSVs. When exposed, the TSVs provided connections to the pixel sensor and to the host PCB on the analog and on the digital tier side, respectively. Multiple processing steps, all to be carried out successfully, were required to obtain the proposed 3D-integrated, entirely wire-bond-less detector. Because of building of such an advanced form for the first time, less than perfect yield of each technological step could be expected. Therefore, testing at intermediate stages of the device construction, for example without bump-bonding on the host PCB was mandatory. Such an approach had also an additional value of enabling tests that were not possible otherwise, e.g. comparison of the front to back side illumination using lightly penetrating X-ray photons from a ^{55}Fe source.

Ultimately, the VIPIC1 dies were LTD-bonded to the sensor wafers using the Ni-DBI® technology on a die-to-wafer basis. A VIPIC1 chip, LTD-bonded to one of the sensor wafers, is shown in Fig. 1b. The picture was taken after the back-side bump-bonding pads were exposed but before dicing of the sensor wafer. The total thickness of the VIPIC1 chip is only 34 μm after thinning. Three sensor wafers were populated with the chips. In total, 52 VIPIC1 chips were LTD-bonded to the sensors, where, in 18 cases, sonograms showed no bonding voids. It was however impossible to distinguish at this stage whether visible voids occurred at an earlier bonding of the tiers of ROICs or at bonding to the sensor wafers. Investigations revealed that the connection voids in the LTD-bonded VIPIC1 chips to the sensor wafers was probably the result of imperfect cleaning, leaving particles of photoresist on the surface of the sensor wafers prior to the bonding. Thus, this is easily correctable in future.

For the staged testing, a special adaptation was applied to the sensor structure. It consisted of pads for LTD-bonding connections on the inner side and wire-bonding pads on the outer side of the sensor dies. These extra pads were patterned in addition to a centrally located array of 64×64 pads laid out with the 80 μm pitch, as required for connection of the readout channels to the sensor diodes. The added pads were inter-connected by metal traces routed on the surface of the sensor dies. This allowed access to all the terminals, i.e. power supplies, biases, and analog and digital signals of the chip [3][7]. Having pads outside of the area covered by the readout chips enabled tests using wire bonding first. After wire-bonded assemblies were characterized and proven functional, the bump-bonding of the whole structure proceeded on the host PCB. A VIPIC1 chip, LTD-bonded to the sensor, and mounted on a PCB using wire-bond connections, is shown in Fig. 1c. The size of the sensor piece is 9.25×8.15 mm^2. The PCB had a hole cut in it, allowing illumination of the tested device either from the front side or from the back side.

D. The Sensor Wafer

For sensors, standard six-inch, 500 μm thick, 5 kΩcm resistivity, n-type wafers were chosen. Processing of wafers to build sensor diodes was done at the Brookhaven National Laboratory facility. Fabrication of the sensor wafers included the following front-side steps:

a) implantation of p-type, 40 μm diameter, diode islands,

b) growing of 300 nm thick thermal oxide in which 20 μm diameter via openings to diode implants were cut,

c) deposition of a layer of 300 nm thick Al metallization and patterning to form DC-coupled, 47 μm diameter, conformal contacts to the diodes and a layer of shielding to cover the traces and wire bonding pads that were added later,

d) deposition of a blanket of 1 μm thick PECVD oxide following the metallization.

The sensor wafers also underwent back-side n-type implantation. It was followed by deposition of 300 nm thick layer of Al and by deposition of about 1 μm thick PECVD oxide to compensate wafer bowing and to protect the backside from scratches in the successive processing. The target for the front-side processing of the sensor wafers was to create layers in such a way that the best surface planarity could be obtained. This requirement was essential for LTD-bonding of the readout chips to the sensor wafers. The goal was to keep the topography and the surface roughness not exceeding 100 nm across the whole wafer that was ready for LTD-bonding.

E. Details of the Processing Procedure for Building LTD-Bonded, Monolithic-like Assemblies

The 3D wafer pairs, containing VIPIC1 chips, underwent multistep processing before individual dies became suitable for LTD-bonding onto the sensor wafers. 3D wafer pairs with ROICs had one side (digital-tier side) first thinned down to the level of TSVs. When the TSVs were revealed and isolated by about 1 μm deep recession etch of silicon, a thin, 50 nm, nitride layer was deposited and an isolation oxide was grown on the surface and, after planarization, about 1 μm thick Al pads (100×100 μm^2) were patterned on the back side of the digital tiers. After these steps, a new layer of oxide was added to the surface that was followed by planarization and LTD-bonding of a 700 μm thick silicon handle wafer. As a result, the pads connecting to the digital tiers were buried temporarily and the processing could be attempted on the analog tier to prepare it for LTD-bonding to the sensors. Processing on the opposite side of the 3D wafer pairs (analog tier) started with revealing and isolation of TSVs in an analogous way that was achieved earlier on the digital tier. Next, a blanket 300 nm thick layer of seed Al was deposited. Then, about 1 μm thick DBI® nickel layer was electro-plated on top of the seed Al layer. The diameter of plated nickel posts was 5 μm. The seed Al layer was patterned to form conductive paths between TSVs and points where nickel posts were to make contacts to the sensors diodes. After that, an oxide layer was grown on the surface and the surface was planarized. Finally, the handle wafer side was thinned to about 450 μm, and the 3D wafer pairs were diced to obtain individual VIPIC1 dies that were ready for bonding to the sensor wafers.

The preparation of the sensor wafers for receiving chips was carried out in a similar manner as described for the analog tier of the 3D wafer pairs. First, a 4 μm diameter via cut was made through the oxide to the sensor metallization. This was followed by plating of DBI® nickel posts off-center of diode implants and on opposite sides of the cuts to the sensor metallization. The latter was necessary to manage the surface topography that was challenging due to the conformal nature of the metallization contacts: sensor Al metallization to diode and Al seed layer to sensor.

The VIPIC1 chips were individually picked, aligned and placed on the sensor wafers, which resulted in bonding. The required alignment in both orthogonal directions was verified with the Vernier-type alignment keys that could be seen through silicon in infra-red light. Baking of the sensor wafers with bonded chips at temperature 200ºC completed the bonding process. The chips after this step were thinned by grinding and by application of a selective silicon etch down to the pads that had been buried on the digital tier side under the handle layer. The pads on the digital tiers (for bump-bonding) as well as the pads on the sensors (for wire bonding) were opened at the same step. Dicing of the sensor wafers with bonded VIPIC1 chips was the last step in building the LTD-bonded assemblies [14] that, at this point were effectively monolithic structures. The diced assemblies of the VIPIC1 chips had Sn-Pb bump balls deposited. The result is shown in Fig. 1d. The bump-bonding balls are about 75 μm in diameter. After deposition of the bump-bonding balls, the assemblies were flip-chip bonded onto the host PCB. One VIPIC1, bonded to the sensor, bump-bonded upside down on the precision host PCB, is shown in Fig. 1e. A dozen assemblies were brought to the last stage, and a few of them were found functional. One device that performed best in the bench tests was used for the tests at the APS at Argonne National Laboratory on the 10 keV beamline.

A cross-section view of the prepared Ni-DBI® bonding connection between the sensor diode and the VIPIC1 pixel electronics is shown in Fig. 2.

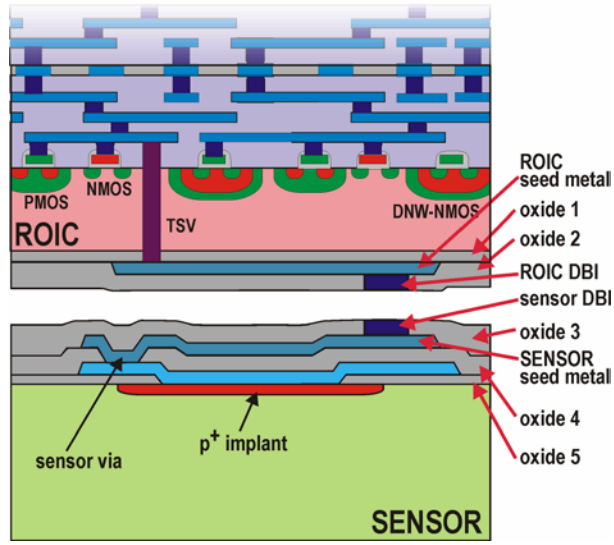

Fig. 2. A cross-section of the Ni-DBI® bonding connection between the sensor diode and the pixel electronics of the VIPIC1 chip.

III. Testing of VIPIC1 Chips LTD-Bonded to Sensors

Testing of the VIPIC1 chips LTD-bonded to sensors was performed using the NI PXIe system with FlexRIO cards driving digital I/O modules [7][10][11]. Power supplies and biases were also provided by the PXIe system with the power supply and Digital-to-Analog Conversion (DAC) modules.

The chips could be tested in the full sparsified readout mode with simultaneous acquisition of the data from all 16 LVDS outputs, while the data serialization clock was run at 166 MHz. The data could be sent in the direct memory access mode without any dead time over the back-plane bus to the memory of the controller module at the resulting rate. A single acquisition could run until filling up of the reserved memory block, which was up to 4 GB. When the memory block was filled up, the acquisition needed to be interrupted to allow dumping the block of data to the hard-drive. Interrupting of the acquisition violated the timing continuity of the stream of data. This could be of a concern, for example, for calculating the autocorrelation parameters (which underlies the photon correlation method) for a synchronous X-ray source, such as the APS. Nevertheless, strings of continuously collected data could extend to a few tens of seconds. This proved to be sufficient for obtaining good results in the targeted application [15]. It should be noted that interruption of the data acquisition does not matter for work with asynchronous sources of radiation, such as laboratory radioactive sources.

The high frequency of the serialization clock allowed sending data related to a single hit (16 bits - with 3 bits of the

start symbol, 5 bits of the counter value and 8 bits of the pixel address) in about 100 ns. Also, the readout control could be programmed in such a way that switching between the time frames was achieved in just a few extra clock cycles of the serialization clock to keep synchronicity with the synchrotron timing. These facts allowed timing resolution equal to 153 ns, which is the bunch separation time in the 24-bunch filling pattern of the APS [16]. The maximum number of hits that could be read out from each group of pixels in this situation was equal to one. This mode of operation was used only in some tests at the APS, where demonstration of the ultimate timing precision of the VIPIC1 chip was targeted. Tests with radioactive sources were typically carried out at much lower frame rates in order to accumulate enough statistical population of events to allow measurements of benchmarking parameters, like gain and noise, with sufficient accuracy. Two laboratory radioactive sources, ^{55}Fe (10 mCi), emitting 5.89 keV and 6.49 keV photons, and ^{90}Sr, emitting electrons with the endpoint energy of 0.546 MeV, were used in the tests. The sensors were biased typically with 170 V applied to their backplane, which was about 20 V above full depletion.

A. Tests with a ^{55}Fe X-ray Source

Exposures to mono-energetic X-rays allow unambiguous measurements of parameters, including the gain of the processing chain and the input referred noise. The gain is typically expressed as the peak amplitude of a pulse per a unit of charge, and the noise is expressed in charge units as Equivalent Noise Charge (ENC). In order to estimate these parameters, scans of thresholds with a resolution of 0.5 mV per step were used and the tested devices were exposed to a ^{55}Fe radioactive source. The thickness of the VIPIC1 chip after LTD-bonding on top of the sensor, as shown in Fig. 1b, is about one attenuation length of 5.89 keV photons. Also, measurements with illuminations from both the front and back sides were allowed with this version of the VIPIC1 detector that featured connections to the chip through the pads deposited on the sensor, as shown in Fig. 1c. It is worth noting that such an opportunity is unique to the VIPIC1 device and is not available in classical hybrid detectors. An illustration of how both illuminations were achieved is given in Fig. 3.

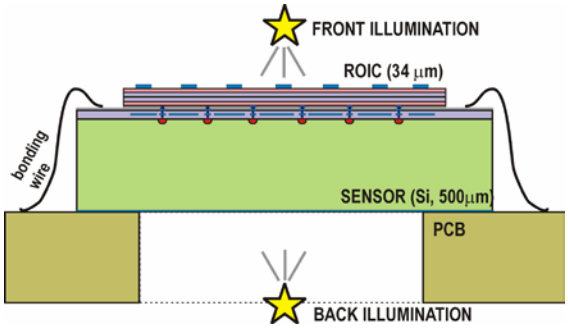

Fig. 3. Illustration of how the front and back illuminations of the silicon sensor were achieved.

Acquisitions were run long enough to accumulate a few thousand counts of hits per pixel for each threshold step, which was typically achieved in a few thousand time frames, where each frame had a duration of about 10 μs. Examples of the obtained integral energy spectra of ^{55}Fe in the front and back side illuminations of the 500 μm thick fully depleted silicon sensor are shown in Fig. 4. Both curves, shown in Fig. 4, are plotted for a typical single pixel from the tested device with the flat field exposure. A peak, centred on about 339.2 mV contains events generating discriminator triggers from spontaneous back and forth crossings of the baseline level due to the noise. A slope, starting on the right side of the noise peak, is strongly seen on the data from the back-side illumination. It results from the charge sharing, as holes diffuse laterally with standard deviation of about 8 μm along their travel to the collecting electrodes on the front side at the applied polarization of the sensor. Recombination of carrier can also contribute to the manifested slope. No slope is visible on the front illumination data. Both integral spectra end at signal levels slightly above 450 mV, as this value represents the amplitude when a photon produces a signal wholly in a single pixel and no charge is lost in the charge drifting in the sensor. This point is used for determination of the gain. Presence of the slope adds slight difficulties in measurement of the gain. The method, based on finding a peak in a differentiated integral spectrum [11] gives two values that are different by about 1.5% as it can be seen in Fig. 4.

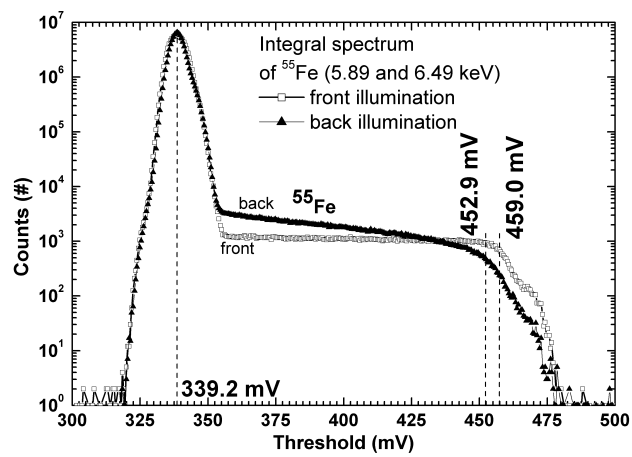

Fig. 4. Integral energy spectra of ^{55}Fe in the front and back side illumination obtained in threshold scan at ΔV=500 μV (V_{dep}=170V).

The regular energy spectra, shown in Fig. 5, were obtained through differentiation of the integral spectra. Each illumination case is shown for two values of the I_{FED} current (defining the resistance in the feedback path of the preamplifier) [11]. The low value of the I_{FED} current is 3 μA (feedback resistance of about 50 MΩ) and the high value of the I_{FED} current is 9 μA (feedback resistance of about 10 MΩ). The curves were normalized to equal the amplitude of the 5.89 keV spectral line and, further, to the known ratio of 5.89 keV to 6.49 keV photons in the emittance spectrum of a ^{55}Fe source. The energy axes of individual spectra, given in charge units, were also scaled according to the measured gain. Hence, all the 5.89 keV peaks could be shown at the same place and the distance between the 5.89 keV and 6.49 keV peaks was preserved for each case. The ability to distinguish two peaks in the spectra in Fig. 5 tells that the total noise must be less than ENC=40 e^- rms. Summing of spectra from all pixels for which gain values stayed within the 2% range around the average yielded the smoothness of the curves.

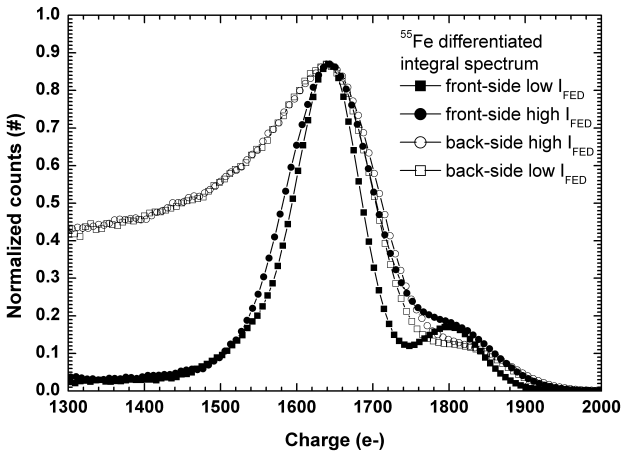

Fig. 5. Normalized energy spectra of ^{55}Fe for the front and back illumination and at varied I_{FED} currents (I_{FED} controls the continuous reset in the first stage of the analog processing chain [11]).

The threshold scans were also exploited to measure the gain and the input referred noise for every pixel in the matrix. The histograms of amplitudes of signals that correspond to 5.89 keV photons are shown in Fig. 6. The results presented in Fig. 6a and in Fig. 6b are for the back and front illumination conditions, respectively. In both cases, a method that operates on integral spectra [11] was used for extracting the signal amplitudes. Only lower I_{FED} values were used and other bias settings were nominal [11] for the acquisitions of data presented in Fig. 6. The distributions are narrow and exhibit only a small asymmetry. Pixels with signal amplitudes below 40 mV (arbitrary criterion) were considered not responding to the photons. Only approximately 50 pixels (1.25% of population) out of 4096 were found dead.

Gaussian fitting of the histograms, led to the following gain values with pixel-to-pixel dispersions correspondingly for the back and front illumination conditions: 65.79 μV/e$^-$ with dispersion of 2.75 μV/e$^-$ rms and 69.64 μV/e$^-$ with dispersion of 2.71 μV/e$^-$ rms. The gain is about 5.5% higher in the case of the front-side illumination. Such a result can be attributed to two effects, i.e. less pronounced end-point knee in integral spectra and some loss of charge in the transport to the collection electrodes in the back-side illumination conditions.

The noise is measured as the width of the noise peak in the integral spectra, resulting from frequency of registering random noise events [17]. The noise can be referred to the input of the processing chain and expressed as ENC thanks to the performed gain calibration. The histograms of ENC values are shown in Fig. 7. Both histograms are for the front illumination conditions. The results presented in Fig. 7a and in Fig. 7b are given correspondingly for the small and large equivalent feedback resistance in the preamplifier. Like the gain distributions, the noise distributions are narrow and exhibit only a slight asymmetry. After Gaussian fitting the histograms shown in Fig. 7, the following ENC values with pixel-to-pixel dispersions were extracted, correspondingly for the small and large equivalent feedback resistance in the preamplifier: 42.3 e$^-$ rms with dispersion of 3.9 e$^-$ rms and 36.2 e$^-$ rms with dispersion of 2.6 e$^-$ rms. As expected, the large equivalent feedback resistance yields ENC about 18% smaller than that for the smaller resistance due to less parallel noise. It is known from simulations that the input capacitance must be less than 20 fF for ENC below 40 e$^-$ rms.

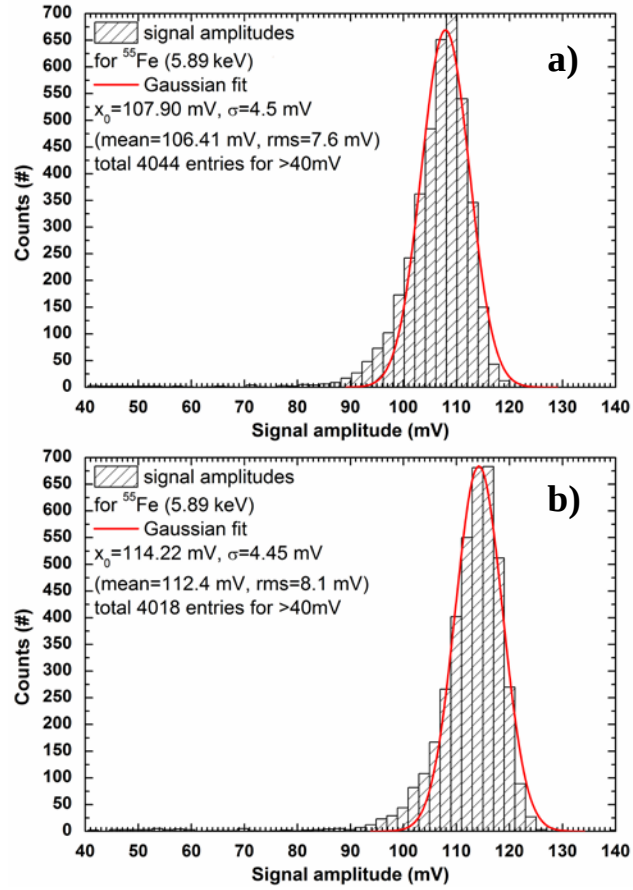

Fig. 6. a) Histograms of amplitudes of signals for photons from a ^{55}Fe source (only Kα 5.89 keV) from back and b) front illuminations.

When analyzing the results shown in Fig. 7, it is apparent that the ENC value and its pixel-to-pixel dispersion are significantly lower than those achieved for the same VIPIC1 chip connected to the detector via bump bonding [11]. A similar observation can be made with respect to the dispersions of the gain values through the analysis of the data presented in Fig. 6. The bump-bonding technique, to which the LTD-bonding is compared, is not the most aggressive one available at present [18]. So, the achieved factor of almost two of noise improvement that has been demonstrated for the LTD-bonded VIPIC1 chip with respect to the bump bonded version may be too optimistic. Nevertheless, a statement that LTD-bonding leads to improvements in performances compared to current hybrid pixel detector technologies is justified based on the findings presented here.

The ENC level equal to 36.2 e$^-$ rms is the lowest measured at room temperature on a hybrid detector, featuring the parameters (front-end speed, power consumption, etc.) similar to the VIPIC1 chip. The reported ENC=36.2 e$^-$ rms is very close to that achievable by Monolithic Active Pixel Sensors [19]. The results, in terms of this most sensitive parameter are cross-verified by the measured spectrum of photons from a ^{55}Fe in Fig. 5, where two spectral peaks are distinguishable.

B. Tests with a ^{90}Sr Beta Source

Electrons, emitted from ^{90}Sr, can travel distances up to a

few millimeters in silicon and they significantly scatter in the detector material as their maximum energy is 0.546 MeV. Using the electrons as a signal source was an objective method of verification of correctness of the operation of the sparsified readout of the VIPIC1 chip. The target for the tests was to verify whether all elements of the electron tracks, generated instantaneously through the nature of the events, are read out entirely within a single time frame. Should track elements appear in more than one time frame, the implication would be that the prevention of double registration of hits [3][7] fails in the chip, or that the sparsification engine gets stuck.

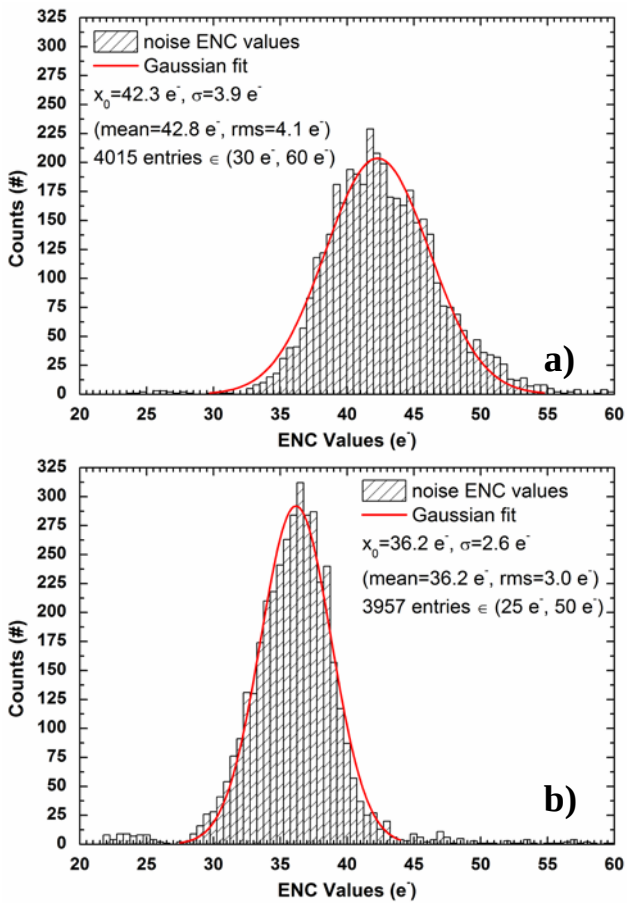

Fig. 7. a) ENC histograms from front-side illumination of VIPIC1 with small and b) with large feedback resistance in the preamplifier.

In order to generate electron tracks that could be seen by the version of the VIPIC1 chip from Fig. 1e, the sensor was side illuminated, as shown in Fig 8. The readout sequence was programmed in such a way that time frames changed every 2.7 μs, leading to reading out maximum of 24 hits for each time frame per every group of pixels in the VIPIC1 chip. Some results of the acquisition are given in Fig. 9. The image shown there is generated as a superposition of several time frames. As a result, a few curly electron tracks could be shown despite the low occupancy. The data acquisition was run without stopping and the data from the consecutive time frames was compared to see if there were any ghost image tracks. The hits from all the tracks were always entirely restricted in one set of frames, confirming correct operation of readout, including the sparsification engine. Discontinuities of tracks is due to the very high setting of thresholds.

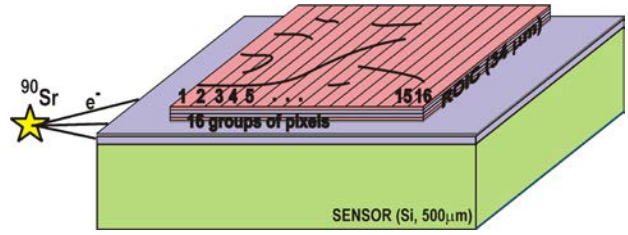

Fig. 8. Illustration of how exposure to a ^{90}Sr source was achieved.

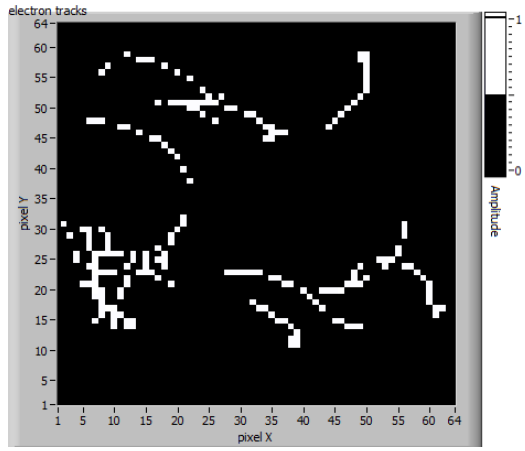

Fig. 9. Superposition of selected 13 frames acquired at Δt=2.7 μs.

C.Timing Performance Tests at the APS

The tests, targeting the characterization of the timing performance of the VIPIC1 detector, were carried out on the 10 keV X-ray photon beam at the 8-ID-I sector at the APS. The direct beam was sent onto the VIPIC1 chip version shown in Fig. 1e. The 24 bunch mode of the APS, where X-ray photons are delivered in picosecond-long bursts every 153 ns [16], was used in the experiment. The intensity of the beam was adjusted to only a few photons per bunch impinging on the whole surface of the VIPIC1 detector. The readout sequence of the VIPIC1 chip was programmed in such a way that the acquisition was synchronous with the APS timing. The synchronization pulses were provided from the bunch clock timing module, which distributed bunch pattern and timing information from the storage ring control system [20]. The module was delivering one pulse for each bunch. The delay of the edge of the signal, defining transitions between time frames in the VIPIC1 chip and sampling outputs of in-pixel discriminators and latching hits for readout, was adjusted with respect to the APS synchronization signal. The delay corrected for operation of the VIPIC1 chip from different clock domain than the synchrotron and the photons could be registered always in the appropriate time frames.

The serializers of the VIPIC1 chip were clocked at the frequency, allowing reading out one hit per group of 256 pixels every APS cycle. The acquisition of data was kept running for a few tens of seconds without any dead time. Following the acquisition, a simple data analysis program was executed. The program segmented the acquired data in vectors modulo 24. Thus, each vector had 24 elements and each element was a set of addresses of the registered hit pixels. Then, the number of hits was counted for every set and new vectors were built, where every element was a simple number of hits. Finally, all vectors with number of hits were added and

the result was normalized to the largest number in the vector. The result obtained should be proportionally reflecting bunch-to-bunch variations of the photon intensity. The vector is plotted in Fig. 10 together with the direct measurements of the synchrotron bunch-to-bunch electron current. Both data sets coincide faithfully. The measurements of the beam current are available in 2 minutes intervals. The acquisition of data by the VIPIC1 chip could not be simultaneous with them, which yielded some differences between the plots. The results presented in Fig. 10 show that it was possible to achieve a timing resolution with the VIPIC1 chip as aggressive as 153 ns under specific data collection conditions.

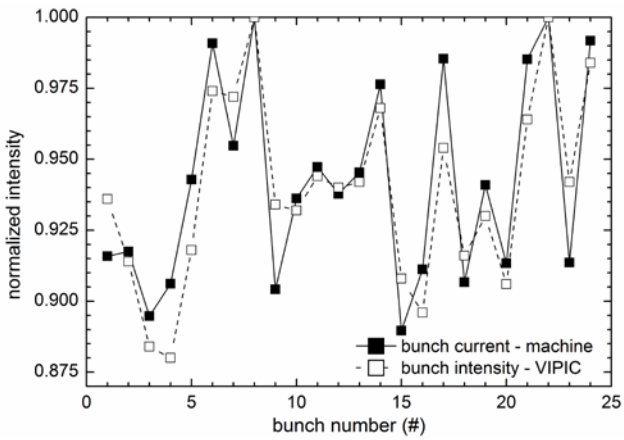

Fig. 10. X-ray intensity measurements of bunch-to-bunch electron beam current variations from the machine and from the VIPIC1 chip.

IV. Conclusions

A proof of the feasibility of a fully 3D-integrated hybrid pixel detector has been presented. Not only it has been shown that building a fully 3D-integrated system based on the bulk CMOS process is feasible but, even more importantly, it has been demonstrated that the performance of such systems can exceed that of older approaches. All this makes the 3D toolbox a valuable tactic for future pixel detectors. The results were achieved with a small 64×64, 80 μm pitch pixel structure, but no compromises were made at any step which would impose any limits on extrapolation of the finding to larger area pixel detectors, for this or other targeted applications. The LTD-bonded devices offer serious advantages, because the readout chips and sensors can be optimized independently, but the final structure is monolithic-like. The detector can be very thin, which is desired, for example, for tracking of relativistic particles (High Energy Physics) or can be thick, which is good, for example, for efficient X-ray detection (Photon Science) as required. Moreover, a very compact, dense assembly and gapless tiling is possible with the LTD-bonded devices. This is achievable through either tiling multiple 3D-integrated readout ASICs on a sensor wafer or through building edgeless fully functional detector modules. A pathway toward both such solutions has been shown by the device described here.

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