The CMS central hadron calorimeter DAQ system upgrade

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The CMS central hadron calorimeter DAQ system upgrade

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ABSTRACT: The CMS central hadron calorimeters will undergo a complete replacement of their data acquisition system electronics. The replacement is phased, with portions of the replacement starting in 2014 and continuing through LHC Long Shutdown 2 in 2018. The existing VME electronics will be replaced with a μTCA-based system. New on-detector QIE electronics cards will transmit data at 4.8 GHz to the new μHTR cards residing in μTCA crates in the CMS electronics cavern. The μTCA crates are controlled by the AMC13, which accepts system clock and trigger throttling control from the CMS global DAQ system. The AMC13 distributes the clock to the μHTR and reads out data buffers from the μHTR into the CMS data acquisition system. The AMC 13 also provides the clock for in-crate GLIBs which in turn distribute the clock to the on-detector front end electronics. We report on the design, development status, and schedule of the DAQ system upgrades.

KEYWORDS: Radiation-hard electronics; Front-end electronics for detector readout; Data acquisition concepts

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Contents

1 Introduction

The Compact Muon Solenoid (CMS) [1] experiment's Hadron Calorimeter (HCal) is a key subsystem for jet reconstruction, missing energy measurements, and lepton/photon isolation [2]. As such, the continued success of the CMS HCal is paramount to the future success of the physics program of the experiment. The upgrade of the HCal is required to mitigate detector performance anomalies related to existing HCAL photodetectors and to take advantage of new technologies to ameliorate the effects of radiation damage to the active detector material, which exceeds design estimates.

The CMS HCal is divided into several subsystems distinguished by their geographic location: the barrel and endcap systems (HB & HE), the outer system (HO), and the forward system (HF). Figure 1 shows where these detectors reside within CMS. This document focuses on the barrel and endcap systems, though the frontend readout electronics are very similar and the backend data acquisition (DAQ) electronics are identical for all subsystems. The HB/HE subsystems are brass and scintillator sampling calorimeters where light from plastic scintillators is collected with wavelength shifting fibers before being converted to an electrical signal with hybrid photodiodes (HPD). Although there are a number of physical sampling layers in the barrel and endcap regions, all (many) of these signals are currently summed optically resulting in one (several) channels per tower in the barrel (endcap) region.

This document will give an overview of plans and progress for the CMS HCal upgrades. Sections 2 will describe the motivations and resulting requirements for the upgrade design. Section 3 and section 4 will describe the design for the upgraded frontend and backend electronics, respectively. Section 5 will show results of integration tests of prototype electronics. Finally, section 6 will conclude with an overview of the installation plan.

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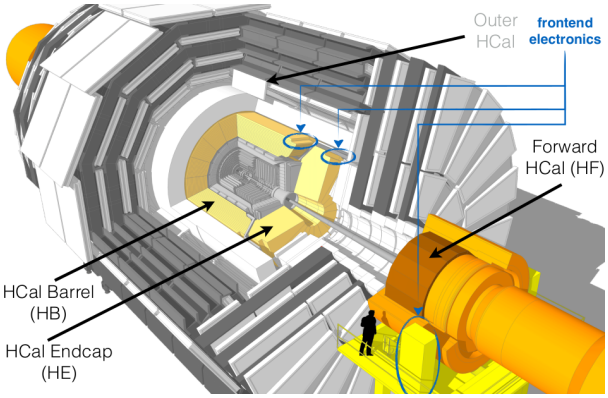

Figure 1. Sketch of the CMS detector. The Hadron Calorimeter sub-components are highlighted in yellow (HB, HE) and orange (HF). The location of the frontend electronic for the different subsystems are circled in blue.

2 Overview of phase I upgrades

During run I operations the response of the HB/HE HPD photodetectors was observed to change for a large fraction of channels, decreasing for some devices and increasing for others. The left plot of figure 2 shows HPD response relative to the response in October 2010 as a function of time. In just over two years, the response migrated more than 15% for about 10% of the channels and more than 5% for at least 40% of the channels. In addition, as a high voltage device, the HPD is known to exhibit anomalous signals related to spontaneous discharge.

Calibration data from the laser injection system has shown that radiation damage is causing the scintillator response to degrade faster than expected in the endcap region. The right plot of figure 2 shows the scintillator response as a function of integrated luminosity and pseudorapidity, η. This study's projections suggest that the calorimeter towers in the forward most regions of the endcap could degrade to as little as a percent of their original response. The use of SiPMs will help to migitate radiation induced damage due to their higher gain, higher photon detection efficiency, and higher S/N.

The large gain of the SiPMs requires improved digitizing Application Specific Integrated Circuits (ASICs) with higher dynamic range than the current ASICs. Given that the integation time will remain 25 ns, further improvements will include temporal information about the pulse edge within each time slice through a TDC to improve the reconstruction capabilities and help to reject pileup or anomalous signals.

The size of the SiPM also facilitates increased depth segmentation because of the higher channel density that is possible. This will allow for depth dependent calibrations to better adapt to layer dependent radiation damage. The existing and proposed depth segmentation for both the HB and HE subsystems is shown in figure 3. The increased depth segmentation will ultimately increase the data read out per event by up to a factor of 5, depending on the polar angle of the calorimeter tower.

Given the proposed changes to both the detector and the digitizing ASIC, a primary requirement of the upgraded DAQ system is increased bandwidth. The amount of data transmitted per

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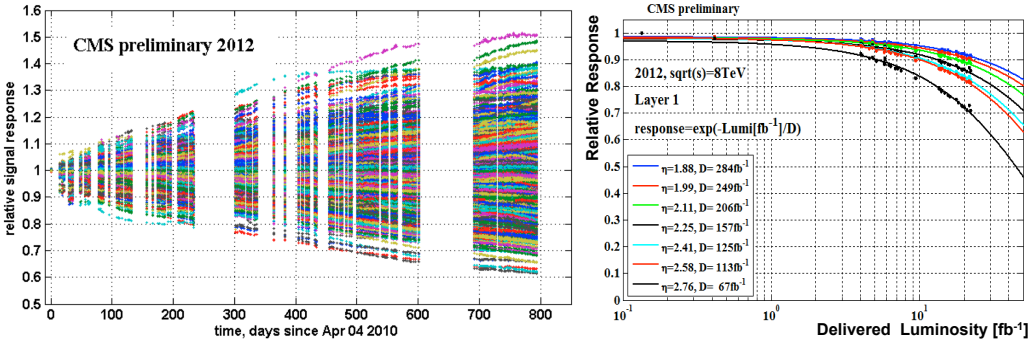

Figure 2. Left: HPD response drift over time for a subset of HPD pixels. Each colored line represents a unique pixel. Right: Relative HE scintillator response to laser excitation as a function of η, represented by different colored curves and points, and integrated luminosity, shown in log scale on the x-axis.

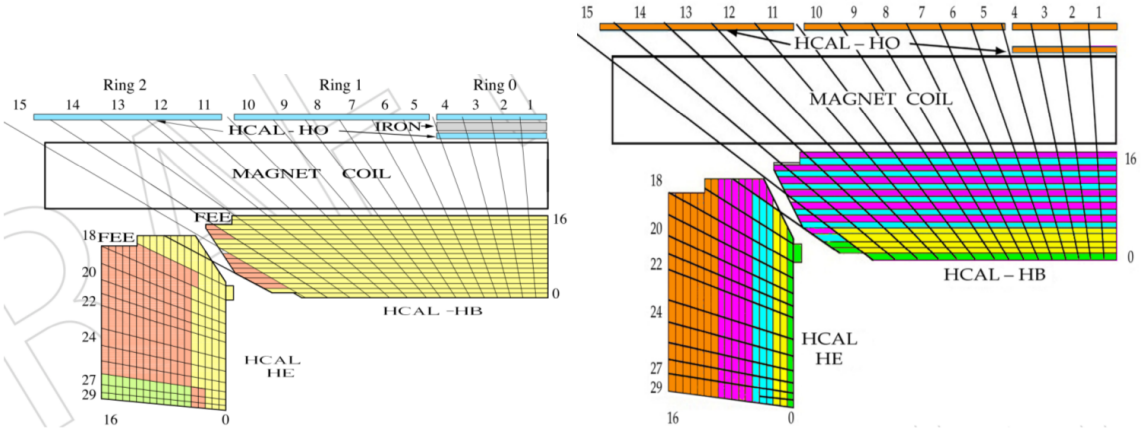

Figure 3. Current (left) and proposed future (right) depth segmentations in the barrel and endcap region. Colors represent groups of physical layers which are optically summed into distinct readout channels.

channel will increase by ∼50% and the number of channels read out on each data link will increase by a factor of 2. Thus, the overall data transfer rate to the backend will be a factor of 3 higher.

The backend electronics will be μTCA-based [3] in order to conform with the CMS upgrade specification [4]. The μTCA architechture offers high bandwidth backplane connections between MCH modules and each AMC as well as power monitoring and hot-swappable components. Thus, it is a marked improvement over the current VME-bus DAQ system which employed many front panel connections for intermodule communication.

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3 Frontend electronics

The conceptual design of the frontend electronics is largely the same as the existing system. All frontend electronics will be located on the detector and thus in a radiation environment.[1] Data will be digitized at 40 MHz and continuously communicated to the backend electronics. Each 20 degree slice of the HB and HE systems is serviced by a single readout box (RBX) which includes six separate modules. One of these modules will manage the distribution of fast (clock, reset, and synchronization) signals and slow signals, I^2C communication, to other modules. There is one calibration module that distributions light pulses to the individual photodetectors. The remainder of the modules will contain 4 QIE cards each with 12 individual Charge Integrater and Encoder (QIE) ASICs [5–8].

The QIE11 ASIC has been designed to accomodate inputs from the new SiPMs by implementing a programmable current shunt before the integration circuit. Due to the large gain and other electronic properties of the SiPMs this will initially be necessary to obtain the required precision, but as radiation induced aging affects photoproduction, this current shunt can be reduced to exploit the large dynamic range of the chip. The dynamic range of the chip has been increased by a factor of 10. It makes use of a range select scheme to produce an output which is effectively a 17-bit ADC with roughly constant, 1–2%, precision over the whole dynamic range. The ASIC will also report a 6-bit code which provides 500 ps resolution on the rising edge of the pulse.

Data from 12 QIEs will simultaneously be captured, aligned, and formatted by a Microsemi IGLOO2 Field Programmable Gate Array (FPGA). This FPGA was chosen for its radiation tolerance and its native 5 Gbps serializers. Additional functionalities such as data integrity monitoring and clock phase adjustment will be handled by the IGLOO2. The IGLOO2 will use the QIE's TDC discriminator and an internal phase lock loop to form a trailing edge TDC in addition to the QIE's native leading edge TDC.

Serialized data from the IGLOO2 is then sent to the frontend-backend optical link. As mentioned previously, each QIE card will need to accomodate 3 times the bandwidth in the frontend-backend link. To accomodate this requirement, the CERN-developed Versatile Tranceiver [9, 10] dual optical drivers will be used. These devices have been verified to be sufficiently radiation tolerant and can operate at up to 5.0 Gbps.

Each QIE card and calibration card will receive 6.5 V of power from a custom backplane. Several CERN-developed switching DC-DC converters [11, 12] are employed to deliver power to individual components.

4 Backend electronics

The HCal backend electronics are responsible for computing trigger primitives, communicating with the the level-1 trigger system, and sending events to the central DAQ system [13]. The backend electronics will reside in a commercial μTCA crate and will consist of two types of custom modules, a "μTCA HCal Trigger and Readout" (μHTR) module and an AMC13 module [14, 15]. Each μTCA crate will also contain one commercial μTCA Carrier Hub (MCH) which will be

[1] Although it is not discussed here, all components of the frontend electronics have been verified to be sufficiently radiation tolerant for integrated doses comparable to those expected from the LHC.

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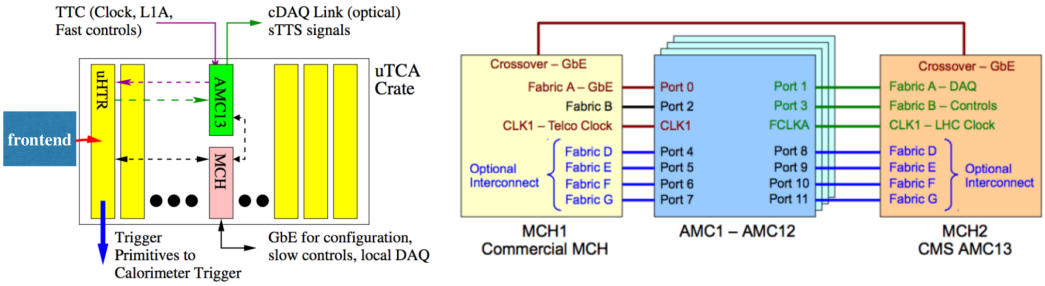

Figure 4. Left: Schematic of μTCA crate with relevant backend components and their communication. Right: Diagram showing various fabric connections utilized for backend communication between each MCH and each AMC.

located in the primary MCH slot of the crate. The secondary MCH slot will house the AMC13 module which will send data compiled from all μHTRs in the crate to the central CMS DAQ system. Figure 4 shows a schematic diagram describing how each of the backend crates will be setup.

The μTCA specifications allow for each MCH to access several high-speed data connections with each of the AMC [16] slots of the μTCA crate. Figure 4 illustrates how each of the individual Fabric connections are utilized. Communication between software and hardware is done via IPBus[2] which relies on virtual buses residing on each of the AMC modules. IPBus implements an ethernet packet to communicate simple read, write, and bit-set commands to hardware components.

The block diagram for the μHTR is shown in figure 5. The μHTR receives data from up to 24 fiber links on 2 Pluggable Parallel Optical (PPOD) receivers each operating at 12x 5.0 Gbps. Data from each of the serial optical links is deserialized by one of the two Xilinx Virtex-6 FPGAs. ADC codes are linearized and the relevant data from individual towers are summed and converted to an energy. The energies are formatted into trigger primitives and sent to the level-1 trigger system [17]. The data is pipelined until a level-1 Accept (L1A) signal is received after which the data is buffered by the back FPGA where zero-supression can be applied before being sent to the AMC13 over the μTCA backplane.

The μHTR can also implement logic to format and compute bits for the level-1 trigger system. This will consist of a peak finding algorithm, lookup tables to convert linear energies to non-linear energies for larger dynamic range, and potential algorithms specialized for pile-up identification. The trigger primitives will be sent to the trigger system via PPOD transmitter.

Some auxillary functions such as power management, MMC functions, JTAG, and configuration storage is handled by a number of mezzanine cards on the μHTR. This will allow for easy replacement, if needed, and has allowed for parallel developement and testing of mezzanines and the mother board.

The block diagram for the AMC13 is shown in figure 6. The board is divided into several tongues which form a PCB stack. Two of the boards contain a 172-pin backplane connection; the third provides access for JTAG and USB connections via the front panel. The front panel also contains four SFP+ optical tranceivers which communicate with the Trigger, Timing, and Control (TTC) system, and the central DAQ system.

[2]IPBus firmware/software suite available from svnweb.cern.ch/trac/cactus/wiki.

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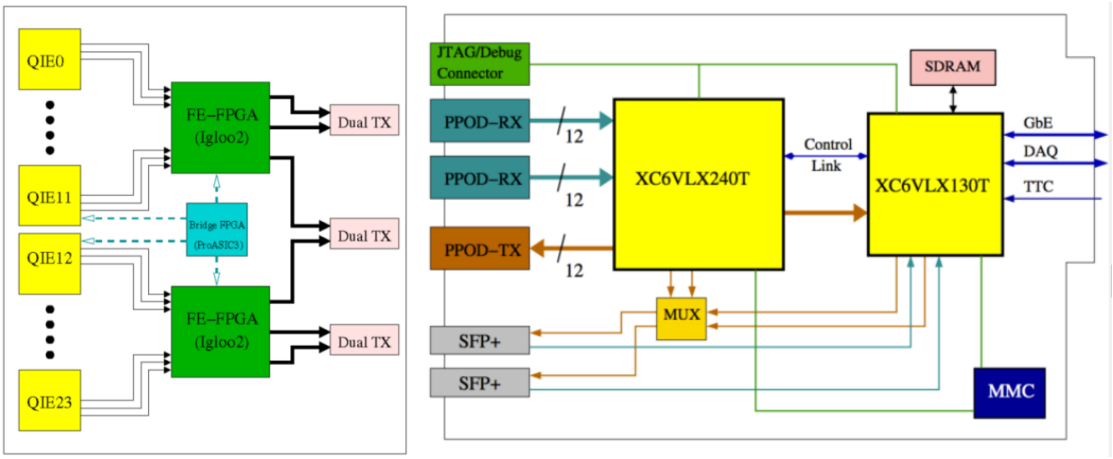

Figure 5. Left: Block diagram for the 24-channel QIE card. Right: Block diagram for the μHTR.

The TTC signal carries both the LHC clock and trigger data using a 160 MHz biphase mark encoding over the receiving end of the optical link. Frontend signals (busy, ready, overflow, etc.) are returned to the Trigger Throttling System (TTS) over the transmitting end of the optical link. The data from the TTC is decoded, separating the data from the 160 MHz clock, on tongue 1 of the AMC13. The clock is then divided by 4 and fanned out to each of the AMC slots over the backplane. The TTC data is transmitted from the Kintex-7 to the Spartan-6 before being sent to individual AMC slots.

The right block diagram of figure 6 illustrates how event building is handled in the Kintex-7 FPGA. Event fragments are collected from each of the AMC slots over the 5.0 Gbps Fabric A connection. CRC checking is performed and data is either buffered or re-transmitted in case of corrupted blocks of data. The TTC data which is decoded and L1As are buffered while each event fragment is paired with its corresponding L1A. These event fragments combine to form an event which is then sent to the central DAQ system via an S-Link Express transmitter.[3] Data is also buffered into a 512 MB SDRAM for monitoring and local DAQ utility.

5 Testing & validation

Integration tests for both the frontend & backend electronics have been carried out using the HF prototype frontend and the HF backend electronics.

Tests with full μTCA crates are underway at CERN. The upgraded backend electronics have been verified to work with the existing frontend electronics as well as the existing and upgraded trigger system. This is a key validation in preparation to commisioning the backend electronics in 2015.

Full integration tests with the upgraded frontend and backend electronics have been carried out both during beam tests with a cerenkov calorimeter and with a standalone pulse injection system. Optical links between the frontend and backend has been verified to work. Monitoring and config-

[3] S-LINK is a CERN specification for a FIFO-like data-link. See hsi.web.cern.ch/HSI/s-link/.

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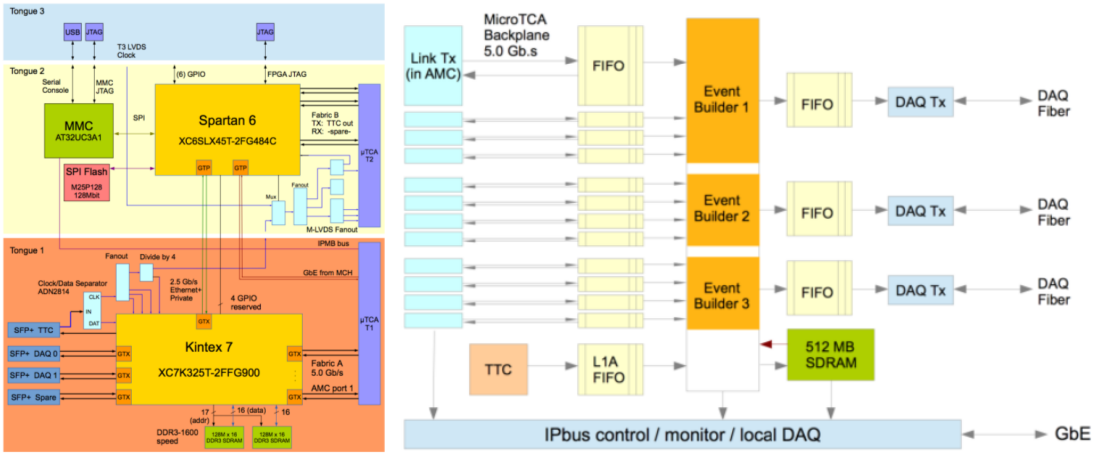

Figure 6. Left: Block diagram describing major functions of the AMC13. Right: Block diagram describing the proceedure for event building within the AMC13.

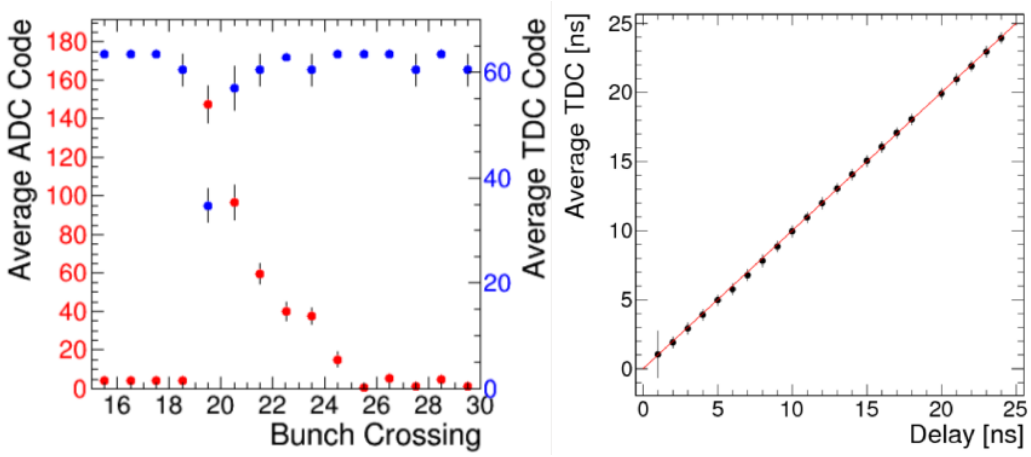

Figure 7. Left: Distribution of average ADC (red) and average TDC (blue) codes for a given run during beam tests. Right: Average and RMS of TDC codes recorded for various input delays.

uration communication protocols for the frontend were verified by testing key functionalities such as programming the QIEs, reading/writing register on various devices within the frontend crate, and in-situ programming of the IGLOO2 over JTAG via the μTCAcontrol system.

Readout functionality was verified by measuring pulse shapes and timing characteristics from ADC and TDC data. The left plot of figure 7 shows the average ADC and average TDC code read out in several bunch crossings around each triggered event. The pulse shape is clearly visible and the TDC code is found to be in coincidence with the rising edge of the pulse, as expected. Using an internal pulse injection scheme with a configurable delay, the TDC resolution was verified. The right plot of figure 7 shows the average and RMS distribution of the TDC code for many different input delays. There is a one to one correspondence between the input delay and the output TDC code. The RMS of these points are typical consistent with the 500 ps resolution of the TDC.

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6 Conclusions

The design of the readout electronics for the phase I HCal upgrade is largely complete. The backend electronics are fully designed, prototyped, and tested. The production modules for the HF backend upgrade will be completed and installed by the start of the 2015 LHC operations. During 2015 operations the backend electronics will be commissioned. Given that the backend electronics for HB/HE will only differ in there trigger primitive algorithms, the backend electronics will be well understood by the time HB/HE is installed during LS2.

Prototypes for the HF frontend electronics have been designed, produced, and tested. Although the formfactor of the HB/HE frontend electronics are different, the functional design has been tested. Prototypes for the HB/HE frontend electronics will be fabricated and tested in early 2015. Full installation of the frontend and backend electronics for HB/HE will occur during LS2.

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