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# Pixellated readout IC: Analysis for single photon infrared detector for fast time of arrival applications

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***Abstract*– The nano-injection sensor is a new approach towards high-sensitivity short-wave infrared photon imagers. It resolves the conflict of requiring a large area for high quantum efficiency and small area for high fidelity by using a relatively large micron-scale absorbing volume, and nano-scale sensing elements, which regulates the electron flow and amplifies the signal. The front-end electronics for the Single Photon Imaging nano-injection detector consists of an ROIC with 32 × 32 pixel array with a pixel size of 100µm × 100µm. Each pixel consists of a charge sensitive preamplifier with leakage current compensation circuit, a shaping amplifier, an AC-coupled comparator with a 7-bit trimming DAC for offset cancellation, a 10-bit counter for photon counting, and a 10-bit shift register for data readout. The ROIC provides dead-time less, continuous readout with 32 parallel LVDS outputs to achieve full frame readout within 5 µs. Simulation results of the ROIC are presented in this work.**

***Index Terms*— *single photon detection, photon counting, time of arrival, dead-time less readout***

## I. Introduction

THE isolated electron-injection sensor is a new approach towards high-sensitivity short-wave infrared photon imagers. It resolves the conflict of requiring a large area for high quantum efficiency and small area for high fidelity by using a relatively large micron-scale absorbing volume, and a smaller sensing element, which regulates the electron flow and amplifies the signal. Different ratios of absorbing and sensing areas can be manufactured to tailor the performance of the detector for specific gain and rise times.

These electron-injection sensors are made from III-V semiconductor hetero-junctions and operate in linear amplification mode. They can simultaneously provide high gain, high quantum efficiency, low noise and achieve reduced dark current levels [1, 2, 3]. Devices with 10 µm injector diameter show an optical gain of ~ 2000 at bias voltage of -3V. The dark current after amplification is ~ 10 nA at room temperature, decreasing to ~ 60 pA at 250 K. It has rise-times of approximately 5 ns at 40 µW optical power and can clearly differentiate between two photons arriving ~110ns apart [3]. Approximately 800 h+ (holes) are generated in the detector when a single photon impinges the detector volume.

A readout integrated circuit (ROIC) has been designed to match the sensor performance with low noise readout electronics and also to handle dark (leakage) currents in the detector. The ROIC provides position sensitivity (100 µm) and time of arrival information within 5 ns accuracy. The digital readout is dead-time less, and allows for continuous operation.

This single-photon hybrid detector is being developed for quantum cryptography applications which require position along with its time of arrival information of the incoming photon. Identifying the correct sequence of incoming photons with a probability of false detection below 6 σ (1 in 1 million) is required for this application. This translates to an accurate time-stamp and high signal-to noise ratio (SNR) requirement for the ROIC.

## II. Read Out Integrated Circuit

### A. Pixel Architecture

Each pixel contains a charge sensitive preamplifier with leakage current compensation able to cope with dark currents of 10-20 nA per pixel. It is followed by a shaping amplifier with a shaping time of 30 ns, selected to reduce noise due long integration of dark current but slow enough so as not to cause ballistic deficit. It is AC-coupled to a differential comparator with a 7-bit differential trimming DAC for offset cancellation. The output of the comparator starts a 10-bit counter to provide a timestamp which uses a 200 MHz gated clock for achieving around 5 ns timing resolution. At the end of a frame (1 µs – 5 µs), data is transferred to a 10-bit shift register, which is readout at the end-of-column. A configuration register is used to program the DAC and setup the pixel's mode of operation. The pixel block diagram is shown in Fig. 1.

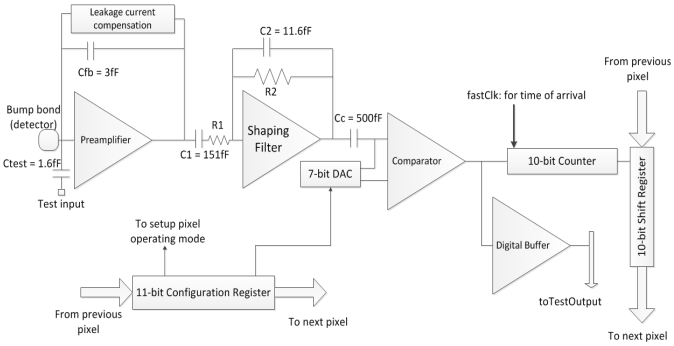


**Fig. 1 Pixel block diagram**

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The Fig. 2 shows the square pixel layout with a 100 µm side length. The layout can be further optimized to reduce overall area by approximately 25%; the main goal for this version of the ROIC was to verify performance.

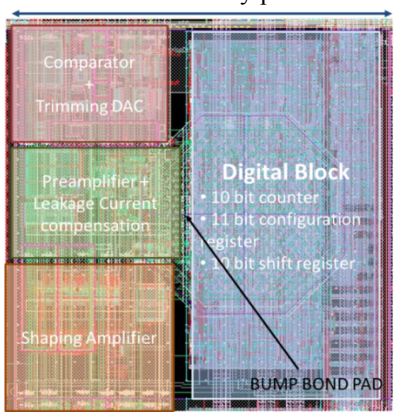


**Fig. 2 Pixel layout**

### B. *ROIC Architecture*

The ROIC consists of an array of 32 x 32 pixels. The shift register of each pixel within a column is daisy chained. The ROIC has 32 LVDS differential outputs for high speed data transfer. The parallel high speed data transfer helps with reading out the entire ROIC within 1-5µs.

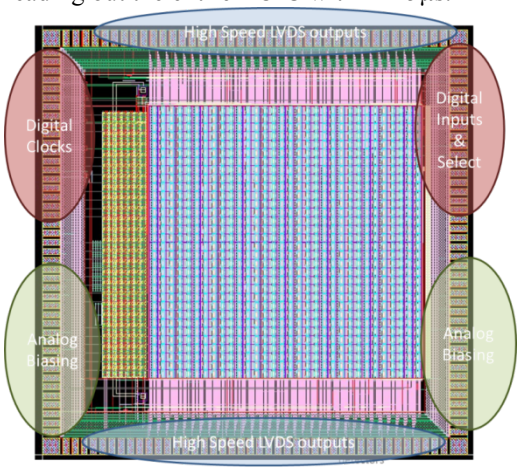


**Fig. 3 ROIC layout**

## III. Front-End Design

This section describes the transistor level design of the blocks within a pixel. The sensor generates approximately 800 $h^+$ of charge for a single photon interaction in the sensing volume; it has an input capacitance of 100 fF. The front-end electronics has to cope with leakage currents of 10-20 nA per pixel, which could be reduced by moderate cooling.

### A. *Charge Sensitive Preamplifier (CSA) and leakage current compensation circuit*

The CSA design is based on a folded cascode core amplifier with two source followers, to drive the feedback and output separately as shown in Fig. 4. The tail current transistor operates in the linear region [4]. The feedback capacitance is 3 fF, and the feedback resistance is around 67 MΩ using an active transistor feedback mechanism. The open loop gain of the core amplifier is 58 dB. The low feedback capacitance is important to provide high voltage gain, however this might result in a large pixel-pixel gain variation and therefore great emphasis needs to be placed on good layout methodology to keep the parasitic components as low as possible. Gain correction might be added in a future implementation.

The leakage current compensation circuit is based on a differential Krummenacher approach [5, 6]. The baseline recovery is achieved after signal integration by a low frequency feedback loop which sets the output of the CSA to a reference voltage Vfed.

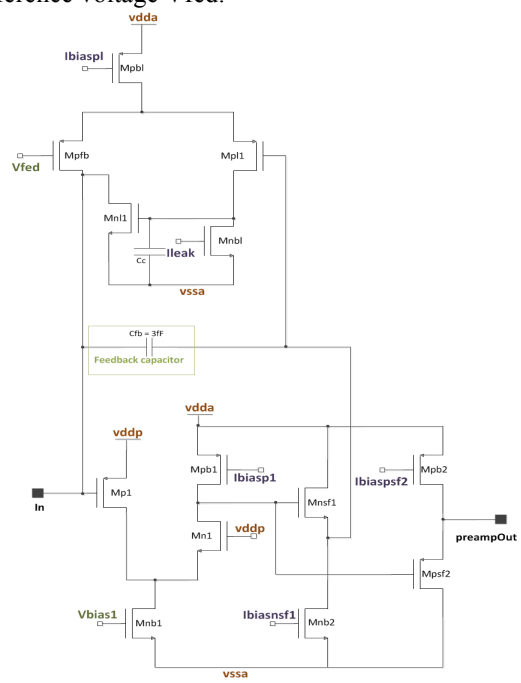


**Fig. 4 Transistor level preamplifier design**

### B. *Shaping Amplifier*

The shaping amplifier behaves as a CR-RC band pass filter and a gain amplifier also based on a folded cascode core amplifier. The two core amplifiers architectures are matched and the primary difference is the reduced currents in the shaping amplifier. It also contains a pole-zero cancellation circuit [7], allowing elimination of output signal overshooting. Shaping time is set by capacitance and resistance (active transistor) values to equal 30 ns and has a voltage gain of 5. Shaping time was optimized to reduce noise due to long integration of leakage current, while ensuring no ballistic deficit. It was essential to achieve a high signal to noise ratio to substantially reduce false detection while maintaining a jitter lower than 5 ns to achieve the desired timing performance.

### C. *Differential comparator and DAC*

The comparator is AC-coupled to the shaper output, reducing sensitivity to baseline drifts. The first stage uses a differential telescopic cascode input with cascode current mirrors to achieve a high DC gain. A $2^{nd}$ stage with a single ended common source transistor is provided to further boost the gain. A 7-bit differential binary weighted current steering trimming DAC, programmable using BitN & P <0:6> is used

to compensate for systematic offsets as shown in Fig. 5. A source follower sets the threshold at the input of the comparator, such that ThP is the DC reference for the input signal and ThN is the threshold voltage.

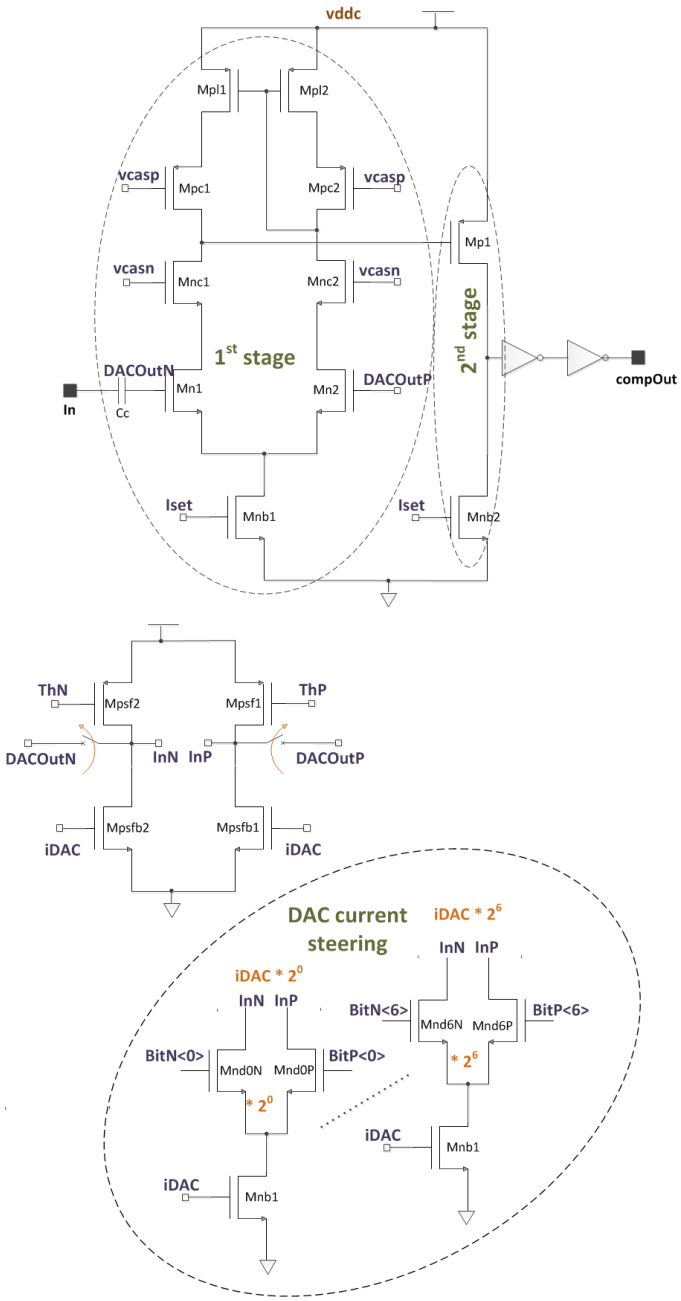


**Fig. 5 Transistor level comparator and DAC design**

### D. *Digital Backend and control*

An 11-bit configuration register is used to independently control each pixel. DAC setup utilizes 7 bits and the rest 4 bits are used to set modes of operation which include pixel disabling, analog test, trim DAC setup, digital test and normal operation.

The digital backend includes a 10-bit counter for time of arrival information. The design uses a global frame clock running at 1 MHz, this provides coarse timing information for the ROIC. A gated fast clock of 200 MHz is also distributed across the ROIC, this clock is used as the counter clock only when a pixel detects a signal. The value of the counter is subtracted from the frame clock timing to provide the time of arrival of the incoming photon. This method reduces the number of free running counters in the ROIC to only those pixels which detect a signal, and is extremely useful in a low data rate application. It is envisaged that the fast clock speed will be increased to 1 GHz for a future implementation of the ROIC.

At the end of a frame, the data of the counter is transferred to a 10-bit shift register, which is daisy chained within a column of 32 pixels. The data is subsequently transferred from the shift register using LVDS outputs per column. While the data is being transferred the counter is available to process data for the next frame.

### E. *Analog Pixel Parameters*

Key design parameters of the preamplifier, shaper and comparator are listed in Table 1.

TABLE I
KEY DESIGN AND PERFORMANCE PARAMETERS OF THE ANALOG FRONT-END

| Parameter | Value |
|---|---|
| **Preamplifier** | |
| Input transistor dimensions | W/L = 15 µm/240 nm; $g_m$ = 300 µS |
| Feedback capacitor (Cfb) | 3 fF |
| Feedback resistor (Mnf1) | W/L = 1 µm/2.5 µm; $1/g_m$ = 66.6 MΩ |
| Power consumption | 22 µW |
| Preamplifier rise time (800 $h^+$ charge) | 6 ns |
| Open loop gain | 58 dB |
| **Shaper** | |
| Input transistor dimensions | W/L = 5 µm/200 nm; $g_m$ = 54 µS |
| Capacitor C1, C2 | 151 fF, 11.58 fF |
| Power consumption | 7 µW |
| Shaping time | 30 ns |
| Noise | 55 e- rms |
| **Comparator** | |
| Capacitor Cc | 500 fF |
| Phase variation | 1 ns rms |
| Power Consumption | 7.5 µW |

## IV. SIMULATION RESULTS

The Fig. 6 shows the analog simulation results of the above blocks. A single photon produces a charge of 800 $h^+$ in the detector at 500 ns. The CSA rise time is 6 ns for majority of the charge with an output voltage of 42 mV. The shaper peaking time is 30 ns, and the corresponding output voltage is 210 mV (with a gain of 5). The delay through to the comparator was simulated to be 12 ns, and the comparator rise time is 500 ps.

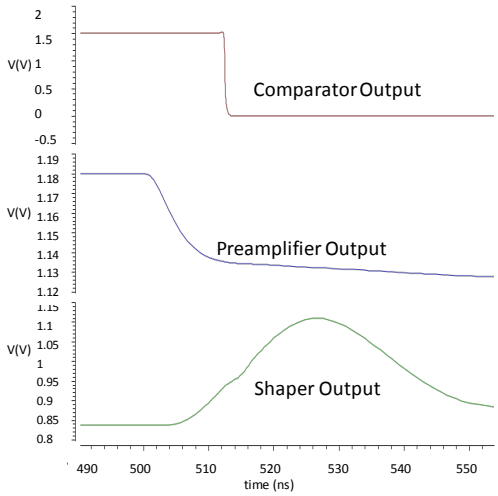


**Fig. 6 Simulation result**

Fig. 7 shows the electronics noise of 55 $e^-$ rms, achieved by a shaping amplifier with 30 ns shaping time. The corresponding jitter due to noise at the output of preamplifier was 1.06 ns rms, and was 3.54 ns rms at the output of the shaper. The signal to noise ratio (SNR) is 9.8 at the output of preamplifier, and 14.5 at the output of the shaper. At this stage the jitter in the system indicates that it is reasonable to expect an accuracy of 5 ns for time of arrival information from the comparator. This does not account for jitter due to the detector shot noise.

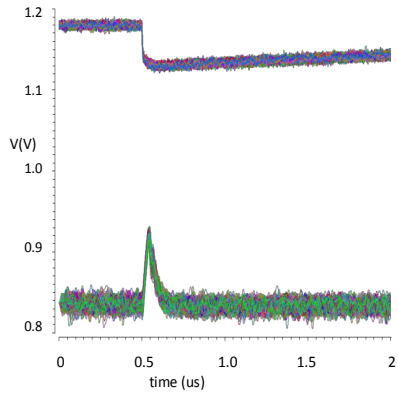


**Fig. 7 Noise simulation**

A further analysis of Monte Carlo simulations of mismatch across the pixels yield a comparator phase variation corresponding to best case and worst case values of 6.27 ns and 19.92 ns respectively. The noise associated with mismatch across pixels further adds to the noise in the system degrading the SNR.

## V. Conclusion

The first implementation of a hybrid pixel detector for quantum cryptography has been presented; Table 2 summarizes the ROIC specifications. The analysis indicates that for low probability of false detection the SNR of the system needs to be high. Increasing the rise time in the sensor and reducing the phase variation in the ROIC will be needed to accurately timestamp the sequence of the incoming photons. Detailed tests of the ROIC are yet to be performed. A future version will implement gain correction in preamplifier, faster time stamping clock (1GHz) and data sparcification. Sensor development is ongoing to increase its gain and bandwidth.

TABLE II
SPECIFICATION OF SPID ROIC

| Parameter | Value |
|---|---|
| Fabrication Process | Global Foundries 130 nm, 1.5V, CMOS LP, 1P8M |
| ASIC size | 5 mm × 5 mm |
| Sensor area | 3.2 mm × 3.2 mm |
| Number of pixels | 32 × 32 |
| Pixel size | 100 µm × 100 µm |
| Analog Power consumption | 45 µW/pixel (approx.) |
| ENC noise (with CDS) | 55 $e^-$ @ $C_{det}$ = 100 fF |
| Counter Resolution | 10-bit |
| Timestamp resolution | 5 ns |
| Full chip readout | 5 µs |
| Trimming DACs | 7-bit |
| Sparsified Readout | No |
| Dead-time less operation | Yes |

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