SUMMARY

The planned luminosity upgrade of the LHC (to HL-LHC) will require the CMS and ATLAS pixel vertex detectors to accurately track particles in the presence of a hit rate of up to 2GHz per cm^2 and withstand a TID of 1Grad over 10 years. The new FCP130 mixed signal ASIC with a Synchronous frontend is designed as a prototype front-end for an HL-LHC pixel readout system which incorporates features such as:

- Leakage current compensation up to 5nA per pixel.
- No ballistic deficit, due to the lack of a shaping amplifier.
- Increased noise immunity due to digital conversion immediately after preamplifier.
- Autozero comparators without the need for trimming DACs.
- Noise filtering based on correlated double sampling.
- Processing insensitive to pileups.
- Eliminates tuning of continuous time filtering, including constant current discharge.
- 3 bit flash ADC with data conversion within 1 BXclk.
- Priority encoder for sparsified readout.
- Low power consumption

This chip has been designed in Global Foundries (GF) 130nm CMOS process. It consists of a matrix of 48×160 pixels, each 100x30µm^2 in size; 192 pixels are grouped together to create a super column. The ASIC is 8.5 x 5.5mm^2 with a charge sensitive area of 4.8 x 4.8mm^2.

Each pixel contains a charge sensitive preamplifier with leakage current compensation, 8 auto-zero comparators and a thermometric encoder for a 3 bit Flash ADC. It also contains a hit processor and a priority encoder for data sparsification. The block diagram is shown in Figure 1.

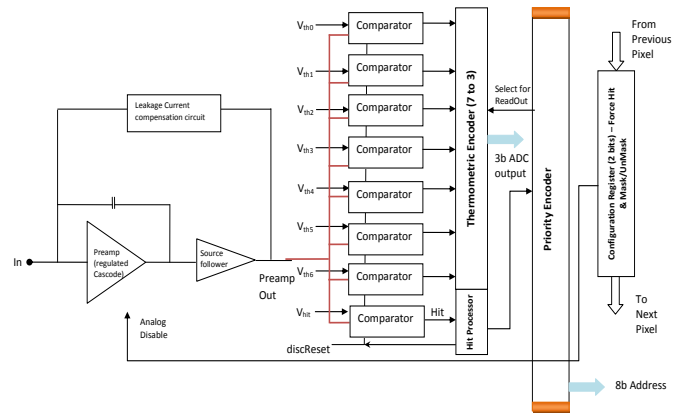

Figure 1 FCP130 Pixel Block Diagram

The preamplifier consists of a regulated cascode design with an NMOS input transistor with an 11fF feedback capacitor, an active transistor feedback with an effective resistance of $1/g_m$ and a source follower at the output. The leakage current compensation circuit consists of a differential pair with a tail current (I_{tail}) large enough to supply both the leakage current (I_{leak}) and the feedback transistor bias current (I_d). a large resistance R_{fi}, along with C_{fi} establishes the dc bias point for the differential pair as shown in Figure 2. For small signals the equivalent feedback resistance is 1/gm of transistor Mf, for large signals the transistor operating point changes and it behaves as a constant current source.

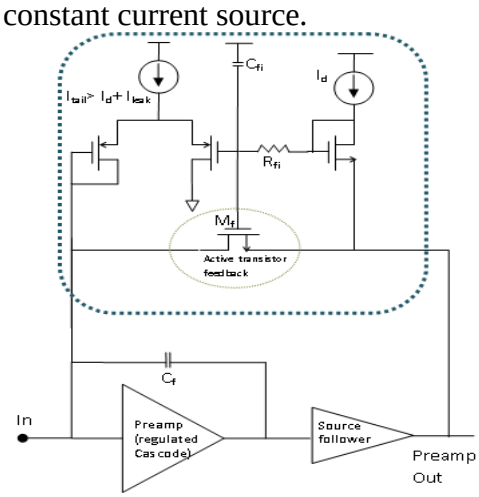

Figure 2 Preamplifier with Leakage current compensation

The unidirectional auto zero comparator is AC coupled to the output of the preamplifier. It consists of 2 single ended stages AC coupled to each other and a low V_T PMOS source follower

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to set the threshold as shown in Figure 3. The 1st stage contains a NMOS input transistor with an overload recovery for very large signals. The 2nd stage consists of a cascode amplifier with a positive feedback regeneration circuit. It uses the BXclk to define the reset and active phases of 12.5ns each. During the reset phase, offset cancellation is achieved by closing the switch across the input transistor. A clamp is used to maintain a constant current from the power supply. The comparator is inherently unstable for very low threshold voltages to achieve fast response for very small signal sizes.

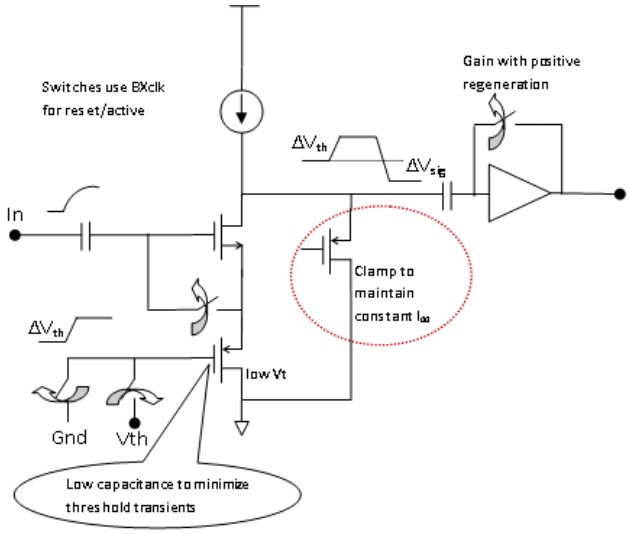

Figure 3. Auto Zero Comparator

The digital part of the pixel consists of a Hit processor, a 7:3 bit thermometric encoder for the ADC output, and a priority encoder for data sparisification. It also has the capability to mask and unmask an individual pixel. The data packet at the output of a supercolumn consists of 11 bits with an 8 bit pixel address and 3 bit ADC value. When there are no hits in a frame(25ns) the default pixel address is 5. The simulation result of a digital supercolumn is shown in Figure 4 where Frame 1 has two hits in Pixel 1 and Pixel 48 with address 16, ADC value 7 and address 63,ADC value 0 respectively. The alertReadout signal indicates valid data, Read Strobe is an external fast clock to transfer data from the super column to the ASIC periphery.

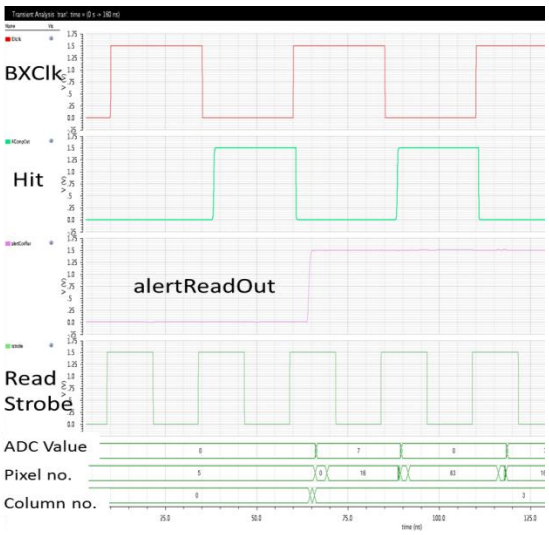

Figure 4. Digital Simulation of super column

Each supercolumn contains a data transfer block; FIFO2daisy is a set of three 5-word deep FIFOs arranged in phases such that in any given BX Clock period, one FIFO is in the Write Phase, one is in the Read Phase and one is being reset. In the Write Phase, the FIFO accepts up to 5 words from the pixel matrix. In the Read Phase, the FIFO outputs any stored words asynchronously to the periphery. At any time, the contents of all three FIFOs can be captured without interfering with normal operations. Then this captured word can be streamed out of one long daisy chain that includes all supercolumns.

The ASIC employs an asynchronous data readout scheme with implicit multiplexing and data latching utilizing a 4-phase handshake protocol. It allows for data packets to be inserted from a supercolumn into an existing stream of data flow to the output.

REFERENCES

[1] G. De Geronimo et al. / Nuclear Instruments and Methods in Physics Research A 484 (2002) 544–556

[2] HeungJun Jeon; Yong-Bin Kim; Minsu Choi; Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium on